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AN ADVANCED PLATFORM FOR DEVELOPMENT AND EVALUATION OF GRID INTERCONNECTION SYSTEMS USING HARDWARE-IN-THE-LOOP

PART III: GRID INTERCONNECTION SYSTEM EVALUATOR

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INTRODUCTION

Background

The world's energy paradigm continues to undergo a rapid shift towards an increased use of renewable energy sources. At the same time, an advanced electric power system (EPS) architecture, including increasing amounts of distributed resources, load control, bi-directional power flow, advanced metering, and improved communications is gaining attention and being implemented by many electric utilities.

In support of this shifting energy paradigm and new EPS architecture, a swiftly-increasing number of renewable energy-based distributed resource installations are occurring. As these installations occur, it is essential to ensure that these systems, each of which interface to the EPS using a grid interconnection system (ICS), are properly interconnected with the EPS according to the relevant standards, which are UL 1741 and IEEE Std 1547™ in the United States.

IEEE Std 1547 and EPS Interconnection Conformance Testing

IEEE Std 1547, which was harmonized with UL 1741, was developed to provide a standard set of requirements surrounding issues such as voltage regulation, synchronization and isolation, response to abnormal grid conditions, power quality, and islanding for interconnecting ICSs with the EPS. IEEE Std 1547.1™, *IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems*, provides a comprehensive set of test procedures for use in determining if a particular ICS meets the requirements of IEEE Std 1547. When following the step-by-step procedures in IEEE 1547.1, it becomes clear that the process of testing an ICS against IEEE Std 1547 is quite comprehensive and can become very time-consuming. Thus, there is significant potential to greatly reduce the amount of time required for running these conformance tests by automating portions of the test procedures using hardware-in-the-loop (HIL) simulation techniques.

HIL and Automated EPS Interconnection Conformance Testing

HIL simulation is a technique by which hardware systems and software models can be placed together into a single closed-loop simulation. This is accomplished by using a real-time simulator (RTS) that runs the software model and the communication interface between software and hardware deterministically and in actual time (see Figure 1).

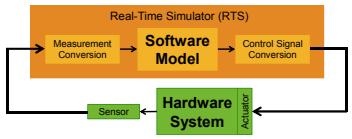

Figure 1 – Typical HIL Simulation Setup

HIL simulation allows for more rapid development of either the hardware systems or software control models. In this case, HIL simulation is used to considerably shorten the amount of time required to complete a full set of grid interconnection conformance tests by placing a software control model of each conformance test in the loop with the ICS under test and the related electrical test equipment. HIL simulation also adds additional testing capabilities, such as testing advanced functions such as voltage (VRT) and/or frequency (FRT) ride-through and volt/var control in ICS.

TEST SETUP

Figure 2 shows the Grid Interconnection System Evaluator setup for testing grid interconnection conformance of a photovoltaic (PV) inverter, though the platform is general enough that a wide variety of ICSs at a range of different power levels can be tested.

For this particular set of tests, the following electrical equipment was used:

- Grid Simulator: 62.5 kVA voltage source at 240 V_{rms} nominal
- AC Load Bank: 436 kVA @ +/- 0.37 pf with 125 W and 312.5 VAR steps
- DC Supply: 250 kW, 0-900 VDC
- Inverter: ~3 kW MPPT PV

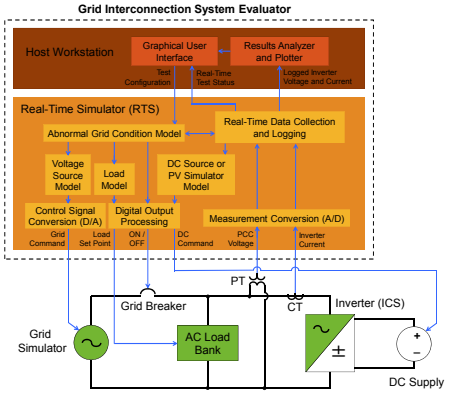

Figure 2 – Grid Interconnection System Evaluation Test Setup

GRAPHICAL USER INTERFACE

Figure 3 shows a screenshot of the graphical user interface (GUI) from which a user can configure, run, monitor, and view grid interconnection conformance tests.

Configuration takes place at the top of the screen where the user selects the desired tests, enters the relevant parameters and a comment, if desired. A graphic at right assists the user with understanding the parameters being entered as they relate to the selected test.

Once configured, the user presses "Start Test", which will verify that the entered parameters are valid and then execute the test using the RTS.

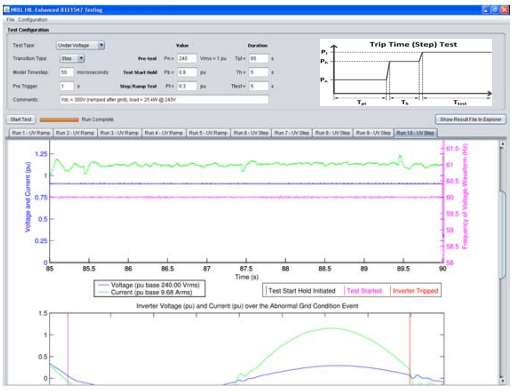

Figure 3 – Grid Interconnection System Evaluator Graphical User Interface

Upon test completion, the GUI collects the test data logged by the RTS over the entire test and sends that to the results analyzer and plotter. Once analysis is finished, a new results tab with the generated report (see Figure 4 for an example) is opened at the bottom of the screen. All results of the test are available in this PDF report.

TEST CONFIGURATION AND SEQUENCE

1. Test Configuration: using the graphical user interface (GUI) (see Figure 3) the user specifies:

- Test Type:
  - Overvoltage (OV)
  - Undervoltage (UV)
  - Over Frequency (OF)
  - Under Frequency (UF)
  - Unintentional Islanding (UI)
- Sub-Test Type (only applicable for OV, UV, OF, or UF tests):
  - Time (measures the amount of time required by the ICS to respond to an abnormal grid condition)
  - Magnitude (measures the voltage or frequency magnitude at which the ICS disconnected)
- Nominal parameter (voltage or frequency) magnitude and interval duration for the three intervals during testing:
  - Pre-test (used to allow inverter to wake-up, sync., etc.)
  - Test Start Hold (temporary period immediately before test occurs—required by IEEE Std 1547)
  - Principal Test

User connects ICS with relevant electrical equipment as shown in Figure 2.

2. Test Execution: Once the user sets the configuration parameters above, the configuration is communicated to the RTS, which then builds its model and executes the test in three intervals. User is apprised of real-time test status throughout the test via the GUI.

3. Results: Upon test completion, data collected throughout the test is passed from the RTS to the Results Analyzer and Plotter, where the result parameters are calculated and plots created. This information is then organized and displayed to user in the same GUI.

4. Repeat: as necessary.

TEST RESULTS

Figure 4 shows an example test report from an undervoltage time interconnection conformance test. There are four key sections to this report:

1. **Report Header**: shows a tabular summary of the user's specified parameters (left) and the relevant results (right) for the test. This section is useful in quickly determining whether the ICS passed this test.
2. **Top Plot**: shows RMS values of the ICS current and voltage magnitude, in addition to the frequency of the voltage waveform as a function of time, over the course of the entire test. The three test intervals (pre-test, test start hold, and principal test) are delineated by the vertical lines.
3. **Middle Plot**: shows the ICS current and voltage waveforms over the course of the entire test. This plot adds additional detail to the top plot so that one can better spot any periodic abnormalities in current output from the waveform.
4. **Bottom Plot**: shows the ICS current and voltage waveforms just before and after the inverter tripped. This plot is most useful for determining the ICS current right as it tripped.

Figure 5 shows plots from further representative tests.

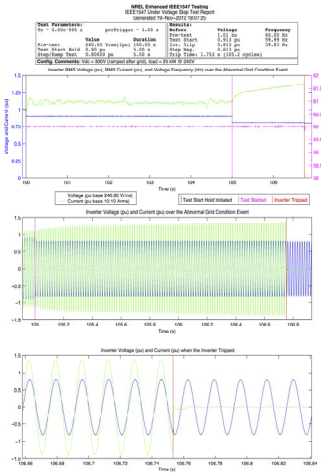

Figure 4 – An example test report for an undervoltage time test

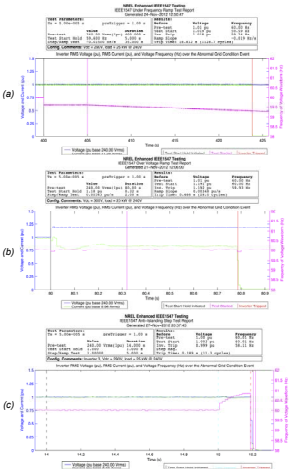

Figure 5 – Further example plots from (a) under frequency magnitude, (b) overvoltage magnitude, and (c) unintentional islanding tests

CONCLUSIONS AND FUTURE WORK

This Grid Interconnection System Evaluator provides a method to vastly increase the efficiency of conducting IEEE Std 1547 grid interconnection conformance tests through the use of HIL simulation techniques and advanced analysis scripts. However, more than just automating a test procedure, this work adds further capability to NREL's advanced platform for development and evaluation of grid interconnection systems. This platform now allows for rapid development of ICS control algorithms using controller hardware-in-the-loop techniques, the ability to test the dc input characteristics of PV-based ICS through the use of a PV simulator capable of simulating real-world dynamics using power hardware-in-the-loop (PHIL), and now the capability to evaluate the grid interconnection conformance of an ICS. This platform offers a unique set of capabilities that will help develop and evaluate the next generation of ICS that will be prevalent in future advanced EPS architectures.

Upcoming work will involve developing methods to leverage PHIL techniques to advance unintentional islanding, VRT, FRT, and volt/var control testing capabilities, and performing more realistic simulations of ICS interfaced at various local EPS.

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