NREL
NATIONAL RENEWABLE ENERGY LABORATORY

The Value Proposition for High Lifetime (p-type) and Thin Silicon Materials in Solar PV Applications

Preprint

Alan Goodrich, Michael Woodhouse,
and Peter Hacke

Presented at the 2012 IEEE Photovoltaic Specialists Conference
Austin, Texas
June 3–8, 2012

Conference Paper
NREL/CP-6A20-55477
June 2012

Contract No. DE-AC36-08GO28308

NOTICE

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information

P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/help/ordermethods.aspx

Cover Photos: (left to right) PIX 16416, PIX 17423, PIX 16560, PIX 17613, PIX 17436, PIX 17721

Printed on paper containing at least 50% wastepaper, including 10% post consumer waste.

The Value Proposition for High Lifetime (p-type) and Thin Silicon Materials in Solar PV Applications

Alan Goodrich, Michael Woodhouse, Peter Hacke

National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401 USA

***Abstract* — Most silicon PV road maps forecast a continued reduction in wafer thickness, despite rapid declines in the primary incentive for doing so – polysilicon feedstock price. Another common feature of most silicon-technology forecasts is the quest for ever-higher device performance at the lowest possible costs.**

The authors present data from device-performance and manufacturing- and system-installation cost models to quantitatively establish the incentives for manufacturers to pursue advanced (thin) wafer and (high efficiency) cell technologies, in an age of reduced feedstock prices. This analysis exhaustively considers the value proposition for high lifetime (p-type) silicon materials across the entire c-Si PV supply chain.

***Index Terms* — monocrystalline silicon, manufacturing cost, bulk lifetime, Czochralski process.**

I. Introduction

The Solar PV Manufacturing Cost Analysis group at NREL assesses the cost reduction potential of all PV technologies to inform strategic R&D decisions. This paper focuses on two important motivating features that underlie NREL's forthcoming *wafer based c-Si road map* – the value of thinner wafers, and the value of enhanced-device performance. For the purposes of this paper, the authors limit the scope of the analysis to standard wafer-based (p-type) c-Si devices.

The "standard" front-contact p-type cell considered in our device modeling runs utilized: 90 ohm per square front surface diffusion; an optical front surface coating: 3 μm deep random pyramid texture, SiN antireflection coating, a front-surface recombination velocity: 40,000 cm/s; 5% front metal shadowing losses; a full aluminum back surface field with a back-surface recombination velocity of 1,000 cm/s; and an internal reflectance of 60%.

Three pathways to higher efficiency devices are considered: high lifetime materials, enhanced back-surface passivation, and enhanced back-surface passivation with improved internal reflectance. Knowing the relative efficiency improvements of each pathway – separately, and in combination, the question then becomes: what is the available budget available to manufacturers to pursue these pathways?

Today, there appears to be evidence that industry stakeholders can pass along, at least some of the higher costs associated with higher efficiencies to the customer, in the form of a higher module price. But, what is the expected long-term price-premium for performance, assuming a mature industry with balanced competition.

II. The Value of Reduced Wafer Thickness

The cost-benefit of reducing wafer thickness must justify the potential for any added costs, as related to:

a. Higher mechanical yield losses
b. The need for non-contact printing of metals
c. Increased problems in wafer bowing
d. The need for augmented surface passivation
e. The need for low-stress tabbing in module fabrication

By thinning the wafer, one reduces polysilicon (grams per $W_{P\ DC}$) costs, and increases some machine throughputs.

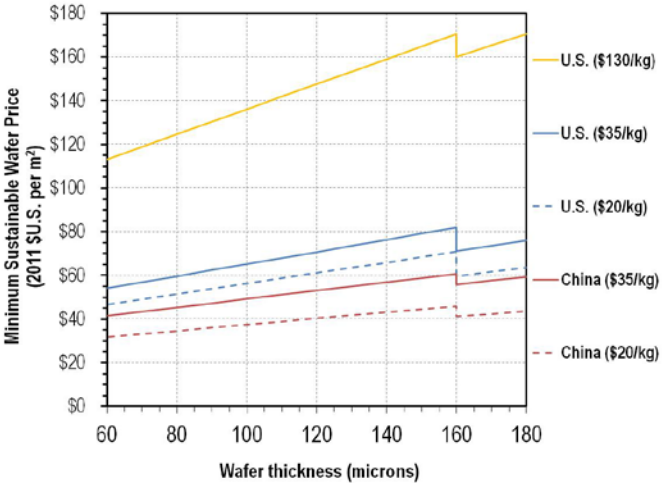

Fig. 1. Cz wafer price-thickness sensitivity; 40 million wafer per month, 130 mm kerf loss. Source: NREL-internal cost models.

Considering all of the cost benefits associated with wafer thinning, but ignoring the challenges, we estimate the savings to be far more limited today than during the 2008 polysilicon shortage.

II. Improving Bulk Lifetimes

If utilizing p-type starting materials (wafers), the dominant loss mechanism appears to be defect-mediated recombination [1], specifically due to the presence of boron-oxygen pairs [2]–[4]. Several methods exist to manage or eliminate these defects, thus enhancing the bulk lifetime of the substrate

materials. We focus on two growth processes, in particular: the Magnetic-confined Czochralski (M-Cz), and Gallium doped Czochralski (Ga Cz) growth technologies.

The first possible method, the M-Cz process, has been found to significantly lower oxygen content, while adding capital expense (~$200K/ station) for each Cz-puller [5, 6].

Alternative dopants, such as gallium greatly reduce the SRH recombination within a wafer, but add other production challenges. For example, due to a lower segregation coefficient than boron, gallium is more difficult to manage during ingot formation – potentially limiting the usable as-grown length of Cz-ingots to around 50% (in comparison to the 80% that is achievable today using boron doping). Also, at least historically, the commercial viability of using boron-dopant alternatives, such as gallium has been limited by the complexities and cost of managing multiple material streams in high volume operations. To avoid cross-contamination, silicon materials from ingot and wafer lines running boron-doped feedstock would have to be run entirely separate from gallium-doped silicon lines [7]. Perhaps until recently, production volumes did not justify the expense of running a dedicated gallium-silicon ingot and wafering line.

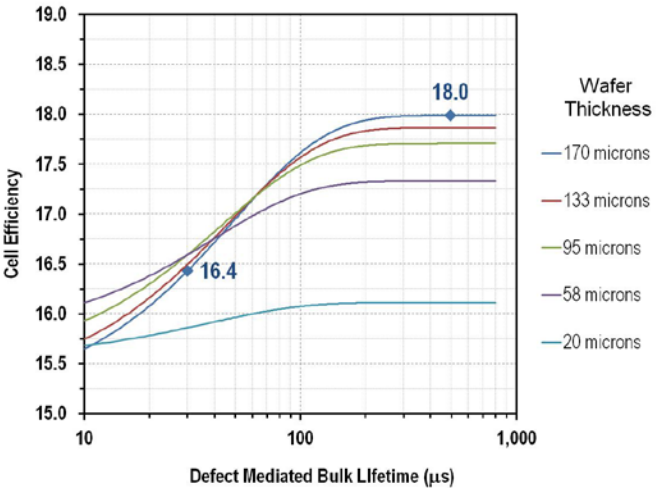

Fig. 2. Modeled performance benefits of higher bulk material lifetime in the standard c-Si cell architecture.

By increasing lifetime from 30 µs to 500 µs, the cell-efficiency is enhanced from 16.4% to 18.0%, which roughly corresponds to module efficiencies of 14.6% and 16.2%, respectively.

Our analysis indicates that the value of high lifetime p-type silicon produced via the M-Cz process is competitive with today's materials; the added cost of the magnets and energy are more than offset by the resulting gain in efficiency. High lifetime materials produced using alternative dopants, such as Gallium, however are not cost effective due to the negative impact on the Czochralski process yields.

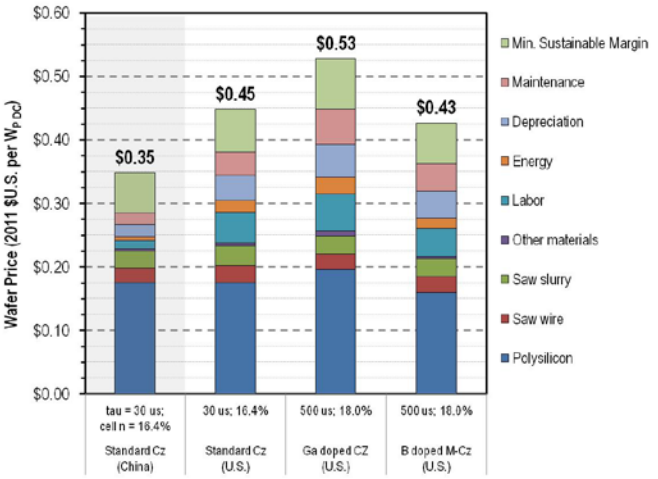

Fig. 3. Estimated Cz-wafer costs, minimum sustainable price: standard (U.S. and China) and high-lifetime (U.S.) processing routes (170 µm wafer thickness, 130 µm kerf-loss, $35/kg poly price). Source: NREL-internal cost model.

III. EHANCING SURFACE PASSIVATION, INTERNAL REFLECTANCE

Other pathways also exist to improve the efficiency of today's standard (p-type) silicon solar cell, including: enhanced surface passivation, reduced shadowing losses, and improved light management techniques.

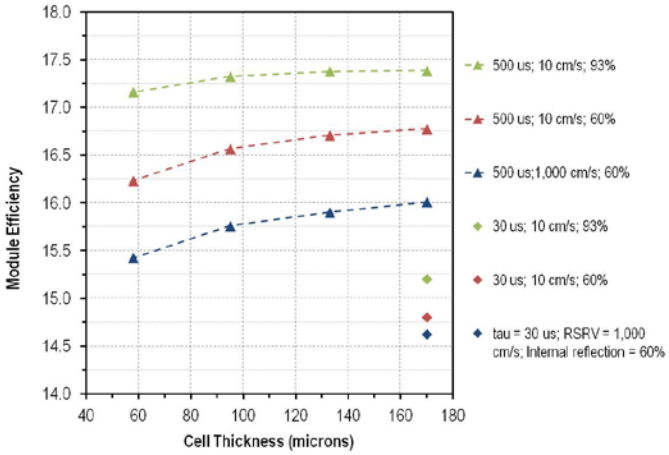

Fig. 4. The theoretical efficiency potential of enhanced back-surface passivation, internal reflectance and lifetime; standard p-type cell. Source: NREL model results.

Until SRH recombination in the bulk is reduced, however, enhancing back surface passivation does not appear to provide a significant performance benefit. In our modeling results, for a standard cell, reducing the back-surface recombination to 10 cm/s while also improving internal reflectance to 93%, as has

been demonstrated by some dielectrics and wide band gap semiconductors, increases the expected module efficiency by ~0.5% absolute. If bulk recombination is reduced through the use of a high lifetime (500 μs) wafer, then the enhanced surface passivation with improved internal reflectance is worth almost 1.5% absolute. This back-surface passivation may also enable thinner wafers by mitigating performance losses that occur as a result of reduced thickness.

III. Assessing the Value of Higher Efficiency

Module conversion efficiency impacts manufacturing and installation costs throughout the solar PV supply chain. The value proposition for high lifetime wafers is, therefore, at least partly defined by the level of cost savings provided to all industry participants – from cell manufacturers to homeowners.

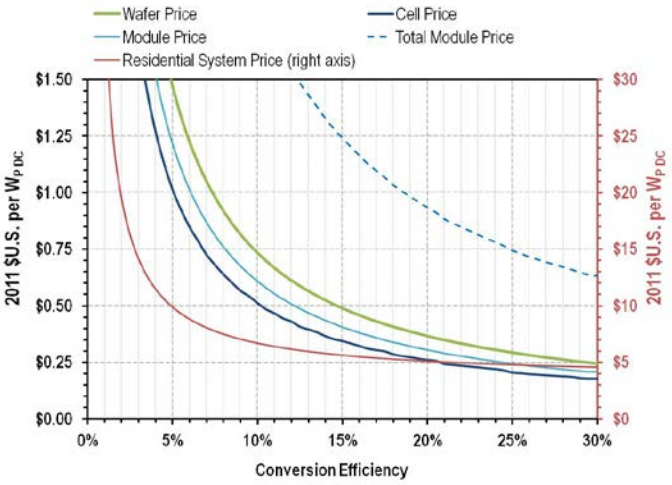

Fig. 5. The value of module efficiency. Source: NREL internal cost models, system installation cost models [8].

In considering the value of an additional 1.6% absolute points of efficiency – the expected enhancement that accompanies the use of high lifetime silicon materials, it is important to quantify the impact on costs for all stakeholders. Installers of residential rooftop systems that utilize higher efficiency modules reduce area-related costs (total system cost savings: $\$0.21/W_{P\,DC}$). It is also likely that they incur lower module shipping costs ($<\$0.01/W_{P\,DC}$ cost savings). In a mature market, where competition exists and supply-demand forces are at relative balance, the installer will likely pass along some of these benefits to the home owner in the form of a discounted system price. In this analysis, we assumed that 50% of the incremental cost benefits associated with higher efficiency is retained by the installer ($\$0.10/W_{P\,DC}$), and half ($\$0.10/W_{P\,DC}$) is used to lower the system price. In-turn, the installer retains 50% of this value-add system price ($\$0.05/W_{P\,DC}$) and passes half on to the module supplier whose high efficiency product enabled the savings.

Higher efficiencies reduce non-wafer based area-related costs for manufacturers of both modules ($\$0.03/W_{P\,DC}$) and cells ($\$0.02/W_{P\,DC}$). These cost savings are in addition to the module-price premium ($\$0.05/W_{P\,DC}$) received by the manufacturer. Half of this net-benefit or $\$0.05/W_{P\,DC}$ is passed on to the wafer supplier whose high lifetime materials enabled the higher module efficiencies. If the higher module efficiencies were realized because of advanced cell processing, then no value would be passed on to the wafer supplier.

In this analysis, any cost savings associated with these pathways are, effectively the budget available to cell manufacturers to adopt enabling technologies, and to overcome the challenges of thin wafers, etc.

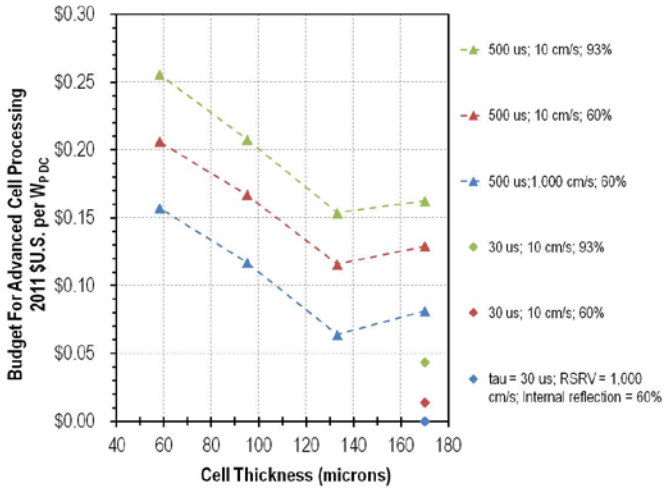

Fig. 6. The value of enhanced back-surface passivation, internal reflectance and lifetime; standard p-type cell. Source: NREL model results.

IV. Summary of Results

Assuming nothing else about the cell architecture is changed, high lifetime (500 μs) silicon materials produced via the M-Cz process can be implemented while providing a cost savings (see Figure 6) – i.e. for cells produced using high lifetime wafers, relative to standard wafers, there exists a budget ($\sim\$0.08/W_{P\,DC}$) for advanced cell processes. High lifetime materials are more valuable if rear-surface passivation is enhanced; the budget for advanced passivation technologies being approximately $\$0.13/W_{P\,DC}$. If using high lifetime 170 μm wafers, a cell manufacturer could tolerate up to $\$0.16/W_{P\,DC}$ in additional costs, in order to incorporate a back surface passivation that also enhances internal reflectance. In this advanced device, the motivation for reducing wafer thickness to between 130-170 μm is limited, due to the additional costs of reduced-diameter boules and a drop in performance.

Excluding the cost of mechanical yield losses that may occur as a result of thinner wafers, the economic motivation for reducing wafer thickness returns for thicknesses <130 mm.

V. CONCLUSIONS

Across the entire value chain, we estimate the total value of increasing module efficiency by 1.6% absolute is worth approximately $\$0.27/W_{P\ DC}$. This does not, however, represent the tolerance for additional manufacturing costs, as the value is shared among industry stakeholders. For a standard cell manufacturer, high lifetime materials produced via the Magnetic-confined Czochralski process offers a positive value proposition. Despite an increase in performance, due to the ingot yield limitations, the Gallium-doped Czochralski materials are not found to be a cost effective substitute.

When utilized in conjunction with an advanced cell concept that also minimizes back-surface recombination and offers enhanced internal reflectance, the case for high lifetime M-Cz materials is even more compelling. This advanced high lifetime cell architecture not only incentivizes the thinning of wafers, but is also more likely to be congruent with the challenges of ultra-thin cells.

ACKNOWLEDGMENT

This work was supported by the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308 with the National Renewable Energy Laboratory.

REFERENCES

[1] D. Swanson, "Approaching the 29% Limit Efficiency of Silicon Solar Cells", in *20th European Photovoltaic Solar Energy Conference Proceedings*, 6-10 June 2005, Barcelona, Spain.

[2] S. Rein, W. Warta, and S.W. Glunz, "Investigations of Carrier Lifetime in P-Type Cz-Silicon: Specific Limitations and Realistic Prediction of Cell Performance", in *Twenty Eighth IEEE PVSC*, 2000, pp. 57-60.

[3] H. Fischer and W. Pschunder, in *Proceedings of the tenth IEEE Photovoltaic Specialists Conference*, New York, 1973, p. 404

[4] J. Knobloch, S. W. Glunz, V. Henninger, W. Warta and W. Wettling: in *Proc. 13th European Photovoltaic Solar Energy Conf.*, Nice, 1995 (H. S. Stephens, Bedford, UK, 1995) p. 9

[5] S.W. Glunz et al., "Comparison of Boron- and Gallium-doped p-type Czochralski Silicon for Photovoltaic Applications", in *Prog. In Photovoltaics*: Res. Appl. 7, 1999, pp. 463-469.

[6] S.K. Chunduri, "Bigger and Better – and Retro?" in *Photon International*, June 2010, inset page 207.

[7] G. Crabtree, T.L. Jester, C. Fredric, J. Nickerson, V. Meemongkolkiat, A. Rohatgi, "Production Viability of Gallium Doped Mono-Crystalline Silicon Solar Cells", in *Thirty First IEEE PVSC*, 2005, pp. 935-938.

[8] A. Goodrich, T. James, M. Woodhosue, "Residential, Commercial, and Utility-Scale Photovoltaic (PV) System Prices in the United States: Current Drivers and Cost-Reduction Opportunities", *NREL-report* No. TP-6A20-53347, 2012.