NREL
NATIONAL RENEWABLE ENERGY LABORATORY

Kerfless Silicon Precursor Wafer Formed by Rapid Solidification

October 2009 — March 2010

Adam Lorenz
1366 Technologies, Inc.
North Lexington, Massachusetts

NREL is a national laboratory of the U.S. Department of Energy, Office of Energy Efficiency & Renewable Energy, operated by the Alliance for Sustainable Energy, LLC.

Subcontract Report
NREL/SR-5200-51934
June 2011

Contract No. DE-AC36-08GO28308

NREL
NATIONAL RENEWABLE ENERGY LABORATORY

Kerfless Silicon Precursor Wafer Formed by Rapid Solidification

October 2009 — March 2010

Adam Lorenz
1366 Technologies, Inc.
North Lexington, Massachusetts

NREL Technical Monitor: Harin S. Ullal
Prepared under Subcontract No. NEU-0-99010-01

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401
303-275-3000 • www.nrel.gov

Subcontract Report
NREL/SR-5200-51934
June 2011

Contract No. DE-AC36-08GO28308

Cover Photos: (left to right) PIX 16416, PIX 17423, PIX 16560, PIX 17613, PIX 17436, PIX 17721

Printed on paper containing at least 50% wastepaper, including 10% post consumer waste.

Project Overview

1366 Direct Wafer technology is an ultra-low-cost, kerfless method of producing crystalline silicon wafers compatible with the existing dominant silicon PV supply chain. By doubling utilization of silicon and simplifying the wafering process and equipment, Direct Wafers will support drastic reductions in wafer cost and enable module manufacturing costs < $1/W. This Pre-Incubator subcontract enabled us to accelerate the critical advances necessary to commercialize the technology by 2012. Starting from a promising concept that was initially demonstrated using a model material, we built custom equipment necessary to validate the process in silicon, then developed sufficient understanding of the underlying physics to successfully fabricate wafers meeting target specifications. These wafers, 50 mm x 50 mm x 200 μm thick, were used to make prototype solar cells via standard industrial processes as the project final deliverable. The demonstrated 10% efficiency is already impressive when compared to most thin films, but still offers considerable room for improvement when compared to typical crystalline silicon solar cells. Close examination of the data presented in his report will make the reader confident that the Direct Wafer program is capable of significantly higher efficiencies that were demonstrated in this initial stage and 1366 is confident that the Direct Wafer process will exceed the standard multi crystalline efficiency once it is fully optimized. Recognizing the urgency of getting to market quickly, this first prototype demonstration of Direct Wafers was completed within a very aggressive timeline (< 4 months). The remarkable progress during this initial phase of technology development inspires the next phase of simultaneously scaling to larger wafer area and implementing plans to improve electrical performance. Matching or exceeding the performance of standard multicrystalline wafers at less than half the cost will have tremendous near-term impact on cost-competitiveness of photovoltaics.

Hardware Baseline

Experiments using molten tin on a hot plate provided an easily-accessible model system, which was very useful for initial Direct Wafer concept verification and understanding the 1st order effects of different process parameters. We built and tested three different methods for extracting wafers from the molten metal, all of which were successful to varying degrees. We selected the most promising hardware arrangement for production of wafers for our Hardware Baseline Deliverable.

Figure 1 shows two tin Direct Wafers.

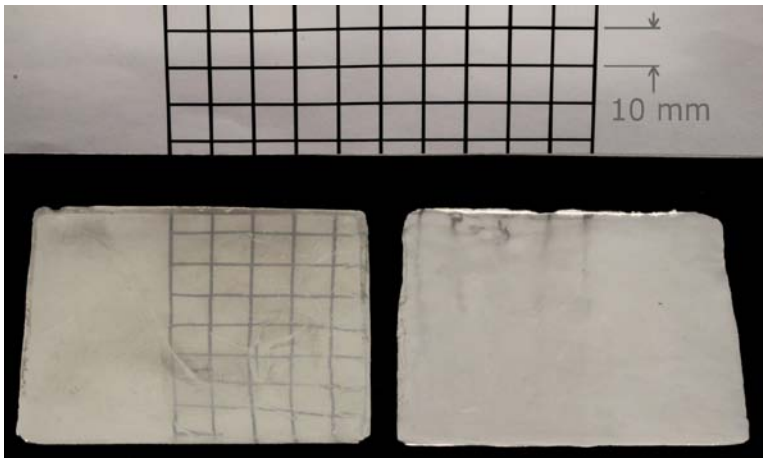

Figure 1. Tin Direct Wafers. Left, surface on one side has mirror-like finish with excellent flatness, evidenced by reflection of grid. Right, Opposite surface is smooth, but not as flat. Credit: 1366 Technologies.

Thickness control of Direct Wafers is possible through control of temperatures, heat transfer conditions, and residence time. We have produced tin wafers ranging in average thickness from nearly 1 mm to slightly less than 100 µm. Thickness uniformity becomes more challenging as wafer thickness decreases, since a fixed variability becomes a larger percentage of total thickness. Measurements on the wafers delivered to NREL were 192 ± 26 µm (13%), 167 ± 26 µm (16%), and 150 ± 34 µm (23%). Surfaces are generally smooth and flat, with substrate side measuring Ra = 0.2 µm.

Figure 2: Thickness measurement. Credit: 1366 Technologies.

Silicon Furnace Build

The prototype Direct Wafer furnace for silicon was a clean sheet design, with well over 100 custom parts fabricated at machine shops and refractory material suppliers. The 15kW furnace has a water-cooled shell and resistive heating elements, with a controlled-atmosphere, high-purity hot zone and means for wafer extraction. Motion actuators and various pneumatics are controlled via PLC with an internally-developed custom software PC interface.

First silicon melt upon commissioning the furnace went very smoothly. Our team's extensive experience designing and building high temperature furnaces made this possible in very short time. Once components were assembled, startup consisted of testing motion, monitoring furnace oxygen levels under various purge gas flow conditions, applying sufficient power for heating, then measuring steady state power levels and calibrating melt temperatures from the freezing point of silicon.

The silicon feedstock currently is fluidized bed pellets, which are useful for the small volumes of our first prototype. Our intent is for larger future systems to accept standard chunk silicon from Siemens rod growth, potentially with modest downsizing of chunks for improved flowability.

Silicon Wafers

Formation of silicon wafers was achieved shortly after the furnace was commissioned, without any major problems. An example of initial wafers produced is shown in Figure 3, with surface roughness data shown in Figure 4.

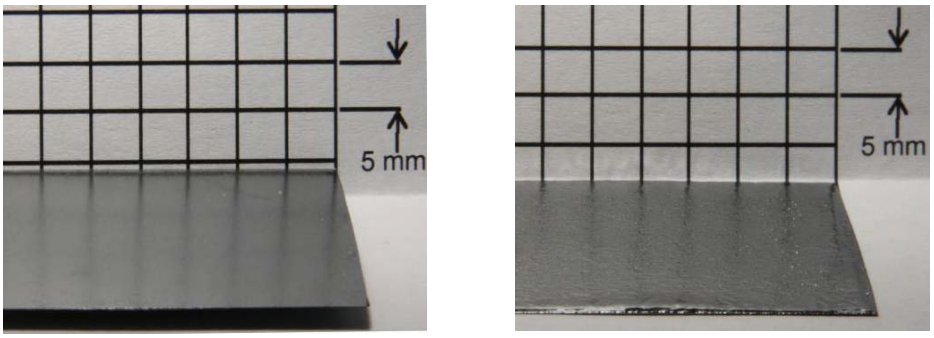

Figure 3. Surface quality on two sides of a silicon Direct Wafer. Credit: 1366 Technologies.

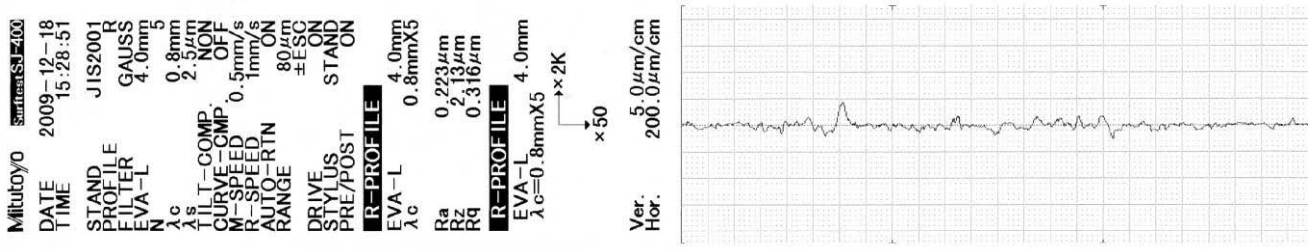

Figure 4: Profilometer data of surface roughness on smooth wafer surface. Credit: 1366 Technologies.

Thickness Control

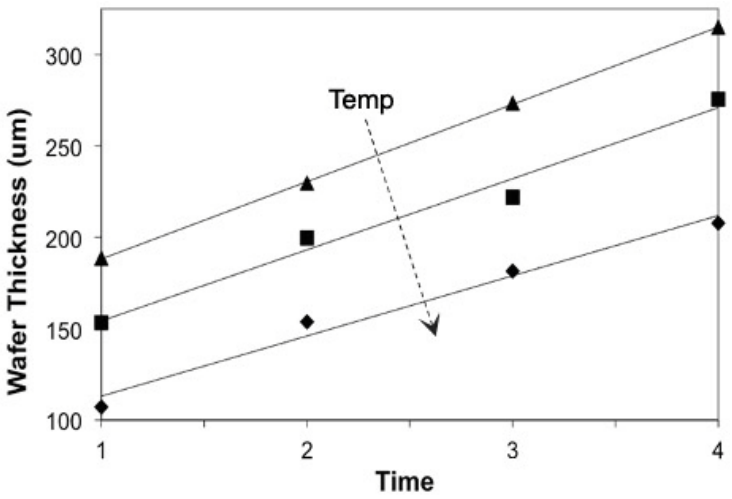

Figure 5. Measured thicknesses of silicon wafers as a function of process parameters of temperature and time.

Achieving the desired ~200 µm thickness for a solar cell required developing a good understanding of the heat transfer conditions during solidification (with significantly different temperatures and latent heat compared to the initial baseline experiments using tin). Figure 5 shows the range of thicknesses produced by varying two key process parameters. We have been able to demonstrate our target thickness is comfortably within our processing window. Measurements on the wafers delivered to NREL (Figure 6) were 184 ± 36 µm (20%), 215 ± 36 µm (17%), and 286 ± 33 µm (11%). Surfaces are generally smooth and flat, with substrate side measuring Ra = 0.2 µm. Thickness standard deviation of 30–40 µm is sufficient for pilot processing into cells and evaluation of electrical performance, but eventual customers will expect tighter specifications. We have established a third process parameter which will enable us to improve uniformity over the entire wafer, and will be exploring this further on our recently-increased-area wafer format.

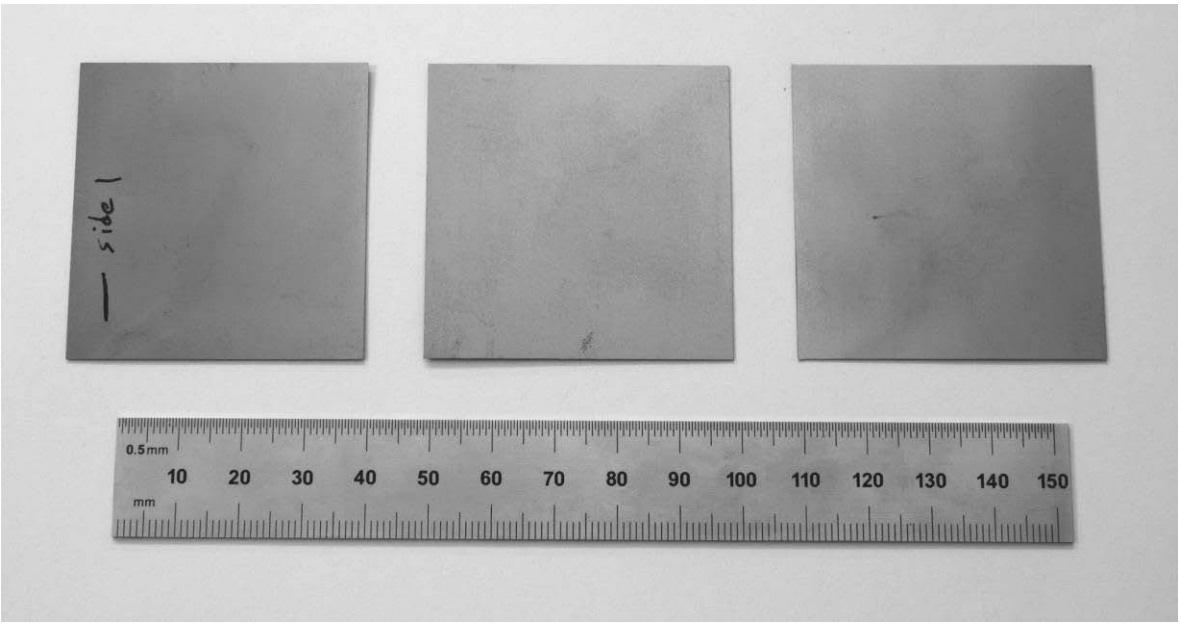

Figure 6. Silicon Direct Wafers submitted to NREL for Deliverable 2 with flat, smooth surfaces, average thickness ~200 µm with deviation < 20%. Credit: 1366 Technologies.

Cell Fabrication

1366 utilized equipment from our pilot cell processing line for testing the electrical performance of our Direct Wafers. The sequence below was used and is representative of industry standard practice.

1. Acid etch / Pre-clean
2. POCL diffusion and glass removal etch
3. SiN front AR coating
4. Screen printed metallization (Al full area back, Ag front gridlines)
5. Belt furnace firing
6. Laser junction isolation

In an optimized production line with the acid etch providing light-trapping texture, and selection of metal pastes, grid design and firing conditions to achieve good BSF, low series resistance and minimal shading, this process sequence normally results in a cell efficiency of 15–16% on multicrystalline wafers or ~17% on monocrystalline wafers. Our efficiency results on multi and mono controls were ~2% absolute lower than typical values. This was expected due largely to smooth front surfaces that reflect more light and a small cell area with higher than typical grid shading. Cell results from this process are the best metric for evaluating wafer electrical quality.

We processed several batches of Direct Wafers with experimental matrices of variable process parameters to determine their influence on resulting electrical performance. For each cell processing batch, which included from 20 to 60 Direct Wafers, a handful of ingot-cast multicrystalline and monocrystalline wafers were processed in parallel as controls to ensure consistent cell processing and provide benchmarks. Examples of the finished cells are shown in Figure 7 and IV results measured at 1366 are shown in Table 1 below.

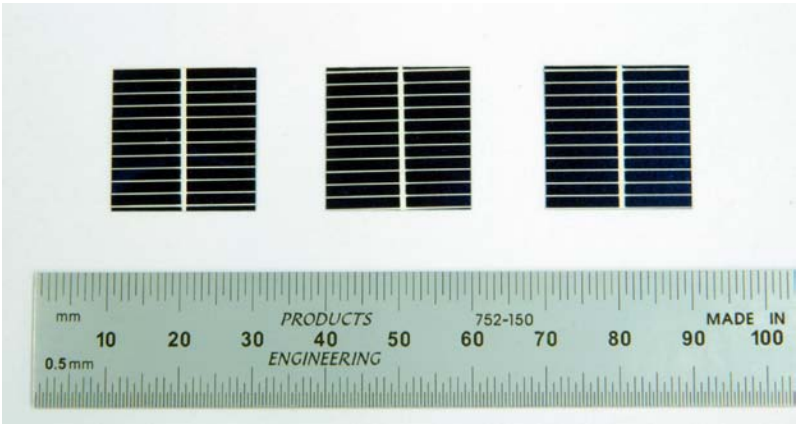

Figure 7. Three solar cells fabricated on Direct Wafers, 4 cm^2 each. Credit: 1366 Technologies.

Table 1: Solar cell IV test results

	Individual Cell Results for Direct Wafer Deliverables			Average of top 6 wafers within cell batch by type		
Solar Cell ID	DW-37-36	DW-37-47	DW-37-49	Direct Wafers	Multi Controls	Mono Controls
Voc	0.544	0.549	0.550	0.551	0.596	0.603
Jsc (mA/cm^2)	24.3	25.0	25.0	25.0	29.2	29.9
Fill Factor	77.0	75.6	76.7	75.6	78.3	79.3
Rshunt (kΩcm^2)	8.6	11.0	4.6	4.9	10.3	10.1
Rseries (Ωcm^2)	1.60	1.83	1.61	1.77	1.33	1.26
Area (cm^2)	4	4	4	4	4	4
Efficiency	**10.2%**	**10.4%**	**10.6%**	**10.4%**	**13.6%**	**14.3%**

These solar cells were submitted to NREL as the final subcontract deliverable and measured in their certified characterization lab. Discrepancies between the measurements were consistent for all three cells. 1366 measurements were ~2% lower V_{oc} and ~5% higher I_{sc}, with fill factors within 1% (all percentages relative). Variation in measured V_{oc} is likely due to lack of accurate temperature control in our solar simulator. Variation in measured I_{sc} could be related to spectral variations in our lamp compared to the true solar spectrum, which may be exaggerated due to poor IR response of our cells. 1366 intends to have a new solar cell fabricated on a Direct Wafer be calibrated by NREL and returned to 1366 for more accurate measurements in the future. Champion cell results verified by NREL are shown in Figure 8.

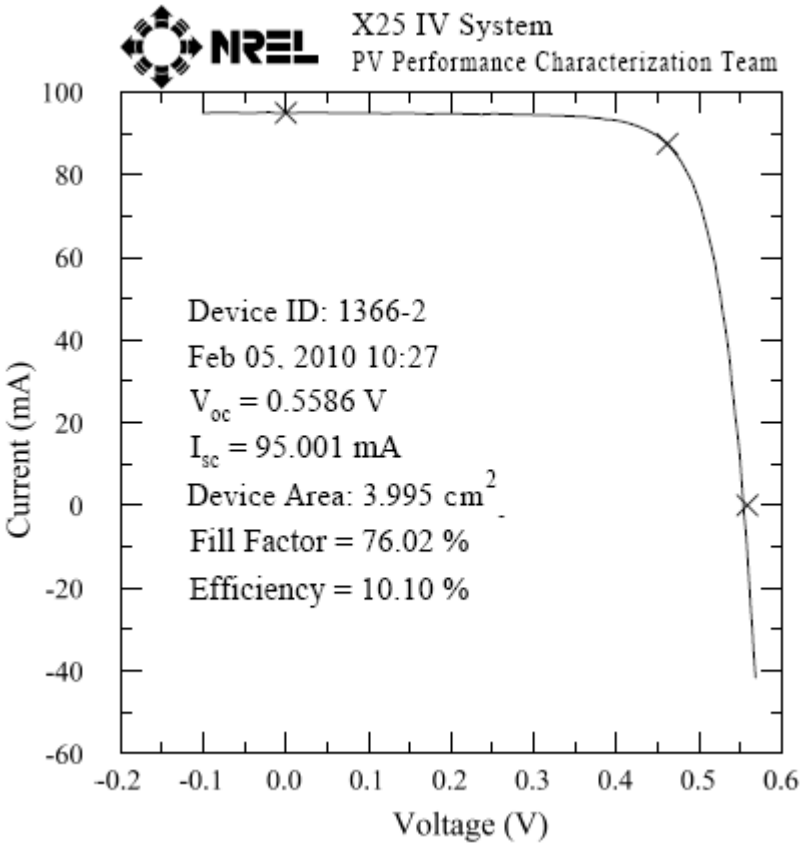

Figure 8. NREL measurement data for solar cell DW37-49.

Material Purity

Trace metals analysis of 30 elements was conducted by bulk acid digestion ICPMS to identify potential sources of contamination. Purity was significantly better than the target of 500 ppbw set for the pre-incubator contract, with the majority of elements below the detection limit of 1 ppbw and a few elements in the low single digit ppbw (Fe, Cu, Al) for totals < 20 ppbw. The purity results were nearly identical in wafers fabricated with the use of two different crucible materials for containing the molten silicon (graphite and quartz). Carbon content was analyzed by the LECO combustion technique, with a detection limit of 10 ppmw, and revealed levels similar to ingot-cast multi wafers, but slightly higher than Cz controls. Oxygen content was analyzed by inert gas fusion technique, with levels in Direct Wafers™ and multicrystalline controls below the detection limit of 10 ppmw, and a Cz control measuring 30 ppmw. The presence of these non-metallics will play a role in cell efficiency and can be characterized further by FTIR to evaluate amounts that are electrically active, but at first pass they are likely not the dominant material defect.

Grain Size, Dislocation Density, and Lifetime

Sopori etch was used to reveal grain structure and dislocation density in Direct Wafers. Typical grain size (representative of the 10% efficient solar cells) was only ~0.1mm. Dislocation density

is fairly uniform and generally below $10^5/cm^2$ with some interior grains completely dislocation free. This is an encouraging sign reflective of the low thermal stresses inherent to the process. Lifetime measurements using a Sinton QSSPC tool were not able to provide any meaningful results on starting material due to trapping defects dominating at the low injection levels inherent to the measurement. After processing of wafers and enhancement by phosphorous gettering and hydrogen passivation, trapping was decreased substantially and lifetimes of 1–3 μs were measured on ~2 Ωcm p-type material. Photoluminescence imaging was also used to determine spatial variation and uniformity appears quite good over a given sample, without any evidence of the dark, dislocation-tangle regions that are a trademark of multicrystalline wafers.

Cross sections of wafers revealed most grains to run perpendicular to the wafer surface, which is desirable to minimize their impact on current collection, but increasing grain size to be larger than the wafer thickness, and preferably >1 mm is viewed to be the biggest opportunity for improvement in electrical performance. Several ideas for controlling nucleation and growth of grains during the wafer fabrication process will be tested as part of a subsequent ARPA-E contract starting March 1st, 2010.

Texturing

The surface quality on Direct Wafers is slightly different on the two sides, with one side capable of being exceptionally smooth (Ra = 0.2 μm). For the majority of cell processing described above, the smooth side was used for the solar cell emitter for ease in screen-printing of gridlines, although both sides have been used successfully. The addition of texture to this surface is desirable for better light capture and improved efficiency, but standard isotexture etching chemistry relies on saw damage for initiation and therefore does not work well on our smooth surface. Currently under development at 1366 under a separate NREL Incubator program, we have an alternative to the isotexture method that provides better light capture without reliance on inconsistent saw damage. This 1366 Texture method works well on smooth surfaces and was tested on Direct Wafers to confirm it would be an appropriate solution for improving light capture. As expected, reflectance and spectral response measurements confirmed that a boost of ~10% relative in short circuit current should be easily attainable by applying this texture method.

Commercialization of Direct Wafer

Achieving our final deliverable less than 4 months after the subcontract start date was made possible by accelerated resource allocation including 6 dedicated engineers plus portions of other staff as needed, and leveraging cell-making expertise and equipment from other aspects of our business. By allocated the extra resources to enable the accelerated schedule 1366 significantly exceeded the contractual required match for this program. To capitalize on the tremendous potential of this one-step wafer-making process, 1366 is further doubling our resource allocation, in part supported by ARPA-E. Near term goals are to further scale wafer area from the current 50 mm to the 156 mm industry standard, and to implement methods of improving electrical quality. Demonstration of performance that can compete with today's multicrystalline wafers is the next critical step, upon which a commercial scale-up to 50–100 MW will rapidly follow. Close examination of the data presented in his report will make the reader confident that the Direct Wafer program is capable of significantly higher efficiencies that were demonstrated in this initial stage and 1366 is confident that the Direct Wafer process will exceed the standard

multi crystalline efficiency once it is fully optimized. Long term capital requirements are estimated to be ~1/10th that of traditional wafering, which will enable very rapid scaling. Low cost, high performance Direct Wafers will be established as the silicon wafer standard of the future upon which grid-parity photovoltaics will be based.

Summary

Under this subcontract, 1366 Technologies successfully demonstrated a new method of making kerfless silicon wafers. Custom equipment was designed, built and tested, then initial process conditions were established to produce small sample wafers with encouraging characteristics. Specifically, 50mm silicon wafers were fabricated with ~200µm average thickness and <40µm deviation. Material purity measured by ICPMS revealed <20ppbw total metals, and dislocation density was below $10^5/cm^2$ reflecting low thermal stresses inherent to the process. Grain size is initially quite small, ~0.1mm, which is likely the dominant property that currently limits measured lifetimes to 1–3 µs as measured on ~2 Ωcm p-type material. Spatial uniformity measured by photoluminescence is very good, and resulting initial solar cells produced with very basic industrial process steps achieved efficiencies within 4% absolute of monocrystalline controls. Future efforts will focus on increasing grain size and scaling to fabricate large wafers. Several aspects of the technology suggest it will be capable of significantly higher efficiencies and matching or exceeding the performance of standard multicrystalline wafers at less than half the cost.