NREL
NATIONAL RENEWABLE ENERGY LABORATORY

Comparison of Minority Carrier Lifetime Measurements in Superstrate and Substrate CdTe PV Devices

Preprint

T. A. Gessert, R. G. Dhere, J. N. Duenow,
D. Kuciauskas, A. Kanevce, and J. D. Bergeson

Presented at the 37th IEEE Photovoltaic Specialists Conference (PVSC 37)
Seattle, Washington
June 19-24, 2011

Conference Paper
NREL/CP-5200-50747
July 2011

Contract No. DE-AC36-08GO28308

NOTICE

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information

P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/help/ordermethods.aspx

Cover Photos: (left to right) PIX 16416, PIX 17423, PIX 16560, PIX 17613, PIX 17436, PIX 17721

Printed on paper containing at least 50% wastepaper, including 10% post consumer waste.

COMPARISON OF MINORITY CARRIER LIFETIME MEASUREMENTS IN SUPERSTRATE AND SUBSTRATE CdTe PV DEVICES

T.A. Gessert, R.G. Dhere, J.N. Duenow, D. Kuciauskas, A. Kanevce, and J.D. Bergeson
National Renewable Energy Laboratory, Golden, CO, USA

ABSTRACT

We discuss typical and alternative procedures to analyze time-resolved photoluminescence (TRPL) measurements of minority carrier lifetime (MCL) with the hope of enhancing our understanding of how this technique may be used to better analyze CdTe photovoltaic (PV) device functionality. Historically, TRPL measurements of the fast recombination rate (t_1) have provided insightful correlation with broad device functionality. However, we have more recently found that t_1 does not correlate as well with smaller changes in device performance, nor does it correlate well with performance differences observed between superstrate and substrate CdTe PV devices. This study presents TRPL data for both superstrate and substrate CdTe devices where both t_1 and the slower TRPL decay (t_2) are analyzed. The study shows that changes in performance expected from small changes in device processing may correlate better with t_2. Numerical modeling further suggests that, for devices that are expected to have similar drift field in the depletion region, effects of changes in bulk MCL and interface recombination should be more pronounced in t_2. Although this technique may provide future guidance to improving CdS/CdTe device performance, it is often difficult to extract statistically precise values for t_2, and therefore t_2 data may demonstrate significant scatter when correlated with performance parameters.

INTRODUCTION

It is now well established that CdS/CdTe thin-film photovoltaic (PV) devices configured in the superstrate design (i.e., light entering the device through a glass "superstrate") represents a commercially viable thin-film PV product. This success has prompted many to consider if further production and/or performance advantages may be acquired if the CdS/CdTe device were fabricated using a substrate architecture. Although various CdTe PV substrate products are easy to envisage, it is not yet clear to what extent present understanding of superstrate device functionality and/or junction formation can be transferred to a substrate design. Indeed, while recent studies at NREL have indicated that some of the experience gained with superstrate devices is applicable to substrate devices, there remain some aspects of junction formation that may be very different. One particularly important example is the extent to which minority carrier lifetime (MCL) measurements can be used to explain differences in substrate device performance, and/or to what extent comparisons can be made between MCL indications on substrate and substrate devices.

To-date studies of CdS/CdTe superstrate devices have established the following insight related to junction formation: Cu diffusion from a Cu-containing contact interface layer (CIFL) increases the net acceptor concentration in the CdTe layer (N_a-N_d), thereby reducing the depletion width (W_D) of the junction. Optimum photovoltaic performance is attained when W_D is narrow enough to produce a drift field in the CdTe absorber that is sufficiently strong to overcome the relatively poor lifetime of the minority carriers (i.e., t_n, electrons in CdTe), but still wide enough to limit effects of voltage-dependent collection (i.e., photocarriers should be generated primarily within, or very near to, the depletion region when the device is biased near the maximum power point [MPP]) [1]. Cu diffusion from the contact can also increase t_n in the CdTe, if the diffusion is performed at a temperature of 250°-320°C [2]. Therefore, an "optimum contact" is produced by "optimum Cu diffusion" that results in a W_D of ~0.5 µm when the device is biased near the MPP, and a t_n in the space-charge region of ~≥0.5-1 ns. Additional Cu incorporation from the contact beyond its optimum concentration causes N_a-N_d to increase further. Although this can produce lower values of reverse saturation current (J_o), and can potentially increase open-circuit voltage (V_{oc}), this high level of Cu incorporation has been found to reduce t_n. Furthermore, excessive Cu diffusion can lead to Cu incorporation into CdS. This will reduce the net donor density (N_d-N_a) in the CdS, reduce W_D in the CdTe, and yield a manifestation of photoconductivity, as confirmed by red light bias quantum efficiency measurements. These complications of excess Cu diffusion combine to limit the benefits of a lower J_o, often reducing both V_{oc} and fill factor of the device. Similar (but longer-term) redistribution of Cu into the CdS layer also has been linked to certain types of device instability [3].

In the above description of CdTe device functionality, MCL values for superstrate devices have been determined primarily through time-resolved photoluminescence (TRPL) measurements. In this technique, a short pulse of 635-nm laser light is directed through the glass superstrate, TCO, buffer, and CdS layers, and then absorbed in the intermixed CdSTe and CdTe layers. The radiative recombination of photogenerated carriers within (or very near) the space-charge region leads to a decaying luminescent peak centered near ~840-850 nm at room temperature. Although reports indicate that the luminescent decay from CdTe devices is often fit with a bi-

exponential function, most reports correlate device performance only to the lifetime associated with the fast decaying component of the luminescence (t_1). In this report we consider the rationale for this method, and explore further if correlating the slower decay observed in TRPL (t_2) with device performance may be warranted.

EXPERIMENTAL

Superstrate CdS/CdTe materials used in this study were produced at NREL and incorporated Corning 7059 glass, SnO_2:F/SnO_2 produced by chemical vapor deposition ($CBrF_3$ + $Sn(CH_3)_4$ + O_2), CdS deposited by solution growth, CdTe deposited by close-space sublimation (CSS) at 630°C, and a vapor $CdCl_2$ process. The ZnTe:Cu/Ti contact was produced as follows: Samples were placed into a multisource vacuum processing chamber and preheated for 120 min to contact-deposition temperature of 340°C. Prior to ZnTe:Cu deposition, approximately 100 nm of material was removed using ion-beam milling with a 3-cm Kaufman-type ion gun, operating at a beam energy and current of 500 eV and 6 mA, respectively, using UHP-grade Ar. ZnTe:Cu layers (4 wt.% Cu) were deposited by r.f. sputtering to a thickness of 0.35 µm. The sample heater was turned off following ZnTe:Cu deposition and allowed to cool to an indicated temperature of ~185°C, at which time 0.5 µm of Ti was deposited using d.c. magnetron sputtering. Following contact formation, a pattern of individual 0.25-cm^2 cells was defined photolithographically on each sample. Cell definition was by two-step chemical etching, using first TFT Ti Etchant (Transene Co. Inc., Rowley, MA) to remove the Ti, followed by an aqueous solution of 39% $FeCl_3$ to remove the ZnTe:Cu and CdTe. A perimeter contact onto the SnO_2 layer was formed with soldered In.

Substrate CdTe devices had the structure glass/Mo/CIFL/CdTe/CdS/ZnO/ZnO:Al on which a Ni-Al Grid was evaporated using a shadow mask. Specific parameters of these substrate devices include the following: Substrate: Corning 7059 or 1737 glass coated with 80 nm of d.c.-sputtered Mo; CIFL: ZnTe:Cu (0.3 to 4 wt.% metallic Cu in ZnTe) sputtered using the same sputtering system as noted above for superstrate devices, but deposited at either room temperature or ~360°C, or sputtered Cu_xTe deposited at room temperature; CdTe deposited by CSS at a temperature of 450-620°C; and CdS deposited by chemical bath deposition or sputtered CdS:O. Either one or two vapor $CdCl_2$ processes were used (400°C, 5 min, 20% O_2 ambient). If one process was used, it was performed after the CdTe deposition. For two $CdCl_2$ processes, the first was performed after CdTe and the second after CdS deposition. The ZnO/ZnO:Al bi-layer was deposited by r.f. sputtering whereas the Al grid was deposited by E-beam evaporation. The transparent conducting oxide and grid deposition procedures are the same as those used at NREL for CIGS device fabrication.

Electrical analysis included light and dark current-voltage (LIV/DIV) measurements at room temperature using an XT-10 solar simulator adjusted to approximate Global AM1.5 current from an NREL-measured CdS/CdTe reference cell. TRPL measurements were performed using 635-nm laser light (250 kHz rep rate) through the glass superstrate and using time-correlated-single-photon-counting (TCSPC) to analyze the decaying luminescent peak at ~820-850 nm at room temperature.

RESULTS

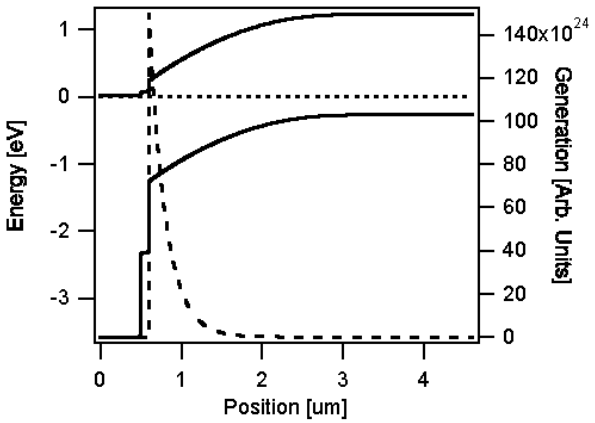

Figure 1. Schematic illustration of the depth-dependant generation associated with the 635-nm excitation in relation to the field strength in the junction region at equilibrium using parameters shown in Table I. Solid lines are conduction and valance bands, dotted line is Fermi level, and dashed line is electron/hole generation.

Figure 1 shows modeled results of carrier generation from 635-nm light relative to both the modeled extent of the CdTe layer (including the CdSTe layer) and the carrier concentration shown in Table I. Because the 635-nm laser light generates photo-excited carriers almost entirely within W_D, luminescence will be suppressed because the junction field will assist carrier separation, thus limiting luminescent recombination. Therefore, in this region, the luminescence is assumed to be dominated by the drift field rather than MCL of the bulk CdTe.

Figure 2 shows typical TRPL data from a CdTe substrate device. The luminescent decay data have been fit with a bi-exponential equation in which initial rapid decay (t_1) is ascribed to the drift-influenced luminescence in W_D described previously. Although the longer-term decay (t_2) typically results from the fitting, the majority of the TRPL signal (typically >90%) is typically accounted for with a single-exponential fit. Therefore, the parameter t_2 from the TRPL embodies higher uncertainty than the value of t_1.

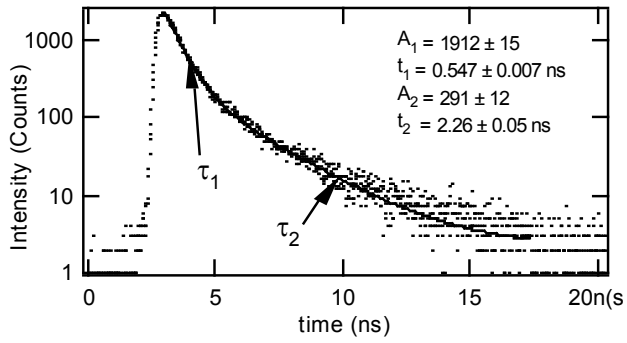

Figure 2. Representative TRPL data for a CdS/CdTe substrate device indicating luminescent PL decay in the drift-dominated region of the device (t_1) and the region believed to be more dominated by bulk and interface recombination (t_2).

As noted in Figure 1, carrier generation is believed to occur primarily within W_D. Further, because t_1 is believed to depend strongly on the strength of the drift field in W_D, correlation of performance and t_1 is generally expected [2,4]. However, more recent studies have suggested t_1 does not correlate well with small changes in device performance. This is unfortunate because improvements of MCL in both W_D and the quasi-neutral region of the CdTe PV device are believed to be one of the more promising routes to enhancing module performance. Similarly, we have also found that the higher V_{oc} observed in some substrate CdTe devices also does not correlate well with higher t_1 (compared to lower-V_{oc} superstrate devices). Both of these results suggest that relying only on luminescence from drift-dominated region of the CdTe junction (i.e., t_1) may not provide the analysis parameter needed for new device research strategies.

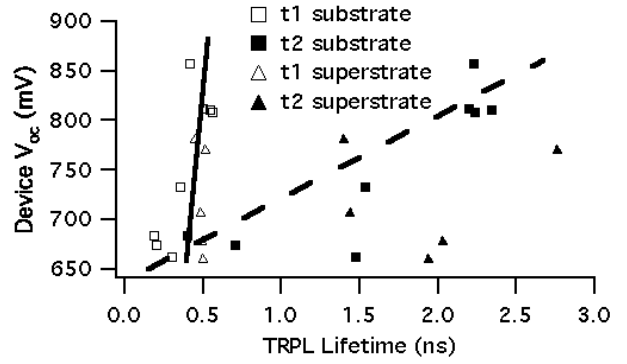

Figure 3. Plot of V_{oc} as a function of t_1 and t_2 MCL that was measured using TRPL. Solid line suggests correlation of t_1 for substrate and superstrate devices, dashed line suggests correlation of t_2 with substrate devices only.

The solid line in Figure 3 suggests a correlation trend of device V_{oc} with t_1 for both superstrate and substrate devices produced in this study. The trend shows, at least for this set of substrate and superstrate devices, that t_1 changes relatively little (~0.25 ns to ~0.5 ns), whereas V_{oc} changes significantly from ~650 mV to more than 850 mV. In contrast, and as discussed previously, although the scatter in the t_2 is relatively large, a correlation with V_{oc} is present, especially for the substrate devices (dashed line in Figure 3).

To explore the effects of parameters that likely impact the rate of luminescent decay, numerical modeling was performed using the software Sentaurus Device [6]. The model assumed an electrical junction between CdS-like layer and a CdTe-like layer with the parameters indicated in Table I. In this model, it is assumed that the SnO_2 layer demonstrates high resistivity, thereby representing functionality consistency with a high-resistance "buffer layer." The parameters varied in the simulation were electric field strength in W_D (by varying the net acceptor density in the CdTe region), the interface recombination velocity (S) at the CdS/CdTe interface, and the bulk MCL (t_n). A similar modeling study exploring related parameters is presented in Ref. 7. In general, this initial modeling study showed that changes in N_A affected both t_1 and t_2. In contrast, variations in MCL and S more strongly affected t_2. These indications suggest the following: A) Studies of recombination in and near the CdTe junction may require analysis of both t_1 and t_2; B) t_2 may be more sensitive to small changes in S and MCL. Figure 4 shows the effect on simulated luminescent decay for MCL of 1 ns and S of 10^5 and 10^7 cm/s. Simulation for MCL of 0.5 ns and S of 10^5 cm/sec produced a modeled luminescent decay between the two curves shown.

Table I. Parameters used in Santaurus Device Modeling

	CdTe	CdS	SnO_2
Thickness (μm)	4	0.1	0.5
Band Gap (eV)	1.5	2.4	3.6
N_A (cm^{-3})	p: 2e14	n: 1e17	n: 1e18
μ (cm^2/Vs) e/h	320/40	100/25	100/25
Defect Density (cm^{-3})	D: 2e13	A: 1e17	D: 1e15
Capture Cross Section (cm^2)	e: 1e-11 h: 1e-11	e: 1e-17 h: 1e-12	e: 1e-15 h: 1e-12
t_n (ns, CdTe)	1, 0.5		
Şcm^2/s)	1e5, 1e7		

The modeled results presented in Figure 4 suggest the following guidance for correlating TRPL data with junction functionality. First, although t_1 will likely be a strong function of N_A in the CdTe region (because electric field is a strong function of N_A), t_1 is unlikely to be a good indicator of small changes in either bulk MCL or changes in S. In contrast, TRPL-derived t_2 should be more sensitive to bulk MCL and S [8]. Considering this guidance, the TRPL data

for both the superstrate and substrate devices of this study were re-evaluated to check correlation of V_{oc} with t_2. These data are shown in Figure 3. Note that t_2 values for some devices are not presented because the TRPL fit required only a single exponential (i.e., a t_2 value with low uncertainty could not be extracted for some devices). Although significant scatter exists in the data, the fact that the higher-voltage substrate devices trend with higher t_2 is encouraging. Presently, a similar trend of higher t_2 with higher V_{oc} for superstrate devices is not as clear.

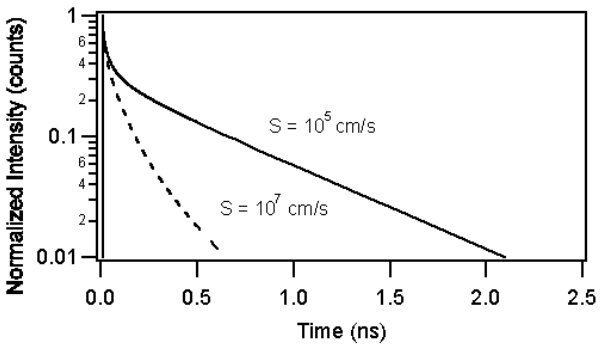

Figure 4. Modeled results showing the effect of normalized luminescent decay on surface/interface recombination velocity for a bulk MCL of 1 ns.

CONCLUSIONS

The majority of MCL studies performed on CdS/CdTe PV devices have correlated device performance primarily with the fast decay observed in TRPL measurements (t_1). This decay is believed to be associated primarily with recombination in W_D, and therefore should be a good indicator of device quality if carrier generation occurs primarily within W_D. Although previous studies have shown that t_1 can be a good indicator of broad device quality, it does not correlate as well with small changes in device performance and/or with differences observed between superstrate and substrate devices. In this case, the parameter t_2 (from the longer-term decay of TRPL luminescence) may not only provide a better correlation with device V_{oc} for superstrate devices but may also provide guidance for inter-comparison with alternative device designs (e.g., substrate devices). It is also suggested that previous studies may yield added value if a larger number of TRPL parameters (i.e., t_1, t_2, and respective amplitudes) are re-examined as a function of device performance.

ACKNOWLEDGEMENTS

This work was supported by the U.S. Department of Energy under Contract No. DE-AC36-08-GO28308 with the National Renewable Energy Laboratory.

REFERENCES

[1] T.A. Gessert, S. Asher, S. Johnston, A. Duda, and M.R. Young, “Proc. 4th WCPVEC, 2006, pp. 432-435.

[2] T.A. Gessert, et al., *Thin Solid Films*, **517**, 200, pp. 2370-2373.

[3] D.S. Albin, R.G. Dhere, S.C. Glynn, J. Del Cueto, and W.K. Metzger, “Degradation and Capacitance-Voltage Hysteresis in CdTe Devices,” *Proc. 2009 SPIE Optics+Photonics Meeting*, NREL/CP-520-46304 (2009).

[4] W.K. Metzger, D. Albin, D. Levi, P. Sheldon, X. Li, B.M. Keyes, and R.K. Ahrenkiel, *J. Appl. Phys.*, **94** (6) (2003).

[5] T.A. Gessert, R.G. Dhere, J.N. Duenow, J.V. Li, S.E. Asher, and M.R. Young, "Comparison of CdS/CdTe Superstrate and Substrate Devices Fabricated with a ZnTe:Zu Contact Interface, *Proc. 35 IEEE Photovoltaics Specialists Conf.,* Honolulu, Hawaii, (2010).

[6] "Synopsys, TCAD SDEVICE Manual, Release A-2008.09, Zurich, Switzerland, www.synopsys.com.

[7] A. Kanevce and T.A. Gessert, “Optimiizing CdTe Solar Cell Performance; Impact of Variations in Minority Carrier Lifetime and Carrier Density Profile,” This Conference.

[8] A. Kanevce, D. Kuciauskas, *J. Appl. Physics*, To be published (2011).