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Degradation of Photovoltaic Modules Under High Voltage Stress in the Field

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ABSTRACT

The degradation in performance for eight photovoltaic (PV) modules stressed at high voltage (HV) is presented. Four types of modules— tandem-junction and triple-junction amorphous thin-film silicon, plus crystalline and polycrystalline silicon modules—were tested, with a pair of each biased at opposite polarities. They were deployed outdoors between 2001 and 2009 with their respective HV leakage currents through the module encapsulation continuously monitored with a data acquisition system, along with air temperature and relative humidity. For the first 5 years, all modules were biased continuously at fixed 600 VDC, day and night. In the last 2 years, the modules were step-bias stressed cyclically up and down in voltage between 10 and 600 VDC, in steps of tens to hundreds of volts. This allowed characterization of leakage current versus voltage under a large range of temperature and moisture conditions, facilitating determination of leakage paths. An analysis of the degradation is presented, along with integrated leakage charge. In HV operation: the bulk silicon modules degraded either insignificantly or at rates of 0.1%/yr higher than modules not biased at HV; for the thin-film silicon modules, the added loss rates are insignificant for one type, or 0.2%/yr–0.6%/yr larger for the other type.

Keywords: photovoltaic, high-voltage stress, degradation, leakage currents, reliability

1. INTRODUCTION

In HV PV arrays consisting of strings comprising multiple series-connected modules, the modules at the terminal ends furthest from the grounded terminal acquire significant HV potential throughout their normal operation. They also incur considerable leakage currents [1, 2] emanating from cell-to-frame leakage paths—from the module cells through the module insulation and package to their frames or anchor points and down to their mechanical support and earth ground. The service lifetime and reliability of PV modules deployed in such a HV configuration can be compromised by leakage-current-induced electrochemical corrosion. The HV leakage currents (LC) that occur continuously during operation can degrade electrical contacts or PV absorber material itself and/or lead to delamination of the layers [3–5], typically leading to high series resistance, lower performance, or even failure. High levels of ambient moisture and temperature exacerbate the HV leakage at any voltage, especially for thin-film modules [6].

We initially set up the HV test bed at NREL's Outdoor Test Facility (OTF) in 1997 to perform HV stress testing of PV modules outdoors, largely motivated by the lack of HV stress testing at that time on current PV products. However, originally the group at JPL [1, 7] addressed the issue of HV-induced electrochemical corrosion and the impacts that encapsulants, moisture, and ionic conduction had on HV LC. Initially, we tested four modules—two amorphous plus two crystalline silicon—on the HV stress test bed between 1997 and 2001 and presented an analysis of this test [2]. After this first test, we removed those four modules and deployed a second round consisting of eight modules, comprising four types of module technologies or packages to perform the same stress exposure at the OTF.

The important LC pathways ascertained from our prior study [2] are reproduced and depicted in Figure 1, which shows conductance through the glass (I_1) and along the interfaces or EVA contained within the module package (I_2, I_3) and out to the frames. In that study, we ignored the contribution to the LC through the back sheet or glass, but have now considered and depicted this pathway as I_4 in Fig. 1. Once the HV bias is given, the size of each the LCs is mostly influenced by ambient conditions of moisture and temperature that affect the outside of the module, as well as moisture intrusion from the edges inward. As a result, one or more of the LC pathways may become the dominant conductance path as ambient conditions change.

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The important features of this type of module package include: the front and back cover glass or sheets, the ethylene vinyl acetate (EVA) pottant used to laminate the cells and back and top covers, the metal frames along the edges used to protect and mount the modules, an edge gasket to protect the glass edges and the frames, and electrical feed-through of the bus-bars or electrical leads out the back side. As shown in Fig. 1, this scheme represents the superstrate thin-film module configuration most closely, because here the PV cells are deposited directly on the top glass. However, a very similar alternate scheme is employed for crystalline (c-Si) or polycrystalline silicon (pc-Si), where there is an extra layer of EVA between the top cover glass and the cells. Another somewhat different construction scheme than that shown is that for thin-film substrate configuration modules such as copper indium diselenide (CIS) or some amorphous silicon (a-Si) modules: in these cases, the PV cells are deposited directly on the back cover, which can be made from glass as for CIS or from a flexible substrate such as stainless steel for a-Si.

At very high relative humidity (RH), we ascertained that LCs are dominated by conductance through the top glass along the glass surface and then to the frames because of the size of the LC and, importantly, its activation energy of ~0.8 eV that corresponds closely to the activation energy for current conduction through soda-lime silicate glasses [8]. We surmised that in this situation of high RH, the top surface becomes coated with a macroscopic layer of adsorbed water, is fairly conductive, and behaves as an equipotential that approximates earth ground potential, so that the LC that cuts through the thickness of the glass is limited by the conductance of soda-lime glass. Similarly, at high RH, the bottom side of the back cover sheet or glass also becomes coated with enough adsorbed water that the LC (I_4) in this path may be limited—depending on construction—by the conductance through the thickness of the back cover. For most silicon technologies, I_4 needs to traverse a finite thickness of EVA before coming into contact with the back cover; I_4 has the added resistance of the EVA.

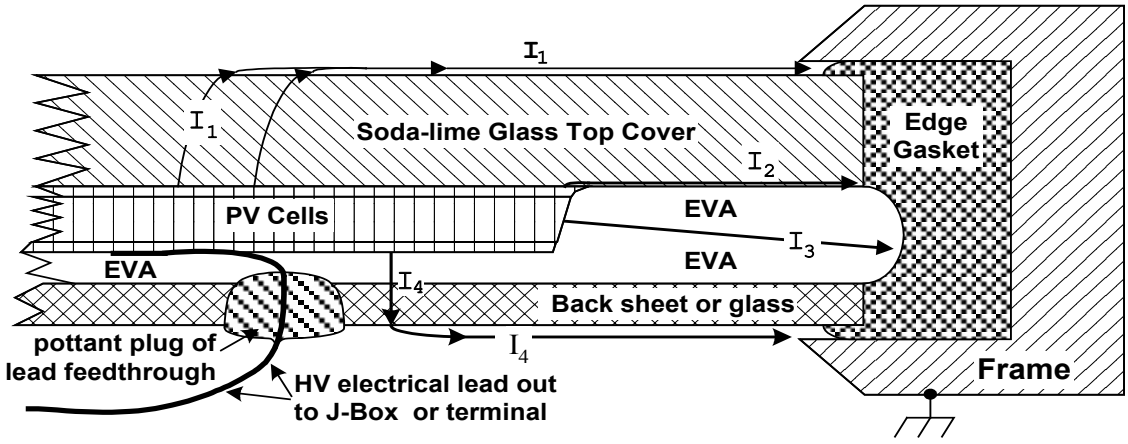

Figure 1. Cross section of typical PV module construction packages, showing leakage current paths I_1, I_2, I_3, I_4.

Presumably after lessons learned about HV conduction by the manufacturers and technological innovations employed to mitigate LC since, not all of the module package construction elements depicted in Fig. 1 are found in some of today's PV modules. For example, some module packages do not include any frames along the edges to mount the modules, so that the LCs to earth ground must then traverse more resistive paths—as for example in modules where the mechanical supports are short rails or anchors potted to the back sides. Another example of a variant construction package is where the module cells are deposited directly onto a flexible substrate on the back sheet, and the top cover is a transparent dielectric polymer sheet. Both of these variations to module construction are employed in multi-junction a-Si PV modules and were included in this new study.

2. EXPERIMENT

The modules were deployed at the OTF at NREL, on an open-air frame rack situated on top of an elevated (~3 m) platform, starting in November 2001. They were erected facing due south (±3°), at a fixed tilt angle (40°±1°) with respect to the horizontal that corresponds closely with the site's latitude (39.74° N). All eight modules were mounted on four, 4-inch long ceramic insulators separating them from the rack structure so as to isolated their frames or anchor points from electrical ground potential. Each module type was biased with either positive or negative polarity voltage,

albeit any single module only saw the one polarity during exposure. Two dedicated programmable HV power supplies—one for each polarity—were employed to bias the modules. The LCs emanating from the HV-biased modules cells, through the module insulation and to the module frames or anchors, and then signal ground were measured by connecting the electrically floating frames/anchors across high-quality precision (2.49 kOhm) drop resistors with low temperature coefficient (2–5 ppm/°C), and then electrical ground, across which the current is converted to a voltage sensed by the differential analog inputs of a data acquisition system (DAS)—a Campbell Scientific CR23x datalogger. The CR23 datalogger was interfaced to a Windows-based PC, both of which contained a certain amount of resident code to perform bias, measurements, and storage. The output voltage levels of HV power supplies were programmed via an external analog signal supplied by the CR23 datalogger executing code to set the bias at a fixed level or to cyclically step the voltage levels. For the first 5 years, the voltages on the modules were held at fixed level ±600 VDC around the clock, except for one minute at noon when the voltage was raised to ±2200 VDC to perform the hi-pot test. In the last 2 years, the voltages were cycled both up and down between 10 and 600 VDC for each polarity, in steps ranging from tens of volts to hundreds of volts, with a typical dwell time of about 100 minutes at each voltage level, thereby executing about 5000 such bias steps per year. The latter bias-step oscillations are designed to emulate the voltage variations observed in modules in actual field operation resulting from varying irradiance.

Additionally, ambient air temperature and RH were monitored by the DAS and the HV power supply voltages. The size of the sensing resistor used along with the analog-to-digital (A/D) converter limited the resolution in current to ~0.2 nanoamperes (nA), so that with signal averaging in 2-minute intervals, we estimate an accuracy of ~10% at 2 nA, which improves at less-sensitive scales. LC values presented henceforth are denoted in nA units unless noted otherwise. All of the sensing resistor circuits and DAS were housed inside an enclosure situated directly underneath the elevated platform. More of the experimental details are explained in the appendix of our previous publication [2]. Because of the potential risk of leakage of the HV bias on the modules onto any elements mounted on their surfaces—such as temperature sensors—we did not measure the HV-biased module temperatures directly. Instead we compensated for this shortcoming by augmenting the HV LC data with proxy module temperatures from: 1) the exact same type of modules deployed on the Performance and Energy Ratings Test bed (PERT) system situated on the roof of the OTF, starting from inception up to 2006; 2) temperatures of newly deployed modules on the same elevated platform in 2005; and accounting for differences between module constructions and air temperatures. By analysis of concurrent proxy module temperatures on the PERT and HV platforms, I numerically estimated that the standard deviation between actual module and proxy temperatures are within ±3 °C for 90% or more of the readings.

The eight modules tested in the second round consist of four types: A) c-Si, B) pc-Si; plus two types of multi-junction a-Si, C) one deposited on flexible substrate with polymer top sheet and metal frames, and D) glass-to-glass superstrate modules without frames, but anchored on the back via short brackets bonded on the rear glass. Relevant details of the construction of a-Si, pc-Si, and c-Si PV modules used in the HV test are listed in Table I below. The module package structures are enumerated in the second column from the left; for the a-Si modules, "TCO" refers to the transparent conducting oxide contact. The encapsulant used to laminate the structures in all types of modules is EVA. HV electrical connections to the modules were made inside their junction box, basically shorting both module leads together, except for the 2J a-Si, which did not have a J-box and so the module leads were shorted inside the enclosure. Prior to deployment, the electrical performance of all modules was characterized by current-voltage measurements performed at standard reporting conditions (SRC). An important feature to keep track of is the ratio of perimeter to area, for if all other variables could be kept equal, the larger this ratio, the more LC. The modules were all dry- and wet-hi-pot tested prior to deployment to insure they passed electrical insulation integrity. After they were taken down in October 2009, their performance at SRC was re-measured—these performance data are discussed later. Additionally, either very similar or identical c-Si, pc-Si, or multi-junction a-Si modules used in the HV test were also deployed on PERT, which serve as a control in low-voltage deployment against which to compare the degradation versus HV-stressed modules. Moreover, for the multi-junction a-Si modules, we have performance data on identical modules that were used in a round-robin study at alternate sites [9] with which to compare degradation against in low voltage deployment.

Table I. Physical Construction and Sizes of PV Module Types Tested

Module Type	Structure: Front to Back	Area (m^2)	Perimeter (m)	Mounts
c-Si	Glass/c-Si cells/Tedlar	0.60	3.4	Al edge frames
pc-Si	Glass/pc-Si cells/Tedlar	0.52	3.1	Al edge frames
2J a-Si	Glass/TCO/a-Si/Al/Glass	0.76	3.7	Rear brackets
3J a-Si	Fluoropolymer/TCO/a-Si/stainless steel	0.45	3.3	Al edge frames

3. LEAKAGE CURRENT DATA

As noted in our prior publication [2], once one fixes the bias voltage, the module LCs are governed predominantly by ambient RH and temperature. This dependence can be summarized by Arrhenius-type behavior where the activation energy and pre-factor to the LC are functions of RH. This characteristic behavior is depicted in Fig. 2 for the pc-Si modules and in Fig. 3 for the c-Si modules occurring within three narrow bands of RH, ±2%-wide about their central values of 10%, 50%, and 95% RH. The LC data depicted in these graphs represent measurements at ± 600 VDC bias on the modules, with both abscissae represented on a logarithmic scale depicted in units of nA, from 1 nA to 10,000 nA. The LC data portrayed are values derived after subtracting out the noise or DC offset levels (~ 0.1 nA) determined for each A/D channel on the datalogger when the bias voltages are zero. The ordinate axes represent the reciprocal of the absolute temperature, in units of $°K^{-1}$. Furthermore, the data are filtered so that only those values for which the RH was stable during the previous 4 hours to within 15% relative of the center values are depicted. So, for example, in the 10% RH band, the stability is gauged by the standard deviations of all measurements being ≤ ±.5% absolute RH. This insures that some amount of stable moisture levels penetrate into the EVA inside the module packages.

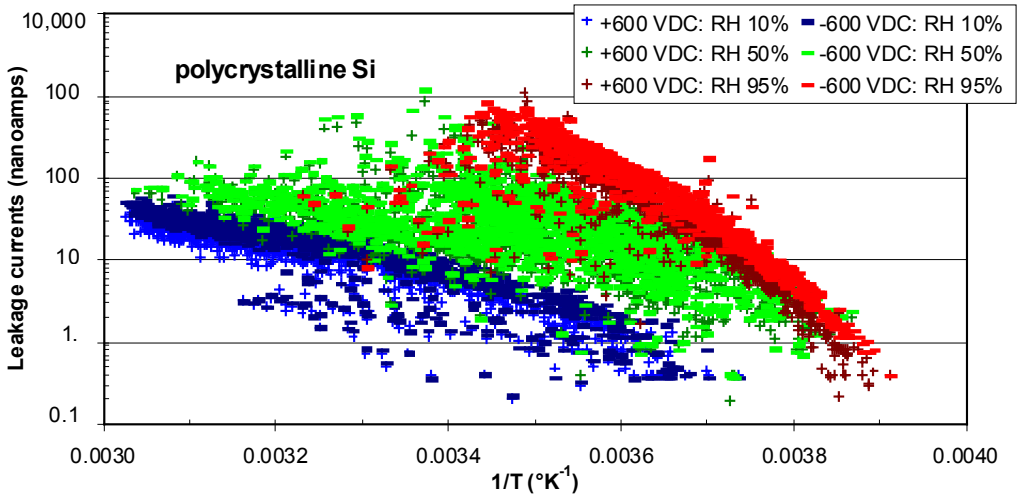

Figure 2. Leakage currents at 600 VDC for pc-Si modules plotted against inverse absolute module temperature, in three bands of RH values, 10%, 50%, and 95%, for positive (+) , negative (-) polarities, in ±2% wide RH bands.

Figures 2 and 3 exhibit similar trends in the LCs: at high RH (95±2%), the activation energy is larger than at low RH, typically being ~1.0 eV for the pc-Si modules, and ~0.86 or 1.0 eV, respectively, for positive or negative polarity, in the c-Si modules. At low RH (10±2%), the activation energies are about 0.56 eV for the pc-Si, and 0.81 or 0.76 eV, respectively, for the positive or negative polarity in the c-Si modules. The maximum values of the LCs are about 1 or 2 microamps (1000 or 2000 nA), respectively, for the pc-Si and c-Si modules at the highest RH. At the lowest RH (10%), the highest LC values for the pc-Si and c-Si modules are 30 and 100 nA, respectively. The c-Si module obviously leaks more current than the pc-Si modules under similar temperature and RH conditions. This larger leakage may represent differences in composition of the top cover soda-lime glasses between the two module types. Although not shown for the sake of clarity, the LCs at 75% RH are similar in size and activation to those at the higher RH; likewise, the LC data at 25% RH are similar in size and activation to those at 10%. In the intermediate data range at 50% RH, it appears as if the activation energies are even smaller than those at low RH. It is believed that this anomalous low activation behavior is an artifact of the way one defines the RH coupled with non-equilibrium effects occurring more frequently at intermediate RH values. RH is the ratio of the partial pressure of water in the atmosphere to the saturated vapor pressure of water at a given temperature. The temperatures plotted on the ordinate axes represent module values, whereas the RH data represent values referenced to ambient air temperature. In other words, it does appear that at 50% RH, one encounters more non-equilibrium conditions than at very low or high RH. The module temperatures can be quite higher than the air temperatures, especially during the daytime, so the RH levels just above the surfaces of the modules are probably quite a bit lower than farther away in the ambient air. In fact if one excludes data where the irradiance levels are below 100 W/m^2, there are few cases of data with reciprocals of the absolute temperature below 0.0034 $°K^{-1}$; and then the activation energies at 50% RH are not very different than those at low RH. At low RH, this effect is marginal because

there is little moisture in the atmosphere and the activation energies between 25% RH and 1% appear to be similar. Because of the dry climate in Colorado (location of the OTF), times of high RH generally correspond to overcast or precipitative moisture conditions when the sun is obscured, in which case module and air temperatures are nearly equal.

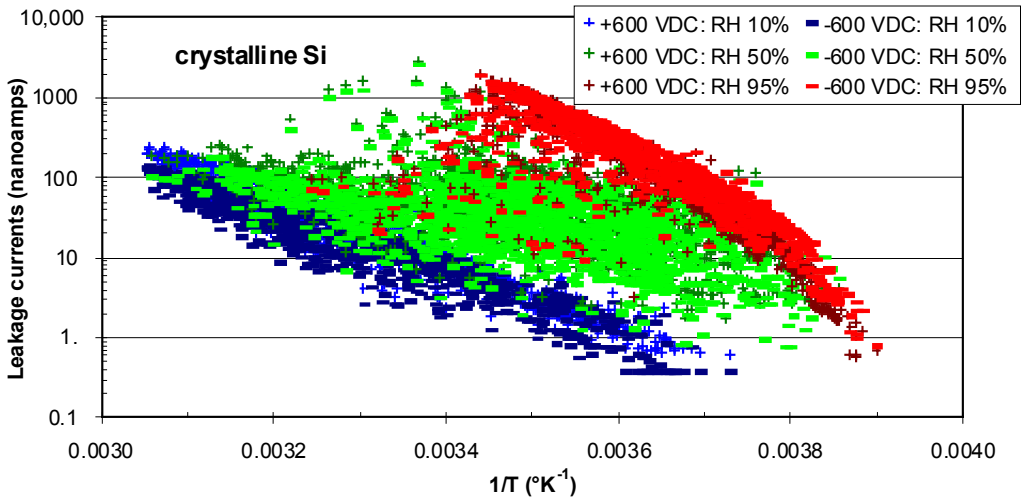

Figure 3. Leakage currents at 600 VDC for c-Si modules plotted against inverse absolute module temperature, in three bands of RH values, 10%, 50%, and 95%, for positive (+), negative (-) polarities, with ±2% wide RH bands.

In the following two graphs, Figs. 4 and 5, the LC data for the 2J a-Si and 3J a-Si modules are plotted on similar semi-logarithmic graphs against reciprocals of absolute module temperatures. Note that the abscissa values are shown down to 0.01 nA, where obvious quantization steps appear in the data that are associated with A/D conversion. These low LC values are evident in the a-Si modules because their leakage data are quite lower than for the bulk Si (pc-Si and c-Si) modules, and because subtracting out the signal offset levels from the raw data effectively spreads or maps out corrected data from the range of 0.1 nA–1.0 nA over one lower decade onto the range 0.01–1.0 nA. This seems especially true for the 2J a-Si module, which has no perimeter frames and concomitantly has the lowest leakage among all four module types. These low LC data are shown for reference only, as there is probably over 50% error associated with the data depicted in the range 0.1–0.01 nA due to correcting for the zero-offset signal values.

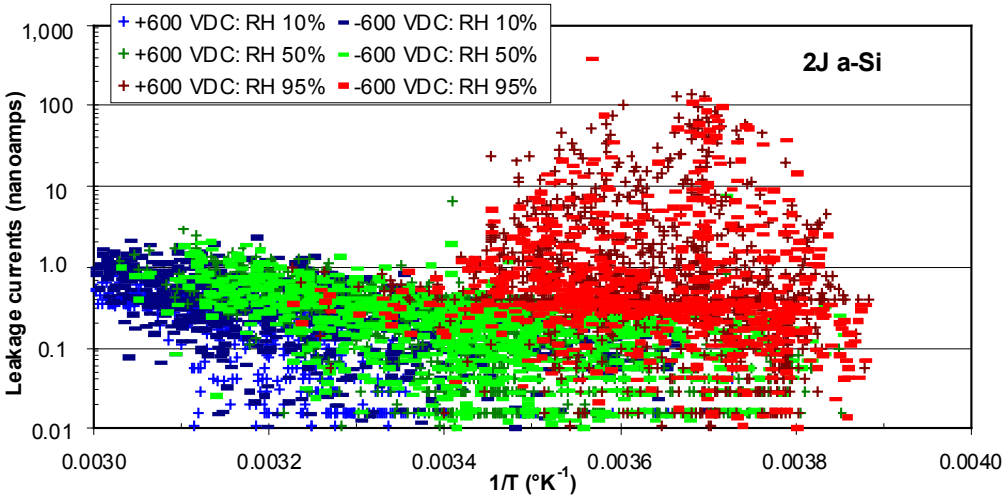

Figure 4. Leakage currents at 600 VDC for tandem-junction a-Si modules plotted against inverse absolute module temperature, in three bands of RH of 10%, 50%, and 95%, ±2%, for positive (+) , negative (-) polarities.

Nevertheless, it's evident from Figs. 4 and 5 that the LCs for these two different types of a-Si multi-junction modules behave substantially different than for the bulk Si modules. The 2J a-Si modules are glass-to-glass laminates with rear bracket mounts, so that even when there is high humidity and the LCs may be dominated by conductance through the glass, they must go through a more tortuous path to get to ground potential than in the cases where the modules have frames, as for the bulk Si modules. Considering the variations in LC data, it does not appear numerically significant to formulate either 2J a-Si or 3J a-Si leakage data as being thermally activated. The leakage from both types of a-Si modules at high RH is likely thermally activated, but the spread in the data is too large to accurately determine the temperature dependence. For the 3J a-Si module with a fluoropolymer top cover sheet and aluminum perimeter frames, it appears that the leakage conductance through either this polymer or the back sheet is lower than what can be accurately measured, except for some LC cases with values up to ~100 nA at high RH. However, the LC data at high RH for both module types seem to comprise two populations: one with and the other without temperature dependence. This dichotomy is very likely due to the appearance of macroscopic amounts of precipitable water on the top surfaces when the LCs are larger, versus those cases of high RH when the modules are dry at leakage is smaller.

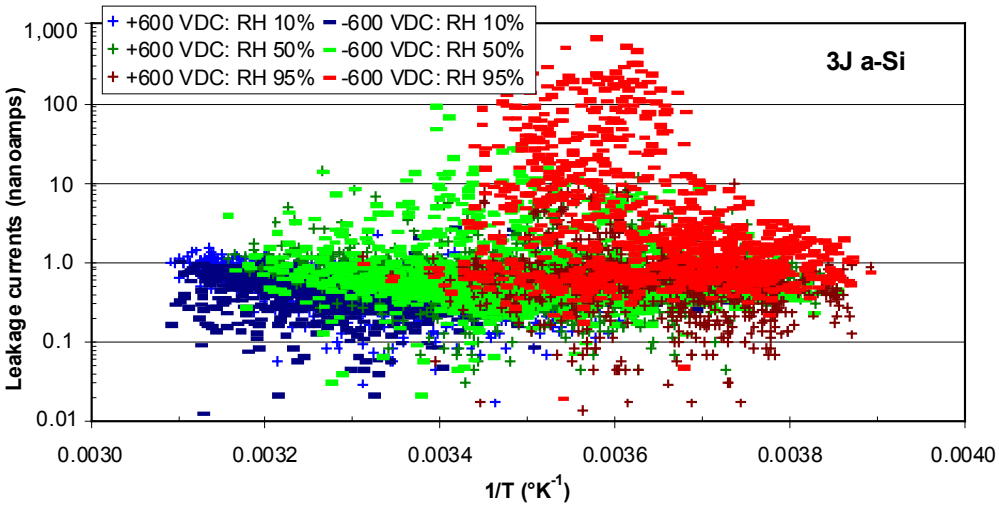

Figure 5. Leakage currents at 600 VDC for triple-junction a-Si modules plotted against inverse absolute module temperature, in three bands of RH of 10%, 50%, and 95%, ±2%, for positive (+) and negative (-) polarities.

4. INTEGRATED ACCUMULATED LEAKAGE: CHARGE

According to the JPL group [1], the amount of electrochemical corrosion sustained by modules biased at HV may be correlated and quantified by the accumulated charge per perimeter length of the module, with the accumulated charge being the integral of the LC over time. They determined the threshold levels for 50% failure rates for the c-Si and a-Si modules as 0.1–1 Coulombs per centimeter (C/cm) and 1–10 C/cm, respectively, for a-Si and c-Si modules, for failure modes common in module constructions available at that time. Since then, module packages have improved, so it's not evident that these threshold levels are still accurate. Nevertheless, these threshold values serve as useful measures to compare against. The accumulated integrated charge in coulombs —without normalizing to perimeter lengths—are depicted in Figs. 6 and 7, respectively, for the bulk Si and a-Si thin-film modules, read along the left-hand abscissae and plotted against time between November 2001 and September 2009. Superimposed on these two graphs along the top portion of the graphs are the partial pressures of water in the atmosphere expressed in millibar (mBar) units, read along the right-hand abscissae plotted also versus time. The data actually portrayed represent only an extremely small random fraction of the entire data set. Times before July 22, 2007, represent HV operations with constant ±600 VDC applied bias. After that date, the datalogger code was changed to apply alternating, cyclical bias voltages between 10 and 600 VDC, in steps or increments ranging from tens to hundreds of volts. Because in the latter case the average bias during this step-stress is considerably smaller than previously when 600 VDC were applied, the time rate of change of the integrated charge is correspondingly smaller after July 22, 2007.

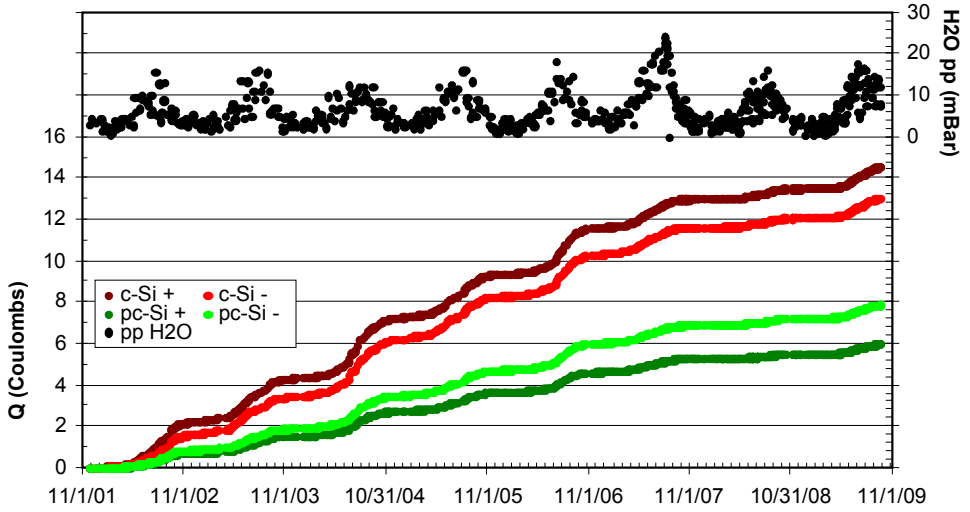

Figure 6. Integrated charge on c-Si and pc-Si modules read along the left-hand abscissae plotted vs. time; and partial pressure of water vapor in the atmosphere, read along the right-hand abscissae, also plotted vs. time.

From Fig. 6, one observes that the occurrence of greatest time rate of change in charge—integrated LC— correspond to times of larger amount of water vapor in the atmosphere for the bulk Si modules. This observation provides a fairly good indication of the dependence of the LC on the amount of water that ultimately soaks onto and into the c-Si and pc-Si module packages. This behavior is contrasted with that of the a-Si modules shown in Fig. 7. For the a-Si modules, the integrated LC charges are extremely low for the 2J a-Si modules of either polarity—between .05 and 0.25 C—and only somewhat more substantial for the negatively-biased 3J a-Si module, which accumulates to ~1.9 C by the end of the test.

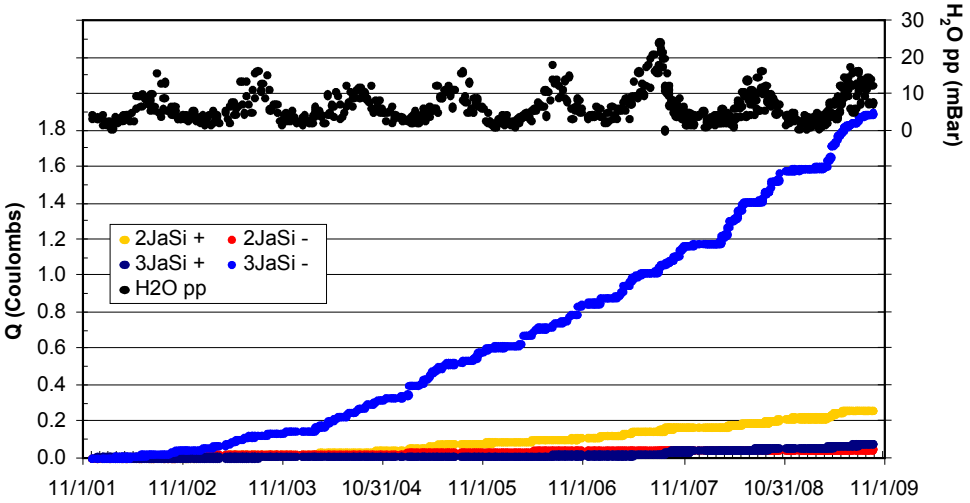

Figure 7. Integrated charge (Q) on 2J a-Si and 3J a-Si modules read along the left-hand abscissae plotted vs. time; and partial pressure of water vapor in the atmosphere, read along the right-hand abscissae, also plotted vs. time.

The time rates of change of integrated charge do not appear to correlate as well with times of high water vapor content in the atmosphere for any of the a-Si modules. Note that for the negatively biased 3J a-Si module—where there is appreciable leakage charge—there seems to be an induction time for this accumulated charge, where in the first 2 years of deployment, the rate of change is small, ~0.08 C/yr. Thereafter, between Nov. 2003 and July 2007, the rate of change increases to ~0.25 C/yr; and then after July 2007, during step-bias stress, this rate nearly doubles to 0.45 C/yr. For the negatively biased 3J a-Si module, one observes that an induction time for appreciable rate of charge increases, and the largest rate of change of charge occurs after application of stepped HV bias commencing after July 2007. This observation may point to a potential source of damage that is different from all the other modules, occurring most often

with stepped-bias stress, which points away from DC leakage current-induced damage to polarization current-induced damage. This polarization current is likely activated more by abrupt step changes in bias than by exerting constant bias.

5. PERFORMANCE BEFORE AND AFTER HV STRESS TEST

The performance data of the featured eight modules are enumerated in Tables II and III, respectively, for the multi-junction a-Si and bulk Si modules. The headings starting from left at baseline, listing in the first 6 columns, are: module and date, simulator test-bed, open-circuit voltage (V_{OC}), short-circuit current (I_{SC}), fill factor (FF), and efficiency under standard test conditions (STC). The next six columns contain similar fields of data, except measured after the modules were taken down from the HV stress test. The different simulator test beds used are the: SPIRE, Large Area Continuous Solar Simulator (LACSS), and/or Standard Outdoor Measurement (SOM). The SPIRE's illumination is pulsed to minimize module heating; the LACSS and SOMS provide continuous illumination. Data are spectrally corrected using the standard reference cell method, knowing the spectral quantum efficiencies for the reference cell and devices under test. From Table II, we see there is apparent degradation in the multi-junction a-Si modules, but we must correct for the normal Staebler-Wronski Effect (SWE) degradation before we can ascertain any additional degradation due to HV stress. The initial SWE loss is defined as the performance drop in the first 1000 kW-h/m^2 of exposure. For these a-Si modules, the dominant sources of the degradation in order of important are FF losses, then V_{OC} and I_{SC} losses.

Table II. Power Performance Measurements at STC for 2J a-Si and 3J a-Si Modules for ± Polarities

Module/Date	Test	V_{OC}	I_{SC}	FF	Eff	Module/Date	Test	V_{OC}	I_{SC}	FF	Eff
At Baseline						**After HV Stress**					
2J a-Si: - Polarity						**2J a-Si: - Polarity**					
8/10/2000	SPIRE	66.83	1.114	66.5	6.54	12/8/2009	SPIRE	61.31	1.033	50.6	4.25
8/10/2000	SOMS	66.28	1.128	69.2	6.85	12/2/2009	LACSS	60.95	1.038	52.9	4.43
						12/15/2009	SOMS	61.12	0.971	52.8	4.30
						12/3/2009	SPIRE4600	61.27	1.098	51.6	4.60
2J a-Si: - Polarity	**Average**	**66.56**	**1.121**	**67.9**	**6.70**		**Average**	**61.16**	**1.035**	**52.0**	**4.40**
2J a-Si: + Polarity						**2J a-Si: + Polarity**					
8/10/2000	SPIRE	63.79	1.100	69.3	6.43	12/8/2009	SPIRE	59.16	0.994	56.0	4.36
8/10/2000	SOMS	63.16	1.121	71.9	6.74	12/2/2009	LACSS	58.38	1.007	57.1	4.45
						12/15/2009	SOMS	58.73	0.932	57.1	4.31
						12/3/2009	SPIRE4600	59.18	1.060	55.7	4.63
2J a-Si: + Polarity	**Average**	**63.48**	**1.111**	**70.6**	**6.59**		**Average**	**58.86**	**0.998**	**56.5**	**4.44**
3J a-Si: - Polarity						**3J a-Si: - Polarity**					
7/16/2001	SPIRE	24.66	2.471	64.4	8.71	12/8/2009	SPIRE	22.40	2.246	50.4	5.63
7/24/2001	LACSS	24.11	2.455	67.5	8.87	12/2/2009	LACSS	22.41	2.261	53.4	6.01
7/16/2001	SOMS	23.71	2.495	66.0	8.69	12/15/2009	SOMS	22.47	2.109	53.3	5.73
						12/3/2009	SPIRE4600	22.54	2.048	56.0	5.73
3J a-Si: - Polarity	**Average**	**24.16**	**2.474**	**66.0**	**8.76**		**Average**	**22.46**	**2.166**	**53.3**	**5.78**
3J a-Si: + Polarity						**3J a-Si: + Polarity**					
7/16/2001	SPIRE	24.85	2.480	65.3	8.93	12/8/2009	SPIRE	22.51	2.247	51.8	5.81
7/24/2001	LACSS	24.29	2.474	68.1	9.08	12/2/2009	LACSS	22.53	2.278	54.1	6.16
7/16/2001	SOMS	24.00	2.496	66.6	8.88	12/15/2009	SOMS	22.79	2.122	53.7	5.87
						12/3/2009	SPIRE4600	22.60	2.059	56.4	5.83
3J a-Si: + Polarity	**Average**	**24.38**	**2.483**	**66.7**	**8.96**		**Average**	**22.61**	**2.177**	**54.0**	**5.92**

Two sources of degradation data are used for the multi-junction a-Si modules in low-voltage configuration to compare against HV losses to scrutinize between HV-induced degradation and normal SWE losses: identical module data from the PERT system plus data from identical modules that underwent a round-robin exposure test at separate geographical sites, including Colorado. For the 3J a-Si modules, we also have data for identical modules put through light-soaking for 1000 h to quantify SWE losses and then set out in the field. During the initial phase of SWE (3J a-Si), we observed an average relative decline of 12.1% relative to baseline for four of these modules light-soaked indoors for 1000 kW-h/m^2; for the 2J a-Si modules, the SWE degradation was 26.0% loss relative to baseline, for two of the same manufacturer's modules deployed on PERT after 188 days (~0.5 yr) outdoors at the OTF. Two other identical 2J a-Si modules from the same manufacturer that underwent a round-robin exposure test [9] degraded ~34.0% relative to baseline, after an entire year of exposure at the OTF. For identical 3J a-Si modules that underwent round-robin exposure deployed at the OTF, the degradation average was 29%, also after an entire year of outdoor deployment.

After the initial SWE onset, the average rate of performance decline for the 2J a-Si modules was 1.1±0.1%/yr relative to average value, using PERT data. For these, we can actually just extrapolate the losses expected by extending the relative loss rate until 7.87 years elapse from date of deployment: the total loss is 31.7% relative to baseline. When the 3J a-Si module was first deployed outdoors on PERT, it degraded by 6% relative to baseline, which appears un-recoverable; thereafter, the performance exhibited seasonal oscillatory behavior superimposed on a long-term loss-rate trend line of ~ 0.31±0.04%/yr relative to average performance value, of which we have fit PERT data for just under 8 years of deployment. Similarly, we arrive at a total loss for the 3J a-Si on PERT of 23.8% relative to baseline. It helps to know that the average estimated time for that the initial 1000 kW-h/m^2 exposure SWE to occur is ~188 days, based on the average daily insolation at the OTF site in Golden, Colorado, at latitude tilt is 5.3 kW-h/m^2 per day.

To compare HV losses with those from the round-robin experiment, we subtract the product of relative loss rate (PERT-derived) times length the HV stress test (HVST) minus 1 year or 6.87 years. Hence the first-year losses for similar 3J a-Si modules are 29%, so to this loss one adds an additional loss of 2.1% (6.9 yr * 0.31%/yr), which is 29.0% + 2.4% = 31.1%. For the 2J a-Si modules, the loss using the round robin data is 34.0 + 1.1*6.78= 41.4%. The measured performance losses from data at baseline and after HVST: for the 2J a-Si, the losses are, respectively, 32.6% or 34.3%, for positive or negative polarity; for the 3J a-Si modules, the losses are, respectively, 33.9% or 34.0%, for positive or negative polarity. For the 2J a-Si modules, the added losses from the HVST are: 0.9% or 2.6%, respectively, for the positive or negatively polarity, going only by PERT data; however, when compared to losses from the round-robin experiment there are no added losses due to HV stress. Similarly for the 3J a-Si modules, using PERT data to compare, the losses of the 3J a-Si modules probably increase by an additional 10.1% or 10.2%, respectively, for the positive or negatively biased modules. However, using loss data from the round-robin experiment for 3J a-Si plus the long-term loss trend from PERT in low-voltage deployment, the 3J a-Si modules lost 2.8% or 2.9%, respectively, for positive or negative polarity due to HV stress.

The losses observed in Table III are substantially different for the c-Si and pc-Si modules deployed on the HVST. First, inspecting changes in the pc-Si modules, there is no apparent change or degradation of performance data between baseline and testing after stressing at HV in the fall of 2009; this is true for either of the positively or negatively biased pc-Si modules. In fact, even though the positively biased pc-Si may seem to have improved—11.44% before, 11.6% after HVST—this is due mostly to the added point from the newer SPIRE4600 simulator in use recently.

Table III. Power Performance Measurements at STC for c-Si and pc-Si Modules for ± Polarities

Module/Date	Test	V_{OC}	I_{SC}	FF	Eff	Module/Date	Test	V_{OC}	I_{SC}	FF	Eff
At Baseline						**After HV Stress**					
c-Si: - Polarity						**c-Si: - Polarity**					
9/14/2001	SPIRE	21.91	4.400	70.4	11.59	12/8/2009	SPIRE	21.69	4.329	71.6	11.10
9/17/2001	LACSS	21.78	4.455	69.4	11.40	12/2/2009	LACSS	21.58	4.276	71.2	10.80
9/14/2001	SOMS	21.38	4.477	68.4	11.30	12/15/2009	SOMS	21.73	4.263	71.0	11.10
						12/3/2009	SPIRE4600	21.72	4.399	71.9	11.30
c-Si: - Polarity	**Average**	**21.69**	**4.444**	**69.4**	**11.43**		**Average**	**21.68**	**4.317**	**71.4**	**11.08**
c-Si: + Polarity						**c-Si: + Polarity**					
10/2/1998	SPIRE	21.71	4.305	66.4	10.92	12/8/2009	SPIRE	21.50	4.309	67.1	10.20
10/6/1998	LACSS	21.55	4.313	65.5	10.80	12/2/2009	LACSS	21.39	4.267	66.7	10.00
10/6/1998	SOMS	21.38	4.479	66.3	10.50	12/15/2009	SOMS	21.46	4.210	67.0	10.30
						12/3/2009	SPIRE4600	21.47	4.346	67.6	10.40
c-Si: + Polarity	**Average**	**21.55**	**4.366**	**66.1**	**10.74**		**Average**	**21.46**	**4.283**	**67.1**	**10.2**
pc-Si: - Polarity						**pc-Si: - Polarity**					
7/25/2001	SPIRE	21.30	3.778	73.6	11.42	12/8/2009	SPIRE	21.25	3.812	73.1	11.40
9/6/2001	LACSS	21.17	3.801	72.9	11.30	12/2/2009	LACSS	21.11	3.748	72.7	11.10
8/27/2001	SOMS	20.94	3.902	72.3	11.40	12/15/2009	SOMS	21.22	3.815	72.6	11.50
						12/3/2009	SPIRE4600	21.22	3.895	72.6	11.60
pc-Si: - Polarity	**Average**	**21.14**	**3.827**	**72.9**	**11.37**		**Average**	**21.20**	**3.818**	**72.8**	**11.40**
pc-Si: + Polarity						**pc-Si: + Polarity**					
7/25/2001	SPIRE	21.36	3.809	73.4	11.52	12/8/2009	SPIRE	21.29	3.848	73.4	11.60
9/6/2001	LACSS	21.22	3.819	73.2	11.40	12/2/2009	LACSS	21.17	3.794	73.0	11.30
8/27/2001	SOMS	20.78	3.938	72.1	11.40	12/15/2009	SOMS	21.35	3.898	73.4	11.70
						12/3/2009	SPIRE4600	21.29	3.912	73.5	11.80
pc-Si: + Polarity	**Average**	**21.12**	**3.855**	**72.9**	**11.44**		**Average**	**21.28**	**3.863**	**73.3**	**11.60**

For the c-Si modules, there does appear to be degradation before and after the HVST: 3.06% or 5.03% losses, respectively, for the positively or negatively biased polarities. We can derive an average degradation rate from an identical module deployed on PERT, plus another one with similar construction from data published previously [11] as 0.41%±0.11%. Using this degradation rate, plus the number of years of the HVST, one arrives at a 3.26% total loss for this type of module in low-voltage deployment. So comparing this with HVST before and after data, we note the added losses incurred for HV operation of the c-Si modules are either 0% or 1.8%, respectively, for the positively or negatively biased polarities.

6. DISCUSSION AND CONCLUSIONS

The HV-induced leakage currents from eight modules, a pair from each module type of c-Si, pc-Si (bulk Si), and tandem-junction and multi-junction a-Si were monitored continuously for almost an 8-year period. The leakage currents from thru c-Si and pc-Si modules appear to be thermally activated with an activation energy that varies with RH, ranging 0.86–1.0 eV at high RH, down to 0.56 to 0.8 eV at low RH. The larger activation energies are fairly consistent with conduction through soda-lime glass, albeit with the different sodium compositions. For the a-Si modules, the leakage currents are much lower than those for the bulk Si modules, by at least a factor ranging between 10 and 100 times smaller, under otherwise similar conditions. The leakage currents from the a-Si did not appear to indicate Arrhenius-type behavior as did the leakage currents from bulk Si modules—leakage currents may have a temperature dependence that is not thermally activated. This is very likely due to innovations made for the a-Si thin-film modules: in one case (2J a-Si), the module contains no edge frames, and thereby the leakage has to travel a more tortuous path to get to ground potential; in the case of 3J a-Si modules, it is probably innovation of module package laminates that mitigates LC in HV deployment.

For the 2J a-Si case, the modules have no frames. The anchors or mounting brackets—through which LC need to travel—are glued to the back glass sheet, and LC needs to traverse either the outer edges of the module across a layer of EVA or traverse the EVA inside the module to get to the back sheet. But more significantly, because the mounting brackets are glued to the back sheet with a silicone epoxy, it's very likely that the metal mounting brackets are not even in direct contact with the glass, or if they are, that they contact the glass at isolated points along the bracket-glass interface, otherwise filled with silicone in between that is quite resistive. Hence, the path that HV LCs must traverse to reach ground contains more resistive hurdles than in other packages with edge frames, so the resistance is much greater even in high humidity conditions, and the activation energy for electrical conductance is not a simple function of RH.

For the 3J a-Si module, the top cover sheet is a fluoropolymer, ETFE, which at least initially is free of ion impurities. Its bulk resistivity is listed in the range of 10^{16}–10^{17} ohm-cm [12, 13], compared to soda-lime silicate glass with a resistivity in the range 10^{10}–10^{13} ohm-cm [8]. In soda-lime glass, sodium is the dominant impurity ion that gives the glass its conductance and activation behavior. In ETFE, the bulk resistivity is between 2 and 5 orders of magnitude larger and there are few or no impurities to mediate higher conductance. However, it is probable that after some exposure—induction time—in the field, the EVA pottant degrades and its byproducts corrode the TCO or metallization in the 3J a-Si module, thereby leading to higher LC conductance in the ETFE. This may account for the induction time observed for the rate of increase of charge in the negatively biased 3J a-Si module. The higher rate of charge accumulation after July 2007 coincides with the abrupt step-voltage term of the experiment, and is probably related to polarization or dielectric relaxation of the ETFE or other packaging materials in the negatively biased 3J a-Si module.

The integrated charge normalized to unit perimeter lengths for the bulk Si modules are: 0.043 C/cm, 0.038 C/cm, 0.019 C/cm, and 0.025 C/cm, respectively, for the positive bias c-Si, negative bias c-Si, positive bias pc-Si, and negative bias pc-Si modules. These accumulated charge per unit perimeter lengths are substantially smaller than the threshold damage for 50% failure figures for c-Si given by the JPL group: between 1 and 10 C/cm. Indeed the changes in performance of the bulk Si modules before and after the high-voltage stress test indicate zero change for the pc-Si modules and a 1.8% total change at most for the positively biased c-Si module, which represents an added 0.23%/yr loss due to high-voltage operation. For the a-Si modules, the only module that sustained significant integrated leakage charge was the negatively biased 3J a-Si module, about 1.9 C, which represents a normalized dose per perimeter length of 0.0058 C/cm. All the other thin-film a-Si modules sustained cumulative normalized doses of charge per unit perimeter of less than 0.0007 C/cm. However, the performance data for the multi-junction a-Si modules indicate added losses due to HV operation: between 0.0%/yr and 0.1%/yr for the 2J a-Si types; and between 0.35% and 1.3%/yr for the 3J a-Si modules. It appears

that even with the lower HV leakage currents or integrated charge, some of the thin-film a-Si modules are slightly more susceptible to damage than the c-Si modules. However, one still needs to consider an acceleration factor for HV stress degradation due to continuous operation to quantify more precisely the HV-related loss rates.

Because of operating the HV stress test continuously 24 h per day, the loss rates should be scaled down by an estimated acceleration factor of approximately 2. Hence, these are: for pc-Si 0.0%/yr; for c-Si 0.1%/yr, positive polarity; for 2J a-Si between 0% and 0.05%/yr; and for 3J a-Si modules ranging 0.2%/yr to 0.6%/yr. The added damage loss rates for the 2J a-Si modules are just above statistical significance, with an error of about ±10%. For the 3J a-Si modules, which experience more significant loss in HV operation, there is enough variability in the degradation data from the two cases of low-voltage operation of identical modules to suggest the loss rates may not be too much higher than those for the 2J a-Si modules. Both of these types of a-Si encompass innovations that helped mitigate damage in HV operation.

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The degradation in performance for eight photovoltaic (PV) modules stressed at high voltage (HV) is presented. Four types of modules--tandem-junction and triple-junction amorphous thin-film silicon, plus crystalline and polycrystalline silicon modules--were tested, with a pair of each biased at opposite polarities. They were deployed outdoors between 2001 and 2009 with their respective HV leakage currents through the module encapsulation continuously monitored with a data acquisition system, along with air temperature and relative humidity. For the first 5 years, all modules were biased continuously at fixed 600 VDC, day and night. In the last 2 years, the modules were step-bias stressed cyclically up and down in voltage between 10 and 600 VDC, in steps of tens to hundreds of volts. This allowed characterization of leakage current versus voltage under a large range of temperature and moisture conditions, facilitating determination of leakage paths. An analysis of the degradation is presented, along with integrated leakage charge. In HV operation: the bulk silicon modules degraded either insignificantly or at rates of 0.1%/yr higher than modules not biased at HV; for the thin-film silicon modules, the added loss rates are insignificant for one type, or 0.2%/yr-0.6%/yr larger for the other type.

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