Striving for a standard protocol for preconditioning or stabilization of polycrystalline thin film photovoltaic modules

2009 SPIE Optics and Photonics Conference
San Diego, CA

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August 5, 2009

NREL/PR-520-46525

Outline of Talk

- Rationale for stabilization/preconditioning procedure
- Proposed Study plan to probe transitory behavior
  - Consists of preconditioning
  - Dark 90°C anneal at open circuit
    - emulates 85/85, but shorter and perhaps induce reversible changes
  - Two branches of subsequent stabilization
    - Light exposure at 1-sun, 60°C
    - Dark exposure at 60°C, in forward bias between optimum power point voltage and open-circuit voltage
- Modules used in study
- Value of C-V profiling as signature
- C-V profiles
  - on CIGS module, sweep directions, frequencies
  - Carrier concentrations, depletion widths on CIGS & CdTe modules
- Performance changes in CIGS & CdTe modules with stabilization/preconditioning procedure
- Summary & conclusions
  - CV -derived depletion width changes & hysteresis appear linked to stability
  - Dark exposure in forward bias likely emulates light exposure at 1-sun

Rationale for Preconditioning Procedure

- Transient and metastable changes in CdTe/CIGS performance pose challenges in assessing performance:
  - Is a unique PV conversion efficiency/performance metric possible without specifying prior exposure history? (probably not)
  - Time between exposure and I-V measurement is critical

- Current standard for thin-film PV certification (IEC 61646) stabilization:
  - calls for light-soaking until change in power ≤ 2% is achieved, after consecutive periods of at least 43 kW-h/m^2 of integrated irradiance
  - designed with amorphous silicon (a-Si) in mind
    - Dominant defect mechanism in a-Si: light-induced Staebler-Wronski effect
  - CIGS or CdTe devices most likely have different defect mechanisms
    - Current procedure may be inadequate when applied to CIGS / CdTe

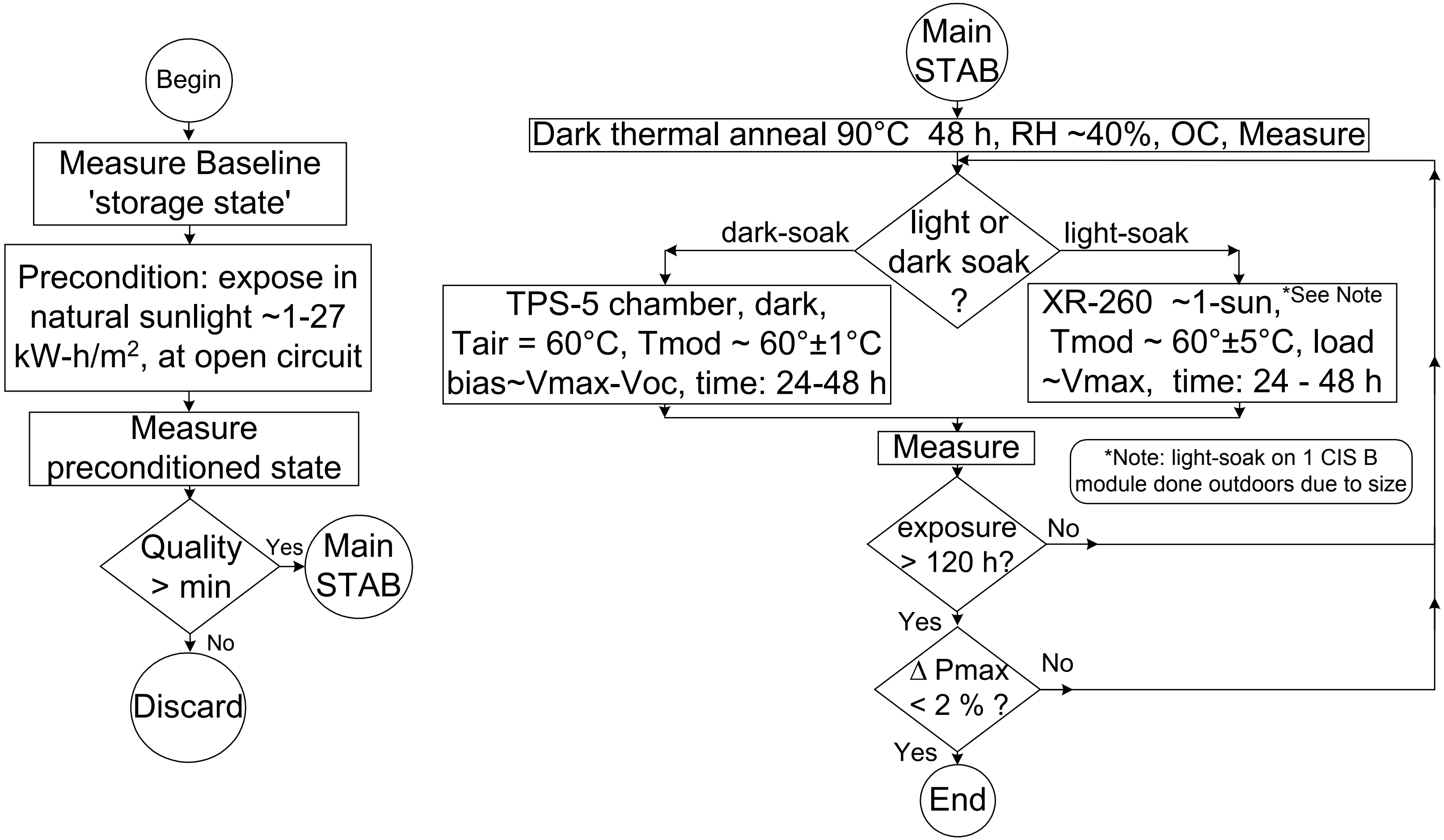
- Appropriate preconditioning or stabilization steps prior to performance testing would lead to reduced error in assessing long-term energy yield, service lifetime and/or reliability.

Defects in CIGS or CdTe

- Ascribed major role in shaping transient or metastable phenomena
- Mobile ions
  - CdTe
    - Cu moving between back contact and CdS/CdTe interface
  - CIGS
    - Cu - In vacancy complexes
    - Se vacancy
- Presence of Traps
  - CdTe
    - Voc increases with time
  - CIGS
    - Persistent photoconductivity
    - Changes in acceptor concentration after thermal anneal
    - Charging/discharging of donors at CdS/CIGS interface
- C-V profiling used as probe for defects in CIGS & CdTe

Proposed Stability Study Plan Flowchart

- Preconditioning step & Main Stabilization Sequence Study Plan
  - Main Stabilization:
    - dark 90°C anneal step, emulates and is shorter version of 85C/85% RH 1000-h certification test
    - consists of two branches: light exposure & biased dark exposure, both @ 60°C
    - Biased dark exposure is advantageous if successful because of ease and lower cost



Begin

Measure Baseline 'storage state'

Precondition: expose in natural sunlight ~1-27 kW-h/m^2, at open circuit

Measure preconditioned state

Quality > min

Yes

Main STAB

No

Discard

Main STAB

Dark thermal anneal 90°C 48 h, RH ~40%, OC, Measure

light or dark soak ?

dark-soak

light-soak

TPS-5 chamber, dark, Tair = 60°C, Tmod ~ 60°±1°C bias~Vmax-Voc, time: 24-48 h

XR-260 ~1-sun, *See Note Tmod ~ 60°±5°C, load ~Vmax, time: 24 - 48 h

Measure

*Note: light-soak on 1 CIS B module done outdoors due to size

exposure > 120 h?

No

Yes

Δ Pmax < 2 % ?

No

Yes

End

Modules Studied

- ❑ Diverse set of CdTe & CIGS modules
  - ➢ Some nascent or new, never used, or stored as controls
  - ➢ Some pre-exposed in hot-humid climate
  - ➢ Some light-soaked indoors

Module Type	Quantity	Exposure Conditions	Pre-existing exposure conditions
CdTe A	2	One each: light soak, biased dark soak	Yes, hot-humid outdoors 3 years
CdTe B	2	One each: light soak, biased dark soak	No, nascent
CdTe C	1	biased dark soak	Yes, indoor light-soak, 1130 kW-h in 2002
CIGS A	4	Two each: light soak, biased dark soak	Nascent: 3 controls from 2003; 1 pre-exposed in hot-humid outdoors 3 years
CIGS B	2	One each: light soak, biased dark soak	No, nascent

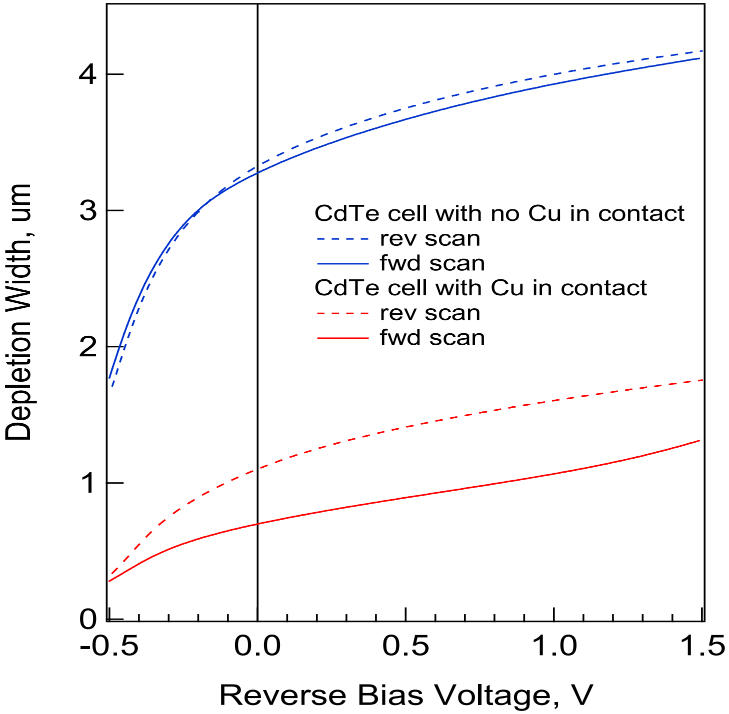
Module characterization tests

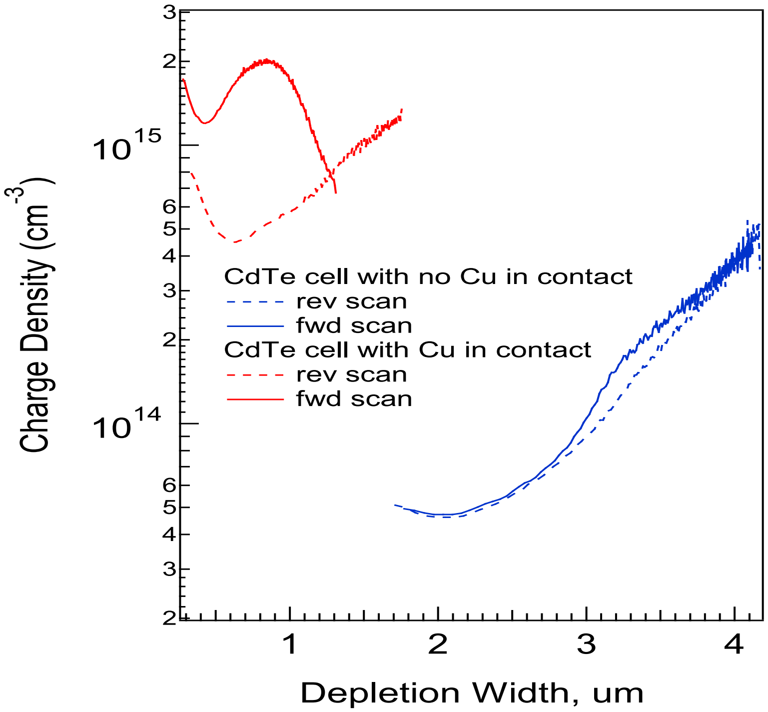
- ❑ I-V
  - ➢ Using large area continuous solar simulator (LACSS) apparatus
  - ➢ Dark & light (STC), part into reverse bias
    - ❖ Derive series resistances, shunt conductances, etc…, via standard diode analysis
- ❑ C-V profiling
  - ➢ Used precision HP 4284A LCR meter
  - ➢ If module cells are uniform, measuring C-V on module with Nc number of interconnected cells, produces signal as if the device under test were a cell sized 0.5-3 cm^2,
    - ❖ due to series connection & magnitude cancellation of cell area (Ac) & number (Nc)

$$\frac{1}{C_{Mod}} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_j} \ldots + \frac{1}{C_{Nc-1}} + \frac{1}{C_{Nc}} \quad \Rightarrow \quad C_{Mod} \approx \varepsilon \cdot \varepsilon_0 \cdot \frac{1}{w_D} \cdot \frac{A_C}{N_C} \qquad (1)$$

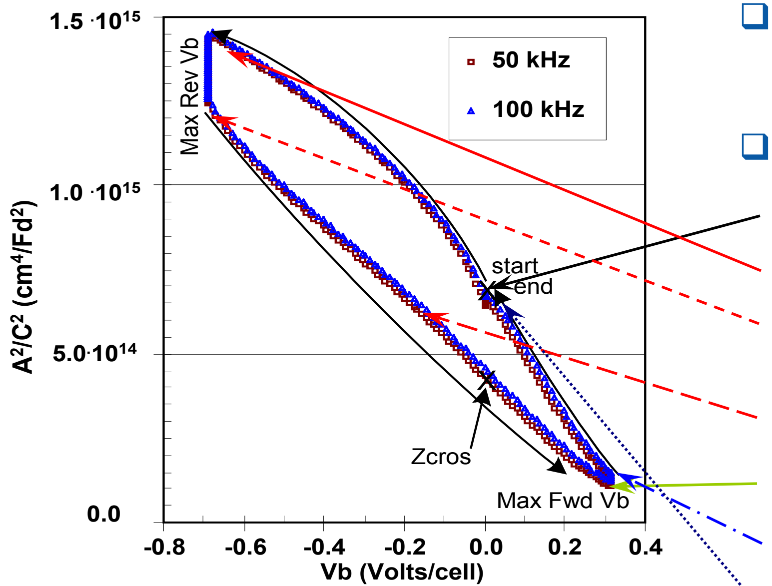
Value of C-V profiling CdTe cells

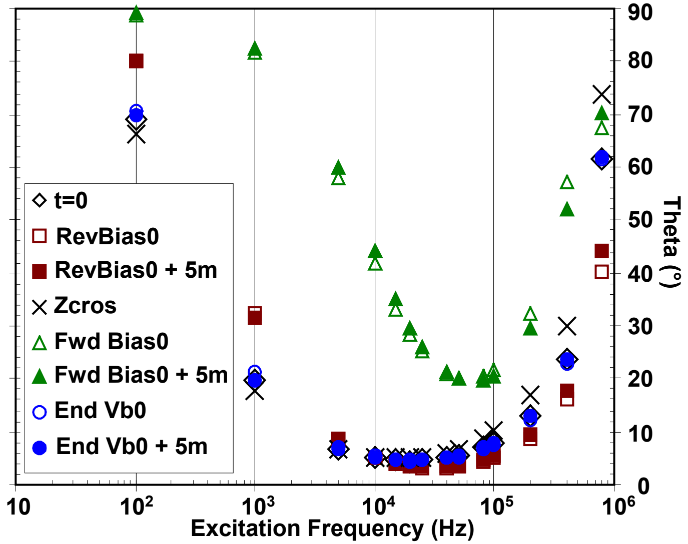
- ❑ Albin, D.S. et al., “Degradation and Capacitance-Voltage Hysteresis in CdTe Devices,” *ibid. these proceedings.*
- ❑ Hysteresis in depletion width vs. bias and derived carrier densities as one sweeps into reverse then up to forward bias appears correlated to amount of Cu in devices
  - ➢ No Cu in back contact ⇨ little hysteresis in C-V profile
  - ➢ Cu in back contact ⇨ hysteresis in depletion width between reverse & forward bias scans





C-V profiling on CIGS Module

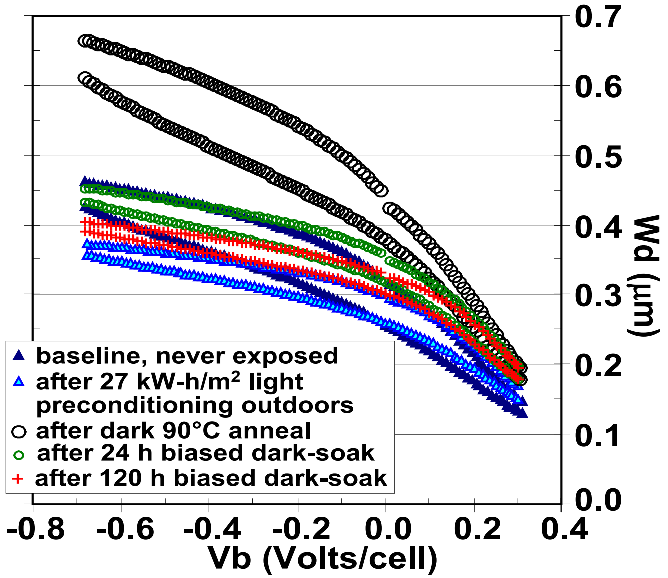


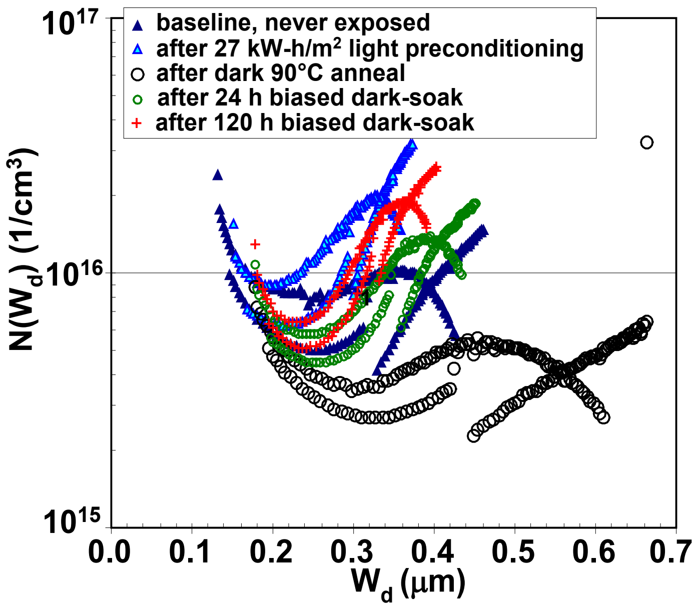


- ❑ Mott-Schottky plot upper graph
  - ➢ A^2/C^2 vs. Vbias
- ❑ C-V scan sweep details
  - ➢ Start Vb = 0
  - ➢ sweep to reverse bias, arrives at extrema
  - ➢ Vb dwells 5 mins. at extrema in reverse
  - ➢ sweep reverses to forward bias
  - ➢ Vb arrives at max fwd bias
  - ➢ Vb dwells 5 mins. at max fwd bias
  - ➢ sweep reverses & scans down to 0
  - ➢ dwell for 5 mins. at 0 bias
- ❑ Multiple C-V profiles run across broad span of frequencies 100 Hz-800 kHz, (lower graph) to determine location of best signal
  - ➢ best signal range ~ 50 – 100 kHz is $\Theta \leq 20^\circ$
  - ➢ Θ = angle between reactive component & total Z vector = arctangent of dissipation

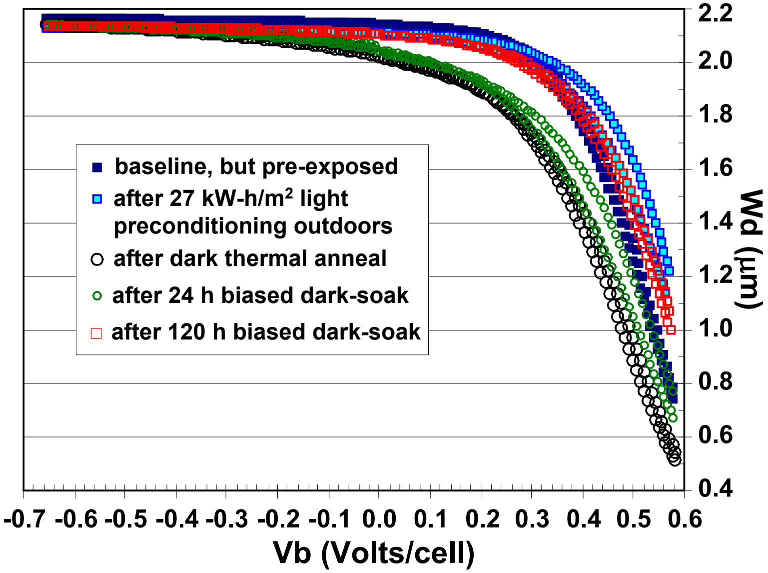
CIGS A module, biased dark exposure branch: carrier density & depletion width

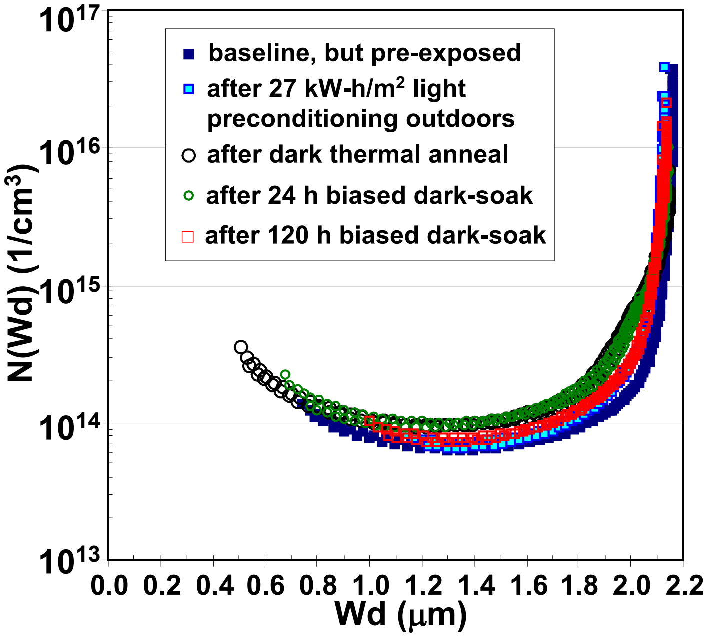
- Depletion width (*Wd) vs. Vbias* upper graph & carrier density (*N(Wd))* lower graph shown
  - Profiles at various stages of exposure: baseline, after precondition, after dark 90°C anneal, after 2 voltage-biased dark soaks
    - *Wd* profiles show variation & hysteresis
  - *Wd* hysteresis between measurements sweeping into reverse bias & then forward bias
    - ~16%-20% varying by exposure,
    - large increase in *Wd* and hysteresis after dark 90°C anneal
- *N(Wd)* Carrier densities
  - At baseline start near ~ $10^{16}/cm^3$
  - Increase preconditioning outdoor exposure
  - Collapse after dark 90°C anneal
  - Increase after 120 h biased dark soak 60°C back up to level after preconditioning exposure
- Similar changes for light-soaked CIGS A





CdTe C module, biased dark exposure branch: carrier density & depletion width





- Depletion width (*Wd vs. Vb* upper graph) & carrier density (*N(Wd)* lower graph) shown
    - Profiles at various stages of exposure, as in previous dark-soak example
- *Wd* profiles
    - Show less hysteresis ~5%-15% of total *Wd* and/or variations (as %) than CIGS during tests
    - larger & span larger range than for CIGS
    - Dark 90°C anneal lowers *Wd*
    - Post-anneal exposure brings profiles close to levels after preconditioning
- *N(Wd)* carrier densities
    - show small or modest variation with exposure and dark anneal
    - Minima ~just under 10^{14}/cm^3, consistent with Albin data for device with no Cu

CdTe A or B, light/dark exposure branches, depletion & carrier densities summarized, compared to CdTe C

- CdTe A
  - Depletion widths (*Wd)*
    - *Wd* vs. Vb profile changes and hysteresis are smallest of all CdTe
    - little changes on dark 90°C anneal
    - subsequent exposures (light/dark) bring *Wd* vs. Vb profiles close to where they were at baseline
  - Carrier densities
    - similar minima ~just under $10^{14}/cm^3$
    - mostly similar to B except spanned *Wd* is less than B modules
- CdTe B
  - Depletion widths (*Wd)*
    - *Wd* vs. Vb profiles show variations & hysteresis similar to C
    - somewhat larger than A
    - exhibit similar changes with dark 90°C anneal:
      - ✓ *Wd* values lowered, span vs. Vb larger
    - subsequent exposures raise & bring *Wd* vs. Vb profiles close to levels observed after preconditioning
  - Carrier densities
    - similar minima ~just under $10^{14}/cm^3$
    - mostly 10^{14}-10^{15}, for *Wd* 0.8-2 μm
    - Show similar variation with exposure
    - dark 90°C anneal has modest effect

Performance changes in CIGS A or B modules due to stabilization procedures

❑ I-V Changes plotted relative to baseline vs. 9 exposure categories

❑ initial preconditioning outdoor exposures increase performance of A1-A3, slightly drops that of B1,B2

❑ dark 90°C anneal substantially degrades performance ~5%-12%, largely due to FF & Voc losses

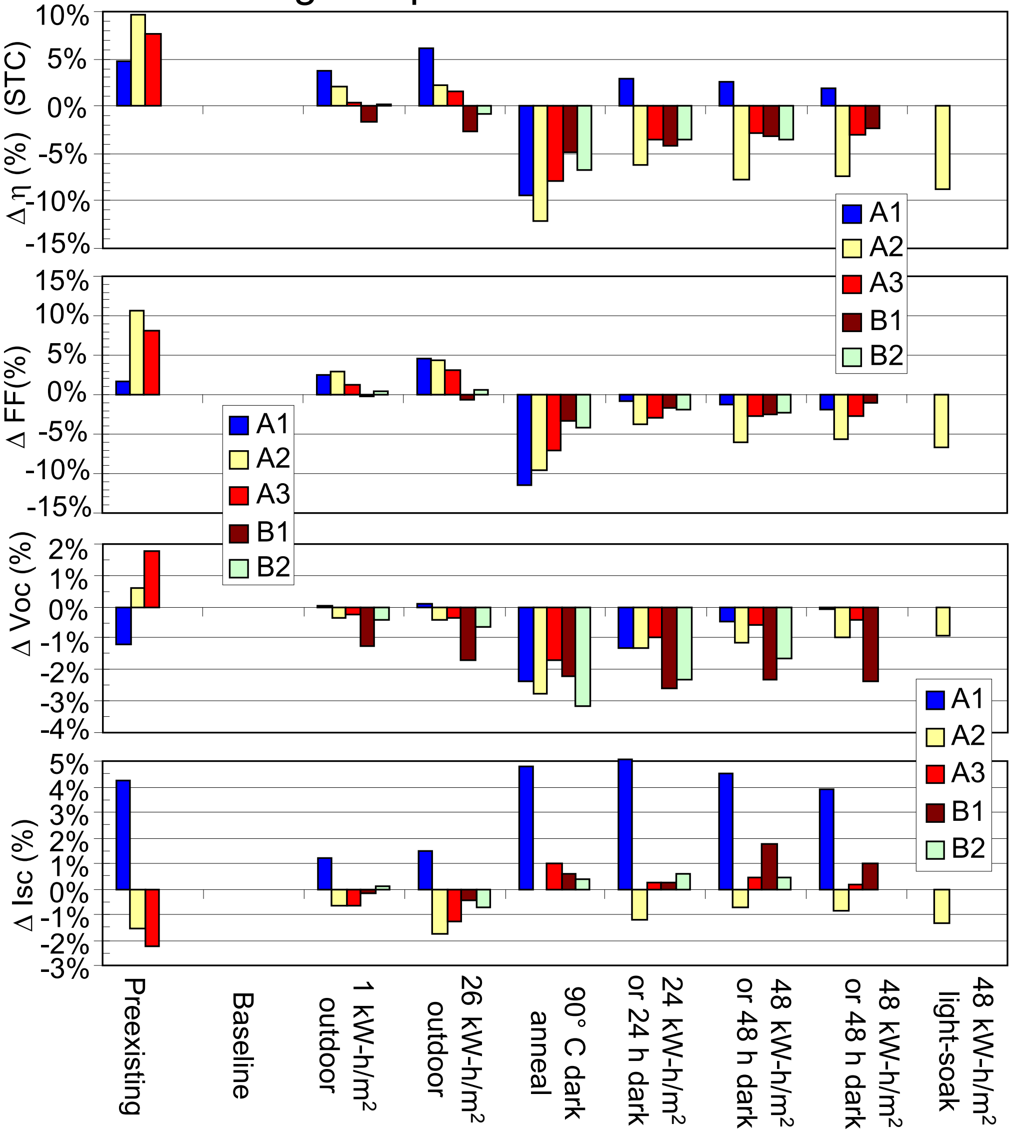
❑Subsequent light/dark soaks only mitigate losses from dark anneal ≤ ½

❑ Performance appear moderately stabilized after 3 exposures

- ➢ $\Delta\ \eta_{STC}$ < ~2% after 3 exposures post dark anneal
- ➢Light or dark exposures appear equally capable of driving toward stabilized η_{STC}

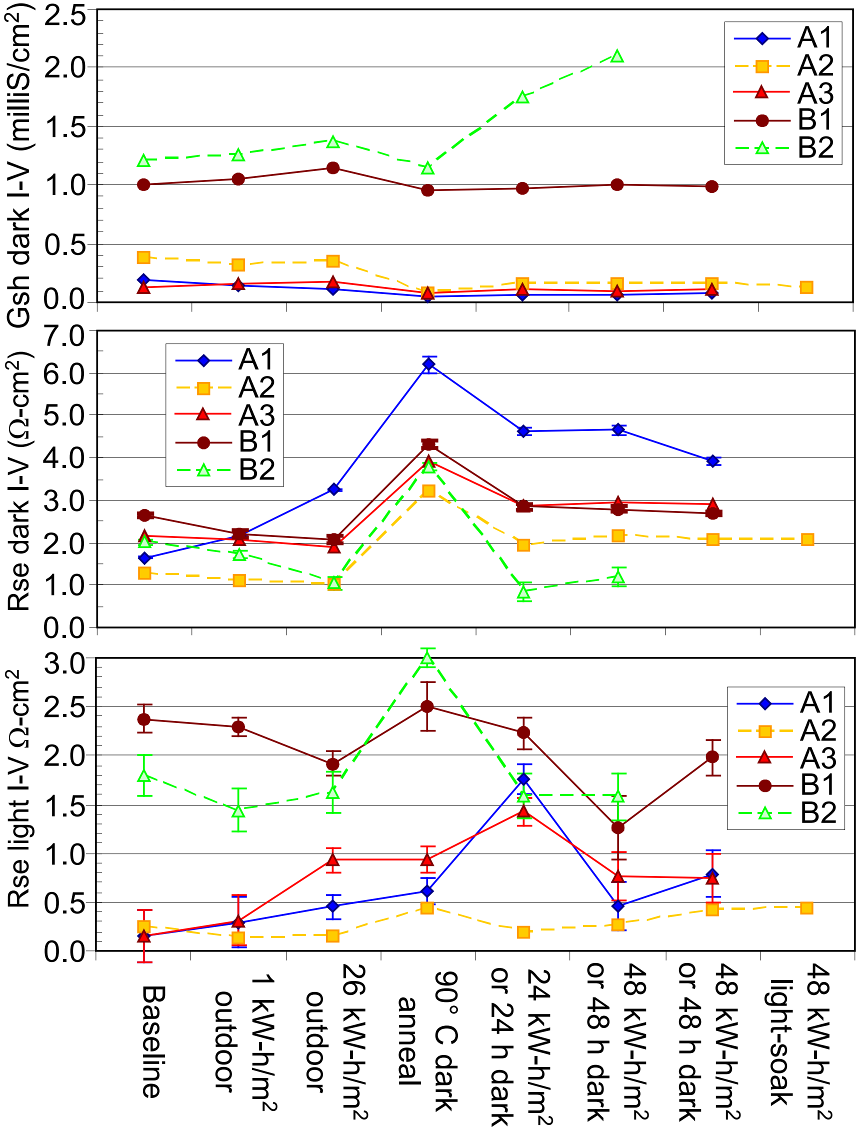
Module odd/even numbers & dark/light colors

⇔ dark/light exposures after dark 90 C anneal



Sources of performance changes in CIGS A or B modules due to stabilization procedures scrutinized

Module odd/even numbers & dark/light colors
⬄ dark/light exposures after dark 90 C anneal

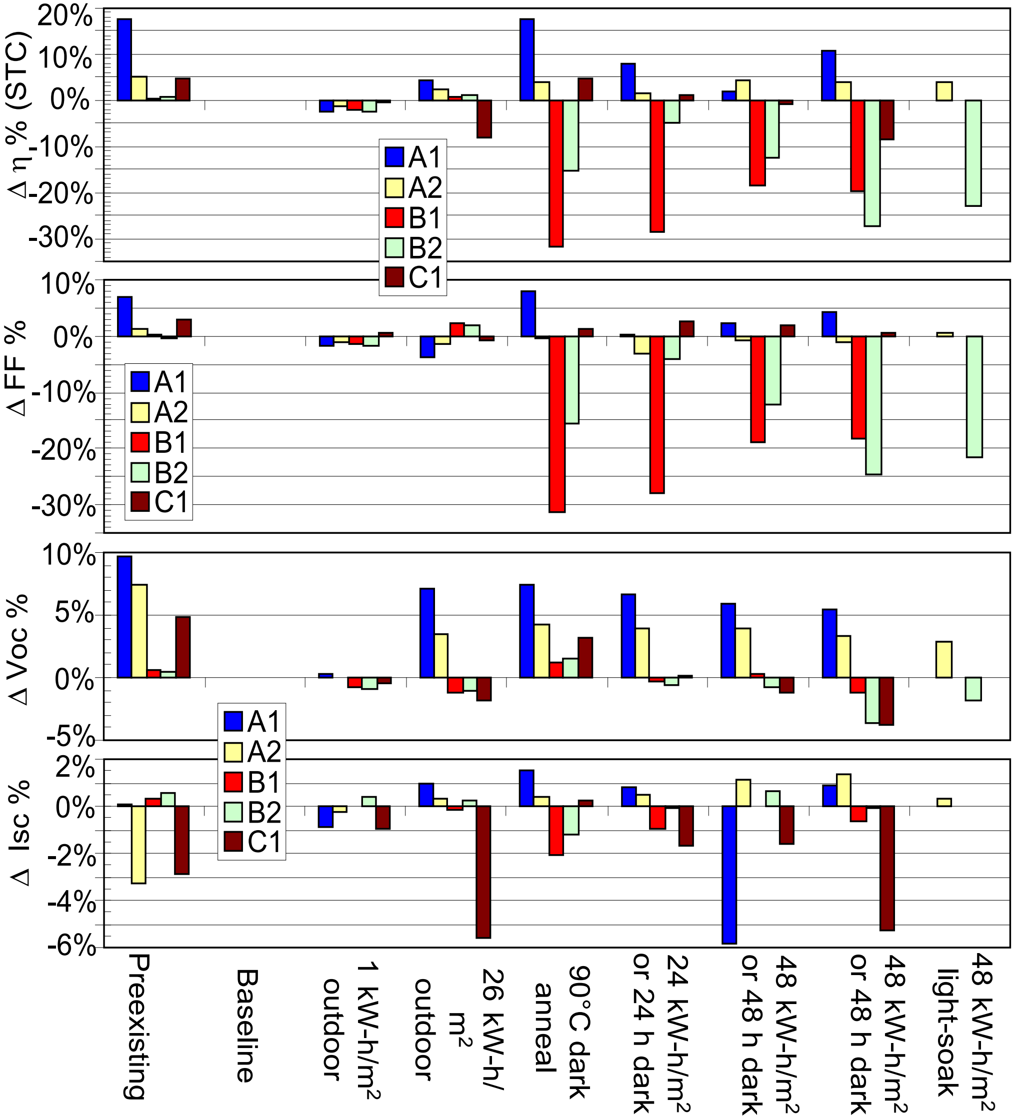


- ❑ Std. diode analysis for series resistance (Rse) & shunt conductance (Gsh)
- ❑ CIGS A
  - ➢ Rse dark/light increase after dark anneal,
    - ❖ Rse (dark) drop in subsequent exposures, but stay somewhat elevated
    - ❖ Rse (light) diminish in latter exposures, are fairly low at end (0.4-0.8 Ω-cm^2)
  - ➢ Gsh are relatively small and drop after dark anneal and all exposures
- ❑ CIGS B
  - ➢ Rse dark/light increase slightly or modestly after dark 90°C anneal, but diminish in subsequent exposures
  - ➢ Gsh increase for exposures after dark anneal for B2, but B1 shows no change after all exposures after dark anneal
    - ❖ somewhat larger than for CIGS A, may be more of source of FF loss

Performance changes in CdTe A, B, C modules due to stabilization procedures

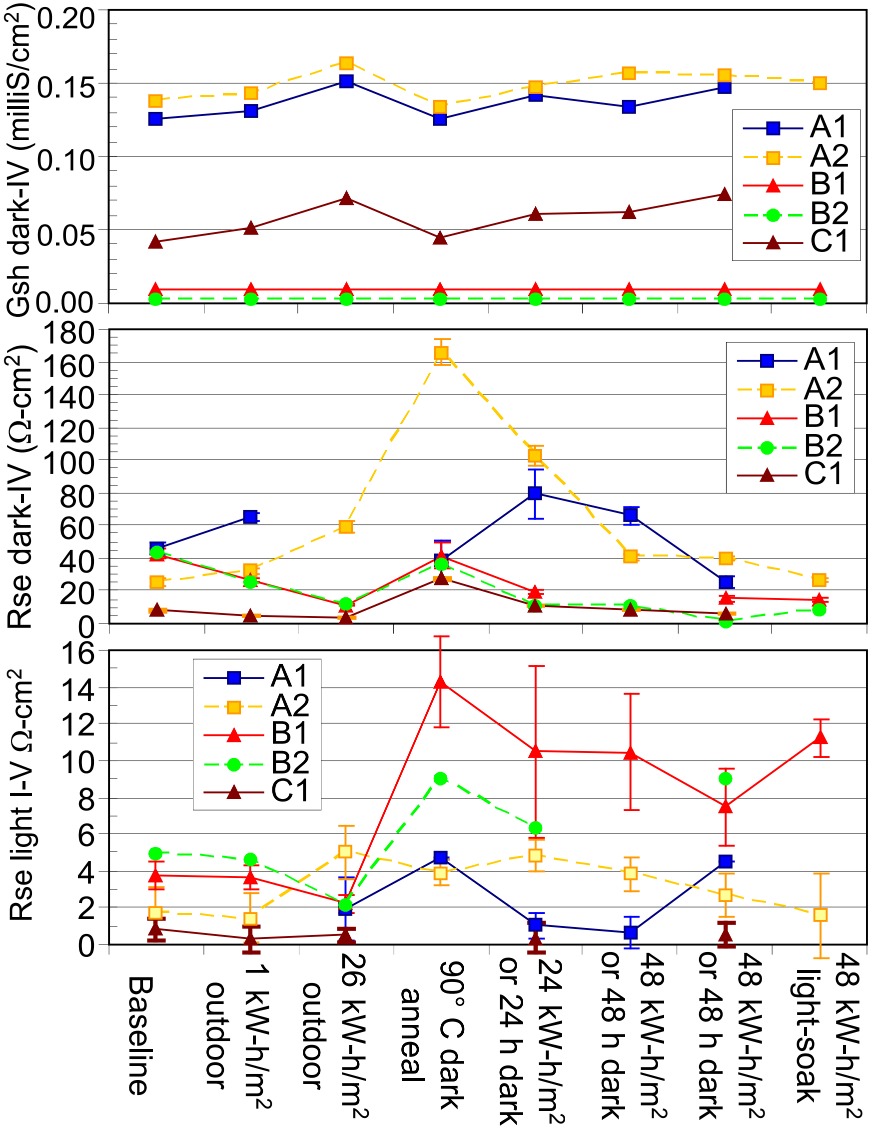
- Changes plotted relative to baseline
- initial preconditioning outdoor exposures result in small changes
- dark 90°C anneal
  - degrades performance of B's due to FF
  - recovers performance of A & C
  - increases Voc for all modules
- exposures subsequent to dark anneal
  - keep A1,A2 gains in dark/light exposures
  - B1 improves in dark soak, B2 improves at 1st then degrades in light soak
  - C1 slowly loses gains in dark-soak
- Performance ($\Delta\eta_{STC}$) post dark anneal
  - A2, B1 moderately stabilized ($\Delta\eta_{STC}$< 2%) after 3 exposures
  - rest not stabilized ($\Delta\eta_{STC}$ >2%)
  - dark exposures appear no worse than, & are equally capable of driving toward stabilized η_{STC} as light exposures

Module odd/even numbers & dark/light colors ⇔ dark/light exposures after dark 90 C anneal



Sources of performance changes in CdTe A, B, C modules due to stabilization procedures scrutinized

Module odd/even numbers & dark/light colors
⬄ dark/light exposures after dark 90 C anneal



- ❑ Std. diode analysis for Rse & Gsh

- ❑ all CdTe modules exhibit very low Gsh
  - ➢ ≤ 0.2 milliS/cm^2, Gsh not a problem at all

- ❑ Rse dark/light
  - ➢ CdTe A:
    - ❖ either slight change or increase initially
    - ❖ drop close to baseline or lower with subsequent exposures
  - ➢ CdTe B
    - ❖ Rse (light) increase dramatically after dark anneal & stay high in subsequent exposures
  - ➢ CdTe C
    - ❖ Rse not a problem
      - ✓ Rse dark increase after dark anneal but drop to lower than baseline in subsequent exposures
      - ✓ Rse light stay low (≤ 1 Ω-cm^2) throughout tests

Summary

- ❑ CIGS A & B (unexposed previously)
  - ➢ FF losses dominate
    - ❖ Rse increases are chief cause for loss in CIGS A,
      - ✓ reversible in exposures (light-soak and biased dark-soak) after dark 90°C anneal, so hard to reconcile that with TCO degradation
      - ✓ more consistent with in changes in semiconductor as shown by changes in C-V carrier densities during tests
    - ❖ Rse increases observed in CIGS B, appear somewhat reversible in subsequent exposures
    - ❖ Shunt losses likely more of problem for CIGS B
  - ➢ Voc loses also present for both A & B, ~2%-4%
  - ➢ Changes in and hysteresis in depletion width (C-V) suggest link to stability in CIGS A
    - ❖ not enough data measured for CIGS B

Summary

- ❑ CdTe A (pre-exposed)
  - ➢ Relatively stable during tests,
  - ➢ modest increases in performance after dark anneal and subsequent exposures
    - ❖ but efficiencies are always lower than for CdTe B even after CdTe B degraded
  - ➢ Voc increases after dark anneal
  - ➢ relative small changes in depletion width and hysteresis thereof during exposure tests is consistent with link to stability
- ❑ CdTe B (unexposed)
  - ➢ FF losses dominate after dark 90°C anneal
    - ❖ Rse (light) increases appears likely main mechanism
      - ✓ do not reverse substantially in subsequent exposures, maybe irreversible changes after dark 90°C anneal at OC
    - ❖ <u>efficiencies are fairly larger than CdTe A even after degradation</u>
  - ➢ larger changes in depletion width and hysteresis thereof during exposure tests consistent with link to stability
- ❑ CdTe C (pre-exposed)
  - ➢ Slight FF, Voc increases with dark anneal & first few subsequent exposures
  - ➢ Isc & Voc losses in latter exposures drop overall performance slightly
  - ➢ modest changes in depletion width and hysteresis thereof during exposure tests are somewhat consistent with the stability- depletion width link

Conclusions

- Devised stabilization / preconditioning study plan procedures that show promise in arriving at more stable performance values when implemented
  - Both types of exposure: light soaking at 1-sun & 60°C and voltage-biased dark-soaking at 60° C appear capable at driving similar performance changes for CdTe & CIGS
    - Have yet to more precisely quantify equivalency of exposure times between two types that produce stabilized performance values
  - C-V profiling and derived depletion widths changes plus hysteresis thereof likely provide valuable co-signature to potential metastability
    - details of hysteresis and link to stability is likely different for CdTe and CIGS

Acknowledgements

- Technical assistance and expertise with chambers & setup
  - Kent Terwilliger,
  - David Trudel,
  - Edward Gelak,
  - Jose Rodriguez
- This work was supported by the U.S. Department of Energy under Contract No. DOEAC36-08GO28308 with the National Renewable Energy Laboratory.