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Degradation and Capacitance-Voltage Hysteresis in CdTe Devices

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ABSTRACT

CdS/CdTe photovoltaic solar cells were made on two different transparent conducting oxide (TCO) structures in order to identify differences in fabrication, performance, and reliability. In one set of cells, chemical vapor deposition (CVD) was used to deposit a bi-layer TCO on Corning 7059 borosilicate glass consisting of a F-doped, conductive tin-oxide ($cSnO_2$) layer capped by an insulating (undoped), buffer ($iSnO_2$) layer. In the other set, a more advanced bi-layer structure consisting of sputtered cadmium stannate (Cd_2SnO_4; CTO) as the conducting layer and zinc stannate (Zn_2SnO_4; ZTO) as the buffer layer was used. CTO/ZTO substrates yielded higher performance devices however performance uniformity was worse due to possible strain effects associated with TCO layer fabrication. Cells using the SnO_2-based structure were only slightly lower in performance, but exhibited considerably greater performance uniformity. When subjected to accelerated lifetime testing (ALT) at 85 - 100 ºC under 1-sun illumination and open-circuit bias, more degradation was observed in CdTe cells deposited on the CTO/ZTO substrates. Considerable C-V hysteresis, defined as the depletion width difference between reverse and forward direction scans, was observed in all Cu-doped CdTe cells. These same effects can also be observed in thin-film modules. Hysteresis was observed to increase with increasing stress and degradation. The mechanism for hysteresis is discussed in terms of both an ionic-drift model and one involving majority carrier emission in the space-charge region (SCR). The increased generation of hysteresis observed in CdTe cells deposited on CTO/ZTO substrates suggests potential decomposition of these latter oxides when subjected to stress testing.

Keywords: CdTe solar cell, capacitance-voltage hysteresis, DLTS, transient ion drift, reliability, degradation

1. BACKGROUND

CdS/CdTe solar cell stability has been an important area of focus. The detrimental effects of localized shunts [1] and micro-nonuniformities [2], improved reliability by mitigating Cu diffusion using Te and O [3], the relative effects of different back contact structures [4], and most recently, the determination of degradation activation energies identifying both Cu and S diffusion [5] have been discussed. In the latter study, higher activation energy mechanisms were shown to dominate lower energy processes, e.g., the heavily studied effects associated with Cu diffusion. Degradation was shown to be stress temperature dependent (Fig. 1(a)). The lower degradation activation energy (E_a ~ 0.63 eV) measured at higher temperatures (100 – 120 ºC) was attributed to Cu-diffusion (E_a reported as 0.67 eV [6]) from the heavily Cu-doped back contact. The mechanism responsible for the higher measured activation energy (E_a ~ 2.94 eV) seen at lower temperatures (60 – 80 ºC) was perplexing until scanning electron microscopy (SEM) showed the formation of Kirkendall voids in the CdS with increasing stress. At this point, it was suggested that bulk S-diffusion (E_a reported as 2.8 eV [7]) into the CdTe from the CdS was responsible for this mechanism. Sulfur out-diffusion from the CdS layer also helped explain the results of a correlation analysis (Fig. 1(b)) in which changes in cell performance (η%) were plotted as a function of changes in 2nd level metrics (open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), and fill factor (FF).

As shown in Fig. 1(b), changes in performance were well-correlated (R^2 = 1 being perfect) with FF change at all temperatures. This correlation was observed to increase with increasing stress temperature. At a stress temperature of 120 ºC, nearly all (97.3%) the observed variation in efficiency could be explained by considering FF alone. Cu diffusion from the back contact was determined to be a major contributor to degradation. With shorter stress times, improvements in FF observed at all stress temperatures were quantitatively related by E_a = 0.67 eV. At higher temperatures, where degradation is dominated by Cu diffusion, increased space-charge recombination reduced V_{oc} and FF.

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The effects of sulfur out-diffusion are perhaps best understood by considering cells stressed at lower temperatures. The moderate correlation with J_{sc} seen at lower stress temperatures (where S diffusion dominates) decreases with increasing temperature. The performance change with J_{sc} in this case was not always negative, i.e., improvements in performance were correlated with improvements in J_{sc}. The latter improvements in J_{sc} could be due to the reduced optical attenuation presented by thinner CdS (i.e., due to S-outdiffusion). Thus, it is shown how an energetically less favorable (S diffusion with E_a ~ 2.8-2.9 eV) mechanism, can dominate more favorable ones (Cu diffusion; E_a ~0.63-0.67 eV), if in fact that mechanism occurs at a critical location in the cell (the junction in this case). We would even suggest, that degradation mechanisms originating at the junction are perhaps even more damaging than those that originate elsewhere (i.e., at the back contact).

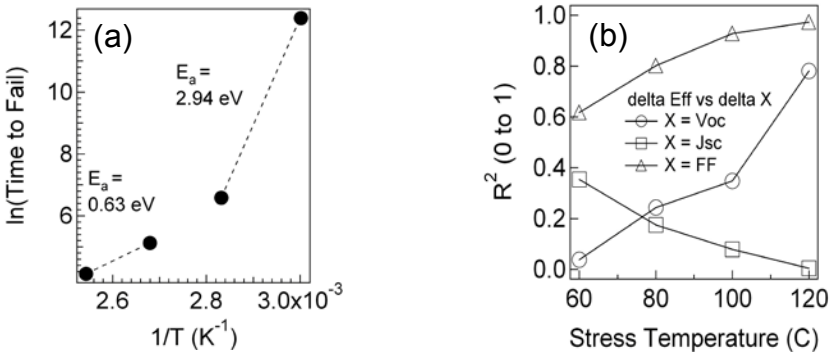

Figure 1. Arrhenius figure (a) showing two different activation energies associated with CdTe stress testing. Correlation data (b) pertaining to performance change (delta Eff) vs. changes in V_{oc}, J_{sc}, and FF as a function of stress temperature.

In ref [5], the CdS/CdTe cells were deposited by chemical bath deposition (CBD) and close spaced sublimation (CSS) respectively on Corning borosilicate (7059) glass substrates which had previously been coated by chemical-vapor deposited (CVD) SnO_2 using a tetramethyltin (TMT) precursor. The SnO_2 structure consisted of a bilayer configuration in which a F-doped, conductive $cSnO_2$ layer was deposited first, followed by an undoped, intrinsic, $iSnO_2$ buffer layer. In this paper, the stress tolerance of CdS/CdTe cells grown by identical semiconductor layer processes (and identical back contact fabrication) using both this TMT-CVD SnO_2 bilayer construction ($cSnO_2$/$iSnO_2$) and a more advanced, sputtered conducting Cd_2SnO_4 (CTO) and resistive Zn_2SnO_4 (ZTO) buffer layer will be discussed. The latter transparent-conducting-oxide (TCO) is arguably the most important technology partition (along with back contact variations) in the superstrate CdTe field. SnO_2 is a proven and cost-effective TCO while CTO/ZTO layers are well known to have yielded the highest CdS/CdTe starting cell efficiencies to date [8]. The relative performance metrics of CdS/CdTe cells using SnO_2 and the more advanced CTO/ZTO layers is shown in Fig. 2.

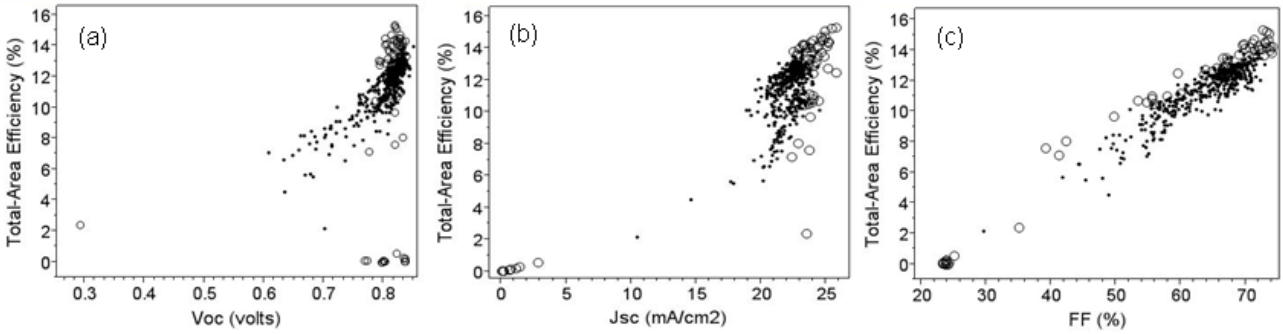

Figure 2. Total-Area Efficiency (%) vs. (a) V_{oc}, (b) J_{sc}, and (c) FF for CdS/CdTe cells fabricated from bilayer SnO_2 (dots) and CTO/ZTO (open-circles) transparent conducting oxide layers

The initial performance data shown in Figure 2 consists of a set of (447) SnO_2-based and (62) CTO/ZTO-based cells fabricated at NREL over the course of several years of research and reflects the variation in performance resulting from

routine variations in processing. Several comments are noteworthy. First, higher performance in CTO/ZTO cells is due to improvements in J_{sc} and FF only. There is no indication that V_{oc} improves when using the CTO/ZTO structure. In a CTO/ZTO/CdS/CdTe structure, the CdS layer is observed to diffuse into both the ZTO and CdTe layers while in $cSnO_2/iSnO_2$/CdS/CdTe structures, CdS diffuses primarily into the CdTe alone [8]. A major advantage of this enhanced interdiffusion is the increased adhesion the CdS/CdTe stack has to the substrate which allows higher $CdCl_2$ anneal temperatures and longer times. CdTe cells grown on CTO/ZTO substrates thus have considerably higher (~2.2 ns) minority carrier lifetimes than similar cells grown on SnO_2-based substrates (<1 ns). Another benefit related to increased interdiffusion is the resultant thinning of the CdS layer which can improve J_{sc}. The majority of the J_{sc} benefit however, is due to the higher transmission of the CTO/ZTO stack relative to $cSnO_2/iSnO_2$. Light transmission through the TCO/glass substrates alone can explain improvements in current of up to 1.5 mA/cm^2 when using CTO/ZTO-based substrates.

A final observation from Figure 2 is that CTO/ZTO cells can exhibit extremely poor performance that is rarely observed when using SnO_2-based TCOs. Some of these "outliers" will be discussed subsequently. Regardless, the use of CTO/ZTO layers obviously improves initial cell performance.

Though the initial benefits of CTO/ZTO TCO layers are well known, there is a paucity of knowledge concerning the relative stability of these materials when used in cells. In 2004, a preliminary determination of the dry heat stability (85 ºC, room-temperature humidity ~ 3% RH) of a number of CTO/ZTO and SnO_2-based CdTe cells was performed (CTO/ZTO cells provided by X. Wu). Uncertainty regarding whether these cells were optimized to minimize edge shunts prevented an open discussion of the results. Re-evaluation of that data, as well as its relevance to this paper, justifies presenting the results at this point.

Figure 3 shows the one-way analysis of variance (ANOVA) in degradation of V_{oc}, J_{sc}, FF, and η% (delta Voc, delta Jsc, delta FF, and delta Eff respectively) measured in 14 stressed CTO/ZTO and 7 SnO_2 based cells after 521 hrs of dry heat ALT.

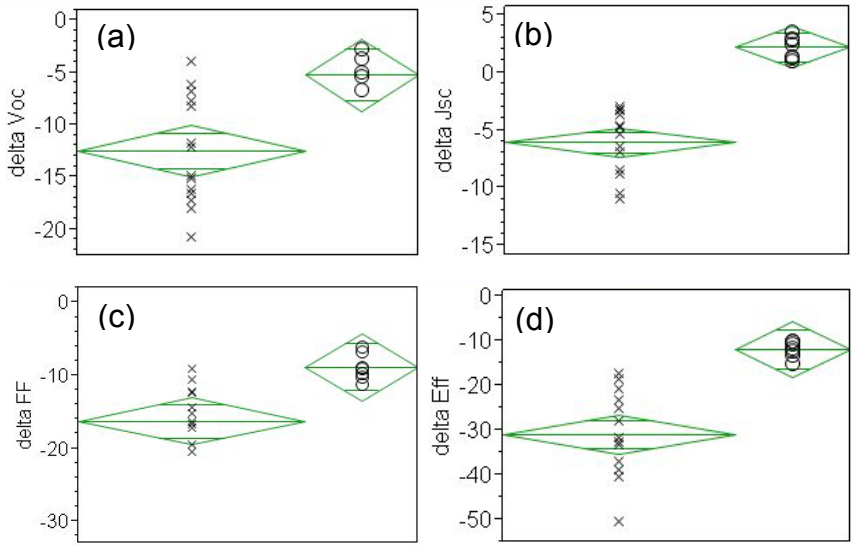

Figure 3. ANOVA of changes in (a) V_{oc}, (b) J_{sc}, (c) FF, and (d) η% measured during dry heat (85 ºC) stress testing of CdS/CdTe cells grown on CTO/ZTO (X's) and SnO_2-based (circles) substrates

The ANOVA "diamonds" represent group means (center horizontal line) and 95% confidence intervals (CI) of the mean (min and max vertical extent of the diamond) degradation observed in cells deposited on CTO/ZTO and SnO_2-based substrates. Statistically significant differences between groups (CTO/ZTO and SnO_2-based cells) exist when the 95% CIs do not overlap. After 521 hours, the mean change in V_{oc}, J_{sc}, FF, and η% for CTO-based cells were measured as -12.5%, -6.0 %, -16.2%, and -30.8% respectively. For SnO_2-based cells these same changes were -5.2%, +2.2%, -8.8%, and -11.6%. Differences in V_{oc}, J_{sc}, and η% degradation based on CTO-type were clearly shown to be significant. Shunting (determined by the inverse-slope of the current-voltage curve at V=0 in the dark) was only observed in 1 out of 14 CTO/ZTO cells after 521 hrs of stress and is therefore not relevant as originally suspected.

2. EXPERIMENTAL PROCEDURE

Techniques for depositing the CdS/CdTe layers were presented previously [9]. The basic structure is that of a borosilicate (7059) superstrate design in which light passes through a glass/TCO construction (either 7059/$cSnO_2$/$iSnO_2$ or 7059/CTO/ZTO), where it is then absorbed in the n-(CdS)/p-(CdTe) heterojunction. For this study, the chemical-bath deposited CdS layer thickness was ~ 80 nm while the CSS deposited CdTe thickness was ~ 8 μm. After the CdTe deposition, the finished structure was exposed to vapor $CdCl_2$ (VCC) in an oxygen/helium ambient (100 Torr O_2 + 400 Torr He). SnO_2-based cells were $CdCl_2$-treated at either 400 or 405 ºC for 5 m. CTO/ZTO-based cells were treated at either 400 ºC/5 m or 410 ºC/10 m. Prior to the back contact step, CdTe surfaces were treated with a NP etch in order to form a beneficial, Te-rich layer and to remove surface oxides [10]. Back contacts concluded with the application of a relatively thick layer (~50–100 μm) of graphite paste containing Cu_xTe and HgTe dopants followed by a similarly thick, final conducting layer of Ag paste. A narrow (~1 mm) margin of CdTe surrounding the perimeter of the dopant/Ag paste contact was used to reduce edge shunting.

SnO_2 layers were again grown by TMT-CVD. The $cSnO_2$ and $iSnO_2$ layers were 500 and 100 nm thick respectively. The resulting sheet resistance was measured at ~ 9 ohms/sq. The CTO and ZTO layers were sputtered onto unheated substrates to a thickness of 320 and 150 nm respectively. Conditions for sputtering these oxide layers can be found in ref [8]. After each sputter deposition, the oxide layer was annealed in 30 Torr He for 15 min at 650 ºC with the oxide film in contact with a CdS/borosilicate plate (i.e., a "close-proximity" anneal). This anneal has a pronounced effect on the CTO layer. There is a large structural change associated with the films transitioning from an amorphous to polycrystalline state. A large decrease in volume is observed, i.e., film thickness decreases by about 10%. The optical band gap of the CTO layer also increases from about 3.0 eV to 3.5 eV with a several order drop in resistivity to ~1.8 x 10^{-4} Ω·cm. The buffer layers were harder to characterize due to their thickness and high resistance. The $iSnO_2$ and ZTO layers (after anneal) have resistivities of about 1-10 Ω·cm and contribute little additional absorption loss to the oxide layer stack.

Performance data using standard current versus voltage (J-V) scans were made on cells after fabrication (t = 0) and during stress testing with a current-calibrated Oriel solar simulator. Capacitance-voltage (C-V) measurements (dark at room temperature) were performed on half the stressed cells using an Agilent 4294A Precision Impedance Analyzer operated manually at 100 kHz with a 50 mV oscillation voltage. Capacitance data was collected by scanning voltage in two directions. Immediately upon applying a voltage of +0.5 V forward bias, capacitance was measured as voltage was quickly swept (~3 s) in a "reverse" direction to -1.5 V where it was held for exactly 5 min. During the subsequent "forward" sweep back to +0.5 V, capacitance data was again collected. C-V data for these two directions will subsequently be referred to as "rev" and "fwd" scans. The rationale for using "two-way" directional scans will be discussed shortly.

Accelerated lifetime test (ALT) conditions have been described before [5]. In short, cells were placed, glass-side up, under an Atlas CPS+ solar light source (~AM 1.5; 1-sun) in machined Al blocks designed to keep the cells at V_{oc} bias. Cell temperature was set at 100 ºC. At times equal to 1, 4.4, 10, 28, 73, and 115 hrs cells were removed and allowed to relax in the dark for 12-24 hrs. After quick measurements of J-V and C-V, cells were again placed under stress. Sometime after the last measurement at T=115 hrs, the temperature controllers failed (over a weekend) resulting in excessive heating and destruction of cells. The actual test temperature of 100 ºC is suspect (temperatures may have been higher) particularly near the conclusion of the test. Regardless, the design of the Al blocks at least assures us that cells were tested at the same temperature.

3. RESULTS AND DISCUSSION

The performance of cells fabricated for this study at t = 0 (initial data) is shown in Table 1. Two different CTO/ZTO and $cSnO_2$/$iSnO_2$ substrates were used and are appended "_1" & "_2". Each substrate was approximately 1.5" x 1.5" in size and provided 8 individual cells. The uniformity in performance of the cells grown on the SnO_2-based substrates was very good as expected. The mean values for V_{oc}, J_{sc}, FF, and η% as a function of $CdCl_2$ temperature (400 ºC vs. 405 ºC) were 0.824 vs. 0.830 volts, 22.7 vs. 23.1 mA/cm^2, 69.9 vs. 70.7 %, and 13.1 and 13.6 % respectively. ANOVA differences in all but FF were statistically significant at the 95% confidence level. A similar analysis between

"_1" and "_2" substrates showed no difference between substrate. The uniformity in performance for the cells grown on the CTO/ZTO substrates was considerably worse. Cells grown on the CTO/ZTO_1 substrate were nearly all dead due to essentially no current. For the cells grown on CTO/ZTO_2, FF appears to be the primary reason for performance variation. This CTO/ZTO substrate yielded the highest efficiency cell of the study (η% = 14.5%)

Dev ID	Substrate	VCC_T (ºC)	VCC_t (m)	Voc (volts)	Jsc (mA/cm2)	FF (%)	η% (%)	ALT	CV
T452_A1	CTO/ZTO_1	410	10	0.768	0.6	24.2	0.1		
T452_A2	CTO/ZTO_1	410	10	0.799	0.7	23.8	0.1		
T452_B1	CTO/ZTO_1	410	10	0.821	2.8	25.1	0.6		
T452_B2	CTO/ZTO_1	410	10	0.772	0.6	23.3	0.1		
T452_C1	CTO/ZTO_1	400	5	0.801	0.1	23.9	0.0		
T452_C2	CTO/ZTO_1	400	5	0.803	0.2	23.4	0.0		
T452_D1	CTO/ZTO_1	400	5	0.796	0.0	24.1	0.0		
T452_D2	CTO/ZTO_1	400	5	0.799	0.0	23.6	0.0		
T453_A1	CTO/ZTO_2	410	10	0.823	24.5	53.3	10.7		
T453_A2	CTO/ZTO_2	410	10	0.829	24.0	55.5	11.0		
T453_B1	CTO/ZTO_2	410	10	0.825	24.4	67.1	13.5	X	X
T453_B2	CTO/ZTO_2	410	10	0.827	24.6	71.1	14.5	X	X
T453_C1	CTO/ZTO_2	400	5	0.795	23.7	55.8	10.5		
T453_C2	CTO/ZTO_2	400	5	0.795	23.7	69.0	13.0		
T453_D1	CTO/ZTO_2	400	5	0.806	24.2	67.2	13.1	X	
T453_D2	CTO/ZTO_2	400	5	0.809	23.9	70.5	13.6	X	
T454_A1	nSnO2/iSnO2_1	405	5	0.832	23.1	69.9	13.4		
T454_A2	nSnO2/iSnO2_1	405	5	0.830	23.0	72.0	13.7		
T454_B1	nSnO2/iSnO2_1	405	5	0.830	23.1	69.5	13.4		
T454_B2	nSnO2/iSnO2_1	405	5	0.832	23.2	71.8	13.8		
T454_C1	nSnO2/iSnO2_1	400	5	0.818	22.6	66.8	12.3		
T454_C2	nSnO2/iSnO2_1	400	5	0.823	22.6	70.8	13.2		
T454_D1	nSnO2/iSnO2_1	400	5	0.826	22.8	69.1	13.0	X	X
T454_D2	nSnO2/iSnO2_1	400	5	0.830	22.6	72.0	13.5	X	X
T455_A1	nSnO2/iSnO2_2	405	5	0.832	23.1	69.8	13.4		
T455_A2	nSnO2/iSnO2_2	405	5	0.825	23.2	70.7	13.5		
T455_B1	nSnO2/iSnO2_2	405	5	0.830	23.3	70.4	13.6	X	
T455_B2	nSnO2/iSnO2_2	405	5	0.829	23.3	71.6	13.8	X	
T455_C1	nSnO2/iSnO2_2	400	5	0.823	22.9	68.7	13.0		
T455_C2	nSnO2/iSnO2_2	400	5	0.824	22.6	71.3	13.3		
T455_D1	nSnO2/iSnO2_2	400	5	0.824	22.9	69.5	13.1		
T455_D2	nSnO2/iSnO2_2	400	5	0.822	22.3	71.0	13.0		

Table 1. Initial (t=0) cell performance metrics

Figure 4 shows the J-V curves for one of the "dead" cells grown on CTO/ZTO_1 (T452_A1) compared with two cells from CTO/ZTO_2 showing the wide variation in performance (T453_A1 and T453_B2) observed when using this particular CTO/ZTO substrate.

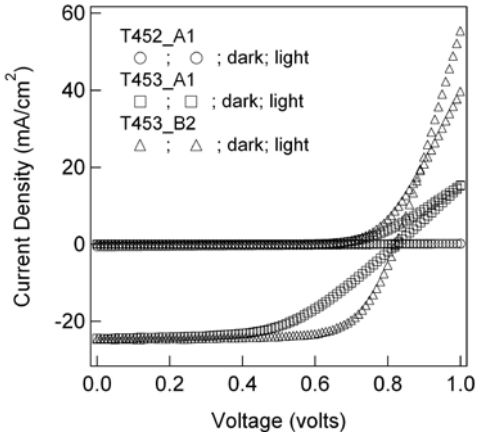

Figure 4. Initial (t=0) J-V characteristics for CTO/ZTO cells

Series resistance, R_s, is obviously the reason for the large variation in initial cell performance for these CTO/ZTO cells. In our experience, such a large variation in initial cell performance among cells that have been identically processed had never been seen when using SnO_2-based substrates, which indicates the R_s variation is purely specific to the CTO/ZTO substrates alone. At first glance, the root cause would not appear to be CTO compositional fluctuations. According to the combinatorial study by Li et al. [11], resistivity varies less than an order magnitude across the entire CdO-SnO_2 pseudobinary. Though these films were deposited by CVD, this suggests that the observed variations in R_s are not due to compositional variations. Also, since the ZTO thickness is only 150 nm thick, even magnitude changes in buffer layer resistivity should not impact R_s in these devices. Typical values for cell R_s are on the order of 1-2 $\Omega \cdot cm^2$ [5]. The contribution to R_s for a 150 nm thick ZTO layer with resistivity of 10 $\Omega \cdot cm$ is only 1.5 x 10^{-4} $\Omega \cdot cm^2$. Rather, examination of devices under an optical microscope show that very small "micro" cracks in the CTO were likely responsible for very high conductive *sheet* resistance, and thus, high R_s. The origin of this "cracking" is currently under investigation. One possibility is the strain introduced by volume shrinkage during the 650 ºC post-deposition anneal.

Because of these problems with CTO/ZTO uniformity, the number of cells for available stress testing was greatly reduced. Table 1 identifies the (4) CTO/ZTO and (4) $cSnO_2$/$iSnO_2$ cells that were subsequently chosen for stress testing (ALT). J-V measurements were performed on all stressed cells, while C-V measurements (also indicated in Table 1) were performed on half this set.

The variation in performance metrics during ALT are shown in Figure 5. Changes in performance are normalized to measurements performed at t=0 (initial data). All data for stressed CTO/ZTO (solid lines) and SnO_2 (dashed lines) based cells are shown in Figure 5. Data with symbols correspond to cells in which additional C-V measurements were made. As discussed previously, decreases in performance correlated well with decreases in FF. In general, Figure 5 shows more degradation in cells using the CTO/ZTO layers corroborating the earlier study performed in 2004. However, the J-V curves show that the mechanism of degradation appears to be different relative to the earlier study.

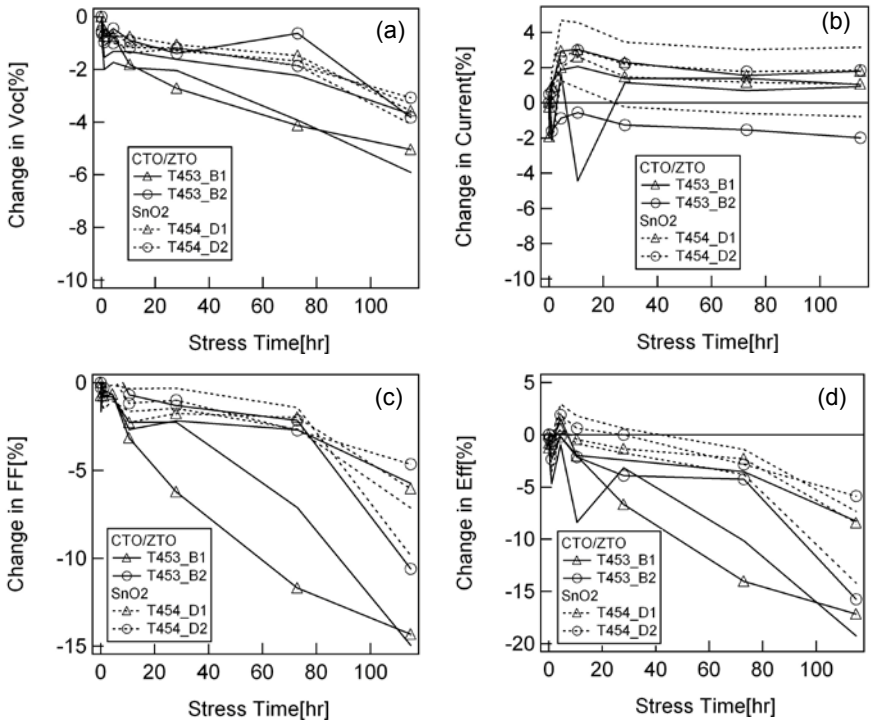

Figure 5. Percent changes in (a) V_{oc}, (b) J_{sc}, (c) FF, and (d) η% during ALT at T~100 ºC

Figure 6 compares very representative J-V curve changes with stress for CTO/ZTO cells from these two independent studies. CTO/ZTO cells made in this study show considerably less V_{oc} degradation than those from the earlier study. Large initial drops in V_{oc} (~15-20%) were observed in all 14 CTO/ZTO cells from the 2004 study at which point, degradation shifted to one involving a decrease in FF. No such shift in degradation was observed in this study.

Rather, both V_{oc} and FF appear to degrade concurrently. Also, the overall degradation observed in the 2004 study was considerably more even though a lower stress temperature was used. After 100 hrs of stress, the overall performance of CTO/ZTO cells from the 2004 study (T = 85 ºC) had decreased approximately 20-30% while in this study (T = 100 ºC), the drop in performance was only about 15-20%.

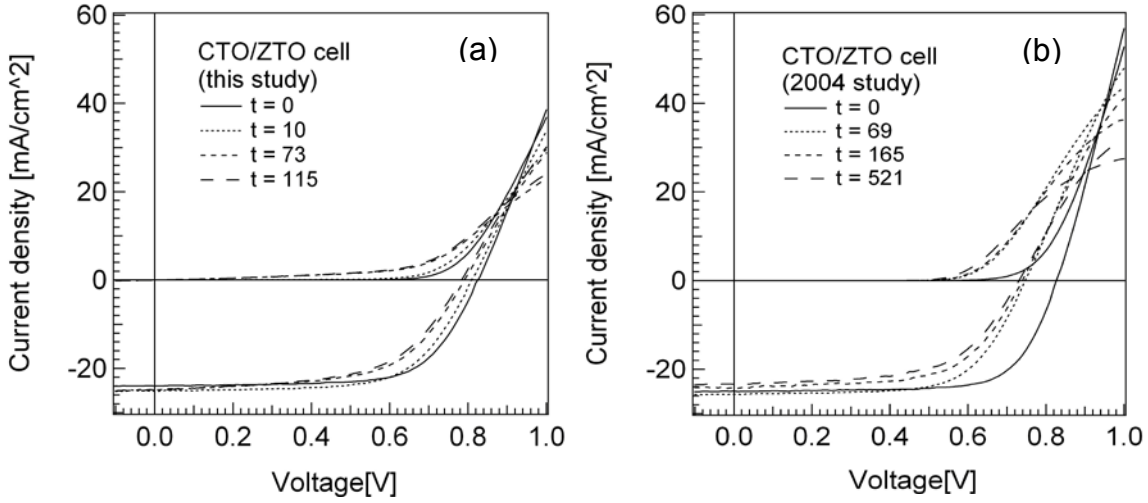

Figure 6. Representative changes in J-V data with stress time (t in hours) observed in this (a) and the earlier 2004 (b) ALT study of CdTe cells grown on CTO/ZTO substrates

In addition to differences in V_{oc} and FF degradation, increased shunting with stress was observed in (3) out of (4) CTO/ZTO cells stressed in this study while only (1) out of (14) cells from the 2004 study showed any increase in shunt resistance. The lack of any significant increase in R_s for the cells from either study also implies that the R_s non-uniformity observed in the as-grown (t=0) case was a function purely of fabrication and not a stability concern.

Since details concerning the fabrication of the earlier CTO/ZTO cells measured in 2004 were incomplete, it is difficult to ascertain why these cells degraded differently. In the present study, the CdS film was grown by CBD. It is not clear whether this was the case for the earlier study. One known difference between these sets of devices concerns the CSS CdTe deposition itself. In this study, H_2 anneals of the glass/CTO/ZTO/CdS stack prior to CdTe deposition were avoided. This was based upon previous knowledge that H_2 anneals were potentially detrimental to SnO_2-based substrates [12]. Indeed the highest efficiency achieved at NREL using a SnO_2-based substrate (V_{oc} = 0.83 Volts, J_{sc} = 24.7 mA/cm$_2$, FF = 74.8, and η% = 15.4) used a CdTe deposition process intentionally modified to avoid this H_2 anneal step [9]. In the earlier 2004 ALT study, it is almost certain that H_2 anneals were used prior to the CSS CdTe deposition since these anneals do not appear to impact the initial performance of CTO/ZTO cells.

It is clear that cell processing has a profound affect not only on the rate of degradation but also on how it manifests. This is important. One should not consider degradation as purely representative of the materials involved. One also needs to consider the more subtle details associated with fabrication, and possibly, the techniques used to deposit those layers. This point is even more poignant when considering the results shown in ref [12]. In this study, the susceptibility of SnO_2-based layers to reduction in H_2 was demonstrated to be process dependent. SnO_2 films sputtered onto unheated substrates were more prone to reduction than similar materials deposited by CVD onto heated substrates.

This paper will now conclude with a discussion of features observed in C-V measurements made during ALT. C-V is commonly used to determine doping profiles in solar cells. Historically, they have also been used to quantify mobile ionic charge, particularly Na^+, Li^+, and K^+ in the dielectric SiO_2 layer of metal-oxide field effect devices, by measuring field-induced, C-V hysteresis [13]. More recently, capacitance transients were used by Enzenroth et al. [14] and Lyubomirsky, et al. [15] to determine the diffusion parameters of mobile ions in CdTe and $CuInSe_2$ cells and materials based upon a transient ion drift (TID) technique developed by Heiser and Mesli [16]. In particular, Enzenroth et al., used the TID approach to associate an increase in mobile Cu_i^+ as a function of Cu added during cell fabrication. C-V measurements are also, now being used to study transients in monolithic, series-connected CdTe and $CuInSe_2$-based thin film modules [17]. C-V hysteresis in modules is not only relevant to understanding product reliability, but also in developing pre-measurement, stabilization procedures for base lining the performance of these products.

In order to capture some of the potential ramifications of C-V hysteresis in this study, we elected to collect C-V data during ALT using both rev (+0.5 V to -1.5 V) and fwd (-1.5V to +0.5V) scans. A key requirement of any measurement made during ALT is that the measurement be quick enough so as not to introduce unintentional relaxation effects during long-term stress testing. Another requirement is that the technique "does no harm". The "two-way" scan C-V approach described earlier is quick, requiring ~ 10 min. to perform for each cell tested which made it amenable to measurements performed as part of a basic ALT protocol. Also, because cell bias is maintained constant only during negative voltages, potentially damaging forward currents at positive bias (and possible cell damage due to heating) were minimized. Finally, the technique is performed at room temperature. Since ALT measurements traditionally use temperature as an accelerant, any quantification of performance change during ALT should avoid thermal heating, and possibly cooling. In retrospect, a more useful two-direction scan technique might avoid the use of forward-bias entirely. An explanation for this will be presented in due course.

Representative C-V data collected as a function of scan direction is shown in Figure 7 below for cells made when both Cu is added and not added as a constituent of the graphite paste contact respectively. Figure 7(a) displays the charge density as a function of depletion width, W_d that would be calculated from C-V data assuming the commonly used, one-sided, n+/p junction model (Mott-Schottky plot). Figure 7(b) is the same data showing only W_d plotted as a function of reverse-bias. In the latter case, no junction model is assumed as W_d is inversely proportional to the measured capacitance, and thus, is a "purer" representation of the data.

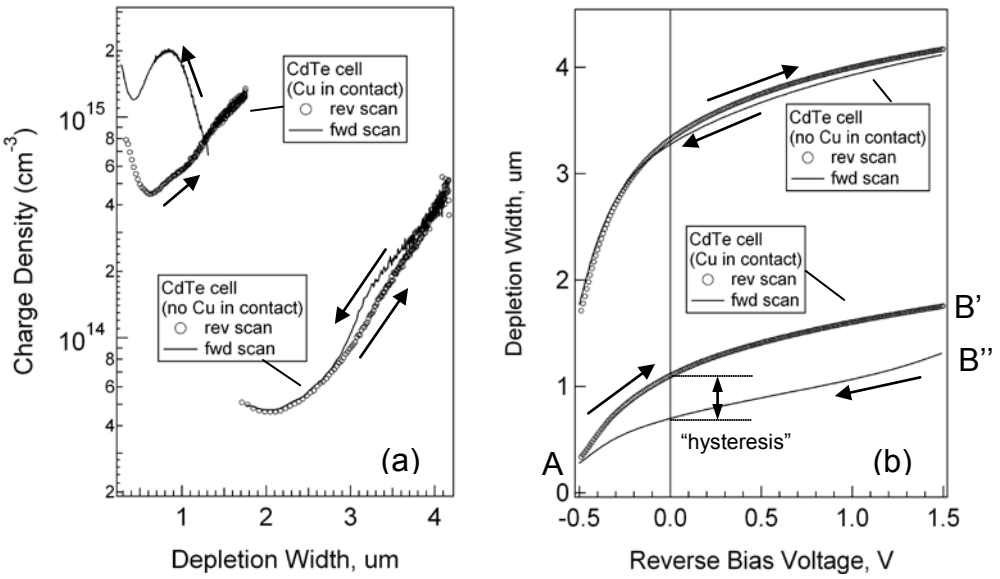

Figure 7. C-V data plotted assuming a 1-sided junction (a) showing charge density vs. depletion width, and (b) as simply depletion width vs. reverse bias voltage.

Figure 7 clearly demonstrates how the introduction of Cu into CdTe as a function of cell fabrication affects the space-charge region (SCR). The strong decrease in W_d (as Cu is added) reflects an increase in ionized acceptor concentration, N_a^- in the CdTe possibly as Cu_{Cd} or as a paired, defect complex. Ref [15] discusses many of the defects (both acceptor and donor-like) that may form. The decrease in W_d, since it can be so easily explained by active doping, is not too surprising. What is less obvious is the large degree of hysteresis associated with the introduction of Cu. When Cu is not intentionally added (i.e., Cu is well-known to be a naturally occurring, trace impurity in CdTe), we see little indication of hysteresis within the accuracy of the measurement technique. This has been confirmed in every cell made in which Cu was intentionally absent. The presence of Cu introduces significant hysteresis in which W_d measured during the second (fwd) scan is always lower than the value of W_d determined during the first (rev) scan. Hysteresis in C-V measurements on polycrystalline thin film cells has also been reported by others [18, 19] in which the authors associated hysteresis with the presence of deep states.

The TID explanation for the hysteresis proceeds as follows. The cell is biased in the dark at point A (+0.5V forward bias) in Figure 7. The bias is immediately decreased to -1.5V (point B'; reverse bias) and the C-V data collected. In this

sense, we are effectively probing the cell SCR with any mobile ions (presumably Cu_i^+) in an "equilibrium" or "relaxed" state. At point B', the cell bias of -1.5V is held for exactly 5 min. During this time, the capacitance is observed to increase, with a corresponding decrease in W_d (point B''). The TID model suggests that as Cu_i^+ (a donor-like defect) moves towards the back contact, the screening effect it has on negatively-charged, ionized acceptors is removed such that the SCR charge density must increase, and W_d decrease in order to maintain charge-neutrality. Thus, the change in depletion width can be explained by assuming mobile, positively charged ions.

From an electronic perspective, the same C-V hysteresis can be explained by considering majority carrier trap emission within the CdTe space-charge. This effect is shown in Figure 8, in which reverse-bias results in the raising of electron energies in the CdTe relative to the window (n) layers.

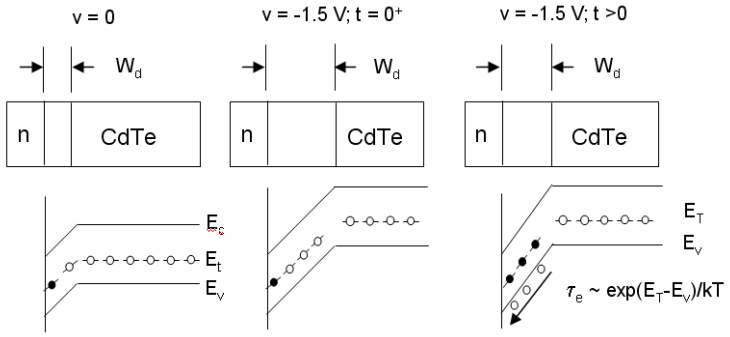

Figure 8. CdS/CdTe band structure during voltage sweep v = 0 (left) to v = -1.5V at $t = 0^+$ (middle) and t > 0 (right). The depletion width initially increases then decreases as holes are emitted from the CdTe space-charge region.

When the cell bias is changed from v = 0 to a reverse bias as shown in Figure 8, the depletion width increases since the negative-charge of the SCR is initially screened, not by mobile Cu_i^+ ions, but rather by holes initially occupying deep states in the CdTe. Given adequate time, these holes are emitted into the valence band where they are quickly removed by the field. Cell capacitance increases with time as holes are emitted, and again, W_d decreases. The hole emission relaxation time τ_{em} associated with this capacitance increase is given by [20]:

$$\tau_{em} = \frac{\exp\left[\left(E_T - E_V\right)/kT\right]}{\sigma_p \upsilon_{th} N_V} \qquad (1)$$

where E_T and E_V are the trap and valence band energies, σ_p and υ_p are the hole capture cross section and thermal velocity respectively, and N_V is the valence band density of states. Note that for large values of $E_T - E_V$ (expected in wide band gap materials like CdTe) relaxation times on the order of minutes are possible.

Relaxation times associated with the capacitance increase from B' to B'' shown in Figure 7 are this order of magnitude. Figure 9 shows a characteristic relaxation curve typical of how capacitance increases at point B.

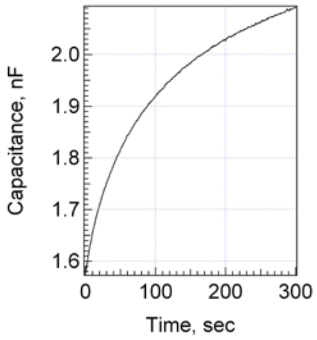

Figure 9. Typical capacitance relaxation observed when holding cells at a reverse-bias of – 1.5 V reflected as a decrease in W_d (Figure 7) pt B'→ B''.

At this point, we have two plausible explanations for the C-V hysteresis observed in this study. Each is based upon a different mechanism. The TID approach [16] associates the magnitude of hysteresis with an increase in free ions within the CdTe. The electronic model implies an increase in deep states with increasing hysteresis. Fortunately, techniques for discerning these two mechanisms have been suggested. For example, the ratio of relaxation times associated with the capacitance change during zero-bias and reverse-bias states (what is referred to as ionic filling and accumulation in [16]) should equal the ratio (qV_{rev}/kT) where V_{rev} is the reverse-bias applied to the cell. This ratio should be much greater than unity. This determination however requires C-V voltages ≤ 0 volts, i.e., ion motion is field-assisted only during the reverse-bias. Another way to assert ionic behavior is to determine the voltage dependence of relaxation when changing the cell bias from V_{rev} to zero. For ionic effects, the relaxation time should be a function of reverse-bias as ions are forced to thermally diffuse longer distances. This is argued as not being so for electronic processes.

In two studies involving both CdTe films [14] and single crystals [15], data was given to suggest the validity of Cu_i^+ ion migration as responsible for C-V hysteresis. In retrospect, the two-direction C-V scan technique used to monitor degradation in this study should have avoided positive voltages. A better procedure would have involved using voltage scans between 0 volts and different reverse-biases while also measuring the capacitance transient at each extreme point. Such a technique would allow for better interpretation of the data while at the same time not compromising the integrity of the ALT study. Positive voltages inject minority carriers into the CdTe which complicates the data analysis. Though useful for Mott-Schottky studies, positive biases are not necessary for determining either trap or mobile ion concentrations.

In order to quantify the observed changes in C-V during ALT, we arbitrarily define the C-V hysteresis obtained in our measurements as the difference in depletion width observed at v = 0, i.e., $W_{d,rev} - W_{d,fwd}$ as shown in Figure 7. A plot of this value with stress (Figure 10) for the cells whose general degradation characteristics are shown in Figure 5 shows an interesting correlation with performance degradation.

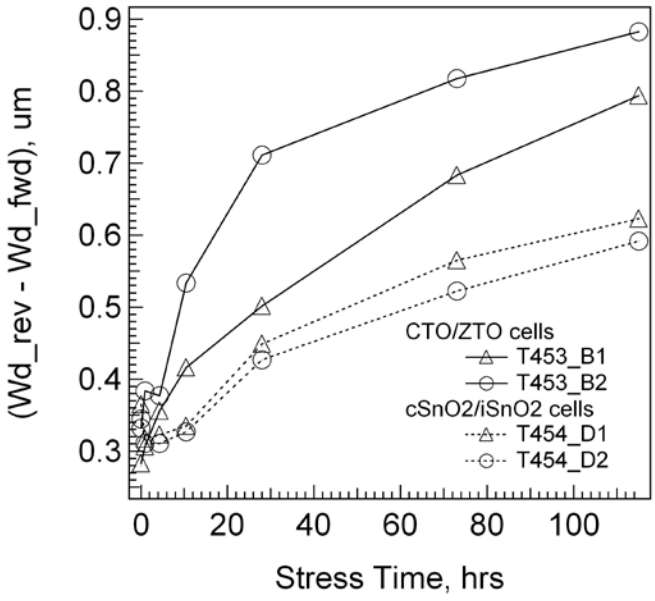

Figure 10. Depletion width hysteresis plotted as a function of ALT stress for CdTe devices grown on both CTO/ZTO and $cSnO_2/iSnO_2$ glass substrates

As cells degrade, there is a near monotonic increase in hysteresis. The Cu-doped, graphite paste contacts contain ample Cu to source Cu well beyond the termination of back contact fabrication. For example, a typical Cu-containing paste contains approximately 0.25 gms of $Cu_{1.4}Te$ for each 10 grams of carbon electrodag. Approximating the molecular weight of the electrodag to that of carbon, and assuming an approximate electrodag thickness of 100 microns (commonly

observed in cross-sectional images) and a CdTe thickness of 10 microns, the potential at% ratio of Cu to Cd is on the order of 0.10. Only a fraction of this Cu is introduced into the CdTe film during routine back contact processing. The presence of this "infinite Cu source" would explain the observed increase in hysteresis observed in the $cSnO_2/iSnO_2$ cells as Cu diffuses continuously, during the course of ALT, into the CdTe film. However, since the CTO/ZTO cells share the same paste contact and back contact processing, the greater rate of hysteresis increase seen for these latter cells in Figure 10 suggests an additional source of ion contamination. The only real difference between the CTO/ZTO and SnO_2-based devices is indeed the TCO stannate layers.

There are three generally accepted methods by which conductivity is improved in these stannate structures. The spinel structure (composed of 32 close-packed oxygen atoms) contains 64 and 32 possible tetrahedral and octahedral interstitial sites of which only 1/8 and 1/2 of these sites are occupied by cations. In the inverse-spinel Cd_2SnO_4 structure, the 8 tetrahedral sites are occupied entirely by Cd^{2+}, while the 16 octahedral sites are shared equally by Cd^{2+} and Sn^{4+}. The most intuitive mechanism by which to improve CTO conductivity is to introduce additional Cd interstitials. Another possibility is to introduce oxygen vacancies though the formation energy may be too high. Finally, n-type conductivity in CTO can be achieved by the replacement of an octahedrally coordinated Cd^{2+} with Sn^{4+} [21]. The latter, combined with basic thermodynamics would explain a consistent observation concerning CTO and ZTO films. CTO films can exhibit high conductivities, yet, ZTO films are always very resistive. Thermodynamically, Zn is a strong reducing agent and will reduce both SnO_2 and CdO, i.e., the Zn—O bond is favored. At the same time, SnO_2 is favorable relative to CdO. In CTO and ZTO structures, it is therefore, thermodynamically possible that Sn^{4+} will tend to replace octahedrally coordinated Cd^{2+} ions (i.e., conducting CTO), and unfavorable that it will replace similarly coordinated Zn^{2+} ions (i.e., resistive ZTO).

It was at first suspected that the complex defect chemistry of CTO and ZTO films as well as their formation could be responsible for the larger degradation observed in CTO/ZTO devices. For example, these films were sputtered onto unheated substrates and then converted by a high temperature CdS proximity anneal. The films undergo considerable modification during this step. It would be presumptuous to assume that post-annealed films are entirely single phase and crystalline, and void of secondary phases. Also, the strongly reducing nature of Zn should always be suspect due to its high chemical potential. Zn, after all, is regularly used as a catalyst to reduce and subsequently remove SnO_2 from glass during routine cleaning procedures. The decomposition of either CTO or ZTO would however not be expected to affect cell performance much. Again, it has been reported that large variations in CTO stoichiometry only affect resistivity slightly [11] and as discussed previously, any change in ZTO resistivity would be over-shadowed by the already high resistivity of the CdTe itself. This is also corroborated by the lack of any significant increase in series resistance observed with stress in these cells as shown in Figure 6. However, changes in CTO and ZTO film composition might manifest electronically by either introducing additional mobile ions into CdTe as well as additional deep states during ALT. The fact that there is no clear mechanism by which the addition of mobile ions from the CTO and ZTO layers would degrade performance indeed does suggest that it is rather, the formation of deep states, and not mobile ions, that may be responsible for the degradation observed in this study. The formation of deep states, and thus increased recombination will directly impact the performance of CdTe solar cells.

4. CONCLUSIONS

CdS/CdTe cells deposited on CTO/ZTO transparent conducting oxides show greater initial performance relative to more conventional SnO_2-based substrates due to the superior optical and electrical properties of the oxide layers and the ability of using more rigorous $CdCl_2$ processing. Open-circuit voltage is not observed to increase when using the CTO/ZTO substrates. Performance uniformity when using the CTO/ZTO substrates was a problem however. When exposed to accelerated lifetime testing under 1-sun illumination, V_{oc} bias, and both 85 °C and 100 °C stress temperatures, the CTO/ZTO cells did not perform as well as similar devices grown on SnO_2-based substrates though the mechanism of degradation is suspected to be strongly determined by how the subsequent CdS/CdTe cells were grown. Considerable C-V hysteresis was observed in Cu-doped CdTe cells. Degradation in cells correlates well with an increase in this hysteresis. The hysteresis itself can be explained by either ionic motion of free charge in the CdTe, or majority carrier (hole) emission and charging of deep states in the CdTe space-charge region. Performance degradation could not be explained simply by considering the motion of ions. Rather, it is suggested, that ultimately, the formation of additional deep states, perhaps through the decomposition of unstable CTO and/or ZTO layers, may be responsible for the increased degradation observed in CTO/ZTO cells.

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14. ABSTRACT *(Maximum 200 Words)*

CdS/CdTe photovoltaic solar cells were made on two different transparent conducting oxide (TCO) structures to identify differences in fabrication, performance, and reliability. In one set of cells, chemical vapor deposition (CVD) was used to deposit a bi-layer TCO on Corning 7059 borosilicate glass consisting of a F-doped, conductive tin-oxide (cSnO2) layer capped by an insulating (undoped), buffer (iSnO2) layer. In the other set, a more advanced bi-layer structure of sputtered cadmium stannate (Cd2SnO4; CTO) as the conducting layer and zinc stannate (Zn2SnO4; ZTO) as the buffer layer was used. CTO/ZTO substrates yielded higher performance devices; however, performance uniformity was worse due to possible strain effects associated with TCO layer fabrication. Cells using the SnO2-based structure, only slightly lower in performance, exhibited considerably greater performance uniformity. When subjected to accelerated lifetime testing at 85 - 100ºC under 1-sun illumination and open-circuit bias, more degradation was observed in CdTe cells deposited on the CTO/ZTO substrates. Considerable C-V hysteresis, defined as the depletion width difference between reverse and forward direction scans, was observed in all Cu-doped CdTe cells. Hysteresis increases with increasing stress and degradation; the mechanism is discussed for an ionic-drift model and one involving majority carrier emission in the space-charge region.

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