



Direct Correlation of CdTe Solar Cell Stability with Mobile Ion Charge Generation During Accelerated Lifetime Testing

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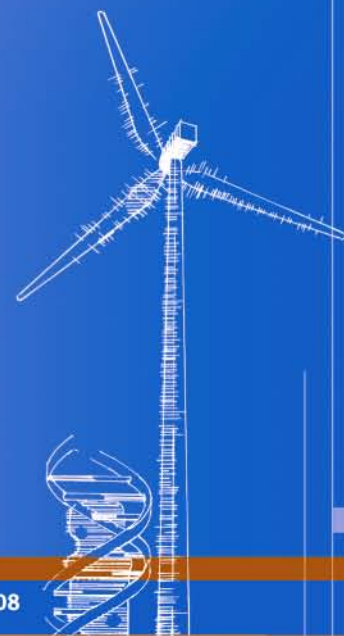
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*Presented at the 34th IEEE Photovoltaic Specialists Conference
Philadelphia, Pennsylvania
June 7–12, 2009*

Conference Paper

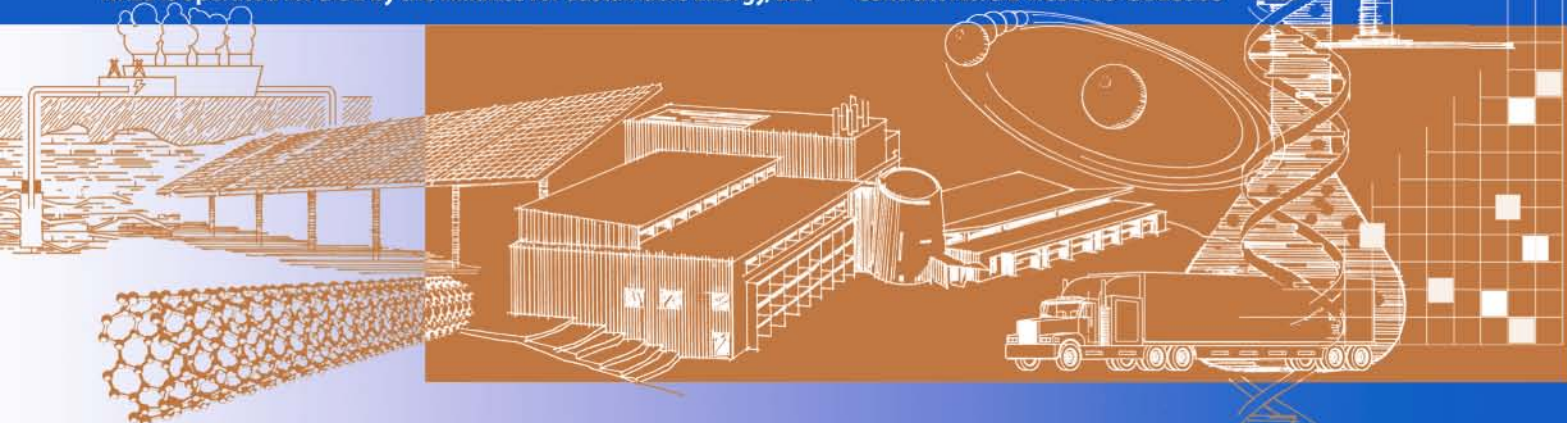
NREL/CP-520-46055

June 2009



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Contract No. DE-AC36-08-GO28308



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THE DIRECT CORRELATION OF CDTE SOLAR CELL STABILITY WITH MOBILE ION CHARGE GENERATION DURING ACCELERATED LIFETIME TESTING

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ABSTRACT

CdS/CdTe cells deposited on cadmium and zinc stannate (CTO/ZTO) transparent conducting oxide (TCO) substrates show greater degradation than similar devices fabricated on SnO₂-based substrates. This has been confirmed in two separate studies in which J-V changes during stress suggest different degradation mechanisms believed to be due to differences in processing. In addition, cells made using the CTO/ZTO substrates exhibit greater variations in initial performance relative to SnO₂-based substrates. A capacitance-voltage (CV) method using different initial bias conditions is used to quantify mobile ion concentration. CV hysteresis was observed in Cu-containing cells and was absent in cells that were not intentionally doped with Cu. With increasing stress, hysteresis increased. A faster rate of hysteresis gain was observed in CTO/ZTO cells relative to SnO₂ cells. A model is introduced for explaining the origin of the hysteresis and why it increases with increasing stress.

BACKGROUND

Small-area CdS/CdTe solar cell stability has been an area of focus. The effects of localized shunts [1], improved reliability through the use of Te and O [2] to mitigate Cu diffusion, and methods for determining degradation activation energies attributed to both Cu and S diffusion [3] have been reported. In the latter paper, higher activation energy mechanisms (S diffusion) were shown to dominate lower energy processes, e.g., the heavily studied effects associated with Cu diffusion. Degradation was shown to be stress temperature dependent (Fig. 1(a)). The lower degradation activation energy ($E_a \sim 0.63$ eV) measured at higher temperatures (100 – 120 °C) was attributed to Cu-diffusion (E_a reported as 0.67 eV [4]) from the heavily Cu-doped back contact. The mechanism responsible for the higher measured activation energy ($E_a \sim 2.94$ eV) seen at lower temperatures (60 – 80 °C) was perplexing until scanning electron microscopy (SEM) showed the formation of Kirkendall voids in the CdS with increasing stress. At this point, it became clear that bulk S-diffusion (E_a reported as 2.8 eV [5]) from the CdS may be responsible for degradation at lower temperatures. S out-diffusion from the CdS layer also helped explain the results of a correlation analysis in which changes in cell performance ($\eta\%$) was plotted as a function of changes in 2nd level metrics (open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), and fill factor (FF)).

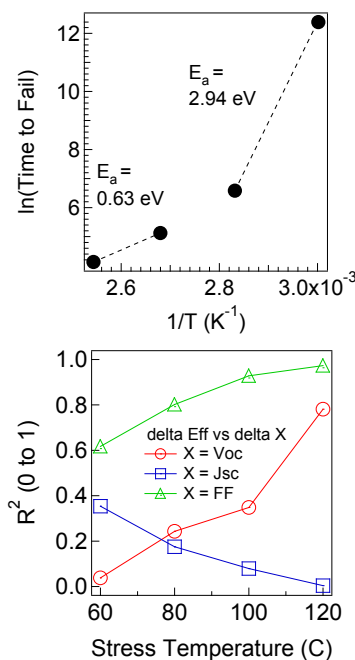


Fig. 1. (a) Arrhenius plot showing two different activation energies associated with CdTe ALT. (b) Correlation plots of performance change (ΔEff) vs. changes in V_{oc} , J_{sc} , and FF as a function of ALT stress temperature.

As shown in Fig. 1(b), changes in performance were well-correlated ($R^2 = 1$ being perfect) with FF change at all temperatures. At the same time, the moderate correlation with J_{sc} seen at lower stress temperatures (where S diffusion dominates) decreases with increasing temperature. J_{sc} correlation at lower stress temperatures could be due to the optical attenuation effect CdS has on photogenerated current. Thus, it is shown how an energetically less favorable (S diffusion with $E_a \sim 2.8$ - 2.9 eV) mechanism, can dominate a more favorable one (Cu diffusion; $E_a \sim 0.63$ - 0.67 eV), if in fact that mechanism occurs at a critical location in the cell (the junction in this case).

In [3], the CdS/CdTe cells were deposited by chemical bath deposition (CBD) and close spaced sublimation (CSS) respectively on Corning borosilicate (7059) glass substrates which had been previously coated by chemical-vapor deposited (CVD) SnO₂ using a tetramethyltin (TMT) precursor. The SnO₂ structure consisted of a bilayer configuration in which a F-doped, *conductive* cSnO₂ layer was deposited first, followed by an undoped, *intrinsic*, iSnO₂

buffer layer. In this paper, the stress tolerance of CdS/CdTe cells grown by identical semiconductor layer processes (and identical back contact fabrication) using both the TMT-CVD SnO₂ bilayer construction (cSnO₂/iSnO₂) and a more advanced, sputtered conducting Cd₂SnO₄ (CTO) and resistive Zn₂SnO₄ (ZTO) buffer layer will be discussed. The latter transparent-conducting-oxide (TCO) is arguably the most important technology partition (along with back contact variations) in the CdTe field. SnO₂ is a proven and cost-effective TCO while CTO/ZTO layers are well known to have yielded the highest CdS/CdTe *starting* cell efficiencies to date [6]. The relative merit of CdS/CdTe cells using SnO₂ and the more advanced CTO/ZTO layers is shown in Fig. 2.

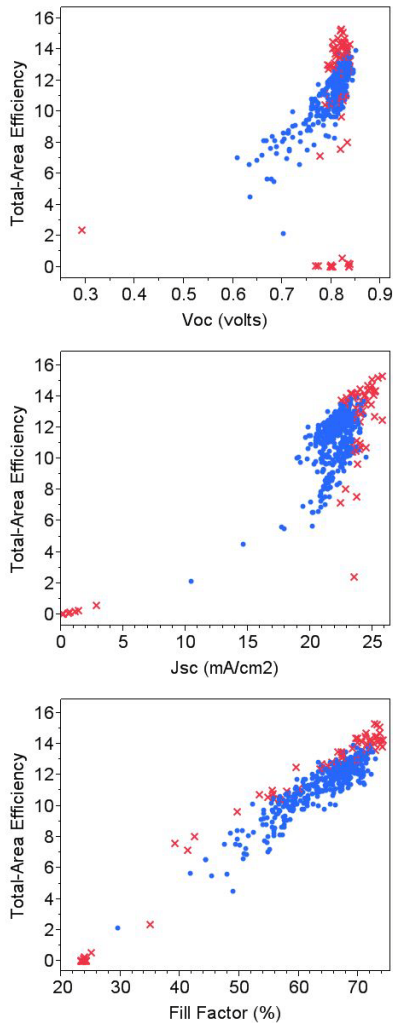


Fig. 2. Top, middle, bottom figures show cell efficiency vs V_{oc} , J_{sc} , and FF respectively for CdTe cells fabricated from bilayer SnO₂ (blue) and CTO/ZTO (red).

The initial performance data shown in Figure 2 consists of a sample of (447) SnO₂-based and (62) CTO/ZTO-based cells fabricated at NREL over the course of several years of research and reflects the variation in performance

resulting from cell optimization work. Several comments are worthy of note. First, higher performance in CTO/ZTO cells is due to improvements in J_{sc} and FF only. There is no indication that V_{oc} improves when using the CTO/ZTO structure. Another important observation is that CTO/ZTO cells can exhibit extremely poor performance that is not observed when using SnO₂-based TCOs. Some of these “outliers” will be discussed subsequently. Regardless, the CTO/ZTO substrates are clearly superior in regards to *initial* performance. Arguments for why the CTO/ZTO structure exhibits higher J_{sc} and FF values are thoroughly discussed by Wu [6] who pioneered the application of these layers for CdTe cells.

Though the merits of CTO/ZTO buffer layers are well known, there is a dearth of knowledge concerning the relative stability of these structures. In 2004, a preliminary determination of the dry heat stability (85 °C/ room-temperature humidity ~ 3% RH) of a number of CTO/ZTO and SnO₂-based CdTe cells was performed. At that time, uncertainty in whether these cells were optimized to minimize edge shunts prevented publication of this work. Re-evaluation of that data, as well as its relevance to this paper, justifies a brief discussion of some key results.

Figure 3 shows the one-way analysis of variance (ANOVA) in degradation of V_{oc} , J_{sc} , FF, and $\eta\%$ (delta V_{oc} , delta J_{sc} , delta FF, and delta Eff respectively) measured in 14 stressed CTO/ZTO and 7 SnO₂ based cells after 521 hrs of dry heat ALT.

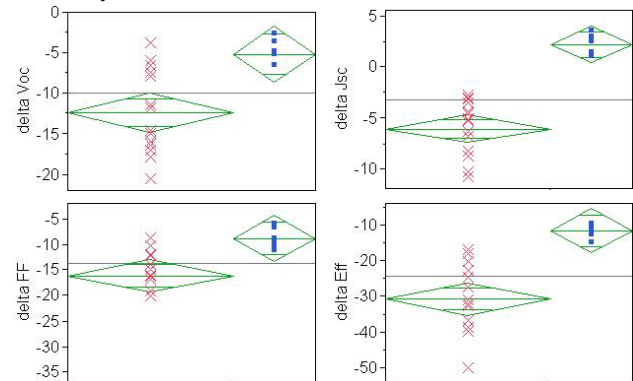


Fig. 3. ANOVA of changes in V_{oc} , J_{sc} , FF, and $\eta\%$ (left to right; top to bottom) measured during dry heat (85 °C) ALT of CTO/ZTO (red X's) and SnO₂ (blue dots) based CdS/CdTe cells.

The ANOVA “diamonds” represent both group means (center horizontal line) and 95% confidence intervals (CI) of the mean (min and max vertical extent of the diamond). Statistically significant differences between groups (CTO/ZTO and SnO₂-based cells) exist when the 95% CIs do not overlap. After 521 hours, the mean change in V_{oc} , J_{sc} , FF, and $\eta\%$ for CTO-based cells were measured as -12.5%, -6.0 %, -16.2%, and -30.8% respectively. For SnO₂-based cells these same changes were -5.2%, +2.2%, -8.8%, and -11.6%. Differences in V_{oc} , J_{sc} , and $\eta\%$ degradation based on CTO-type were clearly shown to be significant. Shunting (determined by the inverse-slope

of the current-voltage curve at V=0 in the dark) was only observed in 1 out of 14 CTO/ZTO cells after 521 hrs of stress and is thus not responsible for the large V_{oc} decrease shown above.

EXPERIMENTAL PROCEDURE

Cell Fabrication

Techniques for depositing the CdS/CdTe layers are previously described [7]. The basic structure is that of a borosilicate (7059) superstrate design in which light passes through a glass/TCO construction (either 7059/cSnO₂/iSnO₂ or 7059/CTO/ZTO), where it is then absorbed in the n-(CdS)/p-(CdTe) heterojunction. For this study, the chemical-bath deposited CdS layer thickness was ~80 nm while the CSS deposited CdTe thickness was ~8 μm. After the CdTe deposition, the finished structure was exposed to vapor CdCl₂ (VCC) in an oxygen/helium ambient (100 Torr O₂ + 400 Torr He). SnO₂-based cells were CdCl₂-treated at either 400 or 405 °C for 5 m. CTO/ZTO-based cells were treated at either 400 °C/5 m or 410 °C/10 m. Prior to the back contact step, CdTe surfaces were treated with a NP etch in order to form a beneficial, Te-rich layer and to remove surface oxides. Back contacts concluded with the application of a relatively thick layer (~50–100 μm) of graphite paste containing Cu_xTe and HgTe dopants followed by a similarly thick, final conducting layer of Ag paste. A narrow (~1 mm) margin of CdTe surrounding the perimeter of the dopant/Ag paste contact was used to reduce edge shunting.

SnO₂ layers were again grown by TMT-CVD. The cSnO₂ and iSnO₂ layers were 500 and 100 nm thick respectively. The resulting sheet resistance was measured at ~9 ohms/sq. The CTO and ZTO layers were sputtered at room temperature to a thickness of 320 and 150 nm respectively. Conditions for sputtering these stannate layers as well as the post-deposition CdS proximity anneals can be found in [6].

Performance data using standard current density versus voltage (J-V) scans were made on cells after fabrication (t = 0) and during stress testing with a J_{sc} -calibrated Oriel solar simulator. Capacitance-voltage (C-V) measurements (dark and room temperature) were performed on half the stressed cells using an Agilent 4294A Precision Impedance Analyzer operated manually at 100 kHz and 50 mV oscillation voltage. Capacitance data was collected by scanning voltage in two directions. Immediately upon applying a voltage of +0.5 V forward bias, capacitance was measured as voltage was quickly swept (~3 s) in a “reverse” direction to -1.5 V where it was held for exactly 5 min. During the subsequent “forward” sweep back to +0.5 V, capacitance data was again collected. C-V data for these two directions will subsequently be referred to as “rev” and “fwd” scans. The rationale for using this “two-way” scan will be discussed shortly.

Stress conditions have been described before [3]. Basically, cells were placed, glass-side up, under an Atlas CPS+ solar light source (~AM 1.5; 1-sun) in machined Al blocks designed to keep the cells at V_{oc} bias. Cell tem-

perature was set at 100 °C. At times equal to 1, 4.4, 10, 28, 73, and 115 hrs cells were removed and stored in the dark for 12-24 hrs. After quick measurements of J-V and C-V, cells were again placed under stress. Sometime after the last measurement at T=115 °C, the temperature controllers failed resulting in excessive heating and destruction of cells. The actual test temperature of 100 °C is suspect (temperatures may have been higher). Regardless, the design of the Al blocks at least assures us that cells were all tested at the same temperature.

EXPERIMENTAL RESULTS

Two different 7059/CTO/ZTO and 7059/cSnO₂/iSnO₂ substrates were used and are appended “_1” & “_2” in Table 1. Performance of cells deposited on a particular 7059/CTO/ZTO substrate was found to vary considerably. Initial cell performance metrics by substrate are shown in Table 1.

Dev ID	Substrate	VCC_T (°C)	VCC_t (m)	V _{oc} (volts)	J _{sc} (mA/cm ²)	FF (%)	η (%)	ALT	CV
T452_A1	CTO/ZTO_1	410	10	0.768	0.6	24.2	0.1		
T452_A2	CTO/ZTO_1	410	10	0.799	0.7	23.8	0.1		
T452_B1	CTO/ZTO_1	410	10	0.821	2.8	25.1	0.6		
T452_B2	CTO/ZTO_1	410	10	0.772	0.6	23.3	0.1		
T452_C1	CTO/ZTO_1	400	5	0.801	0.1	23.9	0.0		
T452_C2	CTO/ZTO_1	400	5	0.803	0.2	23.4	0.0		
T452_D1	CTO/ZTO_1	400	5	0.796	0.0	24.1	0.0		
T452_D2	CTO/ZTO_1	400	5	0.799	0.0	23.6	0.0		
T453_A1	CTO/ZTO_2	410	10	0.823	24.5	53.3	10.7		
T453_A2	CTO/ZTO_2	410	10	0.829	24.0	55.5	11.0		
T453_B1	CTO/ZTO_2	410	10	0.825	24.4	67.1	13.5	X	X
T453_B2	CTO/ZTO_2	410	10	0.827	24.6	71.1	14.5	X	X
T453_C1	CTO/ZTO_2	400	5	0.795	23.7	56.8	10.5		
T453_C2	CTO/ZTO_2	400	5	0.795	23.7	69.0	13.0		
T453_D1	CTO/ZTO_2	400	5	0.806	24.2	67.2	13.1	X	
T453_D2	CTO/ZTO_2	400	5	0.809	23.9	70.5	13.6	X	
T454_A1	nSnO2/iSnO2_1	405	5	0.832	23.1	69.9	13.4		
T454_A2	nSnO2/iSnO2_1	405	5	0.830	23.0	72.0	13.7		
T454_B1	nSnO2/iSnO2_1	405	5	0.830	23.1	69.5	13.4		
T454_B2	nSnO2/iSnO2_1	405	5	0.832	23.2	71.8	13.8		
T454_C1	nSnO2/iSnO2_1	400	5	0.818	22.6	66.8	12.3		
T454_C2	nSnO2/iSnO2_1	400	5	0.823	22.6	70.8	13.2		
T454_D1	nSnO2/iSnO2_1	400	5	0.826	22.8	69.1	13.0	X	X
T454_D2	nSnO2/iSnO2_1	400	5	0.830	22.6	72.0	13.5	X	X
T455_A1	nSnO2/iSnO2_2	405	5	0.832	23.1	69.8	13.4		
T455_A2	nSnO2/iSnO2_2	405	5	0.825	23.2	70.7	13.5		
T455_B1	nSnO2/iSnO2_2	405	5	0.830	23.3	70.4	13.6	X	
T455_B2	nSnO2/iSnO2_2	405	5	0.829	23.3	71.6	13.8	X	
T455_C1	nSnO2/iSnO2_2	400	5	0.823	22.9	68.7	13.0		
T455_C2	nSnO2/iSnO2_2	400	5	0.824	22.6	71.3	13.3		
T455_D1	nSnO2/iSnO2_2	400	5	0.824	22.9	69.5	13.1		
T455_D2	nSnO2/iSnO2_2	400	5	0.822	22.3	71.0	13.0		

Table 1. Initial (t=0) cell performance metrics by substrate

The performance of cells grown on the SnO₂-based TCO is very uniform for a given VCC treatment. This is not the case for the CTO/ZTO-based TCOs. For the CTO/ZTO substrate labeled as CTO/ZTO_1, all cells show little J_{sc} while FF appears to be the primary reason for variations in cells grown on substrate CTO/ZTO_2. Figure 4 shows the J-V curves for one of the CTO/ZTO_1 cells and two cells from CTO/ZTO_2 showing the greatest spread in performance (T453_A1 and T453_B2).

Series resistance, R_s , appears to be the primary reason for the large variation in initial cell performance for these CTO/ZTO cells. In our experience, such a large

variation in initial cell performance among cells that have been identically processed had never been seen when using SnO₂-based substrates, which suggests the R_s variation is associated with the use of these CTO/ZTO based TCOs. At first glance, the root cause would not appear to be CTO compositional fluctuations. According to the combinatorial study by Li et al. [8], resistivity varies less than an order magnitude in the CdO-SnO₂ binary system. This is not adequate for explaining the observed variations in R_s. Also, since the ZTO thickness is only 150 nm, even magnitude changes in resistivity would not seriously impact R_s in these devices (the ZTO layer is nominally reported to be 1-10 Ω-cm [6]). Closer examination of the devices show that very small “micro” cracks in the CTO were responsible for the high R_s. The reason for why some regions of the CTO substrates showed this effect, and also, the origin of this “cracking” is currently under investigation.

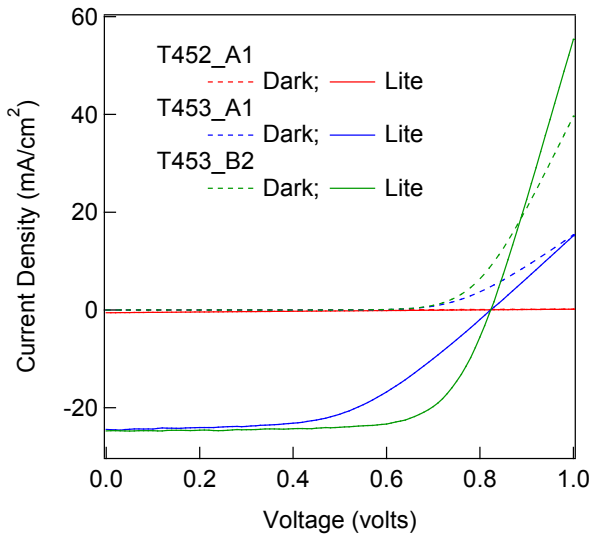


Fig. 4. Initial (t = 0) J-V characteristics for CTO/ZTO cells

Due to problems with CTO/ZTO uniformity, the number of cells for subsequent stress testing was reduced. Table 1 shows the (4) CTO/ZTO and (4) cSnO₂/iSnO₂ cells that were chosen for subsequent stress testing (ALT). J-V measurements were performed on all stressed cells, while C-V measurements (also indicated in Table 1) were only performed on half this set.

The variation in performance metrics during ALT are shown in Figure 5. Changes in performance are normalized to measurements performed at t=0 (initial data). All data for the CTO/ZTO (red) and SnO₂ (blue) based cells are shown in Figure 5. Data shown as “bold” lines correspond to cells in which C-V measurements were also made. Figure 5 shows in general, more degradation in cells using the CTO/ZTO layers corroborating the earlier study performed in 2004. However, the degradation observed in the present study was different. Figure 6 compares representative J-V curve changes with stress from these two studies.

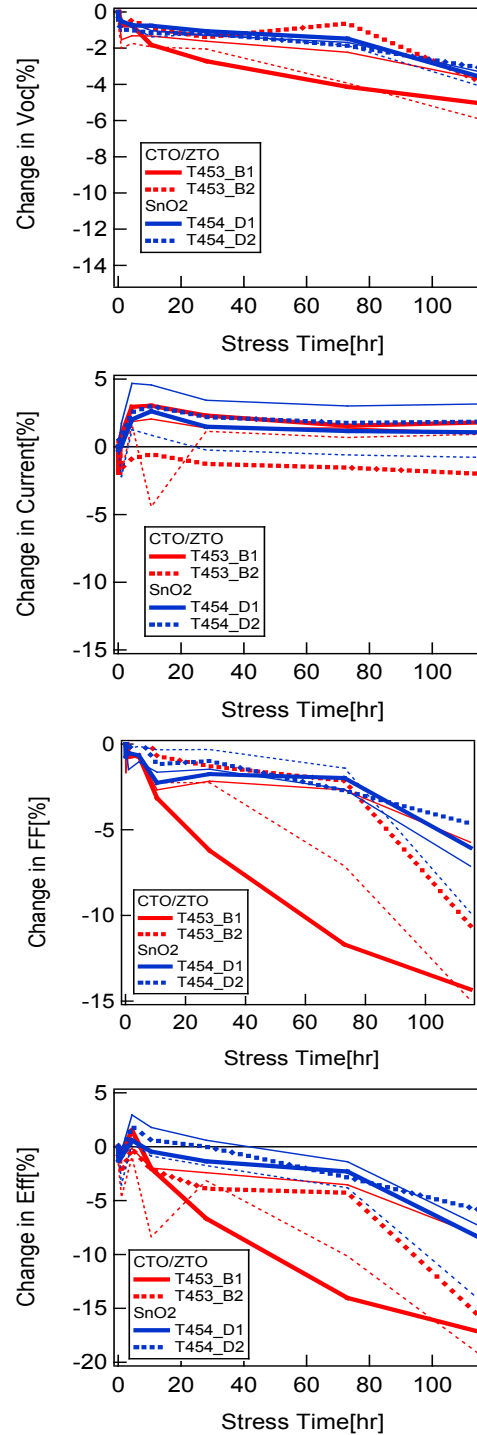


Fig. 5. Performance change during ALT

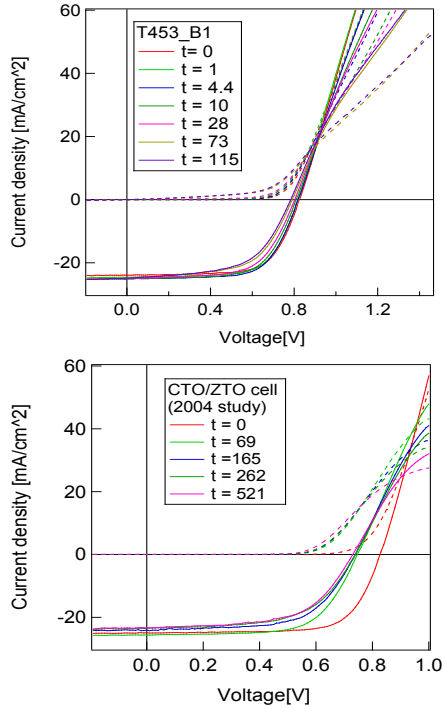


Fig. 6. Representative J-V changes with stress time t (hr) observed in this (top) and earlier (bottom) study

CTO/ZTO cells made in this study show considerably less V_{oc} degradation than those in the earlier study. Initial V_{oc} drops were quite large in all 14 CTO/ZTO cells in the 2004 work. This was followed by a shift to FF degradation as seen in the bottom graph of Figure 6. For the CTO/ZTO cells of this study, shunting was observed. Three out of 4 cells in this case exhibited shunting with stress (see top graph of Figure 6). The lack of any significant increase in R_s for these cells also implies the R_s non-uniformity observed in the as-grown ($t=0$) case was more a function of processing and not a stability issue. Since details concerning the fabrication of the earlier CTO/ZTO cells measured in 2004 were not available, it is difficult to ascertain why these CTO/ZTO cells degraded differently. In this study, the CdS layer was grown by CBD. It is not clear whether this was the case for the 2004 study. What is clear however is that processing of the CTO/ZTO layers has a profound effect not only on the rate of degradation, but also on how it manifests. This is important. One should not consider degradation as purely representative of the materials involved. One also needs to consider the more subtle details associated with fabrication conditions, and possibly, the fabrication techniques used to deposit those layers. *The results shown here are more reflective of how cells were made, and not a general statement regarding the technology.*

This paper will now conclude with a discussion of some interesting features observed in C-V measurements made during ALT. C-V is commonly used to determine doping profiles in solar cells. Historically, they have also been used to quantify mobile ionic charge, particularly Na^+ , Li^+ ,

and K^+ in SiO_2 (MOS structures) by measuring field-induced C-V hysteresis [9]. More recently, capacitance transients were used by Enzenroth et al. to study mobile Cu_i^+ in CdS/CdTe solar cells [10] in which he correlates increased Cu_i^+ densities with increased Cu introduced during cell fabrication. This study in itself was based upon the transient ion drift (TID) investigation of both $CuInSe_2$ and CdTe by Lyubomirsky et al. [11].

Building upon these earlier ideas, we developed a C-V based technique for measuring mobile ion charge generation during ALT measurements. A key requirement of any measurement made during ALT is that the measurement be quick enough so as not to introduce *unintentional* relaxation effects during long-term stress testing. Another requirement is that the technique “does no harm”. The “two-way” scan C-V approach described earlier is quick, requiring ~ 10 min. to perform for each cell tested. Also, because bias is maintained constant only during negative voltages, potentially higher current densities at positive bias (and possible cell damage) are minimized.

Representative C-V data using this approach is shown in Figure 7 below where the red and blue curves correspond to cells made when both Cu is added and not added as a constituent of the graphite paste contact respectively.

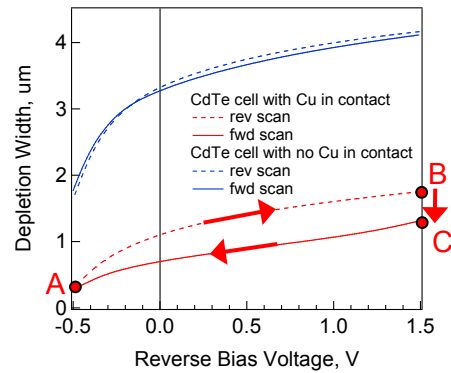


Fig. 7. Representative C-V data of Cu and non-Cu containing CdTe cells obtained using two sweep directions.

This figure plots the depletion width, W_d (inversely proportional to capacitance) as a function of *reverse-bias*. This figure distinguishes two unique ways Cu affects the space-charge. The strong decrease in W_d (blue curves to red curves) reflects an increase in CdTe ionized acceptor concentration, N_a^- , with increased Cu possibly as Cu_{Cd} or as a paired, defect complex. This was expected. What is not as obvious is the hysteresis introduced when Cu is present. When Cu is not *intentionally* added (i.e., Cu is routinely discussed as a naturally occurring, trace impurity in CdTe), we see little indication of hysteresis (the blue solid and dashed lines). This has been seen in every cell where Cu is intentionally absent. In contrast, when Cu is present, we observe a large hysteresis in which W_d measured during the second (fwd) scan is always lower than the value of W_d determined during the first (rev) scan. We attribute this observation to the following. The first scan is performed immediately (point A \rightarrow B in Fig. 7) from +0.5 V

to -1.5 V and reflects the charge state in the depletion width where Cu exists in some hypothetical equilibrium profile shown figuratively by the horizontal red line in Figure 8(a).

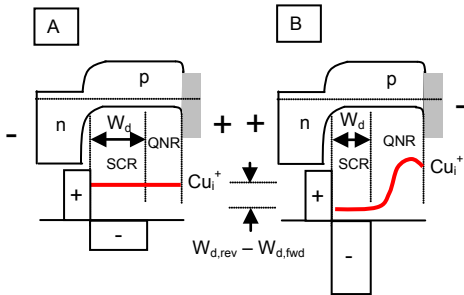


Fig. 8. Variations in depletion width, W_d , as a function of bias during two-way C-V scan procedure. (Band energy and Fermi-Levels not drawn to reflect bias changes)

At point B in Fig. 7, the cell is held at -1.5 V bias for exactly 5 min. During this time, capacitance is observed to increase slowly, reflecting a decrease in W_d to point C. Mechanistically, this can be explained by the field assisted diffusion of Cu_i^+ towards the back contact. We propose that Cu_i^+ , when present in the depletion region, screens negatively charged, ionized acceptors, N_a^- . When removed from the space-charge, N_a^- effectively increases causing a decrease in W_d to maintain space-charge neutrality. After 5 min., bias is applied in the fwd direction from -1.5 V to +0.5 V. The hysteresis is arbitrarily defined as the difference, $W_{d,rev} - W_{d,fwd}$ observed at $V=0$ and in this sense, is proportional to the amount of mobile ions, e.g., Cu_i^+ in the cell.

Electrostatic charging of localized traps, e.g., grain boundaries, might also explain some of the effects shown here [12]. Enzenroth [10] discusses this possibility in his own TID measurements, and we too must also make note of this possibility. However, the mobile ion model above does appear to adequately explain the C-V behavior well.

A plot of the C-V hysteresis with stress time (shown in Figure 9) shows an interesting correlation with performance degradation. As cells degrade, there is a near monotonic increase in hysteresis. The Cu-doped, graphite paste contacts contain ample Cu to source Cu beyond $t=0$. This would explain some of the increase in hysteresis (mobile ion charge generation). However, since the CTO/ZTO and $\text{cSnO}_2/\text{iSnO}_2$ cells use the same back contact, the hysteresis increase should be identical. One explanation, and one also supporting the greater degree of degradation seen in CTO/ZTO cells (Figure 5) is that the increased generation of mobile charge observed for CTO/ZTO cells shown in Figure 9 might represent a decomposition of either the CTO or ZTO layers resulting in the evolution of additional positive ions, i.e., Cd^{2+} , Zn^{2+} , or Sn^{4+} . Though unclear of the mechanism, this might also be responsible for the increased shunting observed in Figure 6. Future experiments are planned to investigate this possibility.

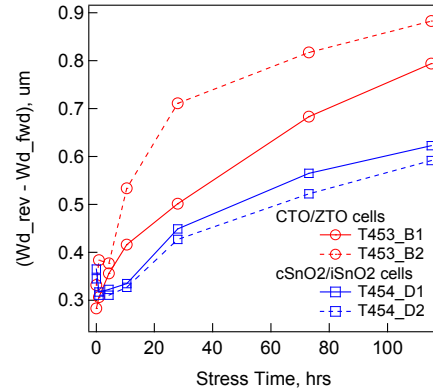


Fig. 9. Depletion width hysteresis plotted as a function of ALT stress time.

SUMMARY

CdS/CdTe cells deposited on CTO/ZTO TCO substrates show greater degradation than similar devices fabricated on $\text{cSnO}_2/\text{iSnO}_2$ substrates. Degradation in CTO/ZTO cells appears to be process sensitive. Considerable C-V hysteresis was observed in Cu-containing cells. Increased degradation occurred in parallel with an increase in C-V hysteresis. A model is presented linking this to an increase in mobile ion charge.

ACKNOWLEDGEMENTS

We would like to thank Jian Li and Joe DelCueto for many useful discussions concerning the C-V data. This work was supported by the U.S. Dept. of Energy under Contract No. DOE-AC36-08G028308 with NREL.

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REPORT DOCUMENTATION PAGE

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1. REPORT DATE (DD-MM-YYYY) June 2009		2. REPORT TYPE Conference Paper		3. DATES COVERED (From - To) June 7-12, 2009		
4. TITLE AND SUBTITLE Direct Correlation of CdTe Solar Cell Stability with Mobile Ion Charge Generation During Accelerated Lifetime Testing: Preprint				5a. CONTRACT NUMBER DE-AC36-08-GO28308		
				5b. GRANT NUMBER		
				5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) D.S. Albin, R.G. Dhere, S.C. Glynn, and W.K. Metzger				5d. PROJECT NUMBER NREL/CP-520-46055		
				5e. TASK NUMBER PVA92450		
				5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393				8. PERFORMING ORGANIZATION REPORT NUMBER NREL/CP-520-46055		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S) NREL		
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER		
12. DISTRIBUTION AVAILABILITY STATEMENT National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161						
13. SUPPLEMENTARY NOTES						
14. ABSTRACT (Maximum 200 Words) CdS/CdTe cells deposited on CTO/ZTO TCO substrates show greater degradation than similar devices fabricated on cSnO2/iSnO2 substrates. This has been confirmed in two separate studies in which J-V changes during accelerated lifetime testing suggest different overall degradation mechanisms which are believed to be due to differences in processing. In addition, cells made using the CTO/ZTO substrates exhibit greater variations in initial performance relative to SnO2-based substrates. A new method using capacitance-voltage (CV) measurements performed with different initial bias conditions is used to quantify mobile ion content as a function of stress. CV hysteresis was observed in Cu-containing cells and was absent in cells that were not intentionally doped with Cu. With increasing stress, hysteresis increased. A higher rate of hysteresis gain was observed in CTO/ZTO cells relative to SnO2 cells. A model is introduced for explaining the origin of the hysteresis and why it increases with increasing stress.						
15. SUBJECT TERMS PV; solar cell; capacitance-voltage; reliability; Cu diffusion; back contact; scanning electron microscopy; ion charge generation; fill factor;						
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UL	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON	
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER (Include area code)	