National Renewable Energy Laboratory
A national laboratory of the U.S. Department of Energy
Office of Energy Efficiency & Renewable Energy
Innovation for Our Energy Future

Development of Large High-Voltage PV Modules with Improved Reliability and Lower Cost

Final Subcontract Report
1 April 2006 – 31 August 2007

J. Wohlgemuth
BP Solar International, Inc.
Frederick, Maryland

Subcontract Report
NREL/SR-520-43828
May 2009

NREL is operated for DOE by the Alliance for Sustainable Energy, LLC Contract No. DE-AC36-08-GO28308

Development of Large High-Voltage PV Modules with Improved Reliability and Lower Cost

Subcontract Report
NREL/SR-520-43828
May 2009

Final Subcontract Report
1 April 2006 – 31 August 2007

J. Wohlgemuth
BP Solar International, Inc.
Frederick, Maryland

NREL Technical Monitor: Richard L. Mitchell

Prepared under Subcontract No. ZAX-6-33628-11

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

NREL is a national laboratory of the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
Operated by the Alliance for Sustainable Energy, LLC

Contract No. DE-AC36-08-GO28308

This publication was reproduced from the best available copy submitted by the subcontractor and received no editorial review at NREL

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

PREFACE

This Annual Technical Progress Report covers the work performed by BP Solar International Inc. for the contract period April 1, 2006 to August 31, 2007 under DOE/NREL Subcontract #ZAX-6-33628-11 entitled "Development of Large High-Voltage PV Modules With Improved Reliability and Lower Cost". The Annual Report has become the Final Report as the BP Solar effort has transitioned from a Photovoltaic Manufacturing Technology Program under NREL to a Technology Pathways Partnership under the DOE sponsored Solar America Initiative.

The following personnel at BP Solar have contributed to the technical efforts covered in this report.

Dinesh Amin	Neil Placer
Roger Clark	Joseph Creager
Danny Cunningham	George Kelly
Bonnie Kinsey	Timothy Koval
Andy Nguyen	Jean Posbic
Bei Wu	Jay Shaner
Nathan Stoddard	John Wohlgemuth
Murray Bennett	Jay Miller
Steve Roncin	Bikash Kumar
Monte Lewis	Soham Dey

The following personnel at North Carolina State University have contributed to the technical effort covered in this report:

George Rozgonyi	Ian Whitting
Magnus Wagener	Yongkook Park

The following personnel at Florida Solar Energy Center have contributed to the technical effort covered in this report.

Neelkanth G. Dhere	Shirish A. Pethe
Bhaskar Kumar	Ashwani Kaul

The following personnel at State University of New York at Stony Brook have contributed to the technical effort covered in this report.

Professor Michael Dudley
Dr. Balaji Raghothamachar
Mr. Yi Chen.

EXECUTIVE SUMMARY

The overall objective of this program was to provide NREL with technical results which enhance its capability to improve PV manufacturing technology by developing a PV module: intended primarily for the grid-connected market; qualified for use in systems with voltages up to 1500 volts; with a minimum standard testing conditions (STC) output power of 250 watts using large (at least 15.7cm x 15.7cm) ultra-thin cast multi-crystalline silicon solar cells; and with at least a 16% conversion efficiency. Achievement of the overall objectives of the program is based on efforts in the following areas:

- Improve cast material quality through thermal modeling of the growth process and characterization of cast material.
- Optimize and implement the $Mono^2$ casting process.
- Perform a statistical analysis of the breakage and correlate with previous process steps.
- Establish methods of simulating conditions that cause breakage.
- Use modeling to provide guidelines and a roadmap for further development of high efficiency thin cells.
- Eliminate heavy metals from the screen-print pastes.
- Develop and qualify a high voltage module utilizing materials qualified for use at high voltages (frames, connectors, encapsulant, termination pottant, adhesives and backsheet).
- Establish a high voltage test bed and test modules and BOS at greater than 1000 volts.

In support of this work, BP Solar has subcontracts with North Carolina State University (NCSU), State University of New York at Stony Brook (SUNY) and Florida Solar Energy Center (FSEC).

ACCOMPLISHMENTS

Although this program was terminated after only one year, there were still a number of accomplishments including some that have already been implemented in BP Solar production.

Casting

BP Solar has developed a new casting process ($Mono^2$) that improved silicon material quality. During this program a potential cell efficiency gain of 5% was demonstrated using the $Mono^2$ process. Work on thermal modeling and process development lead to insulation changes that resulted in an 8% increase in factory output of cast silicon. Work in conjunction with North Carolina State University correlated higher concentrations of CrB with regions of low minority carrier lifetime in cast silicon.

Yield Improvements

BP Solar wire saw production was switched from a wafer thickness of 225 μm using 160 μm diameter wire to a wafer thickness of 200 μm using 140 μm diameter wire. These changes increased the yield of wafers per unit length of cast silicon by 10%, directly translating to a 10% increase in production of watts per kilogram of purchased silicon.

Also during the program it was demonstrated that brick polishing could improve downstream yields. We also verified that a 4 point silicon wafer flex test could be used to simulate solar cell production line breakage.

Cell Development

BP Solar modeled solar cell performance and set-up a road map describing how to achieve cell efficiencies in excess of 15% for 100 μm thick cells. BP also demonstrated the potential to utilize screen print pastes that do not contain lead or any other heavy metals. Finally we demonstrated efficiency gains using iso-chemical texturing on multicrystalline silicon cells.

Module Development

In the module area BP Solar completed the preliminary design of products using a molded plastic frame; developed, qualified and implemented a US vendor of anti-reflective coated glass, achieving a 2.4% increase in output power over non-AR glass for all US produced modules; demonstrated that today's cell interconnect design is very fault tolerant; and developed electroluminescence as a technique to inspect the structure of cells within PV modules.

High Voltage Systems

BP Solar subcontract FSEC to build a high voltage test bed and populate it with PV modules. In addition we identified potential safety issues related to operating high voltage PV systems and demonstrated how a dc arcing can occur in PV systems.

TABLE OF CONTENTS

Section **Page**

1.0 Introduction 1
2.0 Baseline Process 2
3.0 Program Efforts 4
3.1 Cast Silicon Material Improvement 4
3.1.1 Thermal Modeling 4
3.1.2 Mono^2 Casting 6
3.2 Improved Yields 13
3.2.1 200µm Thick Wafers 13
3.2.2 Brick Finishing 13
3.2.3 Attachment of Brick Mounting Plate 15
3.2.4 Detection of Cracked Wafers 15
3.2.5 Simulating production line wafer and cell breakage 19
3.3 High Efficiency Cell Development 21
3.3.1 Cell Modeling 21
3.3.2 Lead-Free Pastes 27
3.3.3 Screen Optimization/Screen Print Characteristics 29
3.3.4 Iso-chemical Texturing 35
3.4 Module Development 39
3.4.1 Molded Frame 39
3.4.2 AR-Coated Glass 40
3.4.3 Smaller Cell Module 40
3.4.4 Fault Tolerant Design 42
3.4.5 Electroluminescence as a Technique to Inspect Encapsulated Cells 43
3.5 High-Voltage Systems Integration 48
3.5.1 FSEC Subcontract for a High-Voltage Test Bed 48
3.5.2 Higher Operation Voltages and Module Performance 51

Acknowledgements 52
References 53

LIST OF FIGURES

Figure **Page**

1a Pre-Change Isotherms 4
1b Post-Change Isotherms 4
2 Run Times in Station with Modified Insulation Package 5
3 Defect Distribution Before and After the Insulation Change 5
4 Comparison of Tops of Ingots 6
5 Isotherms within a crucible when an extra heater has been added to the hot zone for targeted side heating. 7
6a Modeling results for case 1 showing the isotherms during crystal growth. 7
6b Modeling results for case 2 showing the isotherms during crystal growth. 8
6c Modeling results for case 3 showing the isotherms during crystal growth. 8
7 Temperature distribution with two different cooling configurations using the HEM method 8
8 Temperature distribution with continued strongly curved growth (red) compared with a faster cycle time configuration (green) 9
9 Multicrystalline (left) and Mono^2 (right) wafers after selective etching. 10
10. Lifetime scan from a multi Si wafer showing good grains (purple) and bad grains (red-orange). 10
11. LTS temperature scan of multicrystalline silicon in a low dislocation density region. 11
12 Lifetime scan of a diffused, hydrogenated Mono^2 wafer and LBIC scan of a finished Mono^2 cell. 12
13 Distribution of Cell Efficiencies for Mono^2, Mono and Multi Cells. 12
14 Box and whisker plot for three groups of 175 µm, 12.5 cm wafers from bricks cut with band saw, no surface polish 14
15 Box and whisker plot of breaking strength for 175 µm thick wafers comparing wafers from polished bricks to low TTV wafers cut from unpolished bricks 14
16 Temperature and Stress Evolution of Different Time Steps With Epoxy Beam Ingot Holder 16
17 Temperature and Stress Evolution of Different Time Steps With Metal Plate Ingot Holder 17
18 Bandwidth of RUV Signal 18
19 Picture of crack on silicon wafer taken with an optical microscope 18
20 Crack on Silicon Wafer as Detected by Hennecke IR Camera 20
21 Examples of 4 wafer strength tests 20
22 Breakage strength for three groups of wafers with different Total Thickness Variations 21
23 Relative Spectral Response vs. Wavelength for Measured and Modeled Multicrystalline Silicon Cell 23
24 Modeled Cell Efficiency vs. Thickness 25
25 Modeled Efficiency vs. Lifetime for two cell thicknesses 25
26 Modeled Front Surface recombination velocity versus Cell Efficiency for two cell thicknesses 26
27 Modeled Cell Efficiency versus Back Surface Recombination Velocity for two cell thicknesses 26
28 Spatial Variation of Specific Contact Resistance for 8 Wafers 30
29 Specific Contact Resistance Maps for Wafers with silicon nitride 32

30 Specific Contact Resistance Maps for Wafers Without silicon nitride 33
31 Sheet Resistance Maps for Wafers With silicon nitride 34
32 Sheet Resistance Maps for Wafers Without silicon nitride 34
33 Alkaline vs. ICT Textured Multicrystalline Si Wafers 36
34 Reflectance of ICT and alkaline etched Multicrystalline Si Surfaces 37
35 Prototype Plastic Frame Module Installed on Concrete Tile Roof 39
36 Voc vs. Irradiance for Modules with Full Size and Half Size Cells 41
37 Isc vs. Irradiance for Modules with Full Size and Half Size Cells 41
38 Pmax vs. Irradiance for Modules with Full Size and Half Size Cells 42
39 Damaged Module Viewed with Electroluminescence vs. Traditional Long Wavelength IR 44
40a Module Made with 200um Mono Cells: Initial – Immediately After Manufacture 45
40b Module Made with 200um Mono Cells: After 1000 Mechanical Cycles – 1.4% Power Loss 46
40c Module Made with 200um Mono Cells: After 1000 Mechanical Cycles and 50 Thermal Cycles – 2.4% Power Loss 47
41 High Voltage Test Bed at FSEC 48
42 High Voltage Test Bed – Modules Mounted with Insulated Stand-offs 49
43a Variation of Leakage Current, RH and Solar Irradiance with Time on 8/25 50
43b Variation of Leakage Current, RH and Solar Irradiance with Time on 8/26 50

LIST OF TABLES

Table **Page**

1 Cast Crystalline Silicon Process Sequence 2
2 CrB concentration measured by DLTS in good and bad regions of multi Si 11
3 Cell Modeling Using PD-1D 22
4 PC-1D Analysis Showing Potential Improvements in Cell Efficiency for ultra-thin cells 24
5 Module Results Using Lead-Free Pastes 27
6 Results of Large Trial Using Low Bow Al Paste 27
7 Performance Using New Al BSF Paste 28
8 Sheet Resistance of Phosphorus-Doped Emitter, Line Resistance for Various Line-Widths and Average Resistivity of Silver Paste after Firing 35
9 Electrical Performance of cells with ICT etch versus cells with alkaline etch 37
10 Comparison of Module Performance Using Cells with ICT or Alkaline Etch 38
11 Cell electrical results for ICT Pilot Trial – 200µm Thick Cells 38
12 Pmax for AFG AR-Coated Glass vs. AR Control 40
13 Isc for AFG AR-Coated Glass vs. AR Control 40

1 INTRODUCTION

The overall objective of this program was to provide NREL with technical results which enhance its capability to improve PV manufacturing technology, by developing a PV module: intended primarily for the grid-connected market; qualified for use in systems with voltages up to 1500 volts; with a minimum standard testing conditions (STC) output power of 250 watts using large (at least 15.7 cm by 15.7 cm) ultra-thin cast multi-crystalline silicon solar cells; and with at least a 16% conversion efficiency. This module must be capable of achieving a 30% reduction in overall manufacturing cost, will carry an extended warranty of at least 30 years, and will not contain any toxic or hazardous materials.

Achievement of the overall objectives of the program was based on efforts in the following areas:

- Improve cast material quality through thermal modeling of the growth process and characterization of cast material.
- Optimize and implement the $Mono^2$ casting process.
- Perform a statistical analysis of the breakage and correlate with previous process steps.
- Establish methods of simulating conditions that cause breakage.
- Use modeling to provide guidelines and a roadmap for further development of high efficiency thin cells.
- Eliminate heavy metals from the screen-print pastes.
- Develop and qualify a high voltage module utilizing materials qualified for use at high voltages (frames, connectors, encapsulant, termination pottant, adhesives and backsheet).
- Establish a high voltage test bed and test modules and BOS at greater than 1000 volts.

BP Solar has been supported in this effort by subcontracts with North Carolina State University (NCSU), State University of New York at Stony Brook (SUNY), and Florida Solar Energy Center (FSEC).

The baseline for this PV Manufacturing R&D program was the polycrystalline process and production line as it existed at the conclusion of BP Solar's previous PVMaT Contract NREL # ZDO-2-30628-03 entitled "Large-Scale PV Module Manufacturing Using Ultra-thin Silicon Solar Cells". [1, 2] This baseline is described in more detail in Section 2.0.

Technical efforts in the program will be discussed in detail in Section 3.0.

2 BASELINE PROCESS

BP Solar's Crystalline Silicon Technology is based on use of cast crystalline silicon wafers. The process flow at the end of NREL Contract # ZDO-2-30628-03 is shown in Table 1.

Table 1
Cast Crystalline Silicon Process Sequence

Casting
Of
265 Kg Brick Ingots

Wire Saw Wafering
225 μm thickness

Cell Process
All Print with Aluminum Back Surface Field (BSF)
&
Plasma Enhanced Chemical Vapor Deposition (PECVD) Silicon Nitride (SiN) AR

Module Assembly
Hot Bar Soldering for Tabbing and Stringing

Lamination
Fast Cure Ethylene Vinyl Acetate (EVA)

Finishing

The various segments of BP Solar's module manufacturing process as practiced at the beginning of this PV Manufacturing R&D program are described below.

Casting
BP Solar has purchased directional solidification equipment specifically designed for photovoltaics. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semi-crystalline silicon ingot. The size of the cast ingot yields 25 – 12.5 cm by 12.5 cm bricks.

Wafering
During the previous PVMaT Programs BP Solar developed wire saw technology for cutting large area polycrystalline wafers and reduced the average wafer thickness in production to 225μm. During the previous PVMaT Program BP Solar demonstrated the ability to wafer and process 200μm thick wafers in the production line.

Cell Process
The cell process sequence is based on the use of Hot Melt metallization system developed during the previous PVMaT program, where commercially available screen-printed silver based hot-melt paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps include: diffusion, firing of the front and back print pastes and PECVD deposition of a silicon nitride antireflective (AR) coating.

Module Assembly

The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. During the previous PVMaT program leaded solder was replaced by lead-free solder for all of the multicrystalline products. BP Solar uses automated hot bar soldering machines to perform the tabbing operation. Tabbed cells are then soldered into strings using hot bar soldering equipment developed in a previous PVMaT program.

Module Lamination

The module construction consists of a low iron, tempered glass superstrate, EVA encapsulant and a Tedlar back sheet. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

During the previous PVMaT Program BP Solar demonstrated a 2.4% increase in STC output power using AR coated glass, qualified the glass through environmental testing and implemented it on some but not all product lines due to the limited availability of qualified AR coated glass.

3 PROGRAM EFFORTS

3.1 Task 1: Cast Silicon Material Improvement

In this task, BP Solar conducted development projects for improvement of cast material by optimizing the thermal profiles used, engineering the grain structure and minimizing exposure to known contaminant sources.

3.1.1 Thermal Modeling

In order to better understand the crystal growth and to improve both the casting station geometry and the process parameters, the casting process has been modeled using a finite element thermal simulation. In the first analysis alteration of the casting station hot zone geometry was evaluated. The geometry of the insulation interior was modified and the model was run to predict run time. Figure 1a shows the modeled isotherms for the standard configuration. Figure 1b shows the modeled isotherms after the proposed change in the insulation package. The model predicted that the change would decrease the total cycle time by about 15%.

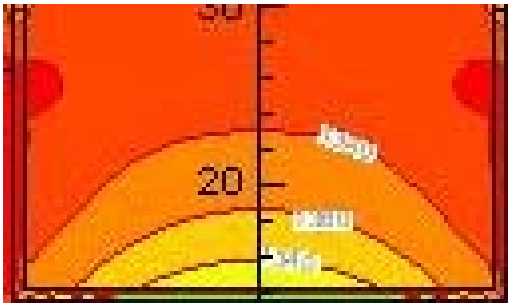


Figure 1a: Pre-change isotherms

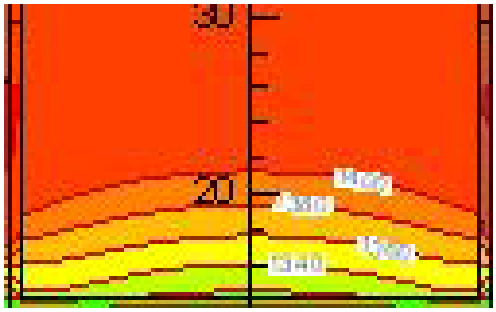


Figure 1b: Post-change isotherms

Guided by the modeling, the proposed changes in the insulation package were made. These resulted in the predicted 15% decrease of total cycle time without introducing cracks in the ingot or lifetime degradation of the resultant material. In fact the lifetime actually improved due to decreased "contamination" resulting from decreased time that the solid is held at high temperature.

Subsequent changes were made to further improve the growth stage and to decrease defects. Figure 2 shows run times for a station during the time period of interest. The average run time was reduced by about 14%.

Figure 3 shows the defect distribution before and after the change with mush (breakdown of crystal structure) eliminated, chips and cracks decreasing dramatically and inclusions increasing modestly. Also energy consumption during casting fell by approximately 18% and sizing cycle time decreased by 15-20% due to the flatter tops of the ingots being produced.

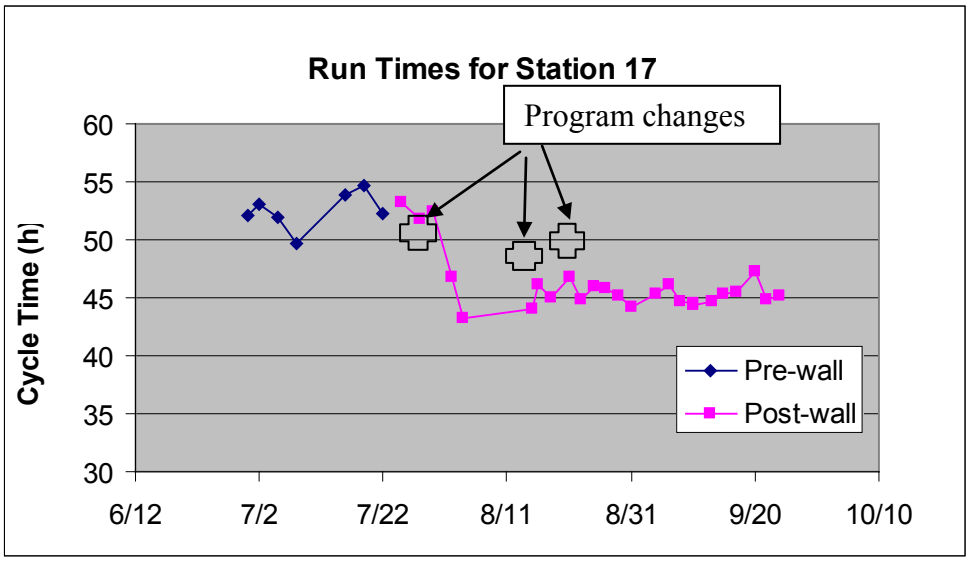


Figure 2: Run Times in Station with Modified Insulation Package

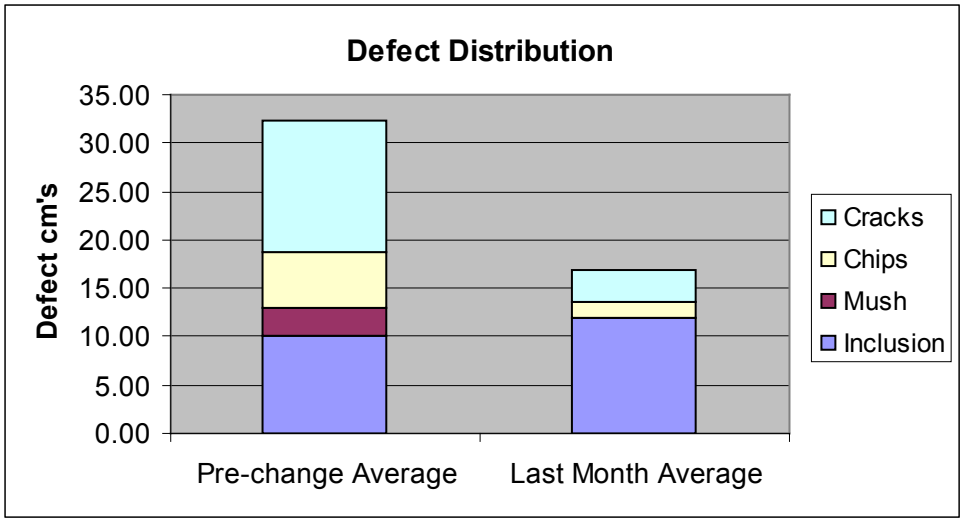
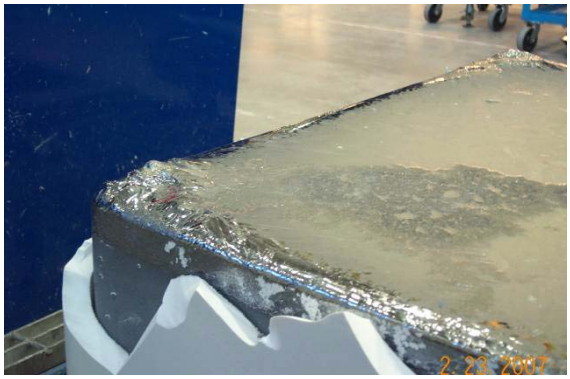


Figure 3: Defect distribution before and after the Insulation Change

In summary, the change in insulation resulted in a reduction in total defects and an increase in the average ingot yield, while the casting run time was cut by 14%. This resulted in a 16% increase in throughput per station for this type of casting stations. This increased the total factory capacity up by 8%.

This type of casting station has always had problems with corner solidification resulting in bulging corners. The sizing saws must cut slowly through a large top area to compensate. Without these high corners, the sizing cycle time could be decreased by 10-15%. The insulation change discussed above helped to solve this problem. Figure 4 shows the tops of ingots made using the old insulation package versus the tops resulting from the new insulation package.

Bad corner from old casting configuration



Average corner from old configuration.

Average corner from new configuration

Figure 4: Comparison of Tops of Ingots

3.1.2 Mono^2 Casting

Recent work at BP Solar has resulted in a new technique for casting ingots with the potential for producing silicon with extremely low defect densities (Mono^2 silicon). The technique involves a proprietary growth nucleation process for the casting of ingots and is used to produce single crystal bricks and wafers or wafers with specifically chosen grain boundaries[3]. The advantage of this process is production of single crystal quality silicon at the cost of a casting process.

3.1.2.1 Modeling of the Mono^2 Growth Process

In the Mono^2 process, the desired growth interface must be as convex as possible, especially at the initial stages of the crystal growth. This causes defects to grow out of the material rather than having more nucleate on the walls and grow in. Several methods for doing this were evaluated, all involving targeted changes to the hot zone configuration. The proposed changes were first

simulated using a finite element thermal simulation package. The most promising methods have been developed successfully as practical solutions.

The first solution involved the addition of an extra heating system into the hot zone. This heater was targeted to heat the sides of the ingot, intending to increase the curvature of the growth interface. Several heater designs and susceptor combinations were investigated. While several embodiments of this approach had the intended effect, it was found that only a mobile heater could fully satisfy the requirements of the entire cycle. Figure 5 gives an example of the heating results we obtained.

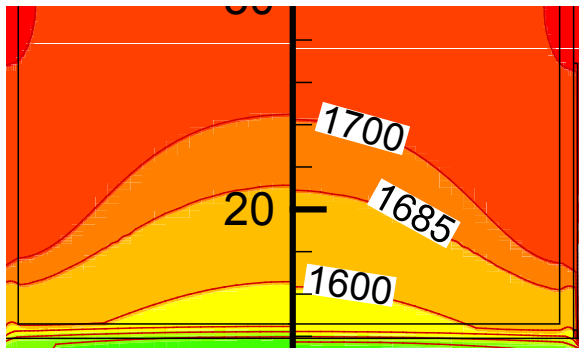


Figure 5: Isotherms within a crucible when an extra heater has been added to the hot zone for targeted side heating.

The second solution involved changing the cooling configuration of the furnace. Again, several solutions were investigated, and often the results of one configuration sparked an idea for the next idea to try. The thermal results of several situations are presented below. While greater curvature was attained, generally the curvature flattens out as growth proceeds. This happened more in some cases than in others.

Case 1 gave little benefit. In case 2 better curvature was obtained. The strongest localized curvature was obtained by active cooling in case 3.

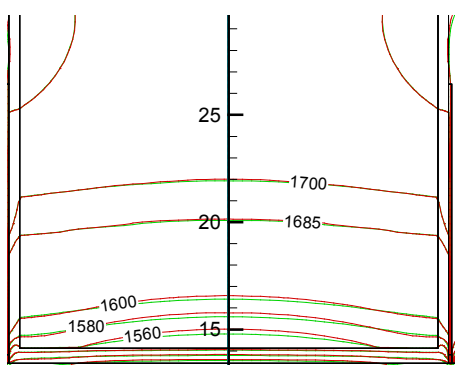


Figure 6.a: Modeling results for case 1 showing the isotherms during crystal growth. Green lines are for standard geometry. Red lines are with altered cooling.

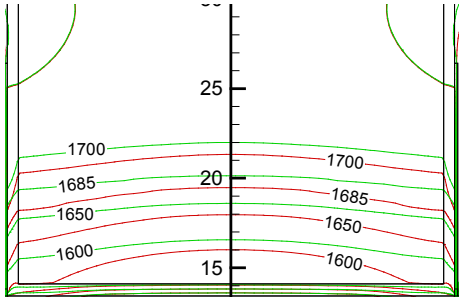


Figure 6.b: Modeling results for case 2 showing the isotherms during crystal growth. Green lines are for standard geometry. Red lines are with altered cooling.

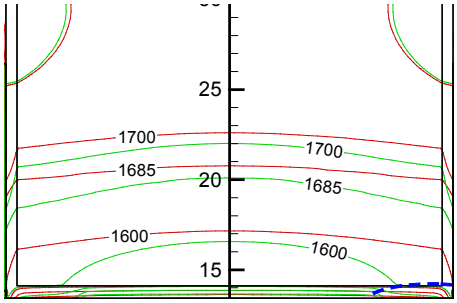


Figure 6.c: Modeling results for case 3 showing the isotherms during crystal growth. Red lines are for standard geometry. Green lines are with altered cooling.

We also investigated the older technology involved in Heat Exchanger Method crystal growth as originated by Schmid and Khattak[4]. Figures 7 and 8 show simulation results obtained using configurations close to the traditional HEM method.

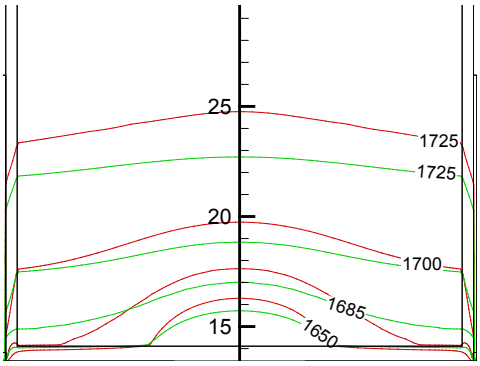


Figure 7: Temperature distribution with two different cooling configurations using the HEM method

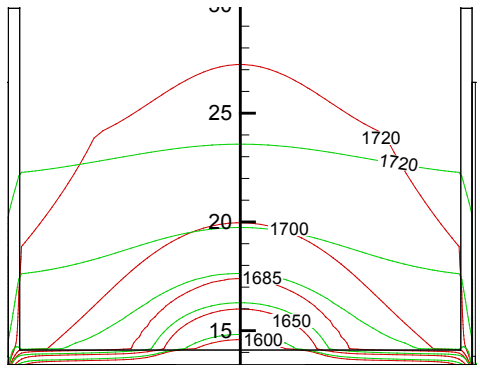


Figure 8. Temperature distribution with continued strongly curved growth (red) compared with a faster cycle time configuration (green)

3.1.2.2 Defect Profiling

A survey of structural defects reveals a considerable difference between traditional multicrystalline cast silicon and Mono^2 silicon. Examples of selectively etched wafers from cast ingots are shown in Fig. 9, where heavily dislocated grains appear as dark regions. Studies of minority carrier lifetime have shown that the dislocation density controls the grain-to-grain lifetime variations in multicrystalline Si even on a sub-millimeter scale as can be seen in Fig. 10. Furthermore, the lifetimes in heavily dislocated grains, with dislocation densities > 10^6 cm^{-2}, do not recover to 'good grain' levels as a result of phosphorus gettering and hydrogen passivation.

The chief benefit of Mono^2 wafers is a broad reduction in dislocation density over multi-crystalline Si, resulting in better gettering and improved overall lifetime. The dislocations that do exist can come from poor growth nucleation or from inclusions incorporated into the bulk of the ingot and causing local stress. In general, the thermal stress inherent in the growth process causes a multiplicative interaction once dislocations are started, increasing the area of dislocations, but not the local density. With proper growth and management of inclusions as developed at BP Solar, this type of behaviour has been all but eliminated. In CZ growth, this type of defect incorporation usually leads to polycrystallinity further up in the ingot due to the long length of the boules. In cast growth, the ingot typically is much shorter than a boule, so dislocation cascades may not produce multi Si regions. Selective etching of Mono^2 wafers has shown that crystal growth can be performed with relatively little dislocation incorporation. In wafers cut from the middle of the height of a brick, the dislocation density was less than 10^3 cm^{-2} over large areas. In some experiments, a relatively homogeneous distribution of $7x10^4$ – $3x10^5$ cm^{-2} was generated. In other experiments, different heterogeneous nucleation sources caused localized regions of high dislocation density.

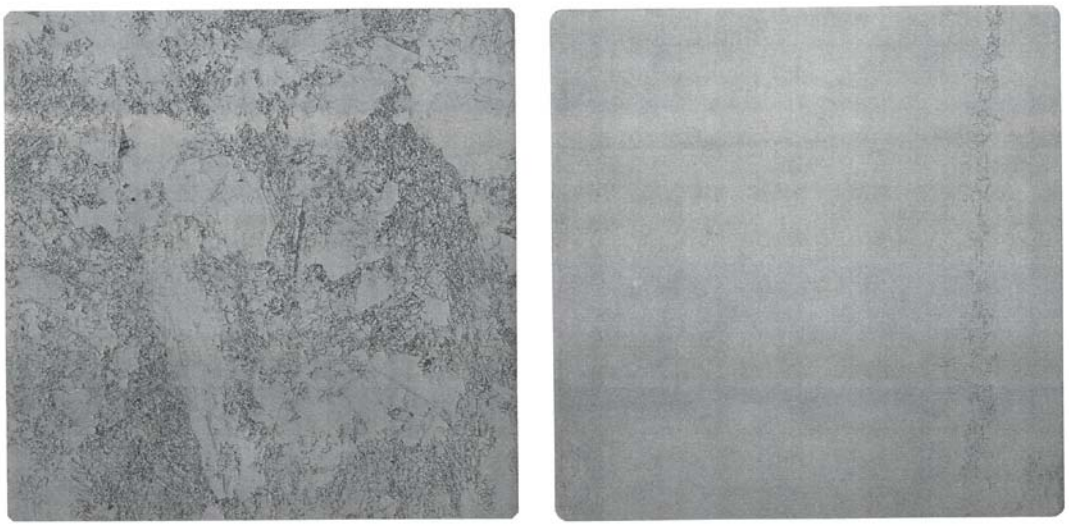


Figure 9. Multicrystalline (left) and Mono[2] (right) wafers after selective etching. Darker areas have higher densities of structural defects, mostly dislocations.

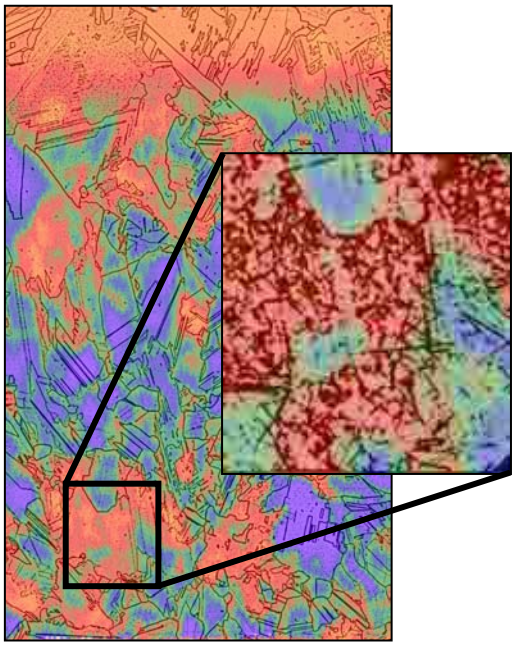


Figure 10. Lifetime scan from a multi Si wafer showing good grains (purple) and bad grains (red-orange). The inset overlays the optical image from a selective etch. Good lifetime correlates with low dislocation density.

In studies of dislocations and lifetime in cast multicrystalline silicon, it has been shown that there is an important behavioral difference between low and high dislocation density regions[5]. Here we go one step further to analyze what elements are responsible for poor lifetime. In grains with low dislocation density (10^3-10^5 cm^{-2}), Deep Level Transient Spectroscopy (DLTS) on as-grown materials shows negligible mid-band trap levels, see Fig. 11. Any lifetime killers are completely precipitated in the as-grown material. Annealing at 900°C and quenching brings out significant

DLTS trap levels resulting from precipitated metals that become dissolved during the anneal. During phosphorus gettering in the range of this thermal budget, precipitated metals in these regions can be nicely gettered, improving the lifetime. Trap A in Fig. 11 has been identified as CrB with an energy of E_v + 0.266 eV and a capture cross section of $2x10^{-16}$. In grains with high dislocation density (>10^6 cm^{-2}), again no traps are detected in the as-grown sample, see Table 2. By contrast, in these regions, there is no effect after annealing at 900°C and quenching. However, annealing at 1200°C followed by quenching in glycol finally reveals some dissolved recombination centers. Metal precipitates in the densely dislocated regions seem to be quite strongly bound to the local structural defects, and seem not to be dissolved into the lattice by typical phosphorus diffusion/gettering conditions. Our studies have corroborated previous work showing that the lifetime of bad areas does not improve during solar cell processing. The cause of the poor lifetime is evidently metal precipitates that are closely entangled in high dislocation areas. For Mono[2] wafers to be successful as solar cells, it is crucial to remain in the lower dislocation density regime in order to allow proper phosphorus gettering.

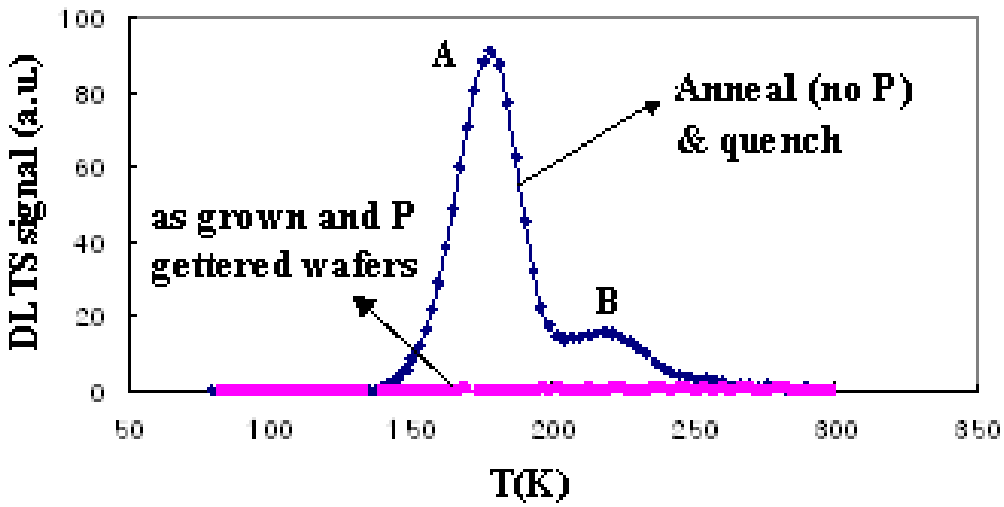


Figure 11. LTS temperature scan of multicrystalline silicon in a low dislocation density region. Two traps are detected only after quenched annealing. These traps disappear again after phosphorus gettering.

Table 2. CrB concentration measured by DLTS in good and bad regions of multicrystalline Si

	As Grown	900°C Anneal + quench	P diffused at 900°C	1200°C + quench
Good Region	No Signal	$3*10^{13}$ cm^{-3}	No Signal	
Bad Region	No Signal	No Signal	No Signal	$2*10^{12}$ cm^{-3}

As-grown p-type Mono[2] wafers have typically had lifetimes averaging from 30 to 50 microseconds, while processed wafers have had averages in the 70-80µs range, see Fig. 12, with large good areas ranging up to lifetimes of 150 microseconds (diffusion length of 680µm). For comparison, multi wafers typically have average lifetimes of 10-20 microseconds as-grown, with a few grains performing as well as Mono[2]. Typical wafers from commercial solar CZ manufacturers have been measured at 40 and 80µs for as-grown and processed material,

respectively. In some cases, the extent of dislocations in Mono^2 increases for wafer positions higher in the brick, but the average lifetime and cell efficiency are basically flat through the height of the brick. As-grown n-type wafers have had minority carrier lifetimes in excess of 100 microseconds.

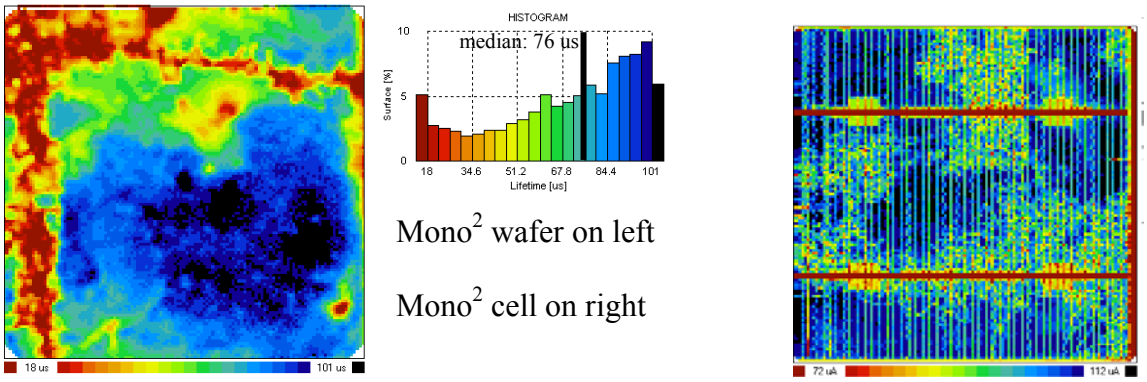


Figure 12. Lifetime scan of a diffused, hydrogenated Mono^2 wafer on left and LBIC scan of a finished Mono^2 cell on right.

Mono^2 solar cells made at BP Solar using standard industrial screen print processing have averaged 16% electrical efficiency for 12.5 cm by 12.5 cm cells, with some cells ranging as high as 17.0% under AM1.5 illumination. Solar cells made on n-type Mono^2 wafers have shown similar promise. On the whole, Mono^2 wafers have had equivalent lifetimes and cell efficiencies to commercially available CZ wafers. See Figure 13.

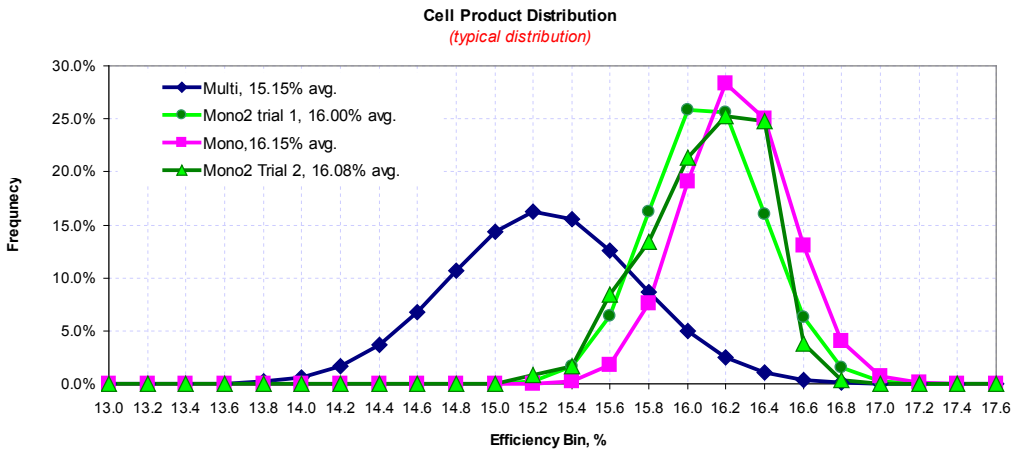


Figure 13. Distribution of Cell Efficiencies for Mono^2, Mono and Multi Cells

3.2 Task 2: Improved Yields

In this task BP Solar studied wafer fracture strength and the formation of micro-cracks in cast multicrystalline silicon wafers and cells in order to improve production line yield.

3.2.1 200µm Thick Wafers

In order to obtain more wafers out of the silicon purchased, an effort to reduce the wafer thickness from 225µm to 200µm was undertaken. During the course of this program a number of experiments were conducted in order to evaluate the potential to make that cell reduction. The following subsections describe some of the technical efforts completed in this task. The net result of this effort was a complete transition of BP Solar production to 200µm wafers by the end of this program.

Also during the course of the program the wire thickness was reduced from 160µm diameter to 140µm diameter with no change in process yield. This change resulted in 5% increase in wafers cut and a corresponding 5% increase in output wattage of modules produced per kg of silicon purchased.

Further efforts to reduce the wafer thickness to 180µm are underway. During this program a number of experiments were conducted using 175 to 180µm thick wafers. Equipment and process requirements for transitioning to 180µm thick wafers have been identified and are now being addressed under BP Solar's Technology Pathways Partnership SAI Program.

3.2.2 Brick Finishing

The possibility that surface roughness may affect wafer strength and yield was investigated. Several silicon bricks were sent to a manufacturer that specializes in surface finishing methods. Bricks that were surface finished were cut into 200µm and 160µm wafers and the cutting yield, strength and line yields assessed vs. standard production.

Data collection and analysis included wafer 4-point bending strength, thickness and TTV (total thickness variation) across an entire brick, surface finish and roughness of the wire sawn face and mechanical yield through industrial cell processing sequences.

The bricks were evaluated for homogeneity of cut-through using thickness measurements of wafers of the entire brick. Variation in average thickness was approximately 2µm front to back indicating minimal wire wear utilizing the 140µm wire. Average thickness variation across a wafer was on the order of 25µm.

4-point bend tests showed that wafers were not any stronger, but were more uniform toward the upper end of the distribution and had fewer weak wafers. Mechanical yield through the industrial cell processing sequence showed the benefits of several points of yield which correlates well with the 4-point bend tests.

12.5cm x 12.5cm wafers from both polished and unpolished bricks were cut on a wire saw at 175um thickness with 140um wire. TTV was measured and the strength testing was performed using the 4-point flex test. Three groups of 50 wafers each were tested. Indications were that the wafers with low TTV were stronger as measured by the 4-point flex test at the 95% confidence level.

Tests on polished bricks indicated no statistical difference in wafer strength between the low TTV unpolished group and the randomly selected group with polished edges. The polished bricks did show a statistical difference in wafer strength from the higher TTV wafers cut from unpolished bricks. The low TTV wafers cut from polished bricks did not show any statistical difference with the randomly selected wafers cut from polished bricks as shown in Figures 14 and 15.

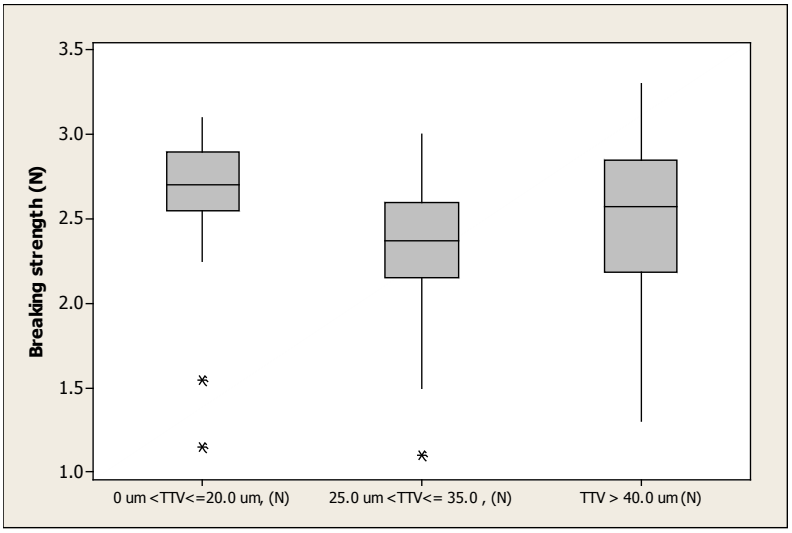


Figure 14. Box and whisker plot for three groups of 175 µm, 12.5 cm wafers from bricks cut with band saw, no surface polish

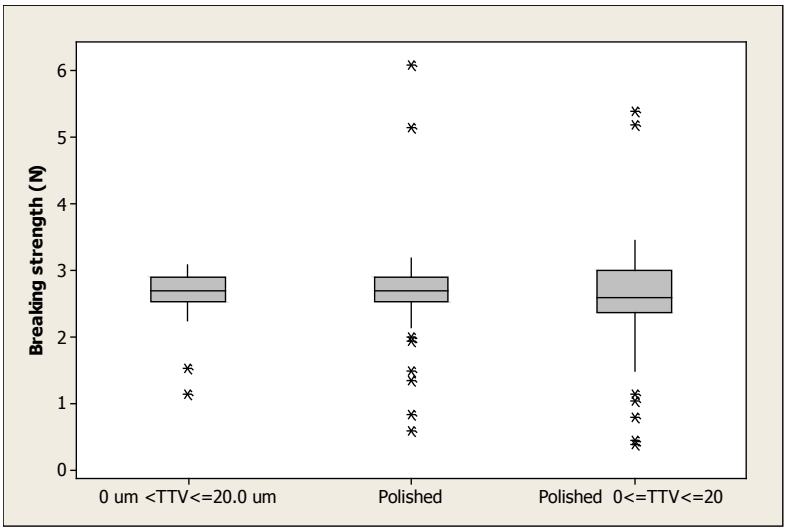


Figure 15. Box and whisker plot of breaking strength for 175 µm thick wafers comparing wafers from polished bricks to low TTV wafers cut from unpolished bricks

Experimental evidence indicated that better downstream yields were attained with polished bricks than with those used directly off the band saws used for sizing. However, with polished bricks a particular failure called a "sad face crack" occurs and appears to be related to how the polished brick surface is glued to the mounting plate before it is inserted into the wire saw. The present adhesive is thermally cured. Trials were run and modeling was performed to see if the sad face cracks were due to thermal stress caused by the adhesive (see section 3.2.3). Results indicated that the use of a slow cure adhesive with polished bricks is a valid method for improving yield.

Brick polishing has been recommended to manufacturing based on its reducing the surface damage of the brick, thus decreasing the probability of crack propagation from the outside of the wafer.

3.2.3 Attachment of Brick Mounting Plate

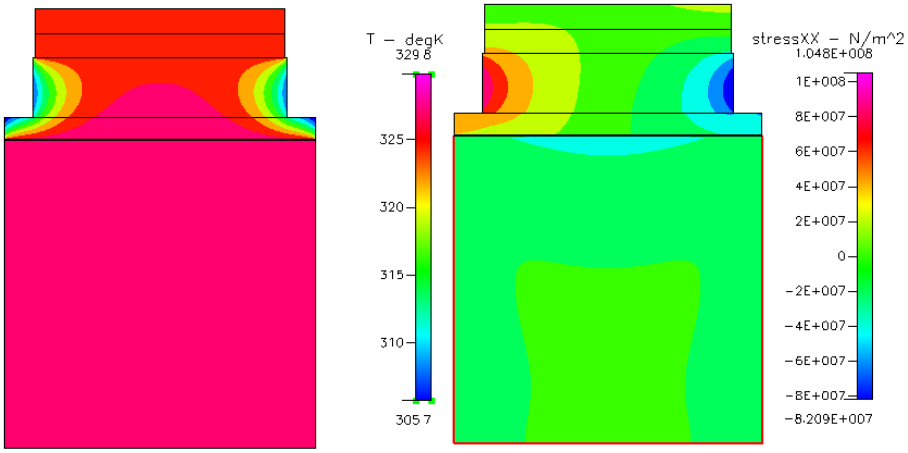
An elastic thermal stress model was set up to study the temperature and stress evolution using different ingot holder materials. Results for use of an epoxy beam are shown in Figure 16. Results for use of a metal beam are shown in Figure 17. The temperature distribution resulting from a metal plate was more uniform for the same time step due to the larger thermal conductivity of metal compared to the epoxy beam. For the stress distribution, the shape of stress after 10,000 time steps is similar; however, the magnitude is one order lower with the metal plate ingot holder. In addition, both the thermal expansion coefficient of metal and the deformation of metal during temperature change are smaller, thus inducing less stress.

Next an experiment was performed to evaluate three (3) new glues that were expected to result in less stress on the ingot. Two of the three were found to be not strong enough for use in the wire saw process. The slow cure glue had excellent results and is being utilized in further experiments

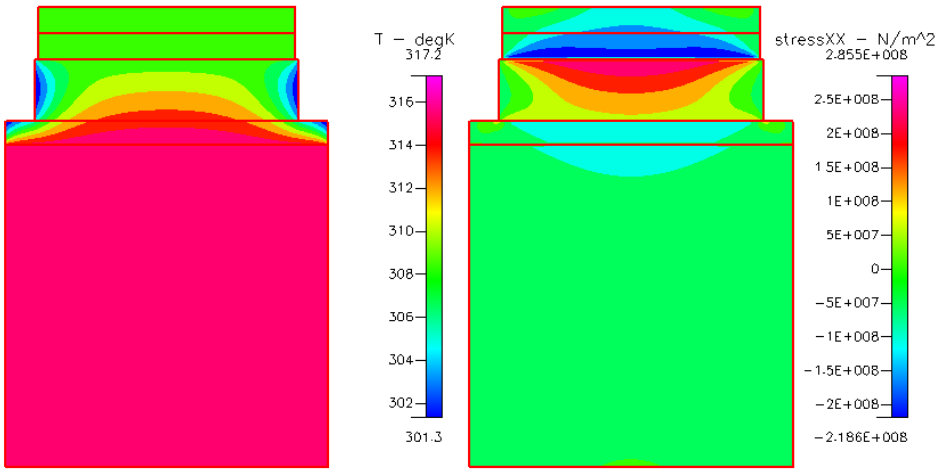
3.2.4 Detection of Cracked Wafers

The University of South Florida has developed Resonance Ultrasonic Vibrations (RUV) equipment that uses ultrasonic vibrations to detect wafers with microcracks that will not survive through the cell line. Longitudinal resonances are excited and detected. The amplitude, peak position and bandwidth of the detected resonances were monitored to see if any or all of these allowed us to separate mechanically sound and unsound wafers. The most indicative response was the bandwidth followed by the peak height. Peak position was deemed too random to be useful. It does seem to be possible to pick out anomalous wafers; however, it did not seem to be possible to set up a simple rule. This is illustrated in Figure 18.

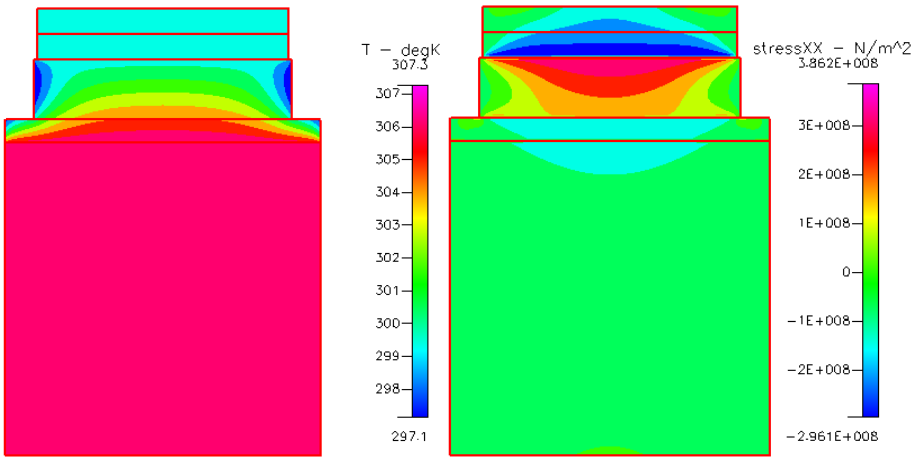
The discrimination of good and bad wafers requires a complicated algorithm (human judgment at this point). Nonetheless, 1600 wafers were sorted, eliminating suspect wafers. These will be run through the cell line in order to determine if the mechanical yield is better than normal. The results however were not conclusive partly because so few wafers were rejected by the equipment.



(a) 1000 time steps

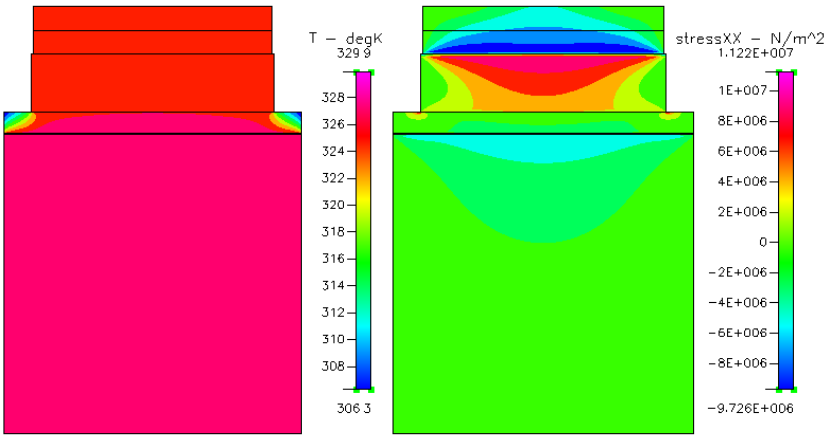


(b) 5000 time steps

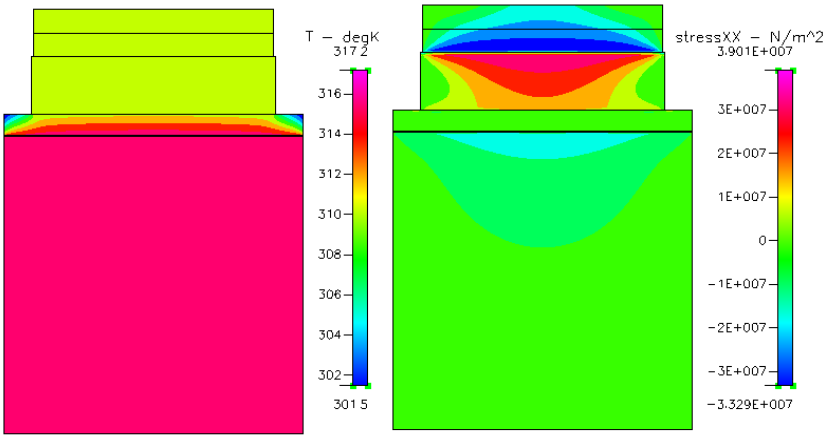


(c) 10000 time steps

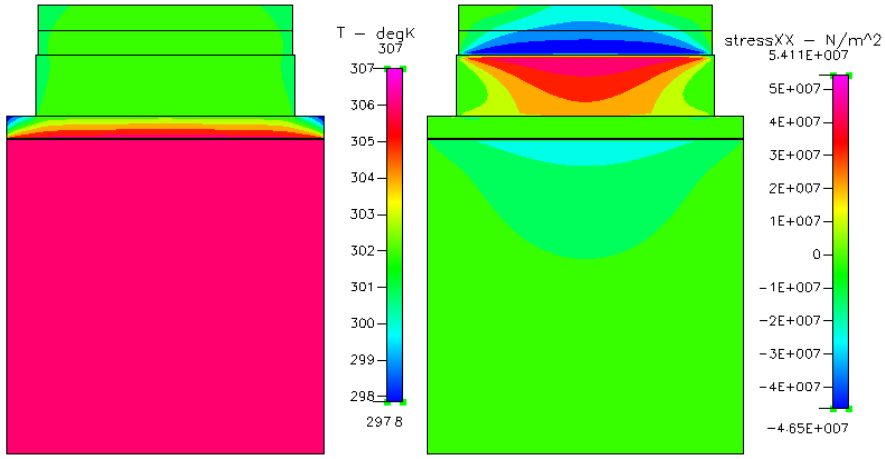
Figure 16. Temperature and stress evolution of different time steps with epoxy beam ingot holder



(a) 1000 time steps



(b) 5000 time steps



(c) 10000 time steps

Figure 17. Temperature and stress evolution of different time steps with metal plate ingot holder

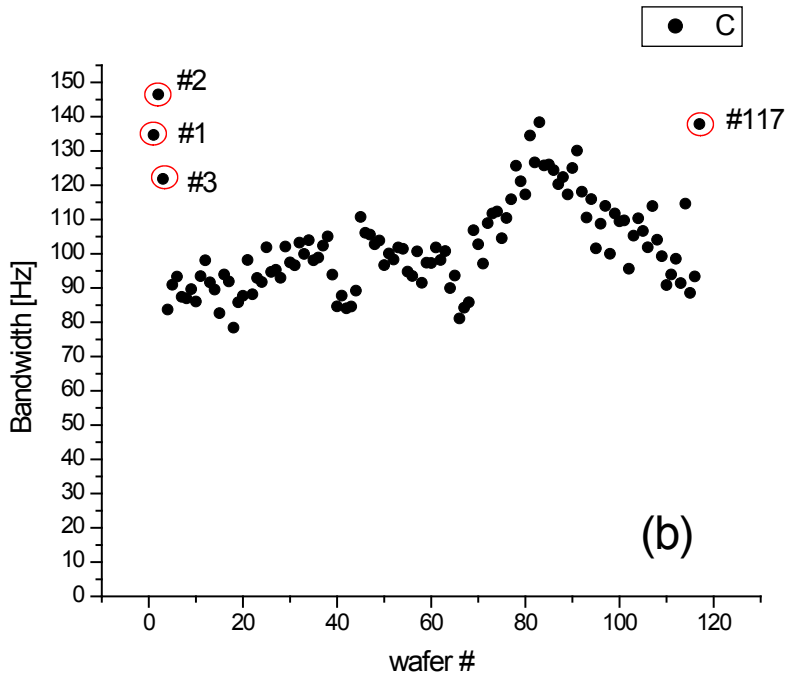


Figure 18: Bandwidth of RUV Signal

Two Hennecke machines designed to detect and sort out wafers with chips and cracks were purchased and underwent trials. They have proven capable of detecting small chips on wafer edges. In addition, the IR cameras in the machines are capable of detecting small cracks. A wafer was tapped lightly to produce a crack in it. The crack as viewed under the light microscope is shown in Figure 19.

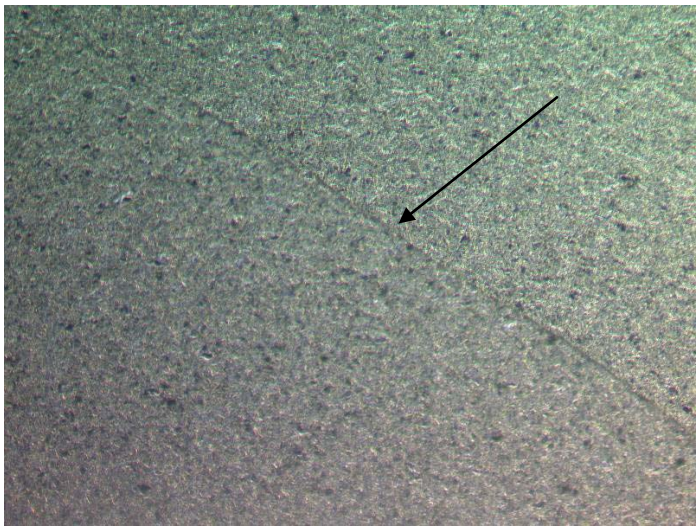


Figure 19. Picture of crack on silicon wafer taken with an optical microscope

The same wafer was run through the Hennecke inspection system to determine if it could identify the crack with the IR camera. A picture taken by the IR camera is shown in Figure 20.

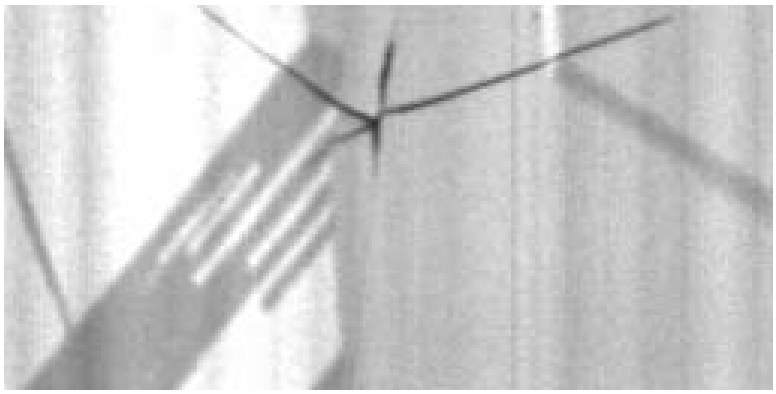


Figure 20. Crack on silicon wafer as detected by Hennecke IR camera

The systems are being used in BP Solar production to sort out chipped and cracked wafers before beginning the cell process.

3.2.5 Simulating production line wafer and cell breakage

As thinner silicon wafers are utilized they may become more and more fragile. The reduction in mass of wafers leads to a decrease in the strength of the wafer, possibly leading to higher breakage in post wire saw processing. It would be useful to determine a method to predict the yield of a set of wafers through the production process.

There are several different ways to measure the strength of a silicon wafer. The ring on ring setup stresses the wafer in the middle. However, this test results in data that is more indicative of the damage on the surface of the wafer. Other strength tests bend the wafers resulting in stress to the edge of the wafer as well as the middle of the wafer. Some of the tests that fall into this category include the point bending, the 4 point flex test, the 4 line bend test, and the three line bend test. Examples of four different types of bending tests along with plots of their displacement and the resultant stress levels are shown in Figure 21.

The four point flex test was selected for this effort because BP Solar has traditionally used this test and has already acquired some preliminary data on this tester. We have observed that wafers with less thickness variation (lower TTV) typically have higher yields though the production line. Therefore, if the four point flex test could measure a difference as a function of TTV it is likely that it could be used as a tool to identify process and handling changes that would increase yield.

Wafers (12.5cm by 12.5cm) were cut on a wire saw at 175µm thickness with 140µm wire. Thickness variations were measured and the wafers were sorted into the following three groups.

Group 1 0 µm <= TTV<=20.0 µm

Group 2 25.0 µm <= TTV<= 35.0 µm

Group 3 TTV >= 40.0 µm

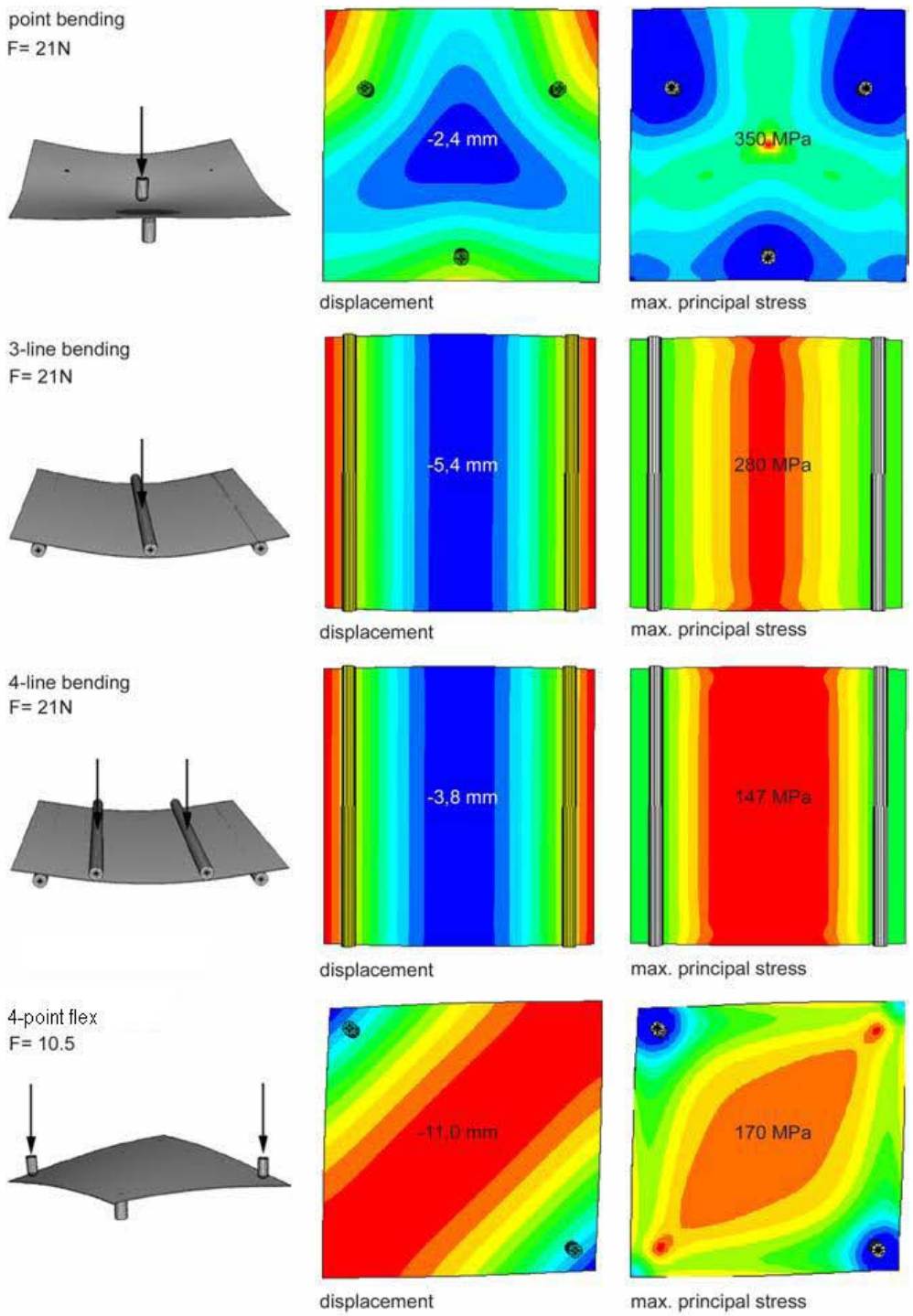


Figure 21: Examples of 4 wafer strength tests[6]

A set of 50 wafers from each group were tested to failure using the four point flex test. A box and whisker plot of the data is shown in Figure 22. There was a statistical difference in wafer strength between group 1 and groups 2 and 3 indicating that the wafers with low TTV are stronger than the wafers with higher TTV using the four point flex test at the 95 % confidence interval.

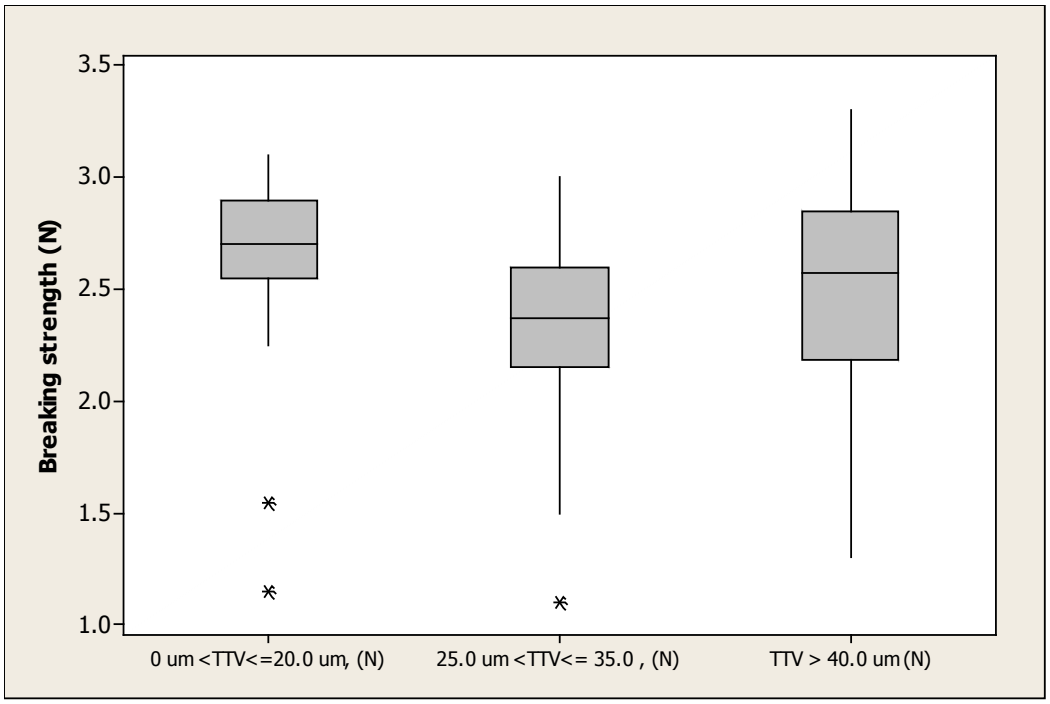


Figure 22: Breakage strength for three groups of wafers with different Total Thickness Variations

3.3 Task 3: High Efficiency Cell Development

This task was expected to result in a road map for increasing cell and module efficiency and successful transfer to production of a lead-free cell process.

3.3.1 Cell Modeling

PC-1D base simulation has been used to model various losses that limit silicon solar cell efficiency and to provide guidelines for further technology improvements as we head toward 100µm thick cells. The AM1.5 global spectrum from ASSTM G173-03 and/or IEC 60904-3 was used to calculate the fundamental limiting losses for a single band-gap silicon solar cell.

There are fundamental or unavoidable losses associated with any solar cell. For crystalline silicon these are:

- 27.8% loss as long wavelength light escapes as Si becomes transparent at these wavelengths.
- 25.2% thermalization loss as extra energy is wasted as heat assuming unit quantum efficiency; that is each photon produces one free electron-hole pair.
- A further intrinsic (radiative & Auger) loss of 17.2%.

These yield a theoretical device efficiency of 29.8% with the AM1.5 spectrum.

There are also avoidable losses which we have modeled for today's cells as:

- 6.6% optical loss
- 6.5% surface and volume recombination losses
- 1.4% loss from parasitic resistance effects.

This yields a usable output of 15.3%, a typical value for our mc-Si solar cell. A detailed look at the avoidable losses will be made in order to develop a plan for increasing cell efficiency.

PC-1D program modeling was utilized to match both the I-V measurements and the quantum efficiency (QE) of the baseline cell. None of the standard emitter diffusion profiles included in PC-1D could yield a match for both the I-V curve and the QE versus wavelength measurements. A reasonable match could only be attained by inputting the diffusion profile from SIMS measurements on actual cells and the reflectance measurements made similar cells. Once these were used as input parameters the performance for both I-V and QE could be matched. Table 3 shows the input parameters used to achieve a match of the model. These parameters will now be used as baselines for evaluating the sensitivity of the present cell structure to changes in thickness, material lifetime, surface recombination velocities and internal reflection.

As can be seen the match of I-V parameters is very good. Figure 23 shows measured vs. modeled quantum efficiency. The match is quite good over the entire wavelength range.

Table 3: Cell Modeling Using PC-1D

Base modeling - for 250 micron multicrystalline cells

PC1D input values	Simulation	Remarks
Metal coverage factor	8.20%	; 143.4cm^2 active area
Reflectance	Measured Reflectance data	; Reflectance Data (approximated from bare 270 microns cell)
Cell thickness	250µm	; simulated & real to match with light escape
Within band absorption	Free carrier absorption	; should be enabled…
Int. optical reflectance	75/92 Front and 75/80 rear	; simulated to match
Lifetime	28µS	; simulated to match mid portion of QE
Bulk Resistivity/doping	0.99 ohm (1.513 x 10^{16} cm^3)	; Typical Material
Front Doping	Measured _SIMS data	SIMS DATA
J_{01} & J_{02}	1.1e-10A J01 & 5.62e-6A J02	; simulated for bare, unencapsulated cells
AL BSF	5e^{18} conc. and 10µm depth, uniform	; simulated to match mid/long lambda response
FSRV	100,000cm/sec	; simulated to match short lambda response
BSRV	800cm/sec	; simulated to match long lambda response
Shunt	20 Ohm	; approximated, typical
Resistive series	2.5 & 11 mOhm front & rear	; assumption /typical (to match encapsulated Rs/FF)

Results

Voc	**0.6103 mV**	; Base reference: 0.610mV
Isc	**5.188 A**	; Base reference: 5.20 Amp
Pmax	**2.291 W**	; Base reference: $2.29W_{encapusulated}$
Eff	**14.66%**	; Base reference: 14.6%

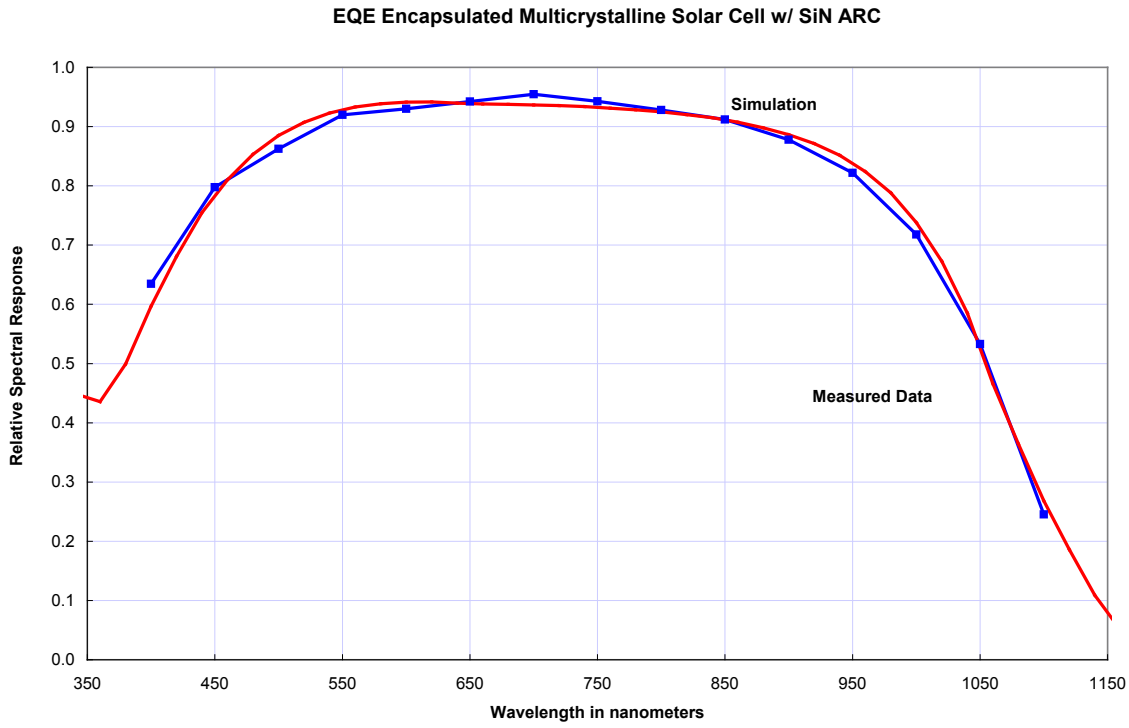


Figure 23: Relative Spectral response versus wavelength for measured (blue points) and modeled (red line) for multicrystalline silicon cell

Table 4 compares the baseline parameters chosen for 250µm thick cells and with the modeled results of a 100µm thick cell. The model for the ultra-thin cell includes an increase in bulk lifetime based on the switch to Mono[2], an increase in the internal reflection, a decrease in the front surface recombination velocity (FSRV) based on the use of an oxide passivation layer and finally a decrease in the back surface recombination velocity (BSRV) based on replacing the Al paste BSF for ultra-thin cells. This modeling indicates one route to achieving approximately 16% efficiency for ultra-thin cells. It does not include any gains achievable from selective emitters or improved metallization geometry.

A number of plots were generated in order to better understand the sensitivity of cell performance (especially efficiency) on the modeled parameters. Figure 24 shows a plot of cell efficiency vs. thickness. The maximum efficiency occurs at a cell thickness of 150µm. The difference in efficiency between 150µm and 100µm is from 14.67% to 14.605% for the baseline properties. This difference can be reduced via the use of better back surface passivation.

Table 4: PC-1D Analysis showing Potential Improvements in Cell Efficiency for ultra-thin cells

PC1D input values	Base Cell – 250 micron	Modeled Cell – 100 micron	Remarks
Metal coverage factor	8.20%	8.20%	No improvement considered
Reflectance	Measured Reflectance data	Measured Reflectance data	No improvement considered
Cell thickness	250µm	100µm	
Within band absoprtion	Free carrier absorption	Free carrier absorption	
Int. optical reflectance	75/92 Front and 75/80 rear	90/95 Front and 90/95 rear	; **20% improvement considered for Internal Reflection**
Lifetime	28µS	100µS	**; ~ 3 to 4 fold carrier life time improvement considered**
Bulk Resistivity/doping	0.99 ohm (1.513 x 10^{16} cm^3)	0.99 ohm (1.513 x 10^{16} cm^3)	No improvement considered
Front Doping	Measured _SIMS data	Measured _SIMS data	No improvement considered
J_{01} & J_{02}	1.1e-10A J01 & 5.62e-6A J02	1.1e-10A J01 & 5.62e-6A J03	No improvement considered
AL BSF	$5e^{18}$ conc. And 10µm depth, uniform	$5e^{18}$ conc. And 10µm depth, uniform	No improvement considered
FSRV	100,000cm/sec	10,000cm/sec	**; One order magnitude improvement considered**
BSRV	800cm/sec	500cm/sec	**; 37.5% improvement considered for Internal Reflection**
Shunt	20 Ohm	20 Ohm	No improvement considered
Resistive series	2.5 & 11 mOhm front & rear	2.5 & 11 mOhm front & rear	No improvement considered
Results			
Voc	**0.6103 mV**	**0.629 mV**	**; 3% improvement achievable**
Isc	**5.188 A**	**5.300 A**	**; 2% improvement achievable**
Pmax	**2.291 W**	**2.429 W**	**; 6% improvement achievable**
Eff	**14.66%**	**15.55%**	**; 6% improvement achievable**

Figure 25 shows a plot of cell efficiency vs. minority carrier lifetime for two thicknesses (250µm and 100µm). As expected the thicker cell takes more advantage of the better lifetime. In the region we are in today (~20 to 30ms) there is little difference between the efficiencies expected from the two thicknesses.

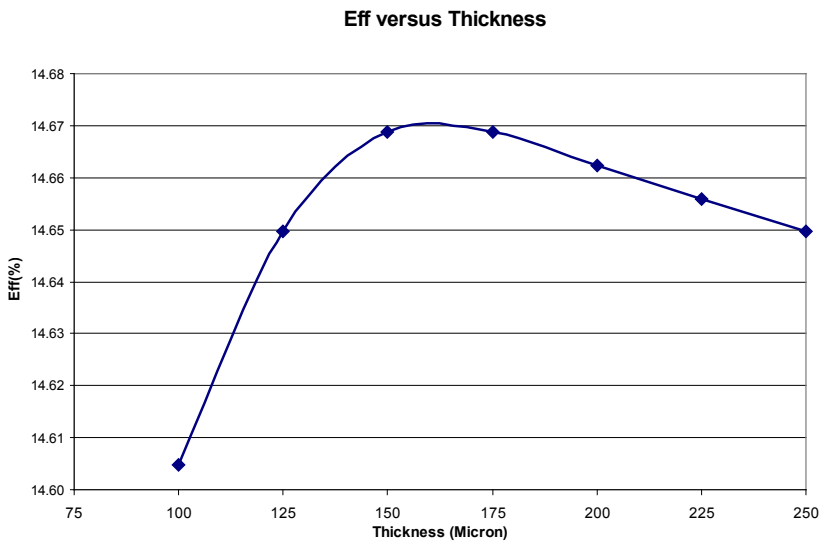


Figure 24: Modeled Cell Efficiency vs. Thickness

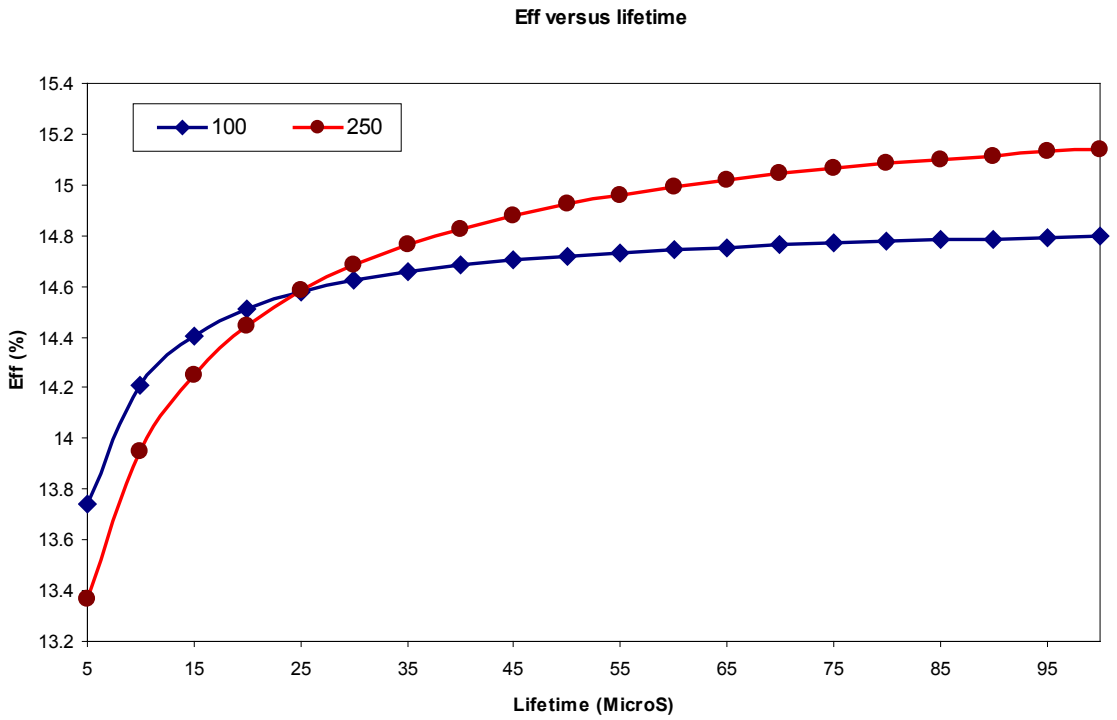


Figure 25: Modeled Efficiency vs. Lifetime for two cell thicknesses

Figure 26 shows a plot of cell efficiency vs. front surface recombination velocity (FSRV). As expected there is little difference in this dependence as a function of cell thickness. Since our baseline analysis indicates that we are at about 100,000 cm/s today, there is significant room for efficiency improvement (from 14.7% to 15.05%) from this parameter.

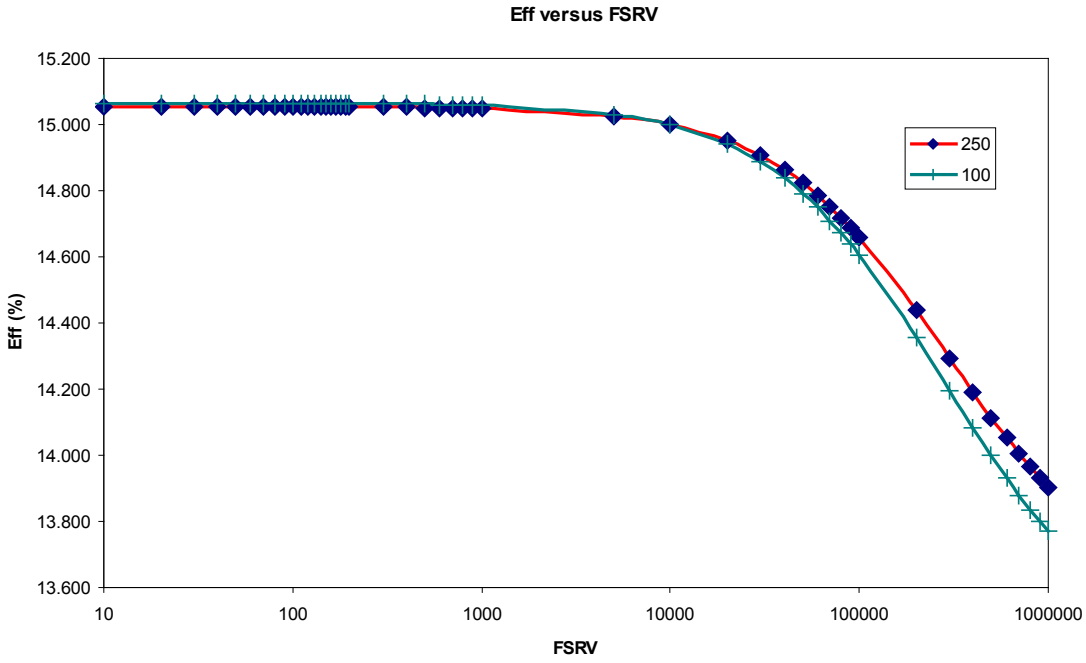


Figure 26: Modeled Cell Efficiency versus Front Surface Recombination Velocity for two cell thicknesses

Figure 27 shows a plot of cell efficiency vs. back surface recombination velocity (BSRV) for thick and thin cells. As expected there is a significant difference in this dependence as a function of cell thickness since the BSRV has more influence in thinner cells. By improving the BSRV we should be able to achieve a small gain in efficiency for 250µm thick cells and a much larger improvement for 100µm thick cells.

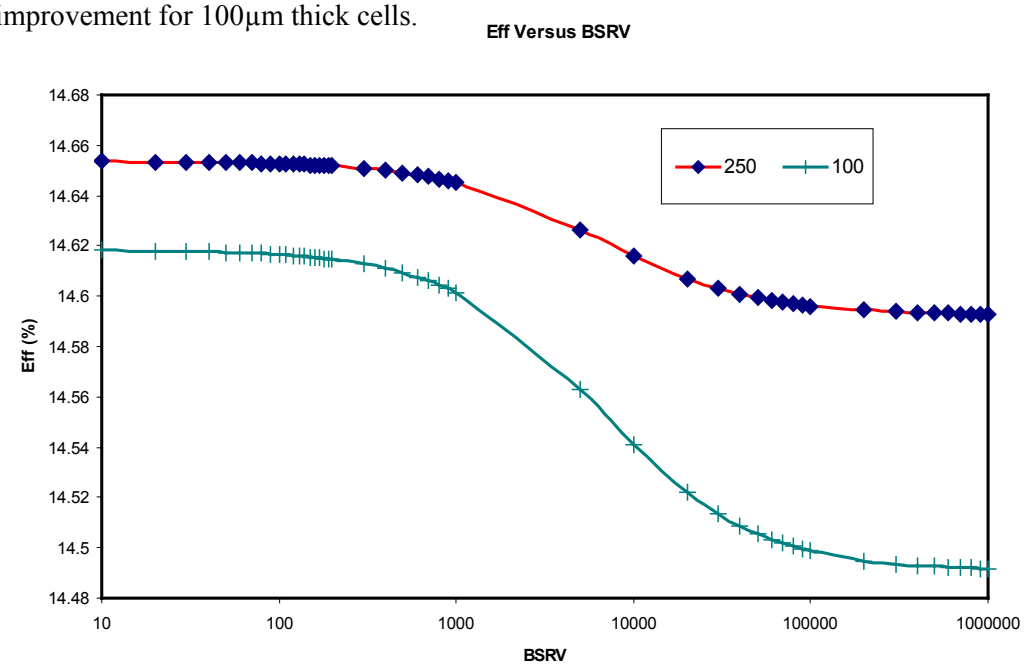


Figure 27: Modeled Cell Efficiency versus Back Surface Recombination Velocity for two cell thicknesses

3.3.2 Lead-Free Pastes

One of the goals of our program was to develop a cell process using screen print pastes that do not contain heavy metals, particularly lead. In addition, we are trying to develop processes for ultra-thin solar cells, so the no-lead BSF paste should be designed to reduce the bowing normally caused by Al paste BSF. Ferro provided us with a lead free Al-Ag paste for back contacts and two lead free Al paste for the BSF. Module results (36 cell) from both the lead-free, low bow Al pastes and a lead-free Al-Ag back contact paste are summarized in Table 5. In all three cases the lead-free pastes produced more power at the module level than the control paste.

Table 5: Module results using lead free pastes

Samples	Voc (V)	Isc (A)	Pmax (W)	FF (%)
Control	**22.036**	**5.126**	**82.447**	**72.9**
BSF A	**22.02**	**5.198**	**84.564**	**73.9**
Delta to control	**-0.08%**	**+1.4%**	**+2.57%**	**+1.37%**
BSF-B	**21.969**	**5.164**	**83.508**	**73.6**
Delta to control	**-0.3%**	**+0.74%**	**+1.29%**	**+0.96%**
BSF A + Al/Ag	**21.97**	**5.177**	**84.26**	**74.0**
Delta to control	**-0.3%**	**+0.99%**	**+2.2%**	**+1.51%**

A pilot trial was performed using ~ 102,000 125mm square, 200um thick multicrystalline silicon wafers in order to evaluate the electrical and mechanical performance of the candidate low bow paste. Standard process conditions were used throughout the production line. The low bow cells had an average bow of 0.4 to 1.8mm while the control group had a bow of 1.3 to 3.3mm. Results are summarized in Table 6. The low bow paste performed better in terms of yield and average cell efficiency.

Table 6 – Results of Large Trial using low bow Al Paste

	Low Bow Al Paste	**Control Al Paste**
Total Quantity of Cells	50,151	52,339
Final Yield (%)	86.03	84.74
Efficiency (%)	15.4	15.3
Voc (mV)	609.8	608.8
Isc (A)	5.263	5.301
FF (%)	75	74

A Design of Experiments (DoE) was conducted to evaluate the performance (cell efficiency and bowing) of thin wafers. This was done in support of both cell and yield tasks. Variables in the experiment were:

- Paste type: Comparing our standard Al BSF paste with a specially formulated low bow paste
- Paste weight: Comparing our standard amount of paste with a 15% reduction
- Furnace firing temperature: Comparing our standard with both higher and lower firing temperatures
- Furnace belt speed: Comparing our standard speed with 10% faster and 10% slower speeds

- Wafer thickness: Comparing ~ 180µm thick wafers with ~ 190µm thick wafers.

The results are summarized below:

- The variable with the most impact on both efficiency and bow was the firing temperature. Both were optimized at the lowest firing temperature used in the trial.

- As expected, thinner wafers bowed more than thicker wafers; however wafer thickness (in the range evaluated) had no impact on cell efficiency.

- Belt speed had no impact on bowing. It does have an impact on efficiency at higher firing temperatures (faster being better), but it has no impact at the lower firing temperature that provided the best efficiency and lowest bow.

- As would be expected, reduced paste weight resulted in less bowing; however it had no effect on cell efficiency.

- The most surprising result was the impact of the paste type. The "low bow" paste actually caused more bowing and lower cell efficiency than the conventional paste, although the bowing difference was insignificant due to measurement variation. These effects are minimized at the lowest firing temperature. At the lowest firing temperature and highest belt speed, the low bow paste improved cell efficiency by 0.3% absolute.

It was concluded that our standard Al BSF paste can be used for 200um thick cells as long as the low firing temperature and reduced paste weight are utilized.

Two trials were then conducted to evaluate low bow, lead-free Al BSF pastes:

1. Paste #1: To evaluate the main effects and the interactions of process factors (paste weight, co-firing temperature and belt speed) on both performance and the observed phenomenon of selective surface blistering.

   Summary of Results:

   - Temperature was found to be a major driving factor affecting blistering
   - Paste weight seems to be a minor contributor to blistering on the surface
   - Good surface finish was achieved at elevated temperatures where good efficiency also occurred.
   - Minor blistering (microscopic level) was still seen at the edges, indicating that the emulsion height may be a possible contributor.

2. Paste #2: To evaluate mechanical and electrical performance of an Al paste from a new vendor. This paste was tested on 200µm thick multicrystalline as well as on thin monocrystalline Si wafers. Table 15 shows the electrical performance results.

Table 7: Performance using new Al BSF Paste

Material	Efficiency (%)	Voc (mV)	Isc (A)	FF (%)
Multi	**15.5**	**615**	**5.32**	**74.1**
Mono	**16.5**	**620**	**5.34**	**76.7**

Summary of Results:

- Bow of ~ 1mm in multi cells and ~ 1.8 – 3.3mm in mono cells was observed
- Observed Al peel-off adjacent to the buss bar for both multi and mono
- Electrical performance was found to be comparable to the standard Al BSF paste for both multi and mono 12.5 x 12.5 cm cells.

Screening of a number of lead-free, low bow Al back pastes was then undertaken. In general, all were found to be comparable with the standard paste. A trial to compare mechanical and electrical performance of several low bow Al BSF pastes was performed. All lots processed at low drying temperatures performed poorly electrically. On 200µm thick wafers the bow was <1mm. Several resulted in beads of Al on the back, others yielded good surface finishes with electrical results equivalent to our standard paste.

Another trial was conducted in order to compare the mechanical and electrical performance of low bow Al BSF pastes with our standard Al back paste using 200µm thick mono wafers. The low bow paste appears more sensitive to the printing set-up and yielded more cosmetic rejects. However, it did result in less bow of the cells (all <2mm) while the cells with standard paste averaged 2.6mm bow. There was no statistical difference in cell efficiency between the two groups.

3.3.3 Screen Optimization/Screen Print Characterization

The top metallization grid is a critical element in determining the efficiency of a solar cell. It is suspected that the Ag-based screen print paste used for fabricating the top metallization occasionally exhibits variations in composition that in turn contribute to variations in the measured efficiency and fill factor of a manufactured solar cell. The objective of this study is to develop a characterization method for monitoring screen print paste variability from one lot to the next and as a function of process variability.

The current transmitted across a metal/semiconductor contact is associated with a contact resistance which depends on the area and/or geometry of the contact. However, the specific contact resistance is an area- and geometry-independent parameter. It depends essentially on the material properties of the semiconductor, contact metallization and the metal/semiconductor interface. Hence, if the structure and doping of the silicon is consistent, measuring the specific contact resistance may provide direct evidence of the variation of the Ag paste over various lots and shed some light on the resulting Ag/Si interface.

Multi wafers with a doped emitter and silicon nitride AR layer were patterned using a special screen designed to evaluate the contact properties. The standard Ag paste used in BP Solar production was screen printed onto the multicrystalline wafers. The sample wafers were subsequently screen printed on their back side with Al and Ag pastes and co-fired under baseline conditions. Afterwards, 2-point probing was performed to measure the total resistance for each contact. The specific contact resistance values were then extracted from those measurements.

Figure 28 shows the spatial distribution of the specific contact resistance for eight different wafers. In many cases the calculated specific contact resistance values increase or decrease uniformly from one region of the wafer to the adjoining regions. In general its value was found to lie within the 10^{-2} to 10^{-3} Ω-cm^2 range, but the variation within a wafer itself was sometimes greater than an order of magnitude.

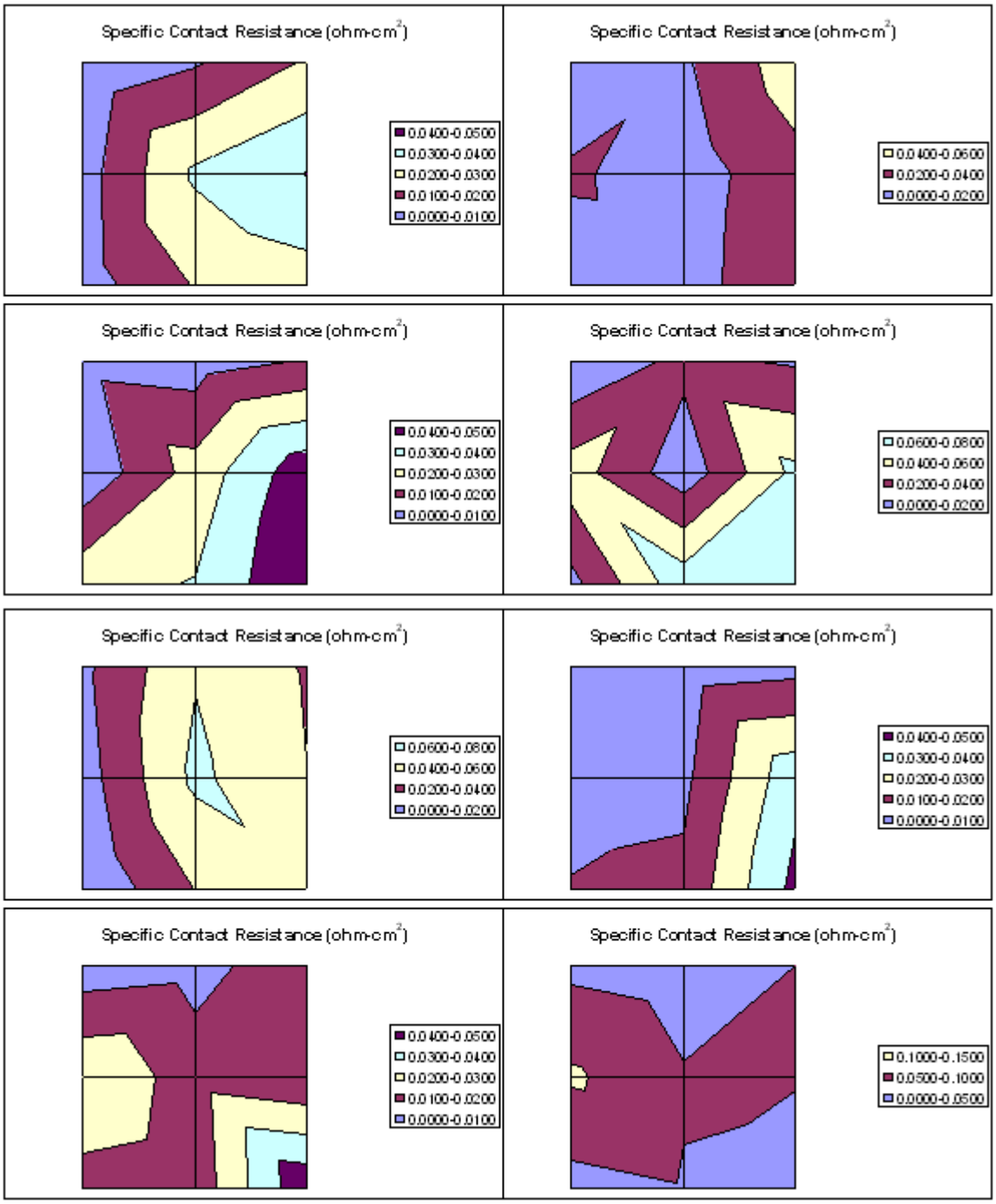


Figure 28: Spatial variation of specific contact resistance for 8 wafers.

The variation in the specific contact resistance could be due to several factors, including:

- The grain orientation of the multi-Si wafers,
- Variation in sheet resistance of the underlying emitter,

- Deviation in the firing profile of the furnace and its corresponding impact on the extent of the reaction at the Ag/Si interface, and
- Variation in the Ag paste itself.

In general, if a single crystalline substrate with a uniform sheet resistance is used and the firing profile is held uniform across the width of the wafer, the specific contact resistance across the wafer is expected to be uniform. More variation in the sheet resistance of the emitter than expected was detected for most of the test wafers during the course of the measurements. Thus, a second approach was sought to determine the magnitude of the specific contact resistance using a metallization pattern which more closely conformed to the grid metallization pattern used on today's cells.

The new pattern can be used to extract sheet resistance and specific contact resistance as well as to extract line resistance. The experiment was designed with the following groups:

1. Controls: multicrystalline wafers with a doped emitter with and without silicon nitride AR layer. These will be used to measure sheet resistance via a 4-point probe.
2. Screen pattern: standard cell process with and without silicon nitride AR layer. The specific contact resistance values will be extracted from those measurements.
3. Line pattern: standard cell process with and without silicon nitride AR layer used to provide line resistance measurements.

Group 1 Results. Five sister wafers were collected from the cell production line at BP Solar Frederick before the silicon nitride deposition. Wafer maps show that for each wafer the sheet resistance values actually vary over the area of the wafer. This variation was from 35-45Ω/□ for one wafer though in other wafers the variation was within a smaller range. On the whole, the average sheet resistance values were limited to 39-41Ω/□ but they do not reflect the spread in the data per wafer.

Similarly, sheet resistance measurements were also performed on 5 sister wafers after deposition of silicon nitride from the cell production line in Frederick. It is assumed that during the actual measurements, the probes of the 4-point probe tester would penetrate the silicon nitride layer to enable the tester to measure the sheet resistance from the underlying silicon substrate. The sheet resistance values were found to vary from 37-45Ω/□ over each wafer. The average values varied from 40-43Ω/□.

In general it was observed that the emitter sheet resistance values determined by the 4-point probe tester were higher than those measured using the contact pattern by approximately 5-70Ω/□. This higher sheet resistance measured could be due to poor electrical contact with the probe. However, the spread in the emitter sheet resistance values captured by the 4-point probe tester for wafers with or without a Si_3N_4 layer were consistent with the spread in the respective values from Group 3 wafers patterned using the special screen. Thus, even though the absolute values of the sheet resistance were not consistent, their relative variation was.

It was also observed for Group 1 wafers, that the sheet resistance values were higher for wafers with a silicon nitride layer than those without by 1-2Ω/□. This observation from Group 1 wafers was contradictory to the observation from those in Group 3 where the sheet resistance values were lower for wafers with a silicon nitride layer than those without by 2-5Ω/□. The silicon nitride layer likely has a positive charge so it induces a negative charge at the silicon nitride/multicrystalline Si interface and therefore aiding in lowering sheet resistance. If that is

indeed true, then our assumption that the probes of the 4-point probe tester are in good contact with the Si is not valid.

Group 2 Results: Figures 29 and 30 show the specific contact resistance maps from wafers with silicon nitride and without, respectively.

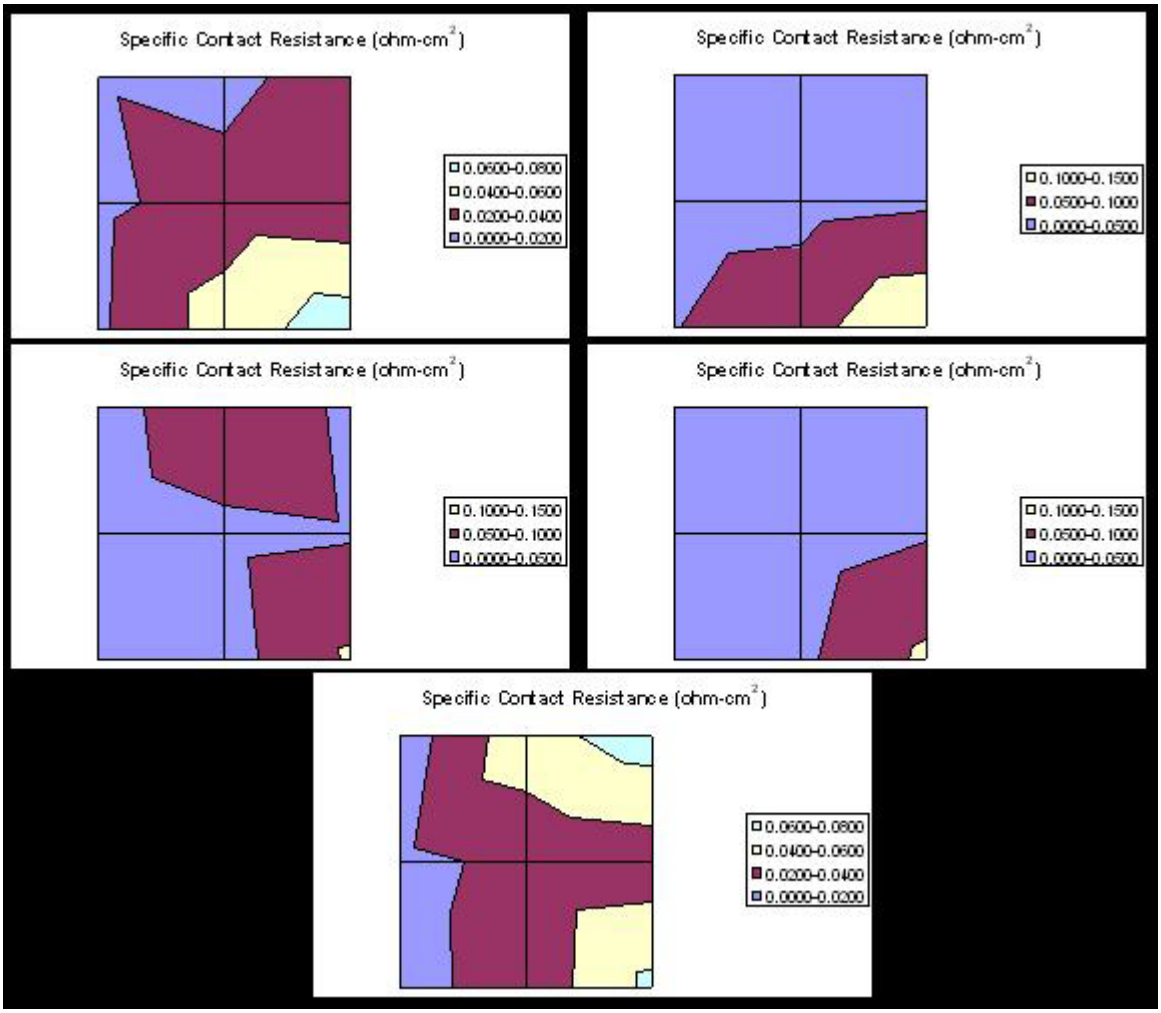


Figure 29: Specific contact resistance maps for wafers with silicon nitride.

The values of the specific contact resistance varied from values in the lower $10^{-3}\Omega$-cm^2 range to values in the upper 10^{-1} Ω-cm^2 range within the same wafer for those with the silicon nitride AR layer. For the wafers with no silicon nitride AR layer, the specific contact resistance values did not exceed 1.5 x $10^{-2}\Omega$-cm^2 for any wafer and varied from the lower 10^{-3} Ω-cm^2 range to the lower 10^{-2} Ω-cm^2 range. This implies that the nitride layer increases the specific contact resistance of the screen-printed metallization with respect to the underlying emitter by over an order of magnitude.

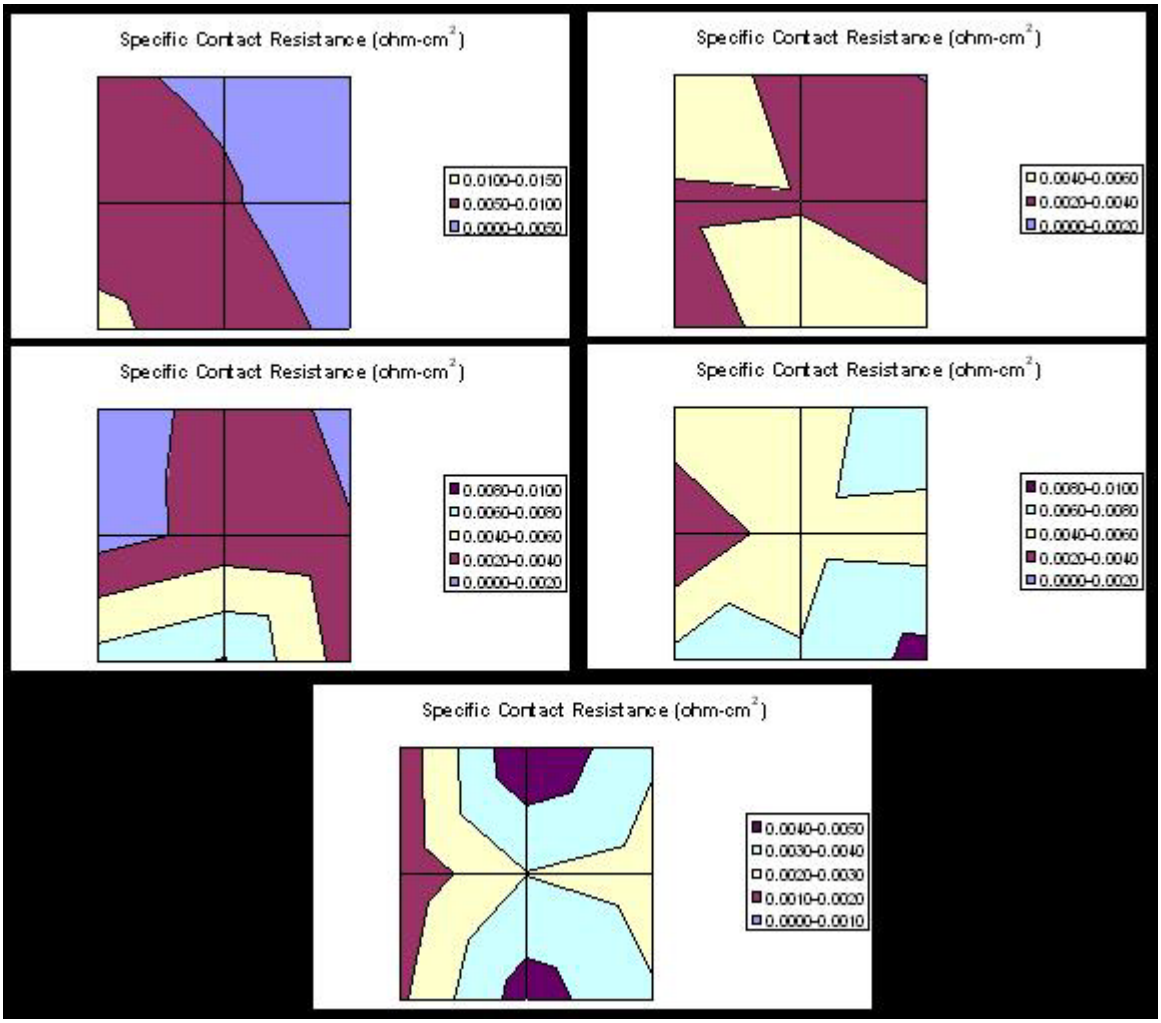


Figure 30: Specific contact resistance maps for wafers without silicon nitride.

The sheet resistance maps of wafers with silicon nitride and without are shown in Figures 31 and 32, respectively.

Like the trend shown by the specific contact resistance, the distribution of sheet resistance values seems to be lower by 2-5 Ω/□ for the wafers with the silicon nitride AR layer when compared to those without. This may be explained by the presence of a thin negative charge at the silicon nitride/Si interface.

Both specific contact resistance and sheet resistance values show a distribution across the wafer both with and without a silicon nitride layer. The specific contact resistance values for wafers with a silicon nitride layer were found to be higher than those without, in the same group, by an order of magnitude. Likewise, the sheet resistance values of the wafers with a silicon nitride layer were found to be 2-5Ω/□ lower than those in the same group without silicon nitride.

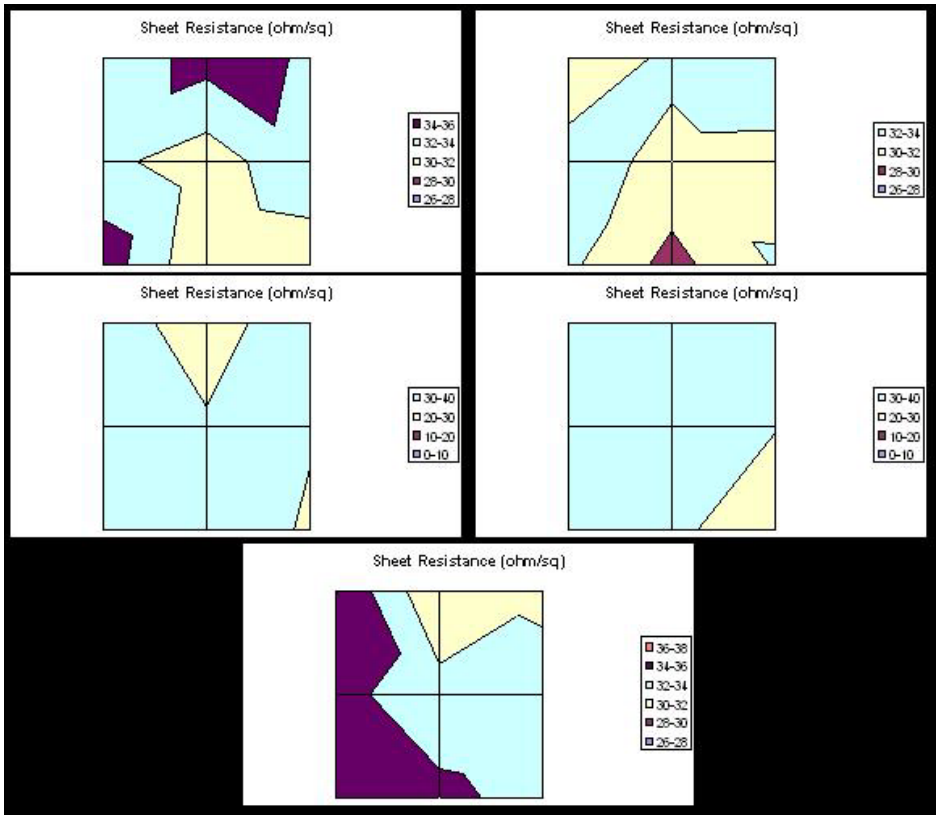


Figure 31: Sheet resistance maps for wafers with silicon nitride.

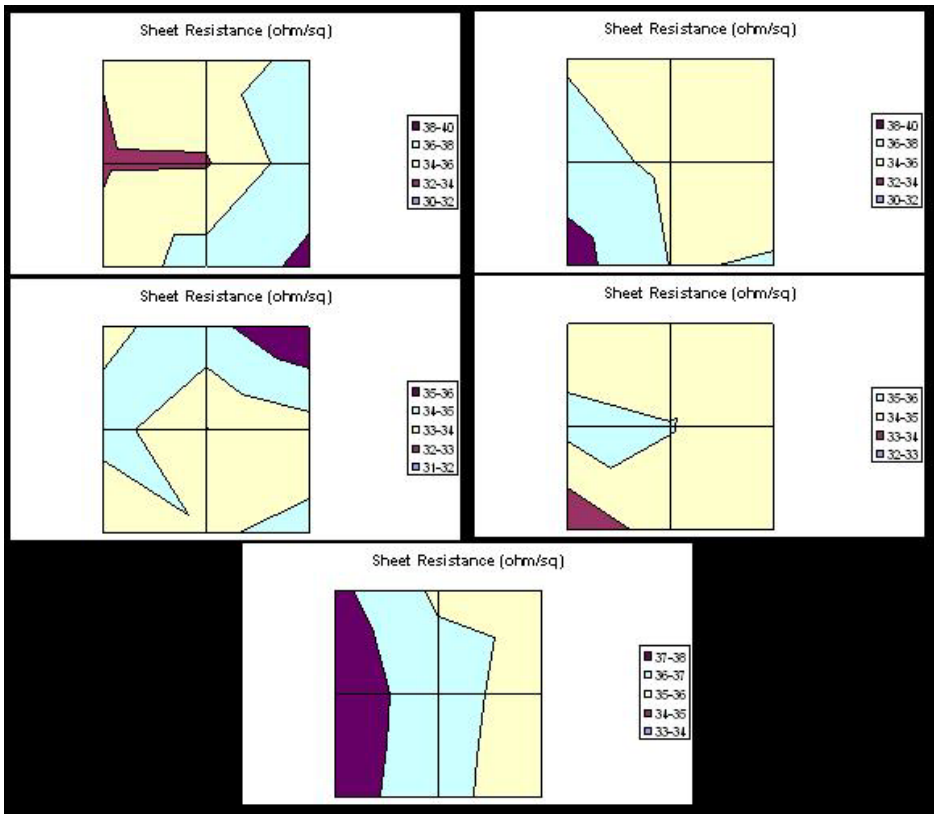


Figure 32: Sheet resistance maps for wafers without silicon nitride.

Group 3 Results. The 4-point probe measurements were performed in order to determine the emitter sheet resistance and specific contact resistance at the paste metallization/silicon interface after firing. The line resistance as a function of the line width and the bulk resistivity of the paste metallization were also determined. Table 8 shows the emitter sheet resistance and the line resistance values for various line-widths and the average resistivity of the Ag paste after firing.

Table 8: Sheet resistance of phosphorus-doped emitter, line resistance for various line-widths and average resistivity of silver paste after firing

Wafer ID	Emitter sheet resistance (Ω/□)	Metallization line resistance for various line-widths (Ω/mm)				Avg. resistivity of metallization (Ωmm)
		0.127 mm	0.101 mm	0.088 mm	0.076 mm	
1	42.95	1.09E-02	1.29E-02	1.62E-02	2.44E-02	2.60E-04
2	43.73	1.09E-02	1.29E-02	1.59E-02	1.89E-02	2.50E-04
3	42.86	1.10E-02	1.28E-02	1.54E-02	1.81E-02	2.69E-04

The sheet resistance for the 3 wafers was found to be 43.18 (+/-0.48) Ω/□. This value is comparable with the sheet resistance measured using a 4-point probe tester for Group 1 wafers. The average bulk resistivity of the Ag paste metallization after firing was 2.60 x 10^{-4} Ω-mm.

The absolute values of resistance measured across a gap-spacing are believed to be measured lower than they actually are. We believe that the apparent lower value of the measured resistances across the gap-spacing is due to leakage current through the silicon nitride layer or the induced inversion layer.

The line resistance measured across four times the line length for any particular line-width was only about half of the total determined from measuring each of the lines individually. In the ideal case, the line resistance should have scaled linearly with the length of the line for any line-width. It is believed that for line resistance measurements where the measurement pads were located in close proximity and the length of the line between them was very long, the current flow via the Ag/Si contact and that along the sheet charge on the silicon might be of the same order of magnitude.

3.3.4 Iso-Chemical Texturing (ICT)

Texture etching is an important process step especially for ultra-thin cells as it can increase light trapping and increase the path length of absorbed light. Multicrystalline silicon offers fewer choices than mono-crystalline silicon as the caustic etches used to texture mono do not work well with the randomly oriented grains in multi. It has been reported in the literature that iso-chemical texturing can be utilized to texture etch multicrystalline silicon.[7] ICT has an additional advantage in that it removes less material from the wafer thereby saving additional Si.

BP Solar purchased an in-line ICT etch station and began experimenting with the process. Initial reflectance measurements of the ICT wafers with a SiN coating indicate that there is a fairly wide process window for achieving good reflectance reduction. Figure 33 shows the comparison between a standard alkaline etched multicrystalline wafer and an acidic ICT textured multicrystalline wafer processed in the new etch station. Reflectance is greatly reduced for the

ICT material while the crystal pattern is nearly eliminated producing a relatively homogeneous surface.

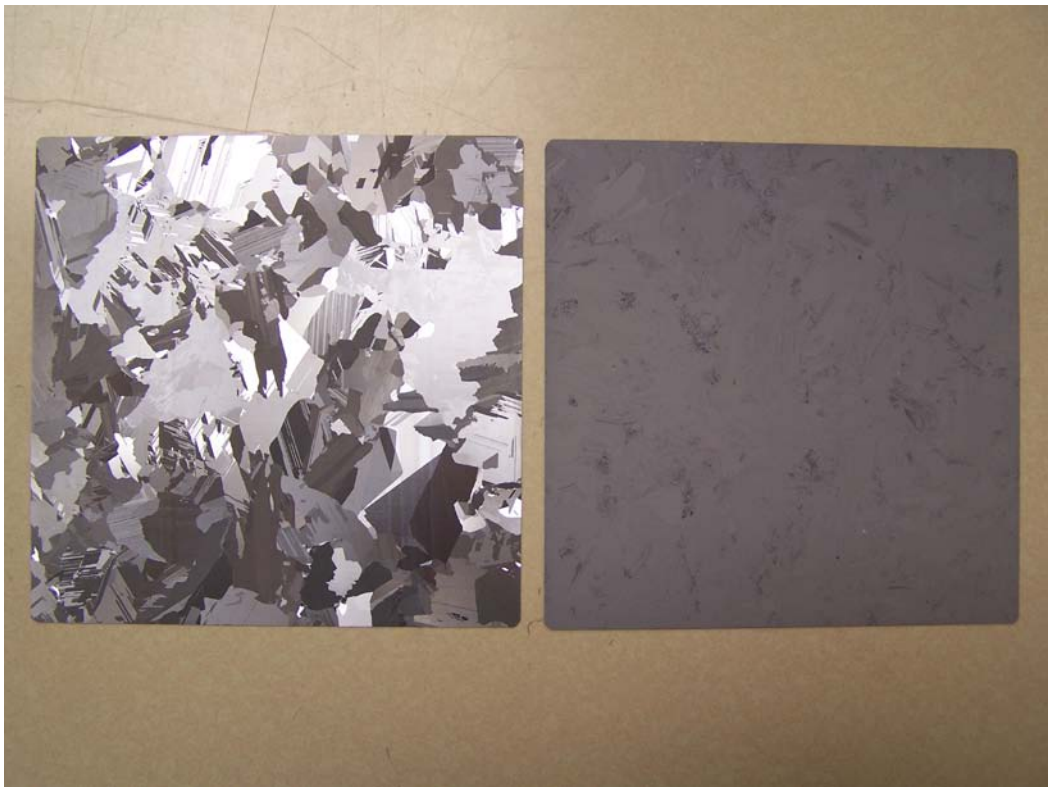


Figure 33: Alkaline versus ICT textured multicrystalline Si wafers

An experiment was performed to compare the performance of ICT etched surfaces versus standard alkaline surfaces using a baseline version of BP Solar's screen print process. Figure 34 shows the reflectance of four samples, two with ICT and two with alkaline etched surfaces. Each had one with a standard thickness SiN AR layer and one with a thicker layer. The ICT samples clearly have less reflectance than the corresponding alkaline samples. There does not appear to be any advantage to using a thicker SiN AR layer although several commercial products are available with thicker AR layers on their ICT etched cells.

The electrical performances of the cells from this trial are presented in Table 9. The ICT materials resulted in a 2.5 to 3% improvement in the average short circuit current values as measured. This gain is offset slightly by lower Voc and fill factor, driven by a reduction in the diode quality of the ICT-etched material. Overall, there was a 1.5% gain in output power.

A pilot trial of 1200 wafers was performed in order to evaluate the large-scale capability of the in-line etch station. Acceptable yields were obtained. Cell measurements in air showed an improvement in current for ICT of about 1.7%. Again, this was offset by a slight drop in voltage and fill factor. Both losses seem to be driven primarily by slightly poorer emitter characteristics, at least partially explained by the higher emitter surface area. As a result, only a 0.3% efficiency gain was realized.

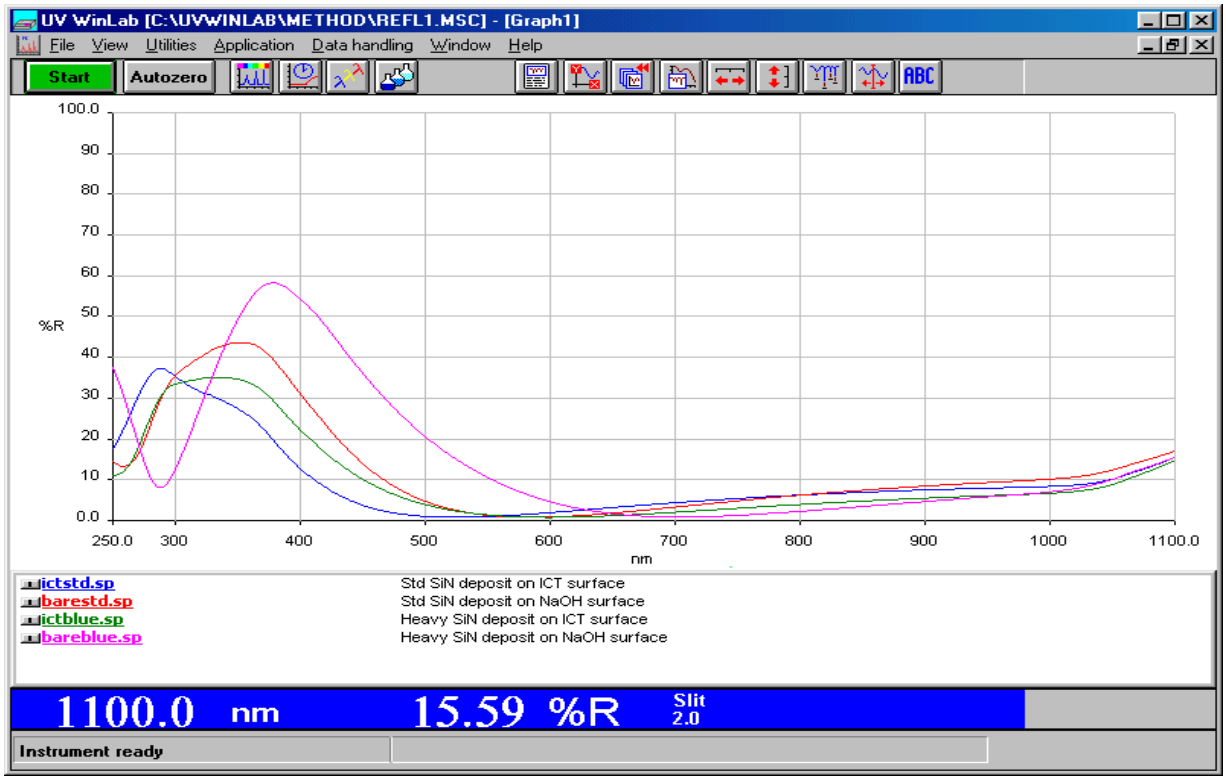


Figure 34: Reflectance of ICT and alkaline etched Multicrystalline Si Surfaces

Table 9: Electrical Performance of cells with ICT etch versus cells with alkaline etch

Surface Texture	Efficiency (%)	Isc (Amp)	Voc (mV)	FF (%)
Alkaline	14.71	5.007	603.0	76.0
ICT	14.93	5.163	598.2	75.4
Difference (%)	1.5	3.1	-0.8	-0.8

The in-line unit was then put through a rigorous processing trial which tested both its capabilities and our ability to maintain a constant etch depth over the course of the trial. Six (6) sets of experimental wafers were run through the machine. These included wafers of various starting material (multi and mono) and thicknesses (225µm, 180µm, 175µm, and 155µm). Some of the material was from different vendors, thus there was potential for varying degrees of starting surface damage. It was determined that differences were generally minor—only one group fell out of spec range resulting in a slightly deeper texture.

The process required a great deal of make-up dosing to maintain a fairly constant etch rate. Several instances of very high breakage occurred which was eventually traced to equipment misalignment. This was remedied and a 99-100% yield rate was achieved on wafers as thin as 175µm. Minor design changes will need to be made to handle wafers thinner than this.

ICT performance on multicrystalline silicon was then evaluated on the module level. Split lot trials were conducted to compare ICT with alkaline etch. Each module had 72 - 125 mm by 125 mm cells. Table 10 shows the electrical results.

Table 10: Comparison of module performance using cells with ICT or alkaline etch

Sample	Voc (V)	Isc (A)	Pmax (W)	FF (%)
Alkaline 1	43.54	5.253	165.83	72.5
Alkaline 2	43.44	5.222	164.46	72.5
Alkaline Average	43.49	5.237	165.15	72.5
ICT 5	43.62	5.282	167.76	72.8
ICT6	43.86	5.379	167.94	71.2
ICT Average	43.74	5.330	167.85	72.0
Difference	0.57%	1.78%	1.63%	-0.69%

ICT resulted in a 1.63% increase in output power driven by increases in short circuit current and open circuit voltage. Fill factor continues to be lower for ICT.

As part of this experiment modules were also fabricated using a lighter diffusion on both alkaline and ICT etched wafers. The alkaline control modules were lower in power than the standard diffusion. For ICT the lighter diffusion resulted in modules with virtually identical performance as the standard diffusion.

Another large pilot trial was run to evaluate ICT vs. alkaline etch in terms of electrical performance of cells and modules. A total of 2,000 wafers (200µm thick) were included in the trial, split into two groups; 1,000 ICT and 1,000 alkaline. Of interest was the mechanical yield of the ICT wafers versus the planar surface as there had been some concern that the texturing might cause them to be more fragile. Several equipment malfunctions made the mechanical yield comparison somewhat complicated, however, for those process steps where there were no issues encountered, the yields were quite comparable. There was a significant gain in short circuit current at the cell level for the ICT group. Again, this was offset by a loss in Voc and fill factor. An overall efficiency gain of 2.3% was realized at the cell level as shown Table 11.

Table 11: Cell electrical results for ICT Pilot Trial

Process	# of Cells	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Control	903	15.27	5.056	607.2	77.1
ICT	876	15.62	5.232	605.6	76.4
Difference		+2.3%	+3.5%	-0.3%	-0.9%

Unfortunately this level of efficiency improvement did not transfer to the modules. When measured on the xenon flash tester the modules with ICT cells had 1.68% higher short circuit current, but this was negated by lower fill factor and open circuit voltage resulting in negligible power gain. However, when these same modules were measured outdoors the ICT modules had an average of 2.9% higher short circuit current, and 1.15% higher output power and efficiency. The unanswered question is whether this increase in module efficiency is sufficient to justify the use of ICT.

3.4 Task 4: Module Development

This task was expected to result in the development of a PV module that is rated and qualified for operation at 1500 volts and would carry a 30-year warranty.

3.4.1 Molded Frame

In order to greatly reduce ground fault failures, especially in large-scale systems where significant quantities of ground connections and high voltages are present, a molded plastic frame was designed. This would electrically isolate each module, therefore eliminating module-to-module grounding. It also allows greater design creativity (irregular shapes, textures, mounting inserts, frame incorporated wiring). The increased potential for a variety of design options led to discussions to identify the most versatile design in order to incorporate the largest number of applications. Ten (10) prototype modules and the accompanying brackets were fabricated and installed on test roofs in order to validate form, fit and function and to serve as effective show pieces demonstrating the advantages of using a molded frame.

The interconnection features built into these prototype modules created a very straightforward and quick installation procedure. The specific design fits in applications where concrete roof tiles and asphalt shingles are used and were produced in both blue and black color versions. It also attaches into the existing fasteners of the concrete tiles which provides an attractive option for both new and retrofit applications. The versatility of color and shape accommodate a broader range of customer requirements and geographic applications. Figure 35 shows one such installation. We are currently in the process of identifying the best design(s) to pursue based on market potential and customer need.

Figure 35: Prototype Plastic Frame Module Installed on Concrete Tile Roof

3.4.2 AR-Coated Glass

BP Solar uses AR-coated glass on some select products. This glass is produced by an overseas supplier and quantities are limited. Therefore, efforts to assist AFG in the development of AR-coated glass in their Kingsport, TN factory were undertaken. An initial set of samples resulted in a 1.8% improvement in module short circuit current versus the 2.4% gain we see with the current commercial AR glass. AFG worked to improve uniformity of their coating process in order to match the2.4% gain. Forty samples of the improved glass from AFG were received and tested. Modules were subjected to BP Solar's internal qualification test sequence[8], which is a more severe version of IEC 61215, "Crystalline Silicon Photovoltaic Modules - Design Qualification and Type Approval." The modules with AR coated glass passed all of these with minimal power loss. Another sample module made with AR coated glass was subjected to the salt spray test for PV modules (IEC 61701). The module successfully passed this test with minimal power loss and minor cosmetic changes.

A pilot run was performed using 240 pieces of the AFG AR glass using the commercial AR glass from Europe as a control. The results for peak power are shown in Table 12 while the results for short circuit current are shown in Table 13.

Table 12: Pmp for AFG AR-Coated Glass vs. AR Control

Pmp comparison			
ARC Glass Supplier	AR Control	AFG	Delta
Average	170.4	170.5	0.07%
Std Dev	0.9	1.0	6.2%
Max	172.7	173.3	0.3%
Min	167.6	167.5	-0.1%

Table 13: Isc for AFG AR-Coated Glass vs. AR Control

Isc comparison			
ARC Glass Supplier	AR Control	AFG	Delta
Average	5.135	5.133	-0.04%
Std Dev	0.023	0.026	11.7%
Max	5.189	5.197	0.2%
Min	5.090	5.073	-0.3%

In general, the AFG glass matched the performance of the commercial AR glass from Europe . All of the production at the Frederick facility has now been switched to the AR glass from AFG.

3.4.3 Smaller Cell Module

One of the module designs evaluated in this program used smaller cells in an effort to improve performance and yield. The first samples were built using 142 half cells on the same glass as our standard 72 cell module made with 125 mm by 125 mm cells. The two modules (72 and 142 cell)

were then carefully measured at different irradiances using a variety of mesh filters. The results are shown in Figures 36, 37 and 38.

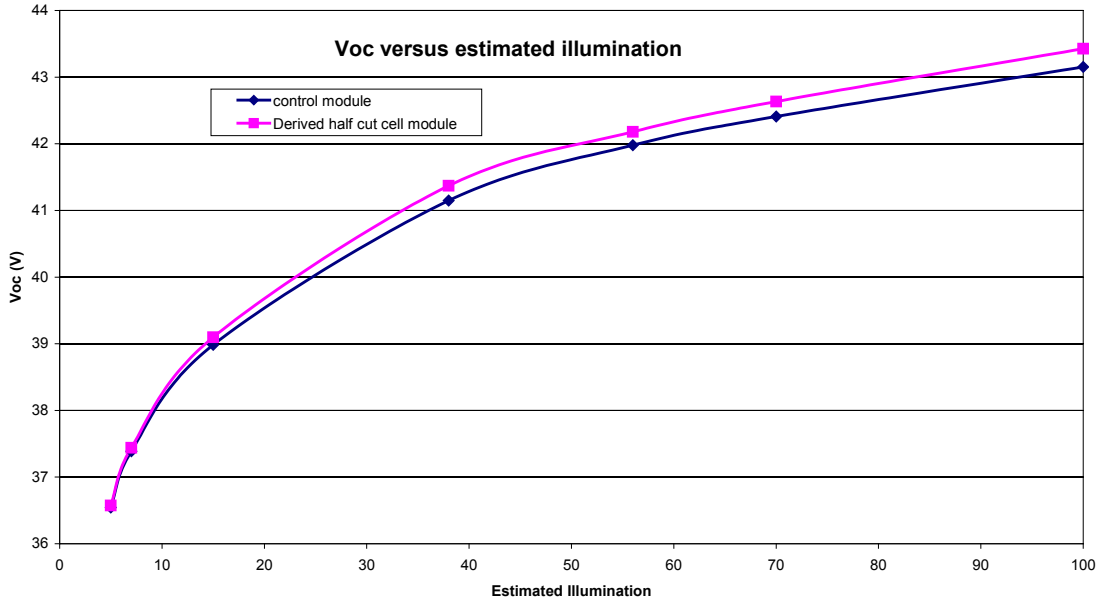


Figure 36: Voc vs Irradiance for modules with full size and ½ size cells. Voc for module with ½ size cells is divided by 2.

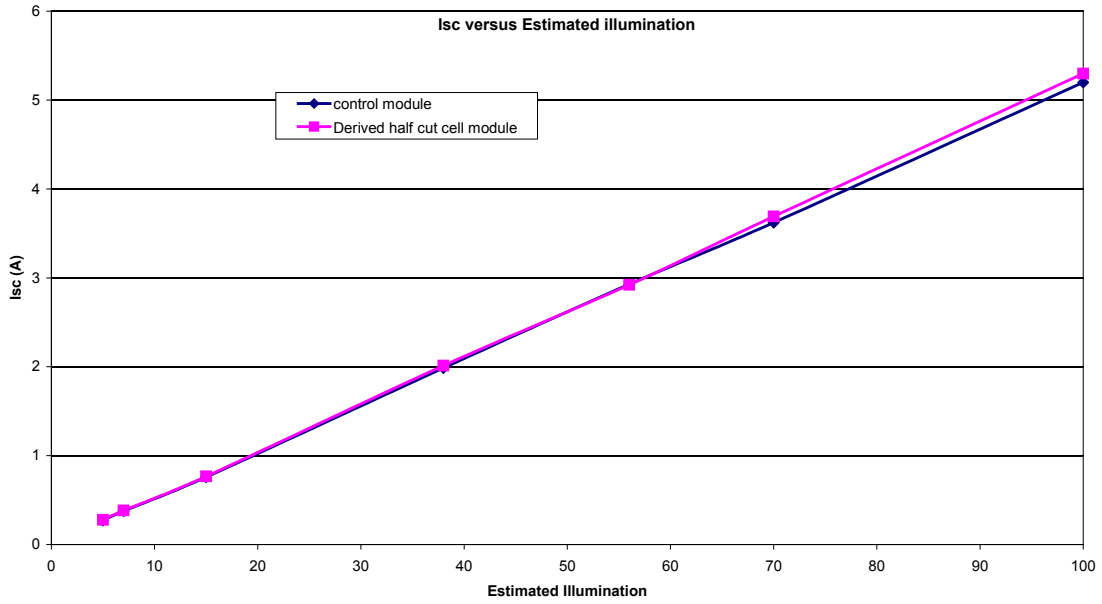


Figure 37: Isc vs Irradiance for modules with full size and ½ size cells. Isc for module with ½ cells is multiplied by 2

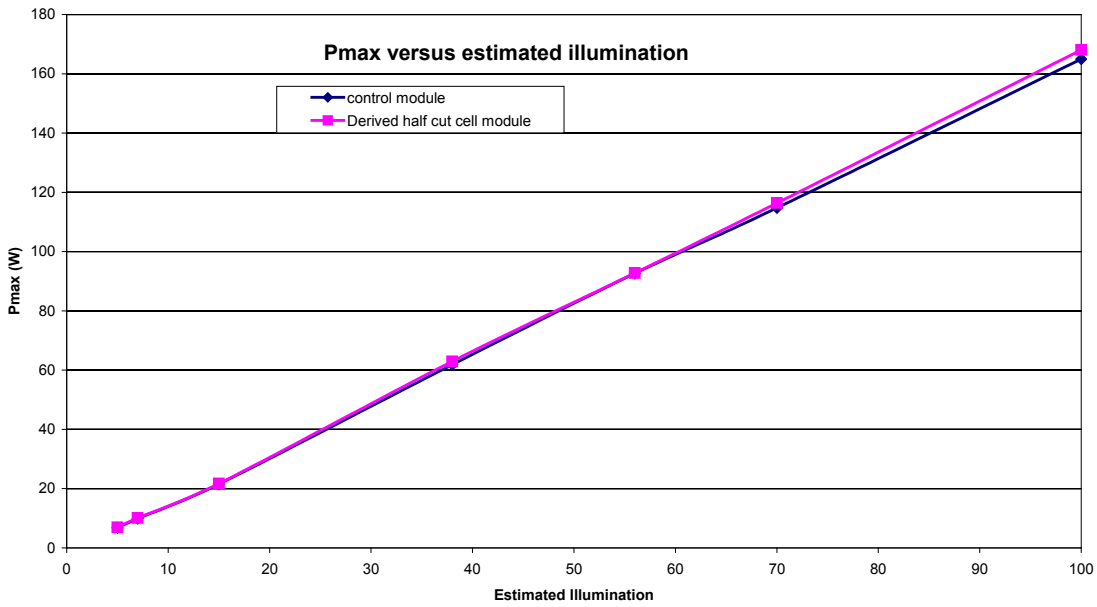


Figure 38: Pmax vs Irradiance for modules with full size and ½ size cells

As expected, the smaller cells yielded higher power (~ 3 watts or 2%) at 1 sun since full-size cell modules are fill factor limited at 1 sun due to series resistance. This effect should be much larger for larger cells. So the next step is to do the same experiment with modules made from 60 standard size 156 mm by 156 mm cells or from 120 half cells each 78 mm by 156 mm.

3.4.4 Fault Tolerant Design

Fault-tolerant circuit design involves using various redundant features in the circuit in order to control the effect of partial failure on overall module yield and array power degradation. Generally this can be controlled by dividing the modules into a number of parallel branch circuits which can also improve module losses due to broken cells and other circuit failures. With multiple cell interconnects, series/paralleling and bypass diodes, it is possible to achieve high levels of reliability. However, we still find that individual modules fail and must be replaced before the system can be returned to its full capacity.

A preliminary review of existing literature on fault-tolerant designs in PV and other industries such as aerospace, shipbuilding and electronic control systems was completed. The most common principle identified is the design of parallel circuit connections to maintain system functionality in the event of a single component failure. There is continuing detailed work by others on how different array designs can improve long-term reliability.

We chose to focus on ways to design fault-tolerance into the module. After discussing the most common failure modes we see, it was decided to focus on the following:

- Broken cells: which will get worse as cells get thinner,
- Interconnect cracking/breaking: which gets worse for larger cells
- Solder bond failures.

It is worth noting that the present design with 2 buss bars and 2 interconnects per cell already has a significant amount of fault tolerance built in. However, it could be improved.

One way to improve the redundancy would be to use mesh interconnects with rather than ribbons. Small samples with mesh interconnects incorporating many (>50) small solder joints to the front grid lines were made. While we were able to do this by hand in the lab, it became clear that it would be very difficult to control the alignment of the mesh to the cell pattern in a production line environment.

The pattern could be made small and dense enough so that the mesh would make contact in almost any location, but this would require an undesirably large amount of the cell to be covered with grid lines. Therefore the use of a conductive coating on the front of the cell seems like a much more promising idea.

Long-term thermal cycle testing of Cu-Al-Cu ribbon versus standard copper ribbon was done in order to determine whether softer ribbon actually improves the lifetime. Our standard in-house test extends the IEC 61215 test from 200 to 500 thermal cycles (-40 C to + 85 C), with current flowing through the cells during the warm part of the cycle. Each module was cycled for 1500 cycles with current flow. The soft ribbon modules lost less than 4% of initial power after 1500 cycles. However, the standard ribbon did even better with neither of the test modules losing more than 1.5% in 1500 cycles. So it is unlikely that a change in ribbon will make a significant improvement in the reliability.

The other area of concern was cracked cells. In the next section we will describe a new tool for evaluation cell breakage within a module. This work indicates that there are probably a lot more broken cells in the fielded modules than we previously suspected. However, we have observed modules with large numbers of broken cells that have very little power loss.

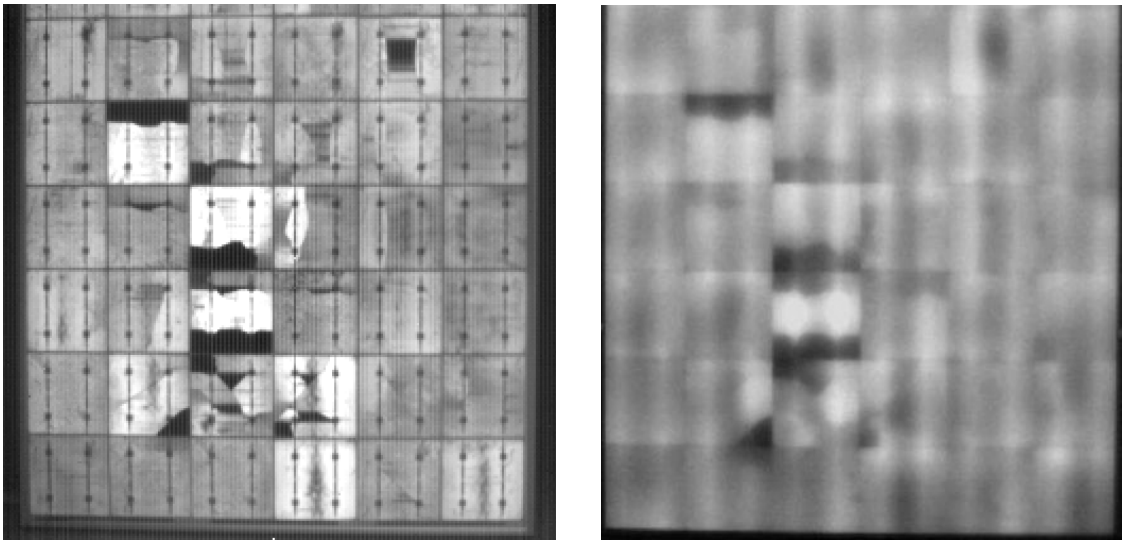
Our conclusions from this work are:

- Today's interconnects can be extremely reliable when designed and processed correctly.
- While we do see broken cells in modules they often have little impact on power output
- The use of redundant tabs soldered across the tops and bottoms of the cells provides a good degree of protection against faults.
- The most likely failure points are those without redundancy like the connection of the output wire or attachment of the cell strings to the bus bars and/or diode boards – which have historically been done manually.

3.4.5 Electroluminescence as a Technique to Inspect Encapsulated Cells

Electroluminescence has been investigated as a method to inspect cells in a module. The technique has advantages over the more traditional IR techniques as it produces images with much higher resolution. The method utilizes the same forward bias condition used in standard IR imaging but lower current densities are used reducing the need for large power supplies.

The main difference between the two is the wavelength of the light used. Electroluminescence uses much shorter wavelengths than heat-based IR (>7500mm). The images in Figure 39 show the same damaged module viewed with the electroluminescence phenomenon versus standard heat IR imaging. This method shows considerable potential for use in failure analysis at the module level.



Electroluminescence Long Wavelength IR

Figure 39: Damaged Module Viewed with Electroluminescence vs. Long Wavelength IR

A set of screening experiments were performed to look at modules made with different cells (multi, mono, Mono^2) as well as with different thickness wafers. Modules as made, after 1000 mechanical load cycles, after 50 thermal cycles and after 10 humidity freeze cycles were tested. Photos of a module with 200µm mono cells are shown in Figure 40.

While this module shows significant cell breakage after mechanical load and again after thermal cycling, it only suffered a 2.4% loss. After the subsequent 10 humidity freeze cycles the module was only down 0.5% from the initial reading. Thus it easily passed the dynamic mechanical load, 50 TC, 10 HF leg of the test with many broken cells. Some preliminary conclusions we have drawn from the initial use of the camera are:

- Many of the micro-cracks originate from the solder bond locations (especially for mono)
- Mono-crystalline Si cells suffer more cracking than multicrystalline Si cells
- There was not a significant difference in terms of degree of cell breakage in the module between those made with 200µm thick cells and those made with 240µm thick cells.
- With the present design there can be a large number of cracked cells without serious power loss
- Cracked cells tend to occur in the center of the module rather than at the edges indicating that it is the deflection of the glass that causes the micro-cracks to grow.

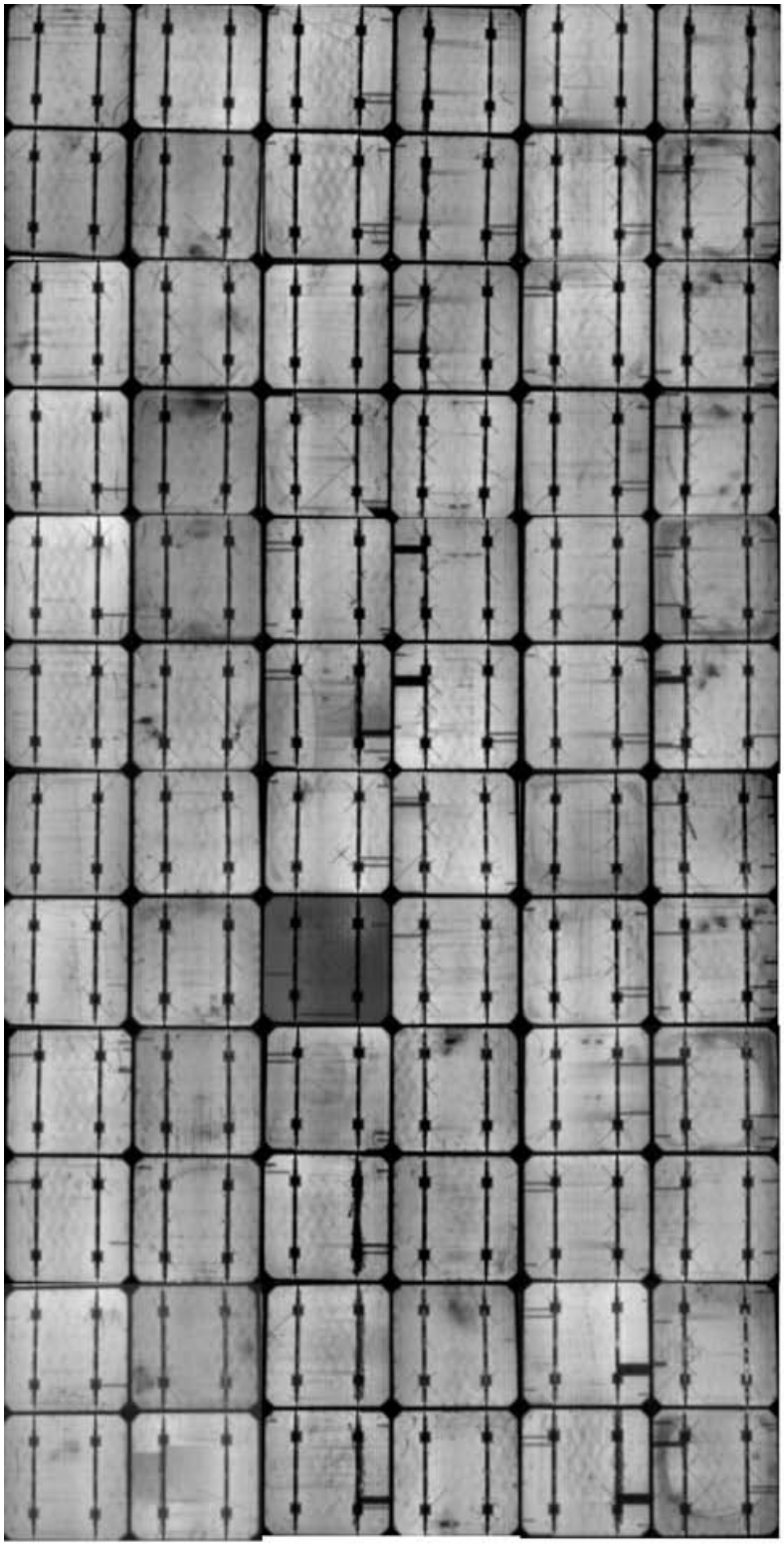


Figure 40a: Module made with 200 μm mono cells
Initial – Immediately after manufacture

Figure 40b: Module made with 200 μm mono cells
After 1000 Mechanical Cycles – 1.4% power loss

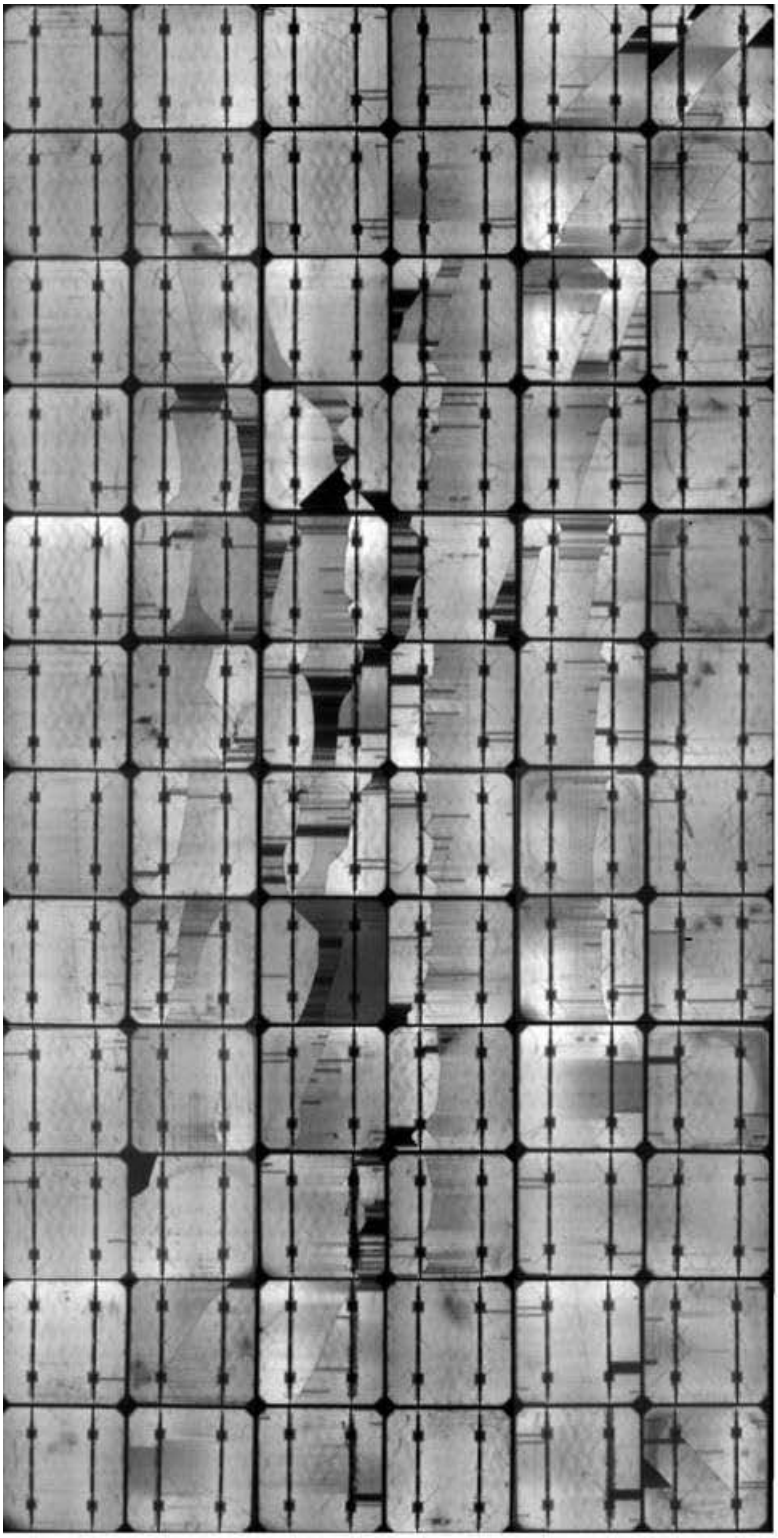


Figure 40c: Module made with 200 μm mono cells
After 1000 Mechanical Cycles and 50 thermal cycles – 2.4% power loss

3.5 Task 5: High-Voltage Systems Integration

The objective of this task was to evaluate the dangers associated with operating modules at high voltage (defined for this effort as greater than 1000 volts). Part of this evaluation was to include a study of the potential hazards of operating at high voltage. This is presented in Section 3.5.2. The second part of this evaluation was to build a high voltage test bed in order to test modules at high voltage for an extended period of time. The set up and initial results of this are presented in Section 3.5.1. The operation of this test bed is being continued under BP Solar's SAI TPP program.

3.5.1 Florida Solar Energy Center (FSEC) Subcontract for a High-Voltage Test Bed

FSEC completed a study of the requirements and a design was completed. A rack of aluminum L channels was constructed at an appropriate south facing tilt for the installation of modules. Back supports for these racks were installed at appropriate distances to make the rack more robust. It is important to have the modules electrically floating due to very high biasing voltages. This was accomplished by mounting the modules on electrically insulated standoffs. All electrical circuits are mounted for safety. An air conditioned NEMA 4 enclosure was installed for housing the power supplies on a concrete base next to the platform. Copper rods were buried 16 feet deep in the ground at all corners of the platform to provide grounding for the structure and electrical circuits. An extra set of copper rods were used to provide grounding to the concrete bases.

Initially five BP Solar multicrystalline Si modules were installed. One is at ground potential. Two are biased at +600V while two more are biased at -600V. Two digital high voltage power supplies and two resistor circuits were used for positive and negative biasing of modules. These power supplies will be replaced by current-limited power supplies after the initial testing of circuits and the data acquisition system. The structure with modules is shown in Figure 41 and 42.

Figure 41: High Voltage Test Bed at FSEC

Figure 42: High Voltage Test Bed – Modules Mounted with Insulated Stand-offs

The first test utilizing the high-voltage test bed was a study of the effect that relative humidity has on leakage current in high voltage biased BP Solar multicrystalline Si PV modules. A study of leakage currents in PV modules has been shown to be effective in early detection of design, material and process flaws in PV modules. Corrosion has been found to occur in some a-Si:H PV modules during accelerated testing under damp-heat with high voltage bias conditions[7]. The objective of this study was to understand the correlation, if any, between the leakage current and mobile corrosive impurities.

Data for leakage current, solar irradiance, relative humidity, wind speed, ambient pressure reference temperature and back-of-module temperature are measured once every 15 seconds and are averaged over 15-minute intervals. Only the averages are stored. The variation of leakage currents, LC1 and LC2 for the negatively biased modules and LC3 and LC4 for the positively biased modules, the irradiance and relative humidity with time for two days are provided in Figure 43a and 43b. For both days the leakage current for one of the negatively biased modules has shown out of range values (>15,000nA) for a short period. Therefore, the range for the data logger will be increased.

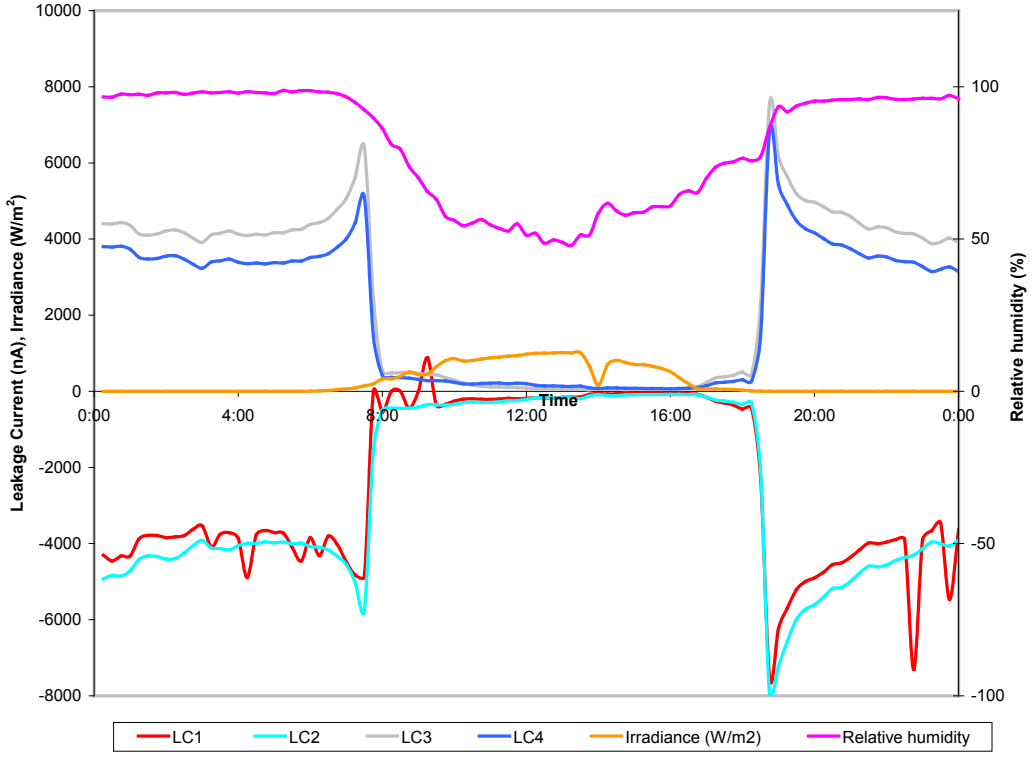


Figure 43a: Variation of Leakage Current, RH and Solar Irradiance with Time on 8/25

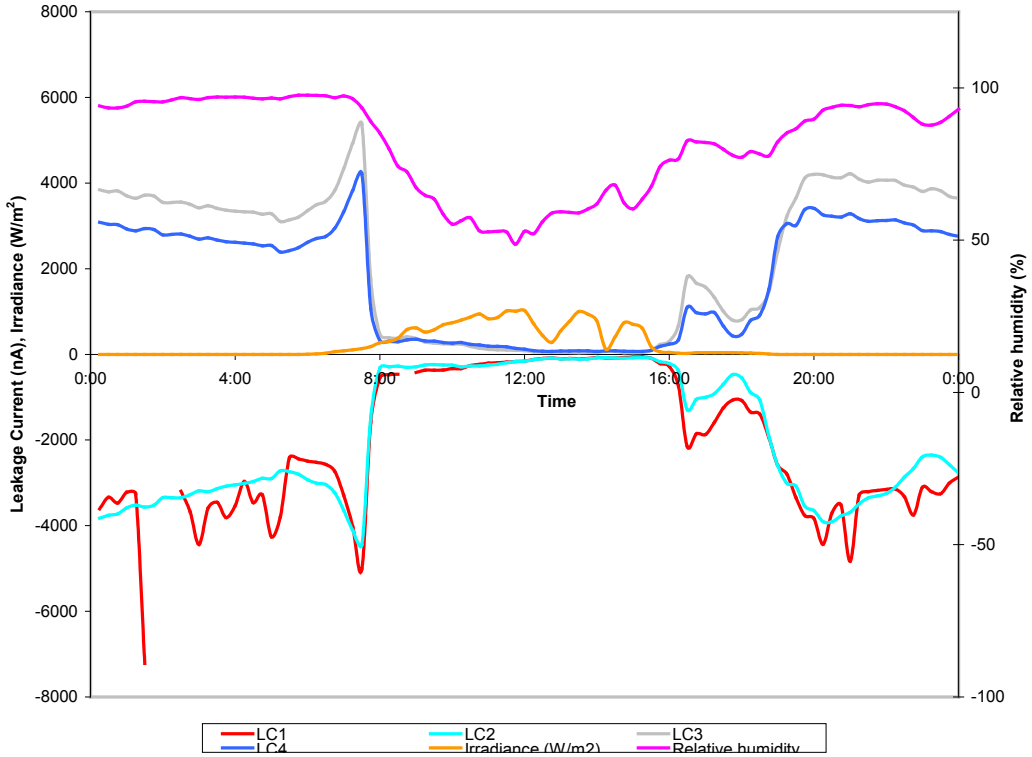


Figure 43b: Variation of Leakage Current, RH and Solar Irradiance with Time on 8/26

It can be seen that the leakage currents of high voltage biased BP Solar multicrystalline Si modules follow the expected trend—the leakage currents increase with increasing relative humidity and vice versa.

In the next phase a second fence (a fence within a fence) will be constructed around the high voltage platform to prohibit entry of unauthorized personnel. Micro-switches will be installed on fence doors such that the main power to the power supplies will be interrupted whenever the fence door is opened. As soon as the second fence is completed, the high voltage bias voltage values will be increased in steps to +1500 volts and -1500 volts.

3.5.2 Higher Operation Voltages and Module Performance

An assessment of high voltage PV systems was completed. This included an evaluation of the various standards and codes in terms of their requirements for or impacts on PV system voltage. Part of this effort was to identify tests that would be required in order to qualify components for use at specified voltages. Internal work focused on improving our understanding of the impact of higher operating voltages on module performance. The major issues under evaluation included:

- DC Arcing. Any open circuit in a high voltage circuit will lead to arcing if the open occurs while current is flowing.
- Ground Faults. With higher voltage, ground faults are likely to be more severe.
- Corrosion. High voltage can drive electro-corrosion of components that would otherwise be stable at low voltage.

A trial was run in order to determine how cable connections fail in real world situations. The trial was designed so that PV generated currents were applied to cable joints that were intentionally not soldered.

The electric supply was produced by series, connecting up to 11 modules with 72-cells each. The test sample was placed in series with these modules. There was no other resistive component in the circuit, thus the string was essentially short-circuited.

Various cable/junction box designs were placed in a series with the string and their mode of failure recorded by video and still pictures when a free cable was brought into contact with the internal terminal. In addition to the visual records, voltage and current measurements were made at the junction box itself.

In all cases, arcs were initiated at the free cable contact within the junction box. These arcs occurred not just in BP Solar designs, but also in third party junction boxes. The arc attained a high enough temperature to not only combust all plastic materials, even those with high combustion resistance – V rating, but additionally melt all metallic parts including copper components.

Arcing ceased once the air gap formed by combustion grew to a point where the arc plasma could not be sustained.

An investigation of potential solutions to this problem was performed. A literature and patent search turned up a number of patents for devices that claim to be able to detect DC arcs and switch off the current in order to extinguish the arc. Future work on this effort has been transferred to the BP Solar SAI TPP.

Acknowledgements

BP Solar acknowledges the financial support of DOE/NREL for this work under the Photovoltaic Manufacturing Technology Program, Subcontract #ZAX-6-33628-11. We would also like to acknowledge the support and assistance of the NREL technical staff, particularly the Technical Contract Monitor, Richard Mitchell.

REFERENCES

[1] J. Wohlgemuth and M. Narayanan, "Large-Scale PV Module Manufacturing Using Ultra-thin Silicon Solar Cells " Final Subcontract Report for NREL Contract # ZDO-2-30628-03, June, 2006.

[2] John Wohlgemuth, Mohan Narayanan, Roger Clark, Tim Koval, Steve Roncin, Murray Bennett, Daniel Cunningham, Dinesh Amin, George Kelly, Nathan Stoddard and Joseph Creager "Polycrystalline Silicon Photovoltaic Manufacturing Technology Development and Commercialization", *Proceedings of the 4th World Conf on PV Energy Conversion,* May, 2006, Hawaii, p. 1099.

[3] Nathan Stoddard, Bei Wu, Ian Whitting, Magnus Wagener, Yongkook Park, George Rozgonyi and Roger Clark "Casting Single Crystal Silicon: Novel Defect Profiles from BP Solar's Mono^2 Wafers" **Solid State Phenomena Vols. 131-133** , 2008, p. 1.

[4] C.P. Khattak and F. Schmid "Directional Solidification of Crack Free Silicon Ingots by Heat Exchanger Method", *Proceedings of 13th PVSC*, 1978, p. 173.

[5] O. Schultz, S.W. Glunz, S. Riepe and G.P. Willeke: Prog. Photovolt: Res. Appl. Vol. 14 (2006), p. 711.

[6] H. Behnken, M. Apel, and D. Franke, "Simulation of mechanical stress during bending tests for crystalline wafers," *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion,* 2003, pp. 1308-1311.

[7] R. Einhaus, E. Vazsony, J. Nils and R. Mertens "Isotropic Texturing of Multicrystalline Silicon Wafers with Acidic Texturing Solutions" *Proceedings of 26th IEEE PVSC,* Sept. 1997, p. 167.

[8] John Wohlgemuth, Daniel Cunningham, Paul Monus, Jay Miller and Andy Nguyen "Long term Reliability of Photovoltaic Modules", *Proceedings of the 4th World Conf on PV Energy Conversion,* May, 2006, p. 2050.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Executive Services and Communications Directorate (0704-0188). Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.
PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE *(DD-MM-YYYY)*
5/25/2009

2. REPORT TYPE
Subcontractor Report

3. DATES COVERED *(From - To)*
1 April 2006-31 August 2007

4. TITLE AND SUBTITLE
Development of Large High-Voltage PV Modules with Improved Reliability and Lower Cost: Final Subcontract Report, 1 April 2006-31 August 2007

5a. CONTRACT NUMBER
DE-AC36-08-GO28308

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
J. Wohlgemuth

5d. PROJECT NUMBER
NREL/SR-520-43828

5e. TASK NUMBER
PVB75301

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
BP Solar International, Inc.
630 Solarex Court
Frederick, Maryland 21703

8. PERFORMING ORGANIZATION REPORT NUMBER
ZAX-6-33628-11

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-520-43828

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES
NREL Technical Monitor: R.L. Mitchell

14. ABSTRACT *(Maximum 200 Words)*
The overall objective of this program was to provide NREL with technical results that enhance its capability to improve PV manufacturing technology by developing a PV module with the following characteristics: intended primarily for the grid-connected market; qualified for use in systems with voltages up to 1500 volts; with a minimum standard testing conditions output power of 250 watts using large (at least 15.7 cm by 15.7 cm) ultra-thin cast multicrystalline silicon solar cells; and with at least a 16% conversion efficiency. This module must be capable of achieving a 30% reduction in overall manufacturing cost, will carry an extended warranty of at least 30 years, and will not contain any toxic or hazardous materials.

15. SUBJECT TERMS
PV; manufacturer; solar cells; modules; high voltage, reliability; low cost; thermal model; grid-connected market; crystalline silicon;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPHONE NUMBER (*Include area code*)
Unclassified	Unclassified	Unclassified	UL		

Standard Form 298 (Rev. 8/98)
Prescribed by ANSI Std. Z39.18

F1146-E(10/2008)