Crystal Silicon Heterojunction Solar Cells by Hot-Wire CVD

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CRYSTAL SILICON HETEROJUNCTION SOLAR CELLS BY HOT-WIRE CVD
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ABSTRACT
Hot-wire chemical vapor deposition (HWCVD) is a promising technique for fabricating Silicon heterojunction (SHJ) solar cells. In this paper we describe our efforts to increase the open circuit voltage ($V_{oc}$) while improving the efficiency of these devices. On p-type c-Si float-zone wafers, we used a double heterojunction structure with an amorphous n/i contact to the top surface and an i/p contact to the back surface to obtain an open circuit voltage ($V_{oc}$) of 679 mV in a 0.9 cm$^2$ cell with an independently confirmed efficiency of 19.1%. This is the best reported performance for a cell of this configuration. We also made progress on p-type CZ wafers and achieved 18.7% independently confirmed efficiency with little degradation under prolong illumination. Our best $V_{oc}$ for a p-type SHJ cell is 0.688 V, which is close to the 691 mV we achieved for SHJ cells on n-type c-Si wafers.

INTRODUCTION
Crystal silicon heterojunction solar cells use hydrogenated amorphous silicon (a-Si:H) as a thin, wide band gap layer that wraps around a high quality c-Si wafer passivating the emitter at the front and the contact in the back. These heterojunctions preserve the minority carrier lifetime in the bulk and reduce the surface recombination in crystal silicon heterojunction (SHJ) solar cells. As a consequence, SHJ cells have a high open-circuit voltage and high efficiency. The low temperature (<250ºC) and manufacturable processes have a great potential for large volume production of solar modules to meet the demand of rapid growth for solar electricity. The best cell efficiency has reached over 22% from Sanyo’s R&D lab [1]. The high open-circuit voltage (0.725 V) is believed to be a key to obtaining a low temperature coefficient for power output. The low processing temperature for c-Si solar cell production enables a low thermal budget and avoids bowing of thin wafers: this is a promising approach for the future thin c-Si wafer manufacturing.

Most crystal silicon heterojunction solar cells are processed by plasma enhanced chemical vapor deposition (PECVD): the standard a-Si:H deposition technique using an rf electric field to decompose silane gas. The Sanyo group has demonstrated high voltage and high efficiency HIT (heterojunction with thin intrinsic layer) cells using this process technique. We use hot-wire chemical vapor deposition (HWCVD) to fabricate SHJ solar cells - an alternative a-Si:H growth technique using a high temperature filament (~2000ºC) to decompose silane. We reported our understanding in the key areas of c-Si surface cleaning, conditions for depositing a good a-Si:H/c-Si hetero-interface, conformal coverage on rough textured surfaces, and effective ways to form emitter and back contacts [2-7]. We have explored the advantages of HWCVD compared to PECVD in the processing of SHJ solar cells. Our best efficiency to-date is 19.1% in p-type FZ-Si wafers and 18.7% in p-type CZ wafers. Our best voltage is 0.688 V and 0.691 V in p-type and n-type FZ wafers, respectively.

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Figure 1: The scheme of a-Si:H/c-Si heterojunction solar cell. Up solid lines are conduction band. Bottom solid lines are valence band. The dash lines are Fermi energy for electrons and holes. Dots are carriers of electron and hole. The circle indicated a high barrier at p-type contact.

The basic principle of a heterojunction solar cell is to use wider gap materials to contact the c-Si such that carriers only go through the contact in one direction [8]. Figure 1 shows the schematics of the a-Si:H and c-Si heterojunction. The barriers at the conduction band only allow electrons to travel toward the a-Si:H (n) side. However, the barriers at the valence band seem to confine holes inside the c-Si because of high barriers at both the a-Si:H and the c-Si emitter and contact. However, holes do pass thorough the barrier and move to the a-Si:H (p) side. It is believed that tunneling occurs in the a-Si:H (p) layers.
Figure 2. Structures of double-side SHJ c-Si solar cells used in this study. a) with ITO contact at the back, and b) with metal directly contacting the back doped layer.

EXPERIMENTAL

We use high quality float-zone (FZ) both $n$-type and $p$-type crystal Si wafers (either polished or anisotropically textured) and CZ wafers for high-efficiency cell development and study. The Si wafers are (100) orientated, 220 to 300 µm in thickness, and 1-4 Ω·cm in resistivity. The minority carrier lifetime is on the order of 1 ms measured by a Sinton lifetime tester. All the wafers are subject to a thorough wet chemical cleaning process and a final 2-5% HF cleaning before being loaded into a HWCVD a-Si:H deposition chamber.

Texturing of the c-Si was done at NREL. We use 3-5% KOH with IPA at 80°C for both $p$-type and $n$-type wafers. The feature size of the pyramids is less than 10 microns measured using scanning electron microscope (SEM).

In the hot-wire CVD process, we use the multi-chamber T-system at NREL [9] to fabricate the emitter and back a-Si:H contact. In general, a load-locked multi-chamber system was used to avoid cross-contamination from different types of dopants in the different layers. We also used various filament materials such as Ta and W but kept the distance from substrate to the filament constant at 5 cm. We use pure SiH₄ at a 20-sccm flow rate and 10 mTorr for intrinsic a-Si:H, with a substrate T of about 100°C. The low process temperature allows us to grow pure amorphous silicon directly on c-Si. The optimized i-layer thickness is about 3 nm and the growth rate ranges from 3 to 12 Å/s. Lower deposition rate allow us to better control the thickness of the i-layer because it only takes a few seconds. The doped emitter and back-contact layers were deposited at a higher temperature from PH₃/SiH₄/H₂ (~200°C) and B₂H₆/SiH₄/H₂ (~250°C) doping gas mixtures. Their thickness is about 4-6 nm.

Figure 2 shows our SHJ cells’ structure. From top to bottom, grid/ITO/a-Si:H/c-Si(n or p)/a-Si:H/Ito/metal in Fig 2 a); or grid/ITO/a-Si:H/c-Si(n or p)/a-Si:H/metal in Fig 2 b). The finished cell is about 1 cm² in area with a 5%-coverage metal grid on top of the ITO. Confirming JV measurements were done at NREL by the accredited PV Performance Characterization Team. Standard JV measurement was done by NREL’s XT-10 solar simulator. High-resolution transmission electron microscopy (HRTEM) was used to study the interfaces, the thickness, and conformal coverage of the a-Si:H and ITO layer.

RESULTS

Figure 3 shows our record 19.1% SHJ cells on p-type FZ wafer. This cell has a $V_{oc}$ of 0.678 V, FF of 0.779, $J_{sc}$ of 35.9 mA/cm². The cell structure is grid/ITO/n/i/p-cSi(p)/i/p/Al. The thickness of i/n layer is about 10 nm (confirmed by TEM measurement). The c-Si wafer size is about 2.5 x 4.5 cm². Front ITO thickness is about 900 nm and was photolithographically defined and etched to 1 cm² for two cells per wafer. A 0.9 cm² mask covers the cell during the JV measurement.

We used a standard RCA 1 and 2 clean procedure after in-house texturing the wafer before deposition of the a-Si:H emitter and back contact. We found this clean procedure was enough to remove the residual impurities and have a good $V_{oc}$ on textured wafers. Earlier, we have used our extensive clean procedure for flat wafers on textured ones with less success. We found that some of the textured features were removed after the chemical wet clean. Therefore, we may keep the surface clean with high $V_{oc}$ but lost the optical enhancement. In searching for a new cleaning procedure for textured wafers, it is helpful that the standard RCA process gives good results. We will start from here and eventually improve the cleaning process.

We found that the double-heterojunction was essential for high $V_{oc}$ [3]. With a-Si:H double heterojunctions, the lifetime of the minority carriers is in the range of 1 ms and the back surface recombination velocity can be reduced to ~15 cm/s. high lifetime and low surface recombination velocity are the factors to improve cell performance. Many other groups [10-13] also reported the effective surface passivation of a-Si:H to c-Si.

In addition to high lifetime, we found that contact formation to the thin doped a-Si:H layer was also critical [7]. We reported before that Ti directly deposited on thin doped a-Si:H layers caused a decrease in $V_{oc}$. Our early SHJ cells suffered from a low FF. The ITO on the back contact of the heterojunction solar cells was considered the cause. We tried to use a metal with much higher conductivity than the TCO to directly contact the a-Si:H doped layer to reduce the FF loss. We succeeded in improving the FF but discovered complications. Figure 2 describes two structures with techniques for forming back
contacts: a) with an ITO intermediate layer to enhance optical back reflection, and b) with simpler direct metal contacts such as Al or Ti. With an ITO contact to the back doped layer, we found that we can reach a high $V_{oc}$ of 0.680 V. When we use Ti direct contact to the same doped-layer the $V_{oc}$ decreases by 56 mV. However, when we deposit a much thicker doped a-Si:H layer (6 times increased deposition time) with the Ti contact, $V_{oc}$ is restored to about 0.680 V. This effect can be very important to avoid possible metal indiffusion at the back and make a high $V_{oc}$ cell. An Al contact to a $p$-type a-Si:H layer seems to form a good contact with a high $V_{oc}$. Notice that our record cell used an Al direct contact to the $p$-layer in the back. This did not cause a rapid decrease of $V_{oc}$ as we mention before with the Ti contact. It seems that some metals are easier diffusers than others.

Table 1 summarizes our best double-side SHJ solar cells' performance. For cells with planar surfaces, it seems that $n$-type c-Si cells have a slightly higher $V_{oc}$ but a worse Fill factor (FF) than the $p$-type c-Si cells. Both 0.691 and 0.688 V are the highest $V_{oc}$ of SHJ cells ever made by HWCVD. We attribute this high $V_{oc}$ to proper surface cleaning before the Si deposition and the a rapid transition from the c-Si surface to growth of a-Si:H by HWCVD. For the textured cell, we have better performance on our $p$-type cells. In $n$-type c-Si, the lower $V_{oc}$ in textured one may be related to the difficulty in cleaning the textured surface. We are still optimizing cleaning with a goal of a $V_{oc}$ close to the planar one of 0.69 V. We are also optimizing our texture to gain more

Table 1. Summary of the best double-sided SHJ 1 cm$^2$ cells by HWCVD, fabricated at NREL.

<table>
<thead>
<tr>
<th></th>
<th>$V_{oc}$ (V)</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$p$-type</td>
<td>0.688</td>
<td>31.6</td>
<td>81.3</td>
<td>17.7</td>
</tr>
<tr>
<td>(planar)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n$-type</td>
<td>0.691</td>
<td>33.6</td>
<td>72.1</td>
<td>16.7</td>
</tr>
<tr>
<td>(planar)**</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$p$-type</td>
<td>0.678</td>
<td>35.9</td>
<td>78.6</td>
<td>19.1</td>
</tr>
<tr>
<td>(textured)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$n$-type</td>
<td>0.664</td>
<td>35.3</td>
<td>74.5</td>
<td>17.2</td>
</tr>
<tr>
<td>(textured)*</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

** Independently confirmed by NREL PV Performance Characterization Team
* measured by using calibrated NREL XT-10 solar simulator.

In summary of our SHJ cells research, we use planar wafers as our baseline because the cleaning and coverage of the films is relatively easy. This gave us a good starting point. We found that the wafer with a carrier lifetime over 700 µs after a-Si:H emitter and back contact, in general, will lead to a $V_{oc}$ over 0.680 V. Once the wafer can have a high $V_{oc}$, we texture the wafer and make high efficiency cells.
in the short circuit current ($J_{sc}$). Our 36 mA/cm$^2$ is much lower than Sanyo’s standard textured cells (37-39 mA/cm$^2$).

We use SEM and TEM to further investigate our textured SHJ solar cell. Figure 4a shows SEM picture of our 19% SHJ cell’s textured surface. It appears that the surface was textured with less than 10 µm pyramids. Our texturing still needs some improvement. The distribution of the pyramid’s size is still too large.

Figure 4b of TEM picture shows that our a-Si:H thin layers and ITO are conformally covering the textured surface even at the tip and the valley of the pyramids. Experimentally, TEM confirms that HWCVD has provided high quality conformal layers even at a few nm in thickness and so does our ITO coating. We believe that the conformal coating of HWCVD is one of the keys to making high $V_{oc}$ textured SHJ cells.

Figure 5. Efficiency of a p-type CZ wafer SHJ cell as a function of light exposure time.

Figure 5 shows light soaking data on our CZ p-type SHJ solar cell. Our data show that there is little degradation on CZ p-type c-Si regard to a-Si:H related issues. We have not excluded B-O related degradation but the stable efficiency is high. We concluded that widely available p-type CZ c-Si can be used for SHJ solar cell. Currently, only n-type c-Si SHJ solar cells are in production.

DISCUSSIONS

We used Figure 6 to discuss the issues with SHJ solar cells and a pathway to even higher efficiency. Figure 6 shows an Internal quantum efficiency (IQE) data of PERL cell from University of New South Wales [14], HIT cell from Sanyo [15], and SHJ cell from NREL. It clearly shows that Sanyo and NREL cell have a similar IQE. However, both IQE have a less response in the infrared region, from 1000 to 1200 nm, compared to the PERL cell. This leads to a $J_{sc}$ deficit about 4 mA/cm$^2$. A record PERL cell has $J_{sc}$ about 43 mA/cm$^2$ and the best HIT cell has a $J_{sc}$ of 39 mA/cm$^2$. Increase red response in SHJ cell will be the key for further improvement of cell efficiency and ultimately a record efficiency over 25%.

Figure 6: Internal quantum efficiency comparison between SHJ cells and PERL cells

SUMMARY

The advantages of using HWCVD in comparison to plasma-enhanced CVD are the fast deposition rate and, more important, the wide deposition parameters for forming conformal covered heterojunctions of high $V_{oc}$. Additionally, the low temperature (below 200°C for entire cell process) makes HWCVD one of only a few promising methods for the production of next generation ultra-thin Si wafer solar cells with low stress.

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