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Expanding the Limits of CdTe PV Performance

Phase I Annual Report
7 February 2006 — 30 June 2007

P. Meyers
First Solar
Perrysburg, Ohio

Subcontract Report
NREL/SR-520-42421
December 2007

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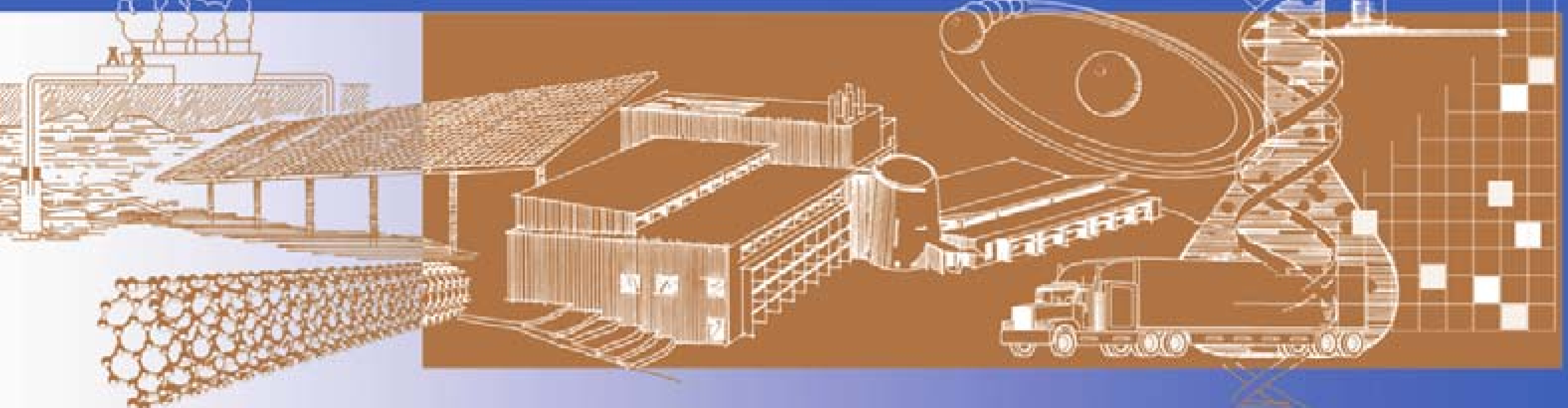

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ABSTRACT

Expanding the Limits (ETL) includes evaluation of a broad range of materials and device structures in order to select a device structure suitable for achieving optimum power conversion efficiency and stable field performance. During Phase I of the program researchers explored radical materials integration concepts and dealt with the complexity of the various materials interactions. Once a suitable range for deposition of each exploratory material had been established devices were produced in order to determine what material or process interactions might exist that would directly impact the suitability of the advanced device concept to achieve unit process improvement. Preliminary evaluation of device performance has been completed on nine alternative CdTe PV device structures. Selected front side and back side structures were evaluated by light soaking as a means of obtaining a rough prediction of baseline field performance. Two front side and one back side structures exhibit improved Jsc and Voc, respectively, compared to First Solar's current Base device structure. The best confirmed cell efficiency was 14.13%. Optimization of combined front side and back side structures is not complete.

Additional work was directed toward assessing the physical limits of polycrystalline PV device performance as imposed by device architecture and materials science. During Phase I of this contract work in this area focused on identification of the key material properties believed to be responsible for existing device performance and methods for their quantitative analysis. An unexpected result of this analysis is the indication that fill factor (FF) has significant deficiencies as a metric for optimizing polycrystalline CdTe PV device performance. It us suggested that effective evaluation of device performance requires by-passing FF in favor of improved 2LM that are more directly related to fundamental material properties. It is suggested that alternative 2LM should relate to photocurrent, carrier recombination, space charge distribution, internal resistance, shunt conductance, and micro-nonuniformity – all as measured at Vmp. Material properties of polycrystalline CdTe are discussed and a path for improving efficiency is suggested.

1 INTRODUCTION

1.1 Objectives

A broad objective of the Expanding the Limits program, ETL, is to provide for First Solar and the PV community an accurate assessment of the potential and limitations of CdTe PV technology. A specific objective is fabrication and analysis of champion cells and modules. Deliverables include 15%, 16% and 17% efficient 1 cm^2 cells at the end of Phases I, II and III, respectively.

ETL contributes to achievement of two DOE PV year 2011 milestones: achieving 10% efficient production CdTe modules and demonstration through accelerated life testing a 20-year life for production CdTe modules. As the largest PV module manufacturer in the United States and the largest thin film PV module manufacturer in the world, First Solar has a clear focus on manufacturing. We have sold >100 MW of PV modules to date and are actively expanding manufacturing capability. By the end of 2008 we expect to have nameplate capacity of 330 MW/yr of thin film PV modules. 100% of our current and planned capacity is based on thin film CdTe PV. ETL complements existing optimization programs by exploring disruptive or "out-of-the-box" device structures that might not otherwise be evaluated through evolutionary optimization of First Solar's current product.

1.2 Technical Approach

Research focuses on three complementary activities: 1) Fabrication of device structures expected to achieve enhanced performance, 2) Analysis of the device physics and identification of the physical, chemical, electrical and optical properties responsible for performance, and 3) Development of the fundamental materials science that underlies the practical realization of the required physical, chemical, electrical and optical properties required to achieve optimum device performance. Research activities are designed to be iterative in that knowledge of the fundamental materials science shall be applied to fabrication of improved device structures in a cycle of continuous improvement.

During the initial phases of the research restrictions imposed by considerations of cost, throughput and process compatibility shall be greatly eased so that the impact of those restrictions can be accurately assessed. Thus, for example, devices may be produced on relatively expensive borosilicate glass. Similarly, considerations of compatibility of device fabrication with the interconnect process shall be largely ignored. Beginning in Phase II, after the technological limits have been better defined; research will be directed toward identifying and overcoming obstacles to commercial implementation of the highest performing device structures.

Exploratory work has been directed toward expanding rather than replacing existing First Solar technology. For example all device fabrication includes CdTe deposited by vapor transport deposition (VTD) on module-scale (60 cm X 120 cm) substrates. Nonetheless, it is expected that modified device structures may necessitate some modifications to device fabrication procedures and these modifications will be developed as required.

Exploratory work is aimed at improving fundamental or "common cause" limits on device performance. Thus, although champion devices cannot be made with poor quality films and it is well known that film defects or micro-non uniformity can significantly degrade performance, development of procedures that reduce spatial non-uniformity (microscopic or macroscopic) or process variation on the production line are not the direct object of this program.

Finally, it is important to note that performance relates both to efficiency and stability. While there is no generally accepted definition for stabilized efficiency within the CdTe PV community, it is well known that voltage bias, illumination, temperature and ambient can affect device performance over time. Although a specific accelerated life test protocol has not been adopted, rudimentary stress testing has been utilized in order to weed out structures and materials that are poorly suited for stable performance in the field. Device measurements and characterization are performed in order to identify and quantify the optical and electrical properties. Interpretation of the results relies in part on pre-existing device simulation studies performed at First Solar.
During Phase I the technical approach has been to screen a relatively large number of "front side" and "backside" device structures. With reference to Fig. 1, front side structures encompass combinations of alternative anti-reflective coatings, glass superstrates, ion diffusion barriers, transparent conducting oxide electrodes, high resistivity transparent layers and n-type window layers. In general the objective is to increase Jsc without reducing Voc or FF. Backside structures encompass alternative low resistance interface layers and metal electrodes. In this case the objective is to increase Voc and FF.

Each alternative structure was evaluated with a relatively wide range of process variations, but full optimization of performance was not expected during this screening phase of the program. Devices that displayed promise of meeting the objectives listed above were stress tested. At the conclusion of this screening process – expected to be completed in the early part of Phase II, one or more front side and backside combinations will be down selected for optimization of the combined structure. Further details of ETL Phase I program tasks, milestones and deliverables are listed in Appendix 1.

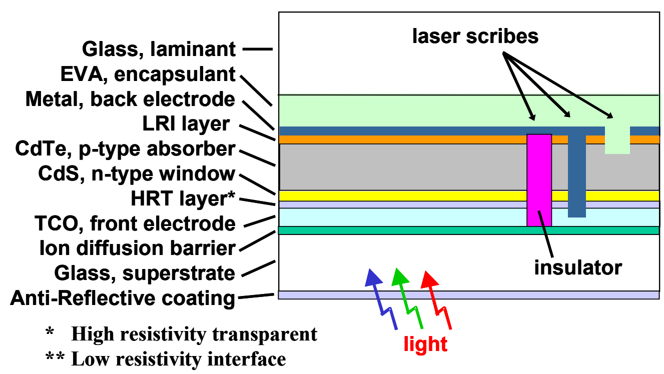

Figure 1: Schematic of CdTe/CdS PV module showing monolithic interconnect.

2 DEVICE STRUCTURE SCREENING STUDIES

During Phase I five front side and four backside device structures have undergone preliminary evaluation and two front side and two backside structures were selected for stress testing. In order to enable meaningful evaluation of progress without disclosing proprietary information, results are displayed in normalized units in comparison to those obtained with our current commercial device structure – referred to herein as the "Base" structure. Initial and post-stress results are displayed in Figures 2-5 below.

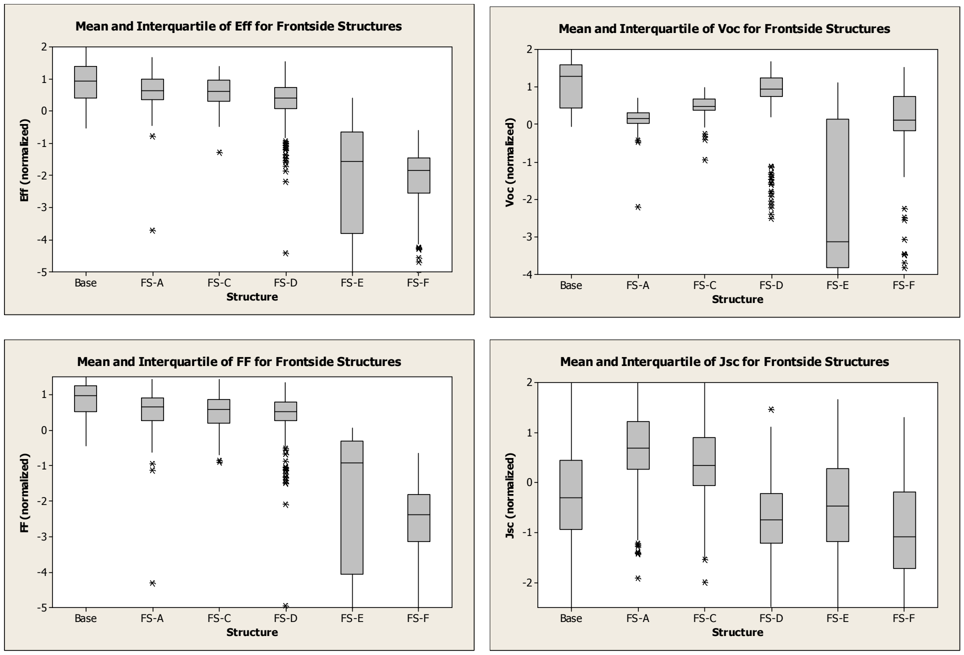

Figure 2: Initial performance of five alternative front side structures plus the Base structure. Data are expressed in normalized units (subtract mean and divide by standard deviation).

Of the five front side structures evaluated, two were selected for stress testing. As displayed in Fig. 3, both structures displayed enhanced Jsc compared to the base case, but due to their relatively lower Voc and FF neither structure exhibited significantly superior overall efficiency.

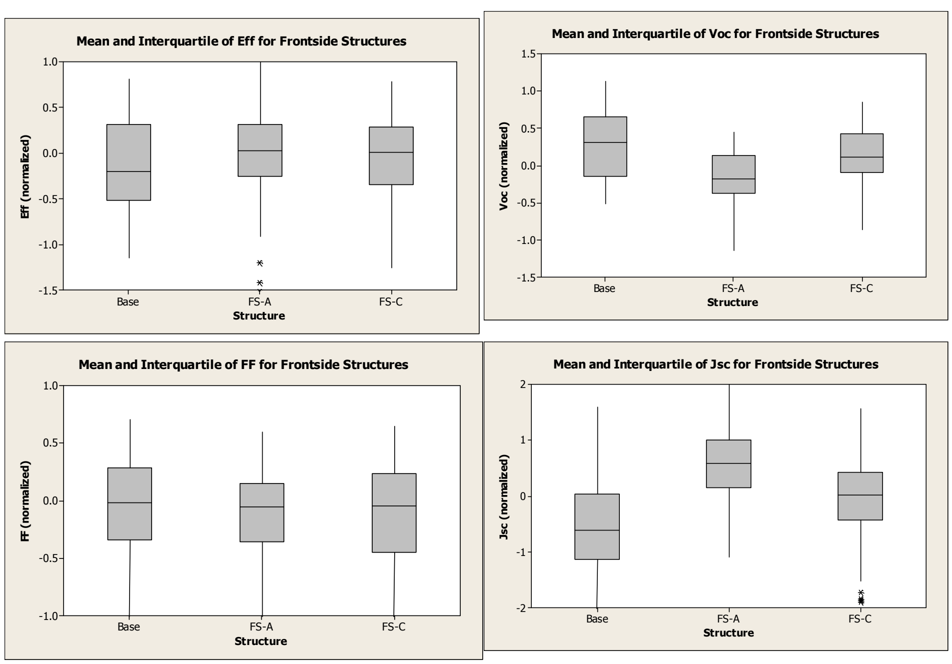

Figure 3: Distribution of post-stress Efficiency, Voc, FF and Jsc for two front side structures plus Base.

Similarly, of the four backside structures evaluated, two were selected for stress testing. Initial performance is displayed in Fig. 4. Fig. 5 shows that after stress testing one backside structure displays enhanced Voc and minimally improved efficiency.

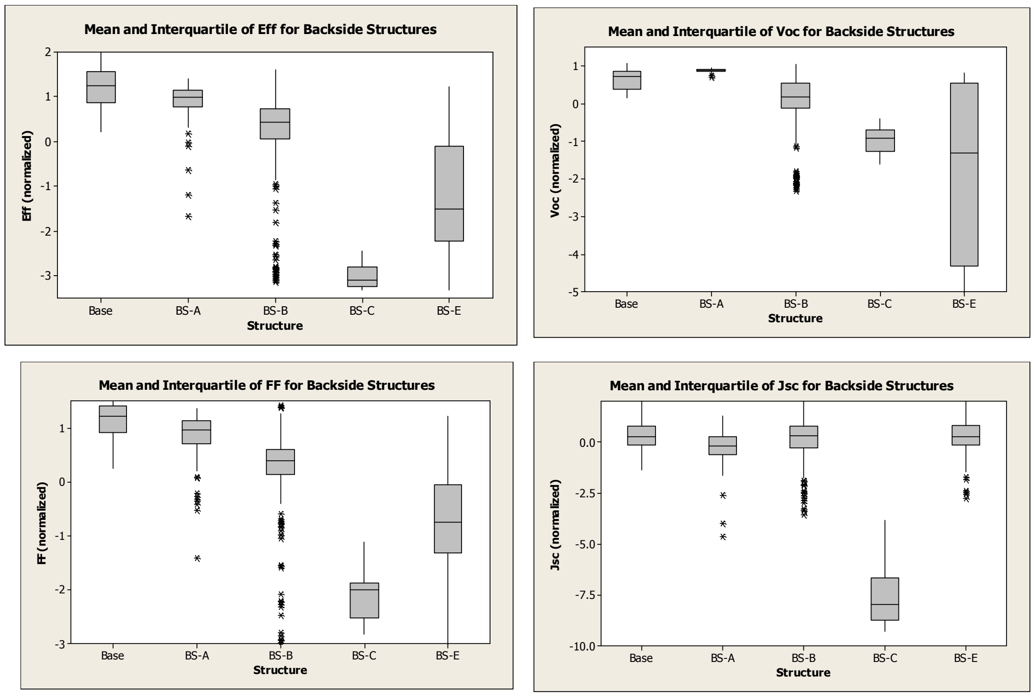

Figure 4: Distribution of initial Efficiency, Voc, FF and Jsc for four backside structures plus Base.

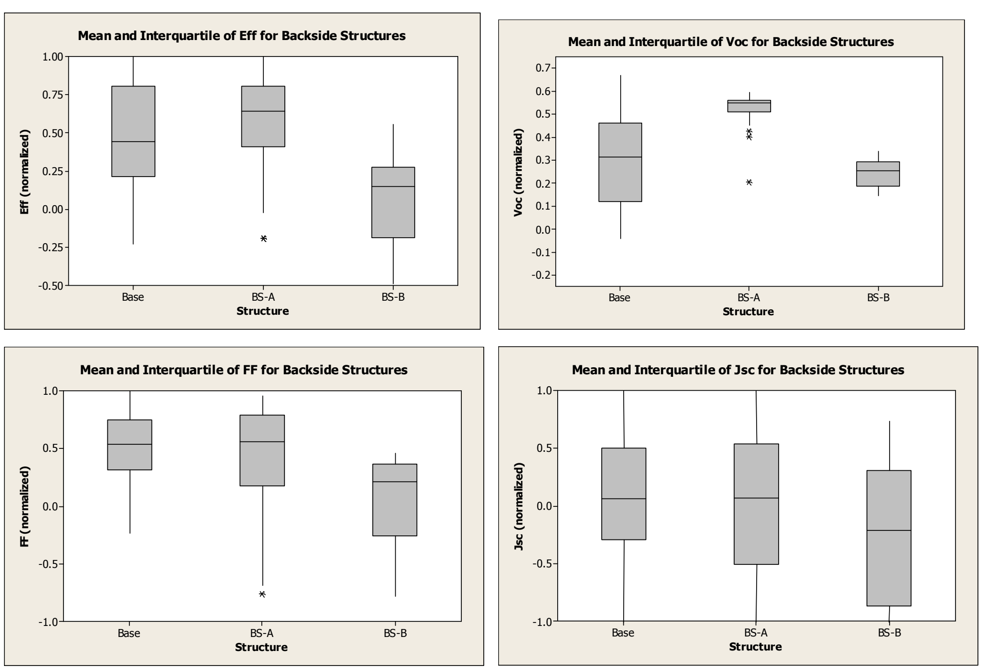

Figure 5: Distribution of post-stress Efficiency, Voc, FF and Jsc for two backside structures plus Base.

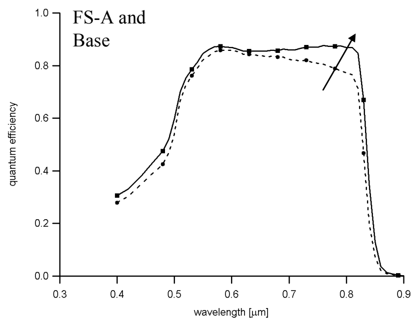

Figure 6: Comparison of quantum efficiency of the FS-A and Base structures indicates qualitative differences responsible for the improved Jsc of FS-A.

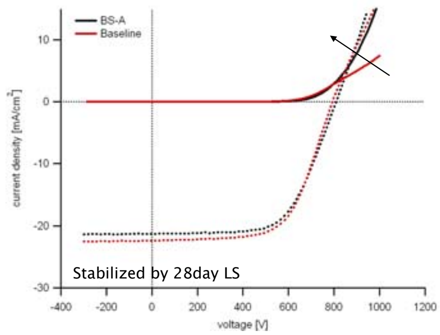

Figure 7: Comparison of the light-dark crossover points from the Base and BS-A structures indicates that the BS-A back contact has qualitatively lower resistance than that of the Base structure.

Additional characterization of devices was performed in order to determine whether the observed improvements in device performance was based on fundamental differences between the experimental and Base structures or simply reflect the upper end of the distribution curve. As shown in Fig. 6, the quantum efficiency curve of FS-A displays a significantly different and improved response than does the Base structure. Fig. 7 demonstrates that BS-A has an improved post-stress I-V contact.

Results to date suggest that Jsc and Voc can be improved over Base performance by incorporation of structures FS-A or FS-B and BS-A, respectively. Evaluation of additional front side and backside structures is planned, however, prior to down selection of at least one front side and backside structure for combination into a single structure for overall optimization.

3 CHAMPION CELL PERFORMANCE

Although the advanced cell designs described above have not yet been optimized, in order to assess progress against the Phase I milestone of a 15% efficient 1 cm^2 cell, researchers prepared 1 cm^2 cells representing the best available technology for efficiency measurement at NREL. Best single cell results were 14.13% (23.8 mA/cm^2 Jsc, 73% FF, 813 mV Voc). The IV curve is displayed in Figure 8.

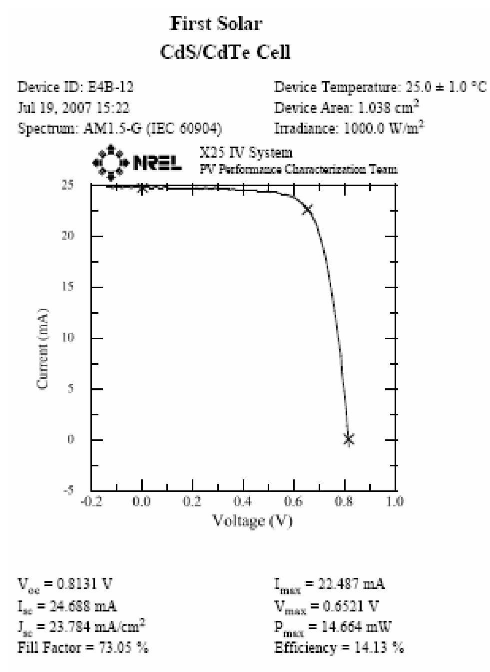

Figure 8: Champion cell performance achieved during ETL Phase I

4 DEVICE ANALYSIS

4.1 Introduction

Device characterization at First Solar has been expanded during phase I of the ETL contract to enable us to perform temperature dependent current voltage and capacitance measurements. A temperature chamber with limited T range (-75C < T < 75C) was chosen for its speed and versatility over a cryostat. A custom built light source and IV scanner are used for IV measurements. An Agilent E4980A was acquired and is used for capacitance measurements. Custom software has been implemented to allow for measurements of capacitance-frequency, capacitance-voltage, capacitance-transients, and current-voltage sweeps at varying bias light intensities, temperature, voltage bias, etc.

4.2 Baseline Measurements

The following results were acquired on a “control” sample. Figure 9 shows the room temperature IV performance of the cell studied. Results from the characterization over the entire temperature range are presented in the following.

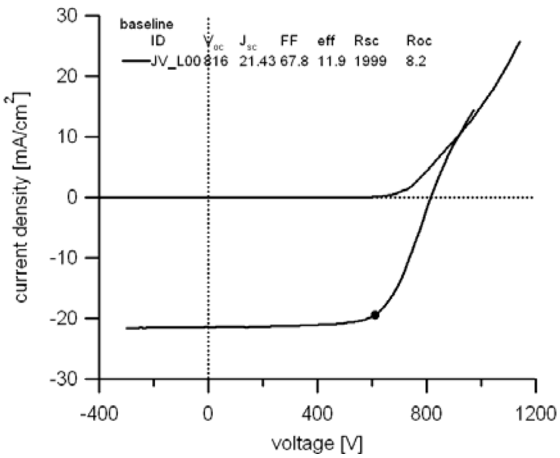

Figure 9: Baseline, RT IV performance.

4.3 I-V-T

The focus of temperature dependent IV measurements lies on determining dominating recombination and loss mechanisms. Parasitic blocking back-contacts are responsive to temperature and therefore their behavior can be investigated and/or mitigated by measuring the device at elevated or reduced temperatures.

Figure 10 shows IV measurements taken at temperatures varying from -75C to 75C in 10C increments. The strong roll-over at low device temperature is clearly noticeable, as is the reduced roll-over at increased temperatures. Also clearly visible is the current contribution from the electron current that occurs at a higher device voltage at low temperature. A commonly used method to determine the limiting recombination mechanism is the extrapolation of the open-circuit voltage vs. temperature. Figure 10 (right) shows this information and provides clear evidence that the recombination is described with an activation energy near the CdTe band-gap.

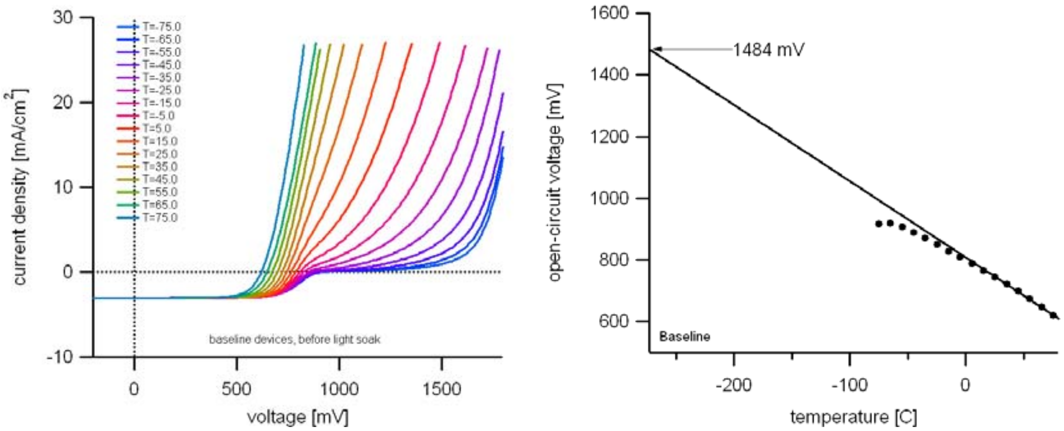

Figure 10: (left) baseline IV measurements (not 1 sun), and (right) extrapolation of Voc vs temperature to zero Kelvin.

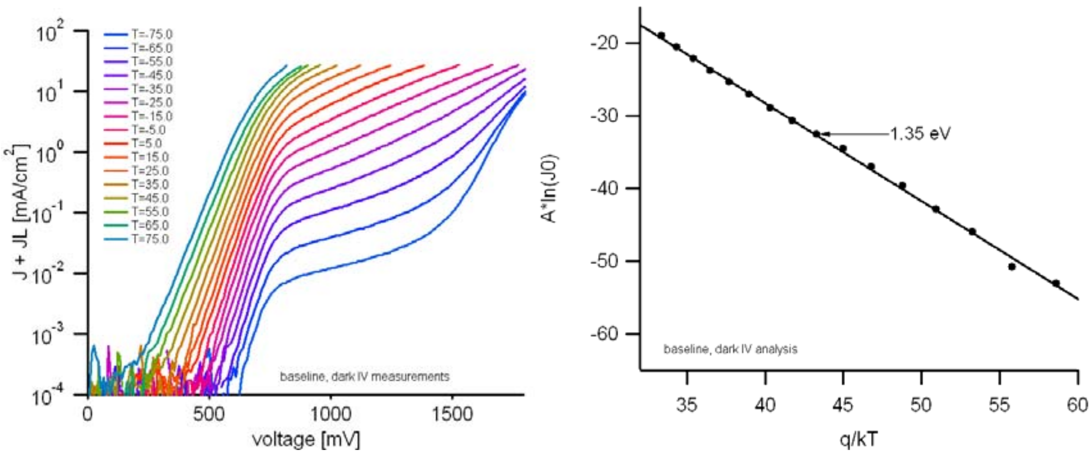

Figure 11: (left) dark IV measurements at various temperatures and (right) extraction of the recombination energy.

Figure 11 shows dark IV measurements. The data are well-behaved and noise-free to currents as low as 10^{-3} mA/cm^2. At the increased temperatures, the effects of the blocking back-contact can be mitigated and it is possible to reliably identify the main junction properties. Using the CurVA program (developed at Colorado State University), diode analysis is performed. The series resistance is found to be 4.15 Ωcm^2. It is noteworthy, that these test samples use different aspect ratios than our standard product and measurements are performed using 2 point probe contacts. Diode quality factor is found to be nearly temperature independent at the higher temperatures with values as low as 1.45. At room temperature, the diode saturation current as measured from dark IV traces is on the order of 10^{-8} mA/cm^2.

The primary diode turn-on is analyzed in the first linear regime for all temperatures and from this information the recombination barrier is estimated by the A*lnJ_0 method as 1.35 eV, which is noticeably lower than the number determined from the "Voc vs T" method. The discrepancy is caused by the changes that are introduced in the device with light bias and voltage bias. The latter method studies dark IV traces at low currents, whereas the Voc method studies traces at the open-circuit voltage under 1 sun illumination. The "less than the band-gap barrier" of 1.35 eV suggests that device performance may be reduced by a secondary recombination path through the CdS/CdTe interface.

4.4 Capacitance-Voltage

Capacitance voltage profiling is commonly used to assess "apparent" doping profiles in thin-film solar cells. The term "apparent" is intended to describe the contribution of deep defect levels that can contribute to the CV profile. We distinguish "doping" and "deep level" contributions to the capacitance signal by performing measurements at varying frequencies, biases, temperatures, and with and without light bias.

The CV profiles have shown a range of temperature dependencies in our standard devices. Representative data is displayed in Figure 12. Under illumination the temperature dependence is always reduced, which could be interpreted such as that the light generated free carriers increase the rate of charge release or capture from these deep levels. Under illumination the zero-bias depletion width is ~0.7 microns over the entire temperature range. The doping profiles show typical increases towards the back-contact, but the relatively high bulk doping prevents the device from reaching full depletion.

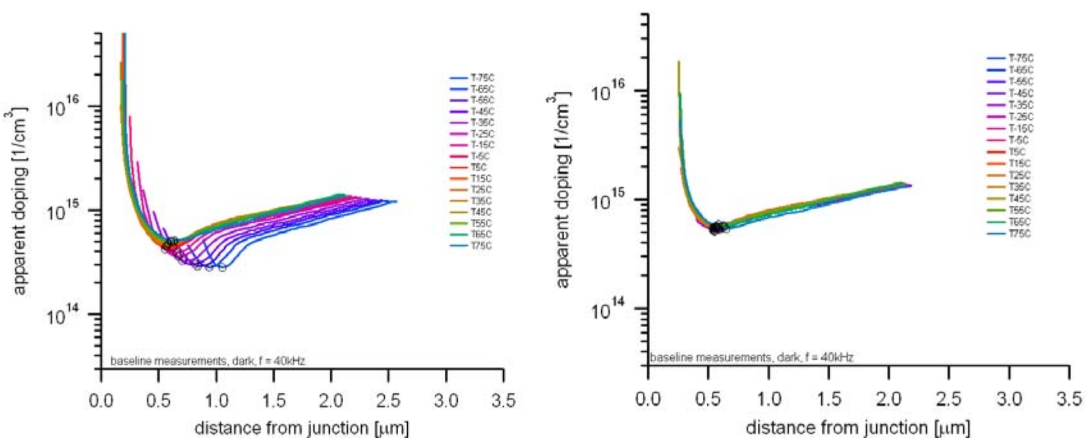

Figure 12: (left) dark and (right) illuminated C-V measurements.

4.5 Capacitance-Frequency

Measurements of capacitance frequency at various temperatures are ideally performed over the broadest possible range of temperatures and frequencies. Our set-up is limited in both aspects and, hence, allows us to study response from a relatively narrow energy range. One prominent response that is typically found in admittance spectroscopy is a Cu related trap level forming a deep acceptor level somewhere between 0.2-0.4 eV.

Figure 13b shows typical results for a standard device measured at zero bias. The observed step has an energy level in the range of 0.3-0.4 eV. At low frequency and high temperatures an additional step seems to appear, but the limited range does not allow identification of its energy.

4.6 Outlook

As we progress in our development, the above described characterization methods will be refined and applied to alternative device structures. A better assessment of doping, possible detection of interfering/compensating deep levels, identification of limiting recombination mechanisms is expected. To further solidify the understanding of these results we pursue device modeling that will reproduce the above shown results.

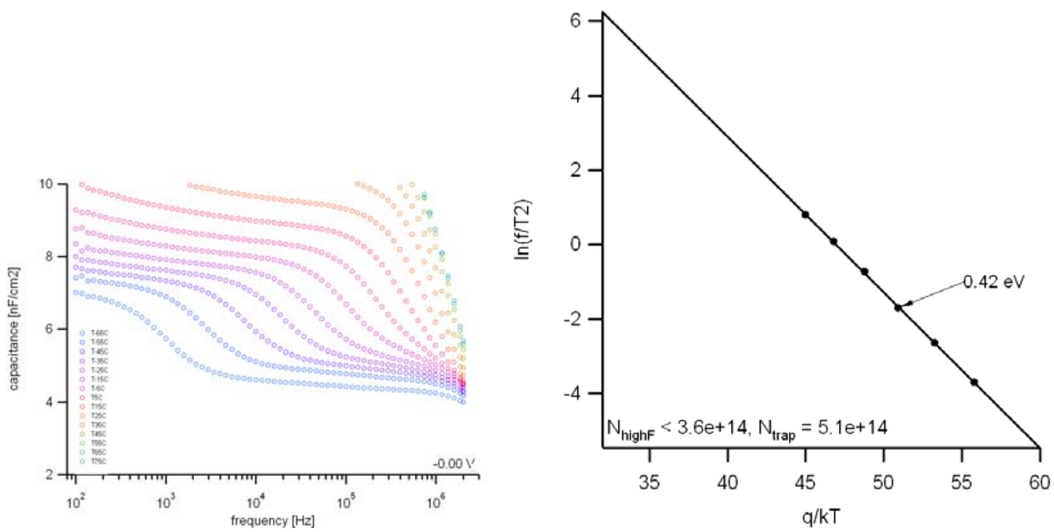

Figure 13: C-f measurements on baseline sample at zero bias and data plotted for determination of the trap level energy.

5 SECOND AND THIRD LEVEL METRICS (2LM AND 3LM)

5.1 Motivation for Alternative 2LM

Although development of improved metrics is not a primary goal of the ETL program, lack of effective methods for practical characterization of device performance slows the evaluation and optimization process and leaves uncertain the specific impact of the various device architecture modifications and process variations. Researchers are therefore considering alternative metrics that can provide practical, effective and timely feedback as we explore advanced cell designs and processing methods.

As the value to the experimentalist is that insight obtained through identification and quantification of loss mechanisms enables more effective development of alternative device designs and process optimizations, in order to be most effective, ideal 2LM should have quantified impact on efficiency, be site-specific, be measurable in the laboratory within a time that allows effective feedback to process optimization.

5.2 Conventional 2LM

Traditional methods of detailed analysis of device performance focus on a development of a detailed understanding of the underlying device physics which can then be compared to experimental results through simulation. In principle simulation of individual device performance provides the experimentalist with detailed information regarding loss mechanisms and areas for improvement in real devices. Work by Samuel Demtsu and Jim Sites[1] provides an excellent baseline for analysis of factors limiting device performance in CdTe solar cells. Second and third level metrics (2LM and 3LM) from their analysis are summarized in Table 1.

Table 1. Third level metrics for each 2LM as quantified by Demtsu and Sites.[1]

	Prod	Record	Target	R- P [Δη%]	T- R [Δη%]
J_{sc} Losses [mA/cm^2]					
Reflection	1.9	1.9	1.8	0	0.1
Glass abs.	1.8	0.7	0.3	1.4	0.2
TCO abs.	1.1	Incl	0.3	Incl	Incl
Cds abs.	4.6	1.4	1.2	2.3	0.2
Deep penetration.	0.7	0.8	0.6	-0.1	0.2
Total				3.6	0.7

A. Current Losses

	Prod.	Record	Target	R- P [Δη%]	T-R [Δη%]
V_{oc} Losses					
v_r/v_{th}	7x10^{-2}	2.5x10^{-2}	1x10^{-2}	0.9	1.1

B. Voc Losses

	Prod.	Record	Target	R-P [Δη%]	T-R [Δη%]
FF Losses					
A-Factor	2.2	1.9	1.8	0.4	0.1
R[Ω-cm^2]	6.0	1.2	0.5	1.4	0.3
G [mS/cm^2]	0.2	0.6	0.3	-0.1	0.1
J_L (V) [FF %]	1.0	1.0	1.0	0	0
Low V_{oc}[FF%]	3.2	2.4	1.8	0.2	0.2
Back contact [FF %]	3.8	0	0	0.5	0
Total				2.4	0.7

C. FF Loses

From an experimental perspective Jsc and its associated 3LM listed in Table 1A are almost ideal in that each loss is independently quantifiable in units directly applicable to device performance. Incident light spectral content and intensity can be independently measured as can losses due to reflection, absorption and transmission. Results from this analysis can be directly compared with photocurrent, Jph which experimentally is essentially equal to J measured at reverse bias. Confidence in these metrics in increased by analysis of the spectral content of each loss mechanism and their comparison with quantum efficiency measurement.

Metrics relating to Voc and FF, at least from an experimental perspective, are more problematic. Although the Demtsu et al. analysis is based on our best understanding of the underlying device physics, in practice it is difficult to use the indicated metrics to quantify the impact that specific elements of the device under test have on measured device performance. In practice the 3LM underlying Voc and FF – e.g., recombination velocity, A-factor, series and shunt resistance and

[1] S.H. Demtsu and J.R. Sites, "Quantification of Losses in Thin-Film CdS/CdTe Solar Cells", Proc. IEEE PVSC 2005, pp347-350; see also Appendix 1 from the Feb. 2004 CdTe Team Meeting.

back contact barriers - are obtained by curve fitting of IV data and there are often a range of adjustable parameters that can be used to fit real IV data within experimental error. Confidence in the model and its fitting parameters can, of course, be greatly improved by additional measurements. For example capacitance-voltage (CV) measurements can be used to define a net dopant profile. As demonstrated by Fahrenbruch[2], however, even in the case of simulation in which the input assumptions are known, analysis of results is quite complex and can be misleading. At least at First Solar analysis of large sets of measurements has been used primarily to develop fundamental understanding and has not been applied directly to the day-to-day device optimization process.

5.3 p-i-n Device Model

Development of a general set of improved practical metrics is beyond the scope of this work as the focus of this program is on developing metrics that help us define the limits of polycrystalline CdTe PV device performance. The scope is further narrowed in that within the ETL program researchers are focusing on the p-i-n device structure. Reasons that the p-i-n structure is believed to be best suited for polycrystalline CdTe devices include:

- CdTe has a strong tendency to self-compensate, thus achieving the high doping levels required to achieve high Voc p-n devices is problematic. Self-compensation is likely to have an even stronger impact in polycrystalline films.
- Device simulations indicate that >20% efficient polycrystalline CdTe p-i-n devices are possible[3,4] - suggesting that there is no efficiency trade-off for adopting the p-i-n structure
- Use of thin CdTe devices reduces material costs
- Use of thin CdTe reduces environmental impact

Figure 14 displays a highly idealized set of energy band diagrams depicting the p-i-n device structure and listing some of the material properties expected to produce high power conversion efficiency. The 2LM and 3LM discussed below have been selected with p-i-n devices in mind and are not necessarily appropriate for other device structures.

5.4 Alternative 2LM

Rather than try to fit the entire IV curve, the approach to metric development currently being explored within the ETL program is to focus on metrics that directly impact power loss at the maximum power point. One method is to separate losses into those affecting current, voltage and power. Losses are grouped into six categories: optical, voltage, recombination current, series resistance, shunt resistance and non-uniformity. As stated above, optical losses directly impact Jsc and are well defined using current metrics; they will not be further discussed here. The other five categories are discussed below.

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[2] A. Fahrenbruch, "A Practical Guide to Simulation", NCPV Team Meeting, NREL 30,31 January 2003.
[3] J. Sites, J. Pan, "Strategies to increase CdTe solar-cell voltage", Thin Solid Films 515 (2007) pp 6609-6102,
[4] N. Amin, K. Sopian, M. Konagai "Numerical modeling of CdS/CdTe and CdS/CdTe/ZnTe solar cells as a function of CdTe thickness", Solar Energy and Materials 91 (2007) pp 1202-1208.

5.4.1 Voltage

Voc as 2LM has many desirable attributes. Measurement is easy, fast, accurate and independent of series resistance effects. In fact its only perceived shortcoming is that it is not site-specific. As the zero order simulation for Voc is obtained by finding the zero current point on the curve obtained by subtracting Jph from the dark I-V curve, from the perspective of device analysis essentially any interface or region of the device can affect Voc.

a)

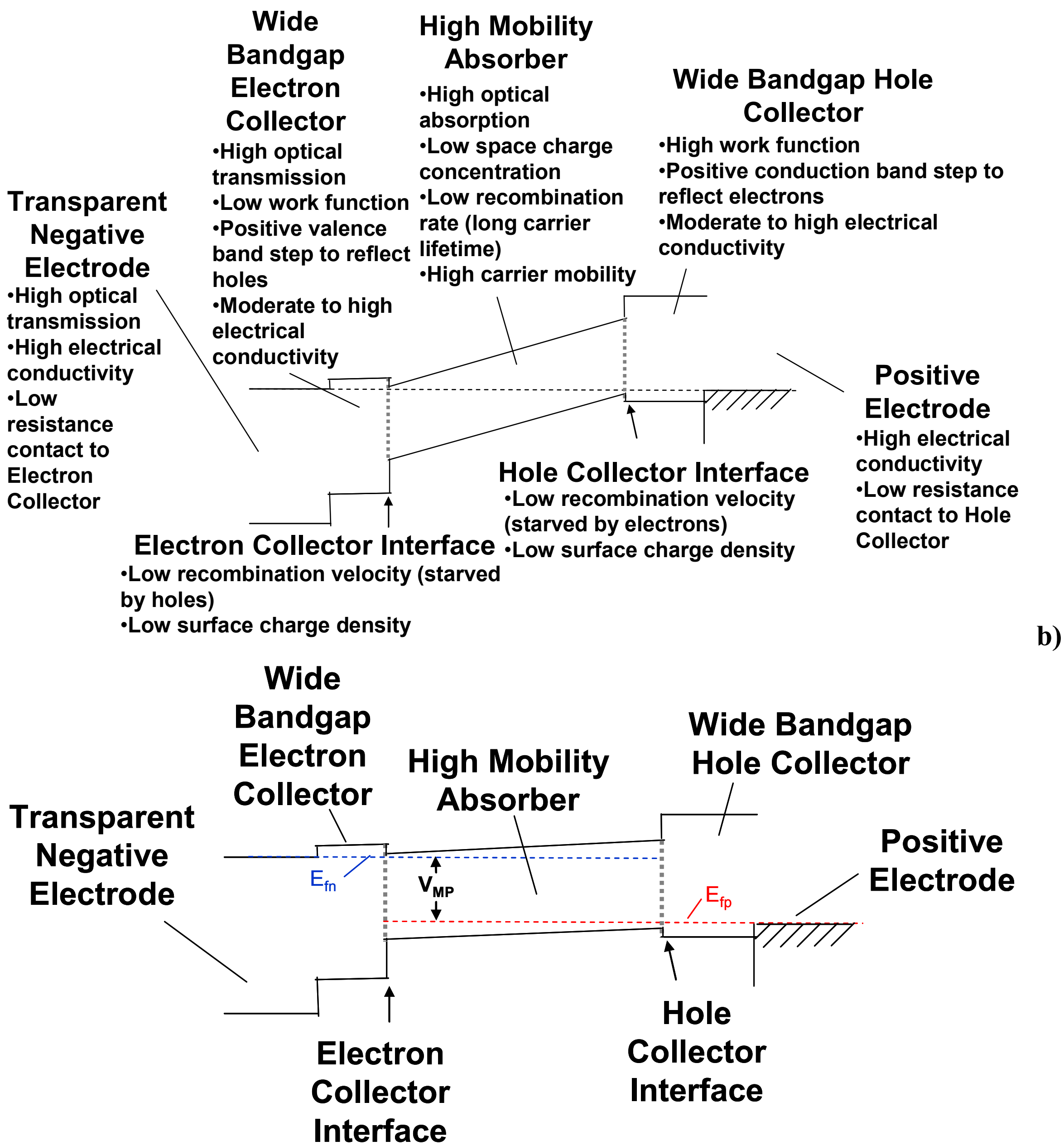

Figure 14: Idealized p-i-n structure conceptual band diagram – a) in the dark with zero bias and b) under illumination at maximum power point.

One nearly ideal reference voltage would be the voltage across the diode at which collection of electrons and holes are equal and therefore the photocurrent is zero. This voltage could be referred to as the intensity crossover voltage, $V_{\Phi X}$, because at this voltage increasing light intensity would not – at least to first order – affect the total current. With reference to the idealized band diagrams in Fig. 14, it is clear that at a forward bias voltage across the diode that is equal to the work function of the electron collector minus the work function of the hole collector, $(WF_{ec} – WF_{hc})/e$, that the conduction and valence bands in the CdTe would be flat. If the bands were flat and if the diffusion length of electrons and holes were equal, then $V_{\Phi X}$ would be equal to the flat band voltage. For this first order analysis we take $(WF_{ec} – WF_{hc})/e$ as the upper limit of $V_{\Phi X}$ and the theoretical upper limit of available voltage.

In practice the $V_{\Phi X}$ is reduced from $(WF_{ec} – WF_{hc})/e$ by fixed and dynamic space charges and by resistive losses. Thus although experimentally one might observe crossover by measuring IV curves with several values of neutral density filters, determination of $V_{\Phi X}$ is difficult because the forward current flowing at that bias point introduces an "IR" voltage, V_{IR}, that adds to the internal voltage and shifts the external voltage. Thus the measured crossover voltage would be $(WF_{ec} – WF_{hc})/e – V_{sc} + V_{IR}$, where V_{SC} designates voltage drop due to space charge. Measured crossover voltage, if it occurs, therefore does not appear to provide clear insight into $V_{\Phi X}$. Furthermore, using crossover voltage as a 2LM violates the principle that 2LM should be measured at Vmp.

Another approximation is that any voltage drop due to space charge reduces the voltage at Vmp by $V_{sc} = \iint \frac{Q_{sc}(x)}{\varepsilon} dxdx$. Space charge may originate from the bulk or at the interfaces and it may be trapped or dynamic where "dynamic" refers to space charge that exists due to the steady state separation between electron and hole quasi-Fermi levels that is in turn caused by illumination and external bias. Temperature could also impact V_{sc} through the temperature dependence of mobility and trap emission rates. From this perspective an effective voltage 2LM would measure the space charge distribution across the device at Vmp. Capacitance would seem to be the best measurement technique for quickly determining space charge. Ideally the C-V curve of a p-i-n device would be independent of bias, illumination and frequency, i.e., a flat line. In practice measurement of capacitance at high levels of forward bias is difficult due to the relatively high currents that flow in this voltage range. It would appear that even with their shortcomings that Voc and forward bias C-V are the most practical 2LM for voltage, even though their impact on site-specific power loss cannot be adequately quantified.

5.4.2 Recombination Current - "Electron Counting"

Once carriers have been created, the primary current loss is through recombination. Recombination current, Jrec, is considered to be composed of three components – $J_{r,b}$, $J_{r,eci}$, and $J_{r,hci}$, where b, eci and hci refer to bulk, electron collector interface and hole collector interface, respectively. Again, the relevant values of Jrec and its components would be those measured at Vmp. As of this writing researchers are considering several methods for measuring each component of recombination current including analysis of QE vs V and measurement of time-resolved photoluminescence, TRPL, from both the front and back.

5.4.3 Shunt Conductance

Shunting represents a second current loss mechanism and refers to current that flows between electrodes through an internal rather than external path. Measurement of the slope of the IV curve at zero bias provides a useful metric for shunts. In principle shunts could be due to distributed defects in the device, but in practice shunts are typically attributed to spatially-isolated defects in the film – e.g. attributed to scratches or scribing defects. If shunting is observed the location must typically be determined by optical inspection or by physically isolating the defective area.

5.4.3.1 Series Resistance

Resistive elements also result in an internal voltage drop. In this case the voltage drop is due to limited mobility or carrier concentration rather than to space charges. Resistive losses include resistance due to materials within the cell including bulk resistances and contract resistances, and including resistance in the electrodes, (e.g. TCO and metal) and in cell-to-cell interconnects. Series resistance due to the TCO and metallic electrodes can be measured independently and, as mentioned in section 4.3, temperature dependence of R_S can also provide insight into its origin. In the absence of reverse diodes, one may estimate series resistance, R_s, from a plot of $\frac{dV}{dJ} vs(J + Jsc)^{-1}$. Alternatively, Demtsu and Sites [5] predict the FF dependence on R_s using to the empirical relationship $FF_S = FF_0 * (1 - R/R_{ch})$ where R_{ch}=Voc/Jsc and $FF_0 = \frac{\upsilon_{OC} - \ln(\upsilon_{OC} + 0.72)}{\upsilon_{OC} + 1}$ and $\upsilon_{OC} = q * V_{OC}/(A * k * T)$. Thus one might estimate total series resistance by fitting FF vs Φ using R_S as a fitting parameter.

5.4.3.2 Micro-nonuniformity

Micro-nonuniformity losses are associated with lateral variations of electrical properties within a device. Due to the exponential dependence of current on voltage in diodes, low turn-on voltage, AKA "weak" diodes have an impact on device performance that is much greater than their relative area. Mapping of electroluminescence, photoluminescence, micro-light beam induced current, and electron beam induced current have all been used to document and quantify spatial micro-nonuniformity. Up to this point, however, the indicated measurements have not been used to quantify power loss and therefore to serve as effective 2LM.

5.5 2LM 3LM Summary

The 2LM proposed are admittedly more difficult to measure than are Voc and FF but on the other hand measurement is expected to be faster and more relevant than performing the complete battery of tests required to uniquely fit an IV curve. Perhaps the most serious shortcoming of the proposed 2LM, however, is their inability to accurately predict overall performance, i.e., unlike Jsc, FF and Voc whose product is power per unit area, the proposed 2LM do not predict overall device power conversion. Development of this alternative set of 2LM is a work in progress, thus the above discussion represents our current thinking on the subject rather than a definitive solution.

[5] S.H. Demtsu and J.R. Sites, "Quantification of Losses in thin-film CdS/CdTe Solar Cells", Proc. 31st IEEE PVSC (2005) p347-350.

On a programmatic level, during Phase I negotiations have taken place between personnel from First Solar and those of several members of the CdTe Team and it is hoped that during Phase II development of advanced 2LM can be accelerated through these collaborations.

6 DEFECT CHEMISTRY

6.1 Collaborative Activities

According to the plan laid out in the statement of work, tasks relating to defect chemistry were to be accomplished through collaboration with members of NREL's National CdTe R&D Team, but collaboration during Phase I was precluded by the failure of parties involved to agree on issues of intellectual property ownership and non-disclosure. In practice Phase I technical activity related to defect chemistry was limited to laying out the motivation and framing the key elements that need to be addressed.

6.2 Approach Toward Achieving 17% (or 20%) CdTe-Based Thin Film PV

A fundamental premise of this program is that the limits of CdTe PV device performance are directly tied to the materials science of the device. Thus the opportunity for improved performance relies on development of materials and device structures that optimize baseline field performance. In this section we discuss the premises that lay the groundwork for developing the knowledge of relevant defect chemistry that can support advanced device design, fabrication and processing.

6.2.1 Defect Chemistry Perspective on Polycrystalline CdTe

Thin film CdTe PV device properties are dominated by defects and interfaces. Edisonian optimization of polycrystalline thin film PV has led us to a device structure that works quite well because of (as opposed to "in spite of") grain boundaries[6]. The view that polycrystalline thin films are better suited to PV devices than are single crystals is supported by the fact that researchers have had much greater success with polycrystalline thin films than with single crystal materials. The "single crystal as an ideal" perspective persists , however, and this perception has significant impact on device optimization strategy. That is, perhaps because grain boundaries do not dominate recombination there is a tendency to view the grain boundary "problem" as having been "solved" which then enables researchers to move on to pursue optimization strategies that treat polycrystalline films as though they were more like the "ideal" single crystals. The quasi-single crystal approach is all the more appealing as we do not have readily available means for characterizing the electrical properties of grain boundaries.

We suggest, however, that the "single crystal ideal" perspective tends to misdirect optimization strategy. Table 2 lists several attributes of a PV device ranked by their relevance to device optimization; the left and right columns suggest rankings appropriate for single crystal and polycrystalline materials, respectively . Whether or not the suggested ranking are exactly correct, the point is that the key considerations involved in designing a device development program are different for polycrystalline thin films than they are for single crystal devices. Taking doping as an example, although substitutional doping does work on a local level in either system, in

[6] –Albeit with Voc ~150 meV below what we believe might be possible, i.e. the GaAs comparison.

polycrystalline materials doping is greatly complicated not only by "bulk" self-compensation but also by segregation of dopants at grain boundaries and interfaces. That is not to say that bulk doping is either irrelevant or futile, but rather to suggest that in the overall strategy one should increase emphasis on approaches that directly affect grain boundaries and interfaces. In this regard the lack of adequate means for quantitative characterization of grain boundary and interface properties is a severe impediment to progress. Experimental characterization and first principles modeling of grain boundary electrical, chemical and physical properties is an important component of any CdTe PV device optimization program.

Table 2. Selected attributes of a device that might be considered in the development of an approach for optimization of device performance. Each column contains the same list of attributes but with different "relevance" ranking order.

Relevance Ranking of Device Attributes (from highest to lowest)	
Single Crystal	**Polycrystalline**
pn junctions	p-i-n structure
initial efficiency as indicator of final efficiency	gb engineering
bulk defect density minimization	bulk defect density minimization
doping	interface passivation
frozen-in diffusion profiles	interdiffusion
interface passivation	miscibility gaps
lattice mismatch	hole reflector
hole reflector	electron reflector
interdiffusion	initial efficiency as indicator of final efficiency
p-i-n structure	doping
electron reflector	pn junctions
miscibility gaps	lattice mismatch
gb engineering	frozen-in diffusion profiles

6.2.2 Areas of Defect Chemistry in Need of Deeper Understanding

The electrical properties and role of grain boundaries are not fully understood. One model of device operation describes grain boundary diagrams as n-type valleys sandwiched by p-type hills.[7] A defect chemistry model consistent with the pnp grain boundary band diagram consists of Cd-rich boundaries (n-type) surrounded by sheets of V_{Cd}-rich CdTe (p-type).[8] An alternative model invokes p-type Cu_2O cladding of grain boundaries.[9] Whatever models are correct it would seem that a definitive understanding of the limits of CdTe PV device performance cannot be achieved without an understanding both of the electrical properties of the grain boundaries and interfaces and of the fundamental chemistry underlying those electrical properties.

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[7] e.g., L.M. Woods, D.H. Levi, V. Kaydanov, G.Y. Robinson and R.K. Ahrenkiel, "Electrical characterization of etched grain-boundary properties for as-processed px CdTe-based solar cells", NCPV Photovoltaics Program Review, eds. M. Al-Jassim, J.P. Thornton and J.M Gee, AIP CP 462 (1999) pp 499-504., see also Iris Visoly-Fisher, S. Cohen, A. Ruzin and David Cahen, "How Polycrystalline Device Can Outperform Single-Crystal Ones: Thin film CdTe/CdS Solar Cells", Advanced Materials 2004, 16, No. 11 June 4 pp879-883

[8] e.g. P.V. Meyers and S.P Albright, "Technical and economic opportunities for CdTe PV at the turn of the millennium", Prog. Photovolt. Res. Appl. 8 161-169 (2000) and references therein, see also J. Da Silvas, S. Wei, J. Zhou and X. Wu, "Stability and electronic structures of Cu_xTe", MRS, April 2007

[9] X. Liu and A. Compaan "Cu K-Edge X-ray Fine Structure Changes in CdTe with $CdCl_2$ Processing", EMRS, 2004.

Another aspect of relates to the 3D nature of polycrystalline films. SEM micrographs of real films indicate that grain boundaries are both perpendicular and parallel to the plane of the film, that some CdTe grains are completely surrounded by other CdTe grains, and that relatively few if any grains extend from the front to back surface of the film. Given the physical structure of the film the concept of p-type grains completely surrounded by n-type grain boundary surfaces would predict virtually no current collection – in sharp contrast with experimental data. It would seem that a device model including the impact of grain boundaries might have to be still more complicated in order to explain this apparent contradiction. For example, boundaries between two grains might have one type of electrical property and boundaries between three grains, i.e., triple points, might have another.

Defect chemistry of CdTe is further complicated by the interaction between defect chemistry and the electrical state of the device as indicated by the electron and hole quasi-Fermi levels. Unlike crystalline Si, for example, defects in CdTe that are formed at high temperature cannot be frozen in by rapid quenching to room temperature. In CdTe devices stability is achieved in the steady state conditions of illumination and voltage bias found in the field. Optimization of device structure and processing has produced modules that have demonstrated long term field performance and have been warranted for 25 years, nonetheless, we do not yet have a detailed understanding of why and how the defect chemistry and electrical properties depend upon conditions of illumination and bias.

Optimization of single crystal electronic material properties has benefited greatly from the "simple" model of dopants based on sp^3 orbitals; i.e., the suggestion that doping with low levels of impurities from columns to the left or right of the elements of the base material will result in p-type or n-type conductivity, respectively. To the best or our knowledge, no such simple defect chemistry models exist for polycrystalline CdTe. Determining the limits of CdTe PV device performance includes establishing a better understanding of defect chemistry and its impact on electrical properties and also requires development of a fundamental device model that includes the impact of specific electrical defects on device performance.

7 SUMMARY AND FUTURE WORK

7.1 Summary of Phase I Accomplishments

- During Phase I of the ETL program researchers evaluated a total of nine alternative device architectures – seven more than were called for in the SOW. Two front side and one backside structure displayed promise of improved Jsc and Voc, respectively.
- A champion cell was produced and delivered to NREL for efficiency confirmation. Efficiency achieved was 14.13% compared to the 15% milestone. Researchers believe that with further modifications to device architecture and optimized processing that Phase II and III efficiency goals of 16% and 17%, respectively, are within reach.
- Equipment for performing detailed device characterization was purchased and installed. Initial analytical procedures were developed and were applied to First Solar production line product.
- Researchers believe that evaluation and optimization of future devices could benefit greatly from an improved set of 2LM. An initial outline of the characteristic of an improved set of 2LM has been presented that more closely ties device characterization to electrical properties of specific areas of the device and does not rely on detailed modeling of device performance. Researchers are actively engaged in establishing effective collaborative agreements that both

protect First Solar IP and enable First Solar and other researchers to develop a better understanding of the 2LM required to establish the limits of CdTe PV device performance.

- Development of a better understanding of defect chemistry associated with polycrystalline CdTe PV had been expected to be carried out in coordination with members of the National CdTe R&D Team. This collaboration was precluded by failure of the parties involved to agree on issues related to non-disclosure and intellectual property ownership. Researchers have laid out a set of premises that frame the relevant defect chemistry issues relating to CdTe PV device performance.

7.2 Future Work

- Continued fabrication and evaluation of advanced cell architectures as described in the SOW in order to achieve the Phase II milestone of demonstrating a 16% efficient cell
- Development of device analysis emphasizing 2LM that are closely linked to a) photon counting, b) electron counting, c) space charge mapping, d) quantification of resistive losses, and e) micro-nonuniformity losses – all measurements to be evaluated at Vmp.
- Device physics simulations that can be used to validate fundamental interpretation of the role of material properties on device performance
- Chemical and physical materials analysis to determine the physical, electrical and chemical nature of grains, grain boundaries and interfaces. (e.g., STEM, LEAP, Auger, ESCA, SKμP, EXAFS)
- Application of accelerated stress test protocols that predict baseline field performance[10]
- Development of pathways that address practical obstacles to commercial manufacturing of advanced cell designs.
- Resolution of intellectual property issues with selected members of the CdTe Team and initiation of collaboration on projects relating to simulation of device performance and to modeling of defect chemistry
- Defect chemical modeling to describe relevant interface and grain boundary chemistries and the stability of those structures in the electrical and illumination conditions existing in the field.

[10] Development of accelerated stress test protocols is not a task of the ETL program, but researchers will employ available stress test protocols.

Appendix 1 Expanding the Limits Phase I Tasks, Milestones, Deliverables

Phase I Tasks

Task 1.1 Down select and develop deposition capability for fabrication of small area (1 cm^2) cells that incorporate an improved front side structure.

Task 1.2 Down select and develop deposition capability for fabrication of small area (1 cm^2) cells that incorporate an improved backside structure.

Task 1.3 Develop a materials chemistry model that identifies the relevant materials science and defect chemistry associated with the down selected device structures in Tasks 1.1 and 1.2.

Task 1.4 Optimize performance of devices incorporating improved front side structure down selected in Task 1.1.

Task 1.5 Optimize performance of devices incorporating improved backside structure down selected in Task 1.2.

Task 1.6 Down select and apply appropriate third level metrics for detailed analysis of device performance and specifically for determination of fundamental limits of device performance of device structures down selected in Tasks 1.1 and 1.2.

Task 1.7 Experimentally confirm the combined material chemistry and device physics models establishing limits on device performance of device structures down selected in Tasks 1.1 and 1.2.

Task 1.8 Down select and develop deposition capability for fabrication of small area (1 cm^2) cells that incorporate a second improved front side structure.

Task 1.9 Down select and develop deposition capability for fabrication of small area (1 cm^2) cells that incorporate a second improved backside structure.

Task 1.10 Develop a materials chemistry model that identifies the relevant materials science and defect chemistry associated with the down selected device structures in Tasks 1.8 and 1.9.

Milestones – Year 1

Month 12 Demonstrate 1 cm^2 15% cells

Deliverables – Year 1

The following deliverables shall be completed and delivered to NREL (in accordance with Section 6.0 below) by the dates indicated:

No.	Deliverable Description	Due Date
Phase I		
D.1.1	1st Quarterly Status Report	15 days after subcontract quarter
D.1.2	2nd Quarterly Status Report	15 days after subcontract quarter
D.1.3	3rd Quarterly Status Report	15 days after subcontract quarter
D.1.4	A journal and conference article	15 days after subcontract year
D.1.5	PV Program Contract Summary Report (if requested)	By December 15
D.1.6	Annual Technical Report	15 days after the subcontract year
D.1.7	15% Thin-Film CdTe solar cell	15 days after the subcontract year

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14. ABSTRACT *(Maximum 200 Words):* This report describes First Solar program researchers exploring radical materials integration concepts and dealt with the complexity of the various materials interactions. Once a suitable range for deposition of each exploratory material had been established devices were produced in order to determine what material or process interactions might exist that would directly impact the suitability of the advanced device concept to achieve unit process improvement. Preliminary evaluation of device performance has been completed on nine alternative CdTe PV device structures. Selected front side and back side structures were evaluated by light soaking as a means of obtaining a rough prediction of baseline field performance. Two front side and one back side structures exhibit improved Jsc and Voc, respectively, compared to First Solar's current Base device structure. The best confirmed cell efficiency was 14.13%. Optimization of combined front side and back side structures is not complete. Additional work was directed toward assessing the physical limits of polycrystalline PV device performance as imposed by device architecture and materials science.

15. SUBJECT TERMS
PV; cadmium telluride (CdTe); device structure; optimum power conversion; polycrystalline; micro-nonuniformity; module; post-stress efficiency; materials integration; back-side structure; front-side structure;

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