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Process Development for High V_{oc} CdTe Solar Cells

Phase I Annual Technical Report
October 2005 – September 2006

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University of South Florida
Tampa, Florida

Subcontract Report
NREL/SR-520-41525
April 2007

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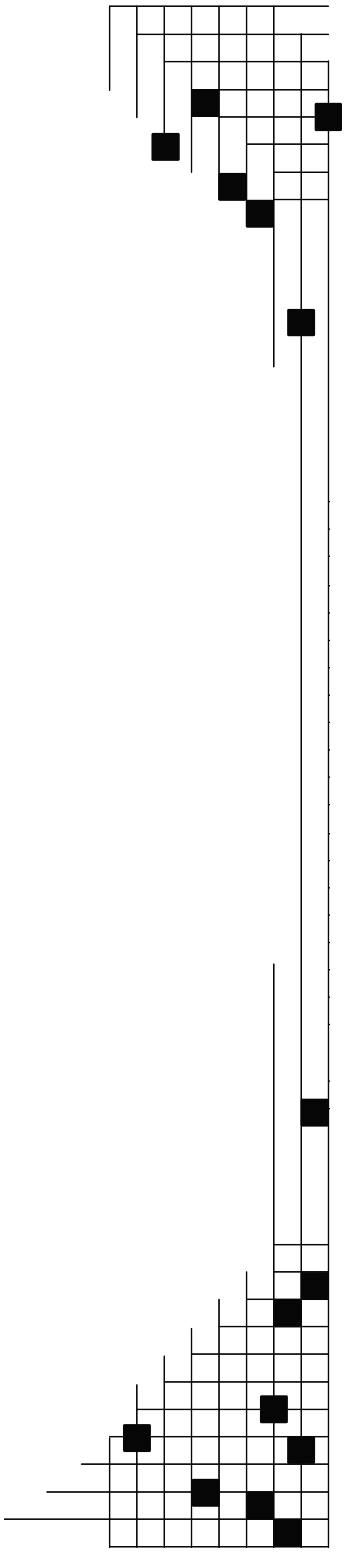

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1.0 INTRODUCTION

This is the Phase I report for this NREL funded project *(subcontract # NDJ-2-30630-18)*. The focus of the project is on the open-circuit voltage of the CdTe thin film solar cell. Although, CdTe continues to be one of the leading materials for large scale cost-effective production of photovoltaics, the efficiency of the CdTe solar cell has been stagnant for the last few years. At the manufacturing front, the CdTe technology is fast paced and moving forward with US-based First Solar LLC leading the world in CdTe module production. In order to support the industry efforts and continue the advancement of this technology it will be necessary to continue improvements in solar cell efficiency. A closer look at the present state of the art performance levels puts the three solar cell efficiency parameters, short-circuit current (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF) in the 24-26 mA/cm^2, 840-850 mV, and 74-76% ranges respectively. During the late 90's efforts to improve cell efficiency were primarily concerned with increasing J_{SC}, simply by utilizing thinner CdS window layers in order to enhance the blue response (<510 nm) of the CdTe cell. These efforts lead to the underscoring of the important role "buffers" (or high resistivity transparent films) play in CdTe cells [1-4]. The use of transparent bi-layers (low-ρ/high-ρ), as the front contact is becoming a "standard" feature of the CdTe cell.

Quantifying the losses in the typical CdTe superstrate structure reveals that J_{SC} has approached its practical limits, much more so than V_{OC} and FF, which is the reason that recently the CdTe community has been turning its attention to V_{OC} as the focus of efforts driven by higher efficiency goals [5].

2.0 OPEN-CIRCUIT VOLTAGE (VOC)

Improving V_{OC} in the typical CdTe/CdS p-n heterojunction solar cell is not straightforward as a practical matter, due to several reasons. The greatest challenge faced by CdTe researchers is the fact that the CdTe cell components (and fabrication processes) have significant interdependencies and cannot be decoupled. For example, copper (Cu) was initially believed to be a key element for the formation of the back contact, until studies of impurity distribution in CdTe/CdS solar cells indicated that this element accumulates at the junction interface, where it also impacts the device performance/characteristics [6,7,8]. Work at USF that focused on incorporating Cu at the interface and not at the back contact, suggested that some Cu concentration at the junction interface (and in CdS) is required in order to achieve high performance [7,9]. Another example of the interdependence between cell components and processing is the effect of the $CdCl_2$ heat treatment, or "activation" process (which is a standard fabrication step). This process is known to have three major effects on the CdTe solar cell: (a) CdTe grain enhancement; (b) enhanced interdiffusion between CdTe and CdS (that leads to the formation of a mixed $Cd_{1-X}S_XTe$ crystal at the junction interface); (c) defect passivation/lifetime improvement via the formation of Cl-related complexes in CdTe. The extent to which these changes take place depends on the fabrication history/properties of the CdTe/CdS structure. Grain enhancement is predominant in small grain (<1 μm approx.) CdTe films, with large grain films (>1 μm approx.) undergoing little or no grain growth. Interdiffusion in CdTe/CdS junctions, during the activation process, is typically less when these are deposited at high temperatures (>500°C typ.). Therefore, the process of improving the V_{OC} (and in general the performance) of CdTe cells is complicated by these interdependencies.

As already indicated above, the focus of this project is on the V_{OC} of the CdTe solar cell. Improving this parameter will require new materials, device configurations, and possibly advanced fabrication techniques. Moving V_{OC} beyond the present state-of-the-art 850 mV mark will require improvements/changes in one or more of the following: (a) recombination; it is

believed that recombination is the dominant transport mechanism at the junction, and therefore reducing the recombination levels (i.e. reducing J_O) could lead to higher V_{OC}; (b) doping levels; the magnitude of V_{OC} is related to the built-in potential of the junction, which is determined by the doping levels in the heterojunction partners. Therefore increasing the doping level (in particular in CdTe) could lead to higher V_{OC}'s; (c) back contact barrier; it has been shown via several modeling efforts that the back contact energy can also affect V_{OC}. Depending on the doping levels in CdTe, the band bending (and therefore V_{OC}) in this layer can be determined by the energy of the back contact. Therefore large work function contact materials could also lead to improved V_{OC}; (d) front contact/buffer: empirical evidence suggests that the front contact can also have a significant influence V_{OC}, and therefore alternative front contact materials (buffers) could also play a key role in improving this device parameter.

The main objective of this project is to develop materials/processes that will lead to the advancement of the open-circuit voltage of CdTe solar cells; the main areas to be investigated are: (a) impurities in the CdTe absorber: the focus in this case will be on controlling the net hole concentration in CdTe, the ultimate objective being to increase the doping in this layer and therefore the built-in voltage (and V_{OC}); (b) high-work function back contact materials; and (c) improved front contact: in this case the focus will be on investigating new buffer layers, as well as studying the effect of impurities in CdS.

3.0 SUMMARY OF FABRICATION PROCEDURES – EXPERIMENTAL METHODS

The main solar cell fabrication processes being utilized for this project are summarized in Table 1. The close-spaced sublimation (CSS) is being used for the deposition of all CdTe films. Although this process is well known for its high throughput (deposition rates over 1 μm/min are easily achievable), it is not very suitable for dopant incorporation; for this project (as it will be discussed later) an attempt was made to incorporate the dopant in the source material. Cadmium sulfide window layers are being deposited buy two methods: (a) chemical bath deposition (CBD), and (b) CSS. To-date no attempt has been made to incorporate a dopant during the CBD process (this is an option being considered for future activities); Indium is being used as as a dopant for CSS-CdS films.

As already discussed above, Cu is an important element used for the fabrication of CdTe solar cells. For certain tasks of this project Cu was eliminated from all solar cell fabrication steps, in order to decouple the role of the various impurities being studied.

It should also be noted that during the early stages of this project the baseline TCO material (i.e. CVD-SnO_2) was temporarily unavailable, due to the prohibitively high costs of the fluorine (F) doping source (Halocarbon 13B1 or bromotrifluormethane $CBrF_3$). Instead sputtered indium-tin oxide (ITO) and SnO_2 (undoped) were used as the front contact bi-layer (ITO/SnO_2).

Solar cells are characterized using standard techniques for light and dark current-voltage (J-V), spectral response (SR), and capacitance-voltage (C-V) characteristics. Materials characterization including x-ray diffraction spectroscopy, energy dispersive x-ray spectroscopy (EDS), and scanning electron microscopy (SEM) are also being carried out at USF. Secondary Ion Mass Spectroscopy (SIMS) and Auger analysis are being carried out in collaboration with NREL.

Table 1. Summary of processes and materials utilized for the fabrication of CdTe solar cells

	Materials	COMMENTS
Substr.	7059 Borosilicate Glass	Borosilicate glass cleaned in dilute HF solution (1:10) and rinsed with DI water
Transparent Contact	SnO_2:F	by MOCVD (Tetramethyltin, O_2, F-source: Halocarbon 13B1)
	ITO	by sputtering of In_2O_3:Sn @ T_{SUB}=300°C, or co-sputtering of In_2O_3 and SnO_2
Buffer Layer (high-ρ)	SnO_2	by MOCVD (as above; undoped)
	SnO_2	by sputtering of Sn (reactive) or SnO_2 targets
CdS		by: (a) Chemical Bath Deposition (CBD) and (b) Close-spaced sublimation (CSS); (5N)
CdTe	CdTe (5N)	by CSS
$CdCl_2$ HT	$CdCl_2$ (4N)	Direct application of $CdCl_2$ onto CdTe by evaporation followed by heat treatment
Back Contact	Graphite	(a) doped with HgTe:Cu; (b) undoped (used as received)
	Mo	by RF sputtering

4.0 FRONT AND BACK CONTACT MATERIALS

Among the main tasks of this project is the study of new materials for both the back and front contacts of the CdTe cell. During the first phase of this project TiO_2 – a material previously considered by the CdTe national Team – was studied and incorporated as a buffer in CdTe cells; titanium selenide ($TiSe_2$), a large work function material [10,11], was investigated as a back contact candidate. This section provides a description of the processing and material properties of these two materials.

4.1 Titanium Oxide (TiO_2)

Sputtering of a ceramic TiO_2 target in argon (Ar), and reactive sputtering of a metallic Ti target (in Ar/O_2 ambient) were used for the deposition of TiO_2 films. The substrate temperature was varied from RT to 300°C. In some cases N_2 was also added to the gas mixture. The electrical resistivity for all TiO_2 films was too high to measure with conventional (4-point probe) means. The film structural properties were studied using XRD and SEM. Figure 1 shows representative SEM images for films deposited under the three main process variations: (i) reactive sputtering from a Ti target (top), (ii) sputtering from a TiO_2 target (middle), and (iii) sputtering in the presence of N_2 (bottom) In all instances the apparent grain size ranges from 100-200 nm; however, the “grains” in films (i) and (ii) appear to be clusters of smaller particles, unlike film (iii) where the grains appear to be better developed; also film (iii) appears to be relatively more porous.

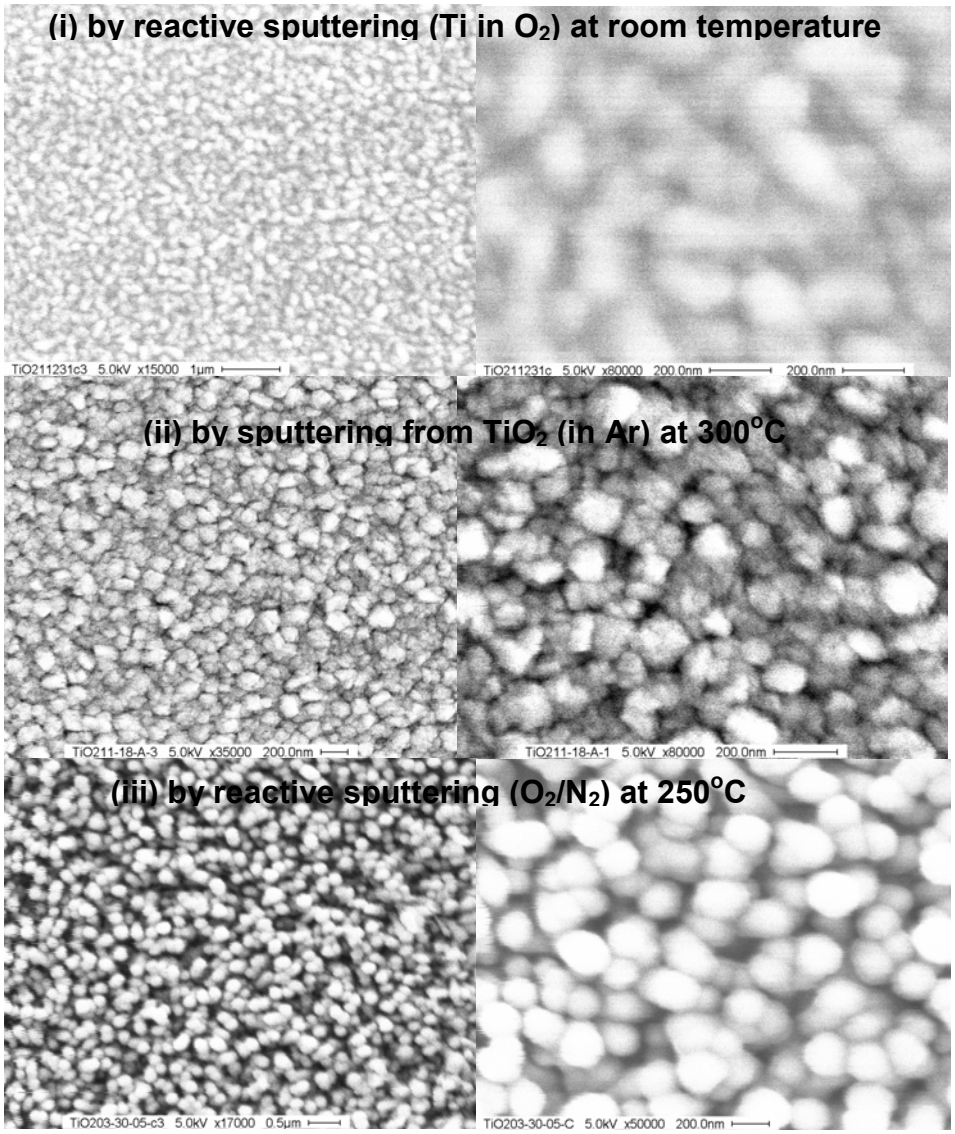

Figure 1. SEM Images of TiO_2 films deposited under different conditions: (i-top) reactive sputtering at room temperature; (ii-middle) sputtering from TiO_2 at 300°C; (iii-bottom) reactive sputtering in O_2/N_2. NOTE: the left image magnification varies for the three films; the right image magnification is the same (see scale at the bottom of each image).

X-ray diffraction analysis of TiO_2 films revealed that reactively-sputtered as-deposited at room temperature films (similar to film (i) in Fig.1), exhibited poor crystallinity – dark blue data in Fig. 2; the same was found to be true for films deposited at higher substrate temperatures from TiO_2 (similar to film (ii) in Fig. 1) not shown in Fig. 2. The cystallinity of these films appears to improve when they are heat-treated at high temperatures (over 600°C) in air – green and purple data in Fig. 2. The remaining film in Fig. 2 (orange data) was deposited with N_2 in the sputtering ambient at a substrate temperature of 250°C. Table 2 lists the peaks identified for the various films in Fig. 2. In all cases the films contained both TiO_2 phases (i.e. anatase and routile).

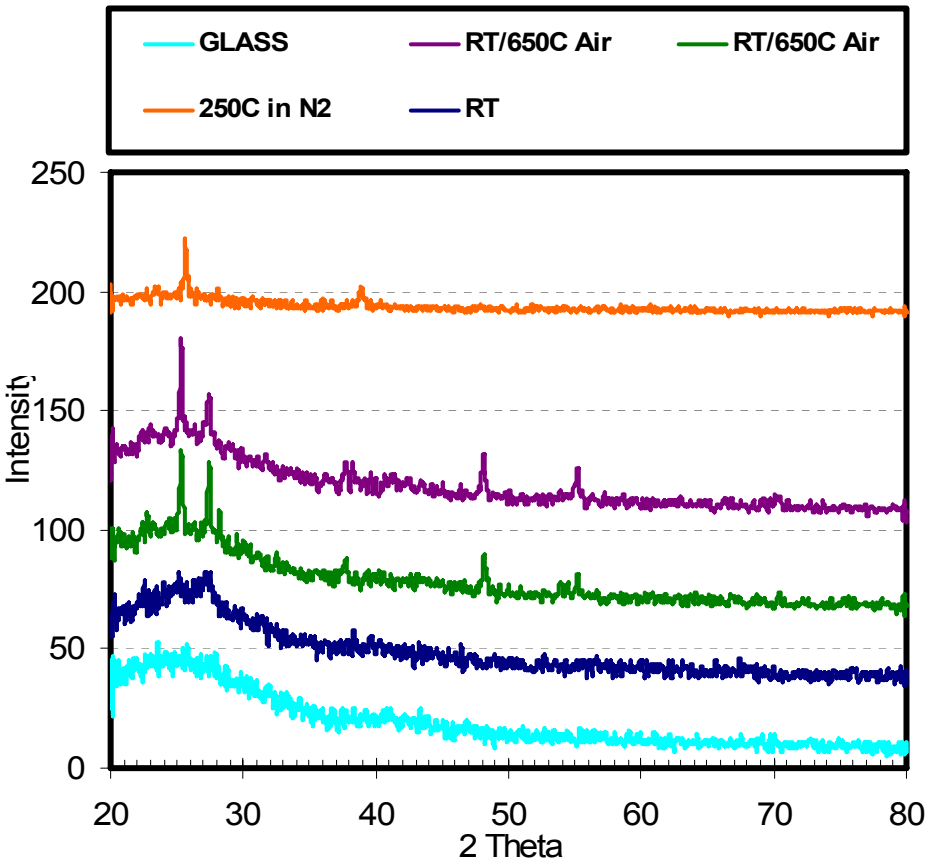

Figure 2. XRD spectra for TiO_2 films prepared under different processing conditions.

Table 2. XRD data for the TiO_2 films shown in Fig. 2; "A" and "R" in the ID column identify the Anatase and Rutile phases of TiO_2 respectively

Sample	2 Theta [°]	d-spacing [Å]	FWHM	Rel. Int. [%]	ID
T_{DEP}=RT	25.329	3.5164	0.2362	89.65	(101) A
Ann. 650°C/Air	27.422	3.2526	0.1181	100	(110) R
(green data)	48.179	1.8888	0.3149	38.26	(200) A
	54.593	1.6797	2.304	6.49	(211) A
T_{DEP}=RT	25.346	3.5141	0.1574	100	(101) A
Ann. 650°C/Air	27.343	3.2617	0.4723	45.44	(110) R
(purple data)	48.105	1.8915	0.2362	43.45	(200) A
	55.18	1.6632	0.576	24.81	(211) A
T_{DEP}=250°C (O_2&N_2)	25.626	3.4763	0.1181	100	(101) A
(orange data)	38.908	2.3148	0.4723	33.66	(200) R

4.1.1 Solar Cells with Titanium Oxide Buffer

The ultimate goal is to incorporate buffers such as the TiO_2 films discussed above, in solar cell structures and study their impact on solar cell performance.

The cell processing characteristics for the devices fabricated with TiO_2 buffers were:
Front contact:
CVD - SnO_2:F
TiO_2 by sputtering (process variations listed in table below)
CdS: by Chemical bath deposition (thickness: 90-100 nm)
CdTe: by the close-spaced sublimation (thickness: 5-6 μm)
$CdCl_2$-heat treatment @ 390°C
Back Contact:
Bromine/methanol (0.01% vol.) etch for7-10 secs
Doped graphite annealed @ 250°C[†]

Table 3 lists *the highest V_{OC}* values obtained for cells fabricated using TiO_2 as a buffer. In one of these instances where the cells were fabricated on TiO_2 sputtered with N_2 in the ambient a V_{OC} of 880 mV was measured (which is the highest V_{OC} measured during this project). Nevertheless, the overall cell behavior for these devices was very poor.

Table 3. The highest V_{OC} (for the identified deposition conditions) obtained for CdTe/CdS cells fabricated on TiO_2 buffer layers

TiO_2 Deposition Conditions					V_{OC} [mV]	FF Range [%]
Ar [mT]	N_2 [mT]	O_2 [mT]	T [°C]	Thickness [nm]		
4.5	1.5	-	180	30	***880***	5-25
4.5	1.5	-	180	10	840	8-27
4.5	1.5	-	180	20	790	13-22
1	-	4	250	30	780	10-12
-	-	5	250	30	820	7-9

[†] **These contacts contain Cu**

The light J-V characteristics of all TiO_2-based solar cells were very similar in all instances, with FF's always being less than 25%; an example is shown in Fig. 3. This J-V behavior suggests strong collection in reverse bias; however, near the zero volt bias point there is a collapse in J_{SC} (i.e. collection) which leads to the poor FF and poor overall cell performance. This could be caused by the high resistivty of TiO_2. If the cause for this collapse in collection is better understood and identified it is possible that TiO_2 buffers can provide a viable option for fabricating higher V_{OC} CdTe solar cells.

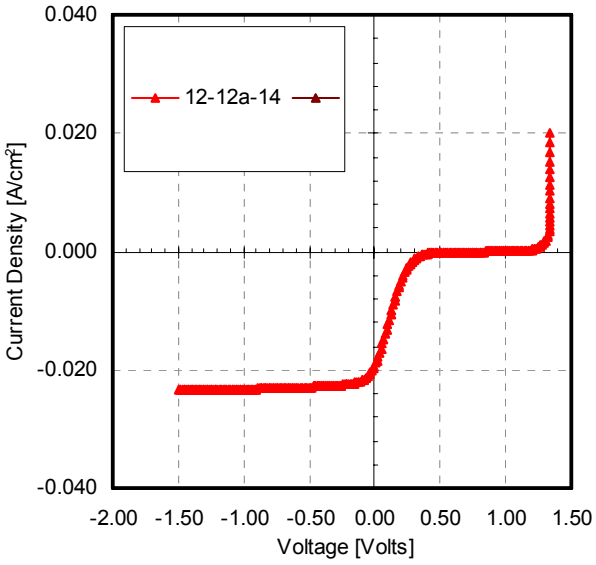

Figure 3. J-V characteristics of a CdTe cell fabricated with TiO_2 as a buffer layer

Although, some general trends were observed (i.e. as a function of TiO_2 processing conditions), the spread of the results (both V_{OC} and FF) was in most cases very large and no conclusions can be drawn at this time; only a few substrates exhibited uniform performance. This behavior points to the possibility that (non-uniform) micro-diodes are affecting the overall device performance A common behavior observed during this study is that within the same substrate (i.e. identically processed devices) increases in V_{OC} were accompanied with decreases in the FF.

Work on TiO_2 buffers has been suspended at the time this report was written. For future activities the possibility of doping TiO_2 in order to decrease its resistivity may have to be considered.

4.2 Titanium Selenide ($TiSe_2$)

As part of the task that addresses the characteristics of the back contact of the CdTe solar cell, this project focuses on the investigation of a promising class of materials, layered compound metals, which combine high chemical inertness with high work function and metallic conductivity. These promising properties make these materials good candidates for the back contact electrode. Chemical inertness is desired to limit chemical reactions at the interface with CdTe, and high work function is required to enable the formation of ohmic contacts (the CdTe layers are typically p-type, i.e. a hole injecting contact is needed). Potential layered compound candidates are the selenides $TiSe_2$, VSe_2, $NbSe_2$ and $TaSe_2$, as well as their corresponding sulfides.

Based on the existing deposition facilities the decision was made to first investigate $TiSe_2$ films; early efforts focused on preparing this compound by selenizing Ti. Metallic Ti films were sputtered deposited on glass slides to a thickness of 200-400 Å, and subsequently exposed to a Se flux under high vacuum conditions; the selenization process is carried out in a CIGS chamber which contains excess Se. It was found that the formation of $TiSe_2$ by this method depends on the substrate temperature. For temperatures below 400°C no $TiSe_2$ was detected. The Ti films appeared (to the naked eye) to change color at temperatures around 400°C. At selenization temperatures of 425°C the $TiSe_2$ phase was detected; this can be seen in Fig. 4 were the xrd spectrum of a Ti selenized film clearly shows diffraction peaks that have been found to correspond to $TiSe_2$. Table 4 lists the identified peaks and compares them to pdf data.

Table 4. XRD analysis for the film shown in Fig. 4

This work		PDF 01-083-0980 – $TiSe_2$		
2θ [º]	d-spacing [Å]	2 θ [º]	d-spacing [Å]	% Difference
14.646	6.0483	14.742	6.004	0.7%
29.6473	3.0133	23.138	3.06227	1.6%

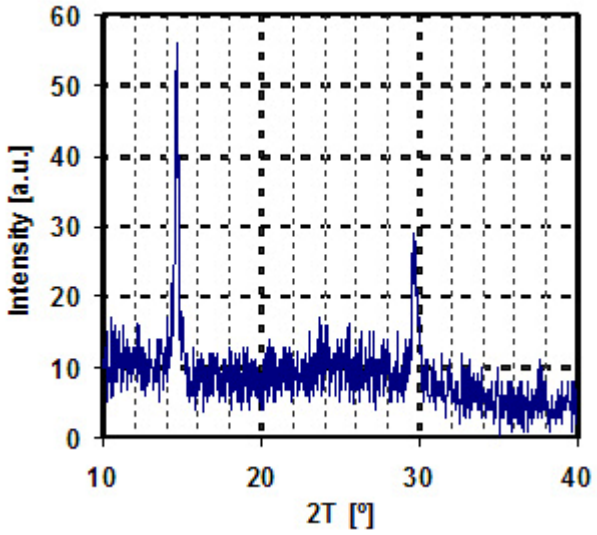

Figure 4. XRD spectrum of a selenized Ti film, showing the presence of the $TiSe_2$ phase

A major challenge faced with the use of $TiSe_2$ as a back contact material has been its formation onto the CdTe surface. Efforts to selenize Ti films deposited directly on CdTe have to-date failed due to the fact that the selenization conditions (elevated substrate temperature/high vacuum) cause the partial evaporation of CdTe. Although selenization of Ti is still being pursued, currently other material candidates and the possibility of depositing $TiSe_2$ by co-evaporation at lower temperatures are being considered.

5.0 THE EFFECT OF CdTe IMPURITIES ON SOLAR CELL PERFOMANCE

A considerable effort of this project is dedicated to incorporating impurities in CdTe in order to increase its net doping (hole) concentration and therefore the built-in junction potential and V_{OC} of the solar cells. During the first phase of this project several approaches have been considered in order to affect the doping characteristics of CdTe; these included: (a) incorporating phosphorous (P) in the CSS CdTe source material; (b) varying the gas ambient during the CSS-CdTe deposition (relative amounts of O_2 and N_2); (c) diffusion of antimony (Sb) into CdTe following the CdTe deposition by CSS. The following sections summarize the results obtained for each of these cases.

5.1 Phosphorous (P) Incorporation in the CdTe Source Material

This series of experiments was one of the first attempts (at USF) to dope CdTe during the CSS deposition. It must be noted that the CdTe films used for the fabrication of high efficiency cells (at USF) are deposited by CSS in the presence of oxygen (mixture of He and O_2); one of the

effects of the use of O_2 during the CSS deposition is more compact grains due to an apparent increase in the nucleation sites; in addition, O_2 is often found to enhance the p-type characteristics of CdTe.

In order to add P to the CdTe source material, powders of CdTe and Cd_2P_3 were mixed and sealed in an evacuated quartz ampoule. The relative amounts of the two powders corresponded to approximately 5% at. of P. The quartz ampoule was subsequently heated to temperatures up to 700°C. After approx. 48 hrs at this temperature the mixed powder was removed from the ampoule, re-pulverized and remixed. This powder (to be referred to as P-doped from this point forward) was then used to deposit "CdTe:P" films by CSS (all CSS depositions described in this section were carried out in an inert ambient - 100% He). The first few depositions resulted in unusually non-uniform films; the reason for the observed non-uniformities is not clear at this time, however, it is presumed to be due to inhomogenieties in the P-doped powder. In order to improve film uniformity the P-doped powder was used to deposit a thick CdTe film (approx. 300 µm) onto a glass substrate. This CdTe:P coated glass slide was then used as the source material for the CSS process; prior to using this source material for cell fabrication it was analyzed using EDS. The analysis indicated that 3% at. P was present, which is in relatively good agreement with the amount of P initially introduced in the CdTe powder (5% at.).

A series of CdTe films were deposited onto CdS/SnO_2(bilayer)/glass substrates for solar cell fabrication (CSS conditions: He-ambient; T_{SUB}=550°C; T_{SRC}=630°C). In order to decouple the effect of the impurities incorporated in the CdTe:P films, some cells were completed without the use of the $CdCl_2$ heat treatment, and all cells were fabricated with Mo back contacts (i.e. no Cu was used for the fabrication of the back contact).

The characteristics of the completed devices were in general very poor bringing into question the quality of the mixed powders; Figure 5 shows the V_{OC} and FF as a function of the processing conditions. The "best" devices from this group of cells were the ones fabricated using optimum (390°C) $CdCl_2$ conditions clearly indicating that the most critical processing step in this case is the $CdCl_2$ treatment, and therefore at this time it appears that "P-doping" is not having a beneficial effect on the device characteristics. EDS analysis of one of the CdTe:P films indicated that no P was present. This result does not necessarily suggest that P is not present at doping levels in CdTe (i.e. ppm), which is well below the detection limits of these technique. The tentative conclusion at this time is that P does not transport at the same rate as CdTe

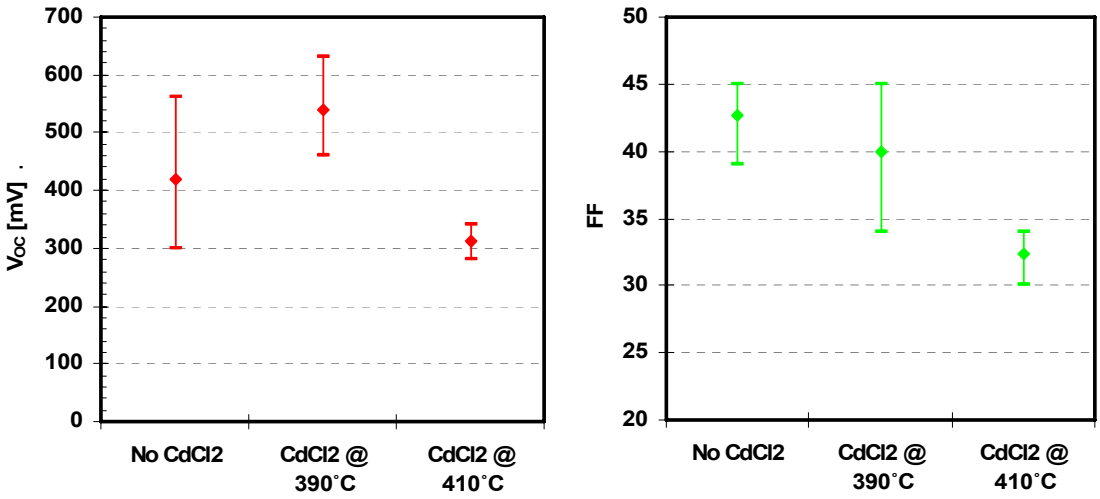

Figure 5. V_{OC} and FF for CdTe cells fabricated from a CdTe:P CSS source

during the CSS deposition process, and the CdTe source may be depleted of P after the first few depositions (possibly by the second or third deposition). Resolving this issue and determining whether any P has been incorporated in the films used for cell fabrication will require further investigation. A series of CdTe:P films has been forwarded to NREL for SIMS analysis.

5.2 The Effect of CSS(CdTe) Ambient

As indicated previously, the CdTe films utilized for the fabrication of high efficiency cells are deposited in an O_2-containing ambient (He/O_2). During the first year of this project the effect of a N_2-O_2 CSS ambient on the characteristics of CdTe cells was studied. All devices discussed here were fabricated using baseline fabrication conditions (CBD-CdS; Cu-doped graphite back contact; $CdCl_2$ heat treatment). The only intentional process variation was the composition of the gas mixture during the CSS-CdTe deposition: The total pressure was fixed at 10 torr, and the relative amounts of N_2 and O_2 were adjusted to result in the following N_2/O_2 ratios: 9/1, 7/3, 5/5, and 1/9. The performance of these devices (V_{OC} and FF) is shown in Fig. 6 (minimum of 3 cells per condition). These results show a clear trend of improving V_{OC}'s and FF with increasing O_2 (decreasing N_2) partial pressure.

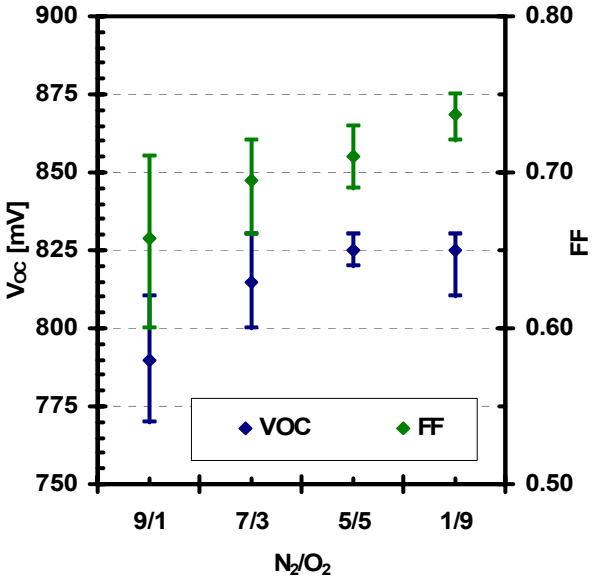

Figure 6. The effect of the CSS-CdTe deposition ambient on the V_{OC} and FF of CdTe solar cells

Dark J-V characteristics for representative devices are shown in Fig. 7. The Ln(J)-V shown on the left suggest that the device fabricated with CdTe with the lowest O_2 partial pressure has a higher dark current (J_O), which partially accounts for the lower V_{OC} and FF for the cells fabricated with a N_2/O_2 ratio of 9/1. However, the other three cells seem to have identical dark currents especially in the range of 0.5-0.75 volts (i.e. near V_{OC}). The dotted line in the same graph marks the J_{SC} magnitude, and assuming superposition it should cross the dark J-V at V_{OC}. Although series resistance effects interfere with the dark J-V characteristics around V_{OC}, all four J-V characteristics seem to be converging around the same value of V_{OC}.

The linear dark J-V shown in Fig. 7 (right) suggest that increasing amounts of O_2 during the CdTe growth lead to a considerable decrease in the forward dark currents beyond V_{OC} (the turn-on voltage of the J-V curve "shifts" to higher voltages). This behavior does not transfer to the light characteristics (i.e. no crossover), and it has been previously attributed to the properties of the CdS films (photoconductivity) and not the properties of CdTe. It is therefore possible that the O_2 used during the deposition of CdTe has an effect on the CdS, since the CdS is exposed to this ambient for approximately 2 minutes prior to the start of the CdTe deposition. The best performers in this group are cells with the largest shift in their dark J-V (i.e. lower forward current at voltages above 1.0 volt). This result seems to point that the observed device performance variations are due to the influence of the CdS and not CdTe, and seems to support a device model where CdS has insulating properties and the device behaves as an MIS structure [12].

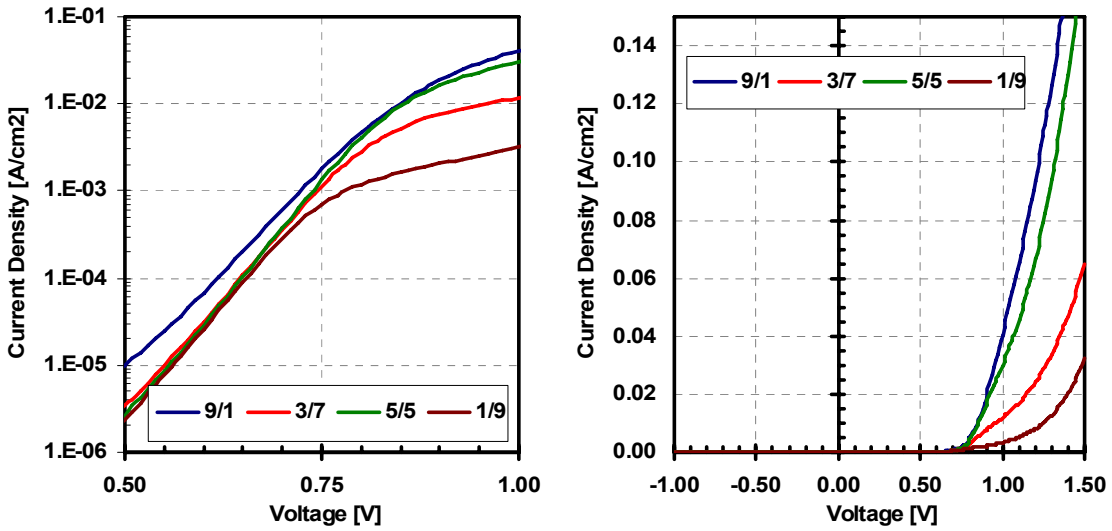

Figure 7. Dark J-V characteristics (left: ln(J)-V; right: J-V) for representative cells fabricated under various N_2/O_2 mixtures (total pressure 10 torr) during the CSS-CdTe deposition

The light J-V characteristics for the same cells are shown in Fig. 7. These suggest that the lower FF (and V_{OC}), for the device fabricated with a N_2/O_2 ratio of 9/1, is due to softening of the J-V curve around the maximum power point as a result of collection losses, and not due to shunting (shunt resistances calculated at a reverse bias of 1.5-2.0 Volts were very similar for all devices). This suggests that the use of O_2 during the CSS-deposition of CdTe affects the strength of the field in this layer (and therefore collection); at this time it is not clear whether the collection in CdTe is affected by O-incorporation in CdTe, or by the properties of the window layer (CdS), which as indicated above appears to be affected by the use of O_2 during the CdTe deposition.

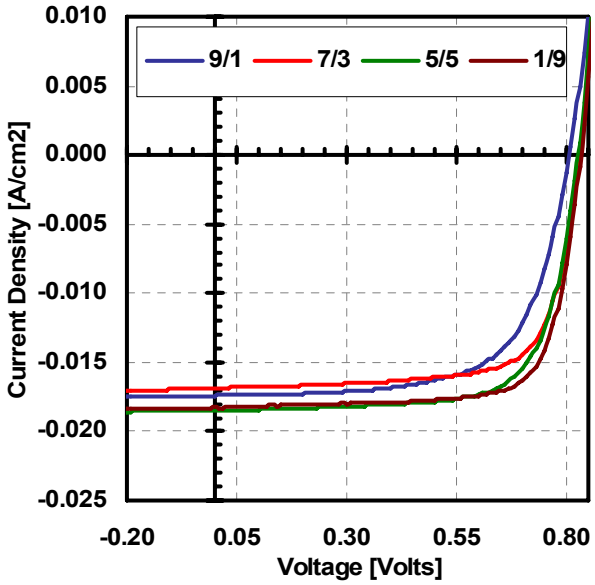

Figure 8. Light J-V characteristics of the CdTe cells of Fig. 6

The same devices (shown in Figs. 7 & 8) were characterized using C-V measurements. The values for the net hole concentration (N_A-N_D) and the depletion width were calculated from the linear portion of the [$1/C^2$ vs. V] graph and the capacitance at 0V bias respectively, and are listed in Table 5. All values for carrier concentration are well within the range typically observed for CdTe devices (i.e. low 10^{14} cm^{-2}). Nevertheless, there appears to be a slight (but consistent) increase in the net hole concentration as the O_2 partial pressure. As previously described (see Fig. 6) the V_{OC} also increased with O_2 partial pressure, by approximately 40-50 mV. To first order it appears that there is a correlation between the net hole concentration and V_{OC}; this evidence supports the claim that oxygen acts as a p-type dopant in CdTe. However, the increase in doping level is also accompanied by a decrease in the depletion width which would lead to poorer collection (and therefore lower FF), which is not the case for these cells.

Table 5. Net carrier concentration and depletion width for the cells shown in Figs 6 & 7

	N_2/O_2			
	9/1	7/3	5/5	1/9
N_A-N_D [cm^{-3}]	1.98 x 10^{14}	2.77 x 10^{14}	3.46 x 10^{14}	3.4 x 10^{14}
W_D @ 0 Volts [µm]	3.03	1.82	1.98	2.03

Even though a small increase in carrier concentration is observed, it seems that there a "saturation" level is reached for this device property. This is most likely associated with the nature of CdTe being a II-VI semiconductor, and the fact that self-compensation is often the limiting factor for achieving high doping levels in these materials. It is also evident that the effect of the CSS ambient (oxygen in particular) is rather complex, and based on these results it could be concluded that both the absorber (CdTe) and window layer (CdS) are affected by the presence of O_2 during the CdTe growth. The results clearly suggest that O_2 is beneficial to the CdTe cell, but fully understanding the role of O_2 will require additional studies.

5.3 Antimony (Sb) as a Potential Dopant for CdTe

Antimony (Sb) is another group V impurity which is being considered as a potential p-type dopant for CdTe. At this time it should also be noted that Sb_2Te_3 has been used as a back contact material to CdTe solar cells, and therefore it may play a dual role in CdTe i.e. as a dopant and also as a back contact electrode, if the processing conditions lead to the formation of the Sb_2Te_3 compound on the surface of CdTe. Following the results obtained with P, it was decided to attempt to incorporate Sb in CdTe via a post-deposition method, rather than during the CSS deposition. Following the CSS deposition of CdTe, a thin film of Sb (20-30 nm) was deposited onto CdTe by sputtering. The structures were subsequently heat treated in inert ambient, in order to cause Sb to diffuse into the CdTe film; annealing temperatures varied from 300 to 525°C, and annealing times from 20 to 160 mins. Some of the early experiments suggested that Sb was evaporating from the CdTe surface; in order to limit Sb loss during the heat treatment, an Sb-coated glass slide (with 200-300 nm of Sb) was used on top of the CdTe for the remainder of the experiments (see Fig. 9); all cells exposed to this process will be referred to as *CdTe:Sb* (or *Sb-doped*). In some instances the CdTe surface was etched in dilute HCl solution in order to remove any Sb remaining on the CdTe surface and eliminate any influence this may have on the formation of the back contact. It is well known that the fabrication process of high efficiency CdTe cells intentionally introduces several impurities in the solar cell, which include copper, chlorine and oxygen. The work described in this section was intended to investigate and understand the role of Sb as a potential p-type dopant. All cells fabricated to-date and discussed in this section were fabricated with CSS-CdTe films deposited in the presence of O_2 (see O_2 effect in a previous section), and the back contacts were fabricated using molybdenum (Mo) sputter-deposited at room temperature (no Cu was intentionally used during the cell fabrication process).

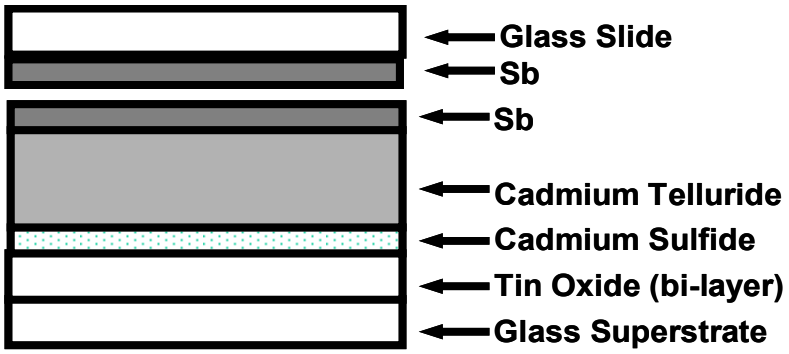

Figure 9. Sample arrangement used for the Sb diffusion experiments

5.3.1 The Need for the $CdCl_2$ Heat Treatment (HT)

The improvements in the performance of CdTe solar cells as a result of the $CdCl_2$ HT are well known. Initial experiments with CdTe:Sb focused on fabricating solar cells with and without the $CdCl_2$ HT, in order to determine whether going forward this step could be excluded from the cell fabrication process and therefore be able to decouple the effects of Sb from other impurities.

Table 6 lists processing conditions and solar cell performance for CdTe:Sb solar cells. These results are among several that clearly underscore the great importance of the $CdCl_2$ HT. The improvements in both the V_{OC} and the FF are substantial and in this case translate to an approximate increase in efficiency from a range of 6.5-7.2 to 11.0-11.3%; an increase of 4-5%. At this time it was decided that going forward with the Sb-doping work, the $CdCl_2$ HT should be included as part of the cell fabrication sequence, simply because its impact on solar cell performance could not be accomplished by other means. However, the intend is to include solar cells fabricated without the $CdCl_2$ HT in this study whenever necessary, in order to better understand the role of the various impurities and processes (see table 7 results).

Table 6. Process conditions and solar cell results for CdTe:Sb cells; the effect of the $CdCl_2$ HT

Sample ID	**"A"**	**"B"**	**"C"**	**"D"**
CdTe	In O_2 ambient; thickness 5-6 μm			
Sb Thickness on CdTe [nm]	20			
Heat Treatment (Sb Diffusion) T[°C]/time[min]	400/25	450/25	430/25	430/25
$CdCl_2$ HT	***None***	***None***	***Yes***	***Yes***
Contact	Sputtered Mo;			
V_{OC} [mV]	710-730	740-750	800-810	810-830
FF [%]	37-41	41-44	61	61-62

The improvements in performance (due to the $CdCl_2$ HT) are evident from the light J-V and spectral response (SR) data, for a representative set of cells, shown in Fig. 10. Although, the roll-over (slope around V_{OC}) behavior, indicative of the presence of a back contact barrier, is evident in all cells, it is more severe in the cells no t exposed to the $CdCl_2$ HT. Large enough barriers at the back contact could also result in losses in J_{SC}, which is also the case for the cells fabricated without the $CdCl_2$ HT.

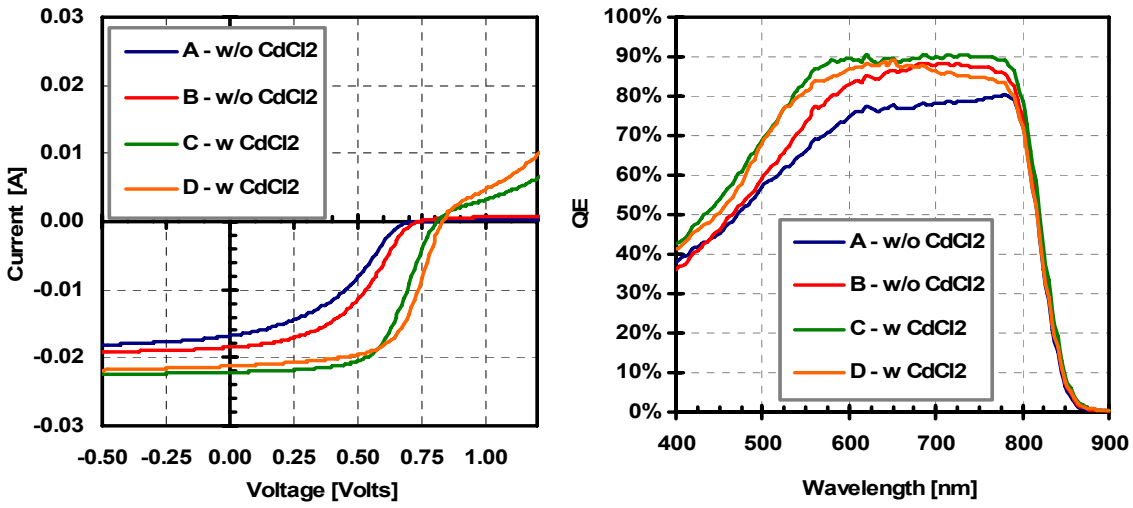

Figure 10. Light J-V (left) and SR data (right) for representative CdTe;Sb cells from table 6

5.3.2 The Effect of Excess "Surface-Sb"

The next set of cells listed in Table 7 are among those fabricated without the $CdCl_2$ HT, and in this particular case the objective was to determine whether excess Sb, left on the surface of CdTe after the diffusion-heat treatment, had an effect on the characteristics of the solar cells. In two of the cases listed in Table 7 the solar cells were etched in HCl following the Sb-diffusion process in order to remove excess Sb.

Solar cell performance is poor in all instances (compared to state-of-the-art cells); the reason for the poor performance is as indicated in the results presented above (table 6 & Fig 10) the exclusion of the $CdCl_2$ heat treatment. Figure 11 shows the light and dark I-V characteristics from representative devices. It is clear, based on the dark and light I-V roll-over, that the limiting mechanism in all cells is a large barrier at the back contact. However, cells etched with HCl (to remove excess Sb from the CdTe surface) exhibit consistently lower V_{OC}'s and J_{SC}'s, and their forward dark currents (beyond the junction turn-on voltage) are suppressed more severely. All these characteristics seem to suggest that the back contact barrier is larger in the case where excess Sb was removed (i.e. cells etched with HCl). It is therefore tentatively concluded that the presence of Sb at the surface of CdTe leads to a reduction in the back contact barrier. Antimony telluride (Sb_2Te_3) has been used by others as an effective back contact material for CdTe [13].

Table 7. Process conditions and performance data for CdTe:Sb cells; the effect of HCl etch

Sample ID	**"400/HCl"**	**"400/NO HCl"**	**"450/HCl"**	**"450/NO HCl"**
CdTe	In O_2 ambient; thickness 5-6 μm			
Sb Thickness on CdTe [nm]	20			
Heat Treatment (Sb Diffusion) T[°C]/time[min]	***400/25***	***400/25***	***450/25***	***450/25***
HCl Etch	***Yes***	***No***	***Yes***	***No***
$CdCl_2$ HT	None			
Contact	Sputtered Mo;			
V_{OC} [mV]	680-690	710-730	630-680	740-750
FF [%]	37-38	37-41	32-37	41-44

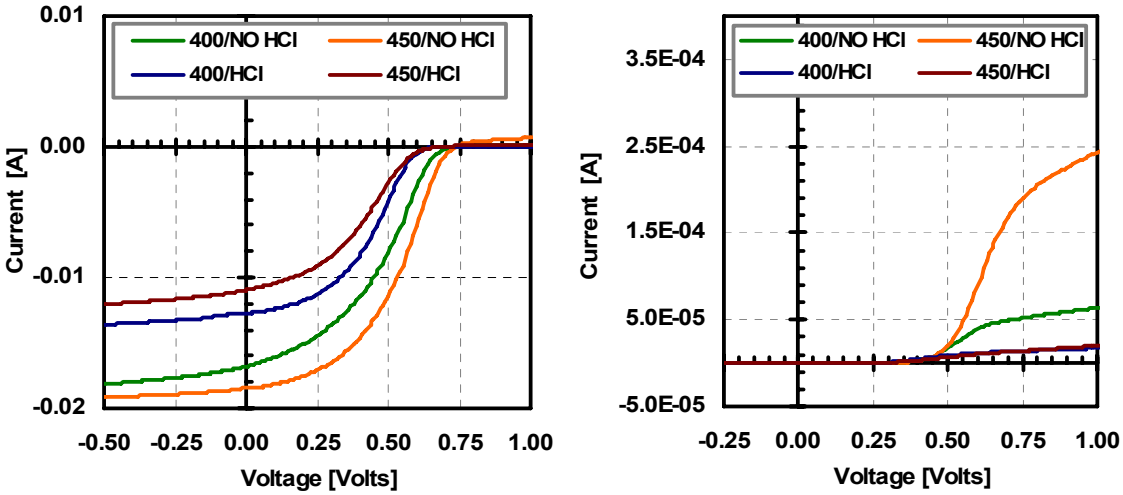

Figure 11. Light (left) and dark (right) I-V for representative CdTe cells from table 7

5.3.3 The Effect of the Sb-diffusion Process Parameters

A set of specific optimum conditions for the Sb-diffusion process has not been established yet; to-date the temperature has been varied from 400-525°C, the time from 20-180 mins, and the thickness of Sb deposited onto the CdTe surface from 20-50 nm; as indicated earlier an Sb-coated glass slide is also placed on the CdTe surface during the Sb-diffusion step.

Table 8 lists the performance data for CdTe:Sb cells for which the annealing time was varied from 40-160 mins. While the annealing time of 40 mins yields the lowest performance cells in this set, the annealing times of 80-160 mins result in essentially identical the V_{OC}'s and FF's.

Table 8. Process conditions and sola cell results for CdTe:Sb cells; the effect of annealing time

Sample ID	**"40"**	**"80"**	**"120"**	**"160"**
CdTe	In O_2 ambient; thickness 5-6 μm			
Sb Thickness on CdTe [nm]	30			
Heat Treatment (Sb Diffusion) T[°C]/time[min]	***400/40***	***400/80***	***450/120***	***450/160***
$CdCl_2$ HT	YES			
Contact	Sputtered Mo;			
V_{OC} [mV]	700-730	750-770	730-770	740-770
FF [%]	58-63	60-62	61-63	61-64

The light J-V for representative cells are shown in Fig. 12. The lowest performer in the group, the cell with the shortest Sb-annealing time, also seems to exhibit the "least" roll-over. It is not clear at this time what mechanism causes this behavior, however, it is possible that increased carrier concentration in the CdTe near the back contact for the cells annealed for long times (80-16 mins), results in increased band bending at that interface which will result in a larger barrier for holes (moving from CdTe to the contact). Resolving this issue will require numerical modeling that can consistently capture these differences in these devices. The doping profiles for the same cells are shown in Fig. 13, and they appear to partially support the increased doping claim; the lowest doping levels are observed in the device with the shortest annealing time.

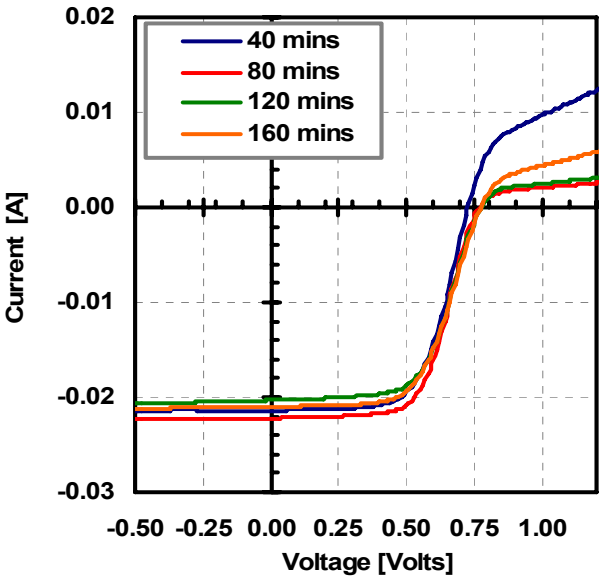

Figure 12. Light J-V for representative cells from table 8

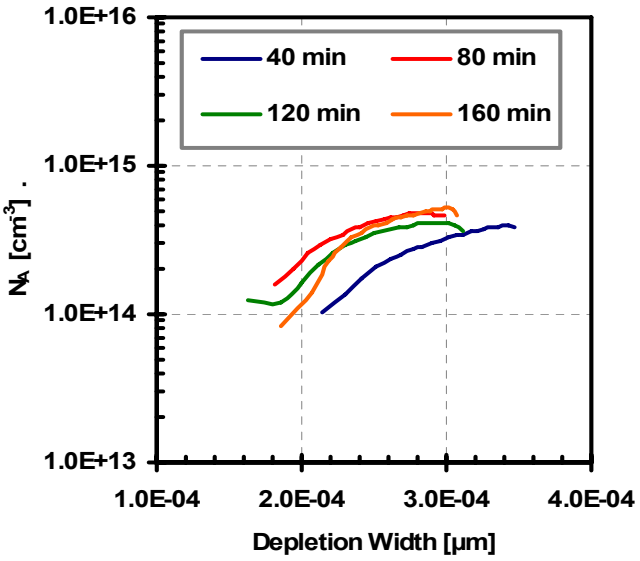

Figure 13. Doping profiles (from C-V measurements) for the cells shown in Fig. 12 (table 8)

Figure 12 shows the SR of several cells for which the Sb-diffusion time was fixed at 25 mins and the temperature was varied from 400-525°C. These data clearly demonstrates that at high annealing temperatures the collection of carriers decreases dramatically independent of the illumination wavelength. This type of behavior could be explained with increased interfacial recombination. Solar cell performance initially increased (up to 450°C); however, above 450°C the performance became "noisy" (i.e. increased scattering in performance data) and clearly decreased above 500°C. Based on these results the annealing temperatures were limited in the 400-450°C range for most experiments.

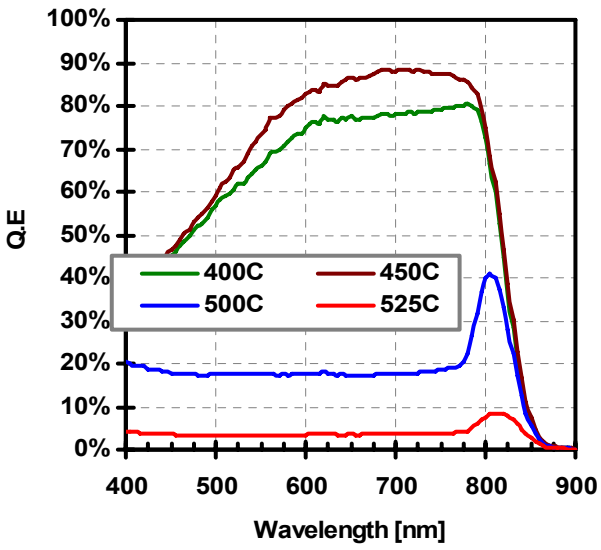

Figure 14. The SR of CdTe;Sb cells fabricated with different Sb-diffusion temperatures

Based on the to-date results with Sb-diffusion, it appears that effective doping of CdTe (i.e. $>10^{15}cm^{-3}$) is yet to be accomplished with this approach. Even though in several experiments there is consistent increase in the hole concentration, the doping levels measured are always within the general range typical of CdTe devices (fabricated w/o Sb) i.e. 10^{14} cm^{-3}. In general Sb may present a unique opportunity for CdTe devices, since it appears to potentially benefit the back contact region of the device (i.e. CdTe surface) as well as the bulk doping of CdTe. From a stability point of view, it may lead to the elimination of Cu from device processing, an element that is often suspected to be responsible for device degradation. Figure 15 shows light J-V characteristics and the CdTe doping profile for cells fabricated on the same substrate, in order to eliminate experimental variations/errors. The only processing difference between the two is that one of the devices was subjected to the Sb-diffusion process. It is clear that the both the V_{OC} and the doping levels in the CdTe:Sb device are higher (the V_{OC} by 50 mV), suggesting that increasing the doping in CdTe further could potentially yield even higher V_{OC}'s as expected.

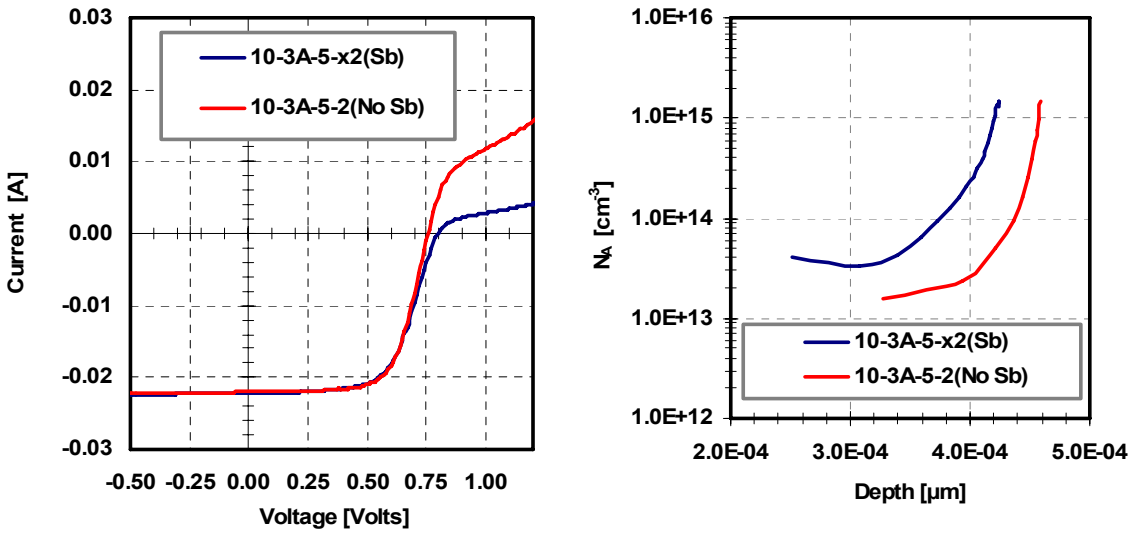

Figure15. Light J-V (left) and doping profile (right) of CdTe cells fabricated with and w/o Sb-diffusion

6.0 INDIUM (In) DOPED CdS

Another activity initiated during the first year of this project deals with using indium-doped CdS films for the fabrication of CdTe/CdS solar cells in order to determine whether increasing the n-type conductivity of CdS could be beneficial to solar cell performance. In theory, one would expect that an increase in the doping in either heterojunction partner to lead to an increase in the built-in potential and therefore V_{OC}. However, it has been previously found that a compensating impurity in this material, such as Cu, leads to improved performance. For this project In is being introduced in CdS in two ways: (a) by evaporating In onto CdS before or after the CdS deposition by CSS, and annealing it, and (b) by using an In-doped CSS-CdS source (purchased with In). At this time results are preliminary, but they seem to suggest that In-doping of CdS results in lower performance.

7.0 SIMS SAMPLES

In order to improve on our understanding of the role of the various impurities discussed in this report, a series of films have been forwarded to NREL for SIMS analysis (listed in table 9). These measurements could provide information on the concentration levels of the "dopants" in the various films, and whether these accumulate at any of the device interfaces, similar to what has been shown with Cu and Cl. Following the results of this set, it may be necessary to follow up with films that have been processed with the $CdCl_2$ heat treatment (following the introduction of the impurities listed below).

Table 9. Samples prepared at USF and being evaluated by SIMS at NREL

Sample #	Thicknesses	Comments
8-9A-2x	CdTe: 9.5 μm	Sb: 2 Å; CdTe(O) sample
8-9B-2x	CdTe: 7.9 μm	Sb: 5 Å, CdTe(O) sample
8-9B-3x	CdTe: 8.4 μm	Sb: 20 Å, CdTe(O) sample
2-24A-6x	CdTe: 4.2 μm	Sb: 2 Å, CdTe sample
2-24A-7x	CdTe: 4.3 μm	Sb: 5 Å, CdTe sample
2-24A-8x	CdTe: 4.2 μm	Sb: 20 Å, CdTe sample
8-10-1	CdTe: 9.6 μm	P doped CdTe film without contact
8-10-1x	CdTe: 9.6 μm	P doped CdTe, contacted with Mo
6-6b-12x	CdTe:7.08 μm, CdS : >1000 Å (approx.)	CdS:In (10 Å before CdS deposition)
6-6a-11	CdTe:4.8 μm, CdS : >1000 Å (approx.)	CdS:In (10 Å after CdS deposition)
8-13-1A	CdS	Source material CdS:In

REFERENCES

1. X. Wu, J. C. Keane, R. G. Dhere, C. DeHart, D. S. Albin, A. Duda, T. A. Gessert, S. Asher, D. H. Levi, P. Sheldon, "16.5%-Efficient CdS/**CdTe** Polycrystalline Thin-Film Solar Cell", Proc of 17th European PVSEC, (2001) pp. 531-534
2. X. Wu, S. Asher, D. H. Levi, D. E. King, Y. Yan, T. A. Gessert, and P. Sheldon, "Interdiffusion of CdS and Zn_2SnO_4 layers and its application in CdS/CdTe polycrystalline thin-film solar cells", Journal of Applied Physics, 89, 8, (2001), pp. 4564-4569
3. C. S. Ferekides, R. Mamazza, U. Balasubramanian, and D. L. Morel, "Transparent Conductors and Buffer Layers for CdTe Solar Cells", *Thin Solid Films*, 480-481, (2005) pp. 224-229
4. S. Gayam, S. Bapanapalli, H. Zhao, L. Nemani, D. L. Morel and C. S. Ferekides, "The Structural and Electrical Properties of Zn-Sn-O Buffer Layers and their Effect on CdTe Solar Cell Performance", *in print Journal of Thin Solid Films (2007)*
5. Gloeckler, M. Fahrenbruch, A.L. Sites, J.R., **"**Numerical modeling of CIGS and CdTe solar cells: setting the baseline", proc. 3rd WCPEC, (2003), pp. 491-494
6. K. Durose, S. Asher, W. Jaegermann, D. Levi, B. McCandless, W. Metzger, H. Moutihno, P, Paulson, C. Perkins, J. Sites, G. Teeter, and M. Terheggen, "Physical Characterization of thin film solar cells", Progress in Photovoltaics, 12, (2004), pp. 177-217
7. K. Barri, M. Jayabal, H. Zhao, D. L. Morel, S. Asher, J. W. Pankow, M. R. Young, and C. S. Ferekides, "Introduction of Cu in CdS and Its Effect on CdTe Solar Cells", Proc. of the *31st IEEE PVSC*, (2005), pp. 287-290
8. B. Tetali, V. Viswanathan, D. L. Morel and C. S. Ferekides, "Effects of Thermal Stressing on CdTe/CdS Solar Cells", presented at the 29th IEEE PVSC, New Orleans, LA, May 19-24, 2002.
9. S. Erra, C. Shivakumar, H. Zhao, K. Barri, D. L. Morel and C. S. Ferekides, "An Effective Method of Cu Incorporation in CdTe Solar Cells for Improved Stability", *in print Journal of Thin Solid Films (2007)*
10. D. Kraft, U. Weiler, Y. Tomm, A. Thissen, A. Klein and W. Jaegermann: "Alternative back contacts for CdTe solar cells: a photoemission study of the VSe_2/CdTe and $TiSe_2$/CdTe interface formation", Thin Solid Films 431 pp.382-386 (2003)
11. R. H. Friend, S. S. P. Parkin and D. Jerome: "The Transport-Properties of Vanadium-Doped Tise2 under Pressure", Journal of Physics C-Solid State Physics 15 (25), pp.L871-L874 (1982).
12. V. G. Karpov, Diana Shvydka, and Yann Roussillon, "Physics of CdTe Photovoltaics: from Front to Back", MRS Spring Meeting 2005, March 28 – April 1, San Francisco, CA
13. D. L. Bätzner, A. Romeo, H. Zogg, R. Wendt, A.N. Tiwari "Development of efficient and stable back contacts on CdTe/CdS solar cells" Thin Solid Films, 387, 1-2, (2001) pp. 151-154

LIST OF PUBLICATIONS ('06-'07)

1. "Surface science studies of Cu containing back contacts for CdTe solar cells", b. Spath, K. Lakus-Wollny, J. Fritsche, C. S. Ferekides, A. Klein, W. Jaegermann, *in print in Thin Solid Films (2007)*
2. "Photoluminescence studies of CdTe films and Junctions", S. Vatavu, H. Zhao, V. Padma, R. Rudaraju, D. L. Morel, P. Gaşin*, Iu. Caraman**and C. S. Ferekides*, in print Journal of Thin Solid Films (2007)*
3. "An Effective Method of Cu Incorporation in CdTe Solar Cells for Improved Stability", S. Erra, C. Shivakumar, H. Zhao, K. Barri, D. L. Morel and C. S. Ferekides, *in print Journal of Thin Solid Films (2007)*
4. "The Structural and Electrical Properties of Zn-Sn-O Buffer Layers and their Effect on CdTe Solar Cell Performance", S. Gayam, S. Bapanapalli, H. Zhao, L. Nemani, D. L. Morel and C. S. Ferekides, *in print Journal of Thin Solid Films (2007)*
5. "Development of $ZnSe_xTe_{1-x}$ p-type contacts for high efficiency tandem structures", S. Vakkalanka, C. S. Ferekides, and D. L. Morel, *in print Thin Solid Films (2006)*

NATIONAL TEAM MEETING PRESENTATIONS

"Stability Studies of CdTe Devices: Cu in Back Contact vs. Cu in CdS", CdTe Team Meeting, March, 2006, Golden, CO

"Fabrication perspective on open-circuit voltage in CdTe/CdS thin film solar cells", CdTe Team Meeting, March, 2006, Golden, CO, Brian McCandless and Chris Ferekides

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14. ABSTRACT *(Maximum 200 Words):* The focus of this project is the open-circuit voltage of the CdTe thin-film solar cell. CdTe continues to be one of the leading materials for large-scale cost-effective production of photovoltaics, but the efficiency of the CdTe solar cell has been stagnant for the last few years. At the manufacturing front, the CdTe technology is fast paced and moving forward with U.S.-based First Solar LLC leading the world in CdTe module production. To support the industry efforts and continue the advancement of this technology, it will be necessary to continue improvements in solar cell efficiency. A closer look at the state-of-the-art performance levels puts the three solar cell efficiency parameters of short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF) in the 24–26 mA/cm^2, 844–850 mV, and 74%–76% ranges respectively. During the late 1090s, efforts to improve cell efficiency were primarily concerned with increasing J_{SC}, simply by using thinner CdS window layers to enhance the blue response (<510 nm) of the CdTe cell. These efforts led to underscoring the important role “buffers” (or high-resistivity transparent films) play in CdTe cells. The use of transparent bi-layers (low-ρ/high-ρ) as the front contact is becoming a “standard” feature of the CdTe cell.

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PV; open-circuit voltage; thin film; solar cells; manufacturer; short-circuit current density; fill factor; high resistivity transparent films; cadmium telluride (CdTe); conversion efficiency; buffers; performance;

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