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Formation of ZnTe:Cu/Ti Contacts at High Temperature for CdS/CdTe Devices

Preprint

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Presented at the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion (WCPEC-4)
Waikoloa, Hawaii
May 7–12, 2006

Conference Paper
NREL/CP-520-39804
May 2006

NREL is operated by Midwest Research Institute • Battelle   Contract No. DE-AC36-99-GO10337

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FORMATION OF ZnTe:Cu/Ti CONTACTS AT HIGH TEMPERATURE FOR CdS/CdTe DEVICES*

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ABSTRACT

We study the performance of CdS/CdTe thin-film devices contacted with ZnTe:Cu/Ti of various thickness at a higher-than-optimum temperature of ~360°C. At this temperature, optimum device performance requires the same thickness of ZnTe:Cu as for similar contacts formed at a lower temperature of 320°C. C-V analysis indicates that a ZnTe:Cu layer thickness of <~0.5 µm does not yield the degree of CdTe net acceptor concentration necessary to reduce space charge width to its optimum value for n-p device operation. The thickest ZnTe:Cu layer investigated (1 µm) yields the highest CdTe net acceptor concentration, lowest value of J_o, and highest V_{oc}. However, performance is limited for this device by poor fill factor. We suggest poor fill factor is due to Cu-related acceptors compensating donors in CdS.

INTRODUCTION

An industry-compatible, high-performance, stable contact for CdTe-based thin-film photovoltaic devices remains an important goal for the CdTe community. Devices with fill factors of 77% have been demonstrated by incorporating a Cu-doped ZnTe contact interface layer between the CdTe absorber and a Ti outer metallization [1]. The interface formed between ion-beam milled CdTe (i.e., no Te layer) and ZnTe:Cu yields a valence band without discontinuity [2]. Because the uncompensated acceptor density (N_A-N_D) in the ZnTe:Cu is generally larger than that in CdTe, a detrimental back-contact barrier does not result, enabling low-resistance current transport at this interface. The high N_A-N_D of ZnTe:Cu, and beneficial reactions between ZnTe:Cu and Ti [3], yields transport at this interface dominated by low-resistance tunneling. For optimum processing conditions, these contact attributes combine to yield devices demonstrating nearly ideal behavior (i.e., light current-voltage [LIV] performance shows very little "crossover" or "rollover").

The high temperature used for ZnTe:Cu/Ti contact allows Cu to diffuse into the CdTe from the ZnTe:Cu. This diffusion can be used to increase N_A-N_D in the CdTe layer – transforming the junction from an n-i-p structure (i.e., CdTe is lightly p-type, the depletion layer [W_d] extends across entire CdTe layer, and device voltage depends on work function near back surface) into an n-p structure (i.e., CdTe is more p-type, W_d is engineered to enable maximum current collection, and device voltage is determined by CdTe N_A-N_D) [4]. Techniques to vary Cu diffusion have included controlling the contact deposition temperature while maintaining a "near optimum" ZnTe:Cu thickness of about 0.5 µm [1], or controlling the ZnTe:Cu thickness while maintaining a "near optimum" deposition temperature of about 320°C [5]. Combined compositional (secondary ion mass spectrometry, SIMS) and capacitance-voltage (C-V) analysis has shown that Cu diffusion from the ZnTe:Cu layer occurs at the same time that N_A-N_D increases in the CdTe, reducing W_d of the device. Optimum LIV performance for these ZnTe:Cu/Ti-contacted devices is attained when W_d is sufficiently narrow to produce a high drift field in the CdTe absorber but still wide enough to limit effects of voltage-dependent collection (i.e., photocarriers should not be generated outside of the depletion region when the device is biased at the maximum power point [MPP]) [6].

Higher-than-optimum Cu incorporation in the CdTe results in even higher values of N_A-N_D than for optimum devices, lower values of reverse saturation current (J_o), and (sometimes) higher V_{oc}. Unfortunately, excessive Cu diffusion also produces voltage-dependent collection (i.e., fill factor reduction) and generation of Cu-related photoconductive acceptor levels in the CdS. Although photoconductive CdS may not be, in itself, a detriment to PV device performance, compensation of CdS N_D by Cu acceptors may negate potential benefits of lower J_o.

The above results suggest that one pathway toward higher device performance is to control Cu diffusion so CdTe N_A-N_D increases, while CdS N_D-N_A is not reduced significantly. In this study, we investigate if advantageous Cu diffusion can result through higher-than-optimum contact temperature and smaller amounts of Cu. We find that this approach provides insight not only into the amount of Cu available for diffusion from the ZnTe:Cu, but clues into performance reduction when Cu enters the CdS.

EXPERIMENTAL

The CdS/CdTe material used in this study was produced by vapor-transport deposition (VTD) outside of NREL [5]. CdS and CdTe layers were ~0.3 and ~4.6 µm thick, respectively. The ZnTe:Cu/Ti contact was produced at NREL as follows: Samples were placed into a multi-source vacuum processing chamber and preheated for 120 min at 360°C. Prior to ZnTe:Cu deposition, ion-beam milling was performed with a 3-cm Kaufman-type ion gun, operating at a beam energy and current of 500 eV and 6

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mA, respectively, using UHP-grade Ar. ZnTe:Cu layers (~9 at.% Cu) were deposited by r.f. sputter deposition to thicknesses of 0.04, 0.1, 0.2, 0.5, and 1.0 µm. The sample heater was turned off following ZnTe:Cu deposition and allowed to cool to an indicated temperature of ~185°C, at which point 0.5 µm of Ti was deposited using d.c. magnetron sputtering. Following contact formation, a pattern of four individual 0.25-cm^2 cells were defined photolithographically on each sample. Cell definition was by two-step chemical etching, first using TFT Ti Etchant (Transene Co. Inc., Rowley, MA) to remove the Ti, followed by an aqueous solution of 39% $FeCl_3$ to remove the ZnTe:Cu and CdTe. A perimeter contact to the SnO_2 layer was formed with soldered In.

Electrical analysis included light and dark current-voltage (LIV/DIV) measurements at room temperature using an XT-10 solar simulator adjusted to approximate Global AM1.5 current from a CdS/CdTe reference cell. C-V measurements were performed in the dark using an HP 4274 LCR meter at a frequency of 100 kHz within a bias voltage range of –2.0 to +0.6 volts (i.e., forward bias to the approximate MPP voltage of the devices).

The same devices used for electrical analyses were also used for SIMS analysis following chemical removal of the Ti layer with the TFT etchant. SIMS was performed from the contacted side of the devices using a Cameca IMS-3F instrument tuned for a mass resolution (M/ΔM) of ~4000 to allow for separation of $^{63}Cu^+$ from $^{126}Te^{2+}$ species.

RESULTS AND DISCUSSION

Figure 1 shows quantified SIMS depth profiles of Cu for devices contacted with various thicknesses of ZnTe:Cu. The figure shows that, at 360°C, thicker ZnTe:Cu layers increases Cu concentration near the ZnTe:Cu/CdTe interface. However, the higher contact temperature (360°) does not diffuse significant Cu into the CdS layer (i.e., Cu concentration remains <10^{18} cm^{-3}) unless the ZnTe:Cu layer is also thick (i.e., 1.0 µm). This suggests that, for these thin contact layers with very low Cu availability, optimizing Cu incorporation into the CdTe and CdS layers cannot be accomplished by controlling contact temperature alone. Comparison of two SIMS profiles with nominally identical contact parameters (1.0 µm ZnTe:Cu, 360°C) reveals significant differences in Cu concentration in both the CdTe and CdS layers. These difference may be linked to the small difference seen in ZnTe:Cu layer thickness. This suggests that accurate control of the ZnTe:Cu layer thickness may be critical for reproducible device performance.

LIV analysis **(**Figure 2**)** indicates several significant observations: First, devices contacted at 360°C require the same thickness of ZnTe:Cu to produce optimum LIV performance as devices contacted at 320°C (i.e., 0.5 µm of ZnTe:Cu is about the optimum thickness at contact temperatures of ~320°C and ~360°C) [6]. Second, unlike previous studies, the V_{oc} for these devices continues to increase up to the maximum ZnTe:Cu thickness investigated of 1 µm. This is consistent with the above observation that less Cu is incorporated into the CdS than in previous studies, and **i**mplies that once a critical temperature is reached (>320°C) performance becomes very sensitive to small variations in ZnTe:Cu thickness. Third, although devices with the thickest ZnTe:Cu layer demonstrate the highest V_{oc}, these devices also demonstrate higher apparent series resistance, "rollover," and "crossover." Increased rollover and crossover are always seen for this contact process when the ZnTe:Cu provides excessive Cu into the device [6]. As will be discussed, we believe these effects are related to donor compensation by Cu acceptors in CdS [7]. Figure 3 shows dark I-V analysis of these devices, confirming systematic reduction of dark J_o with increased ZnTe:Cu thickness. V_{oc} of ~840 mV has been observed for devices that demonstrate short-circuit current densities (J_{sc}) of only ~19 mA cm^{-2}. This attests to the low effective value of J_o for these devices (note that the low J_{sc} is due to the ~0.3-µm-thick CdS layer and the specific type of TCO layer used in these production devices).

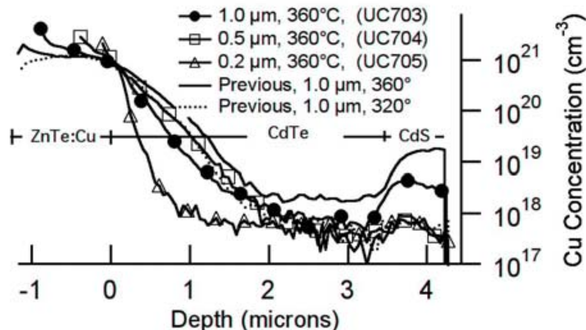

Figure 1. Quantified SIMS depth profiles of Cu concentration in CdTe/CdS devices for indicated contact temperature and ZnTe:Cu thickness. Analysis preformed from the ZnTe side.

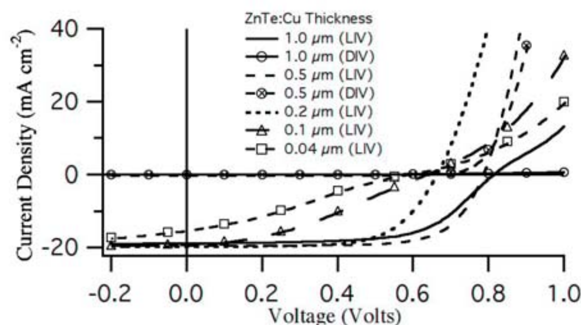

Figure 2. IV characteristics for CdS/CdTe/ZnTe:Cu/Ti devices contacted at 360°C as a function of the indicated ZnTe:Cu thickness. Note that although V_{oc} is highest for 1-µm ZnTe:Cu, optimum performance is achieved at 0.5 µm due to apparent series resistance for devices containing 1-µm ZnTe:Cu.

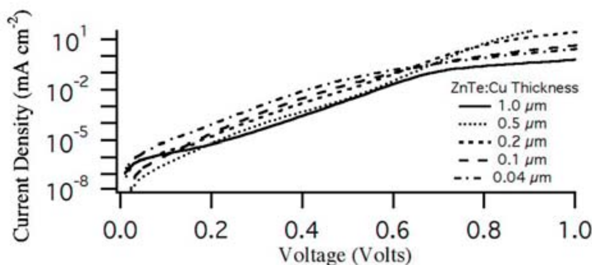

Figure 3. DIV analysis (ln J vs. V) illustrating that the J_o of these CdS/CdTe devices decreases systematically as the thickness of the ZnTe:Cu increases.

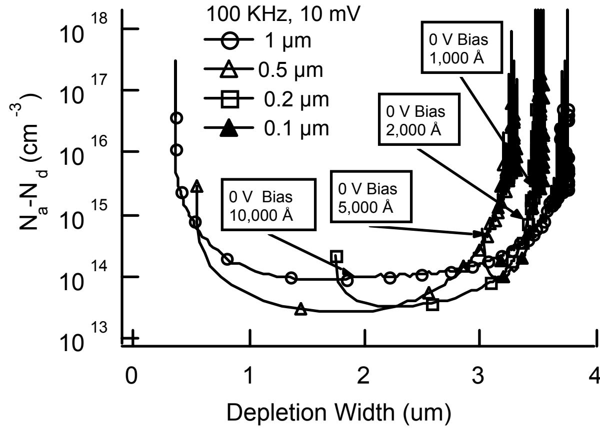

Figure 4. C-V analysis (Room Temperature, dark) for devices with indicated ZnTe:Cu thickness. Maximum forward voltage is 0.6 V. Location of W_{do} is indicated for each data set at location of arrow.

C-V analysis (Figure 4) illustrates how diffusion from the contacts formed at 360°C with various ZnTe:Cu thickness affects the electrical properties of the CdTe layer. Key points are: 1) The depletion width at both zero bias (W_{do}) and at the maximum forward bias (+0.6 V, W_{dMPP}) decreases systematically with increasing ZnTe:Cu thickness. This would be consistent with incorporation of Cu increasing the CdTe N_A-N_D. 2) Devices contacted with the thickest ZnTe:Cu layer (1 µm) produce the highest N_A-N_D values (~$1x10^{14}$ cm^{-3}) – consistent with indicated Cu concentrations shown Figure 1. The fact that the CdTe N_A-N_D is lower for this study than for the previous study [6] is also consistent with the data comparison shown in Figure 1. 3) Only the devices with ZnTe:Cu layer thicknesses of ~0.5 and 1 µm show a W_{dMPP} of ~0.5 µm or less. It is consistent with previous observations that only these devices demonstrate near- optimum performance.

The above results suggest the following: The ZnTe:Cu layer is a much more finite source of Cu for diffusion than was previously appreciated. Otherwise ZnTe:Cu layers thinner than 0.5 µm but deposited at 360°C should produce the CdTe N_A-N_D verses depth characteristics that would yield optimum device performance. Also, and as observed in previous work, increased Cu concentration in the CdTe yields higher CdTe N_A-N_D and lower dark J_o.

MODELING

Accurate interpretation of the type of C-V measurements presented in this study is problematic because the total device capacitance can be distributed among several depleted regions within the structure. These regions typically include the main junction and a region affected by a back-contact potential barrier [8]. To place the interpretation of these C-V measurements on a more solid foundation, the device-modeling program SCAPS-1D (Solar Cell Capacitance Simulator in One Dimension) has been used to simulate expected LIV/DIV/C-V behavior of simple two-layer CdS/CdTe structures [9]. For this simulation, only shallow donors in CdS, and shallow acceptors in CdTe, are assumed (i.e., deep defects are not considered). Absorption in a 0.3-µm thick CdS is simulated by an absorption coefficient (A) of 9e5 cm^{-1} $eV^{-0.5}$, and absorption in a 4.6-µm-thick CdTe layer is calculated using the absorption file provided with the program. Because the valance band at the CdTe/ZnTe:Cu is continuous, flat bands at the back contact are assumed. Other parameters are consistent with those provided with the SCAPS program. Although simplistic, results from this model provide useful insight for interpretation of LIV/DIV/C-V measurements.

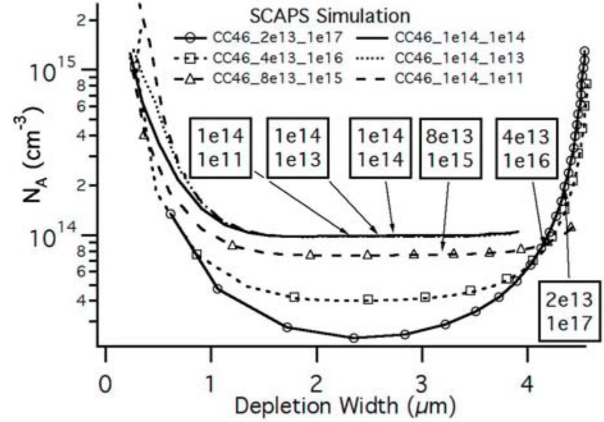

Figure 5. SCAPS simulated C-V characteristics. W_{do} indicated for each simulated curve by arrow. Top and bottom number in tag indicates the value of CdTe N_A and CdS N_D, respectively.

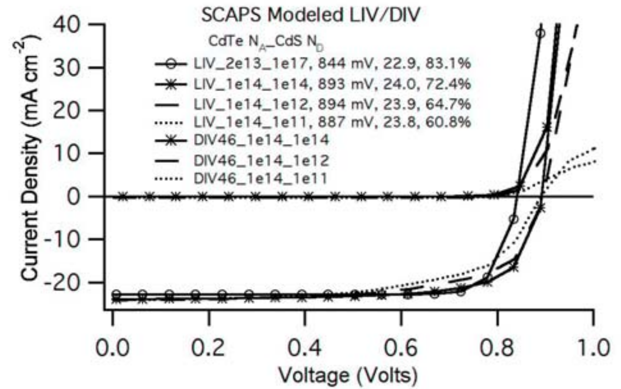

Figure 6. SCAPS simulated LIV/DIV. Left and right values in the tag indicate modeled values of CdTe N_A and CdS N_D, respectively.

Figure 5 shows that the simple SCAPS two-layer model simulates the general trends observed in the C-V measurements presented in Figure 4. We believe this supports the assumption of flat bands at the back of this contact structure [10]. Simulation of CdTe N_A levels between 1e13 cm^{-3} and 1e14 cm^{-3} reveals, for 4.6-µm-thick CdTe layers, N_A-N_D less than ~2e13 cm^{-3} will not be observed (i.e., for N_A values less than ~2e13 cm^{-3}, N_A vs. Width indicates the same minimum CdTe N_A value of ~2e13 cm^{-3}). As expected by charge neutrality, W_{do} narrows when the CdS N_D is decreased while N_A of the CdTe is increased. We believe an increase in CdTe N_A and reduction in CdS N_D occur simultaneously in actual devices, due to Cu diffusion in both of these layers during contacting. Figure 5 also shows that, if the CdTe N_A is fixed at 1e14 cm^{-3} while the CdS N_D is reduced from 1e14

cm^{-3} to 1e11 cm^{-3}, the simulated values of W_{do} even more closely approximate the W_{Dd} values observed in Figure 4. This may provide some insight regarding the amount of compensation that may be occurring in the CdS due to Cu diffusion. One observed artifact in Figure 4 that the present simulation has not reproduced is the extent of W_{dMPP} for the devices contacted with very thin layers of ZnTe:Cu (i.e., 0.04, 0.1 and 0.2 μm).

Figure 6 shows the simulated LIV/DIV curves produced using the same input parameters as used for the C-V results shown in Figure 5. This simulation reveals several artifacts that are consistent with actual data shown in Figure 2. First, as CdTe N_A increases from 2e13 cm^{-3} to 1e14 cm^{-3}, and CdS N_D decreases from 1e17 cm^{-3} to 1e12 cm^{-3}, the V_{oc} of the device increases. Although the absolute value of initial and final V_{oc} remains ~50 mV higher than observed in actual devices, the trend and the amount of V_{oc} increase is consistent for devices contacted with 0.5 μm of ZnTe:Cu compared to devices contacted with 1.0 μm of ZnTe:Cu. Second, for the highest simulated CdTe N_A (1e14 cm^{-3}, and lowest CdS N_D (1e11 cm^{-3}), the V_{oc} begins to decrease. This may suggest the mechanism of V_{oc} reduction observed in actual devices with excessive Cu diffusion [6]. Third, for the highest modeled CdTe N_A (1e14 cm^{-3}), effects of voltage-dependent collection (dJ/dV) are observed increasingly as the CdS N_D is reduced. dJ/dV manifests primarily by a reduced fill factor, and is due to light being absorbed outside of a depleted region that is becoming too narrow. As N_D is reduced, the depletion region becomes narrower because charge neutrality requires the decreasing CdS N_D must be balanced by decreasing W_d on the CdTe side. Fourth, for the highest CdTe N_A (1e14 cm^{-3}), and two lowest values of CdS N_D (i.e., 1e12 cm^{-3} and 1e11 cm^{-3}), the modeled device demonstrates increased series resistance in both the dark and light. This is especially obvious in the case of CdS N_D = 1e11 cm^{-3} where rollover and crossover is observed in the LIV/DIV performance. This modeled increased resistance is consistent with that observed in the data shown in Figure 2 for the device contacted with 1 μm of ZnTe:Cu. The cause of this increased resistance is believed to be due to Cu-related acceptors in CdS compensating intrinsic donors. This reduces the CdS N_D-N_A, thereby moving the Fermi level away from the conduction band when the device is placed in forward bias. This produces a hump in the CdS conduction band that acts as a barrier to majority electrons drifting from the CdTe absorber (producing reduced fill factor) and as a barrier to electrons injected into the CdTe layer (producing 1st-quadrant rollover). [7]

CONCLUSIONS

This study has shown that a higher contact temperature cannot easily be used to offset insufficient Cu availability from a thin ZnTe:Cu contact layer when forming a CdS/CdTe device. Specifically, the amount of Cu that can diffuse from a ZnTe:Cu contact during high-temperature ZnTe:Cu contacting is more finite than expected. This insight may help explain why sample sets produced at different times (but using the same nominal contact parameters) can yield different values of CdTe N_A-N_D. In these cases, small differences in ZnTe:Cu thickness (or Cu content in the ZnTe:Cu) might be expected to have a more significant effect on CdTe N_A-N_D than similar small changes in contact temperature. The ability of thin ZnTe:Cu layers limit Cu diffusion at high contact temperature may also provide insight into the relative stability of devices produced with the ZnTe:Cu contact.

This study also supports early observations that excessive Cu diffusion can lead to reduction of fill factor due to the formation of a W_d that is too narrow for optimum current collection (i.e., dJ/dV effects). However, a more significant fill-factor limitation may be due to Cu-related acceptors compensating CdS donors when Cu diffusion is excessive. SCAPS-1D simulations reveal that increased apparent series resistance results when excessive donor compensation in CdS is assumed. Because the onset of photoconductivity in CdS by Cu produces a distinctive signal in red-light bias (apparent) quantum efficiency, [11] monitoring for detrimental donor compensation in CdS should be possible – even in a production environment. The study also suggests that performance improvement may result if processes can be identified that allow for more Cu incorporation into the CdTe layer, while maintaining a high CdS N_D-N_A.

ACKNOWLEDGEMENTS

The authors wish to thank A. Fahrenbruch for insight and thoughtful discussions regarding CdS/CdTe device performance simulations. This work is supported or funded under DOE Contract No. DE-AC36-99GO19337.

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