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Design and Test of a Variable Speed Wind Turbine System Employing a Direct Drive Axial Flux Synchronous Generator

October 29, 2002 — December 31, 2005

T.A. Lipo and P. Tenca
University of Wisconsin
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NREL Technical Monitor: A. Laxson

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This publication received minimal editorial review at NREL

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Subject of the Research Project

The goal of this funded research project is the definition, analytical investigation, modeling, and prototype realization of a current-source conversion topology tailored to high-power wind turbines. The important features that such a topology should possess for a wind turbine application can be summarized by the following points:

1. The converter must be capable of delivering power grid line current whose fundamental power factor, defined with respect to the corresponding phase voltages, is capable of being controlled. It is usually desirable to control the power factor at unity, but on occasion it may be desirable to generate reactive power of either polarity.

2. The harmonic content of the grid line current must be reduced to a reasonable value. (The desired goal is defined by the IEEE 519-1992 standards.)

3. The efficiency of the overall conversion chain—including the generator—is very important because it is desirable to extract as much energy as possible from the "free" wind.

4. The wind turbine generator usually costs at least several times more than the converter, which, in turn, represents about 10% of the wind turbine total cost. This means that a significant increase in converter cost can be justified if the proposed topology can significantly reduce the generator cost.

5. Failures in the conversion chain contribute to about one third of the total turbine maintenance costs during its lifetime. Consequently it is important to use a reliable topology that is highly fault-tolerant and redundant in case of component failure.

6. The points from 3 to 5 above are even more significant for high-power turbines, while point 2 can eventually be relaxed at such power levels because several turbines present in a large wind farm can be interconnected using appropriate transformers in a manner capable of reducing the harmonics at the interconnection point of the wind farm and the grid.

All these considerations have been evaluated together and have led the investigators to define the conversion concept illustrated in Figure 1, where the square boxes identify topological structures organized into common three-phase bridges. The topology is based on a current-source concept whose intrinsic nature exploits the distance between the generator and the power grid characterizing the wind turbines to realize either a portion or even all of the necessary DC-link inductance. Only two cables are needed between the nacelle and ground, and only the two most reliable modules (diode bridge and generator) are located in the nacelle, thereby reducing the weight of the nacelle and the overall maintenance costs. The average power is converted entirely by the two series-connected, current-source inverters 1 and 2 employing fully controllable switches with bidirectional voltage blocking capability. Nevertheless, it must be highlighted that one of the bridges can use thyristors in several applications where a reduced range (including unity) for the grid fundamental power factor is sufficient, thereby reducing the overall cost of the system.
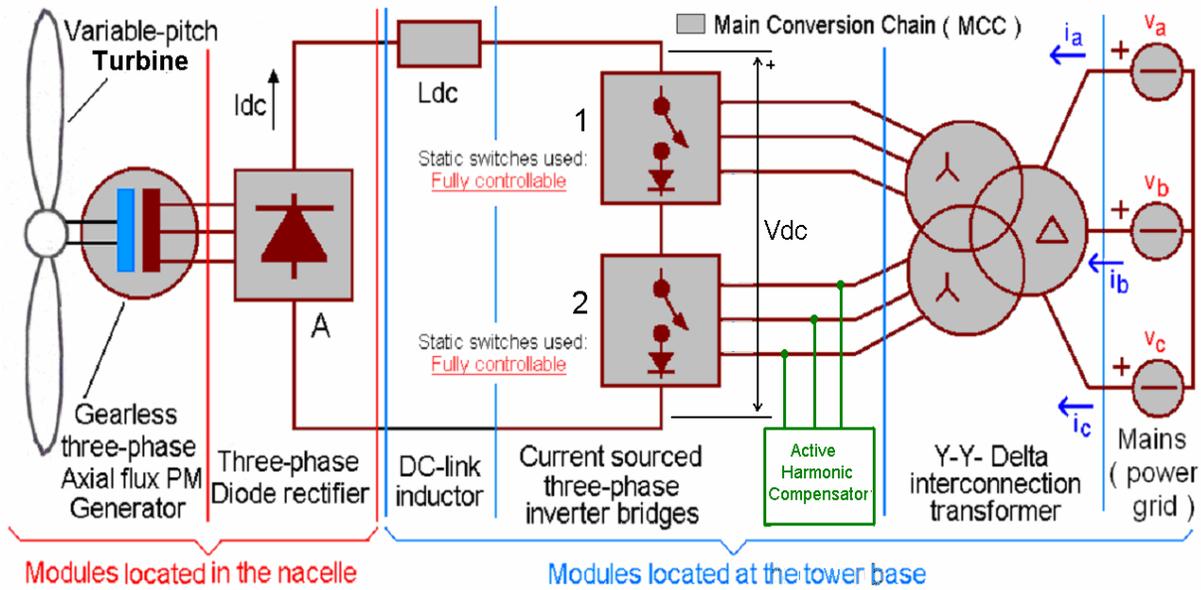
Figure 1. Current source topology for wind turbines highlighting the structure of the interconnect with the grid

The topology shown in Figure 1 is especially tailored for high-power wind turbines, but the inverter-side solution, used for the interconnection with the grid, can be employed in various other high-power applications. Inverters 1 and 2 have the usual topological structure of a three-phase bridge, and they are switched at line frequency, explicitly avoiding pulse-width modulation (PWM), thereby reducing switching losses and allowing the use of high-power but relatively slow devices such as gate turn off thyristors (GTOs) or integrated gate-commutated thyristors (IGCTs). As consequence of this choice, the efficiency of the main conversion chain (Generator – diode bridge – two current-source converters in series) is improved. A significant part of the project has been focused on the power quality aspects and flexibility in reactive power generation by controlling inverters 1 and 2 in a particular manner. The grid currents i_a, i_b, and i_c originate from the inverter line currents following the algebraic relations, which are consequence of the Y-Y-Δ structure of the interconnection transformer to the high voltage utility grid.

The control methodology adopted for the main conversion chain can deliver unity power factor at the grid (transformer primary) under any load condition. Additionally, the operating point of the bridges and the generator design can be matched to minimize the 5th and 7th harmonics of the grid currents when the turbine operates at nominal power. The undesired harmonics are further reduced by the active harmonic compensator, shown in green in Figure 1, which does not deliver any active power. Its control technique is based on the real-time minimization of the "distance" (as defined in functional analysis) between the desired reference and actual line currents [1]. The use of low-cost standard thyristors is possible in either or both bridges provided that well-known commutation circuits are used (for example, ASCI – auto sequentially commutated inverter). This renders the topology suitable for very-high-power wind turbines and potentially improves its reliability due to the well known ruggedness characterizing the thyristors. It is important to observe that an eventual failure of the harmonic compensator (which constitutes the most critical sub-system from the reliability point of view) does not prevent, *a-priori,* the system from continuing to operate. Indeed, the harmonic compensator can be completely disconnected and the topology would remain capable of delivering the full rated power via the two current-source bridges accepting a reduction in the power quality. Even a failure occurring in one of the two current source bridges could permit a reduced power operation by short-circuiting the damaged

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bridge and adjusting the blade pitch of the turbine to obtain the suitable generator voltage for this uncommon condition. If the harmonic compensator remained operational during this fault in the main conversion chain, it could still be used to improve the harmonic content and, in principle, even supply some reactive power if connected properly to the transformer secondary of the current-source bridge that is still operating.

The topology shown in Figure 1 can also be reconfigured to test other proposed solutions. For example, the "indirect synthesis" topology [2] can be obtained by shorting and keeping one bridge inactive (the bridge using thyristors, if this were the case) while the static harmonic compensator is substituted with a Y-connected inductor-capacitor filter (L-C filter). If it is desirable, one can also connect the two current-source bridges in parallel at the direct current (DC) link by providing a three-terminal intergroup reactor instead of a simple inductor. This solution would leave unaffected the behavior on the alternating current (AC) side of the conversion chain while requiring half of the phase generator voltage and the double its line current (when compared to the series-connection solution), as shown in Figure 2. In conclusion, the prototype of the aforementioned chosen circuit realizes not only one single specific topological solution but also constitutes a reconfigurable test bench that allows exploration of different topologies for wind turbines.
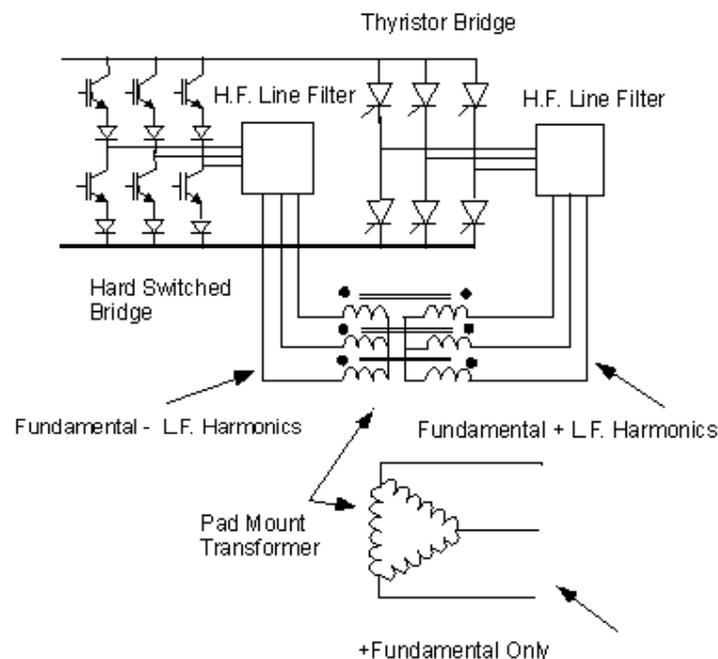
Figure 2. Alternative connection utilizing intergroup reactor

The choice of the tools used to model the selected topology fell on the combination of Matlab/Simulink (by Mathworks) and Simplorer (by Ansoft), mainly because Simplorer possesses an interface which provides the strategic ability to simulate in parallel and communicate with Matlab/Simulink. In this manner, it is possible to devote the simulation of the topology to a true circuit simulator (Simplorer) while keeping the ability to implement its control system entirely in Simulink. Furthermore, all desired simulation results can be transferred to Matlab for their subsequent evaluation, post-processing, and storage.

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Control Principle

This section gives an overview of the operational principles at the basis of the overall controller for the topology shown in Figure 1. It is possible to identify two main control tasks in the systems which are voluntarily separate from each other for the sake of the fault-tolerance of the converter. This also avoids unnecessary mutual dependencies among control loops which usually lead to behavior that is difficult to diagnose and correct.

Controller of the CSI Bridges and DC-Link Current

The first and most important control task is the regulation of the phase angle of the two current source inverter (CSI) bridges 1 and 2, and the consequent regulation of the DC-link current around the desired constant value associated with the actual speed of the turbine via its planned "power vs. rotational speed" curve.

The inverters 1 and 2 are operated independently using the conventional phase-control technique, which leads to the displacement of the fundamental line currents with respect to the related fundamental phase voltages by the controlled angles ϕ_1 and ϕ_2 (for the bridges 1 and 2 respectively). With the use of fully controllable devices, the control angles can range over the interval $[-\pi, \pi]$, thereby allowing not only lagging but leading fundamental power factor operation. This is a key distinctive feature of this solution versus the case in which only thyristors are used in one of the two bridges. Under the assumptions of instantaneous current commutation between any two switches and an ideal transformer, Equations (1) and (2) below constitute the general expressions for the modulus and absolute phase, respectively, of the complex Fourier coefficient C_n of the grid line current i_a. In Equations (1) and (2), $\alpha = (\phi_1 - \phi_2)/2$, $\beta = (\phi_1 + \phi_2)/2$, n is the harmonic order, and I_{dc} is DC-link current (assumed constant).

From these equations, it may be seen that the amplitudes of the harmonics depend only on α; i.e., the difference between ϕ_1 and ϕ_2, while the absolute phase depends only on β, i.e., the sum of ϕ_1 and ϕ_2. From Equation (2) it can inferred that β performs a pure phase displacement of the grid line current waveform because the absolute phases of all harmonics are linearly dependent on β through the harmonic order n. Figure 3 shows the aforementioned angles together with the phasors of the fundamental of the currents in the corresponding phases of the bridges 1 (blue) and 2 (red).

$$|C_n| = \frac{2}{\pi n} \cdot I_{dc} \cdot \left(1 - (-1)^n\right) \cdot \sqrt{2 - 2\cos\left(\frac{4n\pi}{3}\right)} \cdot \left| \cos\left(\frac{n\pi}{6}\right) \cdot \cos(n\alpha) \right| \tag{1}$$

$$\arg(C_n) = n\beta + \tan^{-1}\left(\frac{\cos(4n\pi/3) - 1}{\sin(4n\pi/3)} \right) \tag{2}$$

$$\langle V_{dc} \rangle = \frac{6 \cdot V_{llpk}}{\pi} \cdot \cos\alpha \cdot \cos\beta \qquad \text{Average value of } Vdc \tag{3}$$

V_{llpk} is the amplitude of the line-to-line voltage at the transformer having identical secondaries.

Figure 3. Illustrating angles ϕ_1, ϕ_2 , α, and β

From the previous observations, it follows that the angle α can be used to control the amplitudes of the harmonic components present in the grid line currents while the angle β can be used to *independently* control the fundamental power factor of these currents with respect to the related grid phase voltages. In [1], it was demonstrated that the amplitude of the 5th or 7th harmonic of the line currents, computable via Equation (1), can be nullified for specific values of the angle α while always maintaining an essentially unity fundamental grid power factor. Furthermore, it was shown in [1] that by selecting $\alpha = 0.914 \cdot \pi$ (164.52°), one obtains a minimum sum of the average power associated with the 5th and 7th harmonics, highly desirable for power quality. These results are summarized in Table 1 and Figure 4. It follows that by controlling α to remain close to 0.914 π, while simultaneously and independently controlling β, one can produce also a desired fundamental grid power factor (leading, unity or lagging). The active harmonic compensator shown in Figure 1 is introduced to further improve the harmonic content and - because of the control of the reactive power achieved through β - it does not need to provide any reactive power at fundamental frequency.

Table 1. Values of the Phase-Control Angle φ Reducing the Harmonic Content of the Grid Line Current

$\varphi_1 = (9/10)\pi \ (162°)$	Nullifies the 5th harmonic
$\varphi_2 = (13/14)\pi \ (167.1°)$	Nullifies the 7th harmonic
$\varphi_3 = 0.914\,\pi \ (164.52°)$	Minimizes the total average power in the 5th and 7th harmonics

Figure 4. Amplitudes of the 5th and 7th harmonics versus the phase-control angle

The capability of controlling the generated reactive power is very advantageous for distributed power generation systems such as wind turbines. Neglecting the CSI losses, the average power at the grid is equal to the average power on the DC side, $\langle V_{dc} \rangle \cdot I_{dc}$, and Equation (3) shows how the average value of the sum of the DC-link bridge voltages, $\langle V_{dc} \rangle$, depends on α and β, thereby providing the capability of controlling I_{dc}. Figures 5a and 5b show two simulated waveforms for i_a with $\alpha = 167°$ and with $\beta = 40°$ leading and $\beta = 0°$, respectively.

(a) α = 167°, β = 40° leading   (b) α = 167°, β = 0°
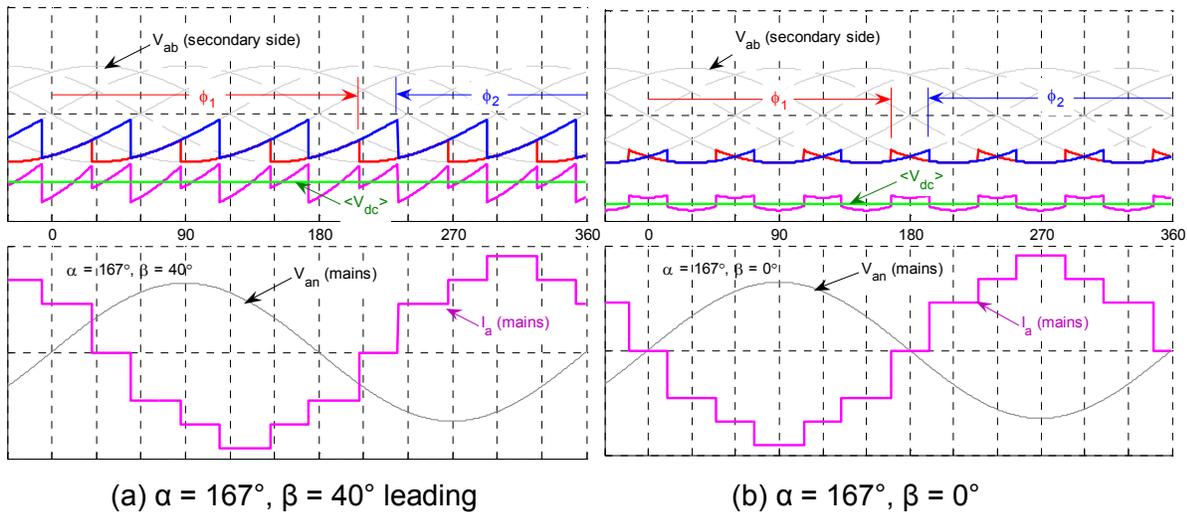
Figure 5. Simulated converter waveforms (bottom) for α = 167°. The waveforms in the upper plots are bridge 1 DC-link voltage (blue), bridge 2 DC-link voltage (red), Vdc (magenta), and average total DC-link voltage <Vdc> (green)

In both cases, the difference between ϕ_1 and ϕ_2 $(2 \cdot \alpha)$ does not change; thus, the shape of the grid current waveform remains unaltered, while it is shifted with respect to the grid phase voltage by the control angle β.

The DC-link current can remain bounded in time if, and only if, the rectified generator voltage and the sum of the two DC-side voltages of the current-source bridges possess identical average values. Because of the nature of the system, no direct or fast-acting control of the generator

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voltage is possible, so that modifying the phase-control angle constitutes the only method by which such equality can be achieved. The value of the phase-control angle able to equate the aforementioned average voltages is obtained via a proportional integral (PI) regulator whose input is the error between the desired and actual DC-link current. It can be observed that the DC-link current contains all the information necessary about the equality between those average voltage values. When they tend to differ, a diverging trend appears in which the current and the PI controller act to eliminate this error by modifying the phase-control angle properly. It is then sufficient, in principle, to measure only the DC-link current at the base of the tower, thereby avoiding other sensors in the nacelle and the consequent complexity and cost to transmit their measurement to the controller located at the ground level. With this control strategy, the rectified generator voltage acts like a disturbance as depicted in Figure 6. Nonetheless, it must be pointed out that for some combinations of DC-link inductance, PI parameters, and control performance requirements, it might be worthwhile to also measure the rectified generator voltage to provide a feed-forward action able to improve the control loop dynamic. This measurement is present in the prototype, although it is not presently used.

Additionally, it must be noted that the blade-pitch mechanical control of a wind turbine acts inside a good range of wind speeds to stabilize the permanent magnet generator voltage at its nominal value characterized by the desired rated power. It is then advisable to design the generator nominal voltage so that its average value is as close as possible to the total average value of the two current-source bridges in series when they operate with the optimum phase-control angle $0.914\,\pi$. This design choice greatly contributes to the reduction of the 5th and 7th harmonics of the grid line current at rated power, already without the correction performed by the active harmonic compensator. The phase-control angle is clearly upper value bounded, mainly by the necessary recovery time in case of use of a thyristor bridge. Should large sudden grid voltage drops and/or voltage escalations in the generator occur, it might become impossible to limit the DC-link current without exceeding the maximum allowed value for the control angle. In this case, the controller provides a proper overcurrent emergency protection to keep the DC-link current at safe values. It is also desirable to detect the onset of discontinuous current operation in the DC link, which could occur at very light load conditions. In such cases, it would be advantageous to simply disconnect the entire system from the grid since the power generated under this condition is minimal. The operational principle of the control loop implementing this control task is shown in Figure 6 for the case of $\beta = 0$; i.e., unity fundamental power factor at the grid under all operating conditions.
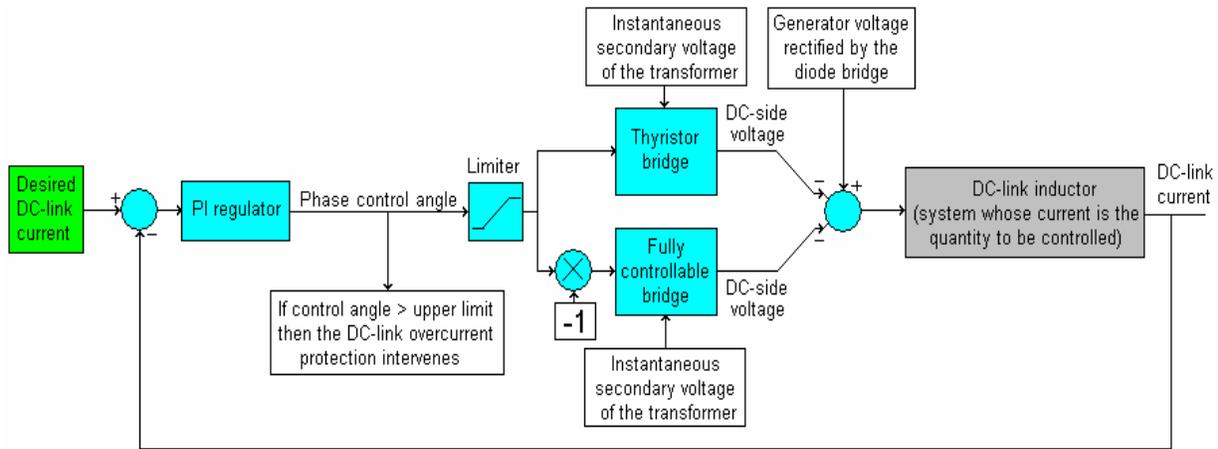
Figure 6. Operational principle characterizing the controller of the main conversion chain for $\beta = 0$

Control of the Active Harmonic Compensator

The second control task consists of synthesis of the proper corrective currents that the active harmonic compensator (a classical voltage source inverter [VSI] three-phase inverter) must inject in the main conversion chain to achieve a further reduction of the harmonics in the grid line currents. Such a task can be conceptually subdivided in three sequential steps listed below and illustrated in Figure 7. For the sake of cost reduction, it is preferable to connect the VSI at one of the transformer secondaries, although in principle it could operate also at the primary. The control task includes:

1. Estimating the amplitude that the purely sinusoidal reference grid line currents must possess to deliver the same average power at the grid

2. Using such grid reference currents to compute indirectly the specific reference currents for the active harmonic compensator

3. Tracking and synthesizing these last currents through a control technique based on the real-time minimization of a proper time-varying functional algorithm.

The required amplitude of the desired purely sinusoidal grid reference current is obtainable through the simultaneous measurement of the average power delivered to the grid and the amplitude of the grid phase voltages. Because the fundamental power factor is already guaranteed to be unity (or any desired value lagging or leading) by the previously illustrated control technique used for the main conversion chain, a simple algebraic division suffices in obtaining the required current amplitude. It must be observed that the measurement of the average power is insensible to the harmonic contents in the transformer primary line currents. By exploiting this property, the aforementioned amplitude estimation is decoupled from the action of the active harmonic compensator. The amplitude estimated at this point must still be corrected by the contribution of the PI regulator devoted to maintain the VSI DC-link voltage close to its desired value. Indeed, if the VSI DC-link voltage decreases or increases, the PI regulator increments or depletes the estimated amplitude respectively.

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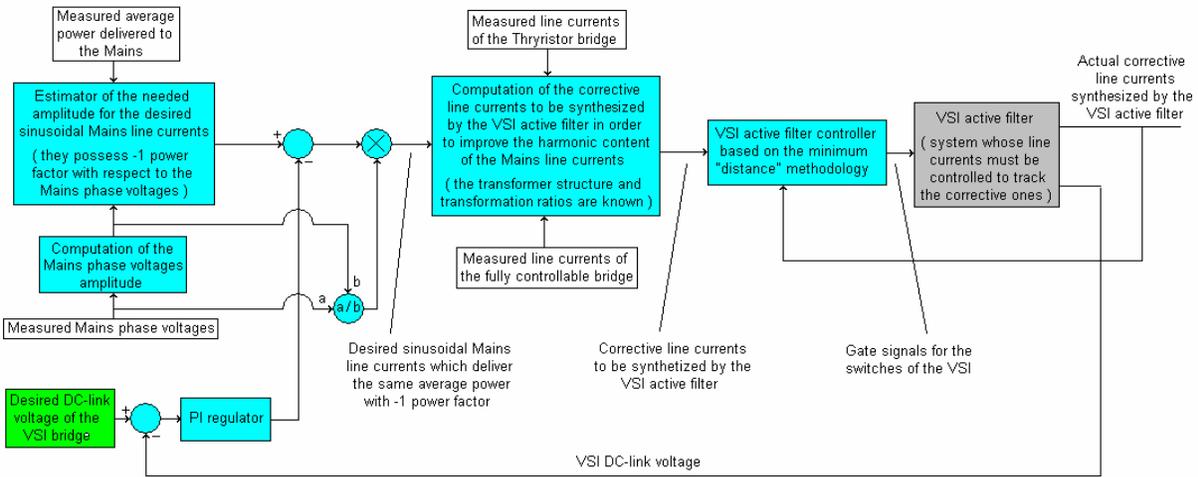
Figure 7. Operational principle characterizing the controller for the active harmonic compensator

In this manner, a quota of energy is delivered or withdrawn from the VSI, thereby stabilizing its DC-link voltage. Once the correct amplitude of the reference grid currents becomes available, the corresponding sinusoidal waveforms for the line currents are straightforwardly obtained through normalization of the measured phase voltages and consequent multiplication by the estimated amplitude. At this point, where the reference waveforms for the grid line currents are known, it is possible to compute indirectly the specific corrective reference line currents to be synthesized by the VSI when it is connected to the same secondary of the fully controllable current-source bridge. This step is quite straightforward and involves only algebraic operations, provided the structure and transformation ratios of the transformer are known, together with the measured line currents at the outputs of the two current-source bridges. The last step is the effective tracking of these corrective reference currents performed by the VSI via proper switching commands issued to its fully controllable (usually insulated gate bipolar transistor [IGBT]) switches. The details of the VSI current-tracking controller have been published by the investigators in [1].

It is nevertheless important to note the basic principle on which such controller is based. The control exploits the real-time minimization of a proper time-varying functional, which, converging to its minimum, gives the optimal switching states for current-tracking. Such functional represents the "distance" among the actual and reference waveforms, as defined in the branch of mathematics usually named "functional analysis." The minimization of the functional is performed on a discrete-time basis defined by a clock signal (whose frequency is not greater than 10 kHz to limit the switching losses in the semiconductors), and the overall resulting controller action could be classified as a type of carrierless PWM. Because the clock frequency will always be limited in practice, a reduced-size L-C filter is advisable at the grid side to filter the remaining high-frequency harmonics.

The following simulation results obtained from the joint operation of Simplorer and Simulink are provided to illustrate the operation of the two control tasks previously explained. Figure 8 shows the grid line currents (blue) before 0.25 s, when only the two current-source bridges are active, and after that instant when the harmonic compensator is enabled. Figure 9 shows the harmonic spectrum (computed after 0.25 s.) up to 2 kHz and shows that no harmonic exceeds 5.2% of the fundamental. Although before 0.25 s. the quality of such waveforms appears poorer, they possess the minimum 5th and 7th harmonics thanks to the overall choices explained above and detailed in

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the following. Figure 10 shows the voltages of the two bridges (blue and red) and their sum (magenta), which, together with the rectified generator voltage (green), influences the DC-link current. Figure 11 shows the regulation performed by the DC-link controller, which stabilizes the phase-control angle close to the optimum value of 165° also after the intervention of the harmonic compensator. This highlights the fault-tolerant decoupling between the two controllers. Figure 12 shows the instantaneous power (negative) withdrawn from the grid, while Figure 13 depicts the shape of the generator phase electromagnetic frequency (EMF) originally assumed for the permanent magnet (PM) generator. Figure 14 compares the estimated (magenta) and actual (blue) Grid line currents, while Figure 15 illustrates how the "minimum distance" controller (operating at 10 kHz clock frequency) tracks the corrective line currents (magenta) demanded by the controller to improve the spectrum of the grid line currents.
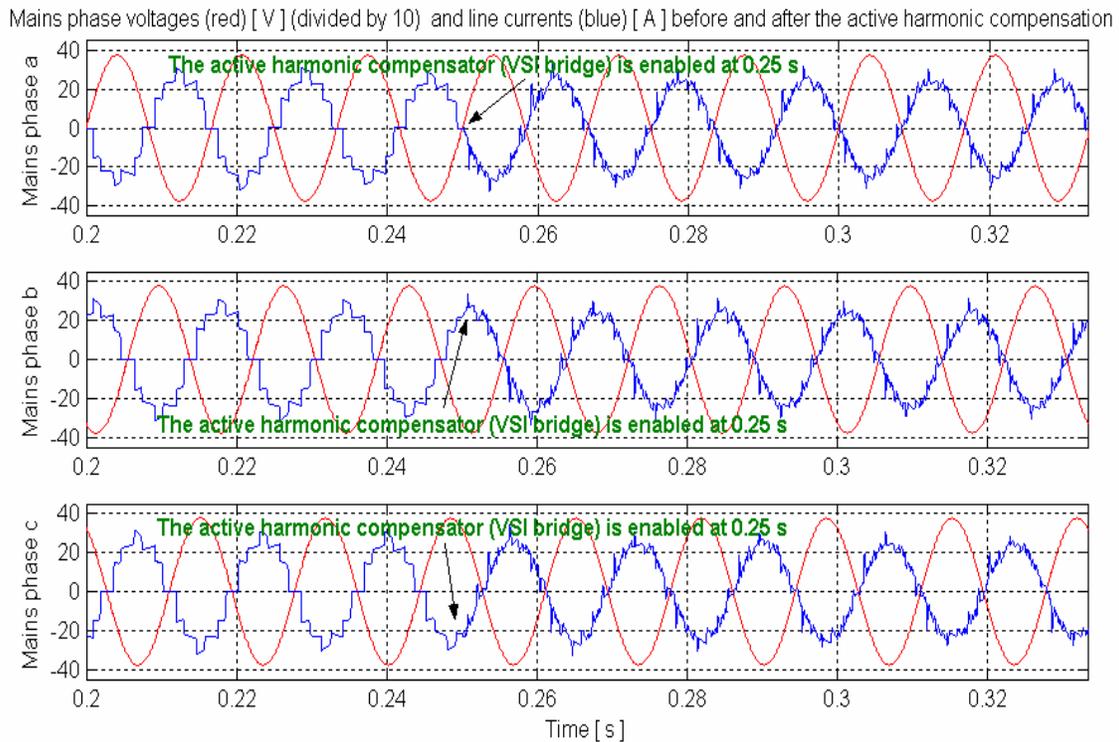
Figure 8. Grid line currents (blue) corrected by the VSI
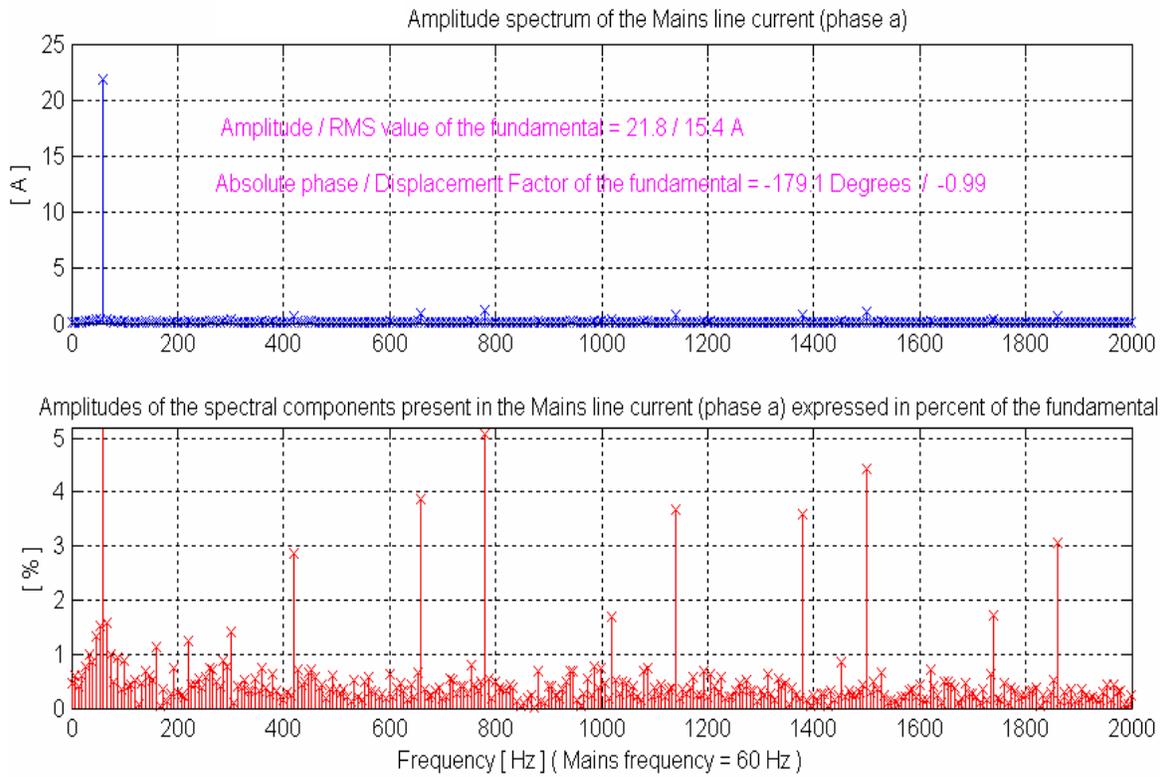
Figure 9. Spectrum of the corrected grid line currents
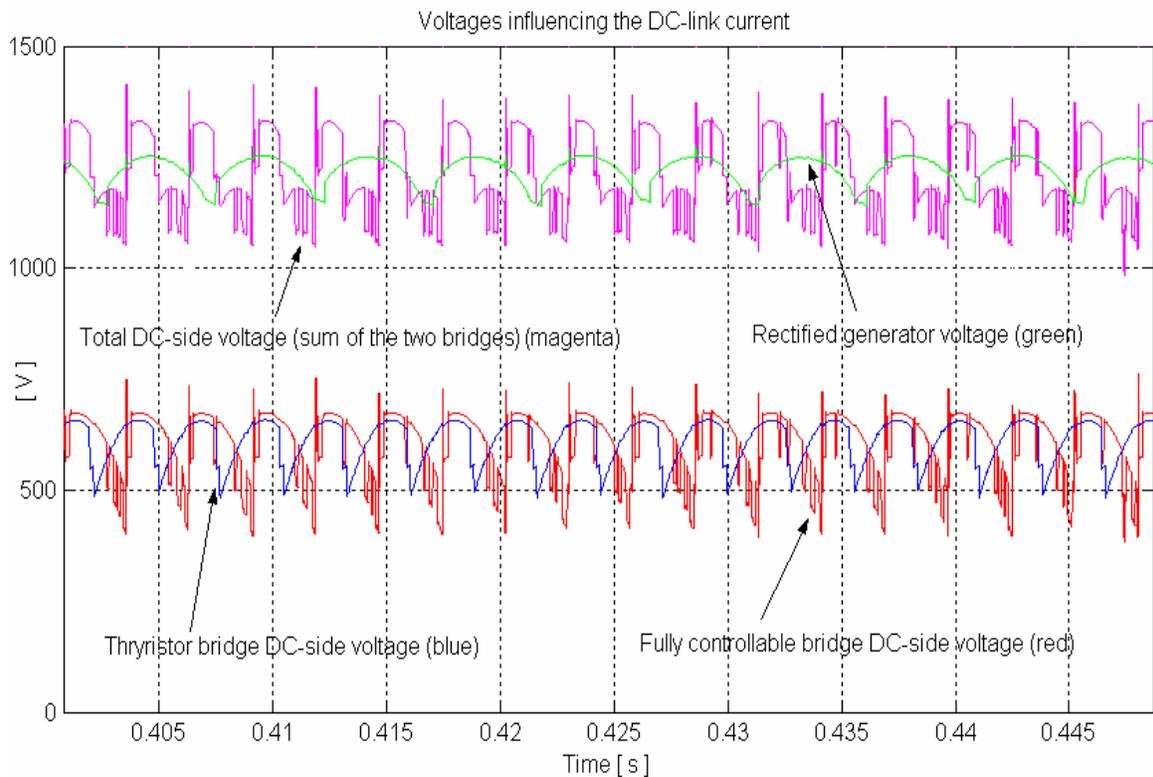
Figure 10. Voltages influencing the DC-link current
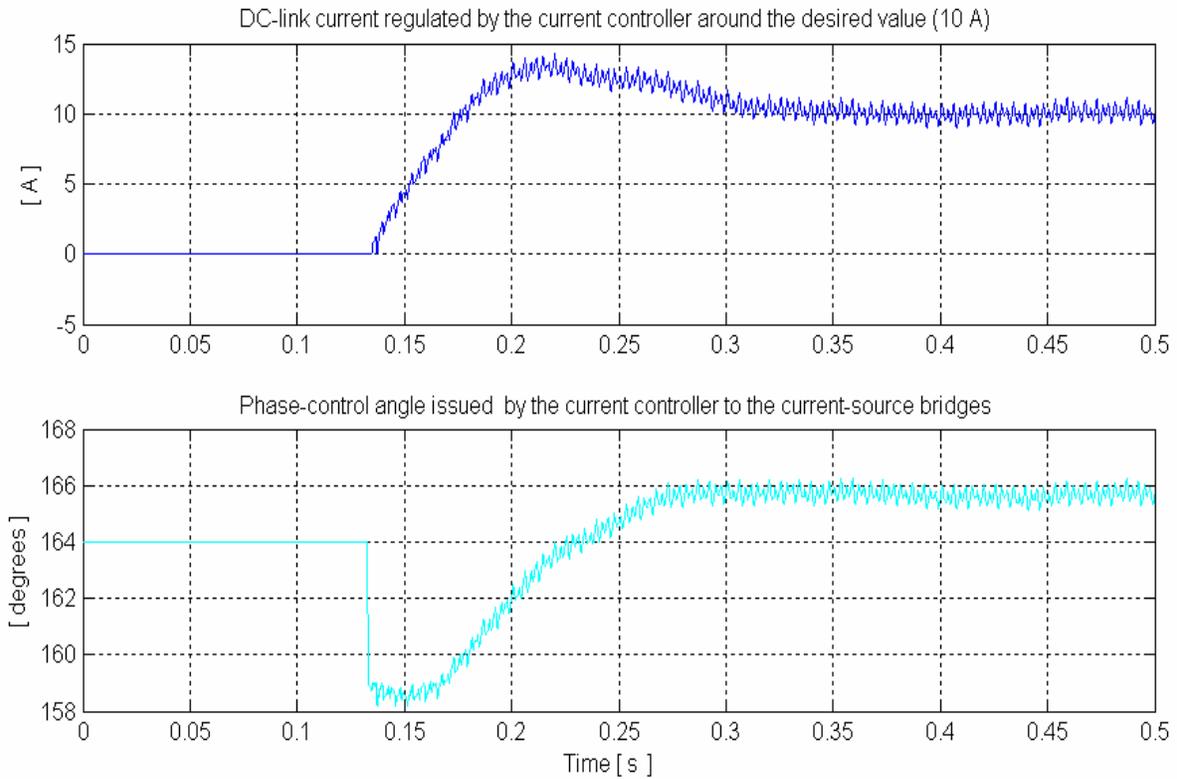
Figure 11. Regulation performed by the DC-link controller
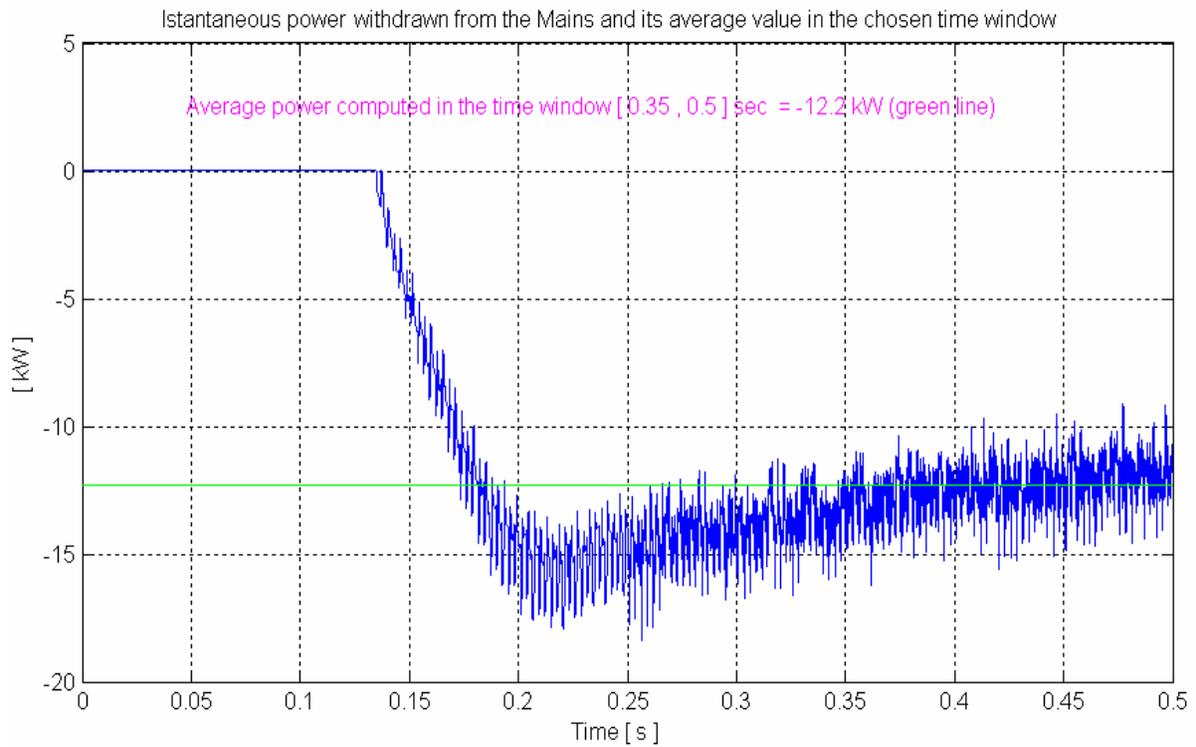
Figure 12. Instantaneous power delivered to the grid
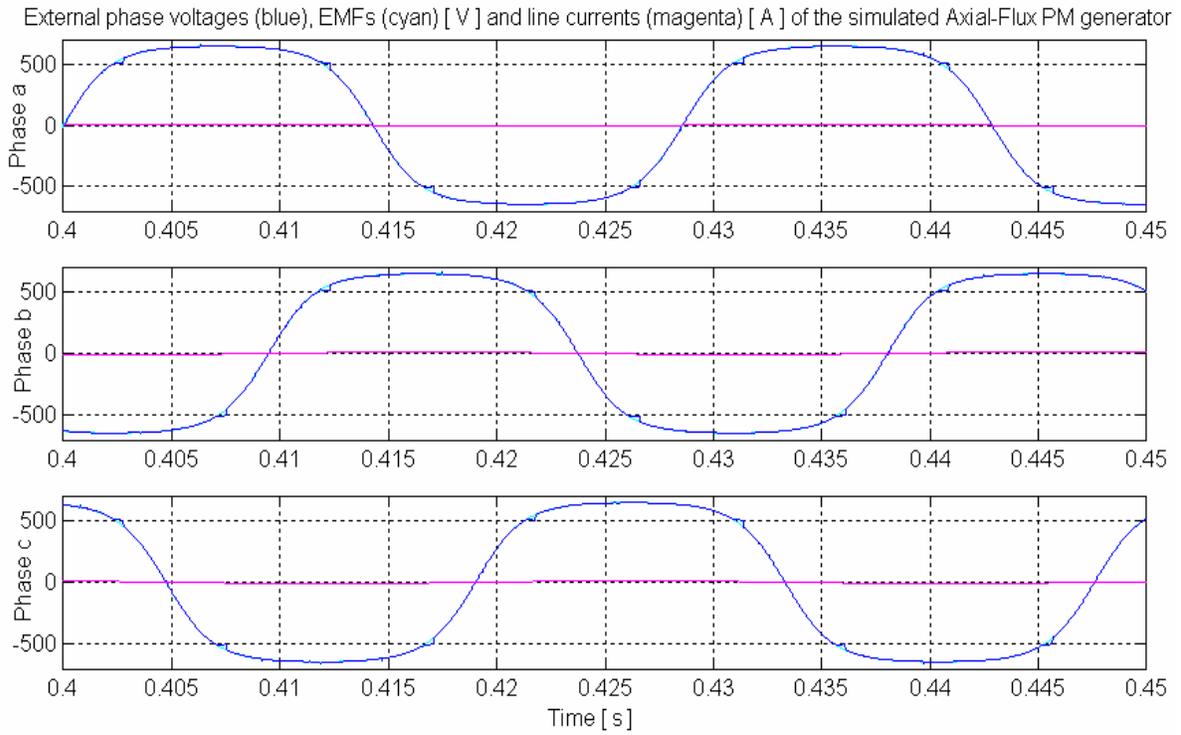
Figure 13. Simulated generator phase voltages
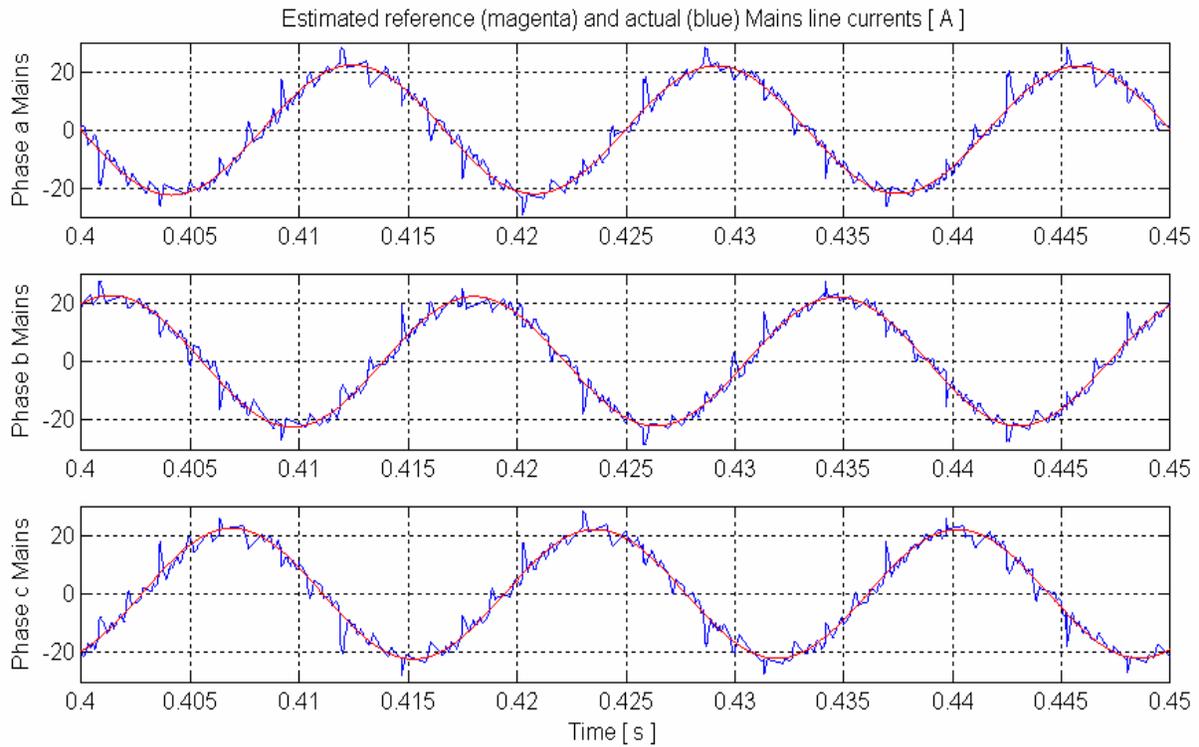
Figure 14. Reference and actual grid line currents

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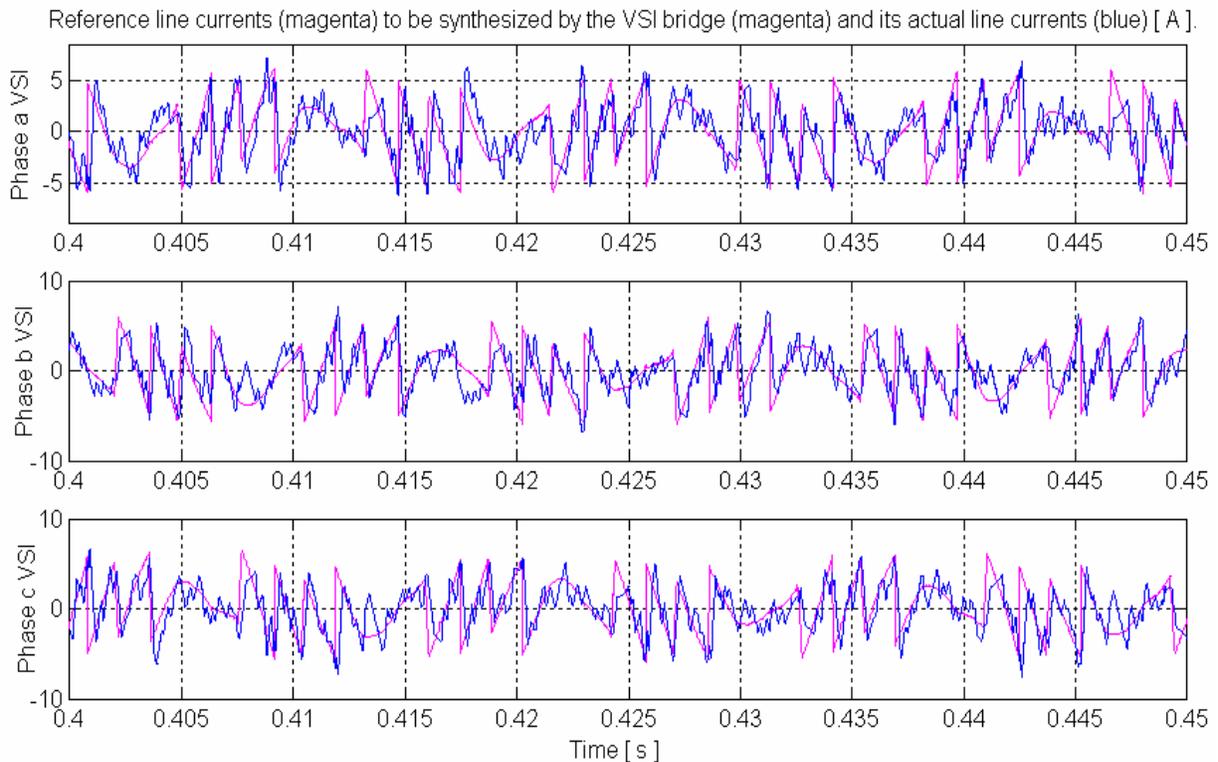
Figure 15. Reference and actual VSI line currents

Structure and Primary Features of the PM Axial Flux Generator

The structure and related drawings of the final PM generator constructed by McCleer Power and Light Engineering are reported in Figure 16, and the waveforms of two line-to-line back-EMFs provided by the manufacturer are shown in Figure 17. The primary features of the machine are as follows:

- 48 poles
- 19-inch external diameter
- 539 V line-to-line nominal root mean squared (RMS) voltage at 700 rpm nominal speed
- Two-sided stator, with a single rotor disk in the middle
- Uses amorphous steel laminations with open slots so that terminal inductance is very low
- Phase synchronous inductance of about 2 mH and phase leakage inductance of about 1.2 mH
- Phase winding resistance of about 0.58 Ω.

The short-circuit current at 700 rpm is approximately 90 A RMS, which is actually slightly larger than the latest 6-pole design by Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). The major external difference from such a design is the operating frequency, 280 Hz instead of 35 Hz, which leads to a rectified fundamental frequency of 1440 Hz instead of 210 Hz. This much higher frequency is still acceptable to avoid DC components in the interconnection transformer. Because of the much smaller fundamental period, the main drawback lies in the higher influence of the commutations in the rectifier, which occurs despite the low leakage inductance. To minimize this effect, fast diodes have been used in the prototype in which the diode rectifier bridge is obtained by using the antiparallel diodes of three 1200 V Semikron IGBT modules, one for each phase leg.

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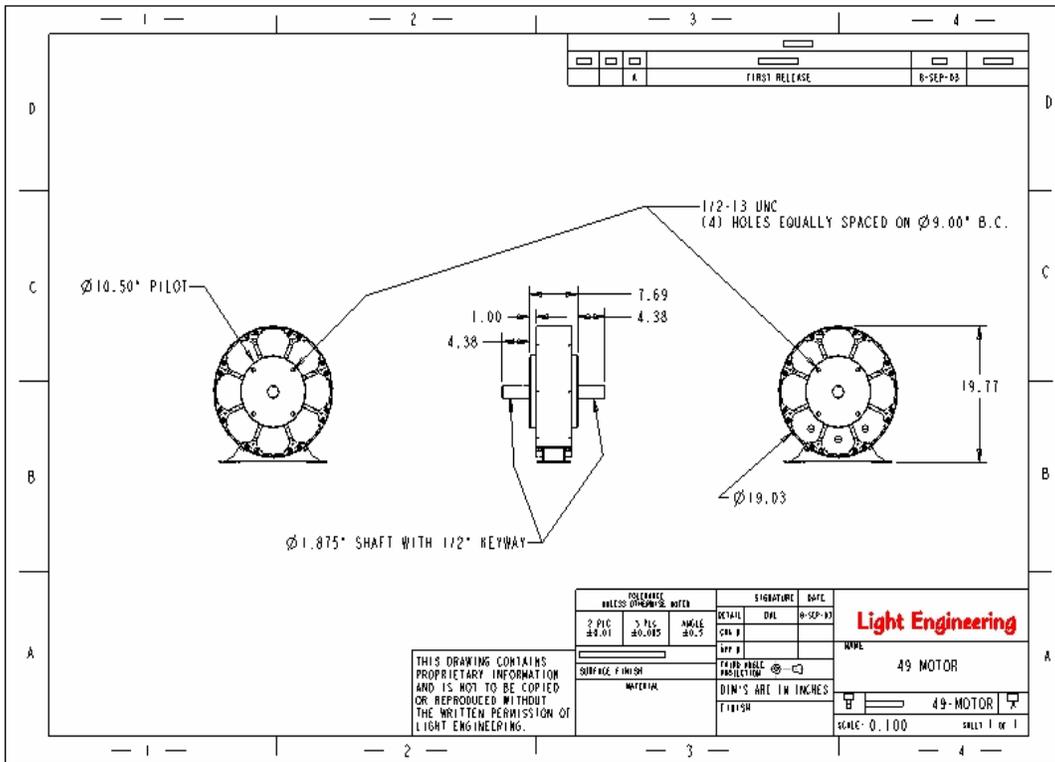
Figure 16. Mechanical drawings of the PM generator frame
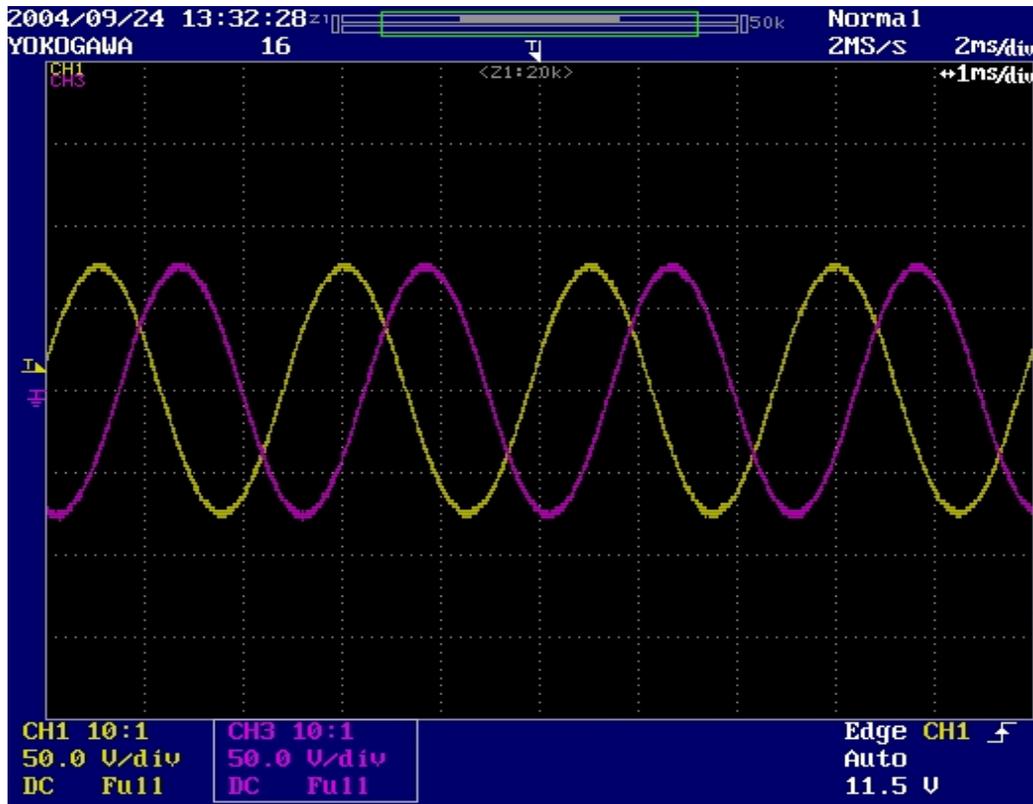
Figure 17. Waveforms of two line-to-line back-EMFs

Overview and Features of the Chosen DSP-Based Control System

This section provides a short description of the final digital signal processing (DSP) system chosen for this research. The controller is a XC 2000 DSP manufactured by AixControl GmbH in Aachen, Germany. Figure 18 shows the portable frame (19-inch rack form factor) that contains the entire DSP system including the controller board XCS 2000, the interface boards, the communication board, and the power supply for all of these components.

The double-processor controller board XCS2000 is shown in Figure 19. The manufacturer has customized the board for this project by providing 24 analog input channels, 8 analog output channels, and 32 digital input/output channels. The board is based on two Analog Devices, SHARC 21161N DSPs programmable through the Analog Devices Visual DSP ++ cross-compiler. The manufacturer provides libraries in C and C++ specifically oriented for power electronics control tasks. The board also features an optoisolated RS-232 interface.

Figure 18. Self-contained frame hosting the XC 2000 system

Figure 19. XCS 2000 controller board

Four signal conditioning and interface boards complement the XCS 2000. Three of these are identical XCI 2000 boards shown in Figure 20 and will be used to control the three bridges present in the topology: two boards for the two CSI bridges and one for the VSI harmonic compensator. The XCI 2000 allows the measurement of eight analog channels with a dynamic range of ± 10 V. protected up to ± 40 V., while it simultaneously provides the eight independent control signals for four independent standard phase legs. A particularly remarkable feature of this board is its ability to interface itself and directly supply the Semikron Skiip modules, including also the analog measurements from their embedded current and voltage sensors.

The two CSI bridges of the prototype are based on salvaged Skiip modules, which has saved a considerable amount of time and cost. However, the project budget could not allow for the purchase of a third Skiip module (in excess of $3000) for the VSI harmonic compensator identified in Figure 1, which has been manually built. The fourth signal conditioning board, the XCI 2020 shown in Figure 21, is used mainly to monitor up to eight analog internal variables of the DSP board and provides eight digital outputs. The dynamic range of the XCI 2020 analog outputs is ± 10 V, and all logic outputs are at transistor-transistor logic (TTL) level, buffered and protected against electrostatic discharges. The system also includes a 100 Mbit Ethernet communication board (XCC 2000) that provides the ability to transfer acquired data and control signals to and from the personal computer (PC) and LabView.

Figure 20. XCI 2000 four-phase converter control card

Figure 21. XCI 2020 universal input/output card

Prototype and Experimental Results

Figures 22 through 33 show views of the 10-kW experimental setup built in the WEMPEC laboratory.

Figure 22. Diagonal view of the experimental setup with the Variac and drive frame in the foreground
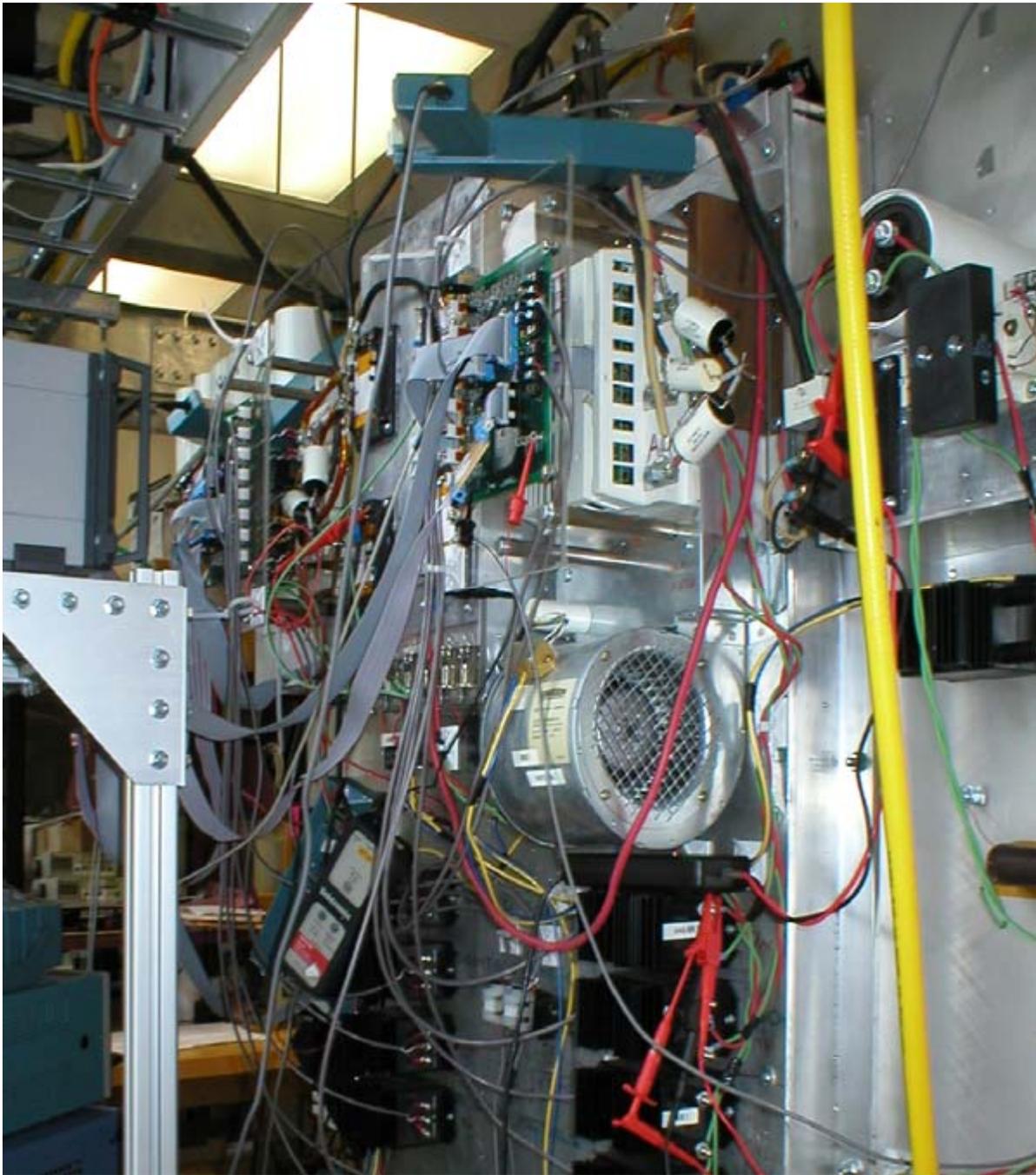
Figure 23. Rear view showing the two CSI bridges, DSP controller, and some of the voltage and current probes connected to the instrumentation
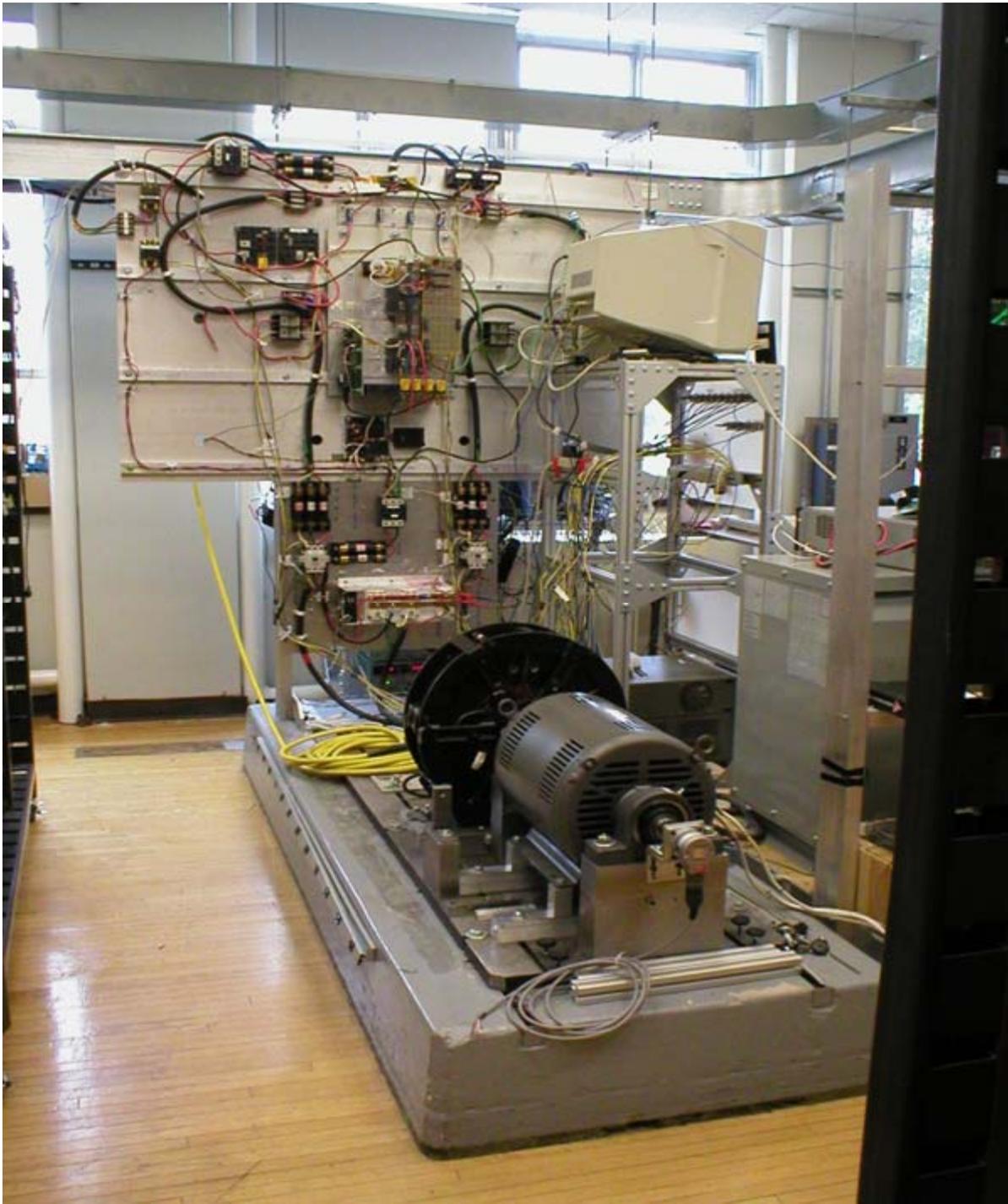
Figure 24. Diagonal view of the setup showing the dynamometer and the PM axial flux generator

Figure 25. Detail of the control panel for the entire prototype. The PC is used to program and set the references to the DSP controller, as well as to collect the measurement from the oscilloscopes

Each bidirectional voltage blocking switch in the prototype has been realized by the series combination of one IGBT (with integrated anti-parallel diode) and one external diode of equal voltage and current rating (1200 V and at least 100 A).
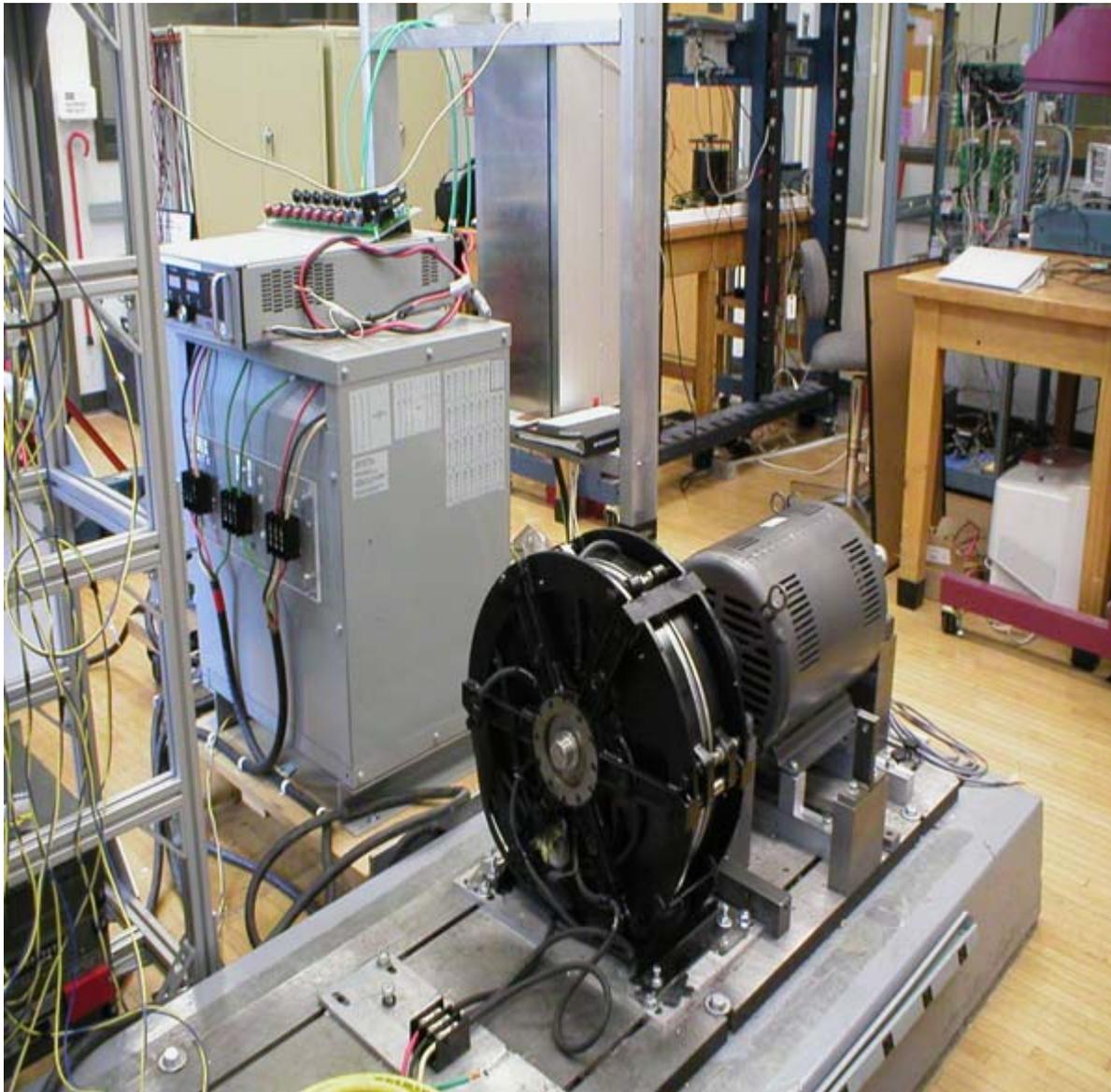
Figure 26. The interconnection transformer, axial flux PM generator, and dynamometer (prime mover emulating the propeller of the wind turbine)
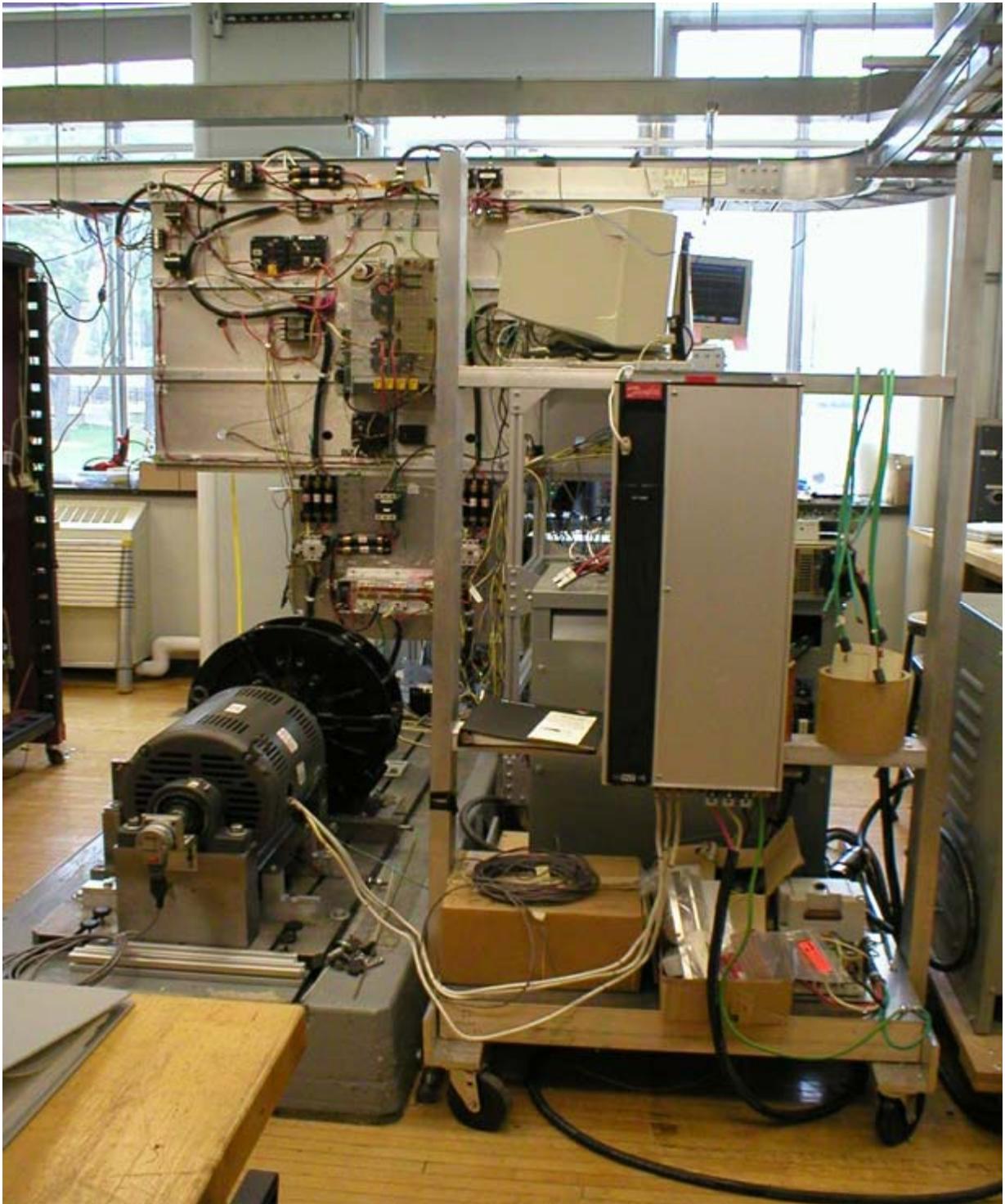
Figure 27. Drive for the dynamometer
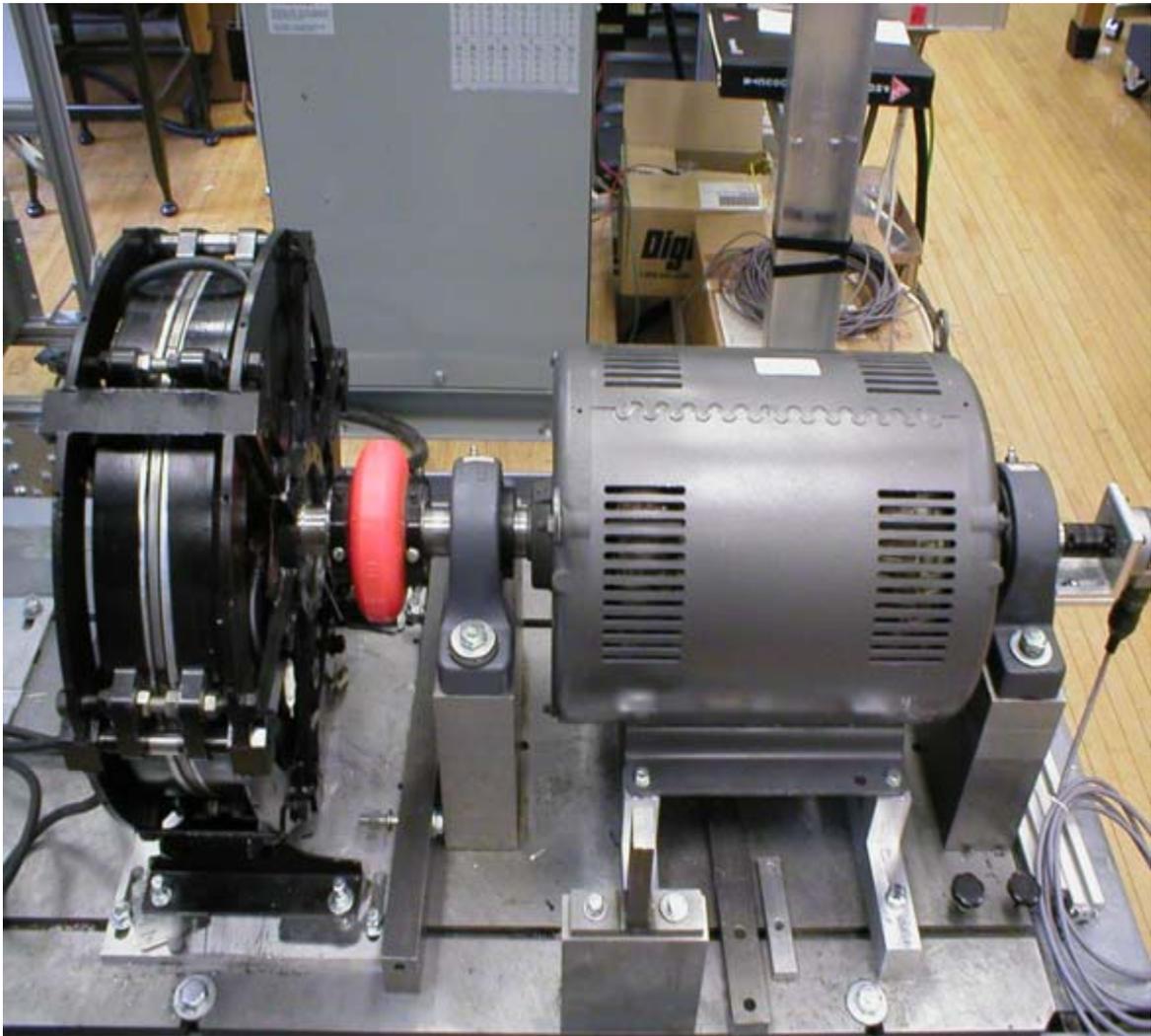
Figure 28. PM axial flux generator (left) coupled with the dynamometer (right)
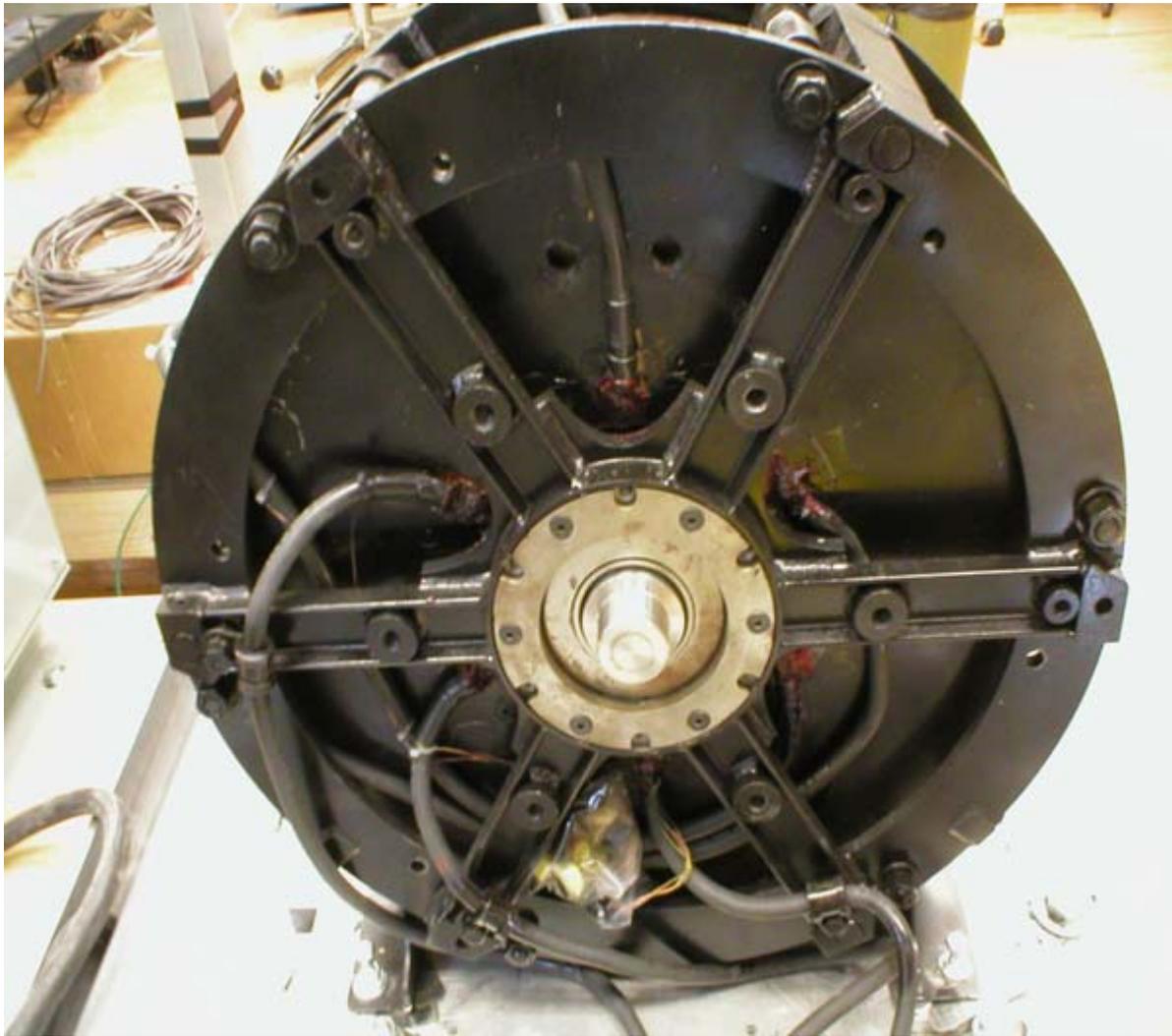
Figure 29. The PM axial flux generator built by Light Engineering

.
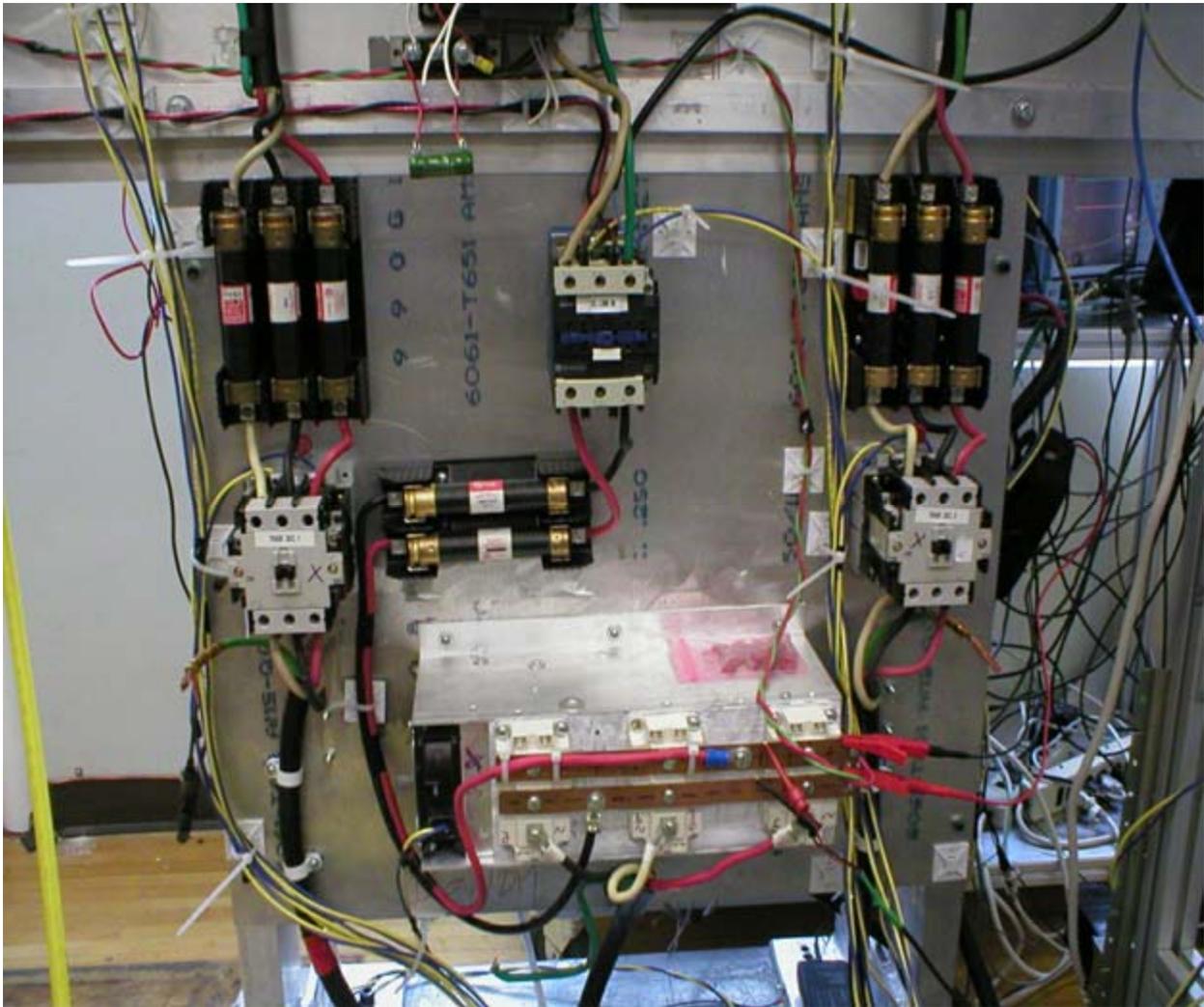
Figure 30. Diode bridge (bottom center) together with the contactors and fuses for DC-link and grid
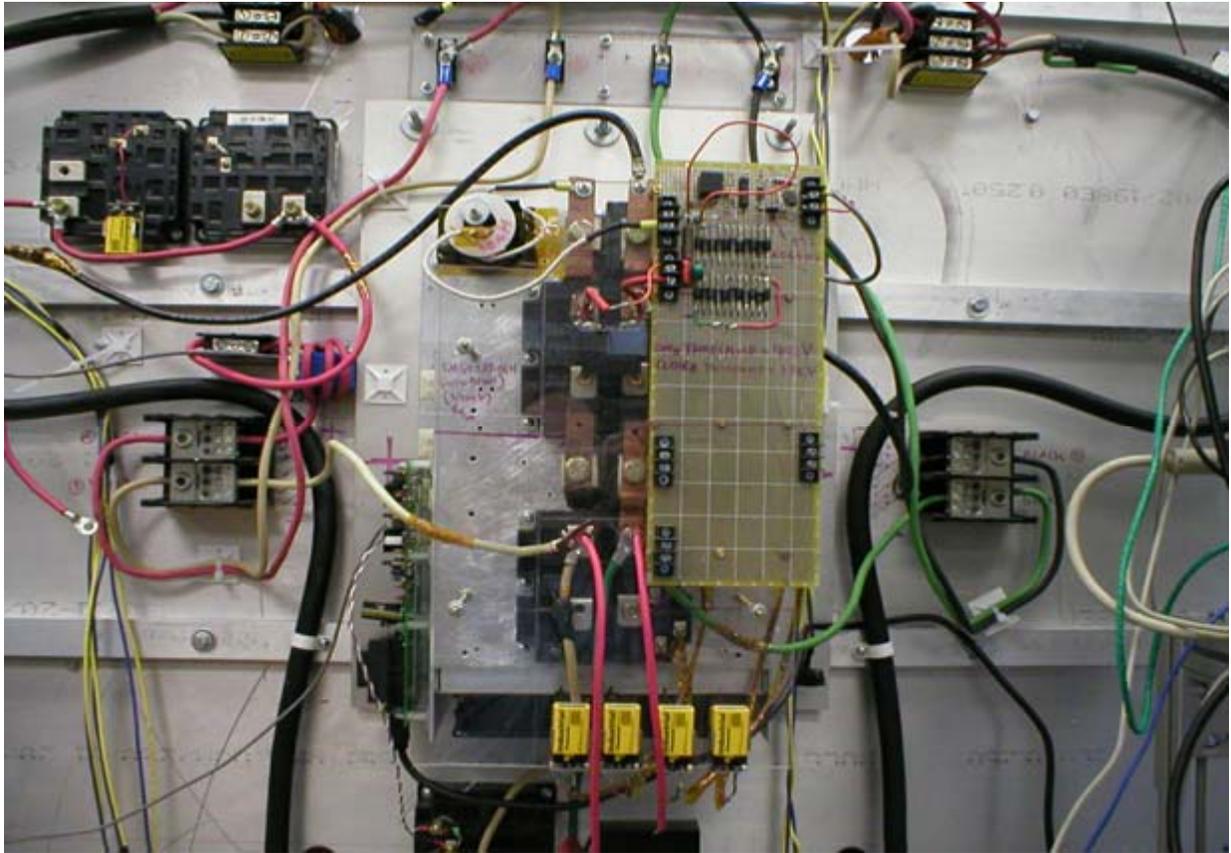
Figure 31. Protection circuit for the DC-link inductor described in [3] and reported in the Appendix
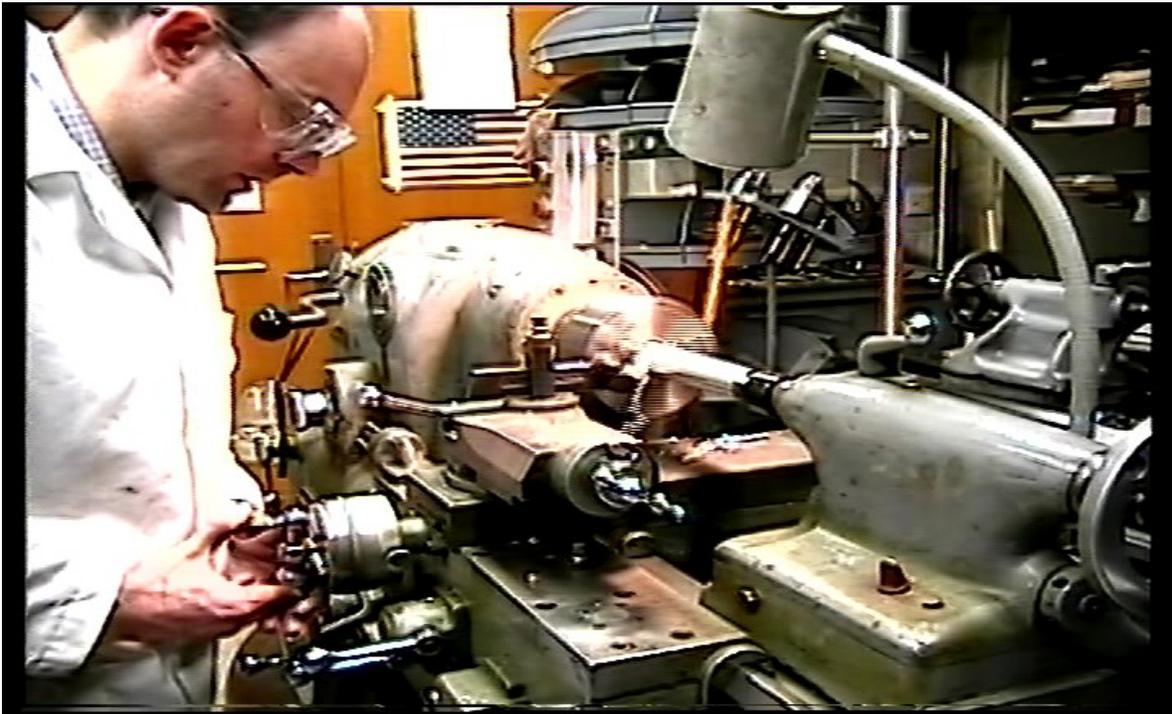
Figure 32. P. Tenca machining parts on the center lathe

Figure 33. P. Tenca machining parts on the milling machine

A selection of experimental results summarizing the control action on the main conversion chain is shown in Figure 34 (a-d) where the operating conditions are specified beneath each plot. These experimental results show the grid phase voltage V_a (magenta, 50 V/div.) and grid line current i_a (yellow, 20 A/div. for Figure 34a-c), 10 A/div. for Figure 34d) for various values of β, with α close to the analytically derived value which minimizes the 5th and 7th harmonics (164.52°). The Fast Fourier Transform (FFT) of the line current i_a is shown in orange in the lower and dedicated systems of axes (5·10^5 samples, rectangular window, 60 Hz/div. horizontal, vertical scale = ½ time domain scale per div.).
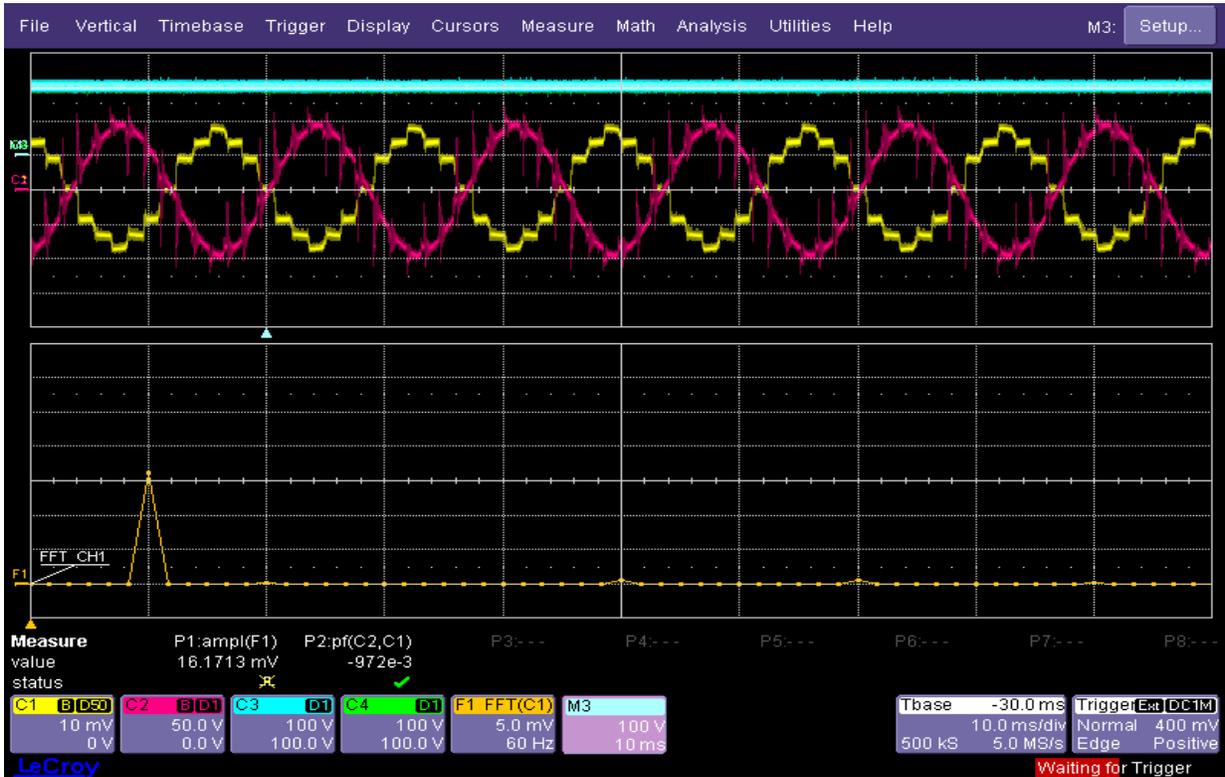
Figure 34a. α = 167°, β = 0°, Vll = 122VRMS, <Vdc> = 325 V, Idc = 15 A
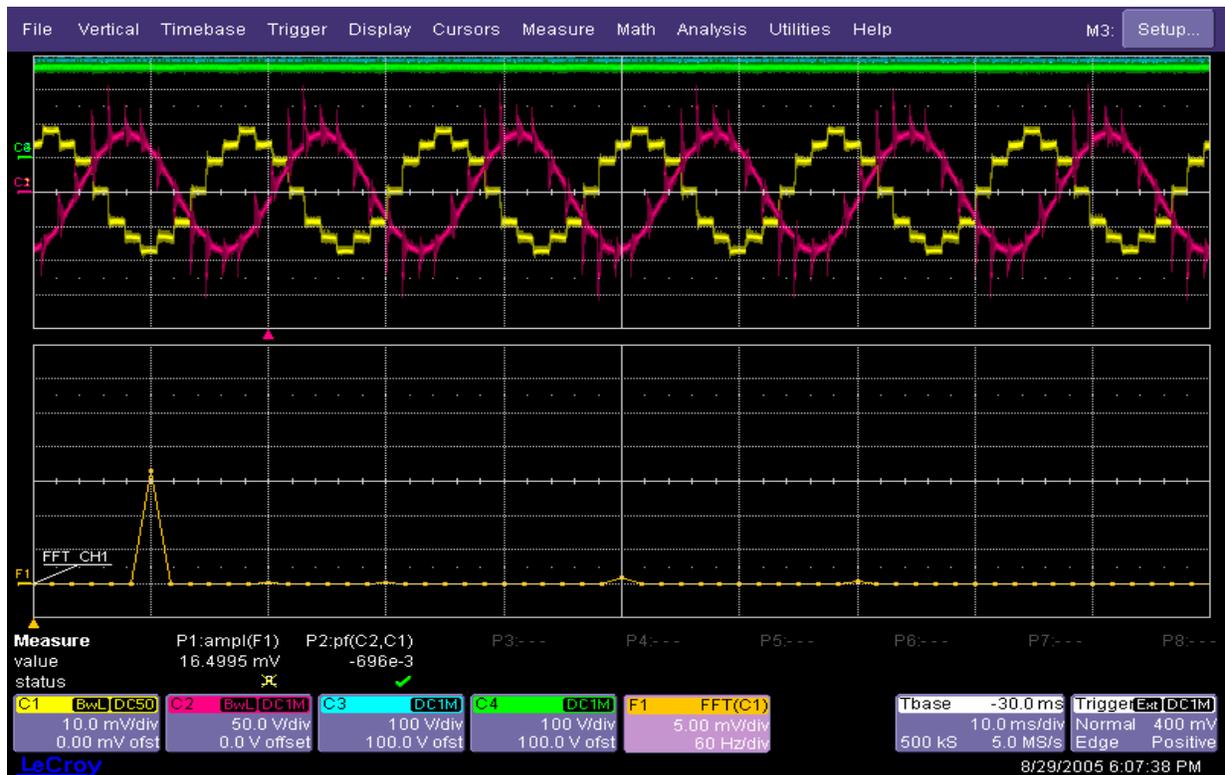
Figure 34b. α = 167°, β = 40° leading, Vll = 120VRMS, <Vdc> = 248 V, Idc = 15 A

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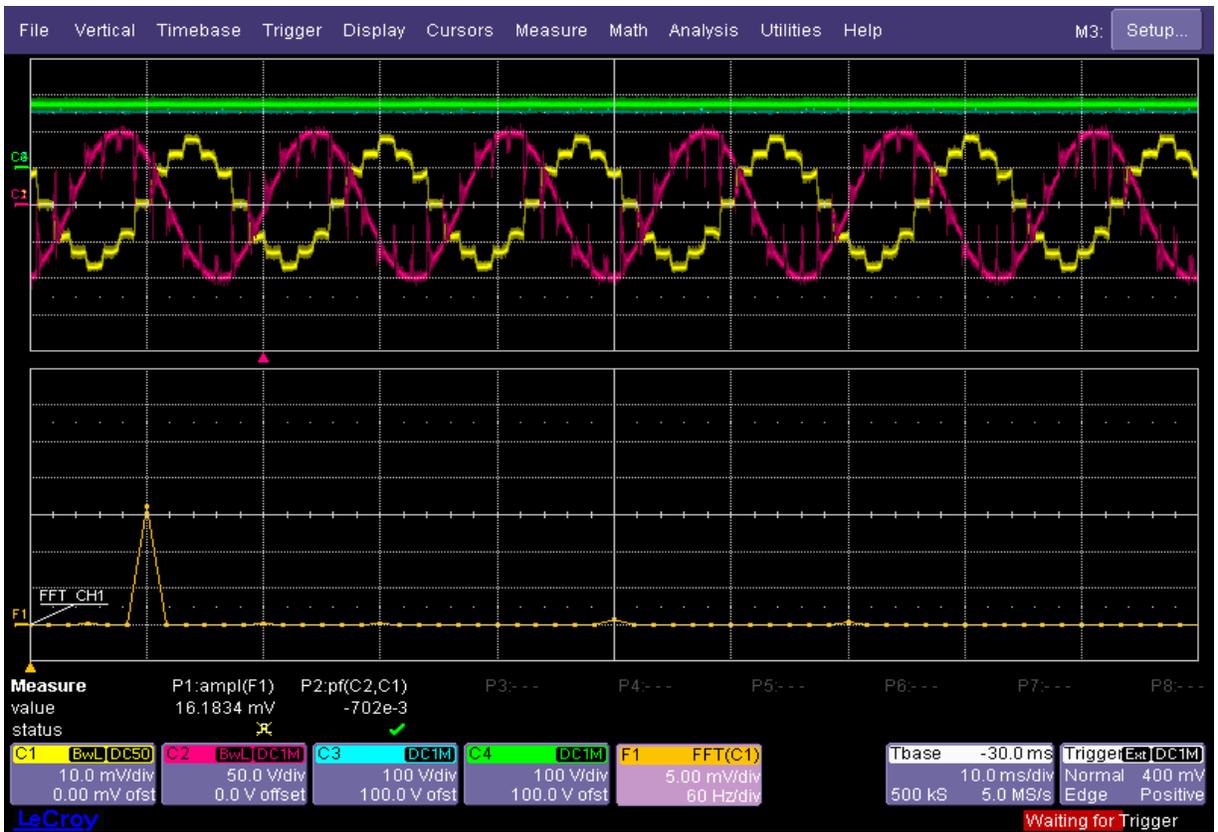
Figure 34c. α = 167°, β = 40° lagging, Vll = 120VRMS, <Vdc> = 248V, Idc = 15 A
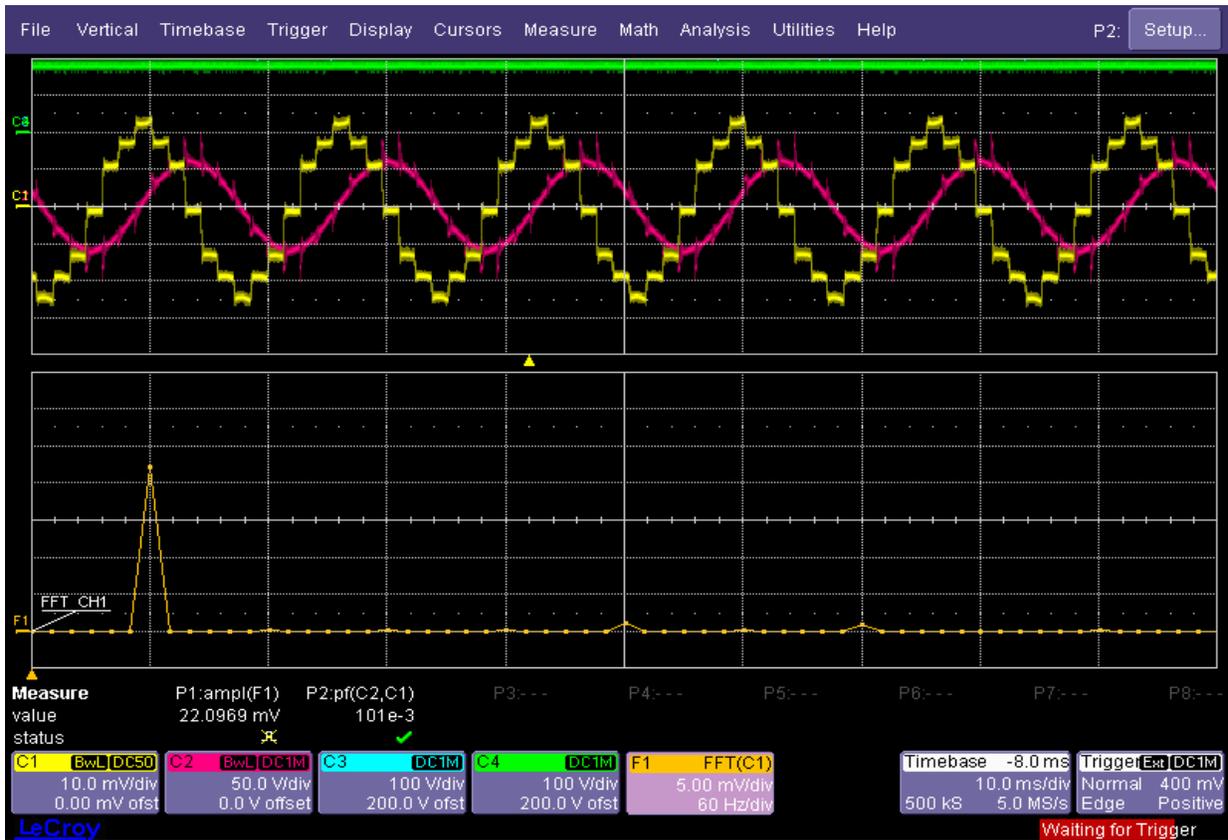
Figure 34d. α = 169°, β = 89.9° leading, VII = 80.8VRMS, <Vdc> = 10.4 V, Idc = 10 A (10 A/div.)

In Figure 34 (a-d) one can see that the 5th and 7th harmonics maintain a very reduced amplitude while the current waveform is shifted by the imposed angle β that can reach values very close to $\pi/2$, also leading, without significant distortion in the grid current waveform.

Further results, reported in Figures 35 through 42, are aimed at confirming the nullification of the 5th or 7th harmonics for different values of the angle α (with $\beta = 0$) as predicted by Equation (1) and Figures 3 and 4. Suitable comments are inserted directly on the captions. The average value of the DC-link voltage for these traces was about 160 V and $I_{dc} = 10$ A (10 A /div.).

Figures 43 through 47 show additional results when the angle β is controlled while keeping α at 167°.
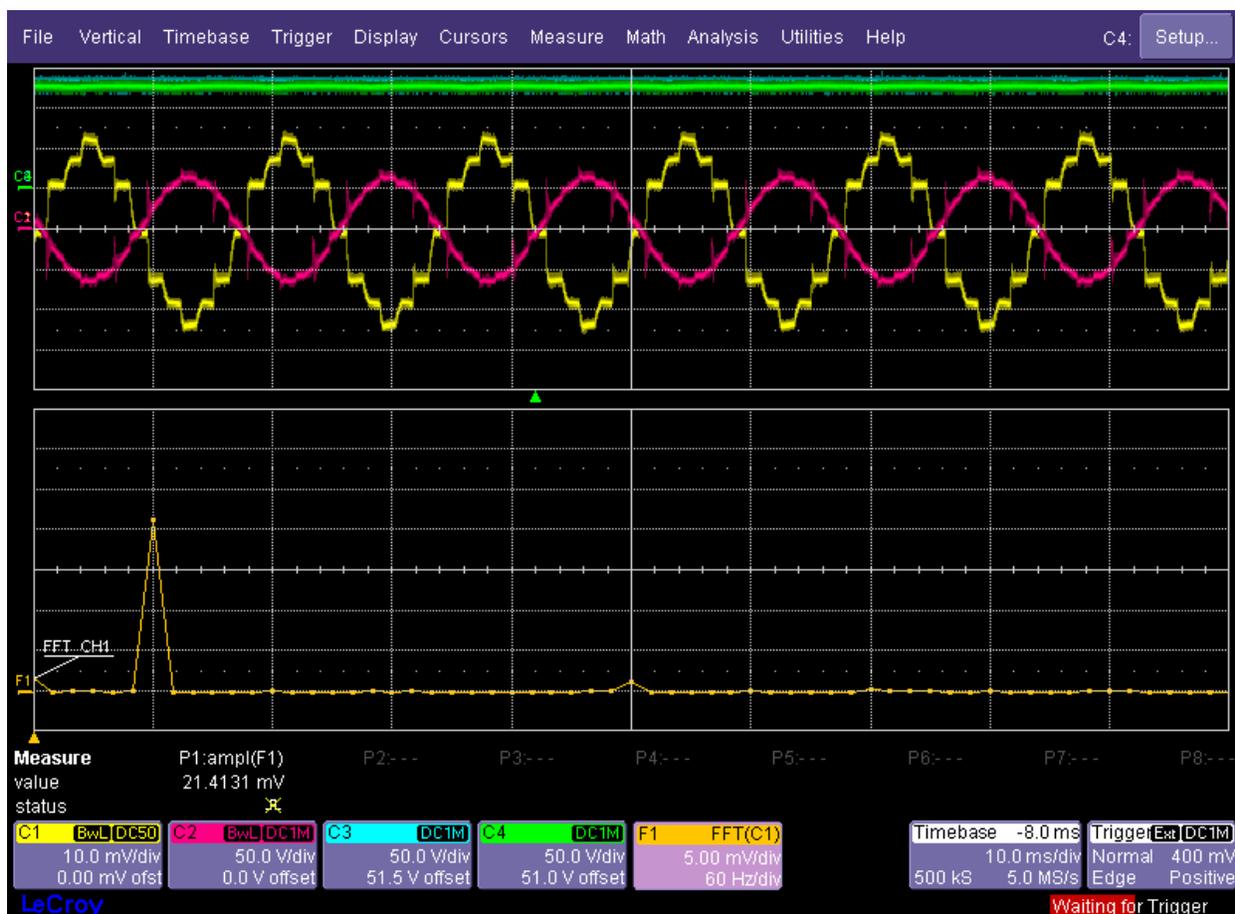
Figure 35. α = 167.8°. Zero of 7th harmonic
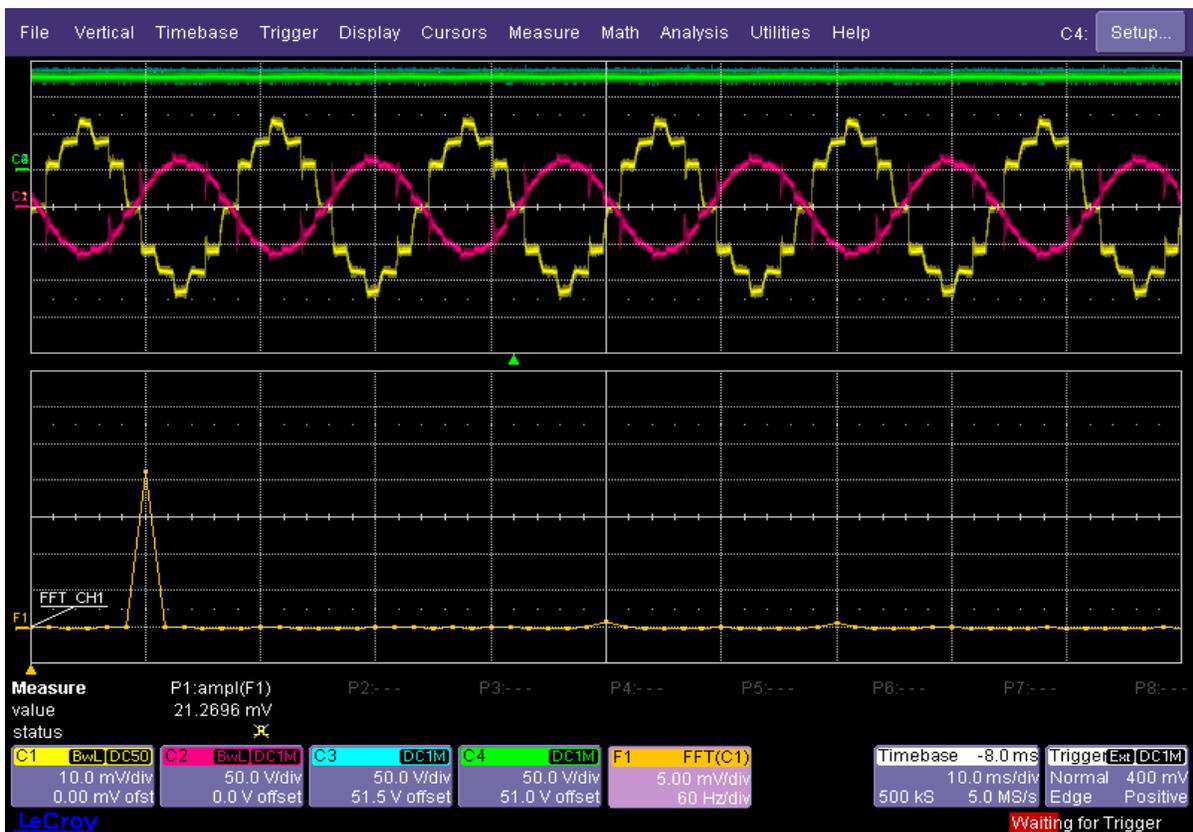
Figure 36. α = 167°. 5th and 7th harmonics minimized
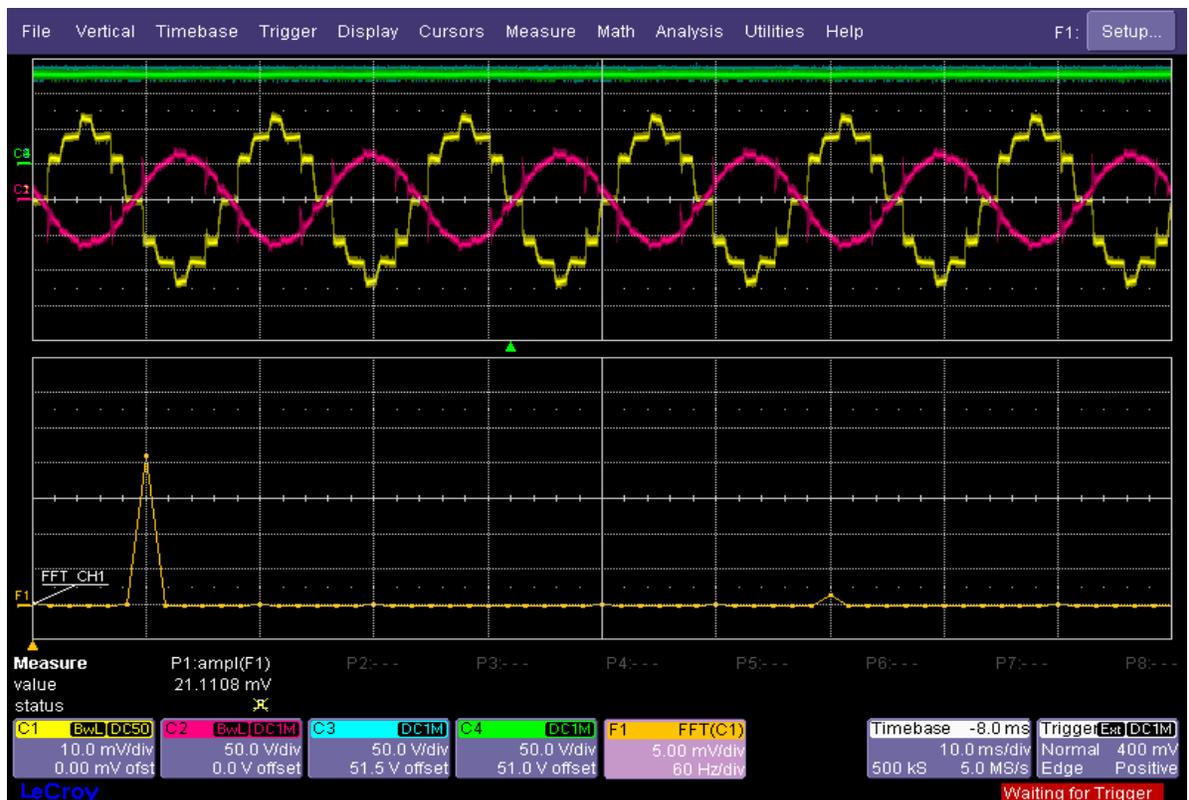
Figure 37. α = 164.4°. Zero of 5th harmonic
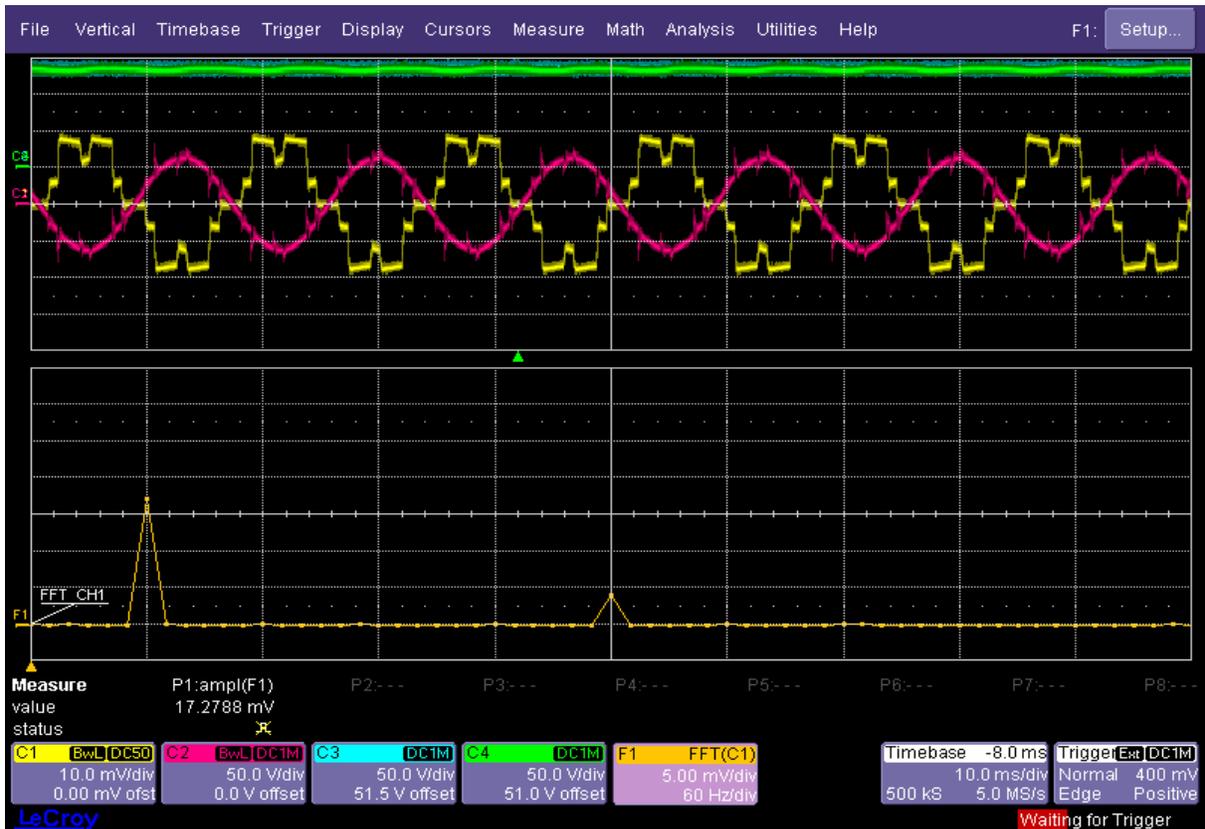
Figure 38. α = 143.9°. Zero of 7th harmonic
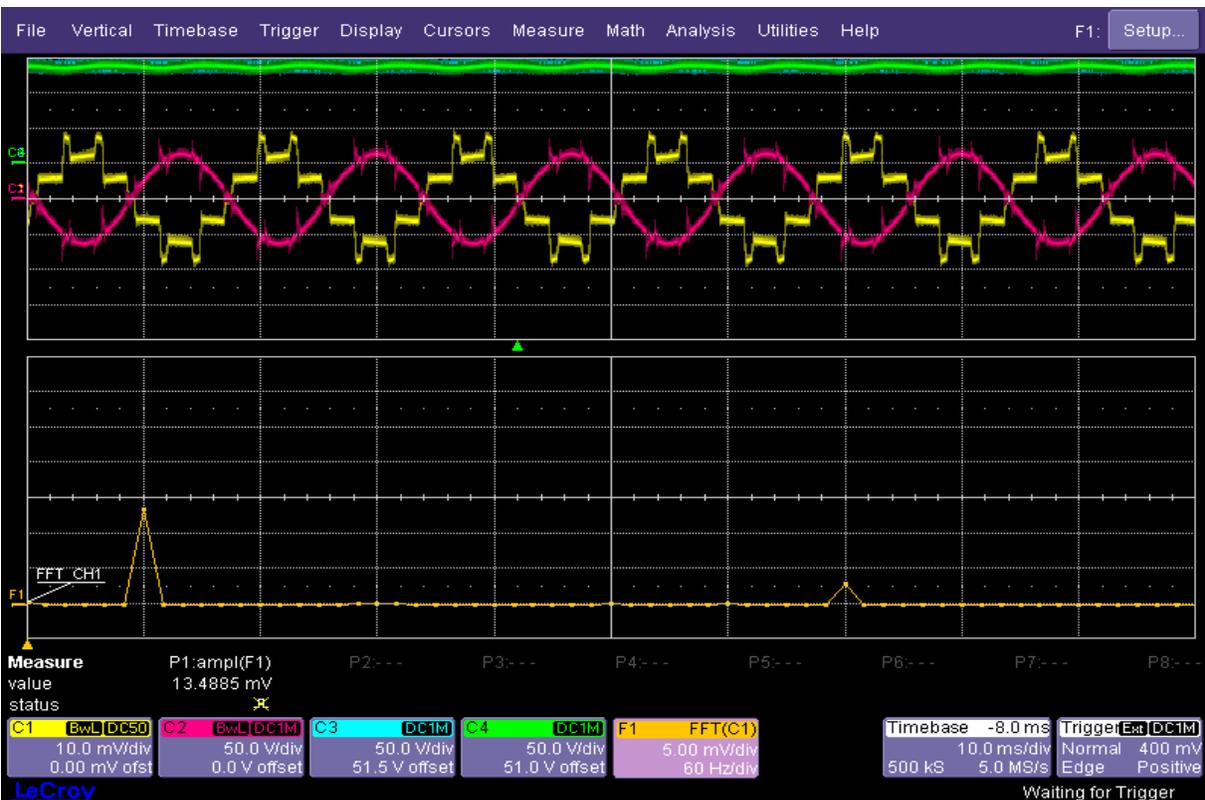
Figure 39. α = 129.5°. Zero of 5th harmonic
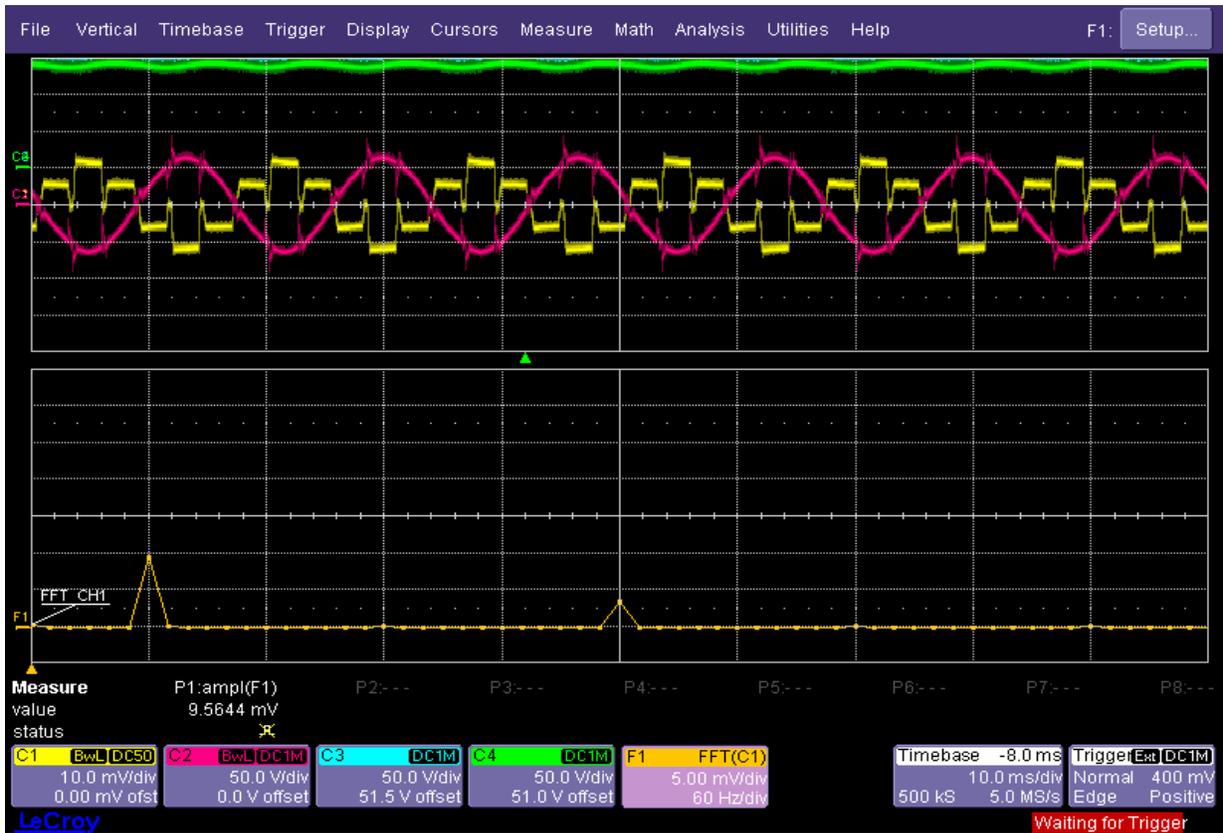
Figure 40. α = 120°. Zero of 7th harmonic
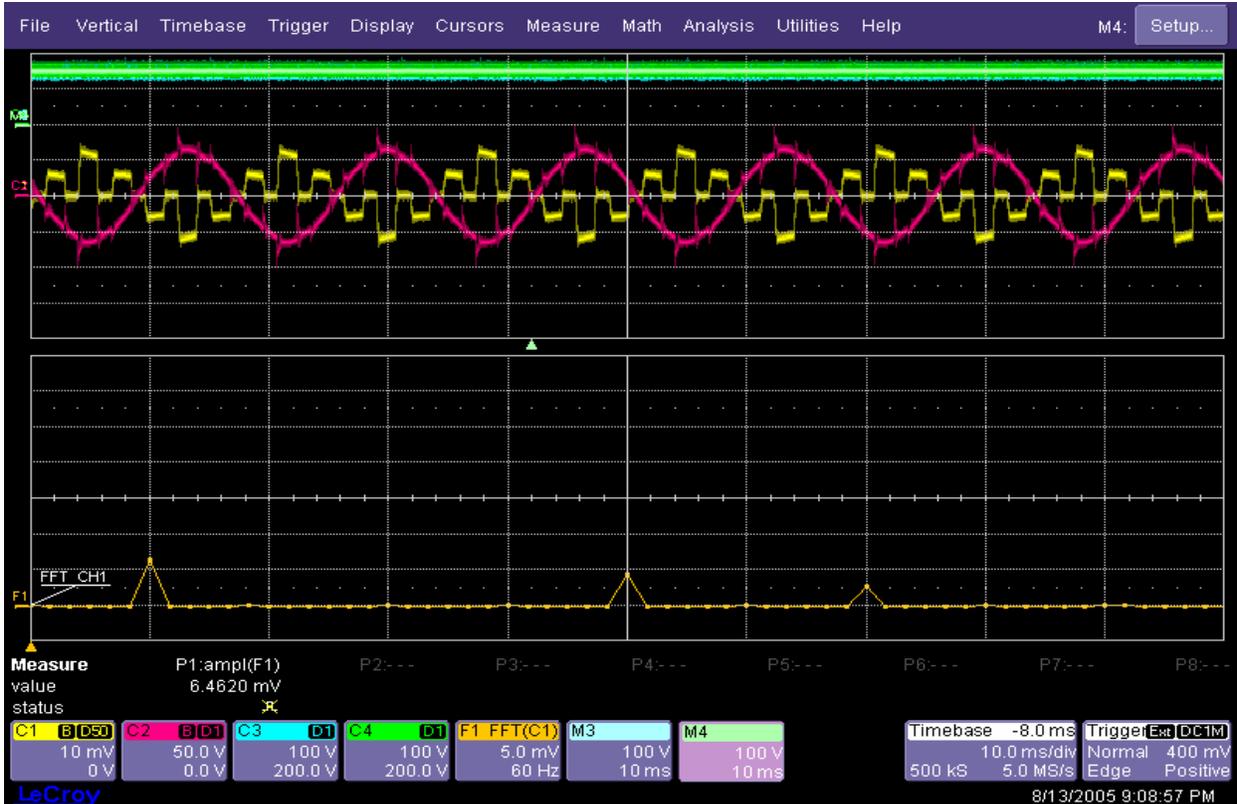
Figure 41. α = 111°. 5th harmonic greater than the 7th
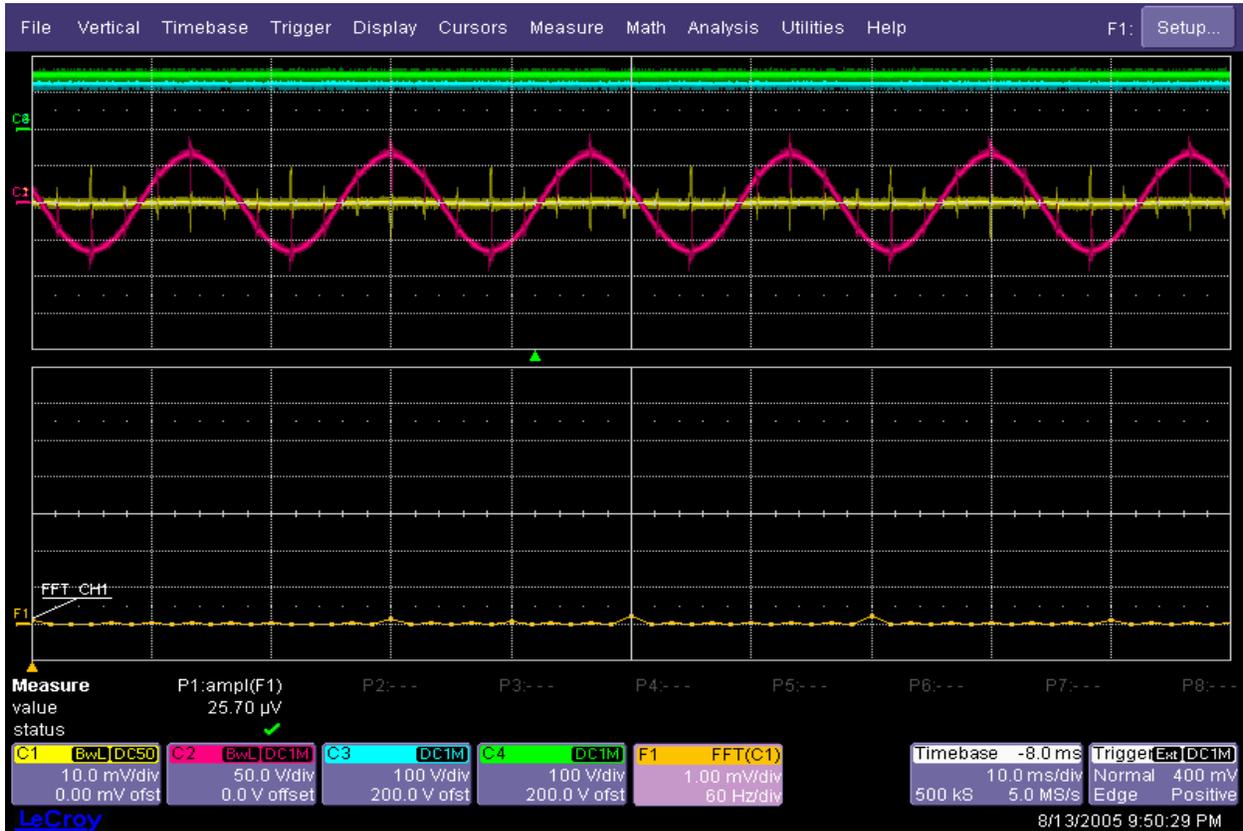
Figure 42. $\alpha = 94.7°$. **The grid phase current is negligible**
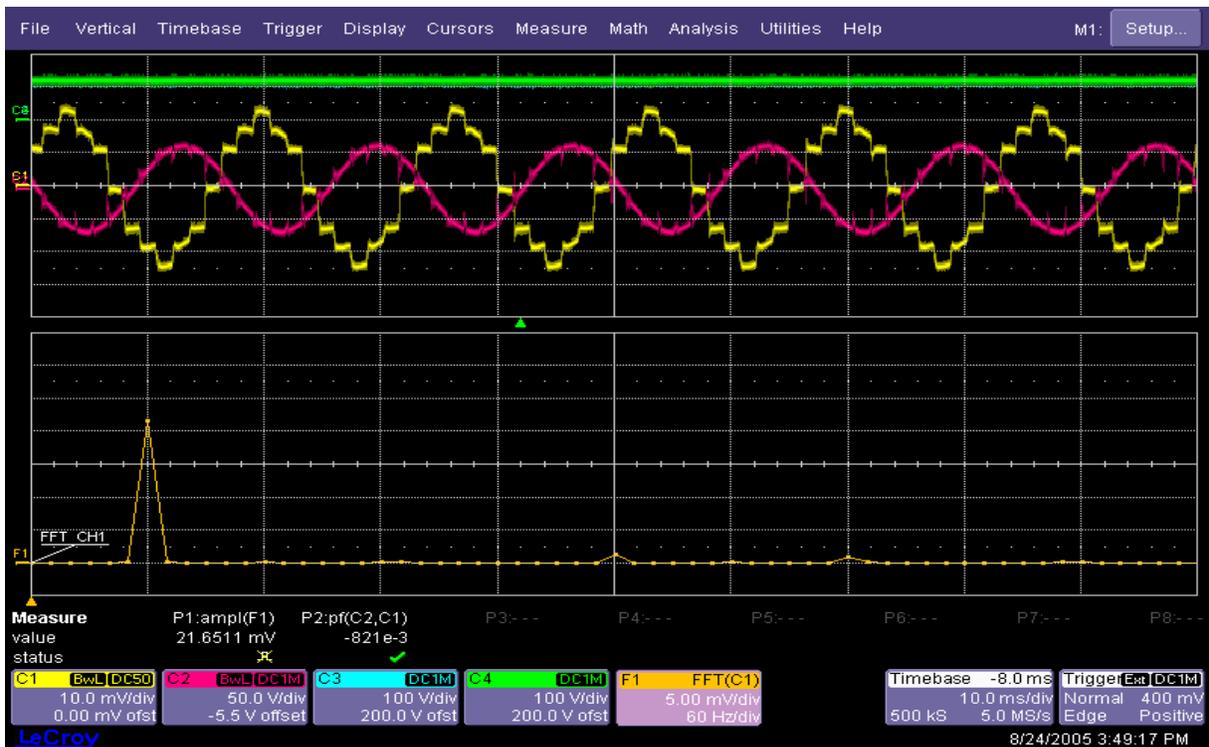
Figure 43. $\beta = 30°$. **PF leading**

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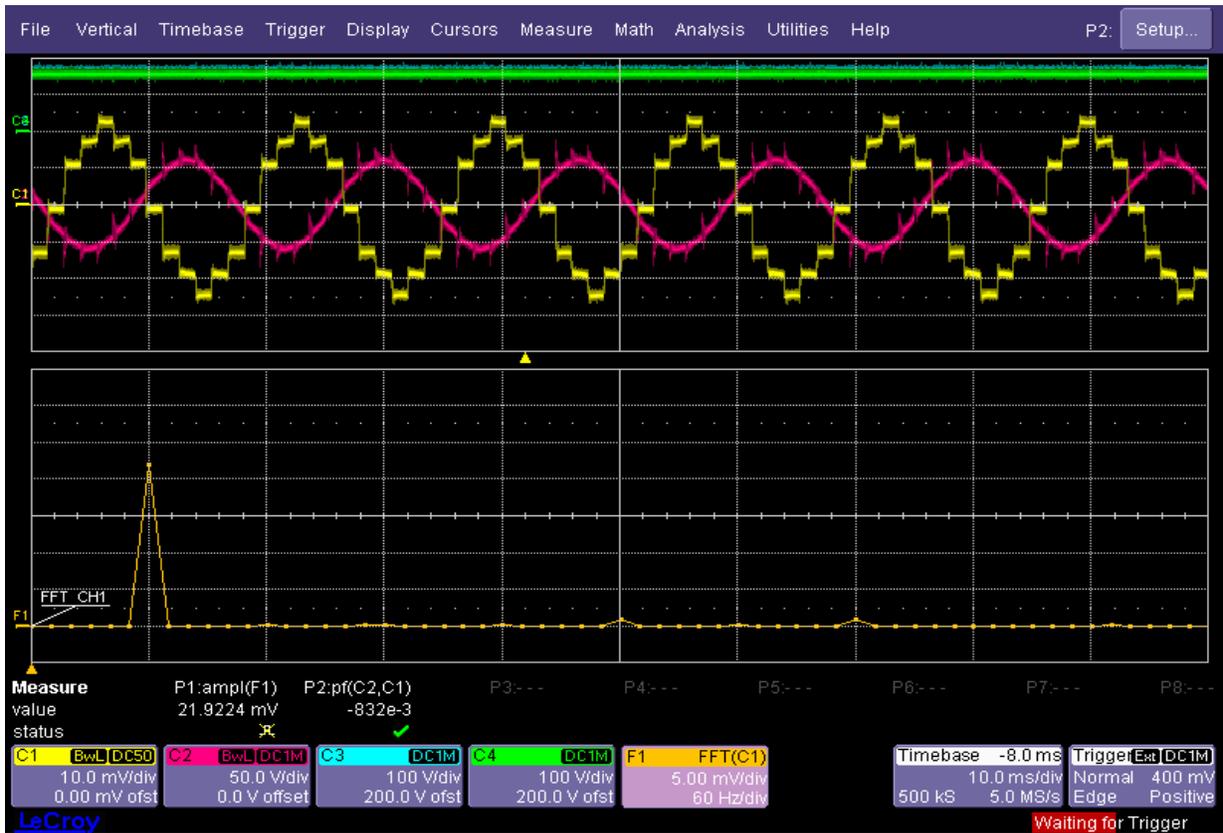
Figure 44. β = -30°. PF lagging
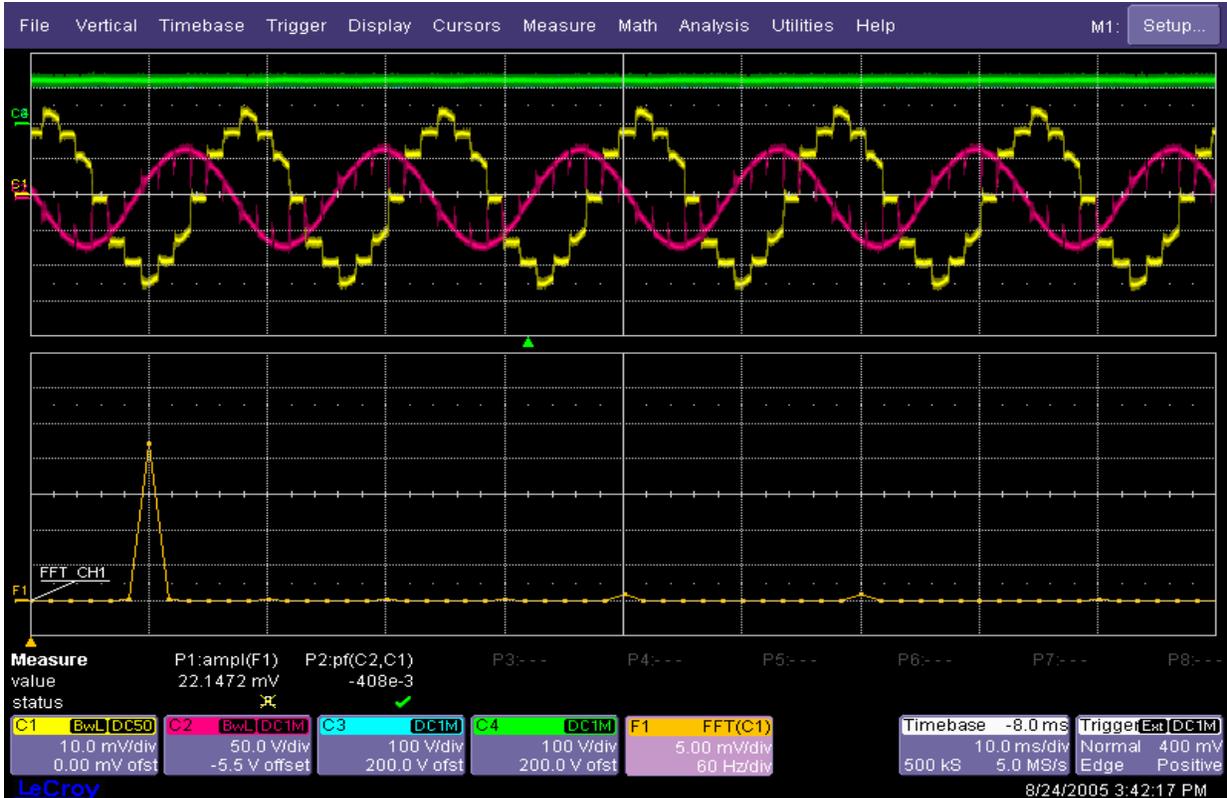
Figure 45. β = 60°. PF leading
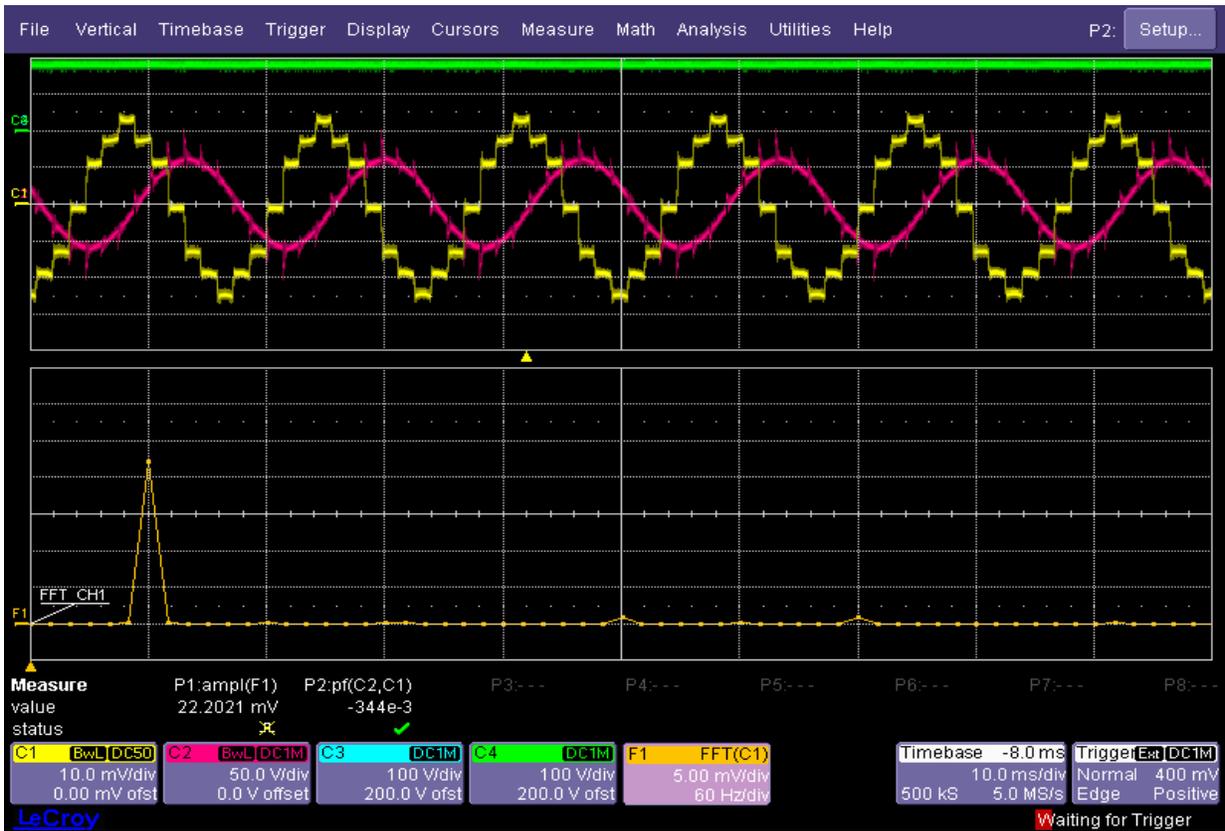
Figure 46. β = -64.6°. PF lagging

Figure 47. β = 89.9°. PF leading

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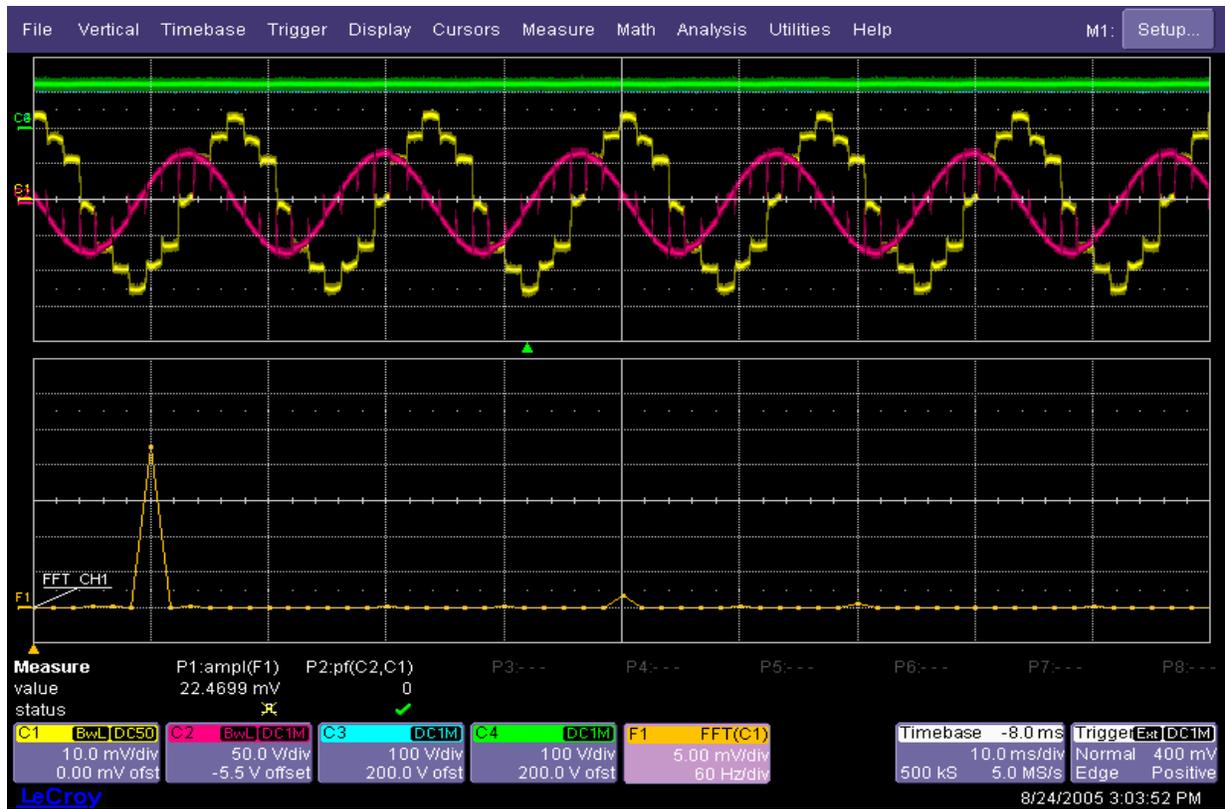
Figure 47 shows a transient response for a step in the DC-link current command from 1 A to 10 A, while Figure 48 shows the opposite transient from 10 A to 1A. The other operating conditions are the same. The yellow waveform is the grid current (20 A/div.) while the magenta waveform is the DC-link current (2 A/div.).

Figure 48. Transient from 1 A to 10 A of DC-link current at <Vdc> = 328 V, 1464 rpm
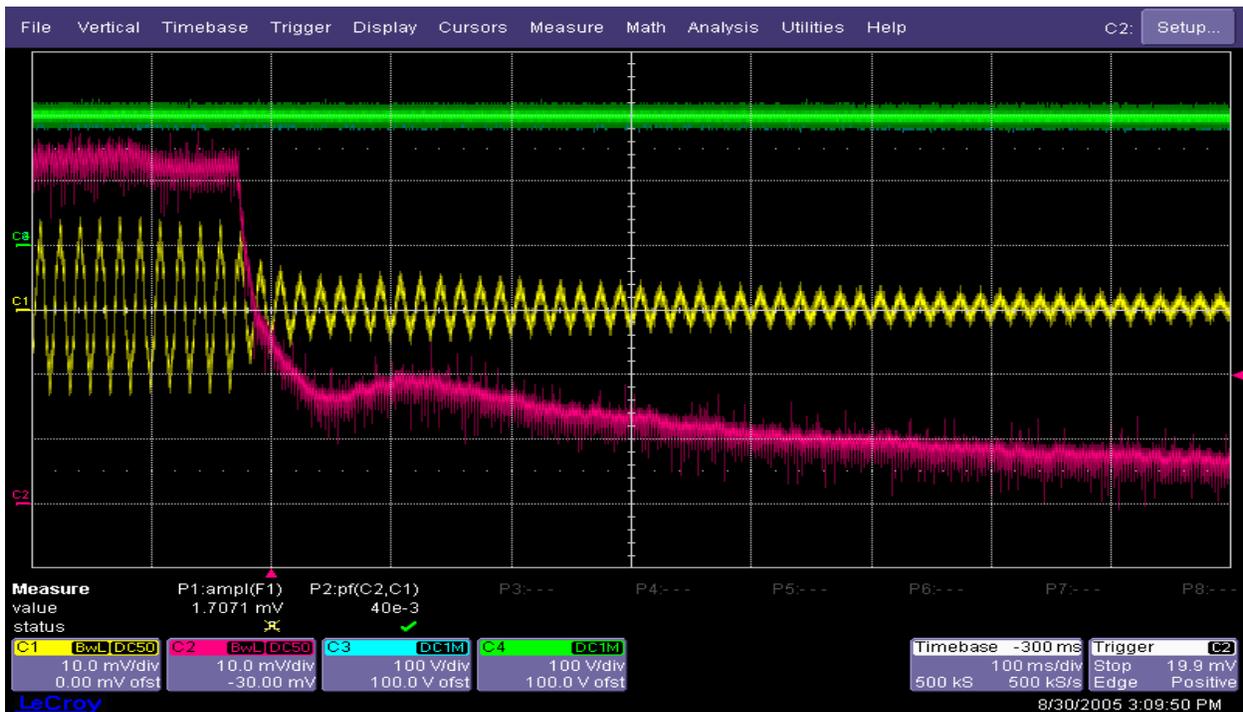
Figure 49. Transient from 10 A to 1 A of DC-link current at <Vdc> = 328 V, 1464 rpm

Suggestions for Future Work

The investigators suggest that the DSP-implementation and the test of the variational control method described in this text be applied to the active harmonic compensator. This method could be applied in a more general context for current control of any type of power electronic power converter.

Conclusions

The proposed line-frequency switched CSI topology allows the use of high-power, slower devices, making it suitable for high-power applications. This topology is particularly well suited for wind-power applications as only the generator and rectifier bridge (consisting of very reliable diode semiconductors) are located in the nacelle, and the two DC link cables that run from the nacelle to the ground can contribute to a significant portion of the DC link inductance. The axial flux PM generator allows the realization of a gearless turbine and greatly improves the reliability of the generator because it does not require external or brushless excitation. With the proposed control scheme, the topology can simultaneously provide relatively low line current harmonics at the grid while producing either leading, unity, or lagging power factor. These features are already achieved without using the active harmonic compensator. The possible use of a harmonic compensator would decrease the harmonic content further and, because control of the reactive power at fundamental frequency is provided by the control angle β, it needs to be designed and rated only for the harmonic components above the fundamental component.

Published Papers Related to the Project Activities

1. Tenca, P.; Lipo, T.A. "Reduced cost current-source topology improving the harmonic spectrum through on-line functional minimization." *Power Electronics Specialists Conference, 2004*. Vol. 4, 2004; pp. 2829-2835.

2. Tenca, P.; Lipo, T.A. "Synthesis of desired AC line currents in current-sourced DC-AC converters." *Second International Conference on Power Electronics, Machines and Drives, March 31 - April 2, 2004*. Conf. Publ. No. 498., Vol. 2; pp. 656-661.

3. Tenca, P.; Lipo, T.A. "A decentralized protection scheme for converters utilizing a DC-link inductor." *Industrial Electronics Society, 2005. IECON 2005*. 32nd Annual Conference of IEEE November 6-10, 2005; pp. 854 – 859 (to appear in *IEEE Transactions on Industrial Electronics*).

4. Tenca, P.; Lipo, T.A. "Conversion Topology for Reducing Failure Rate and Life-cycle Costs of High-Power Wind Turbines." ASME-AIAA Wind Energy Symposium, pp. 111-122, 2005.

Appendix

Publication [3] in the above list of references refers to a passive circuit developed to protect the DC-link inductor against dangerous overvoltages and/or overcurrents potentially occurring after a fault. This circuit was not specified in the original proposal but was developed as a portion of this project as an additional effort. Because the description of such a circuit would have diverged quite considerably from the main topic of this report, it is included here as an appendix.

A Decentralized Protection Scheme for Converters Utilizing a DC-link Inductor

Pierluigi Tenca

University of Wisconsin-Madison
Engineering Hall, 1415 Engineering Drive
Madison, WI, 53706 U.S.A.
tenca@cae.wisc.edu

Thomas A. Lipo

University of Wisconsin-Madison
Engineering Hall, 1415 Engineering Drive
Madison, WI, 53706 U.S.A.
lipo@engr.wisc.edu

Abstract – **This paper proposes a fully passive protection scheme for DC link inductors whose topology is characterized by the circuit having a substantial distance between the rectifier and inverter stations. Inductors of this type can be found intrinsically in very long high-power cables - as in HVDC transmission for example - as well as in DC-links for high-power current source inverters. In such applications the inductor must be duly protected against overvoltages as well as against overcurrents potentially occurring as consequence of an open-circuit or a short-circuit fault respectively. The distance between the inductor terminals prevents the use of well-known localized protections like, for example, simple freewheeling diodes. A key role in the protection scheme proposed by the authors is played by the largely available transient suppressor diodes (often commercially identified as "Tranzorbs") and the solution is kept very simple and reliable by employing only rugged diodes and thyristors. The protection relies only on the energy stored in the inductor without the need of any external supervision circuit or any information exchange between the distant inductor terminals. Experimental results are presented and a generalization of the scheme to a broader application is also introduced.**

I. INTRODUCTION

Often it is necessary to protect the insulation and mechanical integrity of large DC link inductors from damage caused by excessive overvoltages and/or overcurrents usually arising from open-circuit or short-circuit faults respectively. Such large inductors are a very expensive and important parts of the systems in which they operate. For this reason the task of designing a proper protection scheme for them must not be underestimated.

Often large DC current link applications are characterised by the fact that their terminals are located at very considerable distance apart (even several kilometers) as Figure 1 shows. The most common practical case occurs when the effective distribution of the inductance is over long distance, as may occur for high-power transmission cables or for inductors used as DC-link in high power current source inverters / rectifiers [1].

The inductors in Figure 1 have been drawn to call attention to the distributed nature of their inductance which is always a property of the overall loop in which the inductor current flows. Often the inductor constitutes the DC-link of current source converters in which the current i_L as well as the voltages v_A and v_B do not change sign.
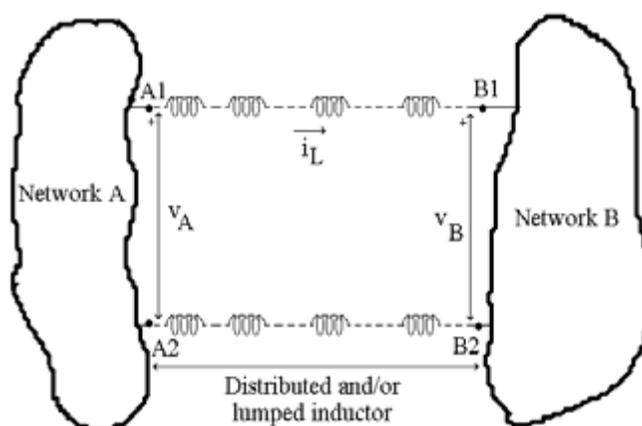
Fig. 1. Situation in which the effective terminals of a DC link inductor are distant from each other.

The distributed nature of the inductance leads one to approach the problem of protection of such inductors in a decentralized manner. Firstly, it is useful to observe that ultimately the portion of electrical network needing protection is the quadrupole A1-A2-B1-B2 identified in Figure 1 and not only a simple bipole.

As consequence the common protection against open-circuit faults constituted by a simple freewheeling diode can not be applied effectively. Indeed it is sufficient to observe that the effectiveness of two possible freewheeling

diodes, one connected between the terminals A1 and B1 and the other between A2 and B2, would be jeopardized by the unavoidable large inductances of the diodes connections to A1 (A2) and B1 (B2). The magnitude of such undesired inductances would arise naturally as consequence of the large distance between the converter terminals. Furthermore a freewheeling diode would not provide any protection against overcurrents or overvoltages possibly arising at the ports A1-A2 and B1-B2 of the quadrupole.

In order to be as more reliable as possible, the protection scheme should be kept as simple as possible, since every added complexity introduces an additional risk of malfunction which is less and less tolerable as the cost of the inductor increases. In particular the protection scheme should possess the following features:

- Absence of any external supervision circuit.
- Independence from any external energy source.
- Capability to operate using only the energy stored in the inductor.
- Absence of information exchange between the two distant ports A1-A2 and B1-B2.

II. PROPOSED PROTECTION SCHEME

As mentioned, it is common that the inductor represents the DC-link of high-power current source converters with the quantities i_L, v_A and v_B having constant sign that can be assumed positive under normal operating conditions. Unless stated otherwise these assumptions will be at the basis of the subsequent discussion.

All quantities i_L, v_A and v_B clearly have design limits and considering the requirements listed in the previous paragraph the authors propose the circuit solution shown in Figure 2 as a decentralized protection scheme. The symbols F_{A1}, F_{A2}, F_{B1}, F_{B2} represent fuses that might be fast-acting or slow-acting depending on the application. The tripole identified as "Thyristor trigger circuit" senses the voltage v_B and triggers the thyristor T_B whenever v_B exceeds the design value considered as the symptom of a fault.

Observing Figure 2 it is possible to analyze how the protection scheme operates in the different possible fault conditions.

I) An open-circuit fault either occurring in network A or consequence of the intervention of fuses F_{A1} and/or F_{A2}, causes the current i_L to flow into the diode D_A and the voltage v_A to equal the negative forward voltage drop of D_A. The current i_L decreases after the fault because of the action of the voltage v_B.

II) An open-circuit fault either occurring in network B or consequence of the intervention of fuses F_{B1} and/or F_{B2}, causes the voltage v_B to rise until its fault value is reached. At this instant the thyristor T_B is ignited through the trigger circuit and the terminals B1 and B2 are almost short circuited.

If the positive voltage v_A is not reduced considerably after this event, the current i_L raises under its presence until at least one of the fuses F_{A1} and F_{A2} intervenes, because its time-integral of the current squared has been exceeded. In this case the current i_L is diverted to flow in D_A.
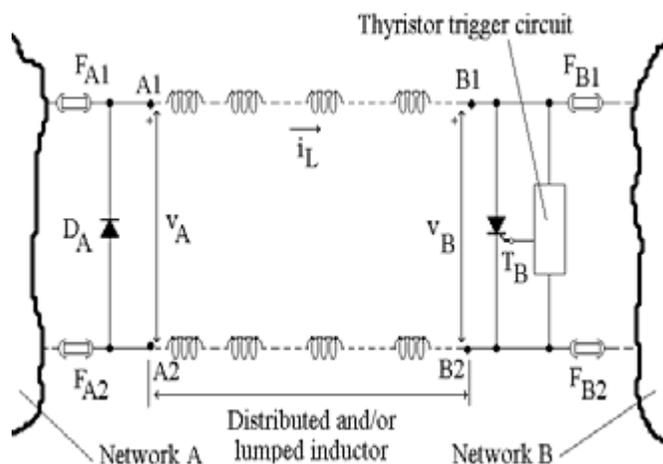
Fig. 2. Basic principle of decentralized protection scheme.

The short circuit produced by the thyristor T_B at the port B1-B2 ultimately leads to the intervention of at least one of the fuses F_{B1} and F_{B2} unless additional possible – but not required - protection policies operating on the network B prevent this from happening. If this is not the case the ultimate operating mode of the inductor is the one in which the current i_L may flow in D_A and T_B only while its value decreases towards zero under the action of the forward voltage drops of these devices.

III) Any faulty operating condition creating an overcurrent i_L which exceeds the I^2t rating of the fuses will ultimately melt at least one of them. As consequence, from that instant onwards the protection scheme behaves like one of the previous cases I or II.

The scheme provides also fast protection for the inductor against overvoltages at port B1-B2 because such an event invokes the intervention of the thyristor trigger circuit and the consequent behaviour as described by the previous case II. On the other hand an overvoltage condition at the port A1-A2 is detected indirectly and with slower dynamics because it must create a rise of the current i_L or - if a controls system for i_L is present in the network B - an elevation of the voltage v_B.

This differentiation between the mode of intervention for overvoltages in v_A and v_B is justified by the hypothesis under which this principle scheme has been developed. Indeed when the inductor constitutes the DC-link of a current source converter operating with positive i_L, v_A and v_B, as assumed, the network A, which is the generating side, may be more affected by short spike voltages that should be ignored.

It should be observed that the proposed scheme strongly favors the protection of the inductor over the networks A and B. This choice arises from the original assumption that the inductor is a highly valuable component whose integrity and survivability deserve the highest priority.

III. STRUCTURE OF THE THYRISTOR TRIGGER CIRCUIT

Thus far only the function of the thyristor trigger circuit has been addressed but not its detailed structure and accompanying design choices. First of all it should be observed that when the occurring faulty condition ultimately leads to the operating mode II described in the previous section, the inductor current i_L cannot be diverted instantaneously into the thyristor T_B because of its finite commutation time. Consequently the thyristor trigger circuit must be able to withstand the entire fault value of i_L until T_B goes in full conduction.

Additionally, in general, it is not possible to identify a single value of i_L that could be used as decisive threshold for triggering the thyristor. This is because an open circuit fault in network B could occur for reasons completely independent from i_L and its value. These observations together with the requirements listed at the end of section I restrict the set of possible components that can be used in the trigger circuit.

The authors have adopted the structure and components shown in Figure 3 to realize the trigger circuit enclosed in the red rectangle for sake of clarity. In order to satisfy the requirement of operating only with the energy stored in the protected inductor, the circuit employs only passive components and does not require any external energy source.

It should be further observed that such a feature is very important because it assures protection even in case of catastrophic fault of the entire system, with consequent loss of all energy sources. In a scenario like this, one can rely only on the energy stored in the inductor. The trigger circuit uses only the local information represented by the voltage v_B and does not require other additional external supervision circuits.

The key detail for the correct circuit operation is the utilization of the nowadays widely available unidirectional Transient Voltage Suppressors (TVS) diodes which are often denominated with the conventional name of "Tranzorb". These components clamp the voltage to a maximum value close to their nominal one with effects similar to a zener diode. Nonetheless, very differently from the zener diodes, they can withstand and dissipate very high instantaneous powers for few microseconds and, furthermore, their first failure mode is guaranteed to be a short circuit [2].

Tranzorbs rated for 1.5 kW – 3kW of dissipated power are commonly produced by many manufacturers and nowadays devices rated for 30 kW and 6 kA peak current are emerging produced, for example, by Sussex Semiconductors [3]. The manufacturer usually specifies the waveform of the surge current that a Tranzorb can withstand safely as an asymmetrical bell-shaped curve having a rise time of 10 μs and a fall time, to ½ of the peak current, of 1000 μs.
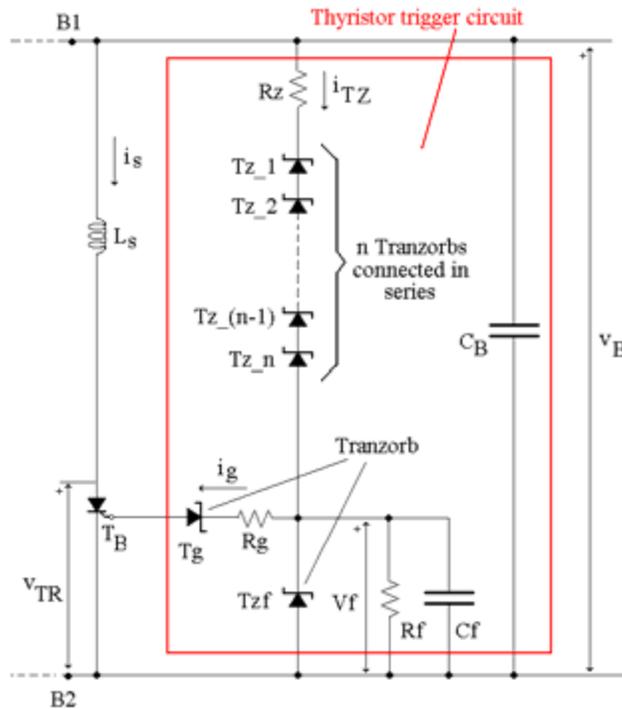
Fig. 3. Structure of the fully passive thyristor trigger circuit.

The nominal peak surge current is roughly equal to the rated power of the device divided by its nominal clamping voltage. The Tranzorbs are widely used as protection devices against overvoltages (especially induced by lightning) since they can clamp the voltage much more effectively than Varistors [4]-[5] and they are guaranteed to fail as a short circuit providing an ultimate protection that is generally used to blow a fast-acting fuse.

The features of the Tranzorbs are particularly suitable for the thyristor trigger circuit because they are components of reduced size which are nevertheless able to withstand a large impulse current. This is exactly the situation occurring in the trigger circuit inside the time interval between the inception of the fault and the instant when T_B goes in full conduction. In this interval the surge current i_{TZ} in the Tranzorbs becomes higher than i_L and the devices must be chosen so that their peak current is not lower than the maximum i_L that can occur in the worst case fault condition. Zener diodes could not be used as substitute of Tranzorbs because there is no guarantee on their clamp voltage and failure mode for peak currents well above their absolute maximum rating.

Following these considerations, it can be observed in Figure 3 that the branch composed by the series of low-value resistor Rz, Tranzorb Tzf and n Tranzorbs Tz_1 – Tz_n, constitutes a path in which the inductor current i_L can flow - until T_B reaches the full conduction - without risk of being abruptly interrupted with consequent onset of potentially destructive values of v_B. The number of Tranzorb diodes in series implies the maximum overvoltage for v_B after which the circuit ignites T_B. As soon as a specific Tranzorb device has been selected according to additional criterion, such as availability for example, the desired maximum v_B determines the number n+1 of devices needed in series.

The layout of the trigger circuit must be as compact as possible and lie as close as possible to the port B1-B2 in order to minimize the parasitic series inductance on the path of i_L. To relax in some extent such a requirement and to protect T_B against excessive dv_B / dt the very low series impedance capacitor C_B is introduced and it is mounted as close as possible to the T_B terminals.

From Figure 3 one can infer the succession of events which lead T_B into conduction after an open circuit fault of type II. Before the fault inception the voltage v_B has a positive value lower than the threshold defined by the number of Tranzorbs in series and their avalanche voltage. As soon as the open circuit fault occurs the current i_L flows into the capacitor C_B and the voltage v_B raises linearly up to the maximum clamping voltage defined by the series of n Tranzorbs Tz_1 – Tz_n. At such instant these Tranzorbs conduct and the voltage v_B remains almost clamped. As consequence, the current i_{TZ} becomes equal to i_L because the capacitor voltage is practically constant. Not later than when the voltage of the small filtering capacitor Cf reaches the clamping voltage of the Tranzorb Tf, a gate current ig appears and its peak is set by the difference of the clamping voltages of Tzf and Tg as well as the resistor Rg. As soon as ig exceeds the thyristor gate trigger current, T_B reaches the full conduction after the delay time specified by the manufacturer which is usually below 5 μs. At this point the thyristor current i_S starts to rise with a slope

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determined by the clamping voltage of the series of Tranzorbs and the turn-on snubber inductance Ls. The inductor Ls must always be present to limit the maximum di/dt for which the thyristor is rated. Ultimately i_S will become equal to i_L, i_{TZ} will drop to zero ending so the commutation process and the surge current in the Tranzorbs. It is important to choose a thyristor whose I^2t is greater than the one characterizing the fuses chosen. By selecting properly the components the whole area of the pulse current in the Tranzorbs remains easily inside the safe limits specified by the manufacturer.

IV. EXPERIMENTAL SETUP AND RESULTS

An experimental setup has been built to test the effectiveness of the proposed protection circuit. The setup is part of a wider one aimed at testing topologies for high power wind turbines. Figures 4 and 5 show the portion of the setup regrouping the power semiconductors and thyristor trigger circuit while the 67 mH inductor to be protected is not shown because collocated far away from the other components.

The components shown in Figure 2 and 3 are highlighted in figures 4 and 5 for sake of explanation and clarity. The capacitor C_B is composed by one extremely low inductance 470 nF snubber capacitor mounted directly on the terminals of the thyristor T_B together with additional two 1nF and 600 pF capacitors mounted on the trigger circuit board. The Tranzorb Tz_1 – Tz_n and Tzf used are devices 1N6284A (1.5KE36A) rated for 1.5kW and 36 V breakdown voltage while the Tranzorb Tg is a 1N6272A (1.5KE11A) rated for 11.5 kW and 11 V breakdown voltage.
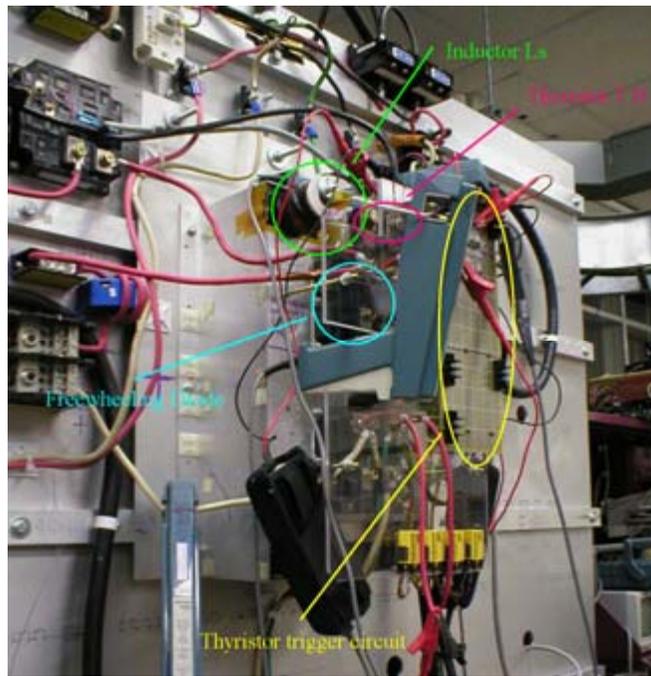
Fig. 4. Particular of the experimental setup.
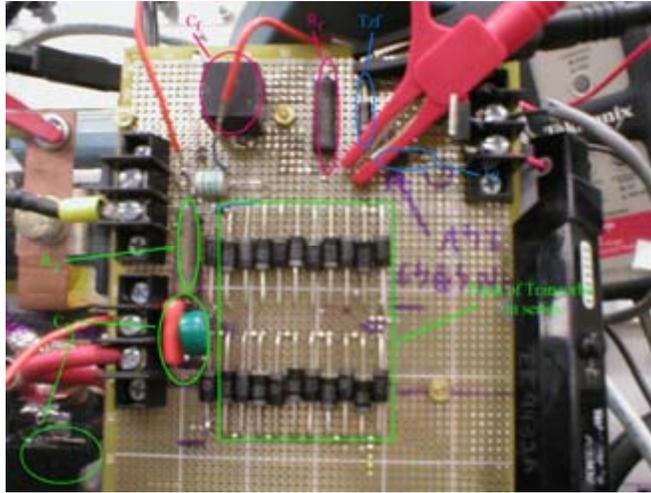
Fig. 5. Detail of the thyristor trigger circuit showing the components.

On the trigger board shown in Figure 5 there are two groups of 11 Tranzorbs each, all connected in series, for a total possible breakdown voltage of 792V. In the test performed only one group has been used setting so the intervention voltage of the trigger circuit was close to 400 V. The resistor Rf and the capacitor Cf have values of 100 Ω and 0.1 µF respectively, both selected for low inductance. The resistors Rg and Rz are 22 Ω and 1 Ω respectively, again both are antiinductive. The thyristor T_B is a device TD310N from Eupec and the turn-on snubber inductance Ls used has a value of 30 µH to limit the di/dt at 13.4 A/µs (with 400V maximum V_B voltage) well below the 120 A/µs which is the device limit.

Two LeCroy digital scopes have been used to perform the measurements. The first scope, a model LT354, (four channels, 500 MHz) is used to monitor the waveforms of the trigger circuit v_{TR} (CH1,blue), i_{TZ} (CH2,green), Vf (CH3, red) and ig (CH4, magenta) and a capture of its screen during a test with i_L = 10 A is shown in Figure 6. The second scope, a model 9304 (four channels, 175 MHz) monitors the waveforms v_A (CH1, magenta), i_L (CH2,blue), v_B (CH3, red) and i_S (CH4, green). The two scopes were connected with the 9304 acting as trigger master on the voltage v_B and the LT354 as trigger slave
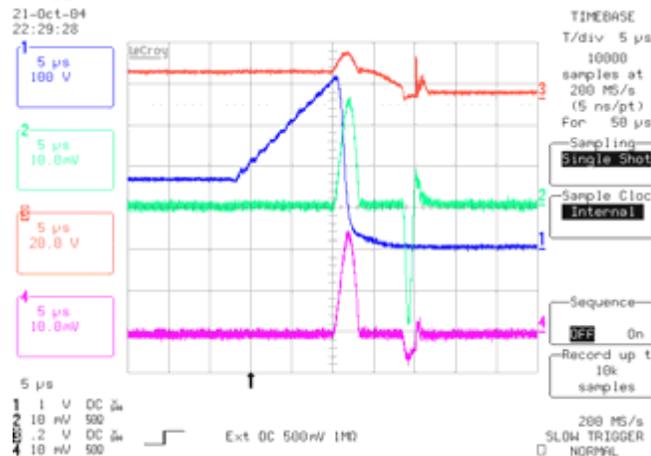
Fig. 6. Display of the LT354 scope with waveforms of the trigger circuit.

Two tests were performed on the experimental setup and in both the network A was constituted by a six-pulse diode rectifier whose input was a 60 Hz three-phase symmetrical system of sinusoidal voltages regulated in amplitude by a Variac. The network B was a 16 Ω power resistor. Between the network A and the fuses F_{A1}, F_{A2}, as well as between the fuses F_{B1},F_{B2} and the network B, solid state switches (high-power IGBTs) were inserted to realize very "clean" open-circuit fault conditions.

The first test was performed by creating an open-circuit condition at the port B1-B2 after that the inductor current i_L had reached the steady state value of 10 A. The scopes were triggered for a 200V value with positive slope sensed on the voltage v_B and the waveforms recorded on a time base scale of 5 µs/div are shown in Figure 7. The upper graph of Figure 7 presents the waveforms of v_A, i_L, v_B, i_S recorded by the scope 9304 while the waveforms of v_{TR}, i_{TZ}, Vf, ig recorded by the scope LT354 are presented in the lower graph.

By analyzing the traces it is possible to observe the operation of the circuit. After the open circuit occurs at the port B1-B2 The voltage v_B raises linearly starting from about 160 V. When it reaches a value close to 400 V the Tranzorbs Tz_1 – Tz_n begin to conduct. Simultaneous and equal peaks occur in the currents i_{TZ} and ig starting at +10 μs because the Tranzorb Tg (11 V) allows the flow of the gate current before than Vf reaches the clamping value of 36V.
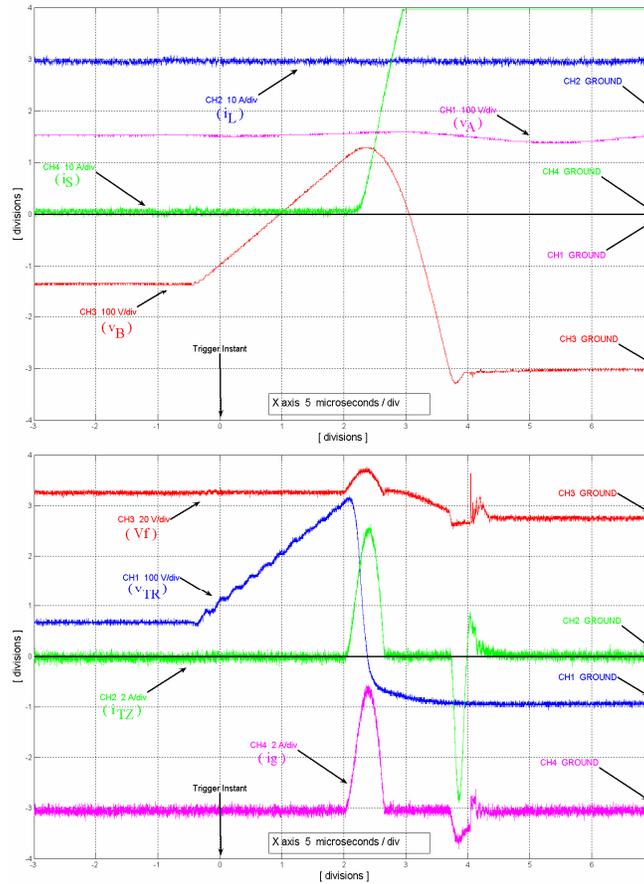
Fig. 7. Waveforms for the test with 10A of inductor current.

The thyristor voltage v_{TR} drops abruptly after ig has reached the ignition value. As consequence of the short-circuit created by T_B the capacitor C_B begins a discharge thyristor transient current through L_S and indeed one can observe that the ramping in the current i_S due to this event. After L_S has been charged, it will perform a partial discharge transient also in the series connection of all Tranzorbs until i_S assumes the same value of i_L.

During this transient the Tranzorbs are directly polarized acting as normal diodes. The negative peak observable in i_{TZ} is due to this process. It is important to observe that the waveform of the current i_L does not show any appreciable transient, confirming that i_L commutates smoothly from the network B to the short circuit created by the triggered thyristor T_B; i.e. the protection scheme has accomplished its task of preventing abrupt changes in the inductor current.

The second test performed was aimed at testing the effectiveness of the protection in case the inductor current i_L was of limited value, i.e. in the range of tenths of Amperes. Figures 8 and 9 show the waveforms of i_L, v_B, i_S recorded during this test repeated on two different time base scales. In Figure 8 one can observe that although the open circuit fault occurs when i_L is small, nevertheless, v_B rises and fires the thyristor through the trigger circuit.

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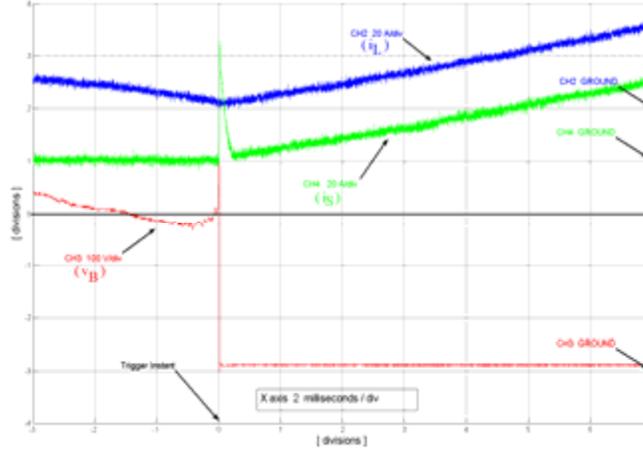
Fig. 8. Waveforms for the test with low inductor current.
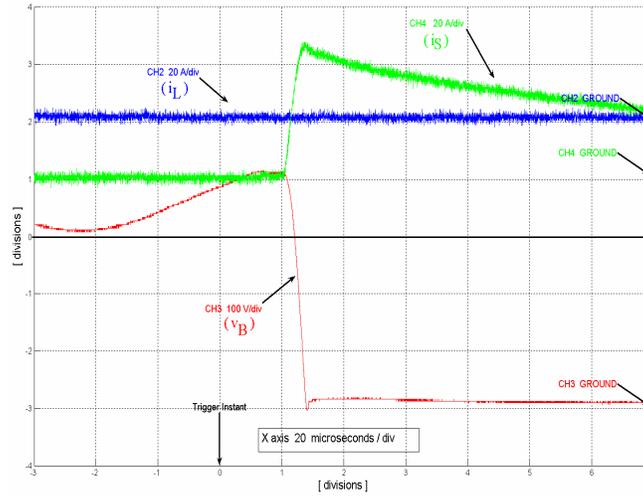
Fig. 9. Test with low inductor current repeated with magnified time base.

The waveform of i_S shows a peak due to the discharge of C_B through the thyristor as explained before. Subsequently i_S decreases by flowing in the directly polarized Tranzorbs until it reaches the same value of i_L. The peak of i_S, its subsequent decrease and the evolution of v_B are magnified in Figure 9. The inductor remains always connected to the voltage source at the port A1-A2 while the thyristor T_B provides the recirculation path for the current i_L. As consequence the inductor currents i_L and i_S begin to rise as clearly shown by Figure 8 and ultimately i_L would provoke the intervention of at least one of the fuses F_{A1}, F_{A2} and the diode D_A as explained in section II, thereby completing the sequence of events for the protection of the inductor.

V. GENERALIZED PROTECTION SCHEME

The protection scheme presented in the previous sections was shown to be valid for unidirectional power flow from network A to network B when the current i_L as well as the voltages v_A and v_B assumed only positive values. The authors consider it worthwhile to propose a generalization of the scheme able to operate also in the common cases where a bidirectional power flow is required by reversing the signs of the voltages v_A and v_B while i_L continues to remain always positive.

The generalized protection scheme under these assumptions is shown in Figure 10. The group composed by the thyristor T_B and its trigger circuit has been replicated at the port A1-A2 but its polarity has been reversed to allow the flow of the current i_L during a fault condition. The unidirectional voltage blocking capability of the chosen Tranzorbs imposes one additional diode (Dta, Dtb) be provided in series to each trigger circuit at both ports. Without this diode the voltage at each port could not reverse its polarity because the Tranzorbs would immediately enter the forward conduction mode.

In the worst fault case, during a hypothetical simultaneous open circuit fault at the ports A1-A2 and B1-B2, the current i_L will flow initially in the capacitors C_B of both trigger circuits until sufficient capacitor voltages are reached

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to ignite the thyristors T_A and T_B. It is worthwhile to note that the capacitor voltages rise independently and simultaneously because the path provided by them is the only one in which i_L can flow initially.

As consequence T_A and T_B are eventually ignited, but always independently, and still without the need of any communication between the circuits located at the two ports. As well it is possible to observe how this protection scheme provides overvoltage protection of both signs although each specific port is capable of sensing only one specific voltage polarity.
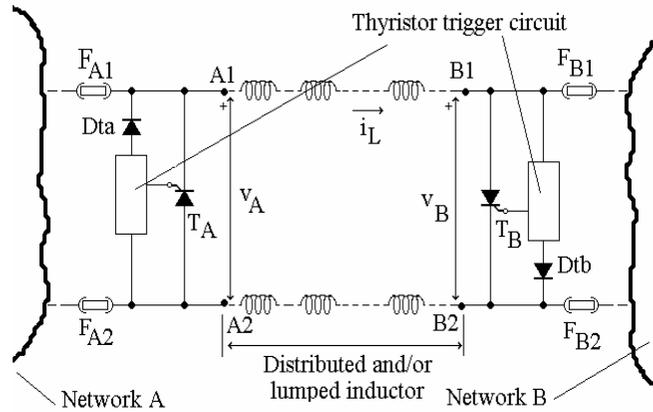
Fig. 10. Decentralized protection scheme for bidirectional power flow.

VI. CONCLUSIONS

A decentralized protection scheme designed to protect geometrically large DC-link inductors from overvoltages and overcurrents has been presented. The protection of the DC-link inductor is considered as a priority choice in case of fault. The proposed protection scheme does not require any supervision circuit or communications between the distant terminals of the inductors to be protected and uses passive devices only, without any need of external power sources, as it exploits the same energy stored in the inductor before the fault event. An experimental setup has been realized to test the effectiveness of the protection scheme and the related results have been presented. Additionally, a possible generalization of the scheme capable to operate also in case of bidirectional power flow across the DC-link inductor has been proposed.

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REPORT DOCUMENTATION PAGE

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
July 2006	Subcontract Report	October 29, 2002-December 31, 2005

4. TITLE AND SUBTITLE
Design and Test of a Variable Speed Wind Turbine System Employing a Direct Drive Axial Flux Synchronous Generator

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
T.A. Lipo and P. Tenca

5d. PROJECT NUMBER
NREL/SR-500-39715

5e. TASK NUMBER
WER6 0301

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
University of Wisconsin
750 University Ave.
Madison, WI 53706-1490

8. PERFORMING ORGANIZATION REPORT NUMBER
XCX-3-32227-04

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
NREL/SR-500-39715

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES
NREL Technical Monitor: A. Laxson

14. ABSTRACT *(Maximum 200 Words)*

The goal of this funded research project is the definition, analytical investigation, modeling, and prototype realization of a current-source conversion topology tailored to high-power wind turbines.

15. SUBJECT TERMS

wind energy; wind turbine; grid; generator; voltage; converter

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE	UL		
Unclassified	Unclassified	Unclassified			19b. TELEPHONE NUMBER *(Include area code)*