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Research Leading to High-Throughput Manufacturing of Thin-Film CdTe PV Modules

Annual Subcontract Report
September 2004—September 2005

R.C. Powell
First Solar, LLC
Perrysburg, Ohio

Subcontract Report
NREL/SR-520-39669
April 2006

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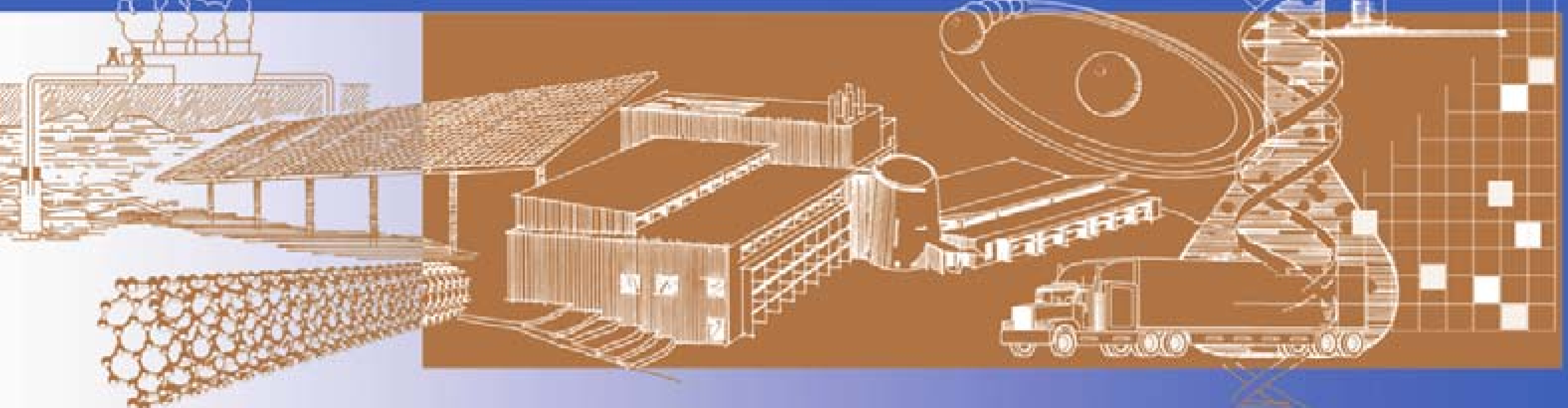

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NREL Technical Monitor: H.S. Ullal
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National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
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Abstract

Cost of photovoltaic (PV) modules is a major impediment to widespread use of solar energy for commercial production of electricity. Thin film technologies are expected to enable significant cost reductions compared to conventional wafer silicon PV technologies. First Solar's Thin Film PV partnership program is directly targeted to reduction of PV module costs ($/W) through a combination of improved module efficiency (W/m^2) and improved process control leading to lower material cost ($\$/m^2$). Competitive pricing is an essential element in development of a vibrant US PV industry that will bring clean, reliable, and affordable energy technologies to the marketplace in support of the EERE mission; cost reduction of development and production are specific elements of the SETP Program Goal[i].

Specific overall objectives of this subcontract are improvement in baseline field performance of manufactured CdTe PV modules while reducing environmental, health and safety risk in the manufacturing environment. Project objectives focus on four broad categories: 1) development of advanced front contact window layers, 2) improved semiconductor film deposition, 3) development of improved accelerated life test procedures that indicate baseline field performance, and 4) reduction cadmium-related environmental, health and safety risks.
During performance of this subcontract First Solar accomplished the following:

- Designed, built, tested and evaluated for production a new generation of advanced distributors for semiconductor vapor transport deposition. More than an optimization, these advanced distributors were developed around a new operating principle and represent a change in the fundamental design that circumvents fundamental deficiencies in earlier designs and produce films that are more uniform across a plate, more uniform plate-to-plate within a run, and exhibit simplified deposition control and increased material utilization.
- Developed an advanced semiconductor powder feeder suitable for vapor transport deposition of ultra-thin CdS films.
- Generated five patent applications – four on advanced distributor design; one on advanced powder feeder
- Through a Colorado School of Mines subcontract - developed a three stage model for distributor operation including a) injector model of powder feed into heated vaporizer, b) distributor model of vaporization and flow of gas within the distributor, and c) deposition model of distribution of gas coming out of the distributor and deposition onto glass. The detailed distributor model was used to carry out a Taguchi design of experiments that identified key features of distributor design essential for producing uniform films.
- Demonstrated module scale application of buffer layer and sputtered CdS films. A module produced with ultra-thin CdS and buffer layers displayed 9.6% efficiency (unconfirmed) compared to <9% efficiency obtained with modules with the same CdS thickness but without a buffer layer.
- Demonstrated ability to reproducibly deposit 900 Å CdS films in manufacturing
- Demonstrated ability to reproducibly deposit 2.5 μm CdTe films in manufacturing
- Developed equipment and ALT methodology to establish good correlation among non-laminated cell, strips and submodules and performed preliminary correlations with field data
- Virtually eliminated hazardous waste generated from off-spec WIP plates and modules.
- Reduced operator exposure to Cd-containing ambients

Acknowledgements

Many people at First Solar contributed to the success of this subcontract. We gratefully acknowledge the contributions of Anke Abken, Dave Berger, Eugene Bykov, John Christiansen, Todd Coleman, Douglas Dauson, Nelson DeVoe, Tony Draper, Marcus Gloeckler, Andy Gray, Akhlesh Gupta, Roger Green, Upali Jayamaha, Peter Meyers, Anne Moser, Mike Steele, and Syed Zafar, as well as personnel from First Solar production, engineering and management.

We are also grateful for the support that we have received from National Renewable Energy Laboratory staff including D. Albin, S. Asher, T. Gessert, T. McMahon, H. Ullal, B. vonRoedern, S. Wei, X. Wu, and K. Zweibel. Contributions from S. Hegedus and B. McCandless of Institute of Energy Conversion; J. Sites, K. Barth and A. Enzenroth of Colorado State University; A. Fahrenbruch of ALF; A. Compaan, V. Karpov, and D. Shvydka of University of Toledo; S. Feldman, S. Gilmore, V. Kaydanov and T. Ohno of Colorado School of Mines; and C. Ferekides of University of South Florida are gratefully acknowledged.

Two lower-tier subcontracts directly contributed to this work. The first project, titled "Direct Integration of Solid-Precursor Powders into Chemical Vapor Deposition Systems", carried out modeling of the heat and mass transfer in the deposition reactor. This work was performed by J.P. Delplanque, R. Kee, and M. Pavol of Colorado School of Mines. The second project, titled "Nonuniformity Loss in Photovoltaics", carried out modeling of performance loss due to spatial variation. This work was performed by V. Karpov and D. Shvydka at University of Toledo.

1 Introduction

1.1 Project Background

First Solar, through its predecessor Solar Cells, Inc. (SCI), began development of thin film CdTe manufacturing technology in 1990 and produced a 6% total area 0.72 m^2 PV module in June 1992. SCI was awarded NREL thin film PV partnership subcontracts in 1993, 1998 and 2002 (the present project). In addition SCI was awarded PVMat subcontracts in 1995 and 1998 and US Department of Energy (DOE) Small Business for Innovative Research (SBIR) contracts in 1995 and 1998. Private funding combined with DOE funding was used both to improve product performance and to develop high throughput manufacturing technology. Significant additional private investment obtained in 1999 resulted in the formation of First Solar, LLC and enabled construction of a manufacturing facility. Initial manufacturing of thin film polycrystalline CdTe PV modules began in 2001. In December 2004 First Solar surpassed 10 MW of cumulative production. Production in 2005 exceeded 20 MW. In May 2005 First Solar broke ground for a 50 MW capacity expansion expected to come on line in Q3 2006.

Throughout its history First Solar technical staff have worked closely with the wider CdTe technical community including researchers at NREL, SNL and the academic community. Since its founding ten years ago First Solar has been an active member of the National CdTe PV R&D Team. CdTe Team activities focus on fundamental issues that underpin and ultimately advance all CdTe PV module technology but are not specific to First Solar manufacturing technology. Similar to its predecessor subcontracts, the current NREL TFPV subcontract to First Solar enables First Solar technical staff to evaluate scientific insights – whether obtained from the broader technical community or through in-house studies- and to adapt those insights into (typically proprietary) equipment or process changes that can improve First Solar module performance and manufacturing technology. Development of equipment or process changes typically requires invention that results in creation of proprietary or patentable technology.

1.2 Technical Approach

First Solar's approach to bringing down the cost of PV modules is to develop thin film PV technology to replace the current mainstream PV technology based on wafer Si. Of the various commercial or near commercial thin film technologies, CdTe PV has the most favorable combination of current performance, manufacturability, cost, and upside performance potential.

The current program focuses onto four key areas:

1. Advanced front contact window (AFCW) layer (See Figure 1.)- A key factor in improving CdTe/CdS device performance is increasing short circuit current density (Jsc) by thinning the CdS window layer. Although thinner CdS enables more photons to reach the CdTe where they can be converted to electrical current, too thin CdS results in dramatically lower open circuit voltage (Voc) and fill factor (FF). In practice the minimum CdS thickness that can be achieved in cells without loss in Voc and FF requires use of an additional high resistivity buffer layer between the high conductivity transparent conducting oxide (TCO) front electrode and the CdS.

Champion cell performance achieved at NREL employed AFCW layers consisting of high conductivity, high optical transparency cadmium stannate (CTO) as the transparent front electrode, high resistivity zinc stannate (ZTO) as the buffer layer in combination with thin sputtered CdS or aCdS:O[ii]. During the second year of the program, program tasks were modified to include investigation of AFCW layers and identification of technical issues related to their possible incorporation into the First Solar production line.

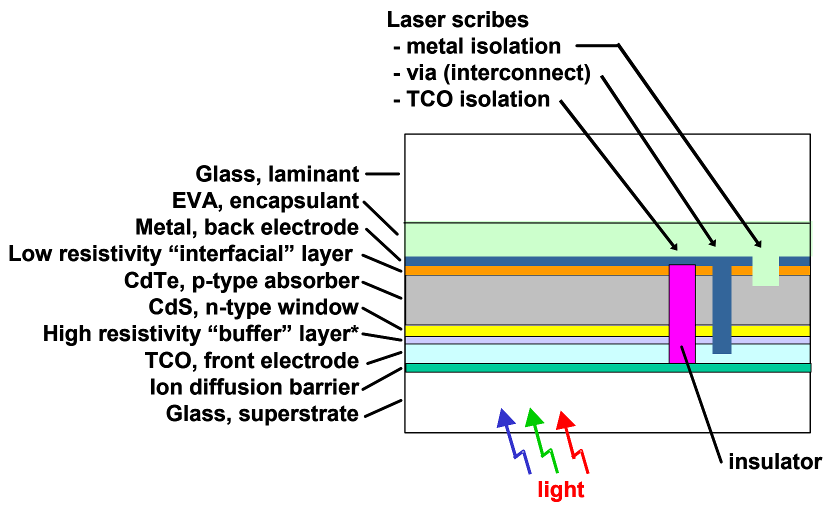

Figure 1. Schematic cross section of First Solar polycrystalline thin film CdTe PV module showing films and interconnect scribes. The TCO, buffer layer, and CdS window films are collectively referred to as the Advanced Front Contact Window layer (AFCW).

2. Development of improved CdTe and CdS semiconductor deposition through improved distributor design, improved process control and improved material characterization metrics - In one sense CdTe PV technology has broad process latitude in that CdTe films deposited by a wide variety of procedures can be processed to produce >10% efficient devices; i.e., CdTe PV is a very manufacturable technology. Nonetheless, optimum device performance has been achieved for only for a relatively few CdTe film deposition processes. Furthermore, for any given film, optimum device performance depends upon film properties in ways that are not fully understood. Realization of CdTe PV's full potential requires not only that semiconductor (CdTe/CdS) film properties be optimized, but also that both process and work-in-progress (WIP) product variation be minimized.

   Another factor is material utilization. Semiconductor material not deposited onto the glass plate is deposited onto chamber walls and rollers. Lost material results not only in higher direct material cost per plate but also in increased maintenance and reduced equipment run time.

   Finally, economics dictates that the equipment have high throughput, low capital cost, high uptime, and produce consistent coatings.

3. Development of improved accelerated life test (ALT) procedures that indicate module baseline field performance - Changes in performance of CdTe PV modules in the field can be separated into packaging-related issues (such as breakage or moisture ingress) and device-related issues. In this project ALT focuses on device-related changes in performance. Device performance is monitored as devices are "stressed" using various temperature-time-illumination levels and sequences; changes in performance are used as indicators of field performance.

4. Improved Environmental, Health and Safety (EH&S) procedures - CdTe PV has a spotless EH&S record with respect to cadmium toxicity issues. There are no documented cases of researchers, manufacturers or end users suffering any Cd-related ill effects associated with their work with CdTe PV modules. Similarly there is no evidence of increased Cd levels in the environment associated with CdTe PV research, manufacturing or deployment. First Solar has purchased an insurance policy to fund solar module reclamation and recycling expenses at end of product life; First solar is the only PV manufacturer of any technology to establish such a policy[iii]. First Solar is proud of its proactive EH&S record.

   That being said, the Cd-toxicity perception issue is real. Some customers and regulators express concern; some competitors use the Cd-toxicity issue for their competitive advantage. Any program can be improved and development of improved EH&S procedures related to Cd are part of this subcontract. Tasks within this program relate to reduction of hazardous manufacturing waste, development of engineering procedures that reduce the exposure of manufacturing personnel to Cd-containing environments and reduced detection response time for potential exposure of personnel to Cd-containing ambients.

1.3 Implementation Approach

Much subcontract work is carried out on the production line using a system of Engineering Test Authorizations (ETA) that provide access by researchers to production line equipment with minimal disruption of production. Additional equipment enables independent fabrication of cells – except for semiconductor deposition by vapor transport deposition. An off-line sputter coater capable of depositing metal, semiconductor, TCO and buffer layers onto 60 cm X 120 cm plates is used extensively for the AFCW program.

First Solar engineers and researchers have had extensive training in and routinely employ Taguchi methods of robust engineering and Six Sigma methods for process optimization and control. Data collection and analysis are greatly facilitated by First Solar's extensive online data collection and storage system that enables analysis of data using Microsoft Access and Minitab. Plates run through the production line are individually bar coded prior to entering the semiconductor coater. Bar code readers at various downstream process locations enable engineers to determine many process conditions for any given plate. Module and submodule IV curves – not just efficiency - of each plate every time it is measured is stored in the data base and can be readily retrieved by researchers at their desks. In addition cell IV measurements are stored in the data base and QE and C-V-f data is stored and is readily transferred to portable storage devices.

2 Advanced Front Contact and Window Layers (AFCW)

2.1 AFCW background

Initial studies focused on adapting the NREL small cell technology to First Solar manufacturing procedures. Process parameters were varied in designed experiments using Taguchi methodology. When initial trials failed to demonstrate the advantages of ZTO (see Figure 2[iv]), researchers began trials with alternative buffer layer materials. It should be noted that requirements placed on TCO/buffer layer in a manufacturing environment are not the same as those of a laboratory setting. Some additional desirable properties that the TCO/buffer layer should have are:

- Ability to adhere to the substrate under severe conditions. Submodule processing requires the TCO to be heated to high temperatures. The TCO has to be stable at these high temperatures. Also, throughout the life of the module, the TCO will be subject to severe temperature and electrical cycling. The interfaces with glass and with the other thin films have to maintain their integrity.
- Ability to block the migration of elements through the TCO. The glass has elements in it that are dopants (e.g., Na) and that can diffuse into the TCO.

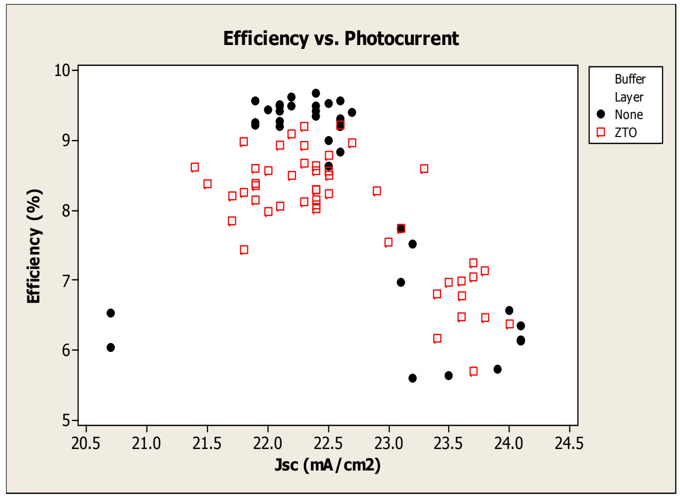

Figure 2. Dependence of cell efficiency on Jsc for devices produced on various thicknesses of CdS - with and without a ZTO buffer layer[4].

- Ability to hide imperfections in processing. Certain thickness ranges of the TCO are more susceptible to color changes than other ranges. The TCO color sensitivity can be altered by adding additional transparent oxides to the stack.
- Reproducible surface texture. TCO texture has a strong impact on optimum semiconductor deposition and other downstream processing parameters. For example, rough topography of the TCO requires that the subsequent coating be thicker to assure complete coverage.

2.2 TCO Deposition Processes

In order to achieve optimum TCO and buffer layer properties suitable for the production environment, existing commercial TCO deposition processes were reviewed. The three major forms of deposition are:

1. Sputter Deposition. This process is done by magnetically enhanced cathodic sputtering under vacuum. The vacuum coater can deposit many different materials including oxides. Sputter deposition has advanced so that deposition can occur at higher temperatures, although not as high as are employed in the VTD process. The major advantages of vacuum deposition are that many different types of materials can be deposited and that the control and uniformity of the coatings is very good. The major disadvantage of vacuum deposition is that the coatings are weakly bonded to the substrate.
2. Spray Pyrolysis: This coating technique was the predecessor of the chemical vapor deposition (CVD) techniques. The coatings are applied at elevated temperatures by spraying droplets of liquid precursors onto hot substrates. The major advantages of spray pyrolysis are that the coatings are more durable than vacuum deposited coatings, the variety of precursors is quite large, and the cost of the system is cheaper than CVD or vacuum deposition. The disadvantage of spray pyrolysis is that the coatings are not uniform in thickness as becomes more evident when the coatings are above 1000 Angstrom in thickness.
3. Chemical Vapor Deposition (CVD): The process consists of vaporizing the precursors and directing the resultant gasses onto a hot substrate. There are many types of CVD processes but the major one, in terms of square feet of material made, is Atmospheric Pressure Chemical Vapor Deposition (APCVD). The advantages of this process are that the TCO

chemistry has good adhesion with the substrate and the coatings can be more uniform than spray pyrolysis. The disadvantages of CVD are:

a. The chemical usage efficiencies run between 10 and 20%.
b. The uniformity of the coatings, although better than spray pyrolysis, is not as good as the vacuum coatings.
c. Capital costs are high.
d. A limited number of chemistries can be applied depending on desired film composition and the substrate.
e. Switching chemistries could take time and capital.

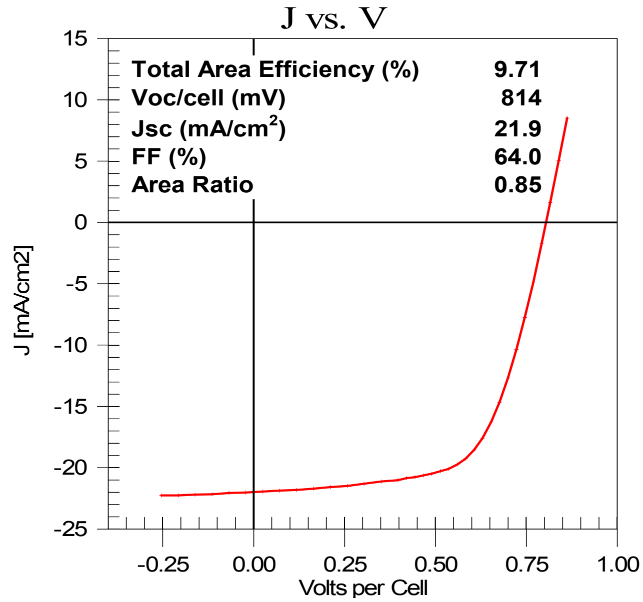

Figure 3. Champion 7200 cm^2 module achieved using a buffer layer.

As of the conclusion of this subcontract researchers had not made a final decision regarding choice of TCO deposition technology. In order to take advantage of the ability to investigate a large number of material systems, experimental trials during this subcontract were limited to investigation of sputter-deposited films.

2.3 AFCW development

Researchers have been investigating various sputter-deposited buffer layers. Best results achieved to date are 9.71% total area efficiency (unconfirmed) with the IV curve displayed in Figure 3. Films made during the same coater run and processed during the same period using the same CdS thickness had efficiency below 9%.

3 CdS/CdTe Deposition Reactor Development

3.1 VTD Background

At the heart of the First Solar manufacturing technology is the semiconductor coater. CdS and CdTe are deposited sequentially in the same piece of equipment using

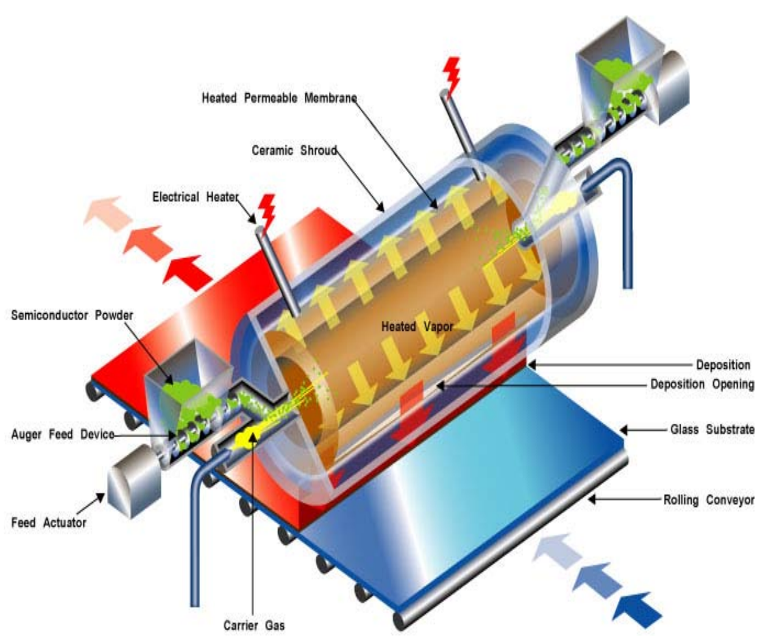

Figure 4. Conceptual drawing of First Solar proprietary VTD system. First Solar's High Rate Vapor Transport Deposition system was awarded an IR&D 100 award in 2003.

separate distributors that both employ the vapor transport deposition (VTD) method. VTD is a high-throughput, large- area coating technique pioneered and patented by First Solar[v,vi]. The system capitalizes on the ease with which CdS and CdTe can be vaporized and on the rapid rates at which quality films can be formed from re-condensing vapors. As depicted conceptually in Figure 4, the method utilizes flash-sublimation of injected semiconductor powders in an inert carrier gas stream to create a dense vapor cloud in a modest vacuum. Inert carrier gas flow directs and controls the dense vapor cloud. Semiconductor films are formed on glass substrates at temperatures >450 ºC at high rates. The inert carrier gas and some vapors not deposited are then exhausted from the chamber.

Since the VTD deposition rates are high, the length of the deposition zones needed to form the relatively thick absorber layer at production line speeds is relatively short. Compact high temperature deposition zones are ideal from a manufacturing equipment perspective as short deposition chambers can be used (lower capital equipment costs) and small critical areas are easier to manage. The production vapor generator and vapor distributor system in use at the beginning of this subcontract and still used today is relatively simple, robust, and durable.

3.2 VTD Technical Obstacles

VTD has been shown to be capable of deposition of device-quality CdS and CdTe films at several microns per second in a production environment, nonetheless VTD is a relatively immature process. At the start of this program film uniformity was relatively good (± 10%), but film properties – as measured by physical characteristics such as roughness and XRD pattern – varied across the plate. Although there were indications that several process factors affected uniformity, the root causes and their relationship to non-uniformity were unknown. As variation in as-deposited film properties are known to result in variation of the optimized downstream process procedure, to the extent that film properties vary across a plate it is impossible to identify a single downstream process that will optimize all areas of a plate. As the relationship between as-deposited film properties and optimized downstream processing is not known, the primary "non-uniformity" metric is variation of I-cell[1] performance across a plate. In addition, although it seems "intuitively obvious" that module performance could be improved if films were uniform across a plate, there was no quantitative measure of the "non-uniformity" loss.

Another technical barrier relates to VTD of thin (<1000 Å) CdS films. As response time of VTD is fast, any variation in input CdS powder feed rate results in non-uniformity in film thickness. CdS deposition is complicated by the particulate nature of the source material; the desired film thickness requires that only a few grains per second of CdS source powder be evaporated. Commercial powder feeders are not available to consistently supply powder at the low rates necessary. Thus one subtask was directed toward development of powder feeders appropriate for controlled deposition of uniform <1000 Å CdS films.

Finally, the film formation process must be integrated with the control of glass properties. The extremely high deposition rates of the VTD method require high substrate temperatures. From the glass perspective, the VTD system heats low-strength, annealed glass to temperatures in excess of the glass softening point. Quenching during venting of the vacuum exit load lock

[1] I-Cells are ~1 cm^2 cells used for quantification of spatial uniformity of device performance within a submodule. I-cells are created by making a set of isolating scribe lines perpendicular to the three cell scribes (TCO isolation, via, and metal isolation) that are used to connect cells in series. Thus each of the 116 cells in a submodule is cut into 57 I-cells whose individual I-V parameters can be measured.

strengthens the glass. The quenching process must be closely coordinated with overall system thermal management in order to achieve glass flatness and strength uniformity. Glass strength is required for field deployment and glass flatness is needed for consistent laser scribing and module lamination.

3.3 VTD Technical Approach

The approach to improving semiconductor film properties while reducing non-uniformity losses involved: a) development of advanced distributors, b) sophisticated modeling and simulation of distributor operation focused on CdTe deposition, and c) quantification of the effect of non-uniform device performance on module performance. Quantification of non-uniform device performance was modeled at the University of Toledo. Modeling results were discussed in an earlier report[4] and will not be repeated here. Computer simulation of distributor performance was carried out by researchers at the Colorado School of Mines and is described in Section 4.

3.4 Distributor Development

Even award winning designs can be improved[vii], however, and during this contract we have developed an alternative distributor concept that has been designated as VTD-2. VTD-2 was built and tested and has demonstrated significantly reduced cross-plate variation.

VTD-2 is not an optimization of the earlier VTD design, rather it is based upon a fundamentally new concept that effectively circumvents the fundamental mechanisms responsible for spatial non-uniformity problems that can arise in a low-pressure, three component gas system. VTD-2 systems are simpler to operate, but are mechanically and thermally more complex. Several different configurations of the VTD-2 concept were tested and one version was selected for production trials. Four patent applications have been filed on the VTD-2 systems.

An example of the improved performance is given in Figure 5which shows improved cross-web thickness uniformity that remains constant throughout a long run. Figure 6 and Figure 7 show that improved thickness and roughness uniformity, respectively, is achieved within individual plates within a run. Moreover the uniformity obtained with a VTD-2 distributor is fixed by construction geometry unlike a VTD-1 distributor which requires operator fine-tuning. The VTD-2 distributor also provides a broad operating window for carrier gas flow.

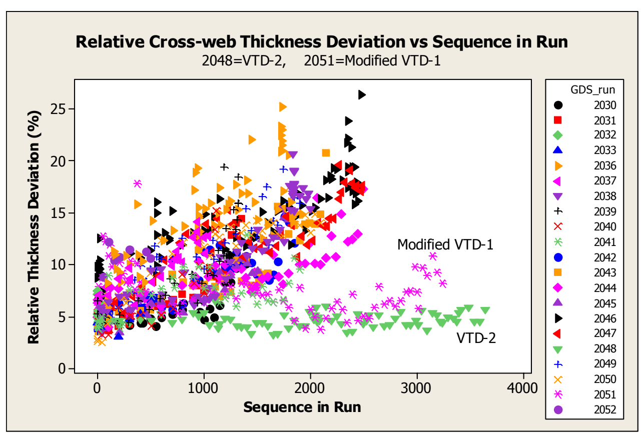

Figure 5. Cross-web thickness uniformity of CdTe films deposited with different distributors. Relative deviation is lower and remains constant throughout a 3600 plate run with the VTD-2 distributor design.

The VTD-2 distributor also has benefits in material utilization. The original VTD-1 distributor was operated with poor material utilization. One variation of a VTD-1 distributor improved utilization by a factor of 1.8. The material utilization with VTD-2, however, improved by 15% over the best VTD-1 distributor and was a factor of 2.1 better than the original VTD-1 system. The improved utilization not only saved material, it increased run durations significantly due to slower build-up on furnace components. Build-up on furnace components is one of the primary factors that cause the decrease in film uniformity throughout the duration of a long run. Tens of thousands of plates of 2.5 µm CdTe plates have been routinely produced. The VTD-2 distributor design provides a straightforward method to control the location of the deposition flux. We thus expect further improvements in utilization as VTD-2 design is optimized.

The VTD-2 system was successfully tested in a number of large production trials. Results have been compelling and the VTD-2 system is now operating 100% of the time for CdTe in one production coater, about 50% of the time in the original production coater, and is slated for 100% usage in new coaters.

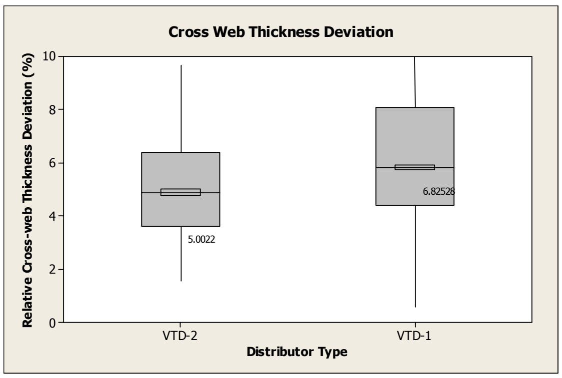

Figure 6. Box plot of relative cross-web thickness deviation. VTD-2 distributors average about a 5% cross-web thickness deviation.

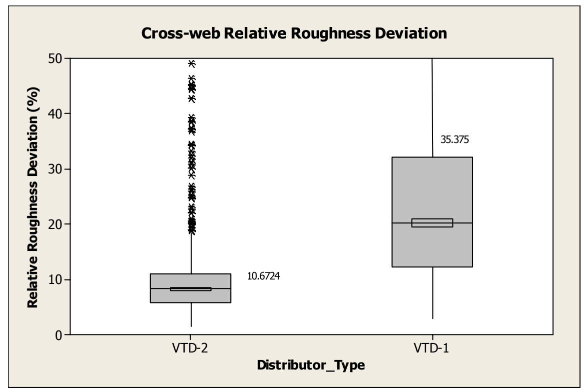

Figure 7. Box plot of relative cross web surface roughness deviation.

3.5 CdS Powder Feed

As discussed in the AFCW section, increased efficiency can be achieved in part through use of increasingly thin CdS films that enable higher Jsc. While sputter deposition of CdS is one option for depositing thin CdS films, tasks in this subcontract were also directed toward VTD deposition of ultra-thin CdS films. CdS film thickness uniformity is also important, as losses in FF and Voc associated areas of a module with too-thin CdS can easily outweigh the advantage of higher Jsc. High rate semiconductor film deposition combined with requirements for uniform deposition of increasing thin CdS films places significant constraints on the uniformity of CdS powder feed. In practice powder feeders must supply only a few CdS grains per second to produce CdS films of appropriate thickness and they must maintain that feed rate consistently over many hours. Evaluation of many powder feeders from several vendors indicates that commercially available powder feeders are not up to that task.

Therefore during this subcontract a significant effort was devoted to development of improved CdS powder feeders that could consistently deliver small amounts of powder into the VTD distributor over the period of a deposition run. CdS powder feeders that operate on different principles from those in use at the beginning of the contract were developed and tested. CdS films <900 Å thick were produced on the production line. In addition, further improvements have been made in the new, improved design. Powder feeders can now be reloaded without interrupting production. Powder clogging has been greatly reduced. Off-the-shelf components are replacing custom components. Sensors have been incorporated to indicate powder level in the hopper. A patent application on the advanced powder feeder has been filed.

4 Distributor Modeling

Despite the simplicity of the basic VTD-1 system, the heat and mass transport processes that occur within it are complex. Demands for meeting production goals make conducting experimental trials using production equipment increasingly difficult and inferring physical mechanisms operating within the distributor based on resulting film characteristics is very tricky. Therefore a program to provide a solid theoretical understanding of the distributor operation was carried out in collaboration with a group from Colorado School of Mines (CSM). The goal of this effort was to guide the experimental work of distributor design and operation.

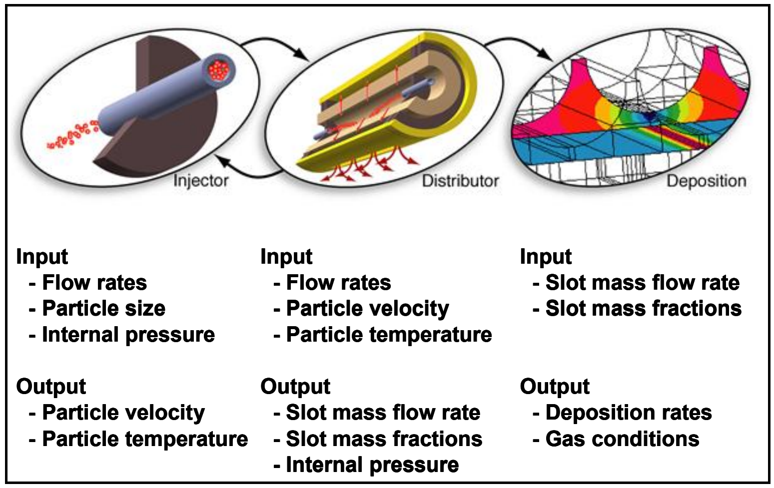

Figure 8. Primary elements of the distributor simulation model developed by CSM researchers.

The CSM team developed a three-stage numerical model of mass and heat flow within the semiconductor deposition system. The model includes details of particle injection, particle sublimation and vapor transport within the distributor, and vapor transport and film deposition of source gas exiting the distributor slot; see Figure 8.

Within the distributor flow field calculations are coupled to the particles by way of mass, momentum, and energy. Convective sublimation is approximated using the extended film model, which describes the particle mass loss and the heat required by the sublimation process. This sublimation model is connected to a model for tracking particle motion through a specified flow field. Distributions of input particle sizes can be tracked as they enter the distributor and sublime. The model is fully coupled. It accounts for physical motion of the powders, radiative and convective heat transfer, and powder sublimation. The sublimed vapor significantly alters the pressure, velocity and composition of the gas phase which in turn affects the motion of the injected powder. Once the injected powder has sublimed, gas flow through the porous distributor is modeled using a combination of Darcy flow, Fickian diffusion, and Knudsen diffusion that defines the composition of source gas exiting the distributor slot. Finally deposition onto the glass substrate is modeled using a 3-dimensional Navier-Stokes analysis using commercially available computer code combined with equations that describe the film deposition reaction.

Clearly the computer simulation involves many complex calculations based upon "best estimates" of conditions within the distributor and deposition chamber. In order to develop confidence in the simulation, initial simulations were performed to replicate experimental results obtained under various VTD-1 operating conditions[4]. Upon successful replication of experimental results, a Taguchi design of simulations was carried out to evaluate the impact of various distributor design variations on expected film characteristics. Each simulation required entering a new set of distributor design parameters followed by calculation of the results using finite element analyses. Time for simulation of each case within the Taguchi design required about one man-day. In contrast, experimental evaluation of the same parameters would have required design, fabrication and testing of each distributor variation plus additional time for equipment installation, operation of the semiconductor coater, and experimental analysis of the resulting films. Direct lost production time would have been on the order of two weeks per trial. Details of the experimental design and of the output parameters monitored are proprietary, but "form, fit and function data" sufficient to demonstrate the procedure, analysis and results follow.

Uniformity of film thickness, uniformity of film structure, and material utilization rate were the three variables selected for monitoring simulated distributor performance. Figure 9 contains the Taguchi design and output parameters. Uniformity is indicated by the signal to noise ratio of all data points generated across a plate during a simulation; material utilization is given in arbitrary units based on the ratio of combined mass of material deposited on the plate to mass of material injected into the distributor

Analysis of the actual computer simulation data as represented in Figure 9 enabled calculation of optimized output parameters as displayed in Figure 10 as well as determining tradeoffs between parameters. Confirmation runs, not shown, verified the self-consistency of the approach.

	Input Variables (Distributor Design)														Output Variables (Film Properties)		
Run No.	A	B	C	D	E	F	G	H	I	J	K	L	M	N	Thick S/N	Texture S/N	Material Utilization (AU)
1	low	low	low	low	low	low	low	low	low	low	low	low	low	low	43	7	2.2
2	low	low	low	low	low	low	low	high	high	high	high	high	high	high	35	7	1.8
3	low	low	low	high	high	high	high	low	low	low	low	high	high	high	20	1	1.8
4	low	low	low	high	high	high	high	high	high	high	high	low	low	low	27	-3	2.4
5	low	high	high	low	low	high	high	low	low	high	high	low	low	high	29	-3	1.2
6	low	high	high	low	low	high	high	high	high	low	low	high	high	low	25	-4	1.7
7	low	high	high	high	high	low	low	low	low	high	high	high	high	low	23	14	1.6
8	low	high	high	high	high	low	low	high	high	low	low	low	low	high	28	14	1.0
9	high	low	high	low	high	low	high	low	high	low	high	low	high	low	35	-3	2.2
10	high	low	high	low	high	low	high	high	low	high	low	high	low	high	25	-5	1.7
11	high	low	high	high	low	high	low	low	high	low	high	high	low	high	25	4	1.4
12	high	low	high	high	low	high	low	high	low	high	low	low	high	low	29	5	2.1
13	high	high	low	low	high	high	low	low	high	high	low	low	high	high	30	19	1.3
14	high	high	low	low	high	high	low	high	low	low	high	high	low	low	35	3	2.0
15	high	high	low	high	low	low	high	low	high	high	low	high	low	low	23	-3	1.7
16	high	high	low	high	low	low	high	high	low	low	high	low	high	high	25	-3	1.2

Figure 9. Design parameters (arbitrary units) for Taguchi computer simulation experiment. A through N are distributor design parameters; output parameters indicate signal to noise (S/N) of film thickness, film texture, and material utilization.

	Input Variables (Distributor Design)														Output Variables		
Optimized Output Parameter	A	B	C	D	E	F	G	H	I	J	K	L	M	N	Thick S/N	Texture S/N	Material Utilization (AU)
"Baseline"	low	low	low	low	low	low	low	low	low	low	low	low	low	low	43	7	2.2
Thickness S/N	low	low	low	low	low	low	low	high	low	low	high	low	low	low	**46**	2	2.3
Texture S/N	low	high	low	high	high	low	low	low	high	high	low	low	high	high	26	**22**	1.2
Material Utilization	low	low	low	low	high	high	high	high	low	high	high	high	high	low	29	-4	**2.6**

Figure 10. Optimized distributor design parameters for each output variable based on computer simulation. (Calculated optimized output parameters are highlighted.)

In practice experimental verification of the optimized VTD-1 design was "overcome by events" as the VTD-2 design employed fundamentally different approach, nonetheless, computer simulation of VTD-1 provided valuable insights into distributor operation and many features of the VTD-1 simulation could be applied to the VTD-2 design.

5 Impurity control

5.1 Chemical analysis

Inductively coupled plasma optical emission spectroscopy (ICP-OES) was used for the determination of trace impurities in deposited semiconductor layers after various processing steps. Correlations between semiconductor deposition, $CdCl_2$ processing, back-contact application and total impurity levels in the device were established. Trace element analysis focused on elements that are believed to have a major impact on device performance and long-term stability. Measurements were performed as part of designed experiments on the production line and for standard production pulls. Data concerning the variation of impurity level after different processing steps support process optimization and failure analysis. The introduction of ICP-OES measurements on a regular base is now being evaluated as a standard production line metric.

In addition, ICP-OES measurements of incoming raw materials are being used to define specifications and impurity limits. Historically, it has been seen that raw material batches from the same purity grade show differences in impurity level of critical elements. It is believed that these fluctuations in purity level are linked to observed differences in final device performance.

5.2 Impurities and Chlorine Issues

$CdCl_2$ processing introduces a certain amount of impurities into CdTe and CdS material. Some impurities e.g. Cu, Sb, Bi, and As are known to act as p-type dopants, others like Al and Si may compensate the p-type doping in CdTe. CdS resistivity and Fermi level are also believed to be affected by impurity accumulation. In order to evaluate the impact of impurities on initial and long-term performance ultra-pure $CdCl_2$ was used for experiments performed on small-area devices. The investigated impurities were blended in defined amounts into pure $CdCl_2$. The total up-take of the impurities into the devices during $CdCl_2$ processing was determined using ICP-OES. As shown \in Figure 11, light-soaking at elevated temperatures lead to an improvement in relative efficiency for devices showing a higher impurity level compared to devices with lower impurity levels. The improved relative stability was more than offset, however, by the reduced initial efficiency observed in intentionally-contaminated devices. That is, devices, which had the

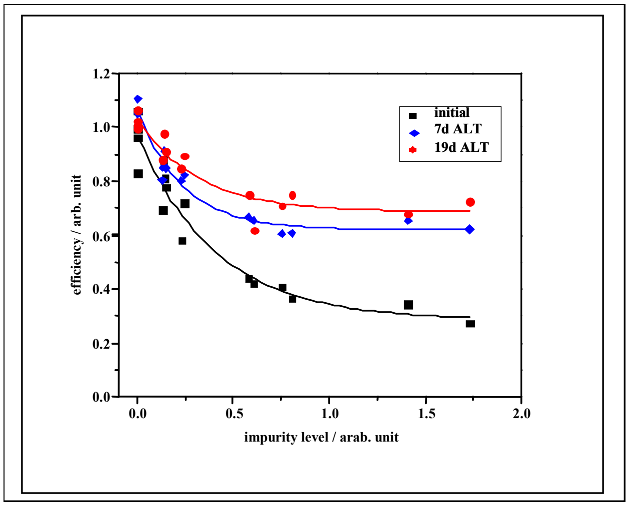

Figure 11. Representative data showing relative changes in efficiency with lightsoak for devices with and without intentionally introduced impurities. Note that absolute efficiency was higher for devices without impurities.

lowest impurity level, exhibited the highest initial efficiencies accompanied by the best light-soak stability.

Further increases in impurity level resulted in further non-negligible losses in initial efficiency, open-circuit voltage, fill-factor and short-circuit current. Light-soaking of these devices at elevated temperatures (~120°C), however, actually lead to an improvement in all 1st and 2nd level metrics; see Figure 12. In general, a higher impurity level of the device leads to major improvements in device performance during light-soaking.

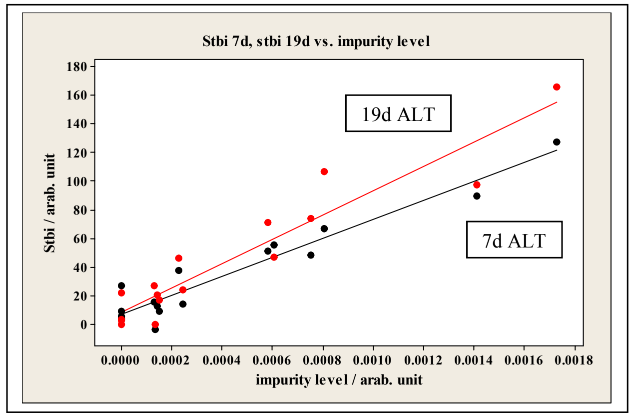

Figure 12. Relative efficiency as a function of added impurity level of devices after 7 and 19 days light soak at 120 C.

Quantum efficiency measurements show that increasing impurity level results in an increase in losses of the red response; see Figure 13. Consistent with the improved device performance during light soak, light-soaking leads to an overall improvement in the red response that occurs in an early stage of light-soaking - in this case after 7 days. Continuation of light-soaking did not change the quantum efficiency response although the JV-response still changed. Samples, which were treated with ultra-pure $CdCl_2$ and had therefore the lowest overall impurity level, also exhibited a similar quantum efficiency response of improving the red response in light-soaking. Re-distribution of the impurities in the device and re-arrangement of defect states may be the root cause for the observed QE performance.

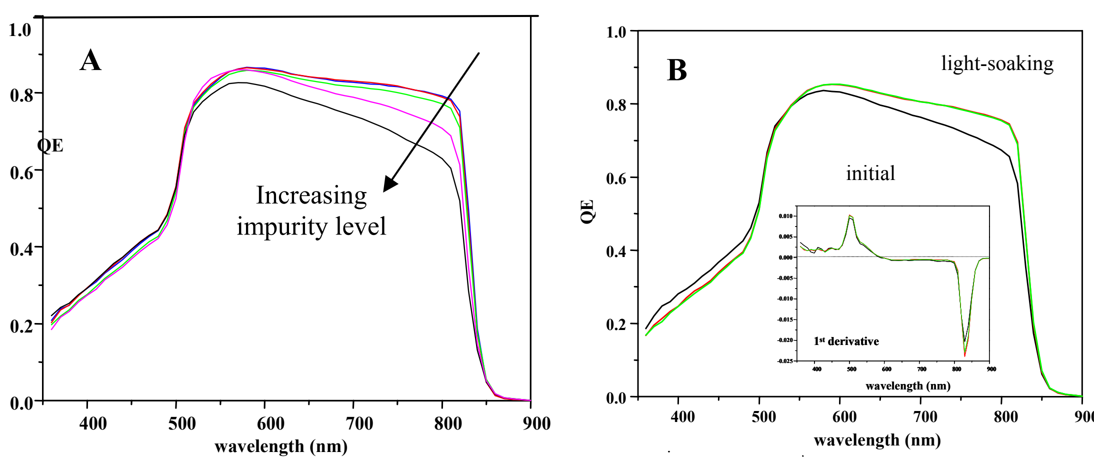

Figure 13. A. Initial quantum efficiency for devices with varying impurity levels and B. Quantum efficiency improvement after light soaking at 120 C for 7 and 19 days.

6 Identification and modification of back-contact chemistry

Device performance is sensitive to the electrical properties of the CdTe to metal electrode interface, i.e., back-contact, and controlling back-contact chemistry during device processing is one of the key factors in achieving long-term stability of high efficiency devices. In an attempt to identify stable alloys that might be important in determining device stability, a series of experiments were carried out that included several process variations including heat treatments up to 100 C above normal process temperature. Working with researchers from NREL, films produced using these variations in device processing were analyzed by XRD. Based on the phase diagrams of metals involved, formation and precipitation of stable alloys was expected within this process space, but in fact no alloying was detected. It is speculated that either the energy barrier for any solid state reaction required to form the alloys was not surmounted or that reactants diffused away from the interfacial region prior to attaining the necessary temperature for alloy formation. In any case, phase formation that could affect device performance or degradation was not detected.

Additional studies focused on back contact surface preparation prior to metal electrode application and specifically on variations in the $CdCl_2$ activation step. Working with IEC, XRD-measurements performed at different stages of the CdTe post-deposition processing indicate the presence of CdO and $CdTeO_3$ and indicate that the humidity level of the $CdCl_2$ heat treatment ambient affects oxide formation. In order to evaluate effects of humidity during $CdCl_2$ heat treatment on device performance, samples were pulled from different $CdCl_2$ manufacturing runs processed under different humidity levels. Although it might be expected that the variation in humidity would result in an altered surface chemistry that would affect device performance, in fact the difference in device performance for the humidity levels studied was not statistically significant.

Ideally the various oxides that form during the $CdCl_2$ activation step would be removed to ensure consistent back-contact formation, thus a series of experiments was initiated in order to explore effects of oxide removal prior to contacting. As acidic-oxidizing etches are not compatible with our back-contact process, various alkaline etches were investigated. Different etch times and concentrations were employed to remove surface oxides and oxy-chlorides. For the treatments investigated, however, neither initial nor long term PV performance was significantly altered compared to non-treated devices. Grazing incidence XRD (GIXRD) (supported by IEC) measurements indicate that none of the etches investigated effectively removed all of the oxide species.

7 Accelerated Life Test Development

7.1 Physical model underlying ALT Technical Approach

Our working hypothesis is that, apart from encapsulation failure, changes in module performance over time are largely determined by changes in cell performance. Changes in cell performance, in turn, depend on changes in the electronic defect distribution within the device. Changes in electronic defects are suspected to be related to defect chemistry of dopants, impurities, vacancies, interstitials and their complexes and may exist within grains or at grain boundaries, interfaces or structural defects. Changes over time in defect type, concentration and location are believed to be driven by deviations between the existing defect state and that steady state associated with the local quasi-Fermi level and chemical potential. Stress on the device, therefore, would best be defined in terms of the magnitude and gradient of the difference between the existing quasi-electrochemical potential and it's steady state value. External factors affecting this "stress" include illumination, external field, and temperature. Mechanisms for changing the defect state include diffusion, migration, electron occupancy, defect mutation and defect chemical reaction.

This view of the electrical properties of CdTe PV devices is both complex and device specific, i.e., observed changes in device performance depend on device structure and material properties as well as on the illumination-bias-temperature history of the device. In principle monitoring and understanding the change mechanisms would provide concepts for tailoring materials properties that influence the stress-induced changes in device performance. Many mechanisms are possible in polycrystalline compound semiconductor thin films, however, and techniques for measuring many important physical, chemical, and electrical and properties have not been demonstrated. Thus although it us helpful to have a broad conceptual basis for explaining changes in device performance, practical application of this model entails sophisticated analytical, scientific and computational capabilities not available within First Solar. Thus we believe that detailed analysis of defect chemistry and its impact on device performance is best left to the larger academic community and the national CdTe Team. First Solar's ALT program relies on empirical studies.

At First Solar a 56 day light soak (LS) at approximately 70 mW/cm^2 illumination and 65 C has been the standard indicator of device field performance. The 56 day light soak has a serious shortcoming, however, in that test throughput is less than one module per day, i.e., <0.1% of modules produced are evaluated for baseline field performance compared to 100% of modules that have efficiency measured. ALT development addresses the throughput issue through investigation of ALT protocols that take advantage of thermal activation on defect mobility and chemistry reaction rates to significantly reduce response time and thereby increase test throughput. Additional studies are aimed at discovering the relationship between ALT and field test results.

7.2 Correlation to 56 day LS

The ALT task objective is development of an Accelerated Life Test that enables timely monitoring of production line performance and enables process optimization to improve baseline field performance. Stress studies focus on stresses induced by illumination, electrical bias and temperature where elevated temperature is also the primary accelerating factor. In the course of this subcontract, experimental trials were primarily performed on submodules pulled from the production line although some of these modules were parts of designed experiments. ALT studies were preformed on 1 cm^2 cells (I-cells) isolated from fully interconnected submodules (working module prior to lamination), "strips" (a section cut from a submodule consisting of 10 cells, each cell 1 cm long by 57 cm wide, connected in series), ½ plates (a submodule cut in half), and (whole) submodules.

Correlation Matrix of Various Experimental ALT Stress Protocols

Test Device			1/2 plate	Strip	Strip	Strip
	Stress Temp		No external heat	No external heat	Elevated	Elevated
		Measure-ment Temp	Room	Room	Room	Elevated
"Sister" (full) plate	No external heat	Room	0.79	0.67	0.57	0.76
1/2 plate	No external heat	Room		0.83	0.74	0.92
Strip	No external heat	Room			0.78	0.97
Strip	Elevated	Room				0.76

Figure 14. Correlation of predicted baseline performance of a) various test structures, b) various stress temperatures, and c) effect of measurements being made in the stress ambient as opposed to after the test structure had been cooled to room temperature.

Lamination was found to have a significant impact on test results and in these ALT trials although lamination did not necessarily improve stability. Furthermore, degradation of the laminant at elevated temperature introduces a practical upper temperature limit to ALT of modules. Thus application of ALT to modules introduces the practical issue of separating device-related changes in performance from packaging-related changes, and results presented here (with the exception of field data) were obtained with non-laminated devices.

A wide variety of ALT protocols is possible but in this program investigations focused on stressing under approximately 100 mW/cm^2 illumination with devices biased to open circuit. In general relatively good correlation was obtained between I-cells, strips, ½ plates, and submodules evaluated using similar ALT trials. Figure 14 displays correlations obtained using various test structures (sister plates, ½ plates, and strips), elevated and "no external heat"[2] and with baseline performance predicted using elevated (i.e., in situ) or room temperature IV measurements. While at least rough correlations are seen in all cases, there exists sufficient variability that it is not clear that any one ALT protocol is superior to the others.

Variation of ALT results originates both from variation in the test itself and variation in the samples tested. As ALT is inherently a "destructive" test in that it can not be repeated on a given device, comparisons were made between ALT results obtained from devices that were as similar as possible. Figure 15 shows that for strips from the same submodule, combined variation in predicted ALT baseline performance was ~1%. Although the small test-related variation within a single ALT protocol provides an existence-proof of a reproducible ALT, the lack of correlation among the various ALT protocols displayed in Figure 1 indicates that results are protocol-specific.

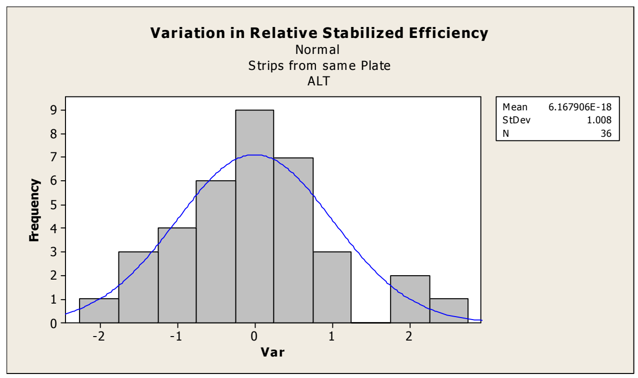

Figure 15. Variation of relative baseline performance as predicted by curve-fitting for strips from the same plate that were stressed at elevated temperature. Variation is defined as 100 X (P-Pavg)/Pavg, where P is the predicted value and Pavg is the average of P on one plate.

7.3 Correlation with field data

In an attempt to better understand the relationship between ALT and baseline field performance, comparisons were made between sister plates exposed to ALT and 36 modules mounted in an outdoor array. Fielded module performance was measured prior to fielding and after stabilization in the field. Fielded modules were part of a designed experiment that include 12 variations in the module fabrication process. Each process variation was intended to "stretch but not break" production line process specifications, and should therefore reasonably reflect production line modules. In this case sister plates were defined by the fact that ALT strips were cut from modules that were produced with the same "process variation condition".

[2] Typical temperature of test structure with no external heat was 65 C.

Both performance and change in performance over time in the field were well-behaved. As displayed in Figure 16 statistically 91% of variation in field performance and 85% of variation in change in performance was explained by process condition. Furthermore, as shown above, variation of ALT on strips within a single plate is ~1%, thus both the field data and results from ALT are well behaved. Nonetheless, as displayed in Figure 17, when change in performance as a result of ALT is compared to change between initial and baseline field performance there is no correlation between the two metrics. This result is interpreted to mean the specific ALT

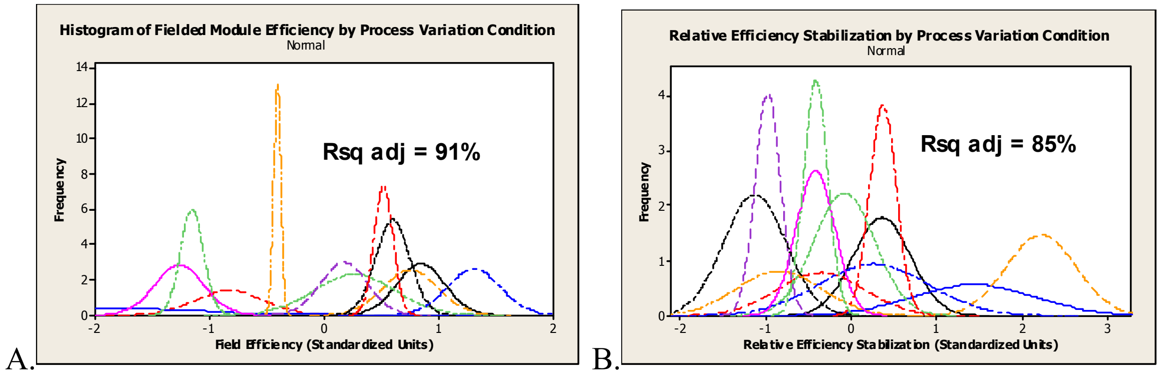

Figure 16 Normalized histograms showing distribution of A. Fielded module baseline efficiency and B. Relative change in efficiency of fielded modules over time for each of 12 process conditions of a designed experiment. Adj Rsq is a measure of the percentage of overall variation that is explained by process condition. Standardized Units are average divided by standard deviation. Positive values of Relative Efficiency Stabilization indicate smaller changes in relative performance.

evaluated is not a reliable predictor of field performance. It does not follow, however, that an effective field performance predictive ALT does not exist. Development of an effective ALT remains an important goal of First Solar and of the CdTe PV community.

7.4 National CdTe R&D Stability Subteam

Work on development of an effective ALT continues both within First solar and within the National CdTe R&D Team. Significant progress has been made by the CdTe Team. In February 2004 the Stability Subteam was formed and at the most recent meeting (May 5-6, 2005) three modes of stress-induced change in device performance were identified: a) decrease in Voc, b) rollover in 1st quadrant, and c) degradation in the resistive terms Rs and Rsh. Several possible mechanisms have been identified that may explain the observed modes, but quantifiable relationships have not been established. Work is ongoing.

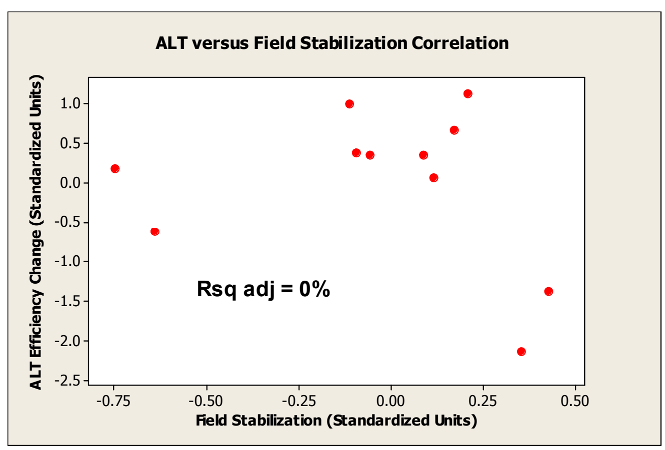

Figure 17. Correlation between change in performance as indicated by ALT and observed change in field data. As indicated by R-sq(adj) there is no indicated correlation between ALT and Field Stabilization values.

8 Environmental, Health and Safety Improvements

8.1 Technical Obstacles

The overarching EH&S technical issue is evaluating potential risks and balancing those risks against immediate costs of risk mitigation. Failure to protect worker health and safety or the environment have major negative moral, legal and economic consequences but ineffective, inefficient or costly risk mitigation procedures can cause an otherwise profitable company to fail. Specific issues addressed in this subcontract relate to:

a. Reduction of toxic waste. At the start of the program off-spec plates or modules were crushed and Cd-containing materials were dissolved with acid. Output from the process was a relatively large quantity of clean glass that could be discarded in a landfill and a relatively small quantity of Cd-containing "cakes" that were disposed of as toxic waste. While the process was effective in reducing the amount of toxic waste, the Cd-containing cakes could not be readily recycled due to the relatively low cost (~$2/kg) of low-purity Cd.

b. Reduction of exposure of personnel to Cd-containing dust. At the beginning of the program there were two process steps that generated significant amounts of Cd-containing dust: 1) removal of "wrap around" CdTe and CdS from the glass surface opposite that intended for semiconductor deposition, i.e., cleaning the "sunny side" of the WIP plate and 2) removal of the CdTe/CdS and TCO layers from a 1.5 cm border of the film in order to provide effective electrical and environmental isolation in the encapsulated module, i.e., the "edge delete" step. These steps occur at different points in the process and each step required personnel to dress in appropriate personal protective equipment (PPE) including respirators and to work in confined spaces. From a manufacturing perspective, both processes were slow and labor-intensive.

c. Determination of inadvertent exposure of personnel to Cd-containing ambients. Cadmium concentration is monitored at several locations in the plant in order to ensure that workers are not exposed to airborne Cd in excess of Occupational Safety and Health Administration (OHSA) action levels. The present procedure includes collection of airborne particles obtained using small fans to pull air through filters and then sending the filters to an external lab for determination of airborne Cd levels – a process that requires 4-7 days. In the event of an unforeseen increase in airborne Cd levels, EH&S response time is limited to time required for determination of measured airborne Cd.

8.2 EH&S Tasks

EH&S tasks were carried out by members of the First Solar EH&S group independently from other subcontract tasks. Typical work flow began with collection of data and investigation of options. Typically solution of EH&S objectives were synergistic with cost reduction objectives so that EH&S personnel worked closely with manufacturing engineers. For example, reduction of personnel exposure to cadmium dust also reduced direct labor; recycling of spent coated modules reduced both labor and costs associated with disposal of hazardous wastes. With respect to specific objectives of this subcontract, the following EH&S objectives were accomplished:

a. Objective - Reduction of toxic waste
   Whereas in the past off-spec CdTe-coated plates were shredded, the CdTe/CdS was stripped in acid and converted to "cakes" which were then disposed of as hazardous waste, now

shredded modules are sent to a Cu smelter where Cd is recovered and recycled. Thus hazardous waste from off-spec plates has been virtually eliminated.

b. Objective – Reduction of exposure of personnel to Cd-containing dust
All processes have been evaluated and there are no module fabrication processes that requires operator use of PPE[3]. Edge delete and sunny-side buffing steps have both been fundamentally re-designed including design, fabrication and environmental testing of automated equipment that virtually eliminates exposure of personnel to Cd-containing dust.

c. Determination of inadvertent exposure of personnel to Cd-containing ambients
Efforts to develop a practical procedure for routine reduction in industrial-hygiene sample turn-around time to 2 hours from the current 4-7 days were not successful. It is emphasized, however, that there have been no cases of unexpected exposure of personnel to Cd-levels beyond OSHA limits. Nonetheless, First Solar continues work to reduce any margin for error and to improve its unblemished record with respect to personnel health and safety.

9 Summary

9.1 First Solar Growth

During the course of this subcontract First Solar has significantly increased manufacturing capacity from less than 2 MW/yr to more than 20 MW/yr while at the same time increasing the average module total area power conversion efficiency from 7% to >9%. First Solar currently manufactures and sells 50-65 W thin film CdTe PV modules at a rate of approximately 1.9 MW/month. Sales backlog (booked sales less current inventory divided by production rate) is more than a year. First Solar is currently building new facilities and installing additional equipment to increase production capacity by 50 MW/yr; the additional capacity is expected to come on line in the third quarter of 2006.

9.2 Subcontract Accomplishments

Specific subcontract accomplishments include:

- Designed, built, tested and evaluated for production an advanced distributor for semiconductor vapor transport deposition. More than an optimization, VTD-2 distributors were developed around a new operating principle and represent a change in the fundamental distributor design. VTD-2 distributors circumvent fundamental deficiencies in earlier designs and produce films that are more uniform across a plate, more uniform plate-to-plate within a run, and exhibit simplified deposition control and increased material utilization.
- Developed an advanced powder feeder suitable for vapor transport deposition of ultra-thin CdS films.
- Generated five patent applications – four on advanced distributor design; one on advanced powder feeder
- Through a Colorado School of Mines subcontract - Developed a three stage model for distributor operation including a) injector model including powder feed into heated vaporizer, b) distributor model including vaporization and flow of gas within the distributor, and c) deposition model including distribution of gas coming out of the distributor and deposition onto glass. Computer-simulated distributor performance replicates observed VTD-1

[3] PPE are required to perform certain maintenance procedures.

distributor performance over the operating parameter space that has been explored experimentally. The model provided important insight into the fundamental physical factors affecting device performance and thereby facilitated design of advanced distributors. The distributor model was used to carry out a Taguchi design of experiments that identified key features of distributor design essential for producing uniform films.

- Demonstrated NREL-confirmed total area module efficiency of 9.32% on 7200 cm^2 (67.12 W, 69.8 V Voc, 1.15 A Isc, 60.4% FF).
- Demonstrated module scale application of buffer layer and sputtered CdS films. A module produced with ultra-thin CdS and buffer layers displayed 9.7% efficiency (unconfirmed) compared to <9% efficiency obtained with modules with the same CdS thickness but without a buffer layer.
- Demonstrated ability to reproducibly deposit 900 Å CdS films in manufacturing.
- Demonstrated ability to reproducibly deposit 2.5 µm CdTe films in manufacturing. Tens of thousands of plates with 2.5 µm CdTe have been routinely produced in production. Evaluation of the impact of CdTe thickness on baseline field performance is ongoing.
- Developed equipment and ALT methodology to establish good correlation among non-laminated cell, strips and submodules and demonstrated procedures for quantitative comparison between ALT and predicted baseline field performance.
- Virtually eliminated hazardous waste generated from off-spec WIP plates and modules.
- Reduced operator exposure to Cd-containing ambients.
- Through a University of Toledo subcontract, developed initial statistical models indicating effects of non-uniformity of cell performance.

With plants under construction to increase capacity to 75 MW/yr by 2007, First Solar is one of the fastest growing PV companies in the world. Technical accomplishments of the current subcontract have been important contributors to First Solar's growth during this period; continued technical progress will be required to further expand the impact of CdTe PV on th PV market.

10 Publications:

1) R. C. Powell, "RESEARCH LEADING TO HIGH THROUGHPUT MANUFACTURING OF THIN-FILM CDTE PV MODULES", Phase II annual technical report, NREL subcontract No. RDJ-2-30630-20, Feb. 9, 2005. Available at http://www.nrel.gov/ncpv/thin_film/pn_techbased_cadmium_telluride.html#annual_final_report

2) Peter V. Meyers, Anke Abken, Douglas Dauson, Upali Jayamaha, Rick Powell and Syed Zafar, "Technology in support of Thin Film CdTe PV Module Manufacturing", Proceedings, DOE SET Program Review, Denver, CO (7-10 Nov. 2005)

3) Other Information Sources: First Solar Website: http://www.firstsolar.com/

Glossary of Acronyms

AFM	atomic force microscopy
ALF	Alan Farhenbruch consulting
ALT	Accelerated Life Test
CdS	Cadmium Sulfide
CdTe	Cadmium Telluride
CSM	Colorado School of Mines
CSU	Colorado State University
CTO	cadmium tin oxide
CV	capacitance-voltage measurement
C-V-f	capacitance-voltage-frequency measurement
DAP	donor-acceptor Pair
DOE	US Department of Energy
EERE	Energy Efficiency and Renewable Energy, a program within DOE
EH&S	Environmental, Health and Safety
FF	fill factor
FS	First Solar, LLC.
GIXRD	glancing incidence X-ray diffraction
HEPA	high efficiency particle accumulator
ICPOES	inductively coupled plasma optical emission spectroscopy
IEC	Institute of Energy Conversion at the University of Delaware
IFL	interfacial layer
Isc	short circuit current (amps)
I-V	current-voltage measurement
IVT	current-voltage measurements as a function of temperature
J_{sc}	short circuit current density (mA/cm^2)
LS	light soak (relates to ALT)
NREL	National Renewable Energy Laboratory, operates under SETP
OC	open circuit
OSHA	Occupational Safety and Health Administration
PL	photoluminescence
PPE	personal protective equipment
PV	photovoltaic
QE	quantum efficiency
Roc	dynamic resistance at open circuit
Rsc	dynamic resistance at short circuit
SC	short circuit
SCI	Solar Cells, Inc (predecessor of First Solar, LLC)
SETP	Solar Energy Technologies Program, a program within EERE
SNL	Sandia National Laboratory
TCO	transparent conducting oxide
TFPV	Thin Film Photovoltaic Partnership, an NREL program
USF	University of South Florida
UT	University of Toledo
V_{Cd}	Cadmium vacancy
V_{oc}	open circuit voltage

VTD	vapor transport deposition
WIP	work in progress
XRD	X-ray diffraction
ZTO	zinc tin oxide

References

[i] Solar Energy Technologies Program, Multi-year Technical Plan 2003-2007 and beyond, US Department of Energy Efficiency and Renewable Energy, www.eere.energy.gov.

[ii] X. Wu and P. Sheldon, "Novel Manufacturing Process for Fabricating CdS/CdTe Polycrystalline Thin-Film Solar Cells", 16th European PVSEC, Glasgow, UK, 2000.

[iii] "First Solar announced Insurance Policy to Fund Solar Module Reclamation and Recycling Expenses at End of Product Life", First Solar press release, 25 May 2005, http://www.firstsolar.com/

[iv] R. C. Powell, "RESEARCH LEADING TO HIGH THROUGHPUT MANUFACTURING OF THIN-FILM CDTE PV MODULES", Phase II annual technical report, NREL subcontract No. RDJ-2-30630-20, Feb. 9, 2005. Available at http://www.nrel.gov/ncpv/thin_film/pn_techbased_cadmium_telluride.html#annual_final_report

[v] R. Powell, G. Dorer, N. Reiter, H. McMaster, S. Cox, and T. Kahle, "Apparatus and method for depositing a material on a substrate, U.S. Patent # 5,945,163." U.S.: First Solar, LLC., 1999.

[vi] R. Powell, G. Dorer, N. Reiter, H. McMaster, S. Cox, and T. Kahle, "Apparatus and method for depositing a semiconductor material, U.S. Patent #6,037,241." U.S.: First Solar, LLC, 2000.

[vii] First Solar's High Rate Vapor Deposition System was awarded an IR&D 100 Award in 2003.

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
First Solar, LLC
28101 Cedar Park Blvd.
Perrysburg, OH 43551

8. PERFORMING ORGANIZATION REPORT NUMBER
RDJ-2-30630-20

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER
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13. SUPPLEMENTARY NOTES
NREL Technical Monitor: H.S. Ullal

14. ABSTRACT *(Maximum **200 Words**)*
Specific overall objectives of this subcontract are improvement in baseline field performance of manufactured CdTe PV modules while reducing environmental, health and safety risk in the manufacturing environment. Project objectives focus on four broad categories: 1) development of advanced front-contact window layers, 2) improved semiconductor film deposition, 3) development of improved accelerated life test procedures that indicate baseline field performance, and 4) reduction of cadmium-related environmental, health and safety risks. First Solar has significantly increased manufacturing capacity from less than 2 MW/yr to more than 20 MW/yr, while increasing the average module total-area power conversion efficiency from 7% to >9%. First Solar currently manufactures and sells 50-65-W thin-film CdTe PV modules at a rate of about 1.9 MW/month. Sales backlog (booked sales less current inventory divided by production rate) is more than a year. First Solar is currently building new facilities and installing additional equipment to increase production capacity by 50 MW/yr; the additional capacity is expected to come on line in the third quarter of 2006.

15. SUBJECT TERMS
PV; thin film; solar cells; CdTe; modules; semiconductor; vapor transport deposition; manufacturing; facilities;

`+			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			
Unclassified	Unclassified	Unclassified	UL		**19b. TELEPONE NUMBER** (*Include area code*)

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