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Process R&D for CIS-Based Thin-Film PV

Final Technical Report
April 2002 – April 2005

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Camarillo, California

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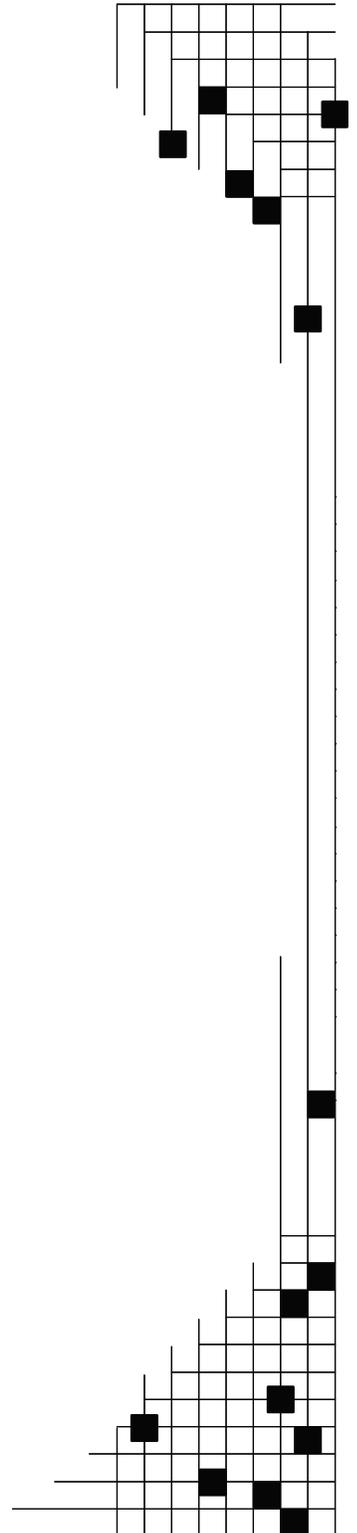
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Preface

Shell Solar Industries (SSI), formerly Siemens Solar Industries, has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2.

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility issues using small area test devices and mini-modules. Statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules [1].

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module. During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and larger 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of Cu (In,Ga)(S,Se)$_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber (Cu(In,Ga)Se$_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL measured average

efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module [2].

From August 1998 through November 2001, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03). The primary objectives of this "Commercialization of CIS-Based Thin-Film PV" subcontract were to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. These objectives were pursued to demonstrate fabrication of efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. An additional mid- to longer-term objective was to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. Throughout this subcontract, SSI capabilities were leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. SSI's approach to this work was to apply design of experiment and statistical process control methodologies. SSI was the first company in the world to produce PV modules based on CIS thin-film technology. This major milestone in the development of PV was recognized by R&D Magazine by awarding the prestigious R&D 100 Award to the SSI family of CIS solar modules. NREL, the California Energy Commission and SSI shared this award. SSI expanded the CIS product line in 1999 to include 20-Watt "ST20" modules and 40-Watt "ST40" modules. Also during the first subcontract phase, a record-breaking efficiency of more than 12% was verified by NREL for an ST-40 module. This result in 1999 far surpassed the DOE year 2000 goal for a commercial CIS module above 10%. During the second subcontract phase, SSI delivered 20 ST-40 large area modules, all with efficiencies over 11%, to meet the subcontract deliverables defined as large area modules with efficiencies over 10%. The average efficiency based on a Gaussian fit to the main portion of the circuit plate efficiency distribution was increased from 10.8% prior to this subcontract to 11.6% for this subcontract. These advancements were due to continuous improvement of all process along with particular attention to process research for two critical processes – CIS formation in new large area reactors and the quality of molybdenum deposited in new high capacity sputtering equipment. Process development improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning. Further R&D of all CIS processes for part size and capacity scale-up was pursued during the third subcontract phase. Major accomplishments included addressing process issues for implementation of high quality high throughput Mo deposition and patterning, high throughput precursor deposition, and higher throughput reaction of the precursor. Circuit plate production capacity was increased by more than an order of magnitude from the beginning of this subcontract while circuit and module efficiencies were steadily improved. The second subcontract milestone – to achieve a pilot production rate of 500 kW per year by the end of subcontract – was first achieved in March of 2001 [3].

Acknowledgments

Shell Solar Industries wishes to acknowledge the contributions of the following people and organizations.

Summary

Compared to traditional wafer-based crystalline silicon technologies, monolithic integration of thin film solar cells can lead to products of comparable performance but with significant manufacturing advantages: lower consumption of direct and indirect materials, fewer processing steps and easier automation. Monolithic integration is required to achieve these advantages since this eliminates multiple process steps and handling operations during both formation of the absorber and during module assembly. The basic module elements for all thin-film technologies (alloys of amorphous silicon, cadmium telluride and CIS) are the same; the module elements are a circuit-glass/cover-glass laminate, a frame, and a junction box. The basic circuit elements are also very similar; they each have a base electrode, an absorber, a junction, a top electrode and three patterning steps for monolithic integration. While the details of these module elements or equivalent module elements differ, the basic cost structures are very similar on an area-related basis. Since the cost per unit area is the same, the cost per watt is inversely proportional to the module efficiency. CIS cells and monolithically integrated modules have demonstrated the highest efficiencies of any candidate thin-film technologies; therefore, CIS is expected to have the lowest manufacturing cost/watt.

The primary objectives of this subcontract are to:
- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that will last up to 30 years while retaining 80% of initial power

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. During this subcontract, predictability of SSI's CIS process was demonstrated by continuously executing the process while increasing throughput. Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. Capacity in 2003 increased to somewhat below 3 MW per year and production for 2003 was just over 1.2 MW. Introducing a new minimodule product accounts for the main difference between production and capacity. The laminate efficiency distribution for 2003 peaked at 11.0% with a full width of only 11% of the average. This distribution is nominally the same as the distribution for 2002 but with an approximately 33% increase in large area laminate production volume. The following quote from the EERE Multi-Year Technical Plan (MYTP) recognizes previous SSI accomplishment, "After two decades of R&D, CIS is being introduced to the market, with prototype modules made by Shell Solar (Camarillo, CA) consistently reaching efficiencies greater than 11%—beating a goal set in the last PV Subprogram 5-year plan by more than a year." Again at least a year in advance and with production modules rather than champion modules, recent SSI accomplishments far exceed the 2003 DOE EERE Multi-Year Technical Plan technical target of 8% module conversion efficiency for thin-film modules.

Dramatic increases in line yield were achieved by improved production protocols and by addressing disparate special causes for process variation. Line yield increased from about 60%

in 2000 to about 85% in 2002. This high line yield was maintained during 2003. A campaign to introduce a minimodule product that would potentially expand near-term and long-term capacity scale-up options began late in 2003 and extending through most of 2004. This was ultimately abandoned. Yield since restarting large area module production late in 20004 has been good but variable due to restaffing and retraining and R&D to implement a new "sputter dose" process. NREL confirmed a champion 12.8% aperture area conversion efficiency for a large area (3626 cm^2) CIS production module. This demonstrates the potential to meet the 2007 MYTP target of 12% average module conversion efficiency for production. Process R&D, both at SSI and in collaboration with NREL teams, demonstrated the potential for further improvements.

Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over sixteen years. However, field failures have also been observed. Field failure mechanisms related to particular package designs and errors during production have been clearly identified. Additional circuit plate or packaging process variables are thought to have affected durability during particular production timeframes. When losses have been observed, the losses correlated with date of deployment or prototype module configuration. Losses are not inherent to CIS; multiple past and present module deployments have demonstrated stability.

SSI is developing "glass/glass" packages that eliminate the TPAT backsheet used in present products. The primarily advantage is decreased packaging costs. Simplification of the package and decreased operating temperature are additional potential advantages. Prototype glass/glass packages for individual 40W circuit plates have passed accelerated tests, including the damp heat test. This package incorporates an edge seal selected in collaboration with the National Thin-Film PV Module Reliability Team. Development of the 40W glass/glass packages was extended to a new 80W product - two nominally 40W circuit plates laminated to a common front sheet.

SSI independently and in conjunction with TFPPP team activities has pursued improved understanding of CIS processes and devices. Extending this work, options for minimizing or eliminating transient effects have been demonstrated during this subcontract. The importance of transient effects is primarily related to production rather than long-term outdoor stability; thermally induced transients are not observed in the field despite daily and seasonal changes in module temperature. Transient effects are an important issue for production since they complicate all activities related to measurements: product ratings, definition of measurement protocols, accelerated testing, etc. The results of process R&D throughout the contract led to some decreases in transients; for example, modifying CdS thickness and sulfur content. The new sputter dose process has demonstrated good performance, decreased variation in long range structure of the absorber layer and particularly has reduced transients. This is a major success and in general, exploration of the full potential of the sputter dose process has just begun.

These production R&D results, production volume, efficiency, high line yield and advances in understanding, are a major accomplishment. The demonstrated and maintained high production yield is a major accomplishment supporting attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. Process and packaging R&D during this and previous subcontract has demonstrated the potential for further cost and performance improvements. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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Introduction

Overview

Multinary Cu(In,Ga)(Se,S)$_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells fabricated at NREL have exceeded 19% efficiency [4]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [5]. Record breaking efficiencies of over 12% for a commercial large area module have been verified by NREL [6]. Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field-testing for over sixteen years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [5].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [5, 7]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic
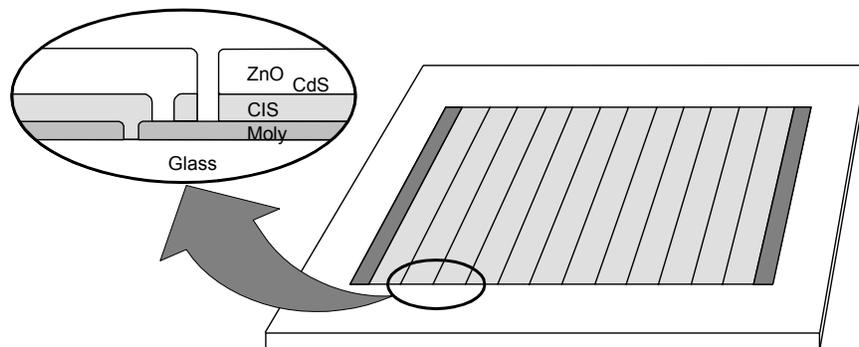
Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [5]. The technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon

(a-Si), cadmium telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [5]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme that is for the most part independent of the thin film technology. Costs for alternative substrates and encapsulation schemes are similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Shell Solar is approximately 11%. This performance is at the lower end of the range for products based on crystalline silicon. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most photovoltaic products are designed for 12-volt or higher applications, but the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically; the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary

ZnO	2.2 µm
CdS	<0.05 µm
CIS	1.2 µm
Mo	0.35 µm
Glass	2 mm
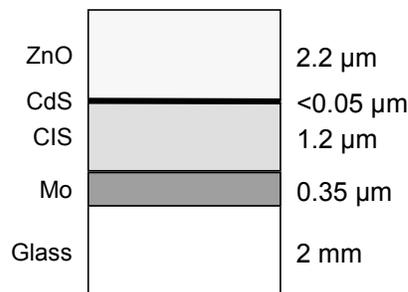
Figure 2. SSI's CIS cell structure (not to scale).

sodalime window glass, which is cleaned and an SiO_2 barrier layer is deposited to control sodium diffusion and improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step

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┌──────────┐     ┌──────────┐     ┌──────────┐     ┌──────────┐
│ Prepare  │────▶│ Deposit  │────▶│   Cut    │────▶│ Deposit  │
│Substrate │     │  Base    │     │Isolation │     │Precursors│
│          │     │Electrode │     │  Scribe  │     │          │
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│ Absorber │────▶│ Junction │────▶│   Cut    │────▶│ Deposit  │
│Formation │     │Formation │     │Interconnect│   │Transparent│
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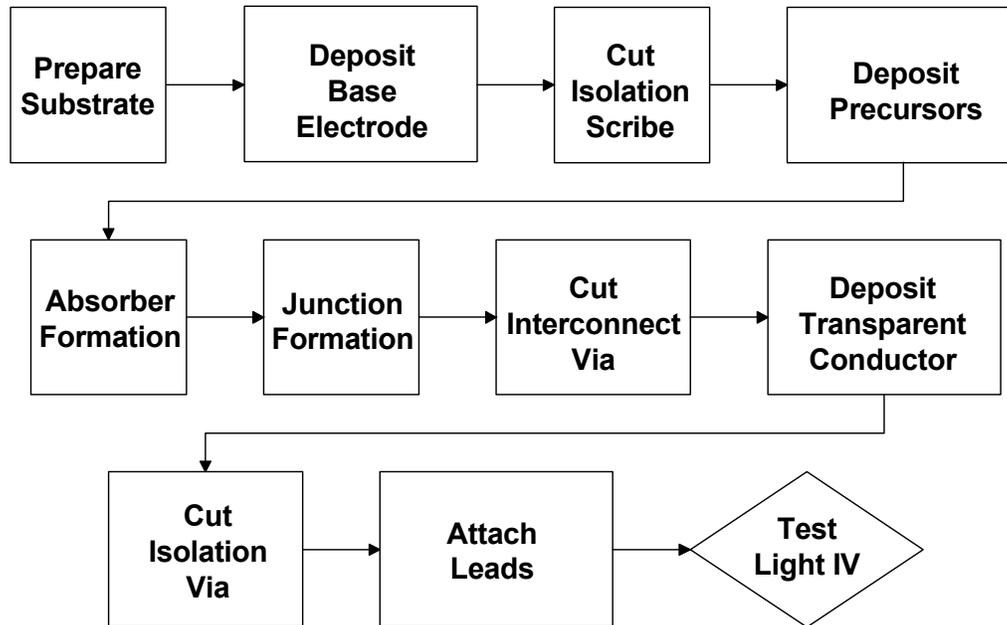
Figure 3. SSI CIS Circuit Processing Sequence.

(referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. Deposition of the precursors occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (15 at% Ga) and then from a pure indium target. During this subcontract an additional deposition was implemented which is discussed in the technical review. CIS formation is accomplished by heating the precursors in H_2Se and H_2S to form the CIS absorber. Beginning at room temperature, furnace temperature is ramped to around 400ºC for selenization via H_2Se, ramped again to around 500ºC for subsequent sulfidation via H_2S and followed by cool-down to room temperature. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer" layer. A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher gallium concentration at the back. Elemental profiles typical of the SSI graded absorber

3

structures are presented in Figure 4. Efficiency, voltage, and adhesion improvements have been demonstrated for the SSI graded absorber structure [1, 8, 9].
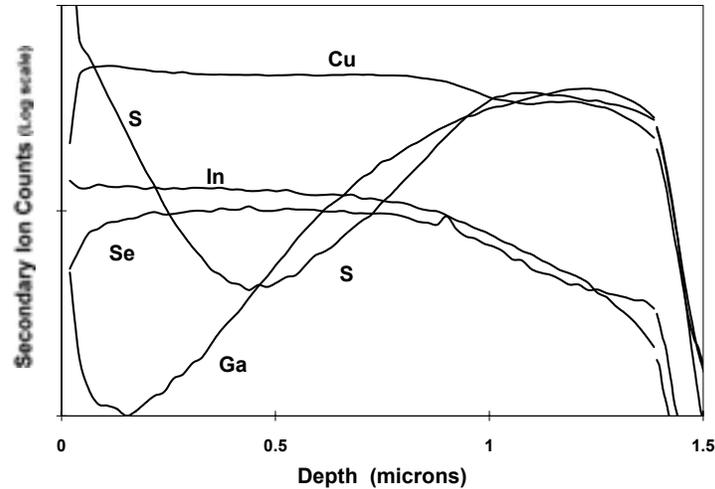
Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 5 illustrates the module configuration used for prototypes and products during this subcontract. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

Figure 5. Single circuit plate module configuration with a TPAT backsheet.

SSI's CIS processing facility produces nominally 1x4 ft. circuit plates for production and process R&D. Full size 1x4 ft. circuit plates are used for ST40, 40W product. Smaller modules in the ST series of products are cut from identical circuit plates; processing through all CIS device fabrication and monolithic integration process steps is the same for full size 1x4 ft. and smaller modules.

Subcontract work included demonstration and adoption of a new module design.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using structures that exercise all aspects of large area module production [10]

- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [11, 12].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [13]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability as measured using the SPC discipline and compared to a predictable baseline process. Confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

Background

The purpose of the Thin-Film Photovoltaics Partnerships Program (TFPPP) is to accelerate the progress of thin film solar cells and module development as well as to address mid and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust modules of 15% aperture-area efficiency. Furthermore, this research is directed at making progress toward this objective by achieving interim goals in thin film module efficiencies; cell and module processing; cell and module reliability and the necessary fundamental research needed to build the technology base that supports these key areas. Participation in the National R&D Teams is paramount to the success of this project. The DOE/NREL/NCPV strategy in undertaking this R&D effort is to maintain the good coupling between laboratory results from fundamental materials and processes research to manufacturing R&D, pilot-line operation, and early entry of advanced thin-film PV products to the ever-growing worldwide marketplace.

The purpose of this subcontract, as part of the Technology Partners Category, is to accelerate the progress of thin film solar cell and module development as well as to address mid and long-term research and development issues by achieving aggressive interim goals in thin film module

efficiencies; cell and module processing; cell and module reliability; and in the technology base that supports these key areas.

Objectives

The primary objectives of this subcontract are to:

- Address key near-term technical R&D issues for continued CIS product improvement

- Continue process development for increased production capacity

- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals

- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability

- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that will last up to 30 years while retaining 80% of initial power

Milestones

SSI shall perform each of the above tasks with the goal of meeting the following targets:

- Scale the substrate size from 1 ft. x 4 ft. to approximately 2 ft. x 5 ft. by the end of the subcontract.

- Achieve pilot production rates of 9,000 kW per year by the end of the subcontract.

- Demonstrate commercial, low-cost, reproducible, high yield and robust module process that achieve the DOE goal for 15% aperture-area efficiency

- Deliverables for the subcontract include CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation.

Deliverables

SSI will deliver 10 representative CIS-based module products at the end of each phase of the subcontract.

SSI will deliver 10 representative CIS modules to the NREL Module Testing Team by the end of each phase of the subcontract.

Technical Review

Capacity and Product Line Expansion Overview (Terms and activities)

Because subcontract activities overlap, many activities are mentioned before they are discussed in detail. This overview is meant to extend the context of SSI technology for discussion of subcontract activities and introduce terms and activities, particularly those that overlap multiple sections.

Most production infrastructure, with the exception of absorber formation reactors, is compatible with larger circuit plates - up to nominally 2x5 ft. Overall capacity increases can be achieved by increasing the substrate size; however, reviewing this approach in light of recent process developments has led to the conclusion that substrate size scale up may not be the only or best route for increasing capacity. Production capacity increases have been achieved through process development to increase the number of substrates processed in an absorber formation batch. This process development addressed tendencies toward increased warping and poorer adhesion for larger substrate loads. Increased capacity by stacking reactors one over another, using the floor space that would normally be required for one reactor, has also been demonstrated. Higher power products can be fabricated using multiple circuit plates rather than larger circuit plates; prototype modules using two 1x4 ft. circuit plates have been tested and the approach adopted for a new product. This two circuit plate product will be referred to as an "ST80" in this report although the final product name has not been determined. Increasing the substrate size is an option that has potential value and will continue to be considered, particularly as a longer-term option.

Production and process R&D have been based on nominally 1x4 ft. circuit plates that are used for the ST40, 40W product. Smaller products and R&D samples have typically been cut from these circuit plates. The module configuration with a TPAT backsheet illustrated in Figure 5 has been used for production of four product sizes, with and without frames, and for R&D. During this subcontract three additional module configurations have been used for process, capacity and packaging R&D: circuit plates designed for a nominally 40W glass/glass package, two nominally 40W circuit plates laminated to a common tempered glass front sheet forming a "ST80" and minimodules. R&D results based on using these packages are reported for efforts ranging from absorber formation studies to packaging studies.

SSI developed "glass/glass" package designs primarily to decrease packaging costs. Simplification of the package and decreased operating temperature are additional potential advantages. Figure 6 is a sketch comparing the present production package and a single circuit plate glass/glass package. In addition to decreased cost, simplification of the package may increase yield. Decreasing the operating temperature will lead to higher efficiency for modules in the field.

Glass / TPAT

Glass / Glass

Cover Glass

EVA

Thin Films

Circuit Plate

Ribbon **EVA**

Ribbon

Seal

**Aluminum
Frame**

Tedlar/Polyester/Al/Tedlar
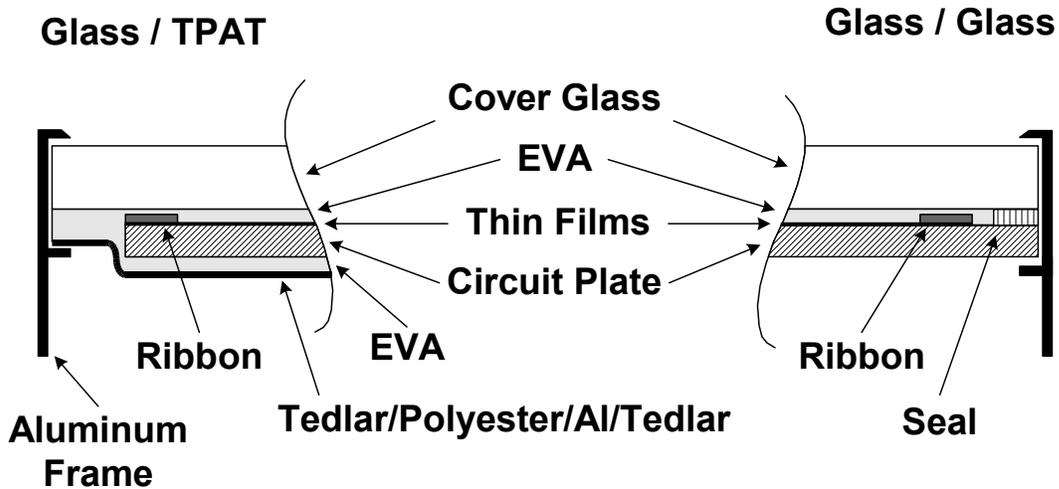
Figure 6. "TPAT" backsheet and "glass/glass" package designs.

Progress toward developing and testing glass/glass packages using a single 40W circuit plates will be reported. These results were extended to a new 80W product (ST80) made using two nominally 40W circuit plates laminated to a common tempered glass front sheet.

Process development primarily during the third subcontract phase emphasized demonstration and implementation of a "sputter dose" process developed by our Munich R&D colleagues [14]. As implemented at SSI, a compound containing sodium is sputtered on the Mo base electrodes prior to deposition of nominally standard precursors and the precursors are processed through nominally the baseline SSI process. The sputter dose process decreased variation in absorber structures and decreased transient effects.

SSI studied and began production of a new product - a 6cm by 6cm minimodule with a plastic encapsulant for consumer applications (Figure 7). This new product would potentially expand near-term and long-term manufacturing capacity scale-up options. Minimodule circuit plates were used as a tool for production R&D such as for position dependent mapping of processes.

Figure 7. Potential 6cm by 6cm minimodule for consumer applications.

Process development to define environmental packages for minimodules, which have unique requirements, led to new understanding of general packaging issues and to new process options. However, minimodule production was ultimately abandoned in favor of power module production.

Early subcontract work emphasized R&D for circuit plate and product size increase while yield and performance issues were emphasized for production of ST40 products. This was followed by a campaign to develop and introduce a minimodule product, which was abandoned. The emphasis when returning to production of large modules was restaffing and retraining for high yield production, IEC qualification and development of an ST80 product. During the last phase of this subcontract, the sputter dose process was introduced.

Process R&D

Performance and Capacity

During this subcontract NREL confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm^2) CIS module (Figure 8). The aperture area for this champion module was defined by taping off the approximately 1 cm inactive boarder surrounding the monolithically integrated CIS circuit in a ST40, 40W, production module. Other than definition of the aperture area, this module is simply one module from the upper end of the production distribution for standard modules. During the third subcontract phase, similar modules made using the sputter dosed absorber formation process were submitted to NREL for measurement as champions and for later use as reference modules. Measurements for one of these modules on the NREL Large Area Constant Source Simulator (LACSS) were within 2% of the NREL measurements of the previous champion.

	Module	per Cell	
Eff	12.8		%
Pmax	46.5		W
Voc	25.3	0.601	V
Isc	2.7		A
Jsc		30.8	mA/cm^2
FF	69.2		%
Area*	3626	86.3	cm^2
Cells	42		

* Aperture area - including interconnect loss
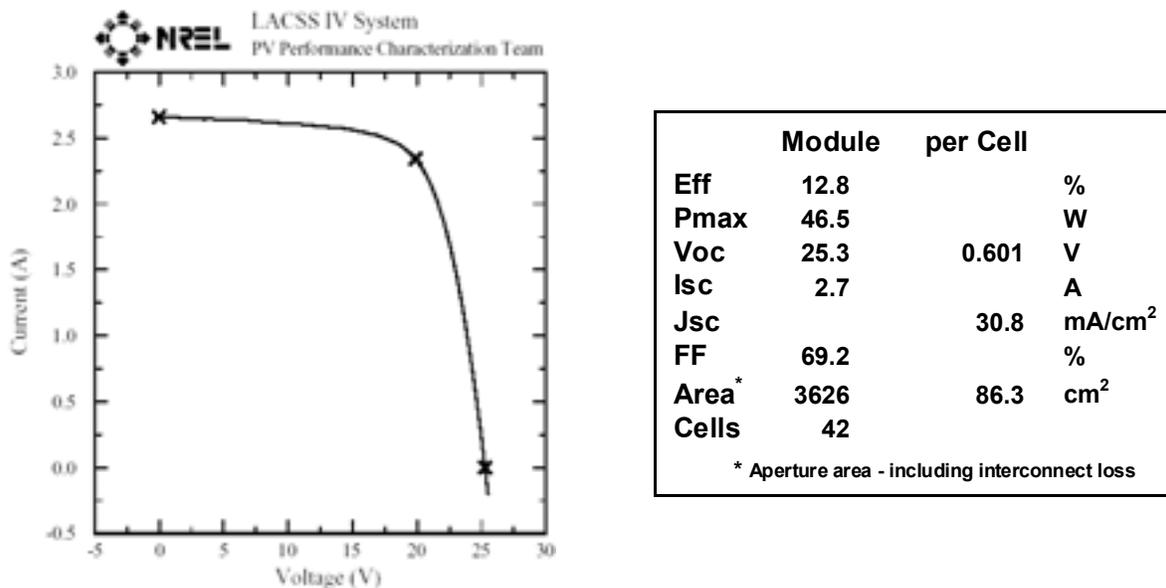
Figure 8. Champion ST40 module from the upper end of the production distribution.

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SSI product measurements are made using a large area pulsed solar simulator (LAPSS) typically with an outdoor exposure prior to the measurement. SSI regularly compares calibration of this simulator with NREL measurements and agreement has been consistently good. For example, modules with sputter dose processing were recently measured at NREL. All LAPSS parameters are within ±2% of NREL outdoor measurements (SOMS). All LAPSS parameters are within ±4% of the average parameters for three NREL simulators.

Figure 9 is the production distribution for approximately twenty one thousand ~1x4-ft. laminates produced during 2003. The average efficiency of this distribution is 11.0%. A Normal distribution fit to the main portion of the distribution yields a standard deviation of 0.60%. Over 88% of this production output is over 10% efficiency. This distribution is nominally the same as
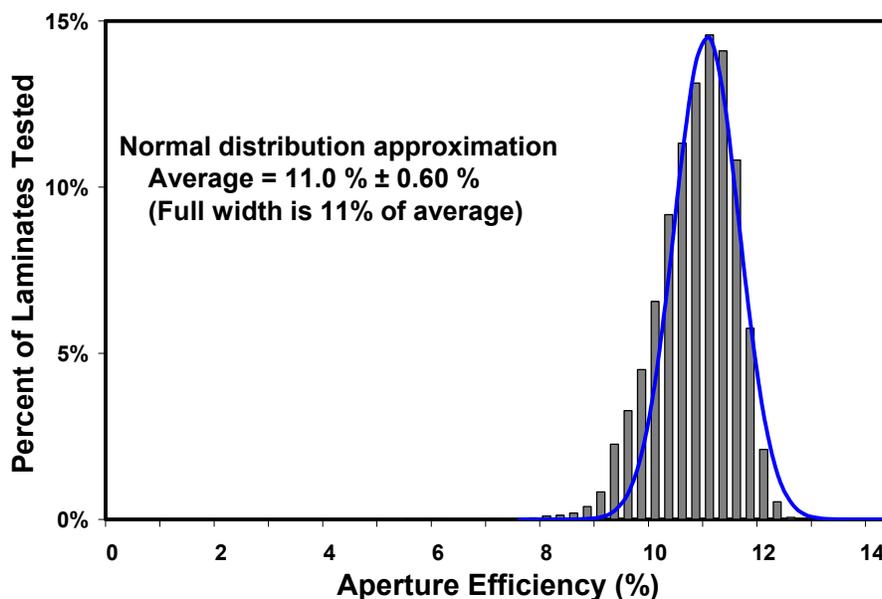
Figure 9. Production distribution for 1x4-ft. laminates produced during 2003.

the distribution for 2002 but with an approximately 33% increase in production volume.

The DOE "Solar Energy Technologies Program, Multi-Year Technical Plan 2003-2007 and Beyond" (MYTP) defines technical targets for specific PV technologies that are deemed necessary to achieve national significance for PV industries [15]. A progression of targets are defined for assumed "baseline systems" that are deployment scenarios developed for 2020 goals. The 2003 MYTP technical target for the baseline system incorporating thin-film modules is 8% average module conversion efficiency [15, Table 4.1.1-1]. The accomplishment demonstrated by the production distribution data in Figure 9 substantially exceeds the 2003 MYTP technical target. The potential to meet the 2007 MYTP technical target of 12% average module conversion efficiency is demonstrated by the NREL confirmed champion 12.8% aperture area conversion efficiency.

Process changes for optimization of the sputter dose process continued through the end of this subcontract. For example, exploring improved transient behavior, even at the expense of lower efficiency, was started during the subcontract and continues. Therefore, there is no large population to report during this timeframe for any one of the sequentially introduced baseline sputter dose processes. The best available comparison between the previous baseline process and a sputter dose process is for an early sputter dose process that is no longer baseline and that exhibited better efficiency but higher transients than later baseline sputter dose processes. Table 1 compares this sputter dose process with a sample of circuit plates processed during the same timeframe but with the previous baseline process (data for unencapsulated circuit plates).

Table 1. Performance comparison with and without the sputter does process.

	Eff*	V_{oc}	J_{sc}	FF	P_{max}	Number
Pre Sputter Dosed	11.5	0.538	36.2	0.592	41.9	326
Sputter Dosed	12.3	0.557	36.8	0.601	44.8	470
Difference	7.0%	3.6%	1.8%	1.5%	7.0%	

* Circuit plates

Historical production rates through to the beginning of the minimodule campaign are charted in Figure 10. Prior to 2003, the data is for ST40, 40W product and smaller modules in the ST series of products produced using the same circuit plate design. Data for 2003 also includes some data for the 6cm by 6cm minimodule consumer product. Capacity during 2003 was somewhat less than 3 MW per year whereas production for 2003 was just over 1.2 MW per year. Introducing the mini module product accounts for the main difference between production and capacity during 2003. No comprable data 2004 is available because of discontinuing minimodule production and restarting production of large modules. Restaffing after shutting down minimodule production and retraining for high yield production began with the goal of achieving the previously demonstrated production rate of about 3 MW per year by the end of 2005. Module fabrication will be moved from a nearby SSI building that also performs module fabrication for silicon products to the buildings housing CIS circuit plate production. With this move, CIS production personnel will be responsible for all aspects of CIS production.
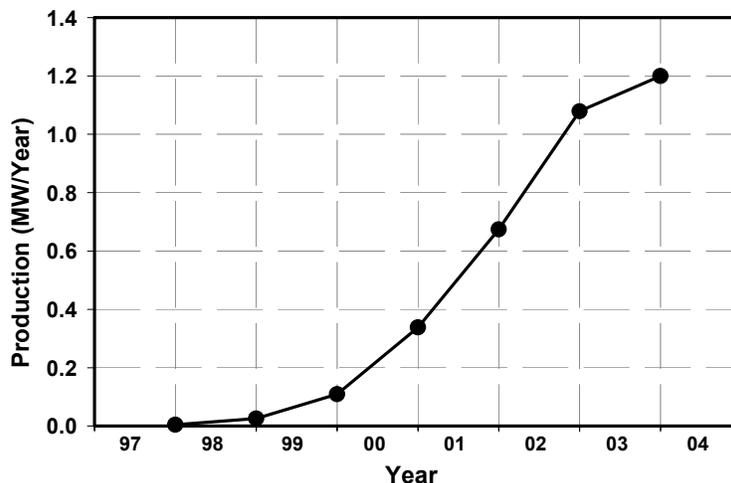

Figure 10. Historical production rate including the first phase of this subcontract (2002).

Capacity grew through improvements in production equipment, processes and procedures. Equipment utilization improvements and process changes allowing decreased process time were implemented for base electrode deposition, precursor deposition, absorber reaction, buffer deposition, ZnO deposition and patterning steps.

Dramatic increases in CIS line yield were demonstrated [16, 17]. Line yield is defined as the ratio of two areas – the area of product produced divided by the area of glass started through the production line. This is a total yield including both electrical yield and mechanical yield through all processing required to produce products. Figure 11 illustrates yield improvements over
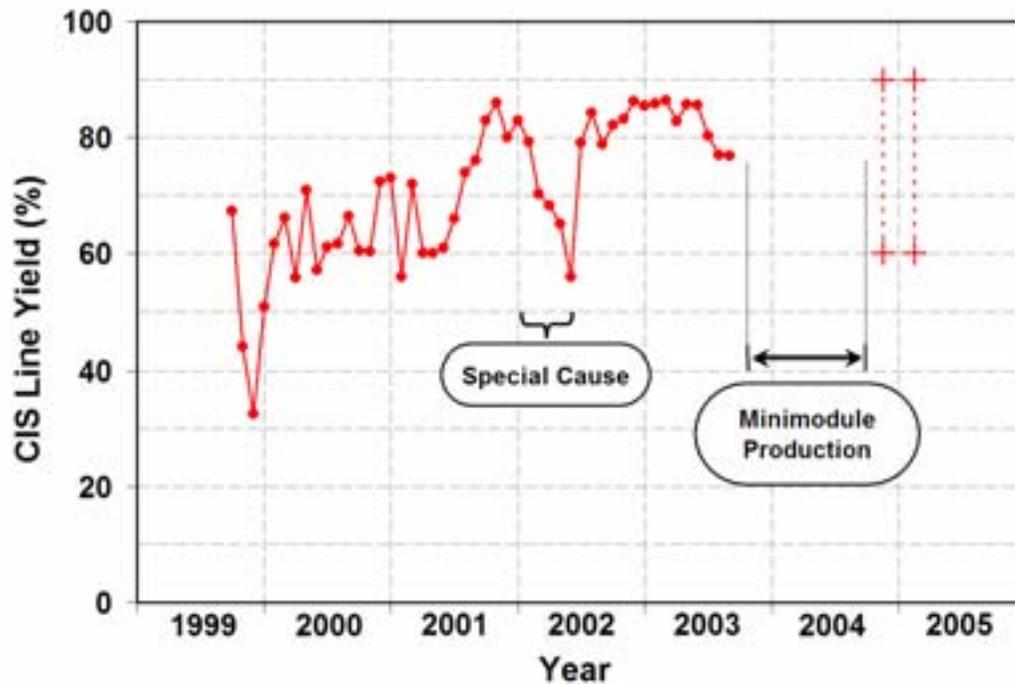
Figure 11. Yield improvements.

approximately the last five years. Yield data from 1999 through 2003, through the beginning of minimodule production, is plotted on a monthly basis. Line yield increased from about 60% in 2000 to about 85% in 2002 and high yields were demonstrated throughout 2003. These dramatic yield improvements were due to continuous improvement of all processes and this major accomplishment supports attractive cost projections for CIS.

Yield since restarting large area module production late in 2004 has been tracked for each product in the ST product line rather than based on total area for all products. Also, yield is posted weekly rather than monthly which inherently introduces more variability in the statistics. Another difference between yield data for previous and the present baseline with the sputter does process is that aesthetic criteria have become more stringent. Yield has been good but variable. Estimates for total area yield made to be more consistent with earlier data, but still on a weekly basis, are plotted in Figure 11 for the last quarter of 2004 and the first quarter of 2005. Weekly

total area yield ranges from about 60% to about 90%. This variability is expected for increasing capacity, restaffing and retraining. Implementation of the sputter dose process also introduced variability as process parameter updates were made based on R&D to decrease transients and the data from the first production scale experience.

The drop in yield through the first half of 2002, Figure 11, was due to peeling. This was found to be due to setup and wear issues for a glass washer. As in versions of SPC definitions for a process that is "in control" and a "special cause", finding and addressing this special cause lead to the immediate and permanent return to high yield. This is an example of the judicious application of manufacturing engineering disciplines such as SPC, analysis of variation and design of experiments that led to clear definitions of near term yield issues. Based on this guidance, the dramatic improvements in monthly yield through this subcontract were the result of improving production protocols and addressing disparate special causes for process variation. Significant improvements were made by developing protocols and procedures for sun soaking modules prior to final testing. Yield improvements as the result of process development included:

- Decreased breakage at multiple process steps related to handling and process definition

- Elimination of shunting along the laser scribe in the Mo base electrode related to both the Mo deposition and laser patterning processes

- Decreased loss due to equipment failures by improving control systems and production procedures

- Decreased peeling related to glass cleaning, precursor deposition, the reaction process, reactor uniformity, and ZnO deposition

- Decreased loss of process runs by improving infrastructure for higher capacity and yield

Process Development

As an example of subcontract work leading to yield improvements, process development led to yield improvements for newly implemented equipment [18]. SSI defined the requirements and procured laser barcode scribing and barcode reading equipment with the goals of increasing capacity by improving productivity and providing high quality data for SPC. Figure 12 illustrates the corner of a circuit plate with both a readable serial number for humans and a 2-dimensional barcode for machines.
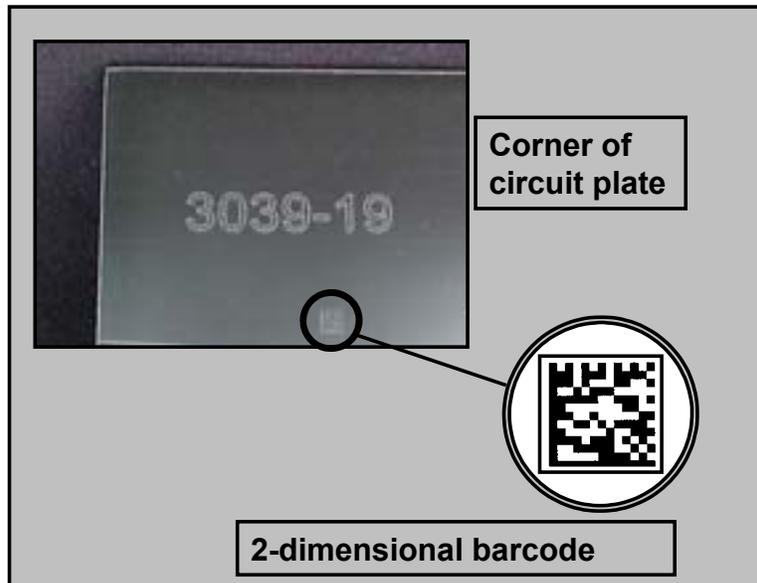
Figure 12. Laser scribed readable serial number and a 2-dimensional barcode.

Laser barcodes scribing replaced hand scribed serial numbers. A study of yield loss due to breakage during the absorber formation process demonstrated that breakage associated with hand scribed serial numbers was one of the major causes of breakage. The use of laser scribed barcodes reduced this kind of breakage by 88%.

Cell gridding and IV and QE measurements were performed by the Battelle/Pacific Northwest National Laboratory group headed by Dr. Larry Olsen (PNNL). Samples were taken directly from the power module production line and therefore representative of production processing. These tasks supported subcontract work on efficiency improvements, yield improvements, study of transient effects and substrate size and capacity scale-up. Procedures and fixtures were developed to create gridded devices on sections diced from patterned production circuit plates. PNNL accommodated SSI needs by changing to grids and hardware for generating the same measurements for minimodules.

Figure 13 illustrates the position of "slices" and cells used to characterize a nominally 1x4 ft. circuit plate. Seven "slices", nominally the same as 5W, ST5 product, were made and measured at SSI to map performance parallel to the long dimension of a 1x4 ft. circuit plate - front to back in a reactor. Samples for cell measurements at PNNL were selected to duplicate this sub-module slice data and extend the data to sample vertical position dependence within the reactor – top to bottom in the illustration.

Top

| 1.1 | | 2.1 | | 3.1 | | 4.1 | | 5.1 | | 6.1 | | | 7.1 |
| 1.2 | | 2.2 | | 3.2 | | 4.2 | | 5.2 | | 6.2 | | | 7.2 |

Slice 1   Slice 2   Slice 3   Slice 4   Slice 5   Slice 6   Slice 7

| 1.3 | | 2.3 | | 3.3 | | 4.3 | | 5.3 | | 6.3 | | | 7.3 |

| 1.4 | | 2.4 | | 3.4 | | 4.4 | | 5.4 | | 6.4 | | | 7.4 |
| 1.5 | | 2.5 | | 3.5 | | 4.5 | | 5.5 | | 6.5 | | | 7.5 |

Bottom

Front   Rear
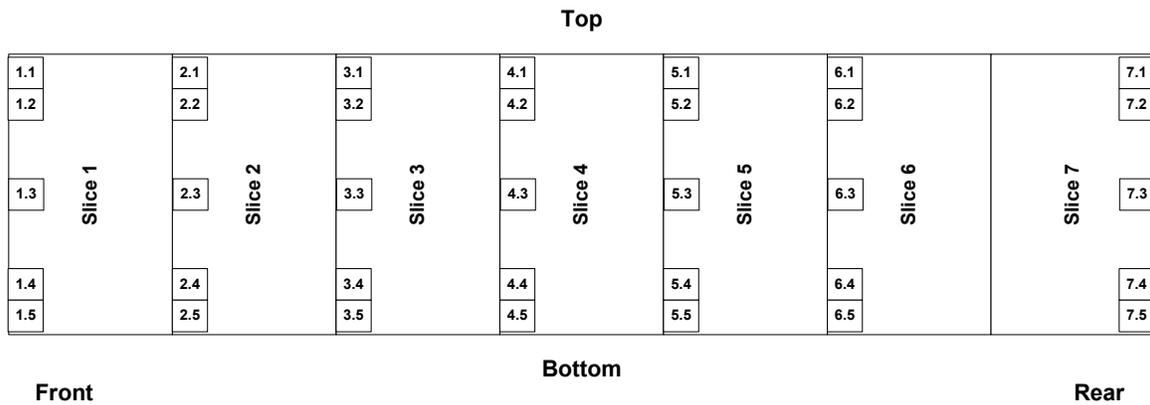
Figure 13. Sub-module slice and cell positions on a nominally 1x4 ft. circuit plate.

Correlations were observed between position within absorber formation reactors and cell IV parameters. The intercept on the energy axis of the square of quantum efficiency versus photon energy was taken as a measure of effective bandgap - a convolution of the effects of absorption and collection through the varying bandgap structure of absorbers. As an example of the results of the efforts with PNNL, the bandgap was found to be well correlated with long wavelength QE, peak QE, Jsc (Figure 14), Eff and position (Figure 15) but not correlated with the short wavelength QE. This indicates that the front to back variation in Jsc is likely due to elemental
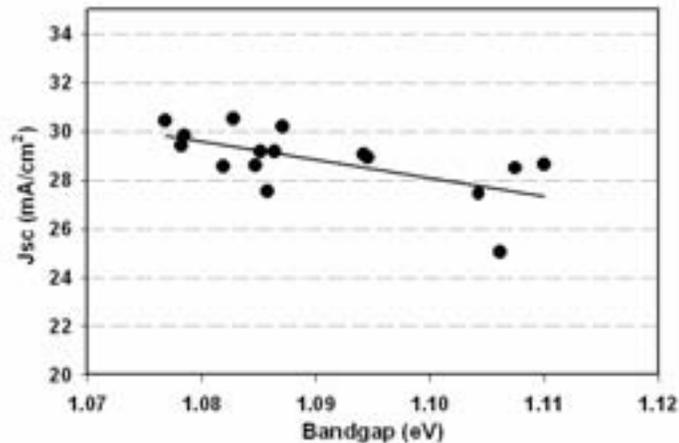
Figure 14. Correlation between bandgap and Jsc.

profile variation in the absorber. The variations observed in these studies were relatively small but important for guiding continual improvement. Efficiency and yield production data, Figure 9 and Figure 11, include the impact on performance of variation indicated by this mapping data. These results are detailed in the second annual report for this subcontract [19] but are not

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repeated in this report since the results are for a baseline process prior to adopting sputter dosing and therefore obsoleted by later subcontract work.
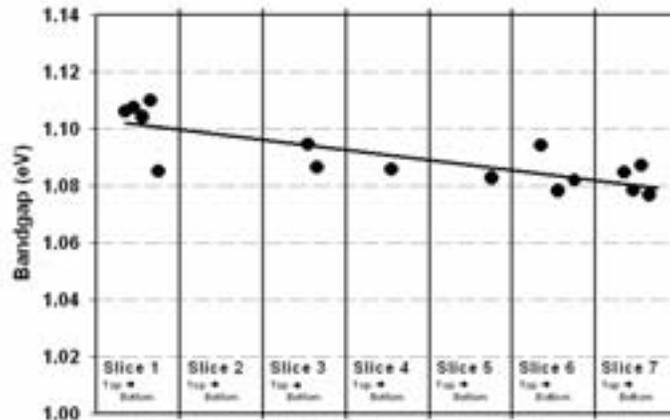

Figure 15. Correlation between bandgap and position - front to back in a reactor.

SSI presently deposits a Mo base electrode and precursors in the same sputtering system. Purchasing an additional sputtering system and performing these processes in separate systems is a scaleup option that could more than double capacity. However, purchasing substrates with the barrier and base electrode layers is another scaleup option if quality and cost criteria can be met. The possibility of using purchased base electrodes with a barrier coating was explored during this subcontract.

Prior to this subcontract work, shunting along laser P1 scribes sporadically caused poor performance. Studies of the interdependence of laser processing conditions and Mo properties, including water or O_2 incorporation during deposition, were conducted to address this issue [3]. An affected Mo region along the edge of the patterned Mo was found to be dependent on both base electrode deposition conditions and laser parameters but primarily on Mo deposition conditions. The affected region is typically seen as lifting and cracking along the edge of the patterned Mo and leads to shunting. Within the range of laser parameters explored, which did not include pulse durations shorter than 10 ns, modifying laser parameters could only minimize the affected region. Only modifying the Mo deposition conditions could eliminate the affected region.

An affected region was found for the purchased Mo and module performance was poor due to shunting. Figure 16 and Figure 17 are optical micrographs of laser-produced scribes in SSI baseline Mo and the purchased Mo. Although features in the glass at the center of the scribe in baseline Mo may appear suspect, there is minimal lifting at the edge of the scribe. Lifting at the edge of the scribe and cracking is observed for the purchased Mo.

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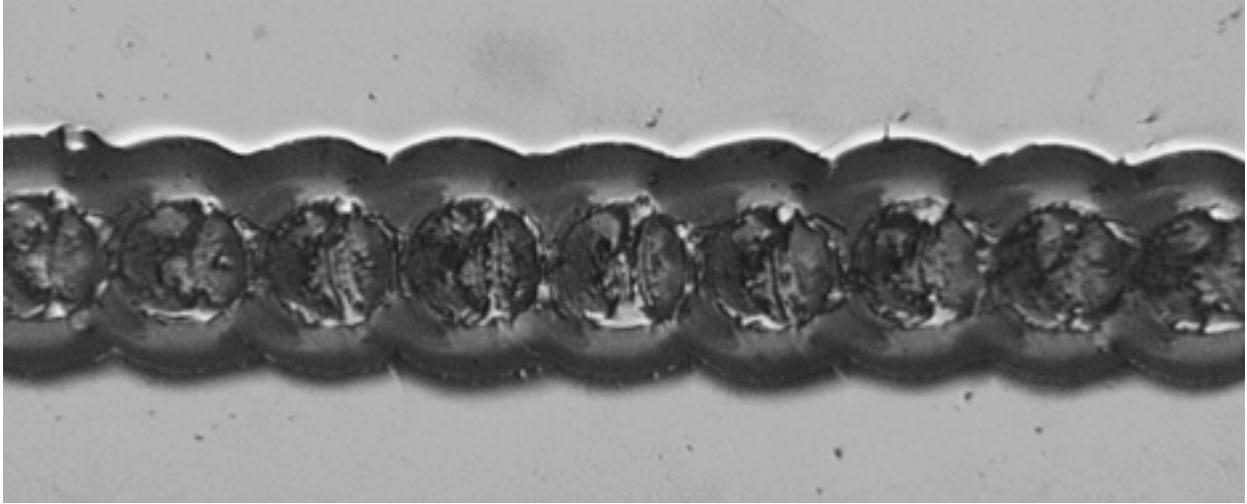
Figure 16. Laser scribed pattern in SSI Mo base electrode.
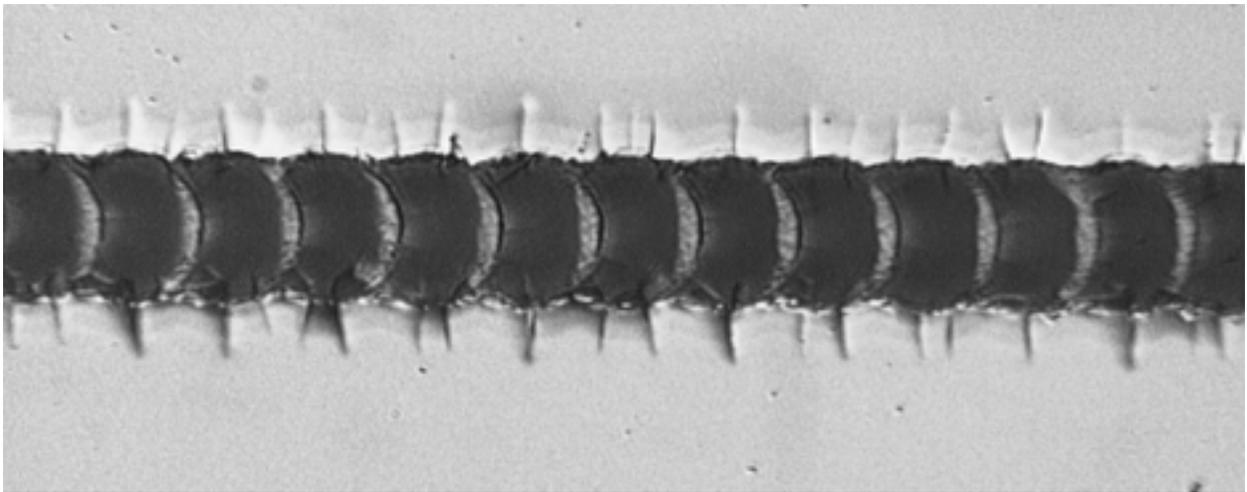
Figure 17. Laser scribed pattern in commercial Mo base electrode.

Dektak scans in Figure 18 quantify differences in lifting at the affected region for SSI baseline Mo and the purchased Mo. Damage at the center of the scribes is also seen in the Dektak scribes. This damage has been further studied by etching off the Mo and characterizing the damage using optical micrographs and DekTak scans. The damage does not appear to have a first order impact on performance. The impact of the pattern in the Mo on sodium content is discussed below.

SSI Mo　　　　Purchased Mo

0.4 μm

⊢⊣
50 μm
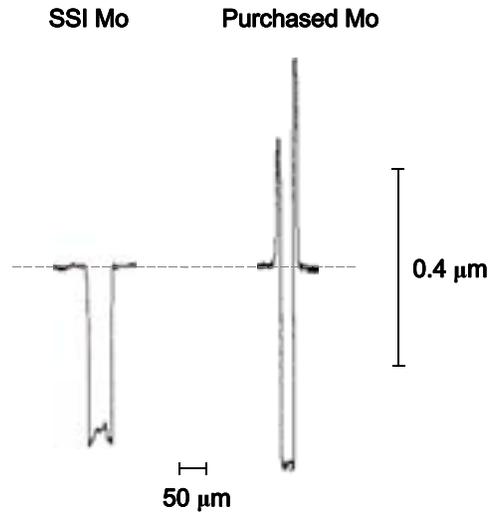
Figure 18. DekTak scans for SSI baseline Mo and the purchased Mo.

SSI products have subjective aesthetic requirements making features that are sometimes seen after selenization, "dark spots", a yield issue. CIS has an aesthetically pleasing uniform black appearance. Dark spots may disrupt this uniformity if the product is viewed close up; the dark spots are not typically visible from a few feet away.

Dark spots typically appear as differences in shades of gray for circular features with dimensions on the order of one or two millimeters. The shades of gray are related to surface texture differences that range from barely noticeable to dramatic and there may be concentric rings with differences in surface texture. Dark spots typically surround a "dark core" (Figure 19). When present, the size of the dark core varies from barely noticeable at the magnification used for Figure 19 to about 0.04 mm.   Dark cores are nearly invisible to the naked eye because of their small size. With few exceptions, dark cores are observed at the center of a dark spot; however,

⊢ 0.1mm ⊣
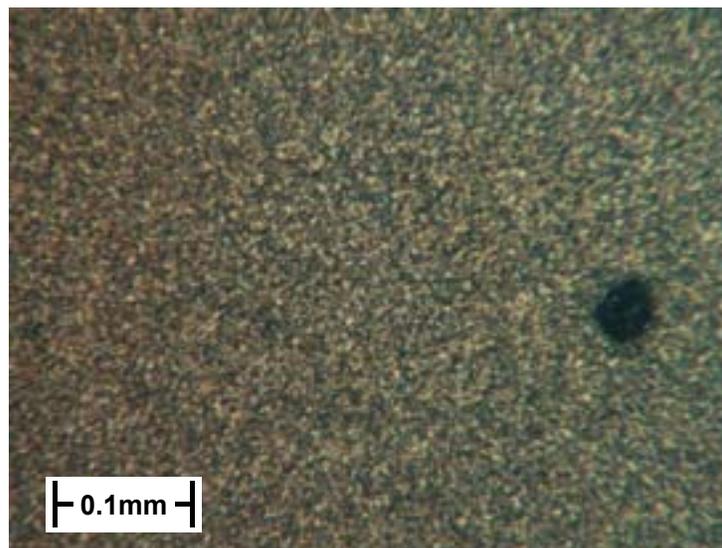
Figure 19. Optically micrograph of a dark spots with a dark core.

dark cores are often observed with no surrounding dark spot. Dark spots at times appear centered on the Mo patterning typically with no dark core.

Sally Asher, NREL, coordinated analysis of samples with dark spots in parallel with analysis of the absorber structures for standard production processes and for process variations; these particular process variations were not defined specifically to explore dark spot generation but samples with dark spots were included in the sample set. NREL has identified the dark cores, or minimally some dark cores, as indium rich regions reacted with sulfur and selenium . Figure 20 is a SEM image of a dark core and Figure 21 is an AES indium map of the same area. These
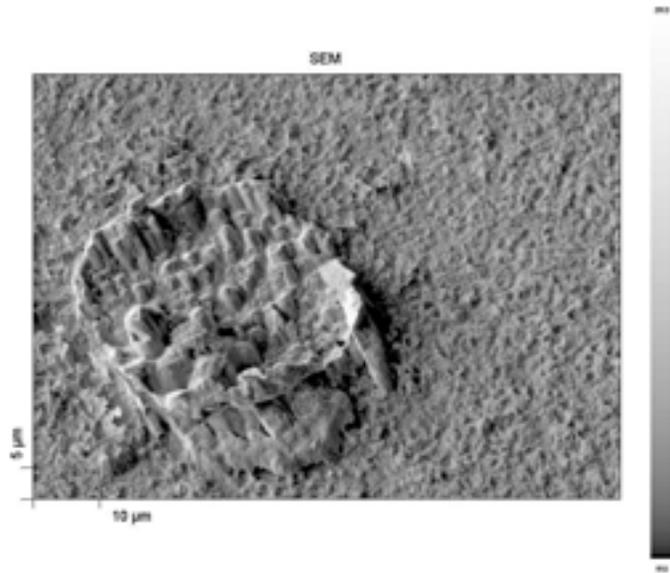
Figure 20. SEM image of a dark core (NREL).
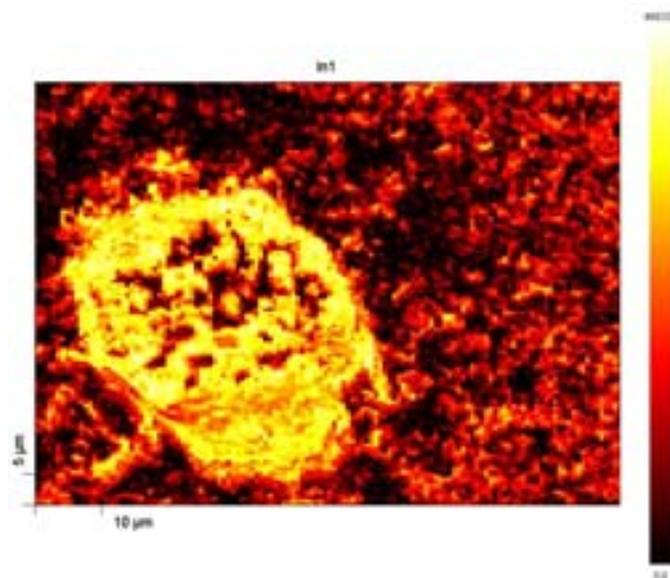
Figure 21. AES In map of a dark core (NREL).

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results are consistent with nonuniform indium sputter deposition, "spits", as the source for some but not all dark cores and dark spots. Specifically, spits are at times seen on precursors with a density of about 20/cm^2, whereas the density of dark cores and dark spots in some locations is much higher.

Present understanding is that dark spots do not have a significant impact on performance although the probability of generating dark spots may correlate with process parameters that do have an impact on performance or adhesion. This is consistent with initial results from NREL indicating that the elemental profiles are nearly identical for the area of a dark spots and typical areas. Although dark spots do not have a significant impact on performance, process R&D was pursued because of the aesthetics issue and to gain understanding of the limits of process options.

Changes in both precursor and absorber formation processes have been shown to decrease the number or visibility of dark spots potentially at the expense of adding additional processing or compromises in performance. Modifying the thermal profile for absorber formation dramatically decreased the occurrence of dark spots but with a potential negative impact on adhesion, process variation and yield. Planarization of precursors by buffing practically eliminated dark spots. However, this process would require further development for production. The appearance of Mo after removing the CIG (for example using tape) is different in the immediate area around a spots and for regions that tend to generate high or low spot densities. Also, improved adhesion may be indicated for the same changes in the precursor formation processes that decreased the number or visibility of dark spots.

NREL performed SIMS depth profile analysis on pre sputter dose baseline absorbers where the precursors faced the glass of an adjacent substrate during absorber formation and two types of absorbers with a low sodium contribution from the reactor. Incorporation of sodium from the uncoated side of an adjacent SLG substrate during absorber formation was suppressed in one case by facing the precursors toward each other and in another by facing the precursors toward an SiO$_2$ coated glass plate ("Face to Face" and "Facing SiO$_2$" in following figures). For analysis, four samples for each process type were selected from approximately the center of the long dimension of the 1x4s. The four samples mapped the position dependence along the short dimension of the 1x4s ("top to center to bottom").

SIMS analysis on each sample included a depth profile for three types of mass analysis: positive ions, negative ions and "molecular" species where the signal is from Cs combined with the elements of interest. NREL typically performs these three profiles to obtain sensitivity to low concentrations of multiple elements (positive and negative scans) and to minimize ambiguity due to geometric effects and matrix effects – differences in signal levels due to the dependence of ion yields on local bonding. Comparing scans helps with interpretation of results from the smaller grain and void region, "fine grain region", at the CIS/Mo interface (see for example Figure 25). However, ambiguity remains due to the combination of matrix effects and the convolution of signals from multiple depths resulting from depth profile sputtering on a sample with surface roughness and particularly with the structure of the fine grain region. DekTak measurements are used to define the depth scale. No corrections are made for surface roughness, sputtering rate differences for different structures in the absorber or sputtering rate differences for CIS and Mo.

Figure 22 displays the sodium depth profiles for the three types of absorbers. Mo and indium are charted for position reference and to show the very good repeatability for SIMS analysis in

general and particularly for the other constituents in this sample set. Sodium levels in pre sputter dose baseline absorbers are higher relative to the low sodium absorbers for all depths or absorber structures (front of the absorber, the fine grain region and in the Mo) and relatively independent of position on the plate. For both low sodium absorbers, there is a distinct top to middle to bottom trend with higher sodium levels near the plate edges. Sodium levels in the front of the absorber (to a depth of ~0.5μ) are lower than in the fine grain structure. This may be due to high surface area in the fine grain structure near the CIS/Mo interface.
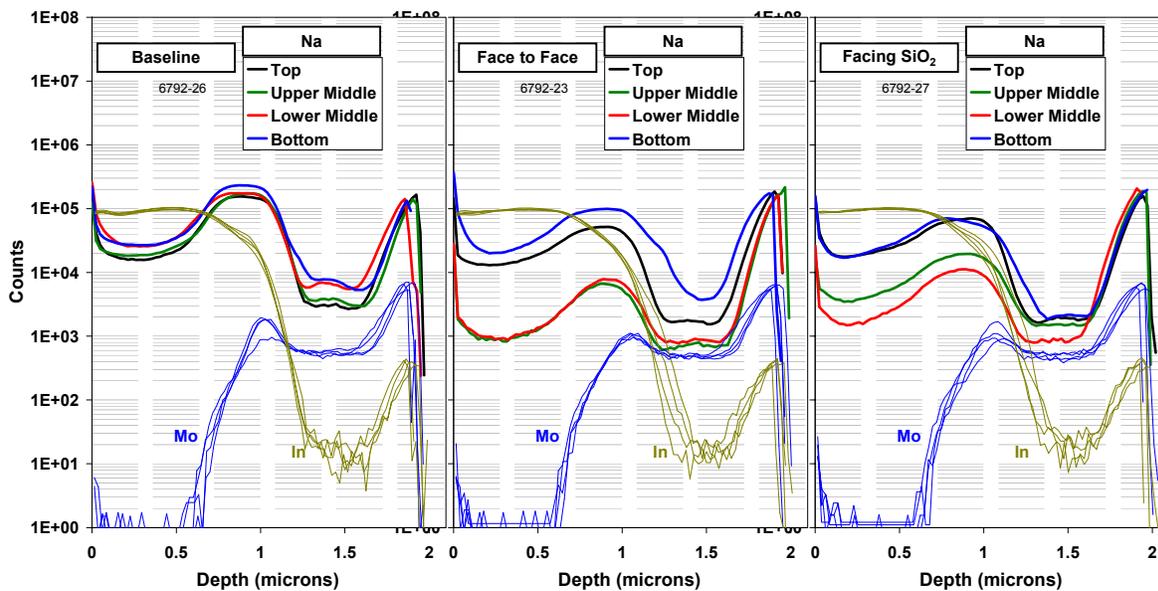
Figure 22. Positive ion depth profiles for Na.

Figure 23 summarizes these results. Representative sodium concentration ("Counts") data in the absorber and in the fine grain region ("Na Near Mo Interface") versus plate position are plotted for the three types of absorbers. These results are consistent with sodium diffusing from the
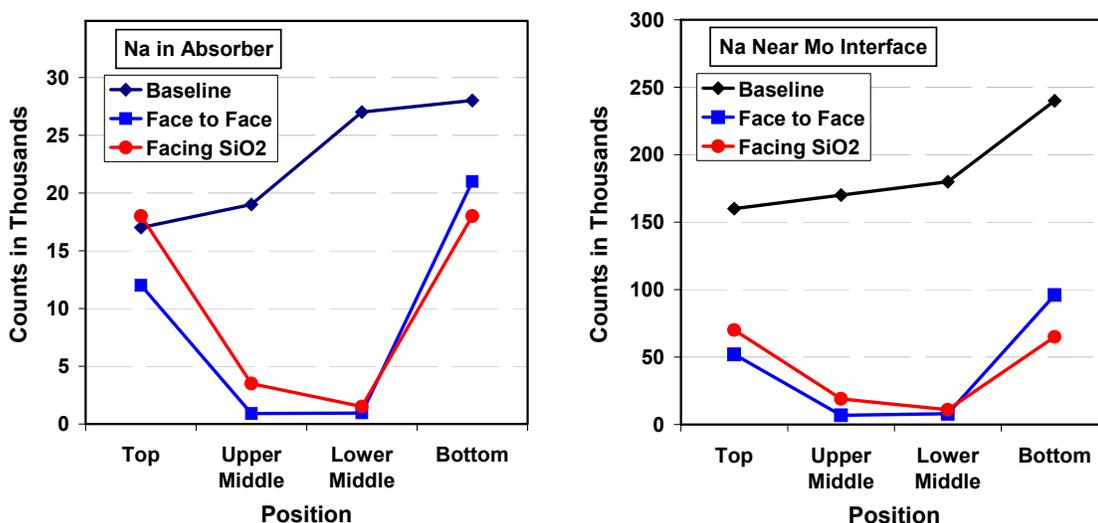
Figure 23. Representative sodium concentration versus plate position (pre sputter dose baseline).

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edges or diffusing from other plates through the reactor and preferentially contributing to sodium in the absorber near the edges of the low sodium plates. NREL analysis of the sodium content variation with position laterally across the absorber between patterning lines indicates minimal variation in the absorber, which indicates that the pattern in the Mo base electrode is at most a secondary source of sodium [20].

NREL provided SSI with SEM micrographs of absorber structures selected to explore the impact of process R&D on dark spot formation, transient effects and the impact of sodium content on adhesion [21]. Sally Asher, NREL, coordinated this study in parallel with SIMS analysis. The study emphasized crossections to explore structural differences in the "fine grain" region near the Mo/CIS interface that is characterized by fine grains and voids. Although there are few images for each sample type, imaged areas were selected as being "typical". Images of areas for the following conditions were supplied:

- Relatively low transients (pre sputter dose baseline)
- Relatively high transients (pre sputter dose baseline)
- Lower Na content
- Modified precursor formation processes for decreased dark spots

The two baseline absorber images, Figure 24 and Figure 25, are typical; a fine grain or gravelly appearance at the Mo/CIS interface, voids are common near the Mo/CIS interface and the main absorber has fairly large (on the order of the film thickness) "grains" or fracture features.

4933-14-3

800nm 35000X
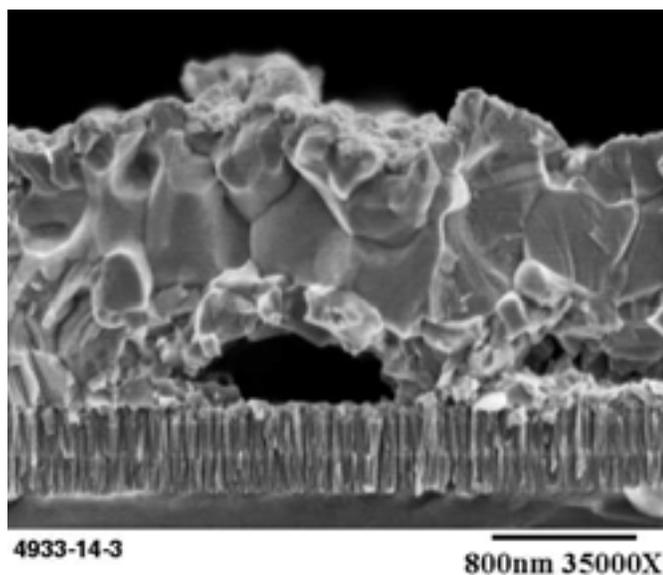
Figure 24. Baseline processing, area with higher thermal transients.

5065-16-3   800nm 35000X
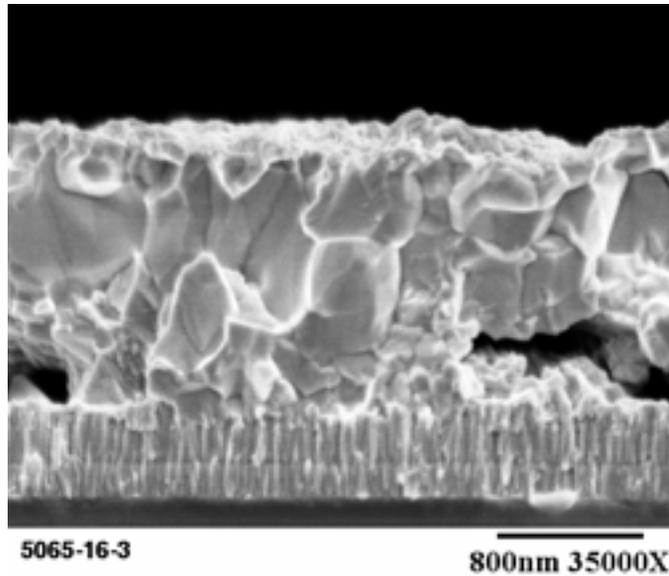
Figure 25. Baseline processing, area with less thermal transients.

The grains are not dramatically different for the two samples; however, grain size is not necessarily a predictor of performance. No distinction between the two samples seems possible; there appears to be no dramatic difference in absorber structure (pre sputter dose baseline) that correlates with transient effects.

The void region is extensive for absorbers with decreased sodium content (Figure 26) and the fine grain, gravelly appearance, at the Mo/CIS interface is more extensive.

5038-14-3   800nm 35000X
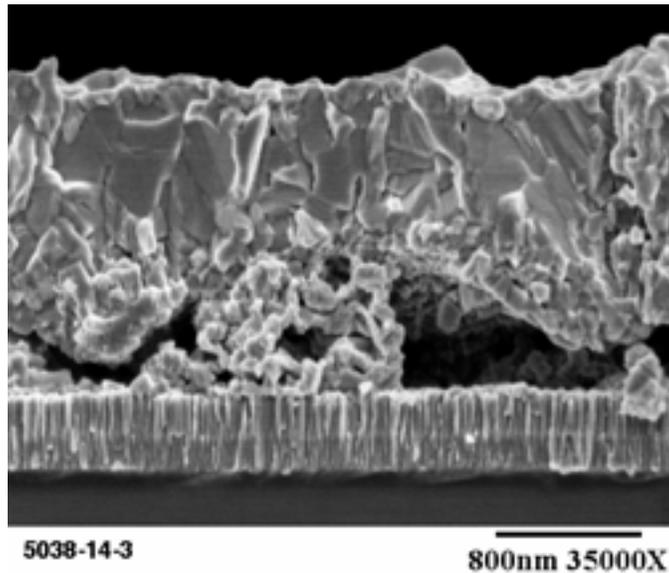
Figure 26. Baseline processing modified to decrease sodium content.

The appearance (Figure 27 and Figure 28) of absorbers (in this case also with ZnO) formed from buffed precursors seems to support the observation of better adhesion:

- A more continuous fine grain or gravelly appearance at the Mo/CIS interface
- Smaller or much smaller voids near the Mo/CIS interface
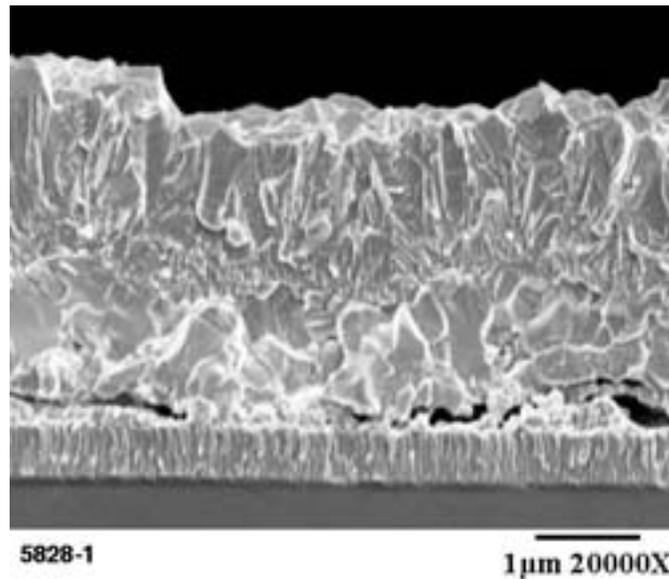
Figure 27. Modified precursor process to decrease spots.
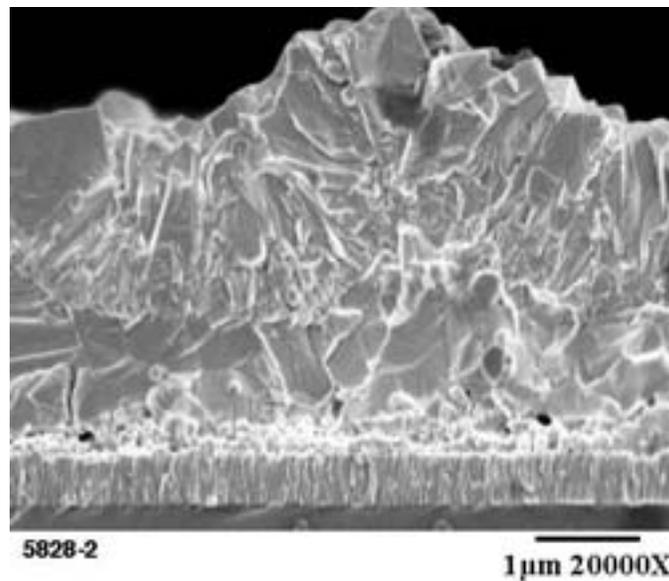
Figure 28. Modified precursor process to decrease spots.

The absorber thickness is variable for the modified precursor process however differences in the appearance of the main grains are within the variation seen for baseline absorbers. The CIS (and ZnO) appears to be thicker at one location in Figure 28 while maintaining a good CIS/Mo interface.

A third process modification implemented during this subcontract, sputter dosing, dramatically decreased the occurrence of dark spots and is now being pursued exclusively. The original impetus for pursuing sputter dosing was to decrease transients. Transients have been decreased and efficiency improved while demonstrating good adhesion, no or minimal dark spots and improved overall visual uniformity.

Circuit plates without sputter dosing are not always visually uniform, even after ZnO deposition that dramatically decreases the visibility of nonuniformities. Circuit plates with sputter dosing consistently exhibit a more uniform appearance. Figure 29 and Figure 30 illustrate the visual appearance for a nominally 1x4 ft. circuit plates prior to ZnO deposition that exhibit nonuniformities without sputter dosing and uniformity with sputter dosing. Although not visible on this scale, dark spots are minimized by sputter dosing.
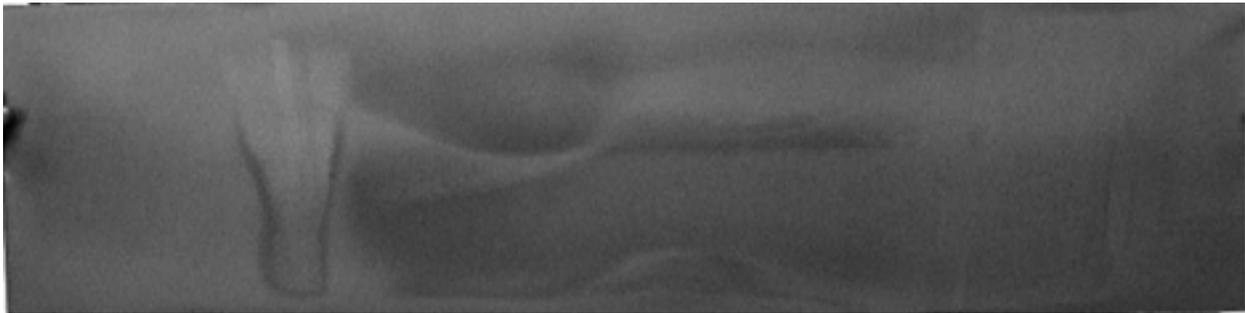
Figure 29. Circuit plate without sputter dosing illustrating frequent nonuniformities.

Figure 30. Circuit plate with sputter dosing.

SSI substrates include a SiO_2 barrier to sodium diffusion between the glass and Mo electrode to avoid poor adhesion and dead areas at pinholes and patterning lines [1]. For SSI absorbers without the sputter dose process, sodium in the absorber is incorporated during reaction of the precursors. The source of sodium is the uncoated side of an adjacent SLG substrate rather than from the substrate on which the absorber is grown. Sodium selenide is observed on the uncoated (i.e. glass) side of circuit plates after absorber formation. This suggests that hydrogen selenide disassociates on the glass surface providing selenium and hydrogen that diffuses into the glass thereby maintaining charge neutrality while sodium diffuses out of the glass. Sodium selenide is the probable molecular species responsible for the transfer of sodium from the glass to the absorber during absorber formation [22].

NREL performed additional SIMS depth profile analysis on pre sputter dose baseline absorbers and two types of sputter dosed absorbers: with precursors face to face during reaction and facing the glass of an adjacent substrate. Four samples for each process type were selected from approximately the center of the long dimension of the 1x4s and used to map position dependence along the short dimension of the 1x4s ("top to center to bottom"). Figure 31 displays sodium and gallium depth profiles based on positive ion analysis for each of the three types of absorber. Mo and indium are charted as references to the positions of absorber and Mo structures and to show the very good sample-to-sample repeatability for SIMS analysis. Sodium levels in the absorbers with sputter dosing approach or exceed the sodium levels in the pre sputter dose baseline
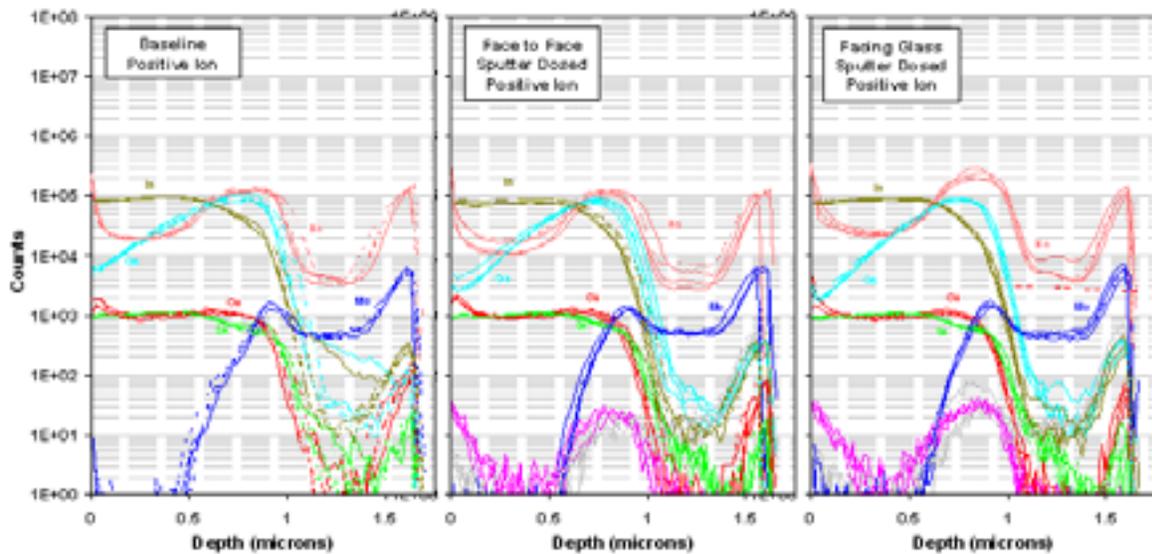
Figure 31. Positive ion SIMS depth profiles of baseline and experimental sputter dosed absorbers.

absorber depending on the availability of sodium from the glass side of adjacent substrates. Variation in the sodium concentration for absorbers without a contribution to the sodium from the glass side of an adjacent substrate (Face to Face) are consistent with sodium from the circuit plate edges or diffusing from other plates through the reactor and preferentially contributing to the sodium near the edges of the substrate. Sodium concentrations through the front of the

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absorber, but excluding the surface, to a depth of about 0.5 μ, appear to saturate at about $2x10^4$ counts if there is adequate sodium available. Sodium concentrations near the back, in the fine grain region, are similar for all samples but highest for the case where sodium is available from both sputter dosing and the glass side of adjacent substrates. A conclusion from the SIMS data is that sputter dosing can provide sodium at levels comprable to the levels incorporated from the uncoated side of an adjacent SLG substrate.

Figure 32 is a chart of circuit power versus relative sputter dose. Efficiency increases and saturates with increasing sputter dose. However, other benefits of sputter dosing, such as
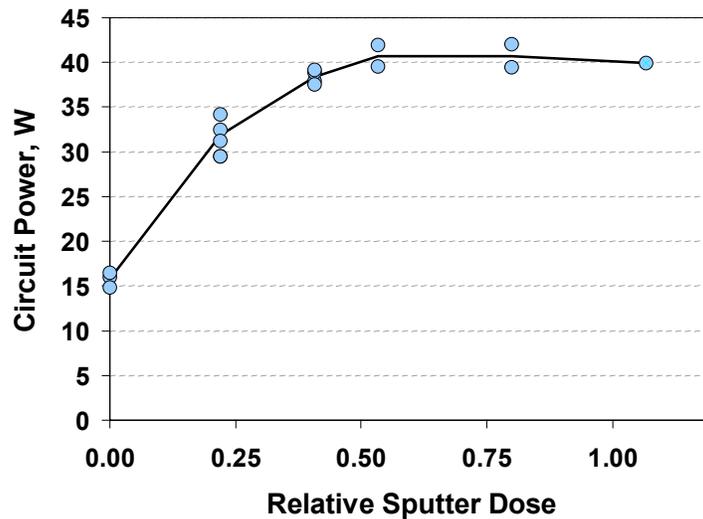
Figure 32. Effect of sputter dose on circuit efficiency.

decreased transients, improved efficiency, good adhesion, no or minimal dark spots and improved overall visual uniformity, may not saturate at the same level and other process conditions during absorber formation can influence results.

SEM images of the pre sputter dose baseline, Figure 24 and Figure 25 can be compared with SEM images in Figure 33 of absorbers fabricated using the sputter dose process [23]. The sputter dose process produces larger grains or fracture features, the void region near the Mo/CIS interface may be more extensive and the extent of the fine grain region is dramatically decreased. TEM analysis of SSI absorbers indicates that grain boundaries are highly ordered rather than a highly disrupted extended grouping of dislocations. Current density is high for CIS indicating that grain boundaries are not strong recombination centers. Data in Table 1 indicates that there is at most a small difference in current density for processing with and without the sputter dose process. This similarity in current density for absorbers with significance differences in the grains and fine grain region is further evidence that grain boundaries in CIS are not strong recombination centers.
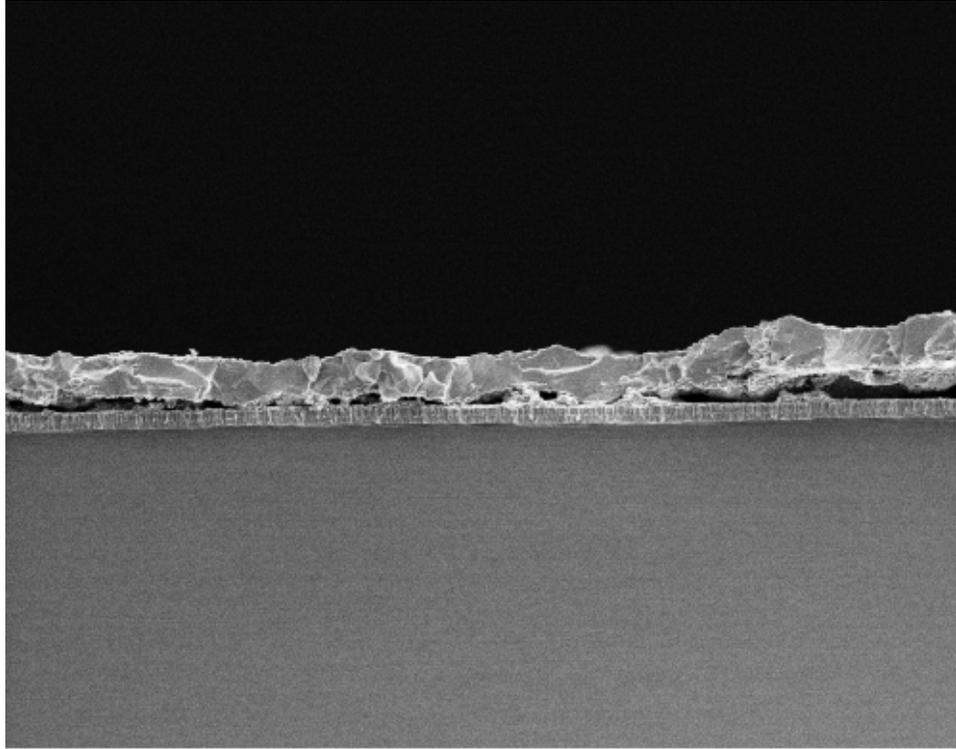
6μm 5000X
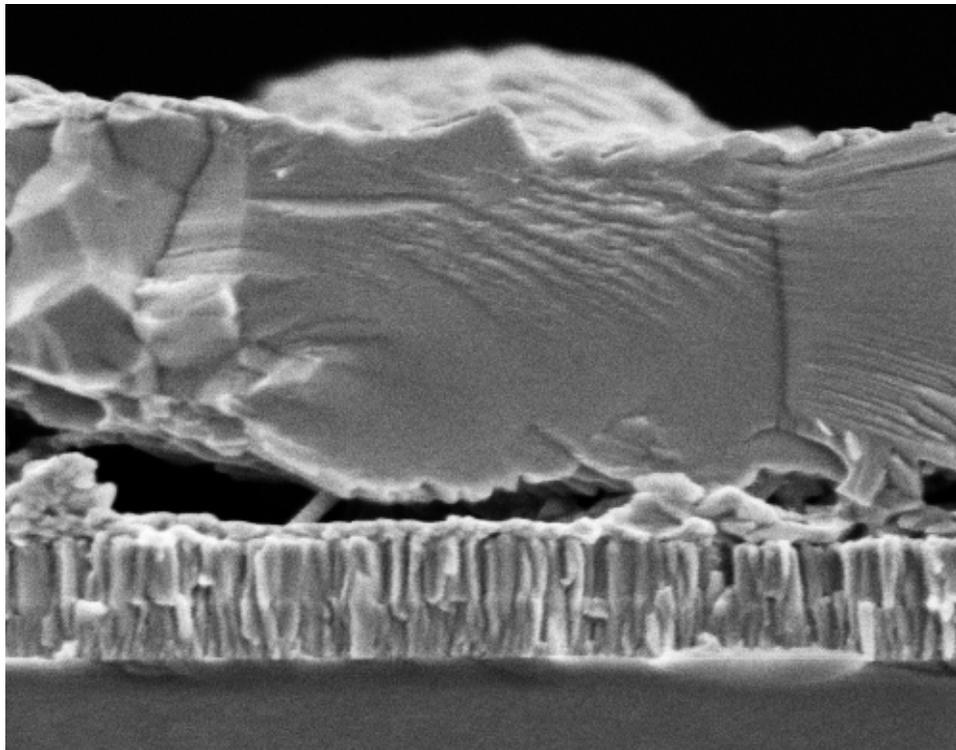
600nm 40000X

Figure 33. SEM images of sputter dosed absorbers.

Process Development - Transient effects

SSI pursued process R&D to decrease or eliminate transient effects. Transient effects introduce issues that are primarily related to production and accelerated testing rather than long-term outdoor stability. Although field failures associated with particular production timeframes, package designs and errors during production have been clearly identified, there is no evidence that transient effects, which have relatively short time constants, impact intrinsic stability or long-term outdoor durability. Thermally induced transients are observed after exposure to high temperatures in the dark during accelerated environmental testing. Thermally induced transients are not observed in the field despite daily and seasonal changes in module temperature. This is consistent with laboratory results indicating that the magnitude of thermally induced transients during accelerated testing decreases when testing is done with illumination, known transient effects are temperature dependent, and the module temperatures reached for actual deployment are less than the temperatures during accelerated testing.

Transient effect are an important issue for production since they complicate all activities related to measurements: product ratings, definition of measurement protocols, accelerated testing, analysis for process definition, analysis of process predictability, interpretation of experimental test results, interpretation of outdoor test results, and analysis for understanding of device structures. For example, measurements after a thermal stress are typically made after a minimum of a two-hour outdoor exposure when conditions allow an exposure over 1/3 sun. Recovery from the thermally induced temporary loss is significant but incomplete for this timeframe. The degree of recovery depends on many aspects of the fabrication process, the details of the thermal stress, weather conditions and actual extent of the outdoor exposure. Variability in the recovery introduces some measurement uncertainty that must be compensated for in experimental design and interpretation of results. For R&D and particularly for production, the two hours exposure is at best an awkward extension of procedures and work.

SSI independently and in conjunction with TFPPP team activities pursued improved understanding of transient effects. Transient effects are difficult to quantify since the magnitude and time constant for transient effects are dependent on processing, handling, light exposure history and measurement protocols. Significant progress has been made through NREL TFPPP teaming activities. Team accomplishments that have been previously reported included:

- Characterization of transient effects

- Definition of a repeatable measurement methodology for systematic study of transient effects

- Demonstration that some potential causes for the effect are not dominant and directed efforts accordingly

- Improved understanding of the effect and CIS devices

- Demonstrated and communicated that transients are important to consider when measuring CIS

- Demonstrated long term stability for normal operating conditions

- Demonstrated process approaches that influence this effect and may eventually mitigate or eliminate the effect, particularly buffer layers and "partial electrolyte" treatments (solutions used during buffer layer deposition)

- Defined areas for future study

Investigation of the impact on transient effects for several processes steps and processing conditions continued during this subcontract:

- Environmental exposure between process steps - Reducing the exposure to ambient humidity before and after the CdS deposition significantly reduces lamination transients.

- Buffer layer variations - Thicker CdS decreases transients while partial electrolyte soaks apparently have no effect.

- Reactor process parameters – Studies for limited variations in process parameters, such as the degree of sulfidation, indicate a dependence on this absorber formation parameter.

- Positions within reactors – Initial results indicate that transients can be, but are not necessarily, dependent on position within a reactor.

- Differences between reactors

- Higher lamination temperature leads to larger reversible changes in device parameters, particularly FF.

- Various coatings on circuit plates before lamination that are typically used to inhibit moisture ingress may also influence the magnitude of transient effects.

- Introduction of the sputter dose process

The following expands on some of these studies.

Transient effects were analyzed for samples from multiple pre sputter dose baseline absorber formation runs made in four reactors. As seen in the following photograph of a reactor for 1x4-foot circuit plates, Figure 34, a group of substrates is loaded in a carrier, placed into the tube reactor, and processed as a batch. The importance of position of 1x4 circuit plates within the reactors was explored by comparing a central plate and a plate from near the outside of the carrier. The dependence on position within the reactor parallel with the long edge of a 1x4 circuit plate, i.e. from the door (front) to the rear of the reactor, was explored by dicing each 1x4 into seven "slices" – each a monolithically integrated sub-module. The end and center slices were laminated while sections of other slices were used for ICP analysis. Each laminate was subjected to nominally 1,000 hours at 85°C and ambient humidity. IV measurements before and after these accelerated test conditions were made after 2 hours of outdoor exposure at over 1/3 sun. These simplified accelerated test conditions for laminates were found to predict behavior through standard high humidity accelerated testing for package designs that provide good protection from water vapor ingress.
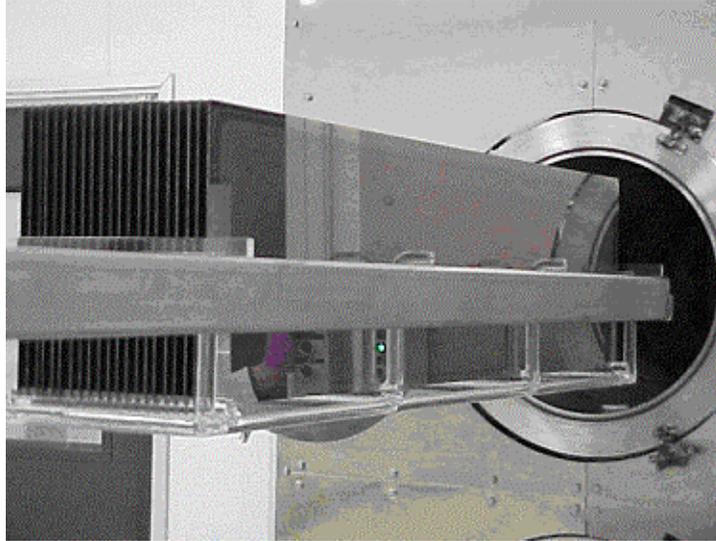
Figure 34. Reactor for 1x4-foot circuit plates.

Results indicated differences between reactors and differences with position within the reactors ranging from minimal to significant. Typical of transient effects, differences in power were dominated by differences in FF. Post thermal exposure data normalized to pre-exposure data for reactors with minimal and significant thermally induced transients are plotted in Figure 35 and Figure 36. In general for all reactors, the door end introduces smaller thermally induced transients than the rear. Similarly, smaller thermally induced transients are generally observed for circuit plates from the outside of the carrier. There was no apparent correlation between position within a reactor or position on a plate and the relatively small variation of sulfur concentration within a run.
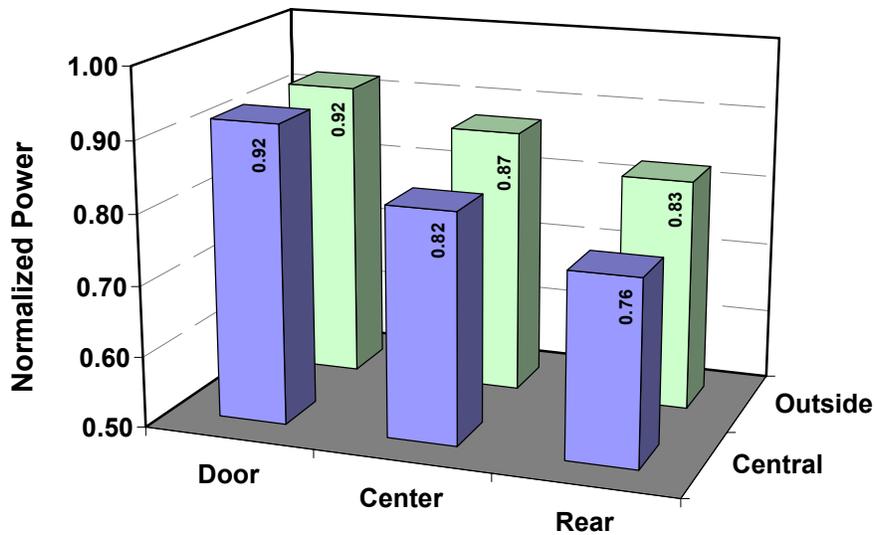
Figure 35. Position dependence of transient effects - reactor with significant variation.

31
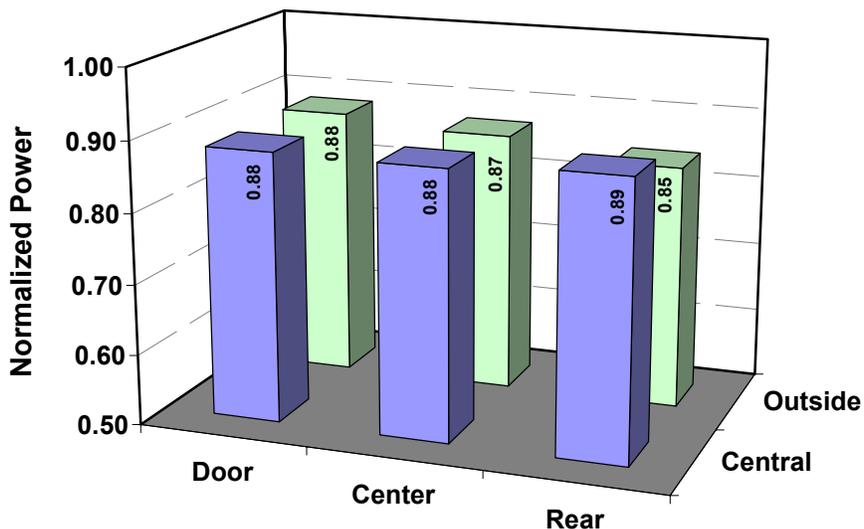
Figure 36. Position dependence of transient effects - reactor with minimal variation.

The impact of sodium concentration variation with reactor position and purposely varied sodium content on transient effects was studied for the pre sputter dose baseline process. Incorporation of sodium during absorber formation from the uncoated side of an adjacent SLG substrate was suppressed in one case by facing the precursors toward each other and in another by facing the precursors toward an SiO_2 coated glass plate ("Face to Face" and "Facing SiO_2" in figures). Performance after an extended exposure at 85ºC was compared for samples fabricated with low sodium, about an order of magnitude lower than typical, and samples from the previously discussed experiment to explore the dependence on position within reactors. ICP analysis was used to determine sodium concentrations. For the relatively small variations in nominal sodium concentration with reactor position, post thermal exposure data normalized to pre-exposure data indicated a weak trend in thermally induced transients with sodium concentration. The trend appears to be real but could not be statistically verified at the 95% confidence level. Samples purposely fabricated with very low sodium content were much more sensitive to thermal exposure; however, the initial efficiency was also very low therefore the significance of this result or comparisons with baseline material is uncertain.

The impact of purposely varied sulfur content on transient effects was also explored for the pre sputter dose baseline process. Performance versus time at 85ºC and ambient relative humidity was tracked for a small number of circuit plates processed using baseline H_2S concentration, 25% of the baseline concentration and 200% of the baseline concentration (Figure 37).
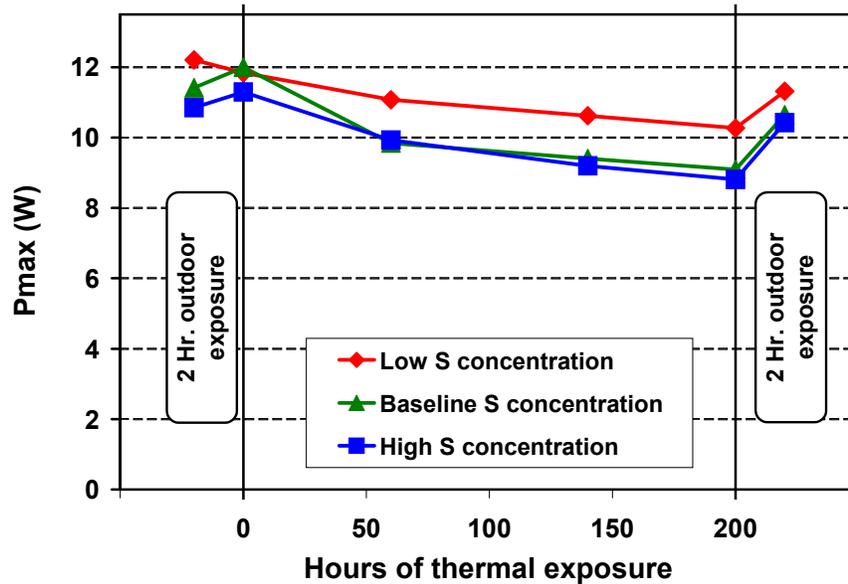
Figure 37. Impact of sulfur content on transient effects.

In contrast with the other two process conditions and typical results, circuit plates processed with 25% of the baseline H_2S concentration declined with the initial outdoor exposure prior to the thermal exposure. Therefore, the starting point chosen for normalization determines the relative stability or relative amplitude of transient effects for the circuit plates in these experiments. Choosing the measurement after lamination and 2-hour outdoor exposure for normalization, as is typical, indicates that the circuit plates processed with lower sulfur content perform better after thermal exposure. There was no indicated difference between the processes when the normalization was to the measurement before the outdoor exposure.

Introducing the sputter dose process significantly decreased transient effects. Figure 38 is a chart of normalized power versus time first for a dark heat exposure of 1,000 hours and then for recovery with outdoor exposure. Results of this dark heat exposure are predictive of results for a hermetic package exposed to standard accelerated test conditions such as damp heat exposure; 1,000 hours at 85ºC and 85% relative humidity. Measurements made during the dark heat exposure include a nominally two hour outdoor exposure prior to measurement on a pulsed solar simulator. The timeframe for outdoor exposure is total hours rather than based on an estimate of the actual sunlight exposed. Without sputter dosing, the power loss during dark heat exposure is highest. Increasing the sputter dose decreases the loss during dark heat exposure; the degree of loss before a two-hour exposure is decreased or the time constant for recovery is decreased. Near total recovery with outdoor exposure occurs for most absorber formation conditions; however, absorbers with the higher sputter dose have less initial loss, less variability in the initial loss and also recover to within the narrowest range at or close to total recovery.

33
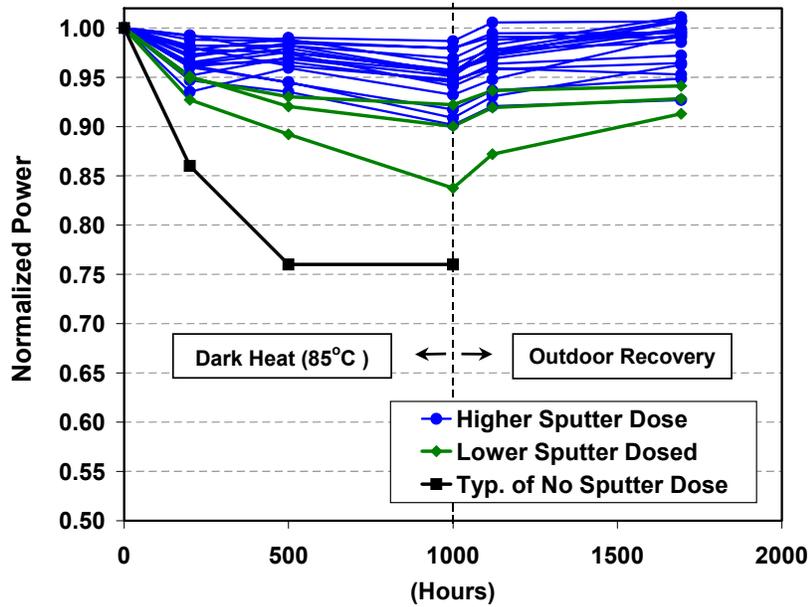
Figure 38. Thermal stability with sputter-dosed precursors.

Figure 39 is a chart of normalized power versus duration of exposure at 85ºC in the dark for combinations of higher and lower sputter dose and higher and lower concentrations of H_2S relative to baseline conditions during absorber formation. Measurements included a nominally two hour outdoor exposure prior to measurement on a pulsed solar simulator. Initial efficiency may be compromised at the lowest H_2S concentrations. Both increasing the sputter dose and decreasing the amount of sulfur in the absorber decrease transient losses during dark heat
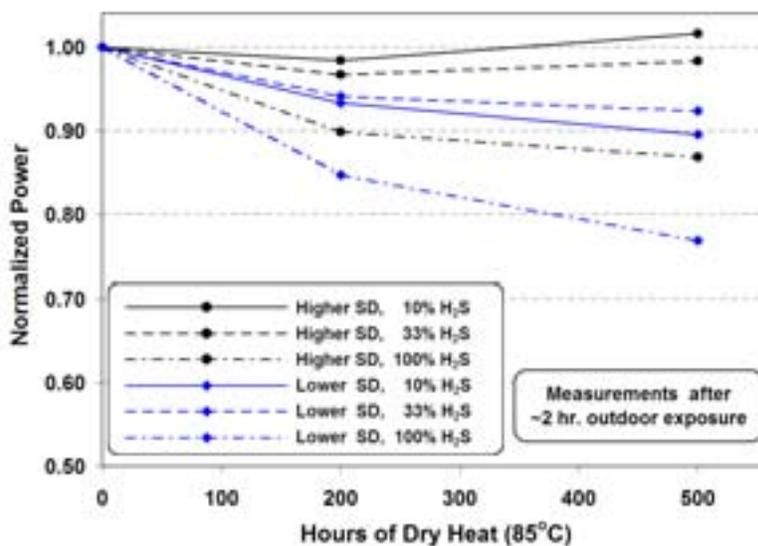
Figure 39. Transient dependence on relative sputter dose and sulfur content.

34

exposure; the degree of loss before the two-hour exposure is decreased or the speed of recovery is increased.

Sally Asher, NREL, used SIMS analysis to explore differences between pre sputter dose baseline absorbers that SSI selected based on the relative degree of transient behavior. Lower concentrations of gallium near the surface correlated with smaller transients. However, this result was not conclusive since sample selection at SSI did not adequately consider the importance of sample position within the reactor or the density of spots. Follow up on this observation was included when analyzing later SIMS data for samples selected to explore the impact of sodium levels and the impact of the sputter dose process on transient effects. A slightly lower concentration of gallium near the front of the absorber (~0.1 μm through ~0.5 μm) correlating with higher sodium levels was observed in SIMS profiles for pre sputter dose absorbers with varying levels of sodium from the reactor, Figure 22. Relative to the pre sputter
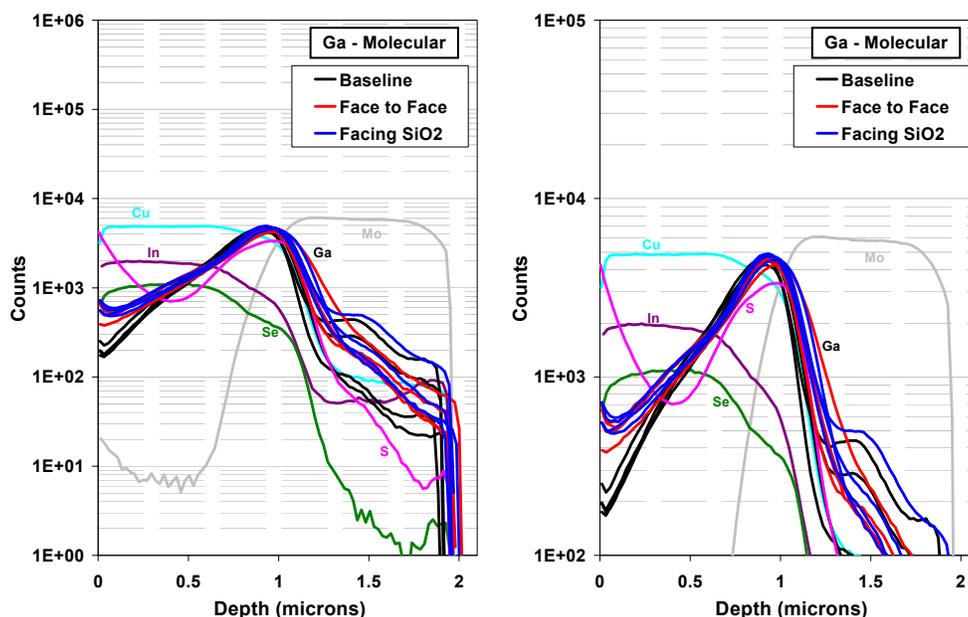
Figure 40. Gallium profile comparisons based on molecular depth profiles (two ordinate scales).

dose baseline process, a similar trend was observed with lower gallium near the front of the absorber for a similar level of sodium introduced by sputter dose processes using two methods to limit incorporation of additional sodium from the reactor (Figure 31). A similar lower concentration of gallium near the front of the absorber correlated with higher sodium availability from the sputter dose process. SIMS determined sodium levels at the front of the absorber (~0.1 to 0.5 μm), near the CIS/Mo interface and through the high gallium region at the back of the absorber were not significantly different for these process variations.

In summary, lower concentrations of gallium near the front of the absorber are observed when increasing the concentration of sodium for the pre sputter dose process, adopting the sputter dose process and when incorporating more sodium with the sputter dose process. SIMS data does not indicate correlation of this trend with changes in the depth of the high gallium region at the back

of the absorbers or the concentration of gallium at the back of the absorbers. Decreasing the sodium concentration in the pre sputter dose process increased the fine grain structure and decreased the "grain size" or fracture surface size (Figure 26). An additional increment in subjective absorber quality as judged by absorber appearance in SEM images is introduced by adopting the sputter dose process (Figure 33). The improvement in transient effects by adopting the sputter dose process may correlate with the improvements in absorber structure. The relatively small changes in measured gallium concentration may be due directly to changes in absorber structure or differences in the SIMS analysis, i.e. the depth convolution of the signal, for changes in the absorber structure. Similarly, the incorporation of sodium in the absorber may be due directly to changes in absorber structure, which is related to when and how the absorber is affected by the constituents introduced by sputter dosing. Any differences in sodium and gallium concentration measured for a finished absorber correlate with decreased transients but may not be responsible for decreased transients.

National CIS R&D Team

During this subcontract SSI contributed to TFPPP National CIS R&D Team activities. Summarizing results for all of the extensive team member activities is not attempted in this report since the expertise for most team activities resides with the team members. Instead, the following experiments are summarized as examples of teamwork where SSI has had major involvement in sample preparation or data analysis.

Vasilis Fthenakis, head of the National Photovoltaic Environmental, Health and Safety Assistance Center at Brookhaven National Laboratory, visited SSI. A review of SSI's process was supplied in advance and Vasilis toured the CIS facilities. The tour emphasized safety systems and Vasilis reviewed the "Process Hazard Analysis Photovoltaics Checklist" that he developed for the Photovoltaics community.

In sample exchanges related to TFPPP team activities, device performance has varied for SSI absorber with buffer and ZnO depositions by NREL or IEC. Consistent good performance for the same sample set has been obtained for SSI absorbers with CdS and ZnO deposited by SSI. The differences in performance for differences in front electrode and buffer layers is an example of R&D for improved understanding of CIS processes and devices undertaken independently and in conjunction with TFPPP team activities.

SSI supplied minimodules and various configurations of 10x10 cm samples for work on barrier coatings by Larry Olsen's group at PNNL. The possibilities for this technology range from alternative encapsulation options for consumer products with minimal environmental protection requirements to enabling low cost PV products with very long lifetimes. These barrier coatings were originally designed for flat organic light emitting diode (OLED) panel displays that are very sensitive to water vapor and oxygen ingress. Initial results are very encouraging [24]. As seen in Figure 41, comparing IV characteristics for coated and uncoated circuit plates that went through accelerated environmental test cycles indicates protection of circuit plates from moisture ingress. This protection can be defeated if the conformal coating is interrupted by steps in the thin films, debris from cutting samples and handling, and surface features that were previously associated with dark spots on SSI circuit plates. Although cost estimates have not been obtained,

the cost of these vacuum deposited multiple layer coatings may be prohibitive. Fewer layers or other potential process variations may provide adequate protection and be cost effective.
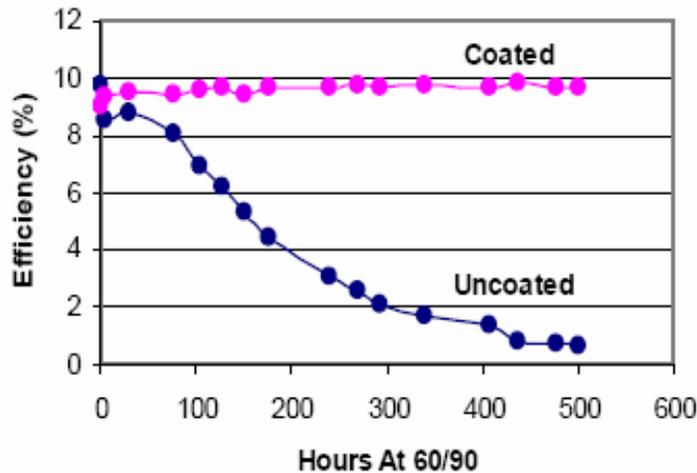
Figure 41. Comparison of accelerated testing results for coated and uncoated minimodules. (From L. Olsen, et al., "Barrier Coatings For Thin Film Solar Cells", National Center for Photovoltaics and Solar Program Review Meeting – 2003).

SSI supplies NREL and other team members with materials from base electrodes to completed modules. The use of these samples ranges from analysis to use as a component in the fabrication of unique devices. SSI also participates in team studies where device structures are completed for other members or partial processing is done for comparative studies. For example:

SSI supplied two types of SSI thin-films to TFPPP absorber team members - complete through $Cu(In,Ga)(Se,S)_2$ absorber formation and complete through ZnO deposition. These films were supplied for electrical characterization at NREL and IEC, and for compositional analysis at NREL, FSEC, and the University of Illinois.

SSI supplied samples of precursors for reaction pathway measurements at Oak Ridge National Laboratories to Suku Kim who is in Tim Anderson's group at the University of Florida.

SSI deposited CVD ZnO on multiple sets of samples with experimental buffer layers from Larry Olsen, PNNL.

SSI supplied absorbers to Kannan Ramanathan at NREL for experiments varying CdS process parameters at NREL with SSI baseline ZnO depositions. The goal is to understand fill factor and open circuit voltage differences for SSI absorbers processed at SSI, NREL and IEC.

SSI supplied thin-films complete through $Cu(In,Ga)(Se,S)_2$ absorber formation for buffer layer experiments at NREL and IEC. Kannan Ramanathan and Raghu Bhattacharya at NREL have made progress on depositing CBD ZnS buffer layers on SSI absorbers. Multiple

devices with efficiencies over 11% have been fabricated on SSI absorbers that produce 14% devices with a CdS buffer layer.

SSI carried out UV exposure testing for devices with barrier coatings from PNNL that were previously exposed to high humidity accelerated testing.

About 60 Mo coated 10x10 cm glass substrates were sent to Seokhyun Yoon, a graduate student working with Tim Anderson at the University of Florida, for CIS studies in conjunction with TFPPP team activities.

About 40 $Cu(In,Ga)(S,Se)_2$ absorber layers on 10x10 cm glass substrates were sent to Tim Anderson at the University of Florida, for laser processing experiments in conjunction with TFPPP team activities.

SSI supplied Mo coated 10x10 cm glass substrates to Angus Rockett, University of Illinois, for CIS studies in conjunction with TFPPP team activities.

SSI deposited CVD ZnO on multiple sets of samples experimental absorbers for Unisun.

SSI patterned Mo coated glass was supplied to Unisun.

SSI provided materials for NREL "baselining" activities associated with developing tools or accelerated tests that predict long term performance.

Mini-modules gridded and measured at PNNL and the associated data were sent to Kannan Ramanathan, NREL, to explore the possibility of doing similar gridding on sections of monolithically integrated modules at NREL. These minimodules where then passed on to David Albin, NREL, as the beginning of "baselining" activities at NREL for environmental studies.

Package Development

Experience indicates that intrinsic stability and long-term outdoor durability of CIS modules can be assured through packaging development. Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over sixteen years. However, field failures have also been observed. Losses are not inherent to CIS since multiple past and present module deployments, typically in 1 kW arrays, have demonstrated long-term stability. If losses are observed, the losses are best correlated with the date of deployment or a prototype module configuration. Also, when losses have been observed, a range of module performance has been observed including no losses. Some failure mechanisms related to particular package designs and errors during production have been clearly identified. Other observations imply that additional circuit plate or packaging process variables have affected durability during particular production timeframes. Overall, results have demonstrated the proof of concept for stability and long-term outdoor durability. This section discusses the results of long-term outdoor testing and process development for lower cost reliable packaging.

Outdoor testing

FM and UL approval has been obtained for the present package used for the ST series of products and a 10-year warrantee backs product performance. Present and potential packages are subjected to both accelerated testing and long-term outdoor testing to develop and improve low cost yet durable packages. One way that NREL supports SSI package development is through long term testing of arrays and individual modules at the NREL Outdoor Test Facility (OTF). As depicted in Figure 42, long-term outdoor stability has been demonstrated at NREL where
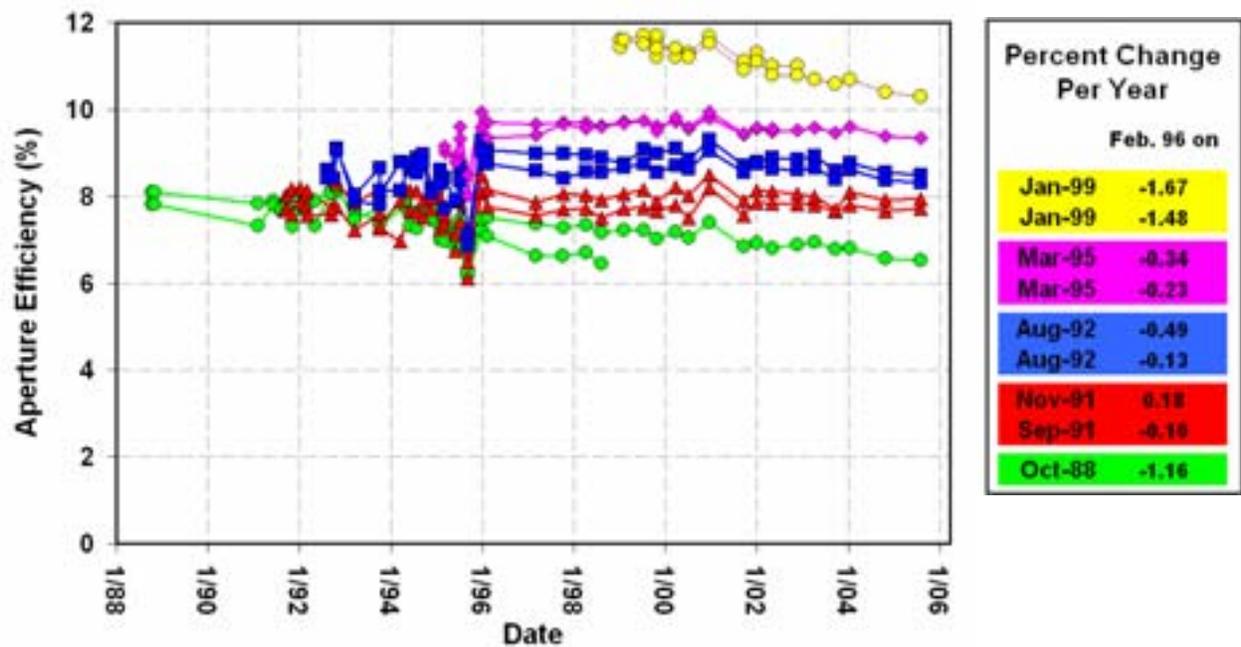
Figure 42. Demonstrated long-term outdoor stability.

~30x30 cm and ~30x120 cm modules with multiple prototype package designs have undergone testing for over sixteen years.

Transient effects typically make pulsed simulator measurements problematic. On the other hand, early outdoor data was noisy whereas data taken on a pulsed simulator was not. Only outdoor data from February 1996 on was considered when calculating changes with time. This approach was checked using pulsed simulator data with and without truncating the data before February 1996. There was no significant difference in the pulsed simulator data with and without truncating the data but the pulsed simulator data erroneously indicates a higher rate of change than the outdoor data. All absorbers with deployment dates of March 95 and later contained sulfur. As indicated by the outdoor data, modules with and without sulfur have demonstrated long-term outdoor stability with losses of less than 0.5% per year. Higher losses (1.2% to 1.7% per year) are observed for some groups of modules with and without sulfur. Changes in FF are similar in magnitude to the change in power, there is a small change in Voc and minimal change in Isc.

SSI installed and dedicated a 245 kW CIS thin film array on the roof of one of its manufacturing building (Figure 43). The system covers more than 31,000 square feet and contains 6144

modules. Installed with support from California Energy Commission (CEC) rebates, SSI receives economic benefits from the power produced by the installation. Environmental and economic benefits of PV are showcased by this array and it is an example of the use of CIS for SSI customers.

Figure 43. SSI's new 245 kW CIS thin film array.

An innovative systems design approach for the CIS array was employed to evaluate a new modular array support structure for flat commercial roofs and to evaluate optimization of array output based on utility rate schedules. The support structure is a modular design for simplified installation and utilizes inexpensive light gauge cold-formed steel c-channels. Roof penetrations are minimized even with an open-rack design that allows for cooling. The robust structure is capable of withstanding 80 mph winds and meeting zone 4 earthquake resistance requirements. System design is optimized by comparing tilt and azimuth dependent hourly and seasonal array output with local utility rate schedules.

SSI has supplied modules to the NREL OTF for three 1kW arrays. In each case, a newer generation of modules has been used to replace older designs using the same test site. The first two arrays demonstrated stability and that thermally induced transients, which are observed after exposure to high temperatures during accelerated environmental testing, are not observed in the field despite daily and seasonal changes in module temperature. This is entirely reasonable since

known transient effects are temperature dependent and the module temperatures reached for actual deployment are less than the temperatures defined for accelerated testing.

Data acquisition began on November 18, 1998 for the third 1kW array of prototype modules. The system is comprised of 28 modules with an average efficiency of 11.4% at STC. The aperture area of each module is $0.3651m^2$ and of the total array is 10.2 m^2. The array is fixed at a 40° tilt aligned true south and is connected to a resistive load through three maximum power trackers. Continually logged data is corrected for temperature. Only data for incident solar irradiance of between 950 and 1050 W/m^2 is used for array characterization. NREL measurements indicated array performance over 1kW. NREL data from late February of 2000 indicated stability within 2% of the measurements made shortly after array deployment.

Later array data indicated that the third began exhibiting power losses. To follow-up on this observation, NREL made outdoor measurements (Daystar) on each module in the array. Six modules were selected for further study as representative of the varying of degrees power loss for all array modules. NREL provided pulsed simulator (SPIRE), continuous illumination simulator (LACSS), and outdoor measurement (SOMS) data for the six selected modules. This data indicated that changes in performance are primarily changes in FF (Figure 44). As is typical of CIS transient effects, observed changes are smaller for measurements made with continuous illumination than for pulsed simulation. For this sample of six representative modules, the change in FF is highly variable ranging from 4% to 18% (LACSS). The changes in FF were denominated by series resistance or "rollover" of the IV curve which is observed for recoverable transient effects and may be accentuated for low level water vapor ingress [19, 25, 26, 27]. The low end of this range is virtually no loss, i.e. within measurement variability. Later NREL measurements indicated basically the same behavior; a range of module performance from virtually no loss to significant losses.
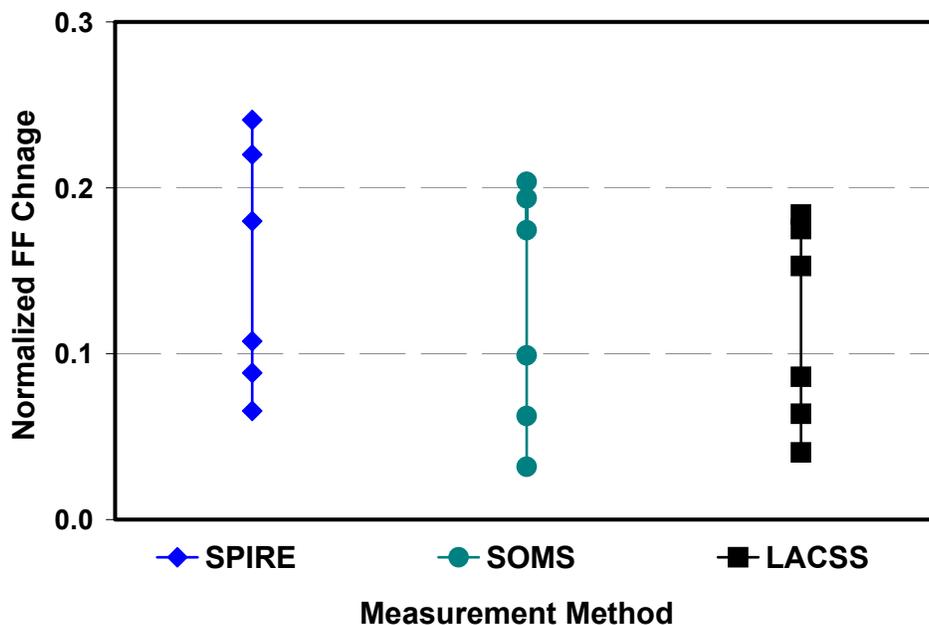

Figure 44. Normalized changes in FF, ranging from virtually no loss to significant losses, for six representative array modules.

Packaging development from early work with mini-modules through ST products has demonstrated that thermally induced losses from lamination or accelerated testing will recover with extended outdoor exposure [3]. SSI has also demonstrated multiple packaging designs, with and without EVA, that protect circuit plates from water vapor ingress during damp heat accelerated testing; exposure for 1000 hour at 85ºC and 85% relative humidity [2, 3]. CIS circuit plates in packages that provide protection from water vapor ingress will pass accelerated environmental tests with an outdoor exposure to reverse thermally induced transient effects. This conclusion was supported by studies by the NREL TFPPP "Transient Effects Group." The team defined a repeatable measurement methodology for systematic study of thermal transient effects that was used to demonstrate reversibility through multiple thermal cycles and thereby support outdoor testing results that indicate long term stability for normal operating conditions [3, 28].

Based on this foundation, SSI testing indicates that no significant humidity ingress occurs during damp heat testing of current SSI products with a TPAT backsheet. Figure 15 is a chart of average efficiency for two groups of 8 modules. One group went through the damp heat
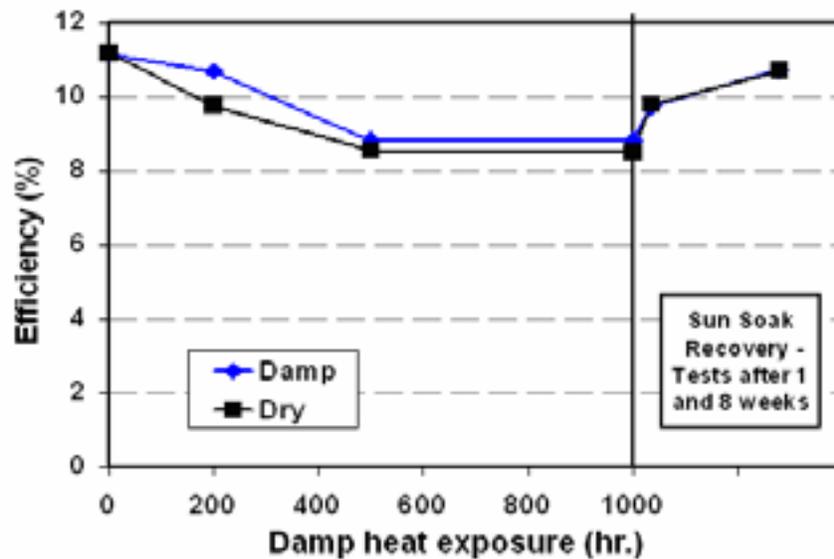
Figure 45. Recovery after the thermal exposure of damp heat accelerated tests with or without including high humidity in the tests.

environmental test and the other went through the same temperature exposure cycle but without humidity [17]. Both groups were then placed outdoors for 8 weeks of recovery. The two groups show the same thermally induced loss and recovery with light exposure; humidity had no impact on the results for current SSI products.

Substantial subcontract work explored differences between data from the most recent array of prototype modules deployed at NREL, the most recent accelerated testing demonstrating stability for production modules, and the combined knowledge from multiple sets of accelerated test results, multiple generations of modules deployed at NREL and the two previous arrays deployed at NREL that were stable. SSI has deployed modules, typically in 1 kW arrays, at test sites

throughout the country and, to a lesser degree, throughout the world. Modules from multiple sites were retrieved for nondestructive and destructive testing to explore the observations of the most recent NREL array.

Early prototype module designs included a wide frame that extended across the front of the modules to cover buss bars for better aesthetics. CIS modules have an esthetically pleasing uniform nearly black appearance. However, the simplest form of bus bar is a shinny tin-coated copper ribbon. Wide frames were used in pre-production modules to cover the shinny bus bars and solder. The inside edges of these wide frames were very close to the outer cells which are narrow strips extending the length of the module; parallel with and close to the wide frame. This geometry proved to be very sensitive to dirt buildup, Figure 46, in a narrow strip at the edge of frame that shadowed the outer cells. Improved performance was demonstrated after scraping away the dirt. However, not all of the subset of modules that showed degradation fully recovered after scraping away the dirt. Dirt clearly can degrade performance but this mechanism explains only some of the degradation for some of the modules. It is assumed that the wide frames also tended to trap water, which also could have lead to degradation.
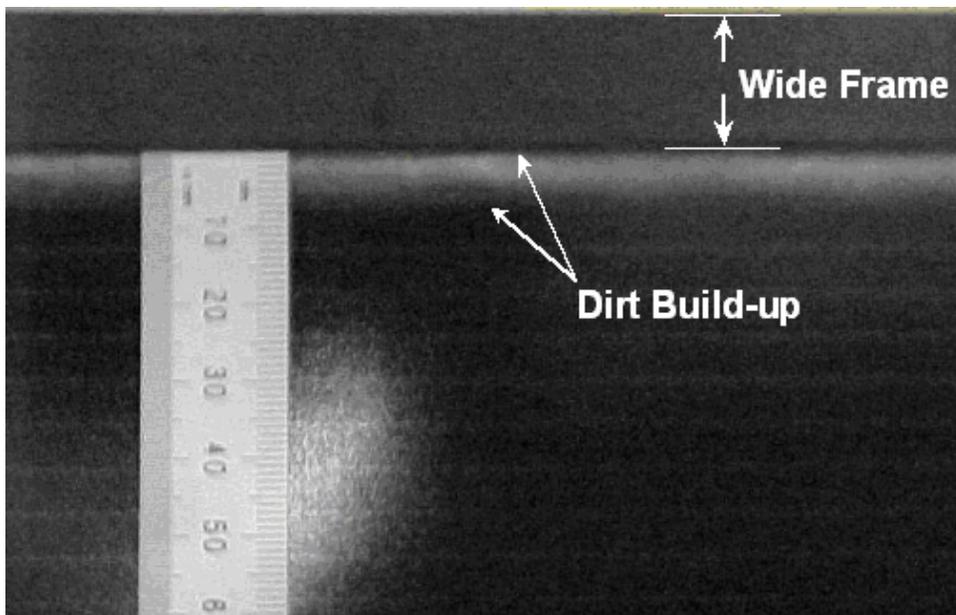
Figure 46. Dirt buildup in a narrow strip at the edge of a wide frame.

Additional testing demonstrated that errors during fabrication caused degradation for some modules and this also accounts for some of the observed OTF array results. In another generation of prototype modules, a uniform dark appearance for the front of modules was achieved with narrow frames, rather than wide frames, by covering the shinny bus bars with black decorative tape prior to encapsulation. For wide or narrow frames, additional tape is used during lay-up for encapsulation to preposition and hold the circuit plate, EVA, glass cover sheet

and TPAT backsheet. The proper approach in preparation for lamination is to tape together the external components, i.e. backsheet to the cover glass, thereby holding all internal and external components together and allowing the tape to be removed after lamination.

Destructive testing found that this tape was at times improperly used to hold internal components i.e. internal components were taped to the circuit plate or cover glass before laying up the complete package (Figure 47). Therefore, the improperly used tape for lay-up provided a path for water vapor penetration past the hermetic seal formed by the combination of the TPAT backsheet and an offset between the circuit plate and the frame (see Figure 5 or Figure 6). The combination of improperly used tape during laminate lay-up and dirt buildup on obsolete wide frames could explain performance variation for at least some wide or narrow frame prototype modules from virtually no loss to significant losses.

One of the modules from the third array at NREL that showed a degraded FF was dissected with help from Tom McMahon, NREL, expecting that lay-up tape would be found. The frames were
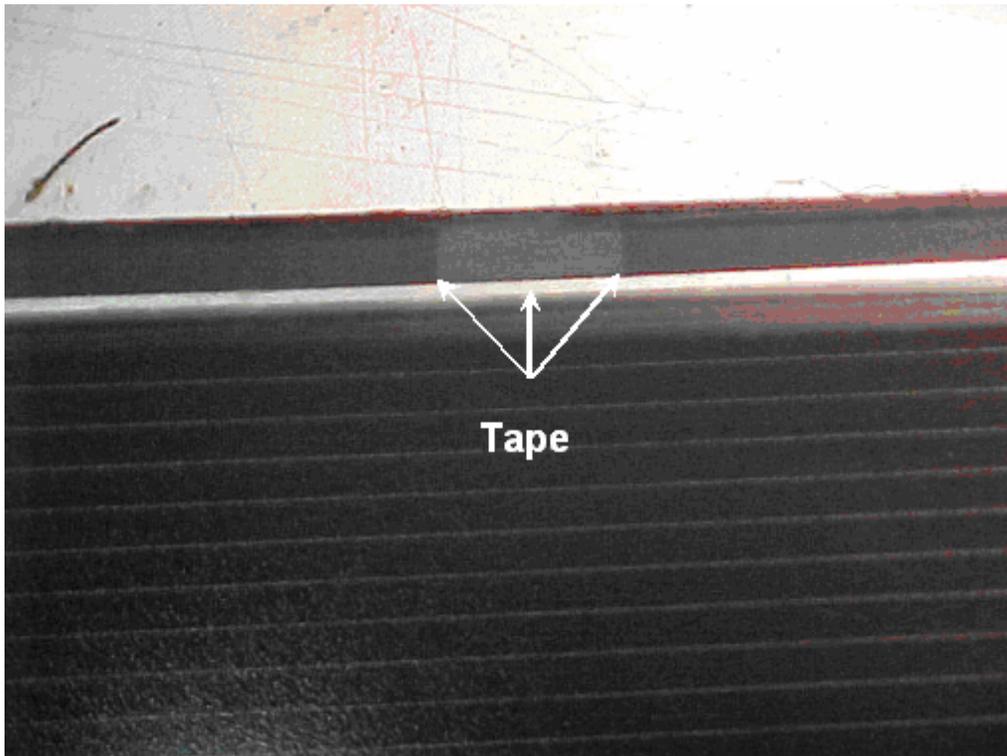

Figure 47. Improperly used tape inside the package.

removed and the edge of the laminate was inspected. Although indentations in the backsheet due to proper use of lay-up tape were found, inspection of the edge gave no indication of improperly used lay-up tape for this particular module.

Adhesion between the backsheet and the circuit plate for this module was tested by cutting into the EVA parallel to the plane of the circuit plate to release a section of the backsheet and then peeling back the backsheet. Lower adhesion of the TPAT along one of the long edges of the circuit plate was observed along with the odor of EVA. These subjective observations may indicate incomplete curing of the EVA leading to lower interface adhesion and thereby higher moisture ingress. Also, glass to EVA adhesion is know to be dependent on EVA curing. In addition to EVA curing, EVA quality, priming, glass surface quality or other lamination and packaging issues could have lead to the lower adhesion of the TPAT along one edge and the odor of EVA. In addition, the ability of the frames to help maintain a physical bond through compression, directly inhibit water vapor penetration or avoid trapping water may depend on these packaging details and the indentations in the backsheet from "proper" use of lay-up tape. Therefore, frame design, proper use of lay up tape, EVE curing and other details of the lamination and framing processes, may have contributed to failure for some modules.

Laser scanning results published by NREL (Figure 48), indicate degradation due to shunting primarily at the edge of modules, which is consistent with an interpretation that packaging issues lead to the degradation [29]. Reverse bias hot spot measurements, made at NREL using a technique based on observing discoloration of heat sensitive sheets, indicated hot spots throughout some degraded modules. NREL IR imaging also indicate shunting at some interconnects [30]. As discussed above, shunting along laser P1 scribes sporadically caused poor performance prior to improvements made during this subcontract. This is a concern and could account for shunting. However, a correlation between the qualitative hot spot data and the modules that degraded could not be established since similar data before degradation was not available, the link between the observed changes in forward bias FF and reverse bias hot spots is tenuous, and a comparison could not be made between hot spots and modules with and without degradation. These hot spot measurements do not seem to clearly contradict the laser scan results indicating problems at the edges and implying a packaging issue for at least some modules; the changes in FF denominated by series resistance or "rollover" of the IV curve implies issues with the diode possibly due to low level water ingress. This may be in parallel with an increase in sheet resistance due to low level water vapor ingress [1].
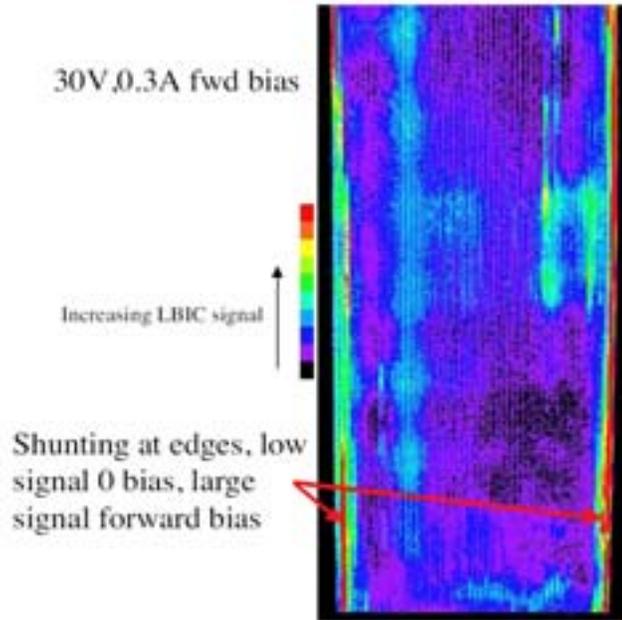
Figure 48. A laser scan of a thin-film module showing shunting at the edges (Figure 8. from reference 29).

High level water vapor ingress is not indicated since, as discussed in the following section on development of the ST80 package, a change in current associated with darkening and broadening of the interconnects can be an indicator of high level water vapor ingress. No darkening and broadening of the interconnects was observed for the dissected array module. Smaller (ST10) modules were retrieved from deployment to explore this issue using destructive and nondestructive testing. Barely detectable corrosion along the edge of cells was observed but not the darkening and broadening observed for the prototype glass/glass package. Also, the electrical performance change with darkening and broadening of interconnects includes a drop in current that is not significant for modules from the third array. Therefore, high level water vapor ingress does not seem to be the cause of degradation for any of the prototype modules deployed at the OTF. This does not contradict the possibility that a lower degree of water vapor ingress could be responsible for the decreases in FF.

Array data from test sites throughout the country is consistent with and augments the information obtained from individual modules and the NREL array. Figure 19 is a chart of average annual decline in power for 32 module arrays deployed at:

      "FSEC" `   - Florida Solar Energy Center, Cocoa, FL

      "Wisconsin" - University of Wisconsin, Madison, Wisconsin

      "Gumbo"   - Gumbo Limbo Environmental Education Center & Florida Atlantic
                    University, Boca Raton, Florida

"NREL"   - National Renewable Energy Laboratory, Golden, Colorado

"Austin"   - University of Texas at Austin, Austin, Texas

"SWTDI"   - Southwest Technology Development Institute, Las Cruces, New Mexico

These test site locations represent diverse climates and, as indicated in the figure, two main module configurations, wide and narrow frames, are included in the data. The two module configurations are equally well described as two production timeframes. The average annual decline ranges from slightly negative, an improvement, through minimal changes to significant losses. If there is a climatic component of the changes, it is obscured by other variation. However, a hot humid environment, which would be expected to be the harshest, is not necessary for changes and, in fact, the array showing a small improvement is from an area (Austin) selected for array deployment because of the hot and humid environment.
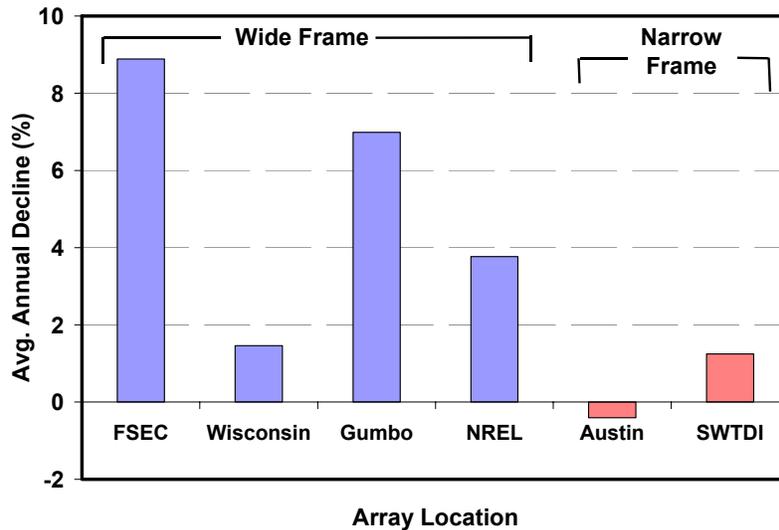
Figure 49. 32 Module Arrays: Average Annual Decline.

The presence of any significant loss is best correlated with module configuration or timeframe [17]. This correlation is also consistent with long-term outdoor stability testing for individual modules, Figure 42, where multiple prototype package designs have demonstrated long-term stability. An exceptions is the two modules deployed in 1998, which is the same timeframe as the arrays that exhibit losses. A range of array performance from improvement through losses is observed for the timeframe where arrays might show significant losses and within the arrays that show losses there is a range of module performance including no loss. Some failure mechanisms, such as improper use of lay-up tape and dirt buildup for wide frames, have been clearly demonstrated. Other subjective observations imply that additional circuit plate or packaging process variables, such as the degree of EVA cure, effected long-term stability for pre-production modules produced in the timeframe when wide frames were standard.

As Phase I deliverables, SSI shipped 60 modules to NREL for use by the TFPPP "Outdoor Testing and Monitoring of Thin Film Modules in Hot and Humid Climates" program. After characterization at NREL, these modules were deployed at the Florida Solar Energy Center. An additional set of 60 modules, as Phase II deliverables, were sent to NREL for this program and deployed at Texas A&M.

Glass/Glass Package Development

SSI is developing "glass/glass" package designs primarily to decrease packaging costs. Simplification of the package and decreased operating temperature are additional potential advantages. Figure 6, in the overview for the technical review, is a sketch comparing the ST40 production package and a glass/glass package.

Glass/glass package development began using single 40W circuit plates and was extended to a new higher power, ST80, product. Figure 50 is a sketch of a proposed ST80 glass/glass package, which was designed for cost reduction and marketability. Two nominally 40W circuit plates are laminated to a common tempered glass front sheet. Laser edge deletion to remove all of the thin films forms an approximately 1 cm boarder and provides electrical isolation from the frame. An edge seal selected in collaboration with the NREL sponsored National Thin-Film PV Module Reliability Team (TFMRT) is used at the perimeter of both plates [31]. A screen in front of the ribbons is included to achieve an aesthetically pleasing uniform black appearance.
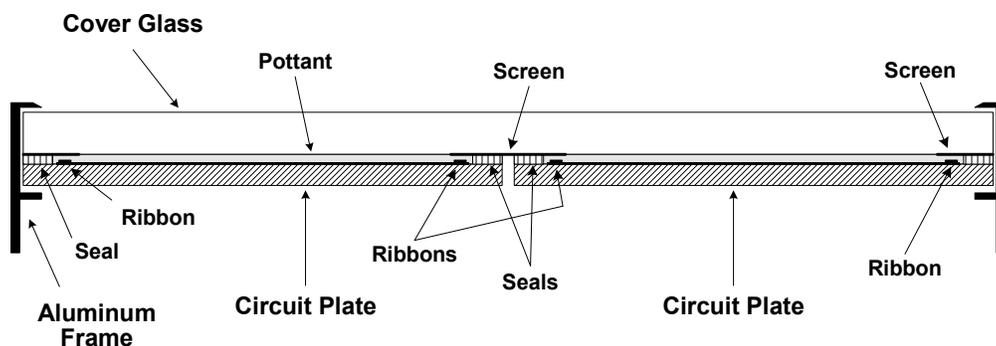
Figure 50. Proposed ST80 glass/glass package.

Glass/glass package development before adopting an edge seal indicated the need for additional moisture protection. Figure 51 is a photo of the edge of a glass/glass module where the interconnect patterning for monolithic integration is visible as vertical lines above the ruler. Darkening and broadening of the interconnects at the edge of the circuit plate was observed for glass/glass packages after damp heat testing. In addition to decreases in FF, decreases in Isc were responsible for some of the power losses. The darkening and broadening was not observed for the glass/glass package after the same thermal exposure but without high humidity or for production products, that employ a TPAT backsheet and frame, after the same thermal exposure with or without high humidity. Therefore the current dominated power loss and darkening and broadening of the interconnects was associated with severe moisture ingress [19].

Figure 51. Darkening and broadening of the interconnects due to moisture ingress.
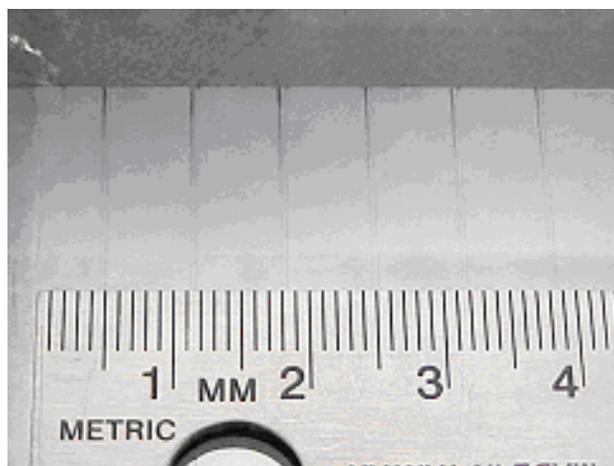
Various package design options were explored including variation in edge seal type, edge seal width, EVA thickness, lamination temperature, EVA gel content, alternative junction boxes, lead routing and even PVB as an alternative to EVA as a pottant. An edge seal was selected in collaboration with the TFMRT and was tested by UL for approval as a new material for use in PV modules. Prototype 40W packages incorporating this edge seal passed accelerated tests, including the damp heat test. In addition to a barrier to humidity ingress, this edge seal solved problems during lamination; breakage of the circuit plate due to compression of the laminate edges was eliminated. This allowed simplification of the process by eliminating the need for fixturing during lamination and allowed the use of thinner EVA thereby reducing materials cost.

Testing of new package designs included exploring the importance of the frame. No detectable humidity ingress occurs during damp heat testing of framed ST40 products using the design with a TPAT backsheet. However, unframed ST40 laminates did not perform as well. In addition to a moisture barrier, the frame may keep the laminate and interfaces under compression. This is not the case for the glass/glass package; there is no statistically significant difference between framed or unframed laminates exposed to high heat and high humidity or unframed laminates exposed to high heat. A frame is not required to avoid moisture ingress for the glass/glass package with this edge seal.

Accelerated testing beyond the normal damp heat test, 1000 hours of exposure to 85ºC and 85% relative humidity, was pursued to identify potential weaknesses in the glass/glass package design, particularly the impact of humidity (Figure 52). Control modules were exposed for the same duration at 85ºC but without high humidity thereby allowing distinction between humidity induced effects and solely transient thermal effects. All measurements for control and test modules were made after a two hour outdoor exposure.
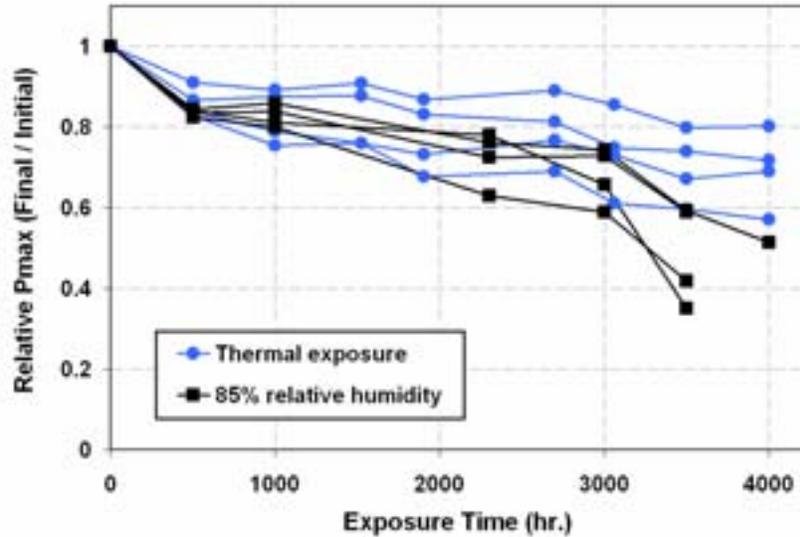
49

Figure 52. Protection from humidity ingress well beyond the standard 1000 hours.

There was no significant difference in electrical performance between controls and glass/glass modules exposed to high humidity and no visible corrosion after 1000 hours of exposure. Corrosion was not observed for 2300 hours of exposure to high humidity. However, the electrical performance seems to be slightly lower than for the controls. This observation is supported by trends in the electrical performance data but not proven since the number of modules tested is inadequate to claim statistical significance at a 95% confidence level. Corrosion was visible on most modules only after 3000 hours of damp heat exposure. Lower electrical performance with no visible corrosion was observed for one module. Corrosion of the interconnects was observed along the short edge of the 1x4 ft. module up to 3 cm in from the edge (Figure 53, short edge to the right). Corrosion along the long edge of a module may be as far inboard as the first interconnect and varied from unobservable through sporadic to continuous.

One module failed catastrophically after 3500 hours due to failure of solder connections to a printed circuit board that extends the circuit plate buss ribbons and routes power to the back of the module. The majority of modules failed after 4000 hours due to this failure mechanism and breakage. These results indicate that the glass/glass package design with an edge seal provides protection from humidity ingress well beyond the standard 1000 hours at 85°C and 85% relative humidity.
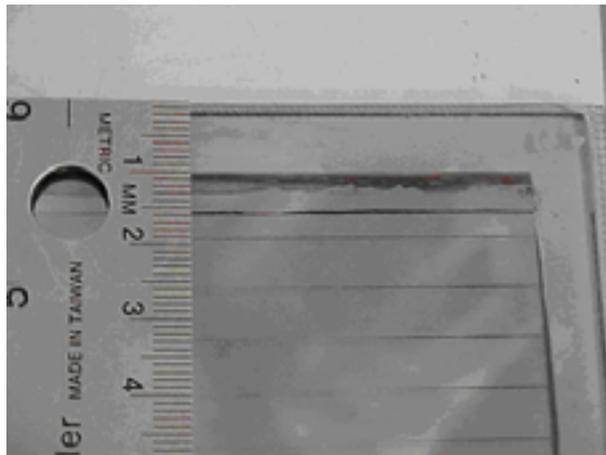
50

Figure 53. Corrosion at the corner of a glass/glass laminate after 3000 hours of damp heat exposure.

Additional testing of the edge seal as required to use a new material in a product was successful. A test plan was developed with UL and testing to qualify the edge seal was completed. The test results classify the edge seal as a "Material Group 1" insulating material in accordance with IEC standard 60664-1 and 60112, which is the top insulating group. Testing primarily with the edge seal as a component rather than in a laminate included:

- Dielectric breakdown strength before and after environmental conditioning

- High voltage arc track rate

- High voltage arc track rate in the presence of aqueous contaminates

- Volume resistance

- Damp heat exposure

- Dielectric breakdown strength for a laminate

- Damp heat exposure for a laminate

Elimination of the TPAT backsheet for the glass/glass package was planned in combination with polishing off contaminates on the back of the circuit plate. However, a back cleaning system purchased for this task proved inadequate for the ST80 where two circuit plates are laminated to one cover glass and the backs of the circuit plates may not be parallel. The approach may also be inadequate for single circuit plates. An alternative plan using lower cost Tedlar backsheet and a lower cost adhesive was implemented (Figure 54). Long-term options include sealing the back of the circuit plate with a low cost coating that is applied during or after lamination or eliminating the CdS.

Figure 54. ST80 glass/glass package.
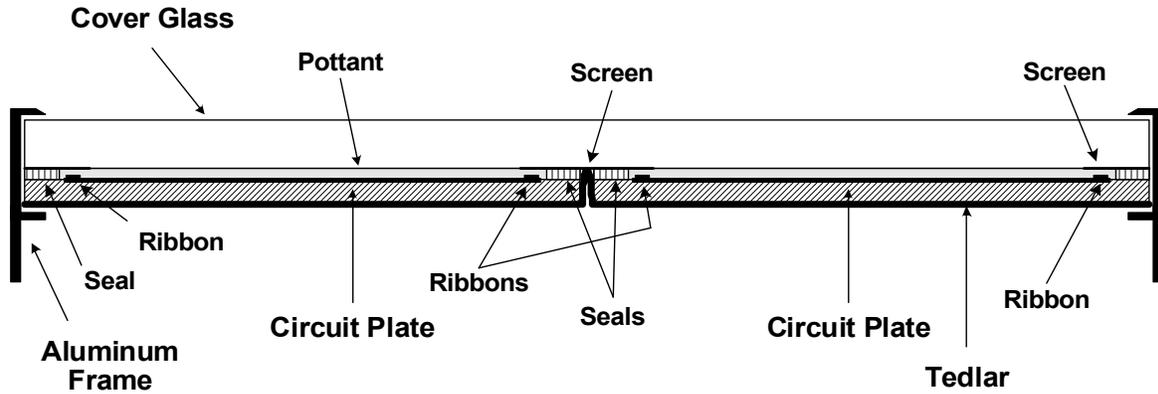
Figure 55 illustrates the layout of the circuit plates, buss bar ribbons and a printed circuit board (PCB) that connects the circuit plates and routes power to a junction box on the back of the module. A black screen printed aperture on the cover glass covers the ribbons, Figure 56, to achieve an aesthetically pleasing uniform black appearance.
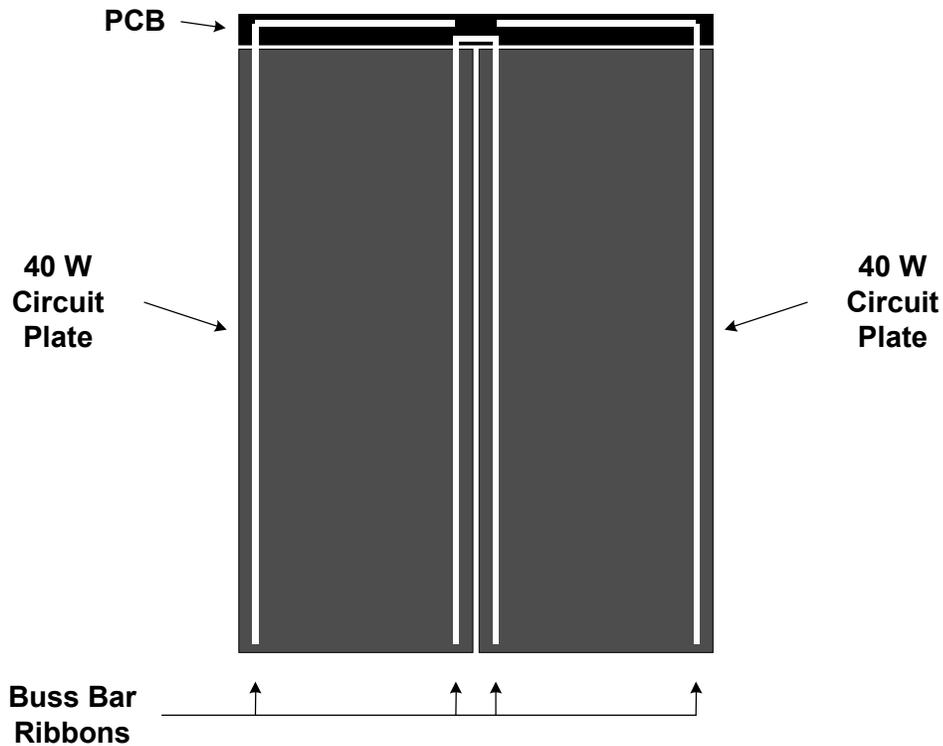

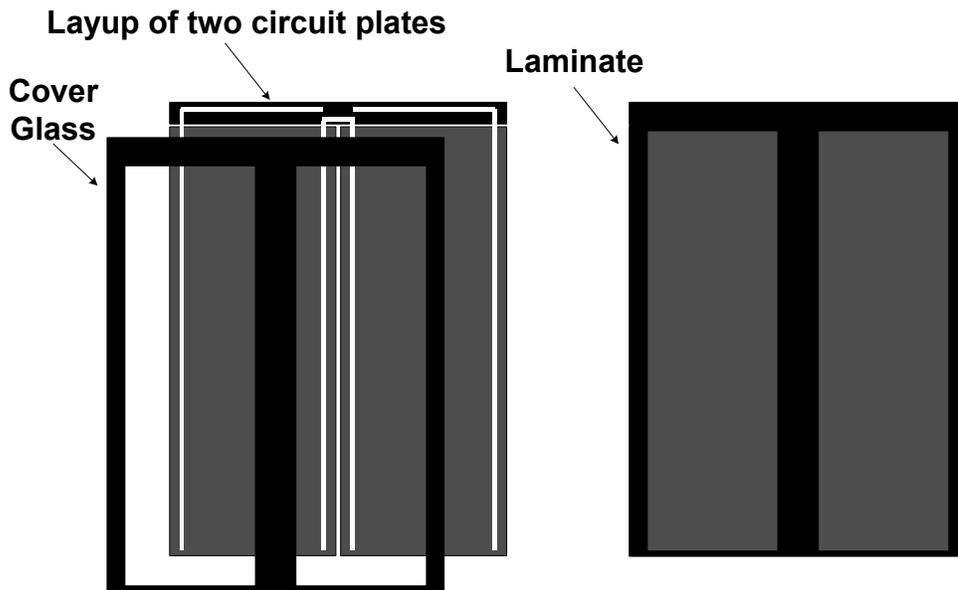**Figure 55. Lay-up of two circuit plates.**

Figure 56. A cover glass with screen achieves an uniform black appearance.

Package process development for minimodules led to the discovery of a corrosion mechanism in minimodules that may also be a consideration for some low cost and very long lifetime power module package options. Corrosion of the Mo in the area of ZnO patterning is observed because minimodule package approaches did not protect the circuit from water vapor ingress as well as the package designs for power modules. This corrosion is observed if both the ZnO and CIS are removed, as is done during mechanical patterning. However, corrosion does not occur if only the ZnO is disrupted and the CIS remains largely intact.

As Phase 3 deliverables, SSI shipped 18 ST80 prototype modules to NREL for deployment as a 1 kW array and other testing at the OTF.

Alternative patterning strategies that were previously developed to avoid near-interconnect adhesion problems are applicable to the minimodule corrosion issue [1]. These patterning approaches were not previously adopted since preferable changes in other absorber formation processes solved the near-interconnect adhesion problems. Some of the alternative patterning approaches included deposition of an insulator over part of the interconnect and subsequent deposition of ZnO over the insulator. A class of materials tested as potential insulators was found to suppress ZnO growth. This lead to new patterning approaches based on growth suppression rather than patterning the ZnO. One of these approaches was effective in addressing the current minimodule corrosion issue since the CIS remains intact (Figure 57). In addition, this type of approach may be valuable for alternative large area package designs if a similar corrosion mechanism occurs that is not seen for present designs.
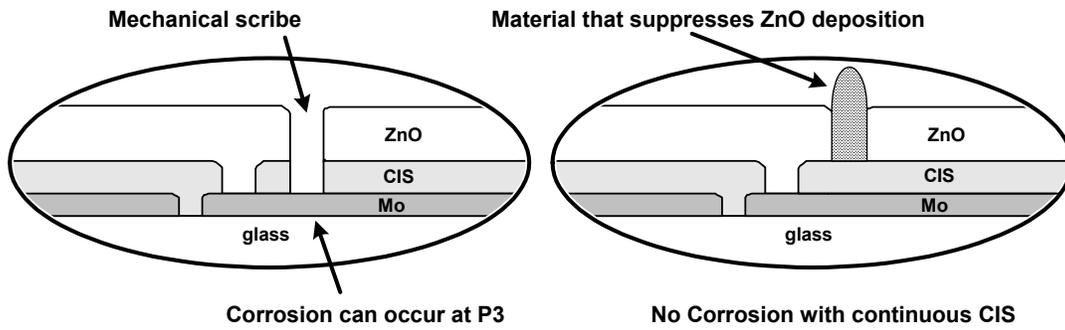
Figure 57. Corrosion avoided when P3 is formed by suppression of ZnO growth rather than mechanically.

Conclusions

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. The following are highlights of accomplishments during this subcontract:

- Executing the CIS process continues to demonstrate process predictability.

- A new minimodule product that would potentially expand near-term and long-term capacity scale-up options was explored but abandoned.

- Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. SSI 2003 capacity was about 3 MW per year whereas production for 2003 was just over 1.2 MW per year. Introducing the new minimodule product accounts for the main difference between production and capacity.

- Average laminate efficiency for 2003 was 11.0% with a full width of only 11% of the average; nominally the same as for 2002 but with a 33% increase in production volume.

- Line yield increased from about 60% in 2000 to about 85% in 2002. This high line yield was maintained through 2003 and redemonstrated after abandoning minimodule production.

- Process development primarily during the third subcontract phase emphasized demonstration and implementation of a new "sputter dose" process where a compound containing sodium is sputtered on the Mo base electrodes prior to deposition of nominally standard precursors. Although exploration of the full potential of the sputter dose process has just begun, decreased variation in absorber structures and decreased transient have been demonstrated.

- Process R&D during this subcontract, both at SSI and in collaboration with NREL teams, has demonstrated the potential for further cost performance improvements: minimization of transients, improved processes, increased efficiency and improved packaging.

- Long-term outdoor stability has been demonstrated at NREL where multiple prototype package designs have undergone testing for over sixteen years.

- Field failure mechanisms related to particular package designs and errors during production have been clearly identified. Additional circuit plate or packaging process variables may have affected durability during particular production timeframes; when losses have been observed, the losses correlated with date of deployment or prototype module configuration.

- Prototype glass/glass packages have passed accelerated tests, including the damp heat test. This package incorporates an edge seal selected in collaboration with the National Thin-Film PV Module Reliability Team.

- Developing and testing of 40W glass/glass packages was extended to a new 80W product made using two nominally 40W circuit plates laminated to a common front sheet. Product release is imminent.

Further device and production R&D can lead to higher efficiencies, lower cost, and longer product lifetime. Production volume, efficiency and yield data supports attractive cost projections for CIS. Prerequisites for commitment to large-scale commercialization have been demonstrated at successive levels of CIS production. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

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30. IR imaging courtesy of Thom McMahon, NREL

31. Solar Edge Tape, True Seal

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14. ABSTRACT *(Maximum 200 Words)*
The primary objectives of this Shell Solar Industries subcontract are to address key near-term technical R&D issues for continued CIS product improvement; continue process development for increased production capacity; develop processes capable of significantly contributing to DOE 2020 PV shipment goals; advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability; and perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that will last up to 30 years while retaining 80% of initial power. These production R&D results, production volume, efficiency, high line yield, and advances in understanding are major accomplishments. The demonstrated and maintained high production yield is a major accomplishment supporting attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. Process and packaging R&D during this and previous subcontracts has demonstrated the potential for further cost and performance improvements.

15. SUBJECT TERMS
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