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Innovation for Our Energy Future

Reliable, Low-Cost Distributed Generator/Utility System Interconnect

Final Subcontract Report
November 2001 — March 2004

Z. Ye, R. Walling, N. Miller, P. Du, K. Nelson,
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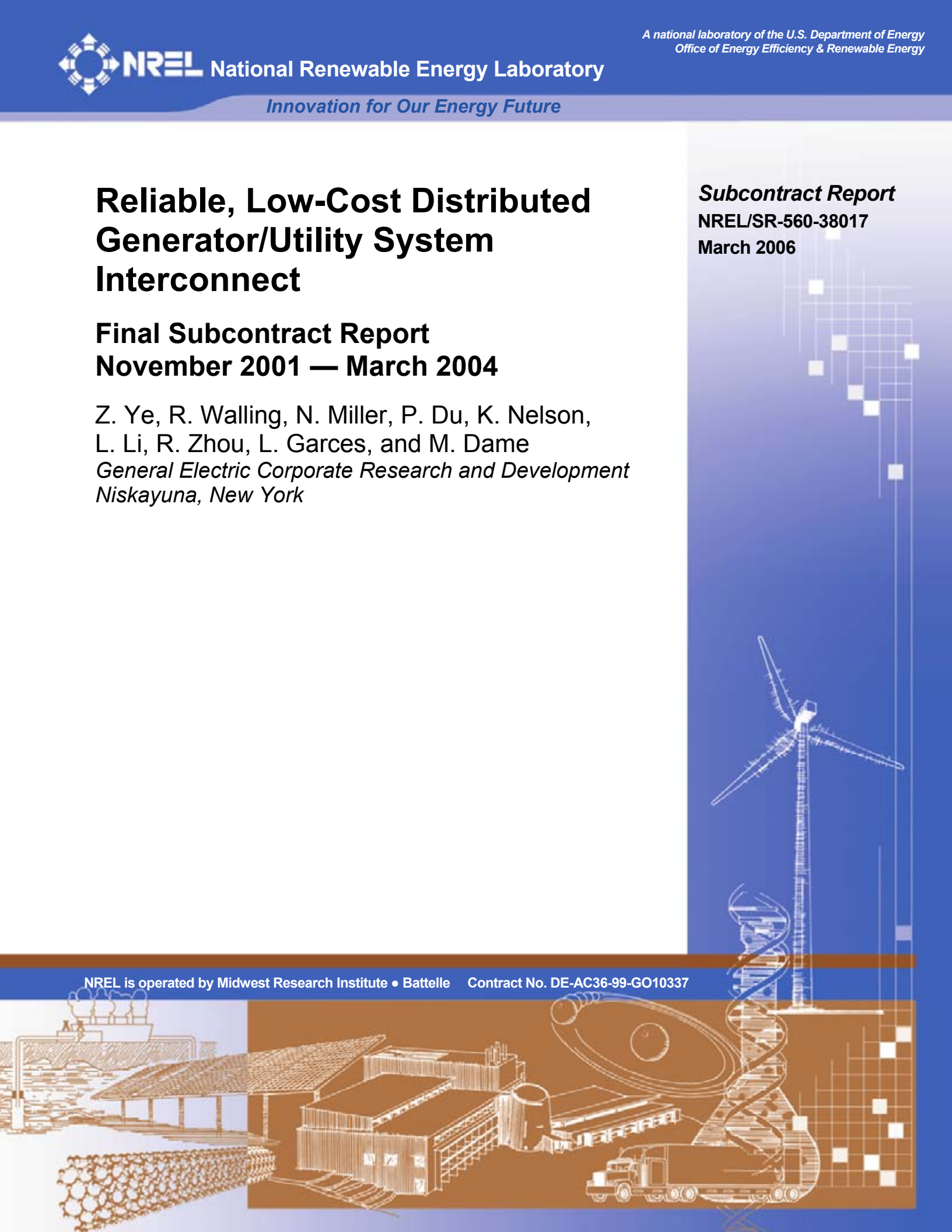
General Electric Corporate Research and Development
Niskayuna, New York

Subcontract Report
NREL/SR-560-38017
March 2006



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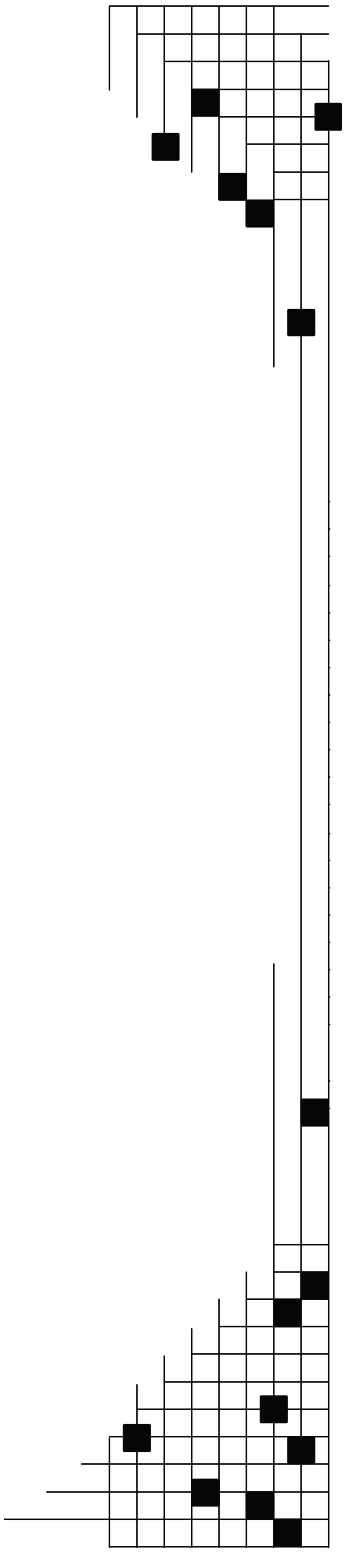

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List of Acronyms

AI	anti-islanding
AVR	automatic voltage regulator
BPF	ban-pass filter
DG	distributed generation
GM	gain margin
EUT	equipment under test
IGBT	Insulated Gate Bipolar Transistor
LVRT	low-voltage-ride-through
NDZ	non-detection zone
NREL	National Renewable Energy Laboratory
PCC	point of common coupling
PI	proportional-integral
PLL	phase-lock loop
PM	phase margin
THD	Total Harmonic Distortion
SFS	Sandia Frequency Scheme
UPS	uninterruptible power supply device

Executive Summary

Standards compliance is key for entry into the distributed generation market. Of the technical requirements laid out in various standards, including IEEE 1547, some (for example, voltage regulation, integration with area EPS grounding, etc.) must be coordinated by the utility system designer/operator. Some can be designed at the interconnect interface, e.g., harmonics, DC current injection, anti-islanding, etc. Most aspects have been addressed before and certain requirements have previously been established by other standards and recommended practices, e.g., IEEE 519, etc. However, some requirements, such as anti-islanding, are relatively new and there are no well-established practices and solutions.

Unintentional islanding of distributed generation (DG) may result in power quality issues, interference to grid protection devices, equipment damage, and even personnel safety hazards. A comprehensive survey of anti-islanding schemes indicated that the existing solutions are either too expensive (e.g., transfer trip), not secure enough (non-detection zone exists), or cause power quality degradation (i.e., waveform distortion).

This report summarizes the detailed study and development of new GE anti-islanding controls for two classes of DGs. One is inverter-interfaced, while the other is synchronous machine-interfaced. These two types of interfaces cover most types of distributed generation, including photovoltaics, fuel cells, variable speed engines (microturbines, sterling engines), small wind turbines with direction conversion, batteries, engine generators (diesel, natural gas, biomass, hydrogen) and small gas turbines.

The accomplishments of the work include:

1. The proposal of a family of new anti-islanding schemes that feature no non-detection zone (NDZ), have minimum power quality impact, low cost implementation (software code only), and robust to grid disturbances
2. Design guidelines for the proposed schemes
3. Evaluation and validation of the proposed schemes under practical application conditions
4. A demonstration that the schemes work for multiple inverters, multiple machines, and mixed inverter and machine based DGs. Additionally, the report shows that some schemes, though they work fine for a single DG, may be ineffective for multiple DGs
5. Experimentally tested and validated schemes.
6. The report also addresses microgrid application issues.

1 Introduction

1.1 Background

Traditionally, distribution power systems are configured in radial structures. Power and short circuit currents flow uni-directionally down from distribution substations. Most protection, monitoring, and control devices are designed based on this premise. Recently, distributed generation (DG) has emerged in the energy market because of their value stories, such as peak shaving, combined heat and power, renewable portfolios, transmission and distribution infrastructure deferral, and so on. These provide economical and environmental incentives to promote DG. However, there are barriers, both regulatory and technical, preventing the entrance of DG into the current energy market due to historical distribution infrastructure as well as energy market structure.

The industry is actively addressing the issues of interconnecting DG to the grid. The current GE project mainly addresses the technical issues of the DG interconnection, while keeping the regulatory issues in mind, i.e., that the technical solutions should alleviate the regulatory barriers.

The proposed GE solution for DG interconnection is to have a universal, modular, low cost interconnect, which can be pre-tested and pre-certified for standards compliance. This will not only improve the general acceptance, but also reduce the cost during the interconnection process, which is usually a tedious, costly, engineered process in current practices.

Standards compliance is important for the interconnection. There are many standards and codes imposed on DG. Those various standards make it difficult to accommodate all of them at once within one DG design. Recently, IEEE 1547 (“Standard for Interconnecting Distributed Resources to Electric Power Systems”) [1] defined a uniform set of requirements for any DG below 10MW. The Standard will drastically reduce many, though not all, barriers of DG applications.

Among the technical requirements in IEEE 1547, some have to be coordinated by the utility system designer/operator, for example, voltage regulation, integration with area EPS grounding, etc. Some can be designed at the interconnect interface, e.g., harmonics, DC current injection, anti-islanding, etc. Most aspects have been addressed before and certain requirements have previously been established by other standards and recommended practices, e.g. IEEE 519. However, some requirements are relatively new, such as the prevention of unintentional anti-islanding, etc. In order to examine the technical gap, an IEEE1547 compliance matrix was developed, as shown in Table 1-1. It can be seen that most functions are either available or can be dealt with using existing practices. There is one function standing out – anti-islanding protection. The function can prevent unintentional islanding and out-of-phase reclosing. Unintentional islanding of DG may result in power quality issues, interference to grid protection devices, equipment damage, and even personnel safety hazards.

Table 1-1 IEEE 1547 compliance matrix

	IEEE 1547 Technical Requirements	Interconnect Functions	Notes
4.1	***General Requirements***		
4.1.1	Voltage Regulation	Available	Interconnect device shall not actively regulate voltage
4.1.2	Integration with Area EPS Grounding	Available	protection for different transformer connections
4.1.3	Synchronization	Available	Existing functions
4.1.4	Distributed Resources on Distribution Secondary Grid and Spot Networks	N/A	This topic is under consideration for future revisions
4.1.5	Inadvertent Energization of the Area EPS	Available	existing function: dead circuit check
4.1.6	Monitoring Provisions	Available	Can be met by current practices
4.1.7	Isolation Device	Available	Can be met by current practices
4.1.8	Interconnect Integrity		
4.1.8.1	Protection from EMI	Available	Can be met by current practices
4.1.8.2	Surge Withstand Performance	Available	Can be met by current practices
4.1.8.3	Paralleling Device	Available	Can be met by current practices
4.2	***Response to Area EPS Abnormal conditions***		
4.2.1	Area EPS Faults	Available	Can be dealt with by current practices
4.2.2	Area EPS Reclosing Coordination	***Anti-Islanding protection***	For DR not closing to the reclsoing device, an anti-islanding function is needed, unless other expensive means is involved
4.2.3	Voltage	Available	Can be met by existing relay functions
4.2.4	Frequency	Available	Can be met by existing relay functions
4.2.5	Loss of Synchronism	Available	Can be met by existing relay functions
4.2.6	Reconnection to Area EPS	Available	Can be met by existing relay functions
4.3	***Power Quality***		
4.3.1	Limitation of DC injection	Available	Can be met by current practices
4.3.2	Limitation of Flicker Induced by the DR	Available	Can be met by current practices
4.3.3	Harmonics	Available	Can be met by current practices
4.4	***Islanding***		
4.4.1	Unintentional islanding	***Anti-Islanding protection***	detection within 2s.
4.4.2	Intentional islanding	N/A	This topic is under consideration for future revisions

There has been an argument that the probability of islanding is extremely low, so that it may be a non-issue in practice. However, there are three counter-arguments: First, the low probability of islanding is based on the assumption of 100% power matching between the DG and the islanded load. In fact, an island can be easily formed even without 100% power matching – the power mismatch could be up to 30% [2] if only traditional protections are used, e.g., under/over voltage/frequency. The 30% power mismatch condition will drastically increase the islanding probability. Second, even with a larger power mismatch, the time for voltage or frequency to deviate sufficiently to cause a trip, plus the time required to execute the trip (particularly if conventional switchgear is required to operate), can easily be greater than the typical reclose time on the distribution circuit. Third, the low probability argument is based the study of photovoltaic DG applications. The photovoltaic DGs are mostly single phase, and at very low penetration in the distribution system. The probability of the DG output reaching the load power

level is very low. Furthermore, even if there is close matching, it is very difficult for a single-phase system to sustain the voltage and frequency in an island. Due to economic ($/kW) and efficiency reasons, modern DG power levels are getting higher and higher. Most DGs currently installed, or being installed, use three-phase synchronous generators. This increasing DG penetration, as well as the increased presence of larger-size DG units, increases the possibilities for islanding.

Regardless of these arguments, anti-islanding is still a major concern from utilities based on a recent survey. The top list of concerns includes: 1) anti-islanding, 2) voltage regulation, 3) protection coordination, and 4) power quality. As a result, islanding is an issue that must be addressed.

To prevent unintentional islanding, a transfer trip is traditionally used, mostly for larger units in the MW ranges. (A transfer trip is where the trip signals used to open switchgear on the distribution system are communicated to the DG to initiate simultaneous trip of the DG.) For smaller DGs connected at distribution level, a transfer trip is too expensive. Also, an increasing number of distribution systems are configured to provide multiple alternate feed points to a particular feeder section. A transfer trip can be exceedingly complicated and expensive to implement when trip signals from multiple points need to be communicated, as well as the current status of the system configuration to determine which trip signal is relevant at any given time. While other low cost communication means and infrastructures are under development, it is always desirable for DG to have local intelligence to detect islanding events. The local intelligence includes monitoring the grid by local sensing (passive means) and actively injecting signals to detect grid loss (active means).

Although there are many types of distributed generation, including traditional reciprocating engines and small gas turbines, as well as emerging technologies, e.g., fuel cells, microturbines, sterling engines, photovoltaics, wind turbines, basically, there are two types of interfaces for grid interconnection. One type is rotating machines, including synchronous machines and induction machines. The other is an inverter, as part of the overall power conditioning system that converts variable frequency variable voltage AC sources or DC sources to regulated frequency/voltage AC sources that can be interconnected to the grid. The report will address both inverter-interfaced and synchronous machine-interfaced DGs.

A comprehensive survey of existing anti-islanding schemes was conducted. In the following, some of the key issues are highlighted based on the survey.

1.1.1 NDZ for Passive Schemes

It has been shown [2] that any passive anti-islanding protection will have non-detection zone (NDZ), i.e., if the DG and the load power match closely enough, the passive protection may not be able to detect the island because the monitored signals, such as voltage, frequency, or their derivatives are too small to detect. The non-detection zone is depicted in Figure 1-1. If the criterion is fast detection, such as to coordinate with circuit reclosing, the effective non-detection zone is expanded. Given the 100% DG/load power matching testing condition as defined in the testing Standards [3] [4], any passive scheme will fail the anti-islanding testing. Furthermore,

passive schemes tend to falsely trip, and widespread tripping of DGs due to a power grid disturbance can be detrimental to grid security [5]. In practical applications, passive schemes (relays) are still widely used as anti-islanding means, while the application limitations are normally specified, e.g., minimum load, minimum reverse power, etc. These specifications basically provide sufficient generation/load power mismatch so that traditional protection schemes can pick up the islanding event due to the fact that the power mismatch is outside of these schemes NDZ. This solution essentially limits the DG application and penetration in the long term.

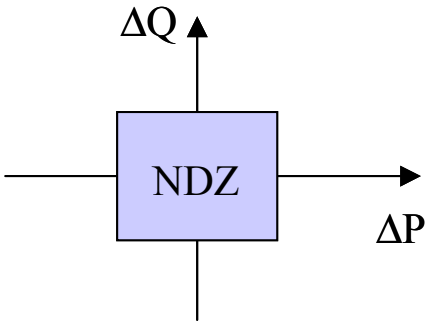


Figure 1-1. Non-detection zone for some passive schemes

1.1.2 NDZ for Some Active Schemes

Some active schemes use an actively injected disturbance added to the normal control signals. The concept of these schemes is to create power mismatch when the DG output and load power demand are closely matched. However, these schemes still could have a NDZ, i.e., when the power mismatch already exists, then the disturbance could coincidently balance the power mismatch. As a result, an island still could be formed. In this case, the NDZ is not centered at origin, but shifted as shown in Figure 1-2.

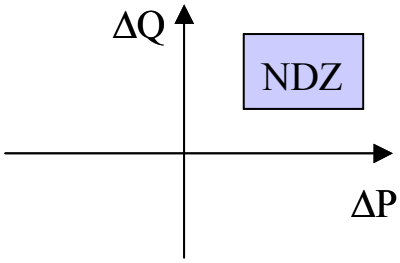


Figure 1-2. Non-detection zone for some active schemes

1.1.3 Power Quality Degradation for Some Active Schemes

Some active schemes use distorted signal injections. In this case, when the grid is lost, the waveform distortion will create a condition that the normal voltage or frequency will not be sustained. Figure 1-3 shows one example, where v(t) is the inverter output voltage, i(t) is the inverter output current. Another injection example is to create asymmetrical waveforms. These schemes will cause noticeable power quality degradation at normal grid-connected operation.

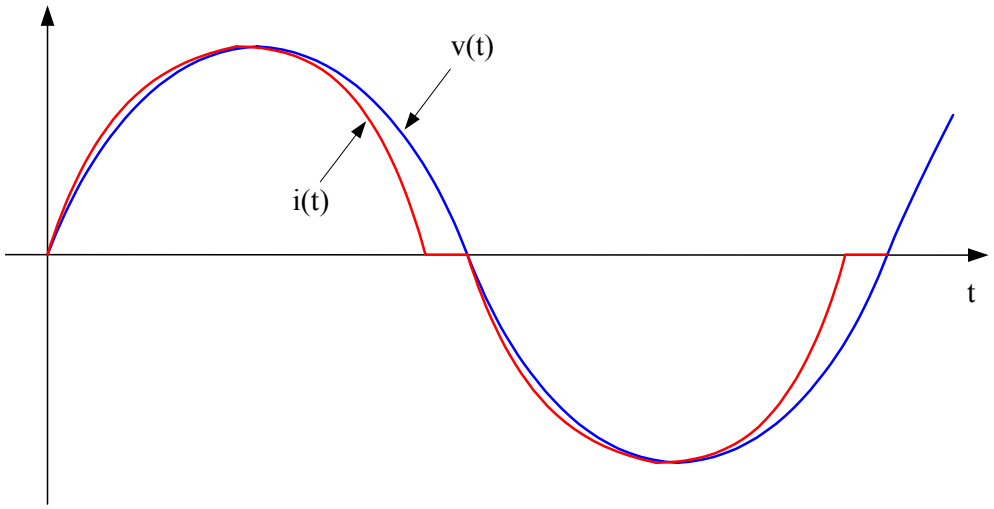


Figure 1-3. Example of power quality degradation caused by some active schemes

1.1.4 Multiple DG Dilution Effect

Some schemes may work for a single DG, but may not work for multiple DGs, for example, impedance measurement. This scheme injects a current perturbation signal at certain frequency on top of the base reference. With multiple DGs, as in Figure 1-4, the injected currents may cancel each other, unless they are synchronized (synchronization of injected signal is not always easy to do). Therefore, this class of schemes always has issues for multiple DGs operation.

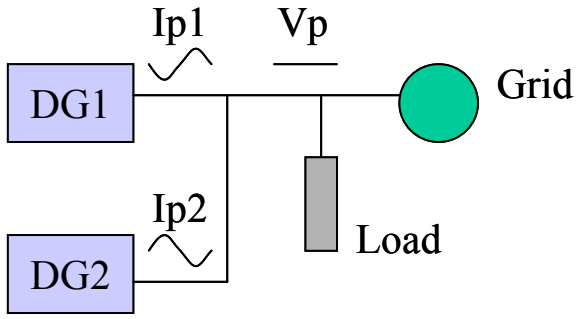


Figure 1-4. Multiple DGs' dilution effect for some active schemes

1.1.5 External Devices

In some applications, external devices are used for detecting islanding, e.g., ENS device. This solution, first of all, is too costly, especially for small DGs. Secondly, if the scheme uses the same impedance measurement principle, which may still have problem for multiple DGs. The scheme is illustrated in Figure 1-5.

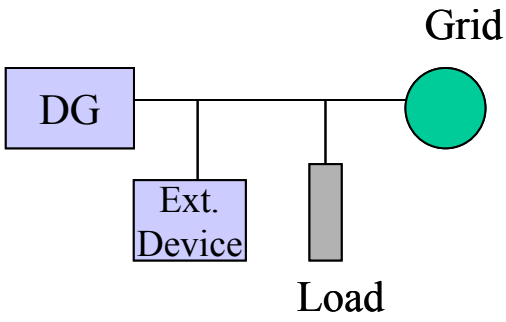


Figure 1-5. Some active schemes use external devices

1.1.6 Stability Concern Caused by Active Schemes

For schemes with positive feedback, there is always a concern that system stability may be affected, i.e., if the positive feedback is too strong, or the grid is too weak, the system may be destabilized even when the grid is connected. So far, the impact on the stability has not been well quantified.

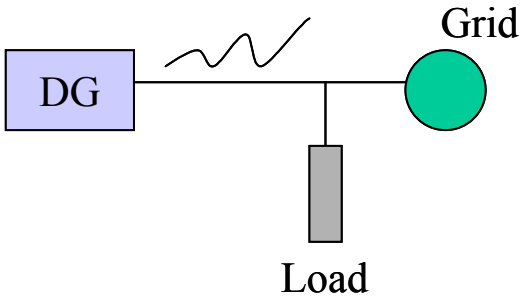


Figure 1-6. Stability concern caused by some active schemes

1.1.7 Anti-Islanding for Machine-based DG

Most anti-islanding schemes, especially active schemes, have been developed for inverter-based DGs. Little work has been done for machine-based DGs, partly due to their bigger size, which results in more engineering and more affordable in using external means. However, it is always desirable to have built-in anti-islanding control to have reduced cost and improved reliability because of the local intelligence.

1.2 Objectives

This report summarizes the study and development results of GE proposed anti-islanding schemes for both inverter-based and machine-based DGs. The objectives of the study include:

1. Propose anti-islanding schemes that feature no non-detection zone (NDZ), minimum power quality impact, low cost implementation (software code only), and work for multiple DGs
2. Provide design guidelines of the proposed schemes; the guideline helps optimize the design parameters and predict stability margins
3. Evaluate the proposed schemes under practical conditions
4. Experimentally test and validate the schemes.

1.3 Report Outline

The report is organized in four sections:

1. Study and development of anti-islanding control for inverter-based DG.
2. Testing of the anti-islanding control for inverter-based DG.
3. Study and development of anti-islanding control for synchronous machine-based DG.
4. Facility microgrid study.

2 Anti-Islanding Control for Inverter-Based DG

2.1 Grid-Connected Inverter Modeling

2.1.1 Data for the Inverter Modeling

The specifications of the three-phase inverter being modeled are listed in Table 2.1. The inverter is based on a GE Grid-Connected Inverter product platform used for sterling engines and fuel cells. There are two reasons for using a three-phase inverter to demonstrate the concept proposed by this work. First, it is close to a commercial product offering, so it is easier for technology transfer. The other reason is that, although previously the majority of grid-connected inverters were single-phase, mainly for PV applications, more and more new DGs tend to use three-phase inverters as grid interface. Therefore, technology for a three-phase inverter is gaining more and more practical value. Besides, the technology for three-phase inverters can be extended to single-phase inverters, as will be discussed later.

Table 2-1 Data for the Inverter/RLC load/Grid

Inverter			
fs	8000	Hz	switching frequency
Vdc	900	V	input DC bus voltage
Lf	2.100E-03	H	output inductance
Vl-l	480	V	line-to-line voltage
Vl-n	277	V	line-to-neutral voltage
P	100000	W	rated power
PF	1		power factor
P	100000	W	active power output
Q	0	Var	reactive power output
RLC Load			
R	2.304	Ohm	resistance
L	3.395E-03	H	inductance
C	2.072E-03	F	capacitance
Qf	1.8		load quality factor
fload	60	Hz	load resonant frequency
Grid			
f	60	Hz	grid frequency
Vl-l	480	V	line-to-line voltage
Vl-n	277	V	line-to-neutral voltage
Lgrid	3.056E-04	H	grid inductance, 5% of inverter impedance
Rgrid	0.012	Ohm	grid resistance, X/R=10

Generally, the overall power conditioning system includes front-end conversion and regulation, for example, DC/DC conversion for prime movers with DC output (e.g. fuel cell, PV, Battery), or AC/DC conversion for prime movers with AC output (e.g., microturbines, sterling engines). They may have an energy management system, such as a battery charger, at the DC bus. In either case, the input to the inverter is a regulated DC source. To simplify the discussion, the front end DC/DC or AC/DC converters are not modeled in the simulation study. In the models, the input to

the inverter is simplified as a DC voltage source. Another simplification is the inverter output filters, which could have different variations in practical applications, for example, the output filter could include L, or LCL, or LC plus a transformer, with or without harmonic filters, etc. Here to simplify the analysis, only an L (inductor) filter is considered.

2.1.2 Switching Model

Figure 2-1 shows the inverter, load and grid system diagram with inverter being modeled as switching model. The switching devices used for the inverter are IGBTs. In Saber, IGBTs can be modeled as ideal on/off switches that represent the inverter discrete switching behaviors. The switching model not only captures the voltage and current ripples, it also includes dead time and delays that are based on the IGBT device characteristics and gate driver design in the actual hardware. The controller used in the Saber model is based on actual production code in C language. The code includes all the sensing functions, scalings and quantization. This way, once the new algorithms are coded and simulated, the same code can be readily compiled and loaded to the hardware for testing.

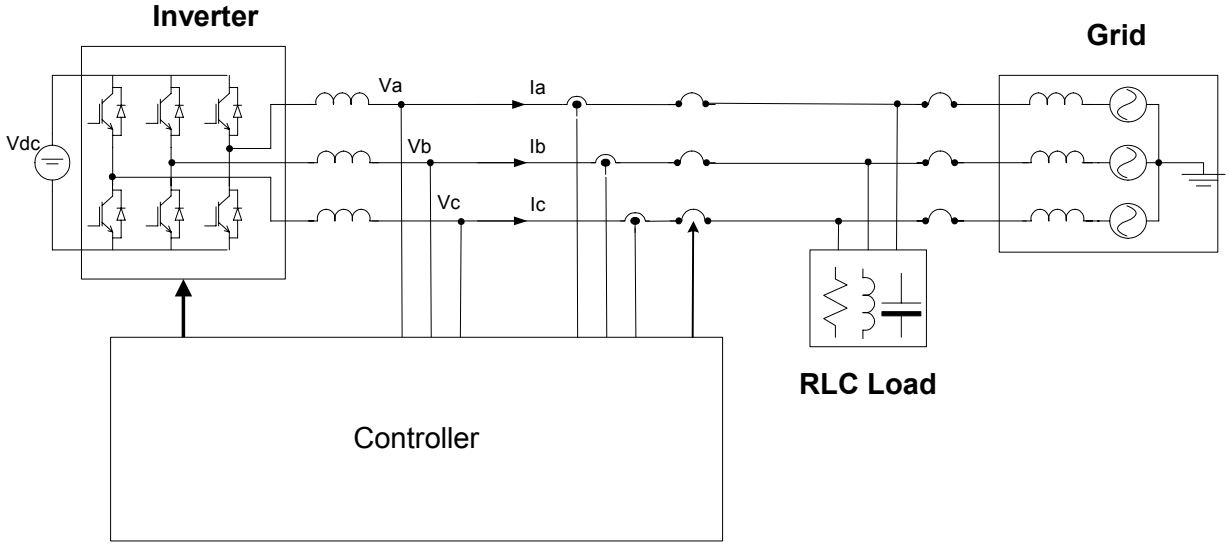


Figure 2-1. Inverter switching model with RLC load and grid

2.1.3 Averaged Model

Figure 2-2 shows the inverter, load and grid system diagram with inverter being modeled as an average model.

The switching model is ideal for validating new algorithms. However, it has two limitations that deviate from the average model development. The first limitation is that the switching model takes a long time to simulate. Typically, it takes more than 10 minutes to simulate several seconds. During the new algorithm development process, using the switching model would have been inefficient. The second limitation of using a switching model is that it cannot perform small-signal analysis due to its discrete behaviors. The two limitations can be overcome by using an average model. There are two parts that need to be averaged. One is the switching network. The other is the controller. The switching network can be represented by controlled voltage and current sources with averaged switching duty cycle. The controller, instead of using actual code with discrete behaviors, equivalent continuous functions, such as Proportional (P), Proportional-

Integral (PI), is modeled to represent the control behaviors. This way, the control functions are greatly simplified. Because of the averaged switching function and simplified controls, the average model simulation speed is at least one order faster than the switching model. Besides, the average model can be used for small-signal analysis, a function provided by some software, e.g.. Saber.

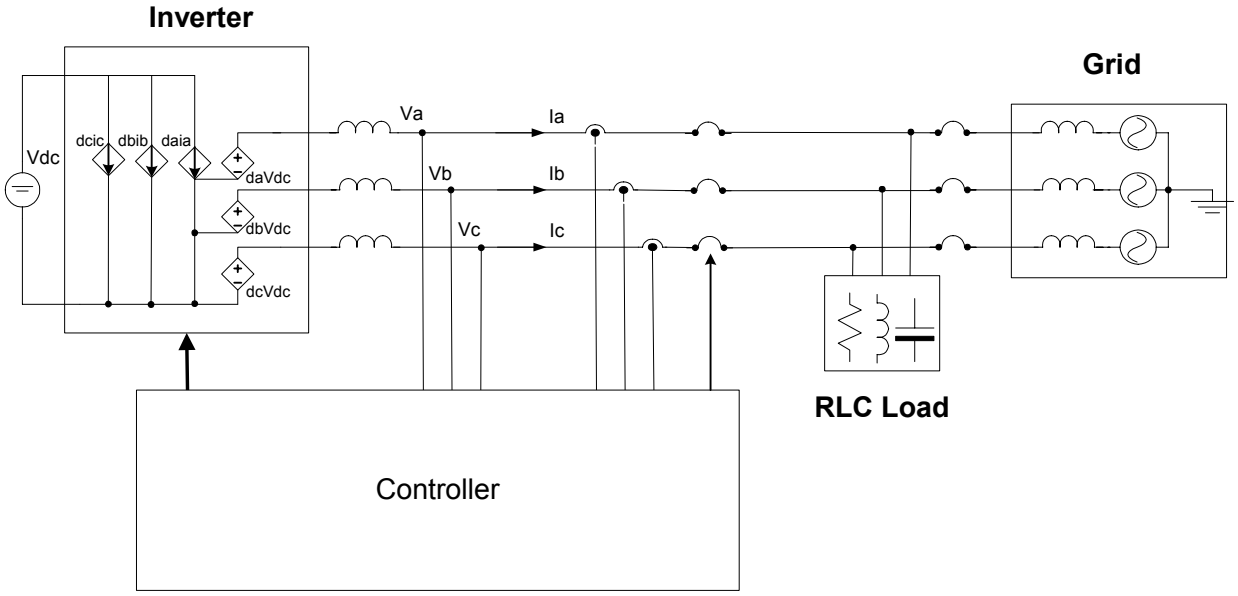


Figure 2-2. Inverter switching model with RLC load and grid

2.1.4 Control Block Diagram

There are two basic control modes for the grid-connected inverters. One is constant current control; the other is constant power control. It is still arguable that an inverter should be allowed to regulate voltage during grid-connected operation. The current IEEE 1547 Standard does not allow DG to actively regulate voltage, while some people in the industry suggest that DG voltage regulation may have some positive impact on the grid.

In this study, only constant current and power controlled inverters are considered. In detailed analysis, constant-current controlled inverters are used as an example to demonstrate the concepts, which can be easily extended to constant-power controlled inverters.

The control design for a three-phase inverter can be realized either in ABC (stationary) or in DQ (rotating) frames. The latter is more popular in modern digitally controlled inverters.

2.1.4.1 Constant Current Control**.** Figure 2-3 shows the inverter with constant current control. The inverter output currents are regulated to the given current references. The controller is greatly simplified with a few key functional blocks like ABC/DQ transformation, DQ phase-lock loop (PLL), summing function, linear regulator (proportional-integral) and DQ/ABC transformation. Many functions to deal with practical issues are not modeled in the average model, e.g., negative sequence regulation, DQ decoupling, device protection, etc. The

simplification, however, captures the key behaviors of the inverter and the dominant factors that may influence the anti-islanding control function.

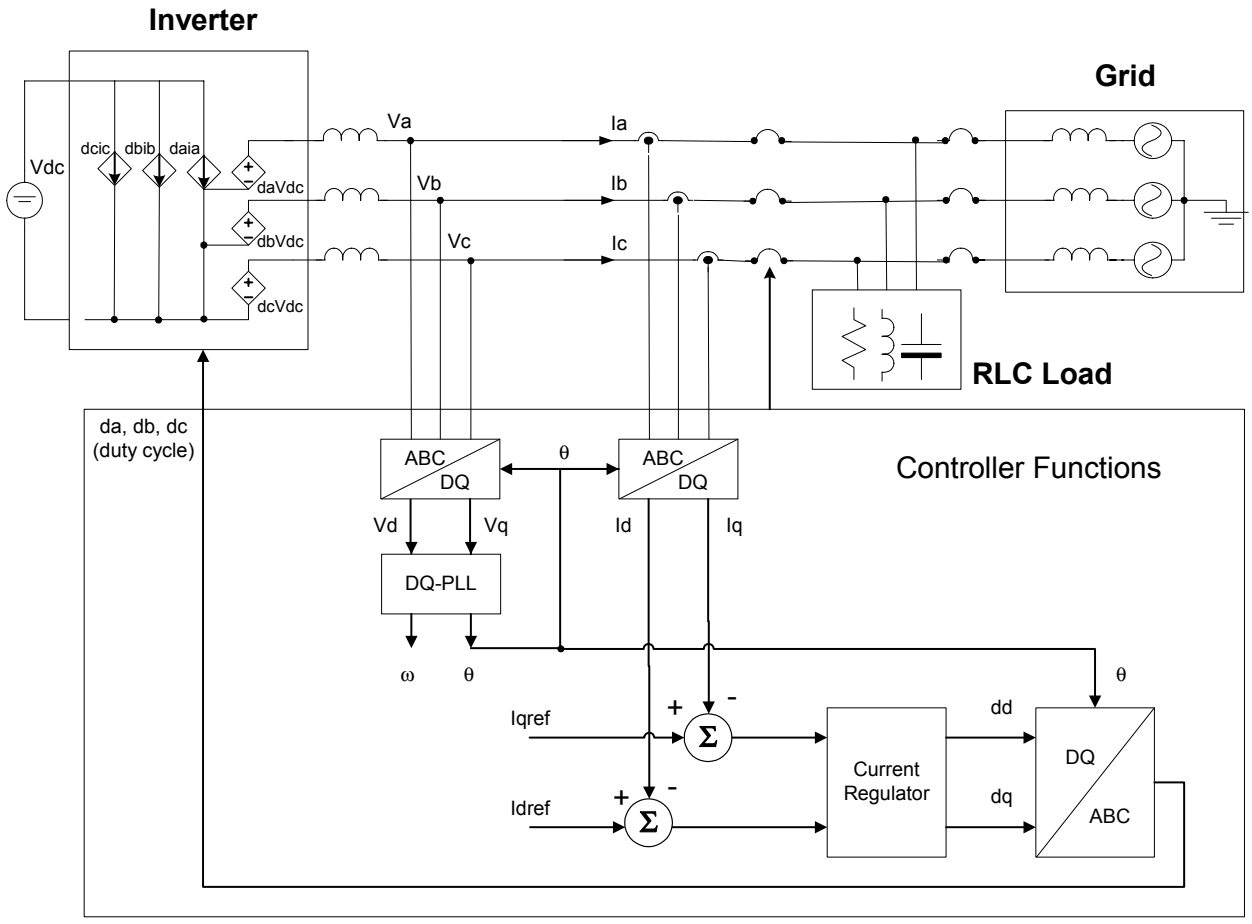


Figure 2-3. Constant-current controlled inverter block diagram

2.1.4.2 Constant Power Control. Figure 2-4 shows the inverter with constant power control. The power loops are on top of the current loops. In some cases, the reactive power reference Qref could be a power factor reference. The inverter output power will follow the power references. Usually, the power loops are slower than the inner current loops.

Figure 2-5 shows a variation of the constant power control. Instead of using the active power reference, a DC bus voltage is regulated, while the input to the inverter is a constant power source to represent the prime mover. In this case, the output of the DC bus regulator is proportional to the active power, thus the loop is on top of the idref. When DC bus voltage is increasing, meaning the power from the prime mover is increasing, it is charging the DC capacitor. In order to maintain the DC bus voltage, the idref will be increased so that the power can be transferred to the inverter output.

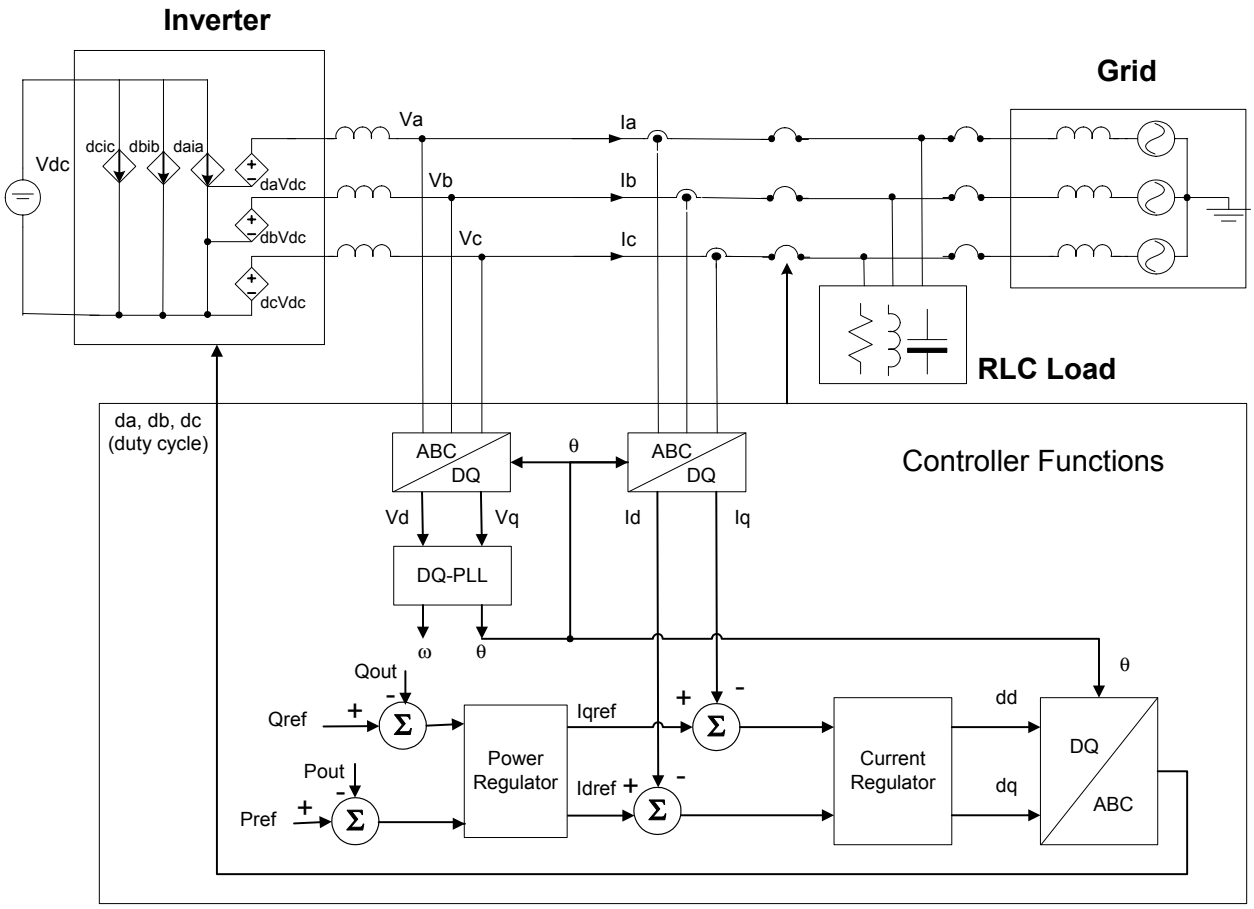


Figure 2-4. Constant-power controlled inverter block diagram

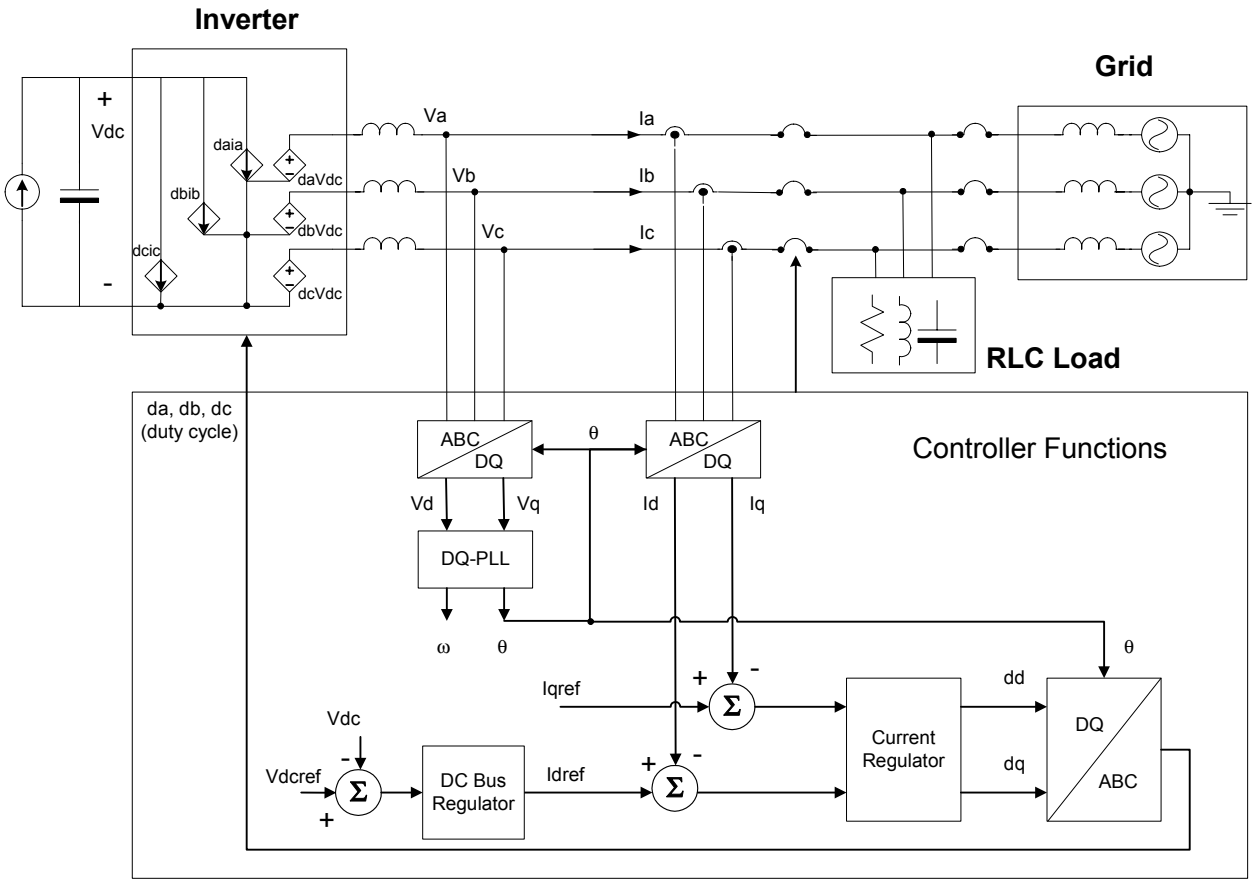


Figure 2-5. Constant DC bus voltage controlled inverter block diagram

2.2 GE Anti-Islanding Concepts and Implementations

2.2.1 Basic Concepts

The proposed GE anti-islanding schemes are based on two concepts: one is positive feedback, the other is DQ implementation. Neither of these concepts, alone, is new. However, combining these two concepts leads to a family of new anti-islanding schemes that are not reported elsewhere. It will be demonstrated later that the new family of the schemes have much better performance than existing ones.

2.2.1.1. Positive Feedback. All passive anti-islanding schemes have a non-detection zone (NDZ). Given the 100% power matching test condition, any passive scheme will fail. Besides, passive schemes are normally subject to nuisance trips, if the settings are too aggressive in order to reduce NDZ. Some active schemes still have NDZ if no positive feedback is used. It appears that, in order to guarantee no NDZ, active controls, such as using positive feedback, should be used. The basic idea behind the positive feedback control is to drive away the voltage or/and frequency once islanded.

Although the concept has been proposed for more than a decade, most studies are focused on numerical simulation and lab testing. The design of the schemes is mostly on a heuristic basis.

The proposed GE anti-islanding (AI) scheme also adopts the positive feedback concept. Both frequency-domain and time-domain analysis is conducted to provide insight into the scheme mechanism, as well as to provide details of design guidelines.

A brief description of the positive feedback mechanism is provided below.

First, an RLC load, as defined in Standards, is assumed. The relationships between the RLC load active/reactive power and the voltage/frequency are:

$$P = V^2 / R \tag{3.1}$$

$$Q = V^2(\omega C - 1/\omega L) \tag{3.2}$$

Based on (3.1) and (3.2), two positive feedback mechanisms can be established. One is voltage (magnitude) feedback; the other is frequency (of the voltage) feedback.

For voltage feedback, the mechanism is described as in Figure 2-6. When the inverter sensed output voltage is increasing, the anti-islanding (AI) feedback will command the inverter active power output to be increased. Due to the load characteristic in (3.1), the voltage will keep increasing in order to balance the active power. The increased voltage will further drive the inverter active power up due to the AI feedback. As a result, the voltage will be eventually out of the nominal ranges so that the islanding can be detected. Similar but opposite destabilization occurs when the sensed voltage is decreasing initially.

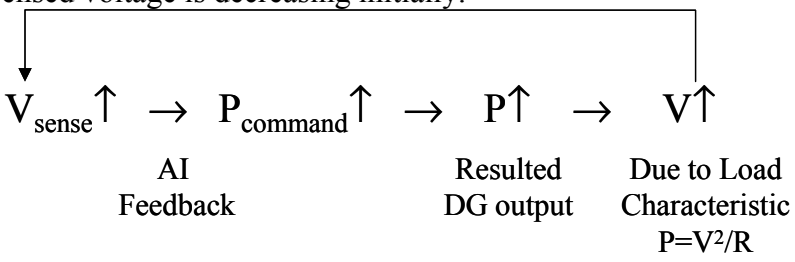


Figure 2-6. Voltage positive feedback concept

For frequency feedback, the mechanism is described in Figure 2-7. When the inverter sensed frequency is increasing, the anti-islanding (AI) feedback will command the inverter reactive power output to be increased. Due to the load characteristic in (3.2), the frequency will keep increasing in order to balance the reactive power[1]. The increased frequency will further drive the inverter reactive power up due to the AI feedback. As a result, the frequency will be eventually out of the nominal ranges so that the islanding can be detected. A mirror image response, with similar destabilization, occurs when the sensed frequency is decreasing initially.

[1] Unlike active power, reactive power has a sign. In this report, a positive reactive power Q means the reactive power is flowing into the inverter, and going out of the load according to Equation 3.2.

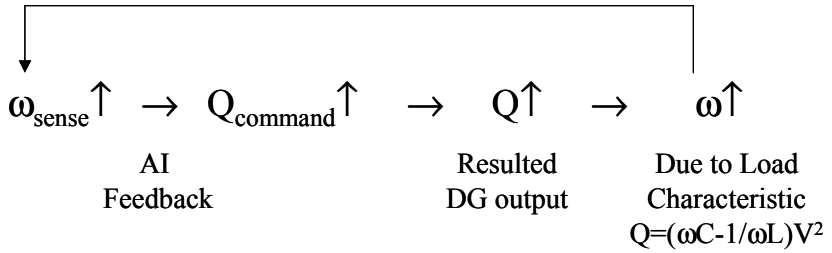


Figure 2-7. Frequency positive feedback concept

Certainly, this philosophy can apply to any DG, including inverter-based and machine-based DGs.

2.2.1.2 DQ Implementation. The positive feedback mechanism described in the previous section can be easily implemented in a three-phase inverter with control in DG frame. Here, a constant current-controlled inverter is used as an example for illustration.

There are two key concepts in the DQ implementation. First, the active power is proportional to the D-axis components, while the reactive power is proportional to the Q-axis components. Therefore, the active and reactive power command should feed into D-axis and Q-axis, respectively. Second, since the overall vector (voltage or current) is the synthesis of the D and Q axes, changing one axis not only changes the magnitude of the vector, but also changes the angle between D and Q axes. The angle change will result in frequency change, as frequency is the derivative of the angle.

Figure 2-8 illustrates a D-axis voltage feedback scheme. When the inverter sensed and computed D-axis voltage is increasing, the AI feedback will command the inverter D-axis current reference to be increased. This will result in increased active power output. Due to the load characteristic in (3.1), the voltage will keep increasing in order to balance the active power. The increased voltage, thus D-axis voltage, will further drive the inverter active power up due to the AI feedback. As a result, the voltage will be eventually out of the nominal range so that the islanding can be detected. Similar but opposite destabilization occurs when the sensed voltage is decreasing initially.

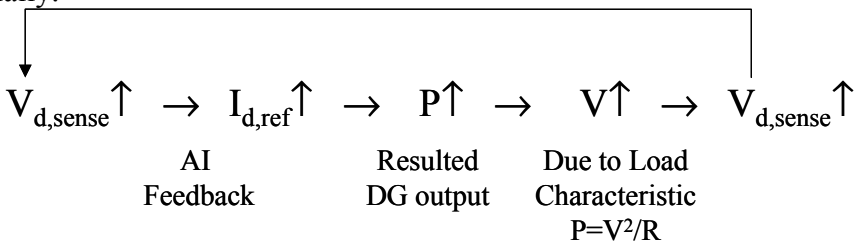


Figure 2-8. Voltage positive feedback in DQ implementation

Figure 2-9 illustrates a frequency feedback scheme. When the inverter sensed frequency is increasing, the AI feedback will command the inverter Q-axis current reference to be increased. This will result in increased reactive power output. Due to the load characteristic in (3.2), the frequency will keep increasing in order to balance the reactive power. The increased frequency will further drive the inverter Q-axis current, thus driving reactive power up due to the AI feedback. As a result, the frequency will be eventually out of the nominal ranges so that the

islanding can be detected. Again, destabilization also occurs when the sensed frequency is decreasing initially.

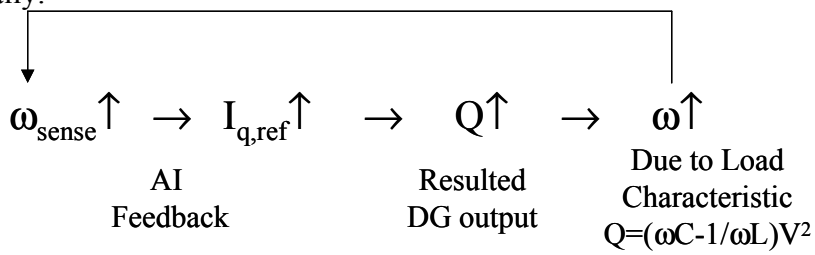


Figure 2-9. Frequency positive feedback in DQ implementation

The difference between Figure 2-6 and Figure 2-8 implementation is that, in Figure 2-8, due to DQ implementation, both voltage and frequency will be driven. As illustrated in Figure 2-10, driving the D-axis will affect both the vector length and angle. The angle change will result in frequency change. When the inverter is operating at unity power factor, however, the angle will not be affected because the voltage only has D-axis component.

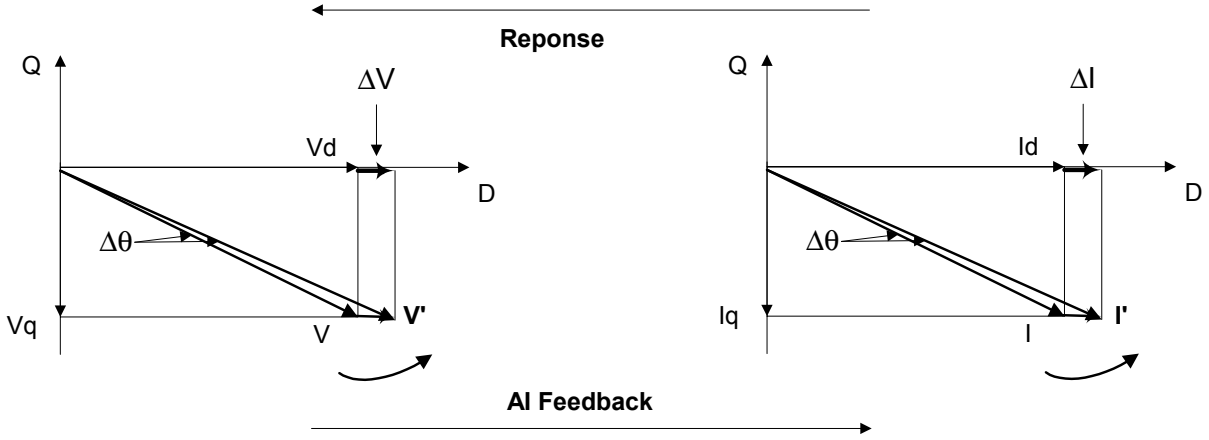


Figure 2-10. Vd change causes both magnitude and angle changes

Aside from the feedback shown in Figures 2-8 and 2-9, the DQ implementation can generate a family of schemes by using different feedback paths, for example, from Vd to Idref, from Vd to Iqref, from Vq to Idref, from Vq to Iqref, from ω to Idref, from ω to Iqref. As long as the feedback paths can establish the basic mechanisms shown in Figure 2-6 or Figure 2-7, the positive feedback will work as anti-islanding control. The multiple-path feedback in DQ frame is the second basic concept of the GE anti-islanding schemes.

2.2.2 GE AI Implementations

Based on the positive feedback and DQ implementation concepts, a family of new schemes has been proposed and implemented.

2.2.2.1 Voltage Schemes. Figure 2-11 shows one of the voltage feedback schemes, called voltage scheme 1, from Vd to Idref. The scheme is implemented with the highlighted (red) path – Vd is passed by a band-pass filter (BPF), a gain, and a limiter, and becomes a current variation Δi adding to the Idref. The design guideline of the BPF, gain and limiter will be discussed later in the report.

Other voltage schemes, such as from Vd to Iqref, Vq to Idref, and Vq to Iqref, can also be implemented, but not discussed here. The voltage scheme mentioned hereafter is referred to as the voltage scheme 1 in Figure 2-11.

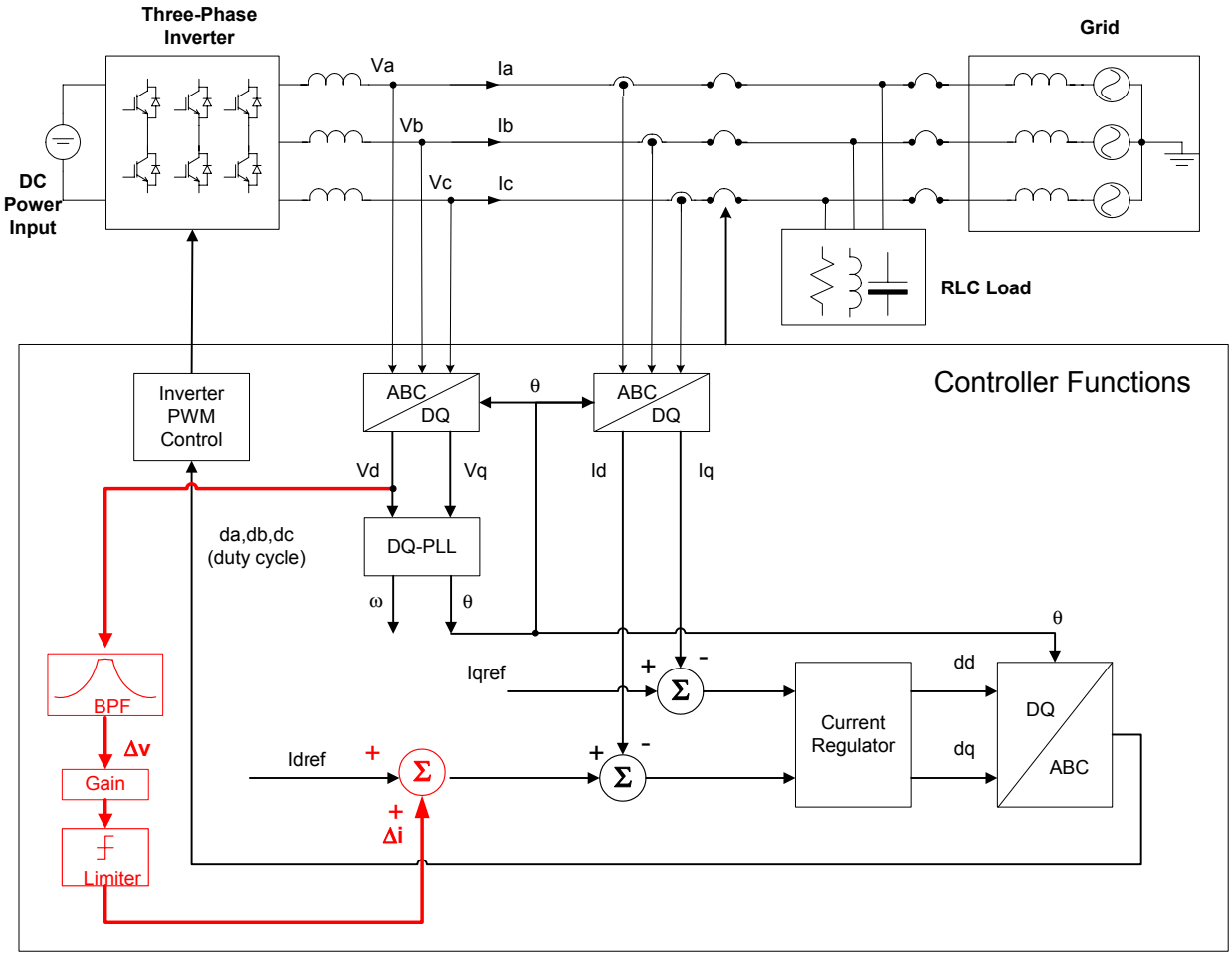


Figure 2-11. Voltage scheme 1: Vd to Idref

2.2.2.2 Frequency Schemes. Figure 2-12 shows one of the frequency feedback schemes, called frequency scheme 1, from ω to Iqref. The scheme is implemented with the highlighted (red) path – ω is passed by a band-pass filter (BPF), a gain, and a limiter, and becomes a current variation Δi adding to the Iqref. The design guideline of the BPF, gain, and limiter will be discussed later in the report.

Other frequency schemes, such as from ω to Idref, etc., can also be implemented, but not discussed here. The frequency scheme mentioned hereafter is referred to as the frequency scheme 1 in Figure 2-12.

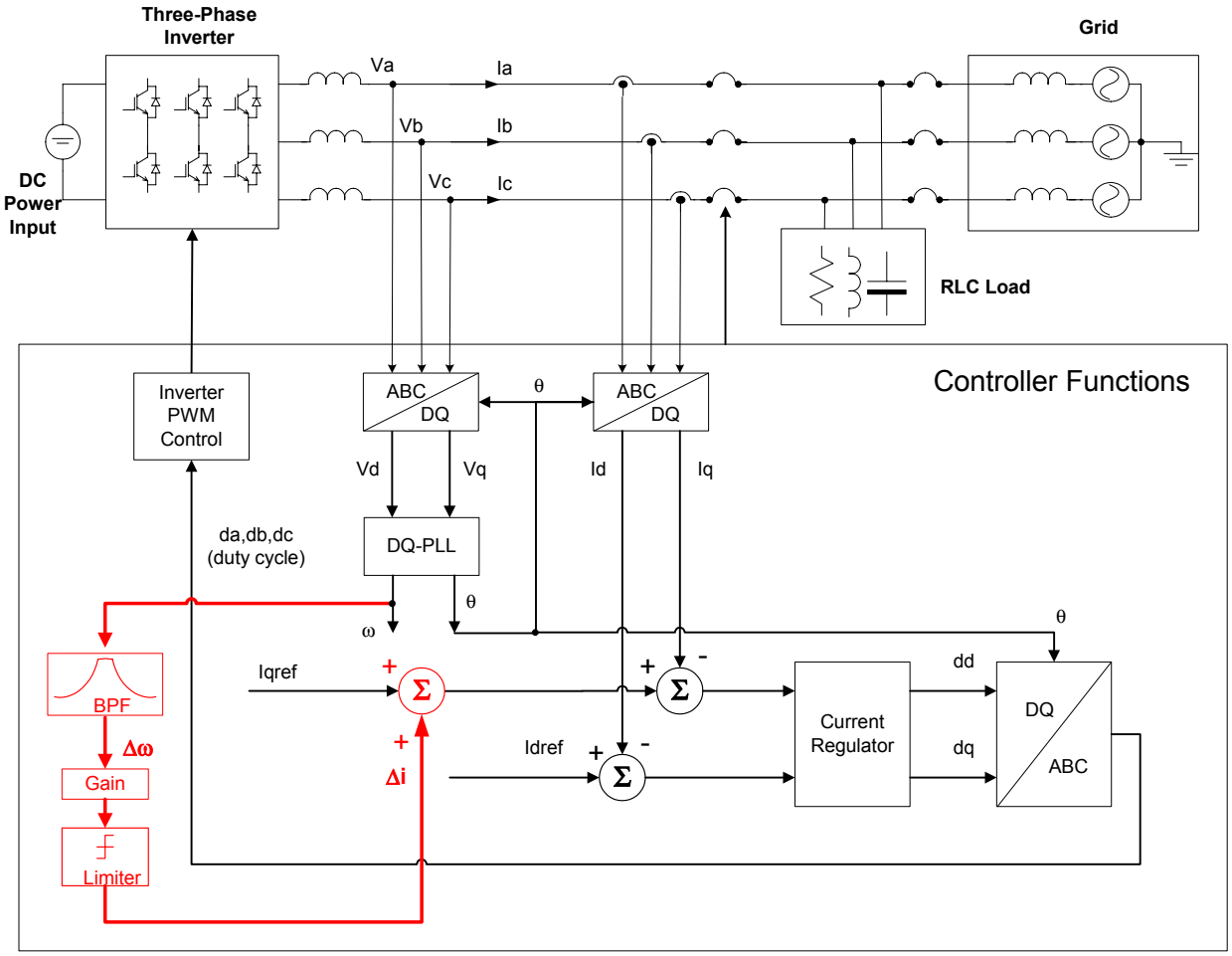


Figure 2-12. Frequency scheme 1: ω to Iqref

2.2.2.3 Implementations for Single-Phase Inverter. Philosophically, the concept can apply to any power generation systems, including single-phase systems. The key is to establish the positive feedback mechanism and DQ implementation. For a single-phase inverter, DQ implementation is not as obvious as in a three-phase inverter. In fact, single-phase quantities can still be transformed into DQ frame by creating a virtual Q-axis. For example, a DQ phase-lock loop can be implemented for a single-phase system, as shown in Figure 2-13. Once the DQ quantities are obtained, the same positive feedback and DQ implementation concepts can apply to the single-phase system. Figure 2-14 shows the overall implementation for a single-phase inverter with a simplified control block diagram.

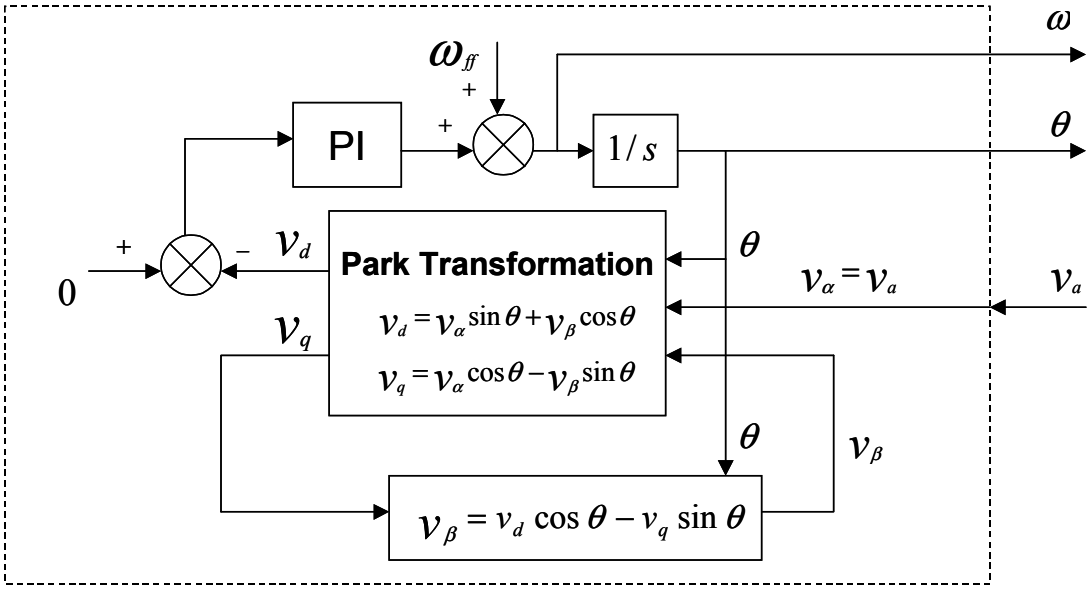


Figure 2-13. DQ phase lock loop implementation for a single-phase system

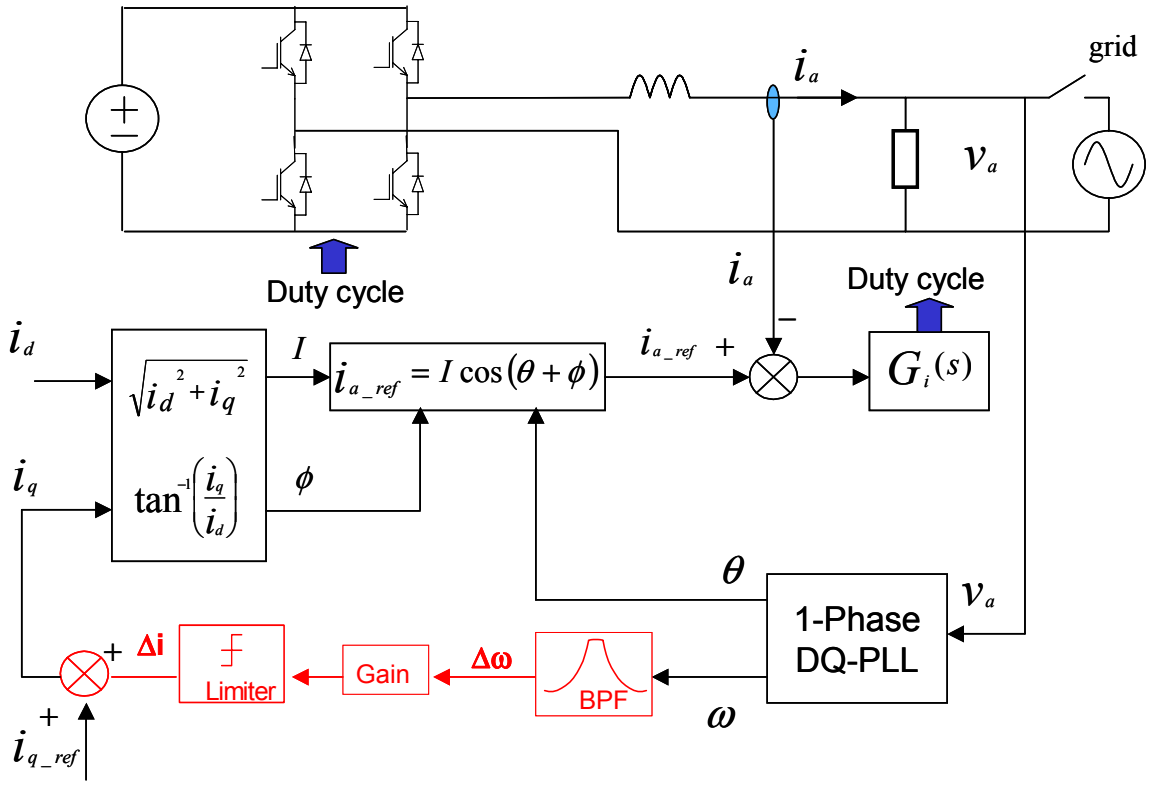


Figure 2-14. Frequency feedback scheme implementation for a single-phase inverter

2.3 Design Guidelines Based on Frequency-Domain Analysis

In order to understand the GE anti-islanding schemes, and to support the development of design guidelines, a frequency domain analysis has been conducted. The frequency-domain analysis is based on a loop-gain concept.

2.3.1 Stability Theory Based on Loop Gain

Figure 2-15 shows a generic feedback system, which includes the plant open loop transfer function G(s), compensation H(s), reference x, and output y. The loop gain, T(s)=G(s)H(s), can be measured by opening the loop, as shown in Figure 2-16, and injecting small-signal perturbation ε(s), then measuring the T(s). The loop gain T(s) Bode plots can be used as control loop design performance (e.g. cross-over frequency) evaluation, as well as stability [e.g., gain margin (GM), phase margin (PM)] evaluation. The anti-islanding control design guidelines can also be analyzed based on the loop gain measurement.

Figure 2-17 shows a stable system loop gain Bode plots; while Figure 2-18 shows an unstable system loop gains.

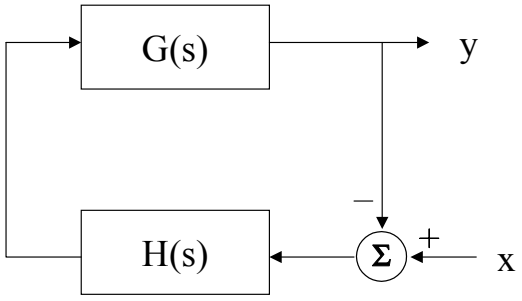


Figure 2-15: Feedback system with closed loop.

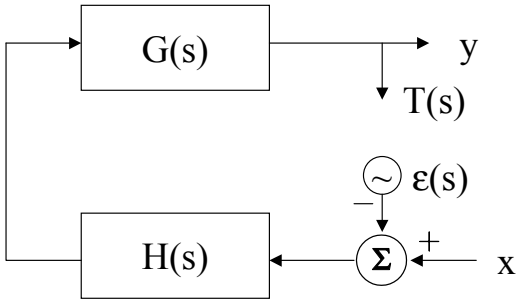


Figure 2-16. Feedback system with open loop for loop gain measurement

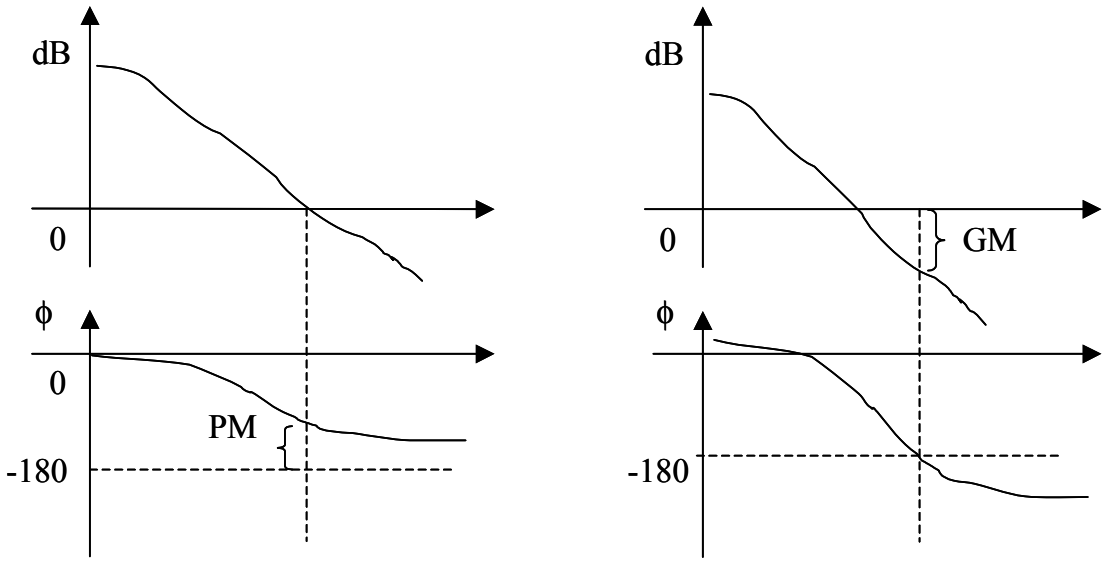


Figure 2-17. Loop gain Bode plots for a stable system

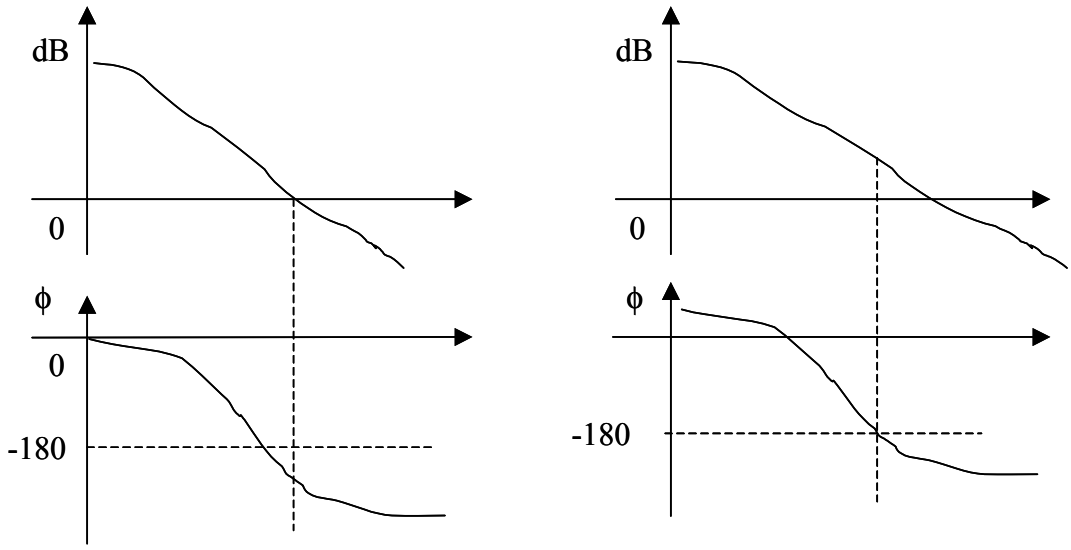


Figure 2-18. Loop gain Bode plots for an unstable system

To measure loop gain of the proposed schemes, the loop is opened as shown in Figure 2-19, taking the voltage scheme as an example. The small-signal perturbation is injected as injection(f), then the response of $\Delta i(f)$ is measured after reaching steady state. The measured Δi is the loop gain. Although Saber provides the small-signal analysis function based on the average model, its validity is in question for a high-order system. After validation by time-domain simulation, it is concluded that the Saber built-in small-signal function does not provide satisfactory results for the system being studied here. Therefore, the approach of using individual frequency injection in time-domain is used to generate the loop gain Bode plot. In the following sections, the individual frequencies of the injection signals are 0.5Hz, 1Hz, 5Hz, 10Hz, 20Hz, 100Hz, and 1000Hz. The Bode plots are generated using curve fitting based on the measured response of the individual points.

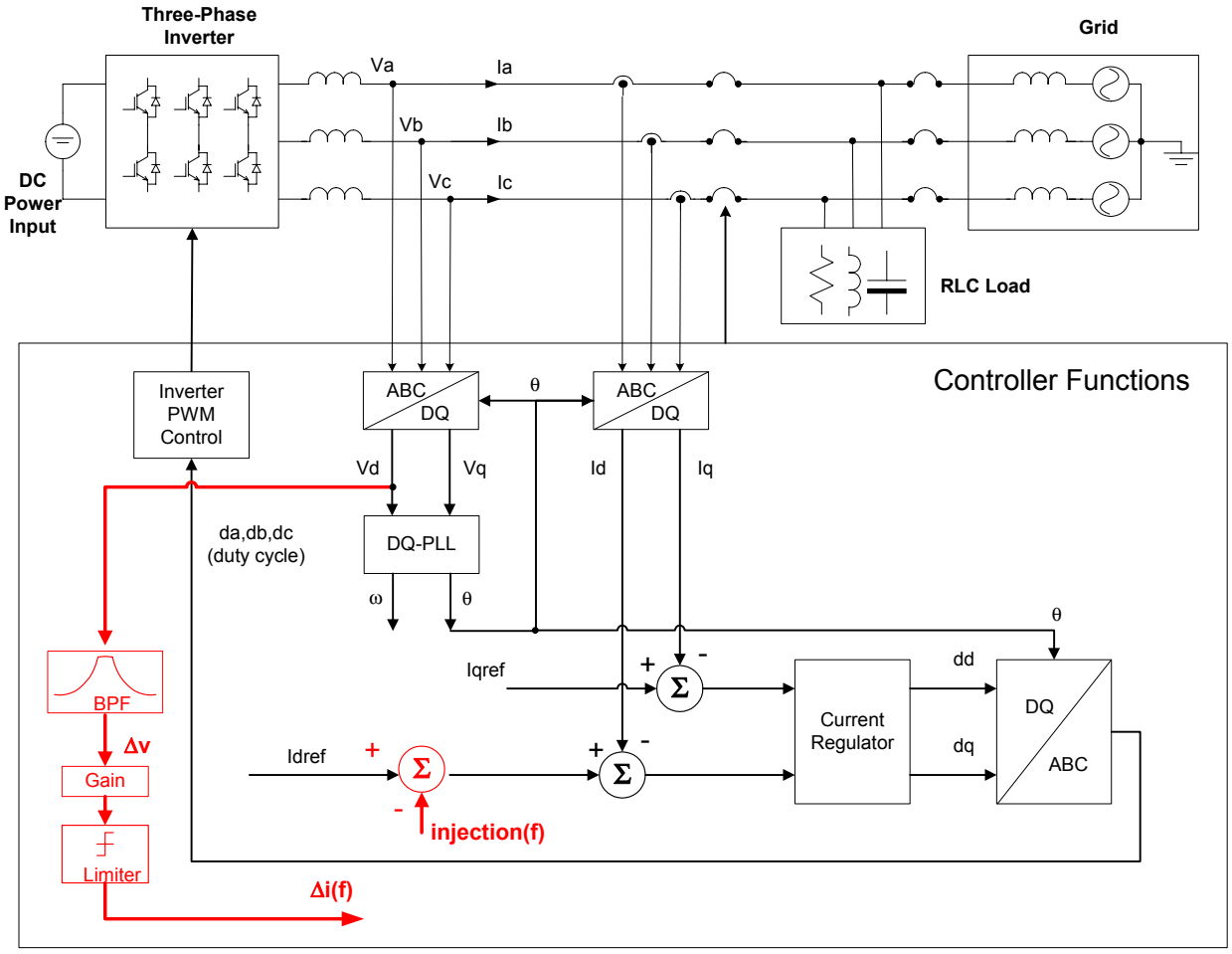


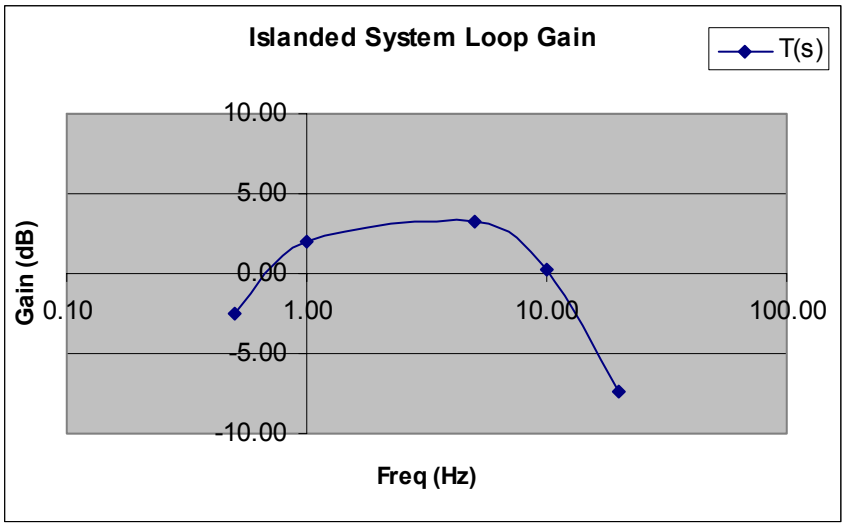
Figure 2-19. Loop gain measurement for the voltage scheme

2.3.2 GE AI Design Guidelines

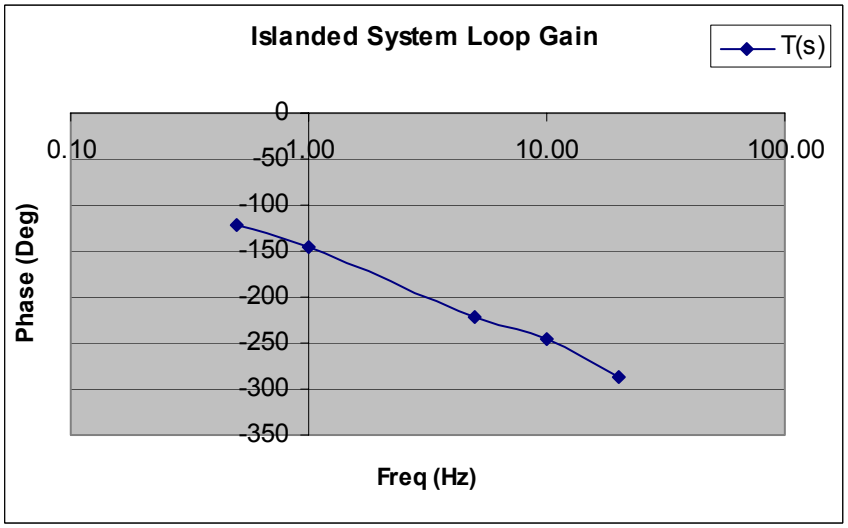
In the following, the voltage scheme is used as an example to illustrate the design guidelines.

2.3.2.1 Gain. There are two critical design criteria for the gain. First, when the DG is grid connected, the gain should be small enough so that the system is stable, as indicated by sufficient gain and phase margins. When islanded, the gain should be large enough so that the islanded system is unstable, indicated by a loop gain with no phase or gain margins, for example, the phase is more than 180 degree lagging when the gain is above 0 dB. Otherwise, the system may run into another steady state that may still be within nominal ranges, thus resulting in a non-detection zone.

Figure 2-20 shows the voltage-scheme loop gain Bode plots after islanding. The inverter operates at full power (100kW). It shows an unstable islanded system – when the gain is crossing 0dB (around 10Hz), the phase is lagging more than 180 degrees (around –250 degrees).



(a) Gain



(b) Phase

Figure 2-20. Islanded system loop gain for the voltage scheme

Given the same design, the loop gain when grid-connected is also examined, as shown in Figure 2-21. The gain is below 0 dB at all measured frequencies. Therefore, there is no need to examine the phase. The system is stable.

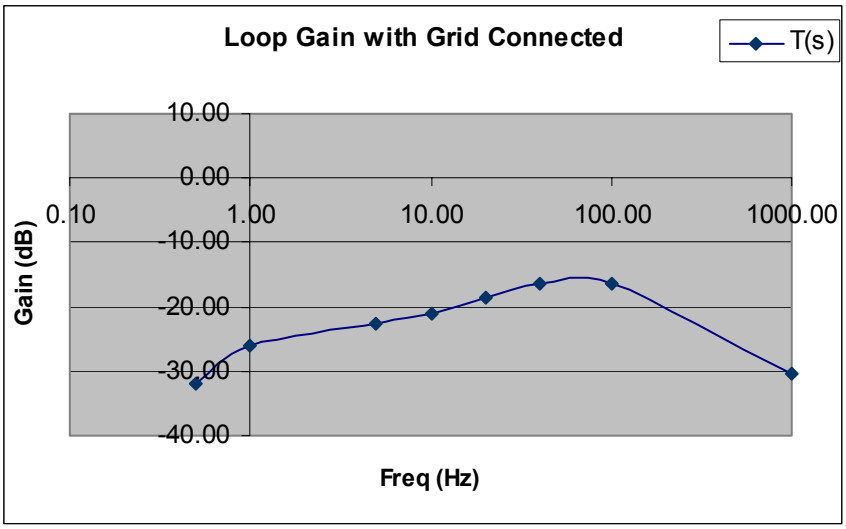


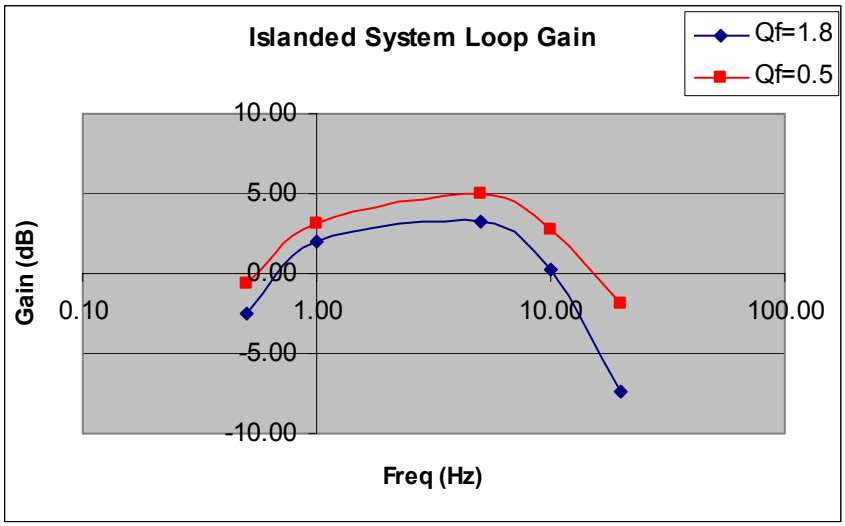
Figure 2-21. Loop gain of the voltage scheme when grid connected

2.3.2.2 Band-Pass Filter. The reason for using a band-pass filter (BPF) is to avoid noise injection (low-pass needed) and DC offset (high-pass needed) caused by AI loop. The noise will cause power quality problems, while the DC offset will affect the steady state reference tracking. Because of these two conflicting requirements, an appropriate band with both high-frequency noise and low frequency offset performance must be traded off. Given the 2-second anti-islanding protection requirement, a 1 to 10Hz (0.1s to 1s responding time) band-pass filter is chosen for the design.

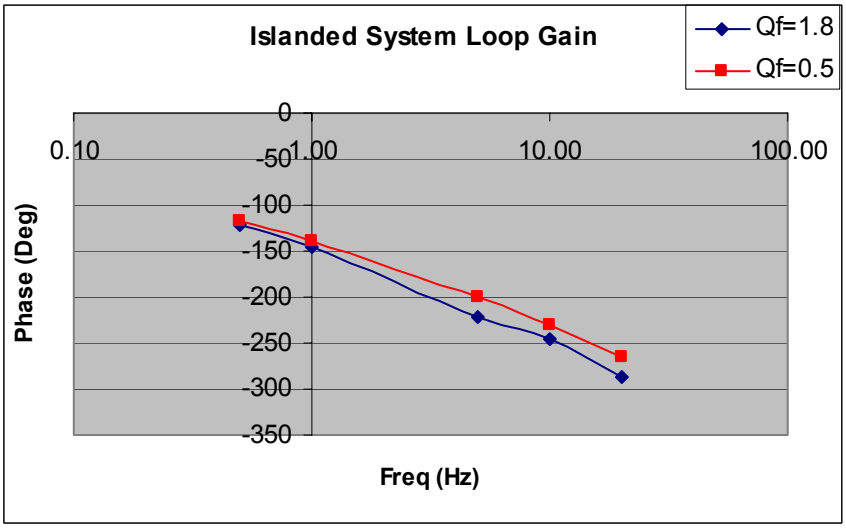
2.3.2.3 Limiter. The limiter function is to specify the maximum allowable current injection. Two factors determine the limiter settings. One is the inverter over-current capability. The other is the maximum allowable power factor, if injecting the current to Iqref. In the design, 150% current and 0.8 power factors are assumed as limits. Based on these two limitations, the value for the limiter can be designed accordingly.

2.3.2.4 Quality Factor. In addition to the control design criteria for gain, BPF, and the limiter, the following analysis shows different operational factors that affect the loop gains, such as, load quality factors, power levels.

Figure 2-22 shows the loop gains with different quality factors, Qf=0.5 and 1.8, for the voltage scheme. It can be seen that the loop gain decreases when Qf increases. Therefore, a higher Qf is a worse case scenario. The design based on worst-case Qf=1.8 should work for other lower Qf conditions. Meanwhile, one must make sure that the loop gain when grid connected must be below 0dB, as shown in Figure 2-21. This will ensure the system is stable while connected to the grid, and when islanded, the island will not be sustained due to its instability.



(a) Gain

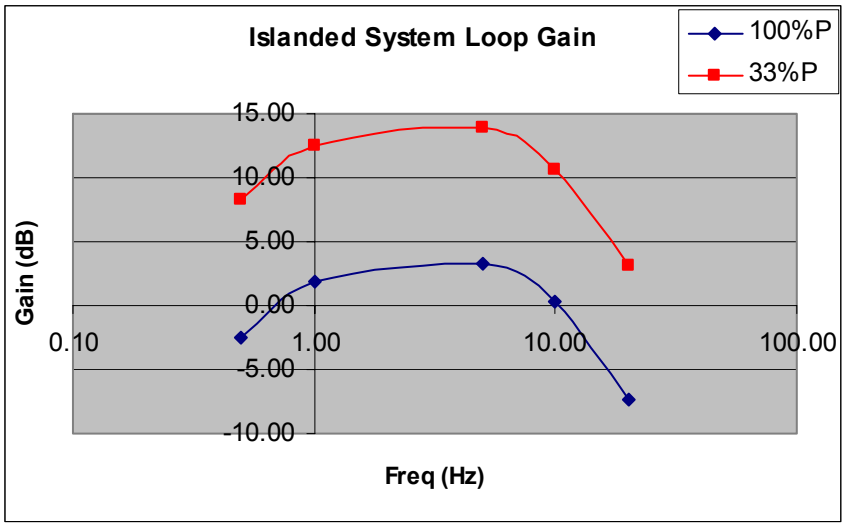


(b) Phase

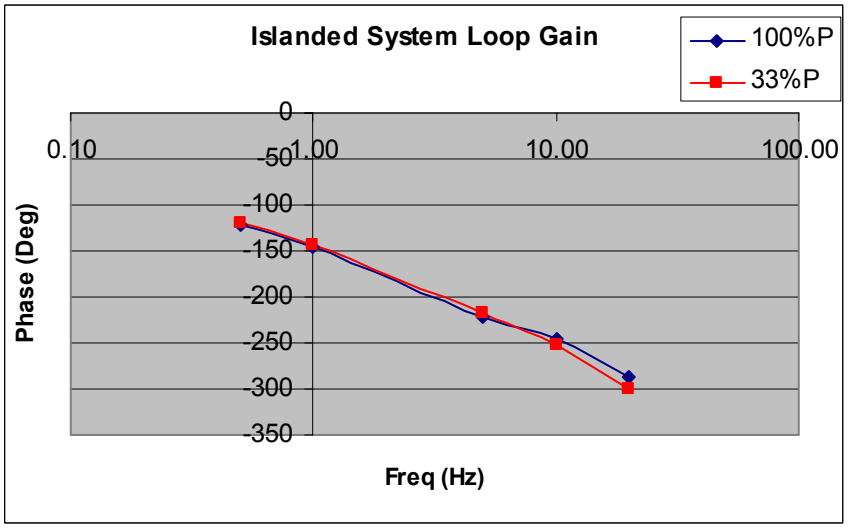
Figure 2-22. Loop gains of the voltage scheme for different quality factors (Qf)

2.3.2.5 Power Level. The loop gains under different power levels are also examined. As shown in Figures 2-23, a higher power will result in a lower loop gain. It implies that:

- The worst-case design point is at full power.
- In order to make the AI control response consistent at different power levels, the AI feedback gain can be designed adaptive to the power by using gain-scheduling control technique. This study of the gain-scheduling control is not covered in this report.



(a) Gain



(b) Phase

Figure 2-23 Loop gains of the voltage scheme with different power levels

The grid impedance impact on the loop gains when grid connected will be discussed in a later section.

In summary, the frequency-domain analysis not only provides the insight of the schemes, it also helps optimize the design parameters and identify dominant factors that influence the performance.

2.4 Performance Evaluation with Time-Domain Simulation

The switching model of the inverter is used for the time-domain simulations. The switching model not only demonstrates the system behaviors, it also provides waveform quality information, e.g., Total Harmonic Distortion (THD). Besides, the code used in the switching model is based on the code for the actual hardware. Therefore, the simulations can help optimize the parameter settings for experiments and guide the experimental testing.

For all simulations, the inverter anti-islanding function is enabled at 1.4s and the grid is disconnected at 2.4s.

2.4.1 Performance Evaluation for Voltage Scheme

2.4.1.1. Baseline Case without Al. Before testing the effectiveness of the proposed anti-islanding schemes, a baseline case without anti-islanding is simulated, as shown in Figure 2-24. The inverter is operating at 100kW. The load quality factor is 1.8. With close generation/load matching, the inverter can easily run on with voltage and frequency at nominal ranges, as shown in Figure 2-24(a). A small noticeable deviation of the frequency [Figure 2-24(a) bottom trace] is due to a small reactive power mismatch [Figure 2-24(b) middle trace]. The frequency will reach steady state when the reactive power is balanced.

2.4.1.2. Voltage Scheme with P=100kW, Qf=1.8. Figure 2-25 shows the anti-islanding case with the voltage scheme under the same power level and load quality factor conditions as in the previous section. It can be seen that the voltage [Figure 2-25(a) top trace] becomes unstable after islanding. The frequency [Figure 2-25(a) bottom trace] does not change much because the inverter is controlled to unity power factor. The feedback output delta_i [Figure 2-25(b) bottom trace] is dynamically driving the inverter output current change that leads to voltage change. The oscillation is caused by the current limit that results in saturation and nonlinear behavior.

The detection of the islanding can be either under/over voltage/frequency, and/or the unique dynamic characteristics that are not exhibited during grid-connected operation, normal or even transient.

2.4.1.3 Voltage Scheme with P=33kW, Qf=1.8. Figure 2-26 shows that the scheme works fine with lower power level (33kW). In fact, compared with the 100kW case, the dynamic is even stronger as predicted in the frequency-domain analysis, which indicates that the positive feedback loop gain is higher at lower power level. It can be seen from Figure 2-26(a), the voltage dips more and even the frequency is moving away from its normal range. Here, no gain-scheduling control is considered in the simulation. With gain-scheduling control, the response dynamic could be independent from power level.

2.4.1.4. Voltage Scheme with P=100kW, Qf=5. Figure 2-27 shows the case that a larger load quality factor Qf will reduce the feedback loop gain, resulting in less effective control of the anti-islanding alorithm. This is consistent with the frequency-domain results.

2.4.1.5 Voltage Scheme with P=100kW, Qf=1.8, and Reduced Gain. When the gain in the feedback loop is reduced, the anti-islanding control becomes ineffective. Figure 2-28 shows a case with the gain halved from the previous design. It can be seen from Figure 2-28(a) that the voltage and frequency stay at normal levels, even though there is a small dynamic change in the current injection delta_i from the AI feedback loop. Apparently, the loop is not strong enough to drive the voltage and frequency away. After a small dynamic, the system maintains the balance and continues to run on.

This is consistent with the frequency-domain results shown in Figure 2-22, where the loop gain is below 5dB. With the gain halved, the loop gain will have -6dB (=20log(1/2)) reduction that will lead to a stable system because the loop gain will be below 0dB. Basically, the time-domain simulation results can be predicted by the frequency-domain analysis.

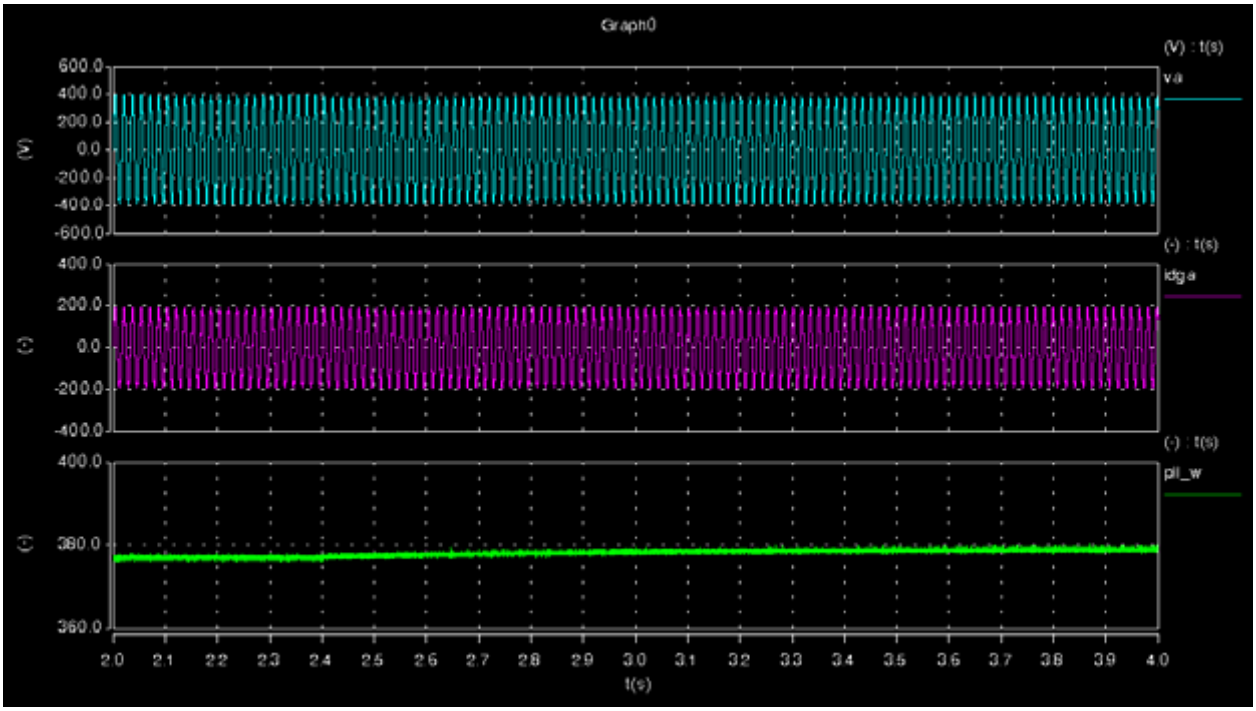


Figure 2-24(a). Simulation results without anti-islanding function enabled (Qf=1.8,100kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency in (rad/s))

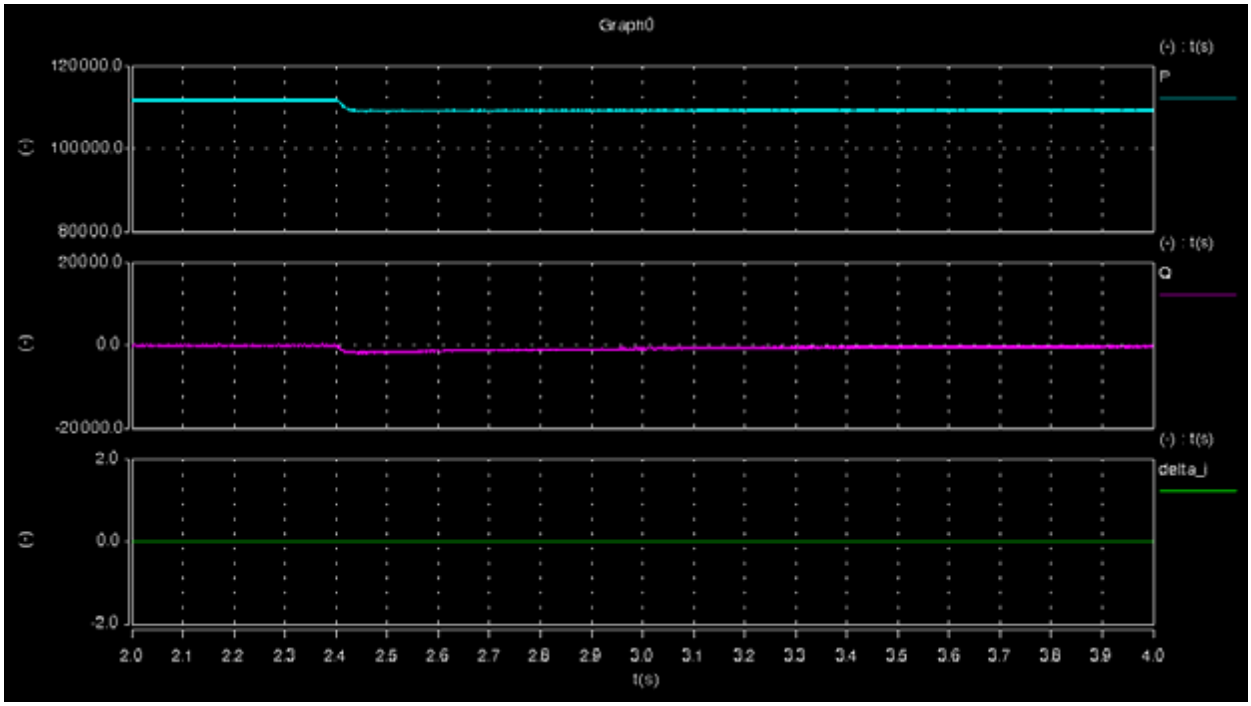


Figure 2-24 (b). Simulation results without anti-islanding function enable (Qf=1.8, 100kW).

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

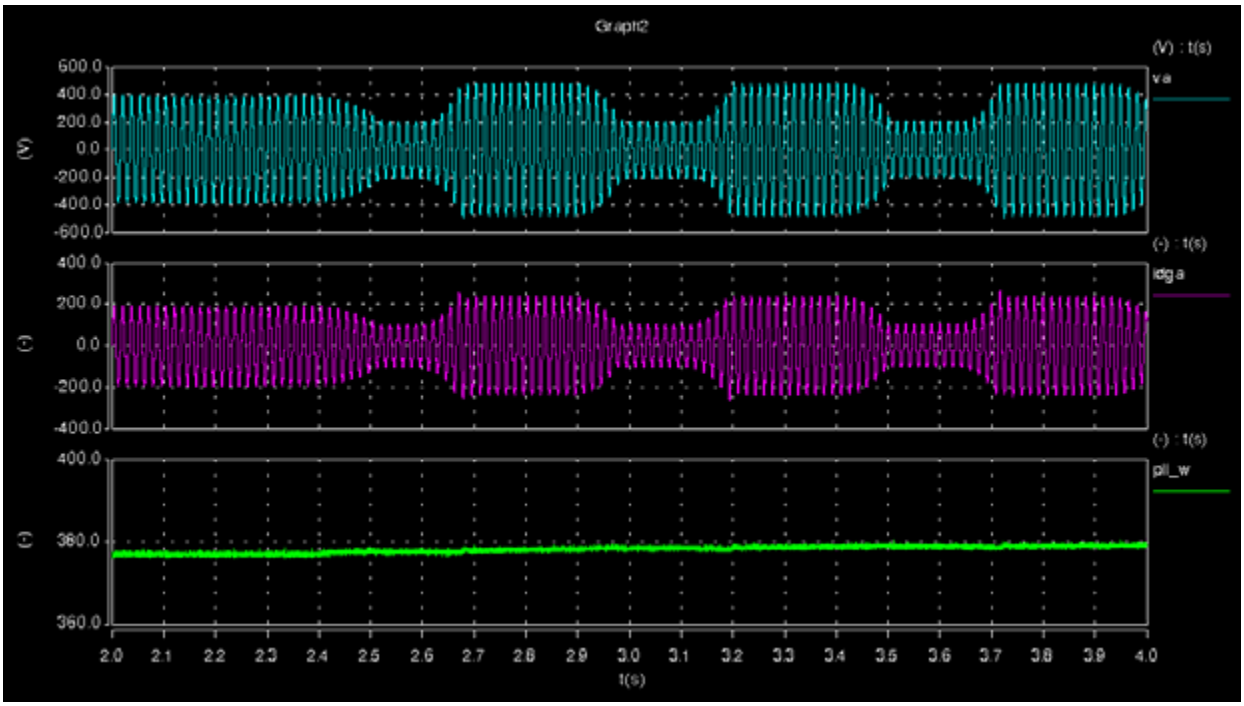


Figure 2-25(a): Simulation results with voltage feedback scheme (Qf=1.8, 100kW).

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

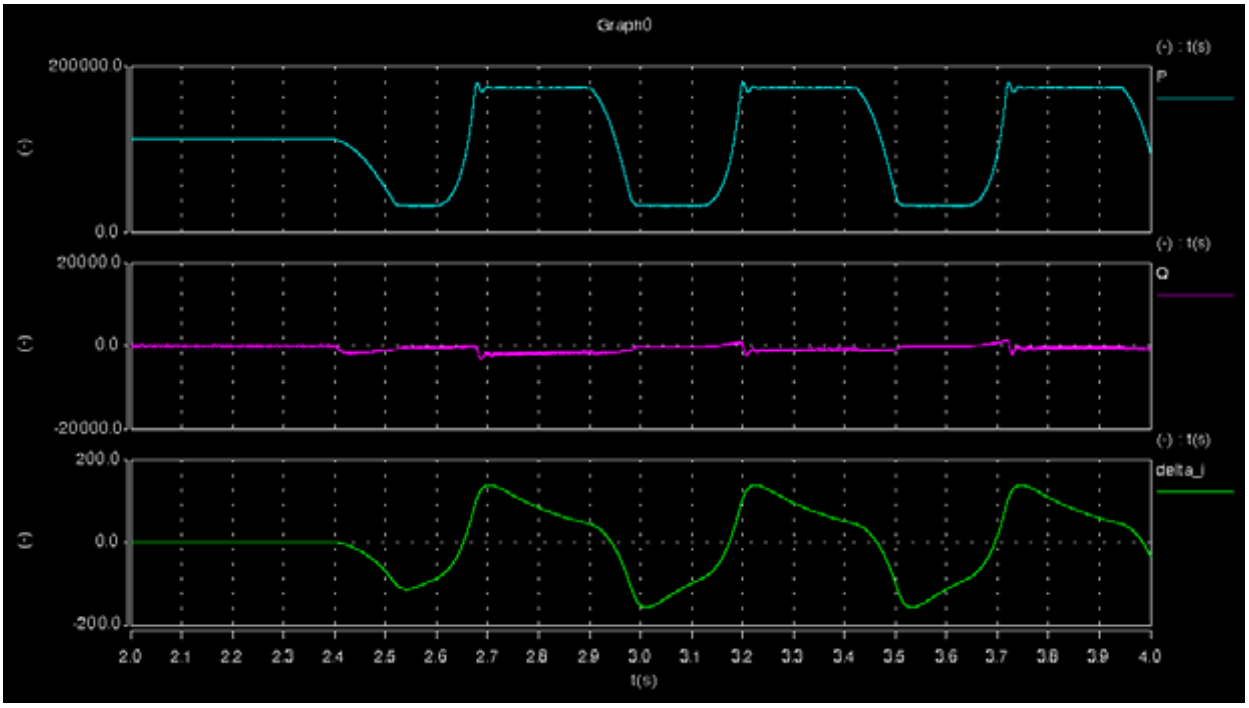


Figure 2-25(b). Simulation results with voltage feedback scheme (Qf=1.8, 100kW).

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

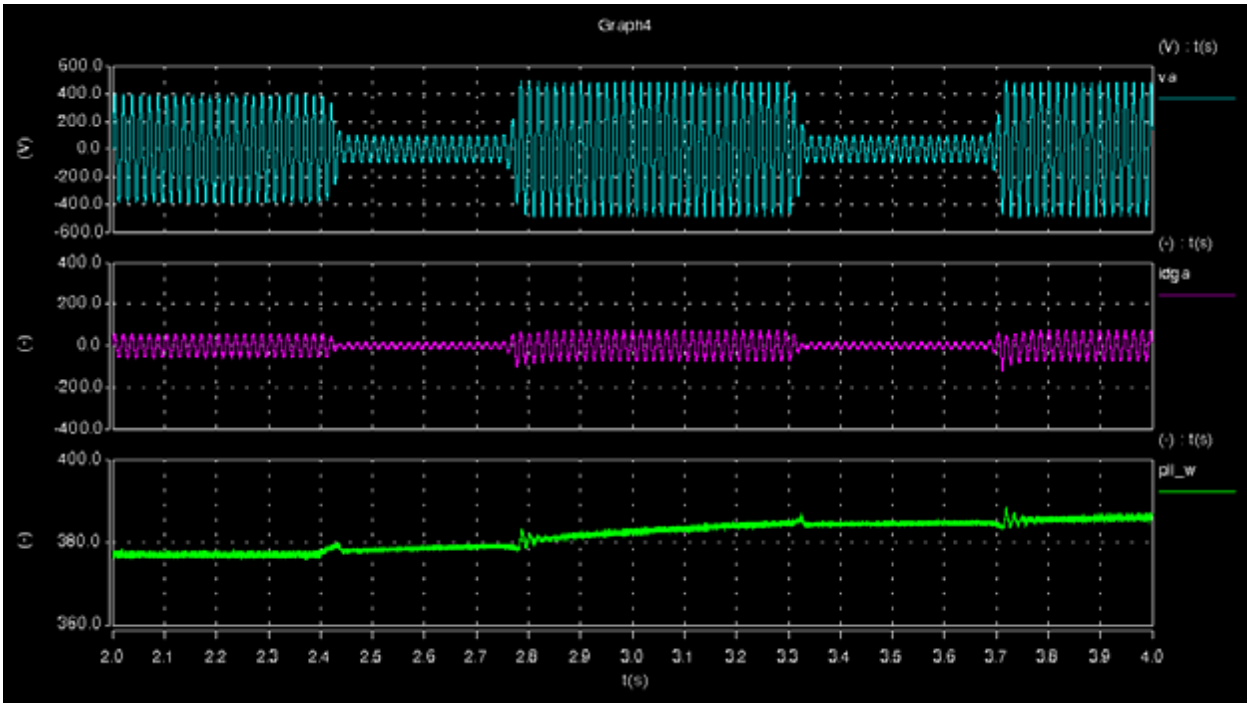


Figure 2-26 (a). Simulation results with voltage feedback scheme (Qf=1.8, 33kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

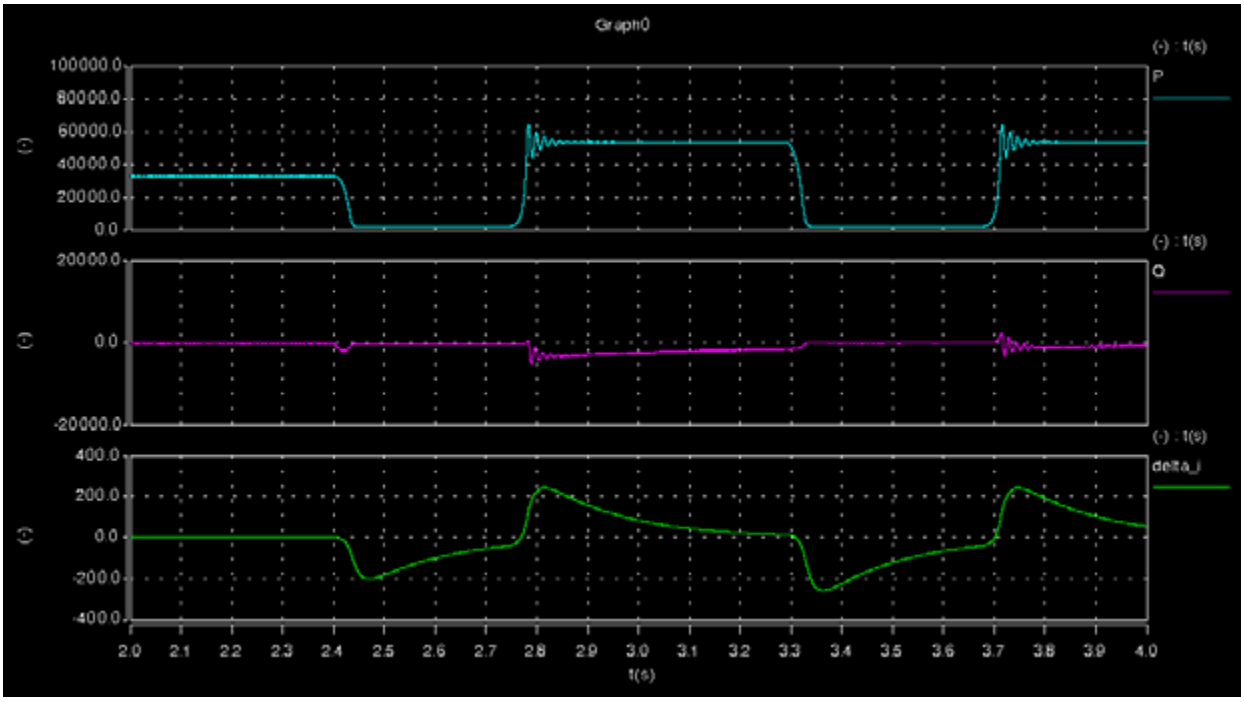


Figure 2-26(b). Simulation results with voltage feedback scheme (Qf=1.8, 33kW)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

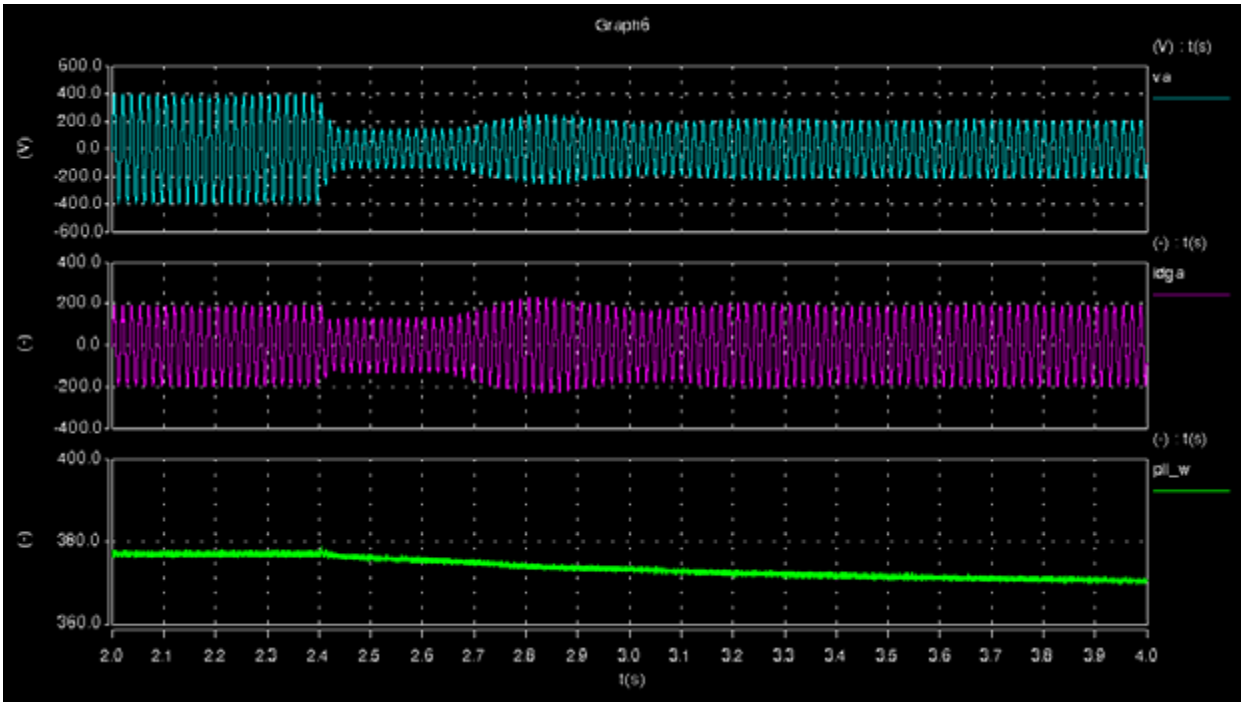


Figure 2-27(a). Simulation results with voltage feedback scheme (Qf=5, 100kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

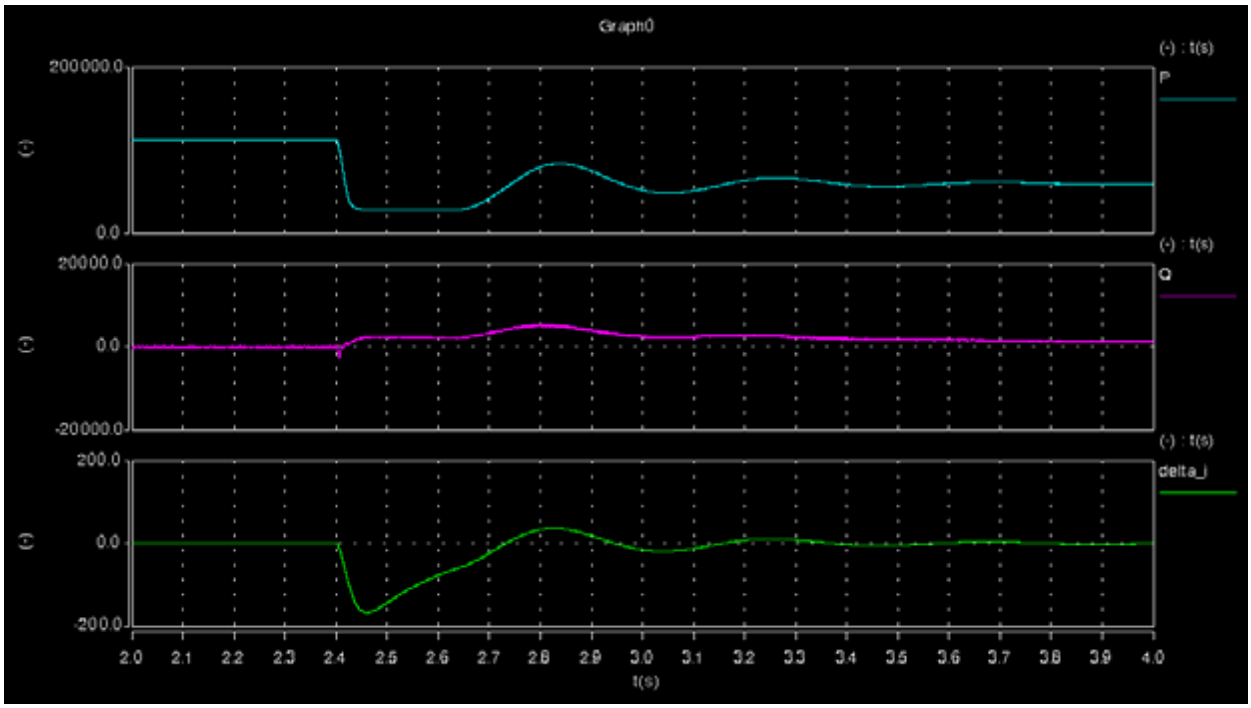


Figure 2-27(b). Simulation results with voltage feedback scheme (Qf=5, 100kW).

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

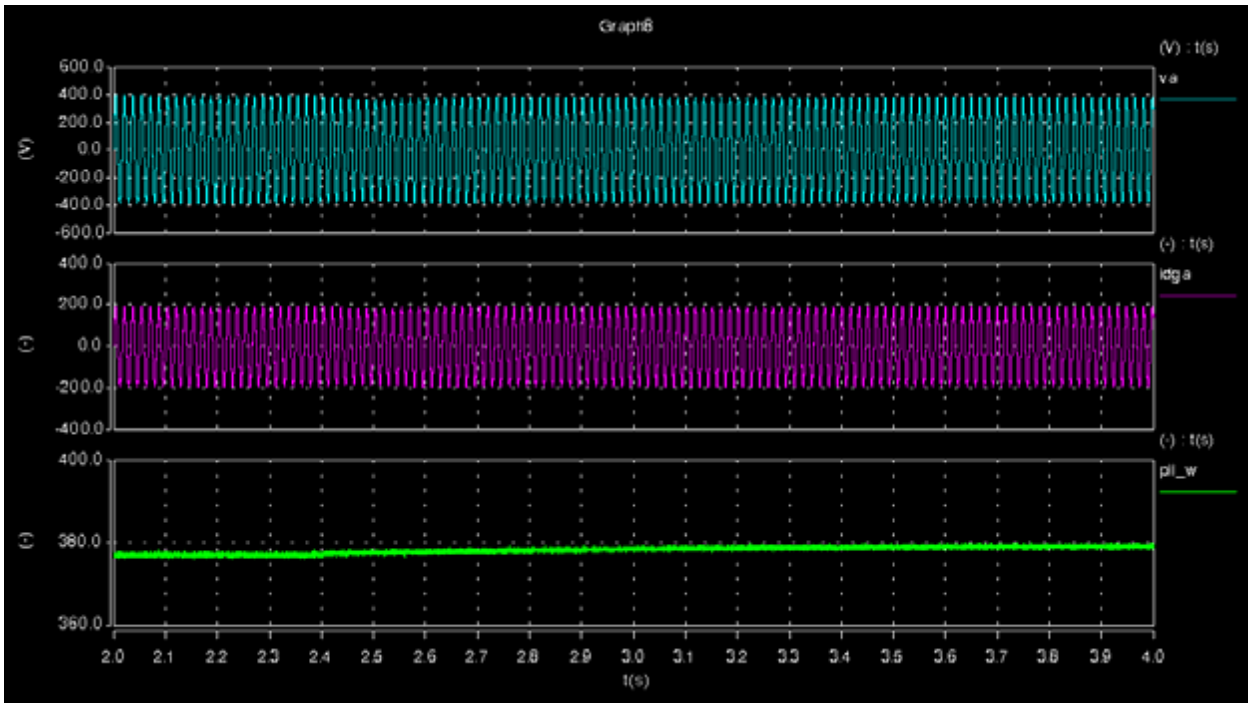


Figure 2-28(a). Simulation results with voltage feedback scheme (Qf=1.8, 100kW, gain halved)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

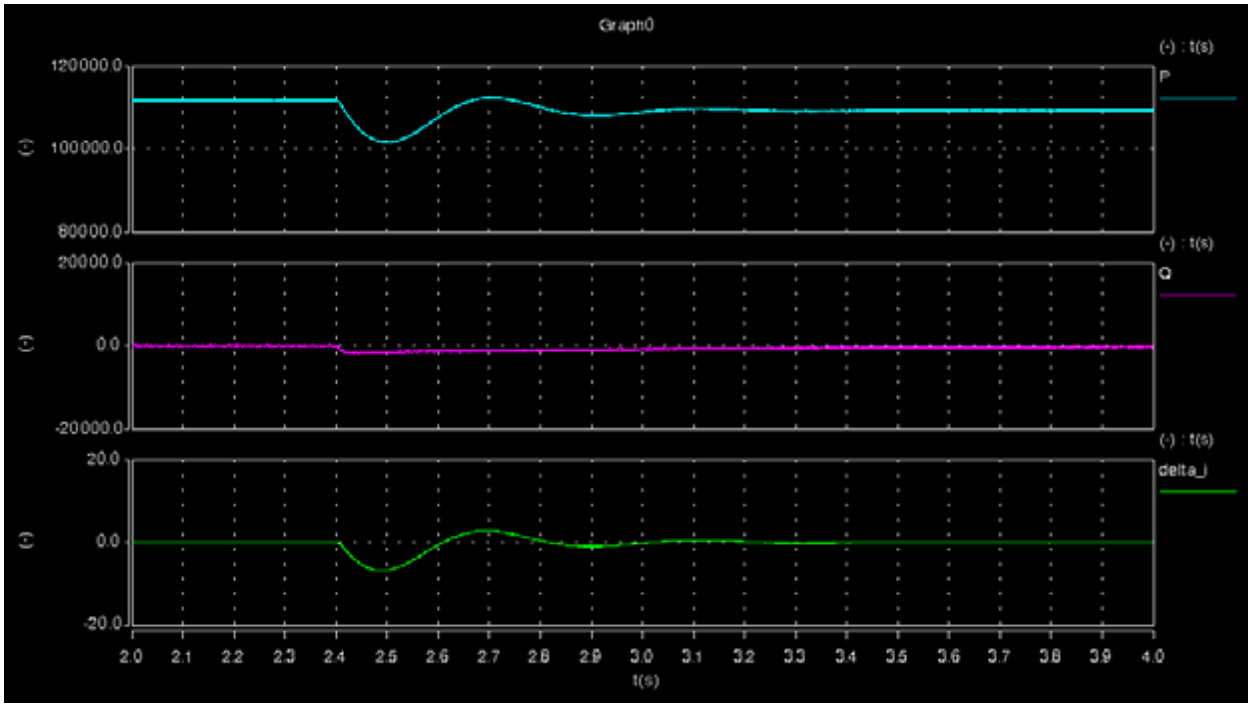


Figure 2-28(b). Simulation results with voltage feedback scheme (Qf=1.8, 100kW, gain halved)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

2.4.2 Performance Evaluation for Frequency Scheme

2.4.2.1. Frequency Scheme with 100kW, Qf=1.8. Similar cases are also simulated for the frequency scheme. Figure 2-29 shows that the AI control consistently drives the frequency away, while the voltage is also changed from its normal range. The noticeable difference between the voltage scheme and frequency is that the changes caused by the frequency scheme are monotonically increasing or decreasing in one direction [Figure 2-29(a) bottom trace], while the voltage scheme changes more dynamically. After further investigation, it is found that the stronger dynamics of the voltage scheme are due to two factors: 1)the current limit that results in saturation and oscillation, and 2) the voltage scheme is more sensitive to the gain – when the gain is low, the scheme won't be effective. When the gain is increased slightly, the scheme will result in strong dynamic and cause the saturation.

Given these features, the frequency scheme seems to be more desirable than the voltage scheme because, in practice, too much voltage variation (especially over voltage) may cause equipment damage even for a short period.

2.4.2.2 Frequency Scheme with 33kW, Qf=1.8. Figure 2-30 shows the case when the power is only at 33kW (33%). Similar to the voltage scheme, the dynamic is stronger at lower power level. The frequency [Figure 2-30(a) bottom trace] changes faster than the case with 100kW output.

2.4.2.3 Frequency Scheme with 100kW, Qf=5. Figure 2-31 shows the case that, similar to the voltage scheme n Figure 2-27, a larger load quality factor Qf will reduce the effectiveness of the anti-islanding control. The frequency [Figure 2-31(a) bottom trace] changes much slower than the case with Qf=1.8. Another observation is that the frequency decreases after islanding in this case, while it increases in the previous case. This is because of their different initial conditions at the time of grid disconnection (2.4s). The AI control destabilizes the system once islanded. The changing direction of the system variables depends on their initial conditions.

2.4.2.4 Frequency Scheme with 100kW, Qf=1.8, and Reduced Gain. Similar to the voltage scheme, when the gain in the feedback loop is reduced, the anti-islanding control becomes ineffective. Figure 2-32 shows the case that the gain is set to one-tenth of the previous design. It can be seen from Figure 2-32(a) that the voltage stays at a normal level. The frequency is oscillating but still close to the normal range, even though there is a small dynamic change in the current injection delta_i from the AI feedback loop. The loop is not strong enough to drive the voltage and frequency away within the 2-second requirement.

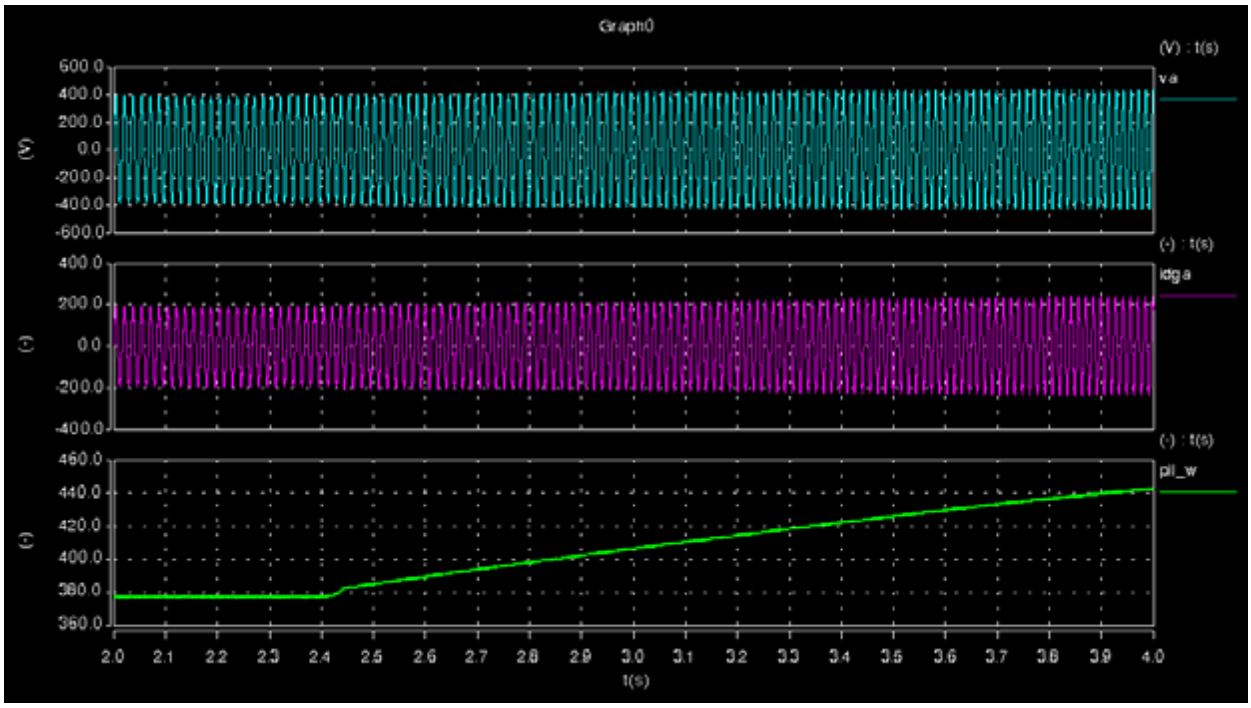


Figure 2-29(a). Simulation results with frequency feedback scheme (Qf=1.8, 100kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

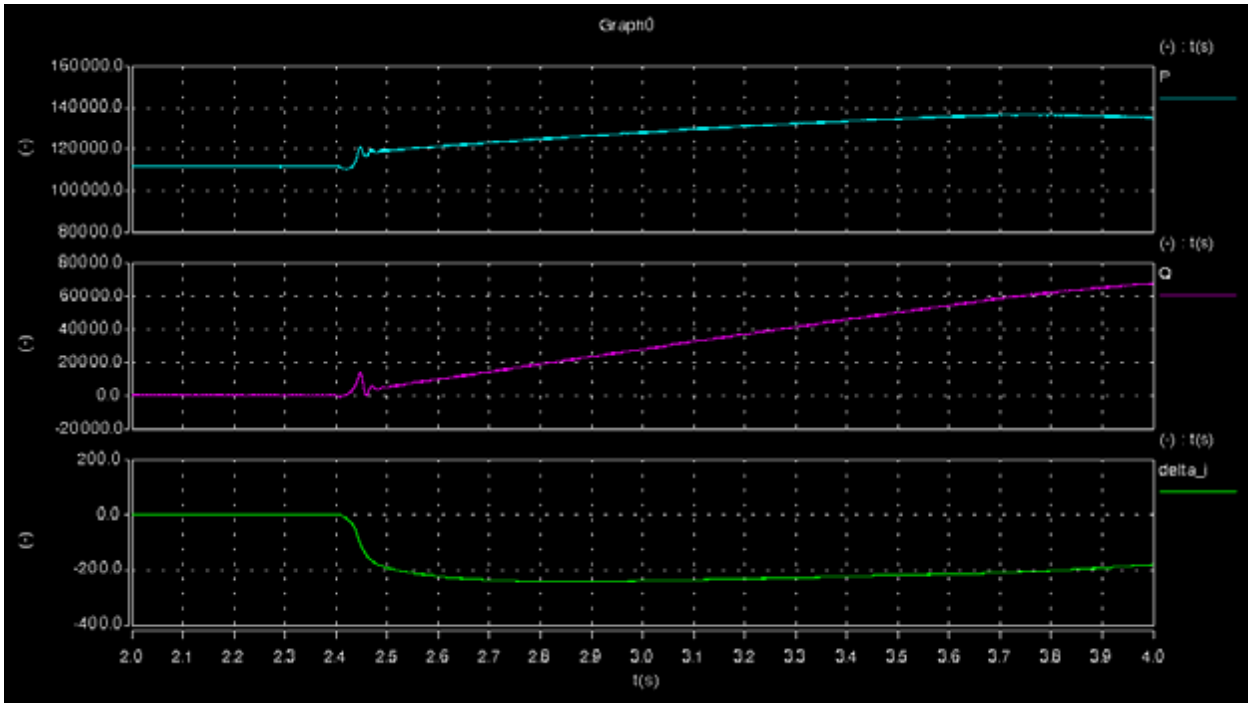


Figure 2-29(b). Simulation results with frequency feedback scheme (Qf=1.8, 100kW)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

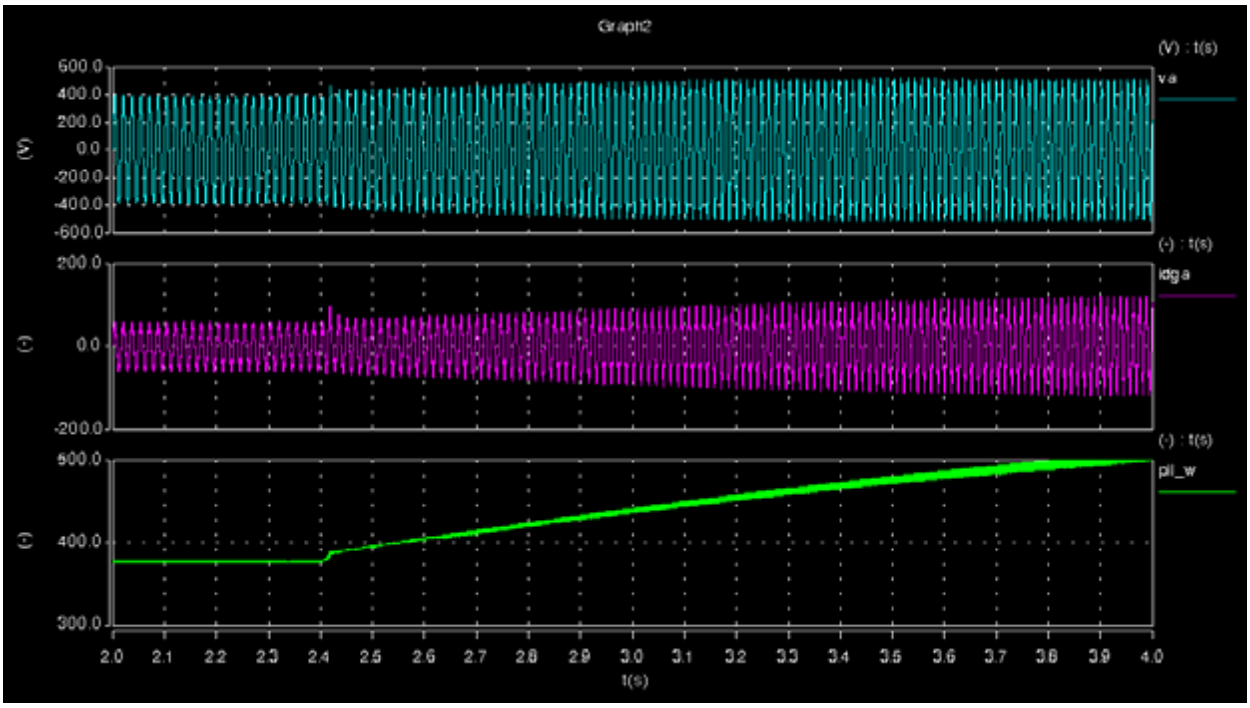


Figure 2-30(a). Simulation results with frequency feedback scheme (Qf=1.8, 33kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

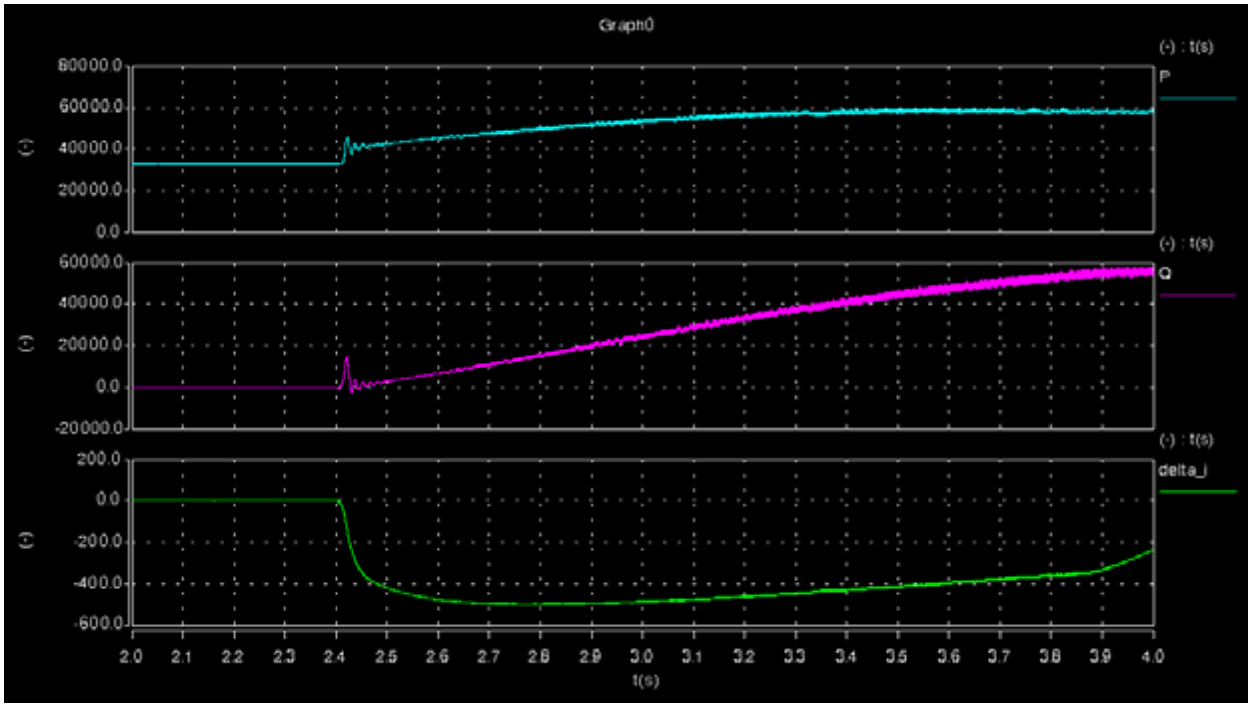


Figure 2-30(b). Simulation results with frequency feedback scheme (Qf=1.8, 33kW)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

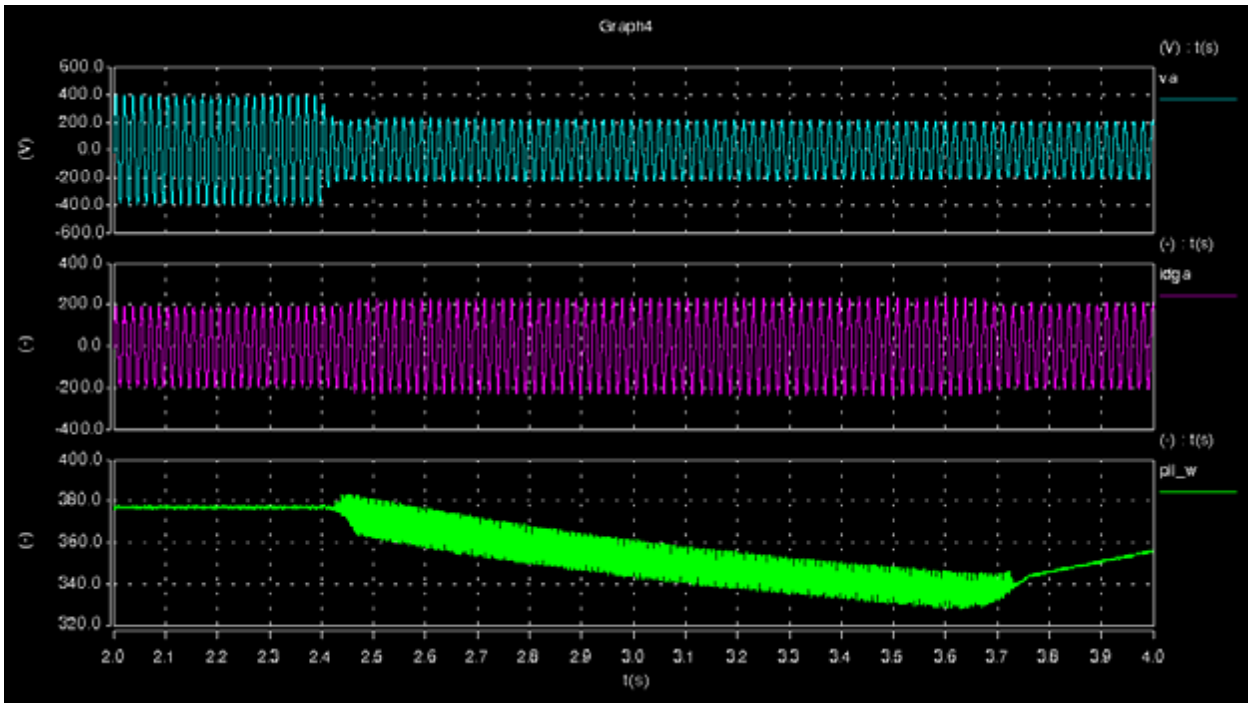


Figure 2-31(a). Simulation results with frequency feedback scheme (Qf=5, 100kW)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

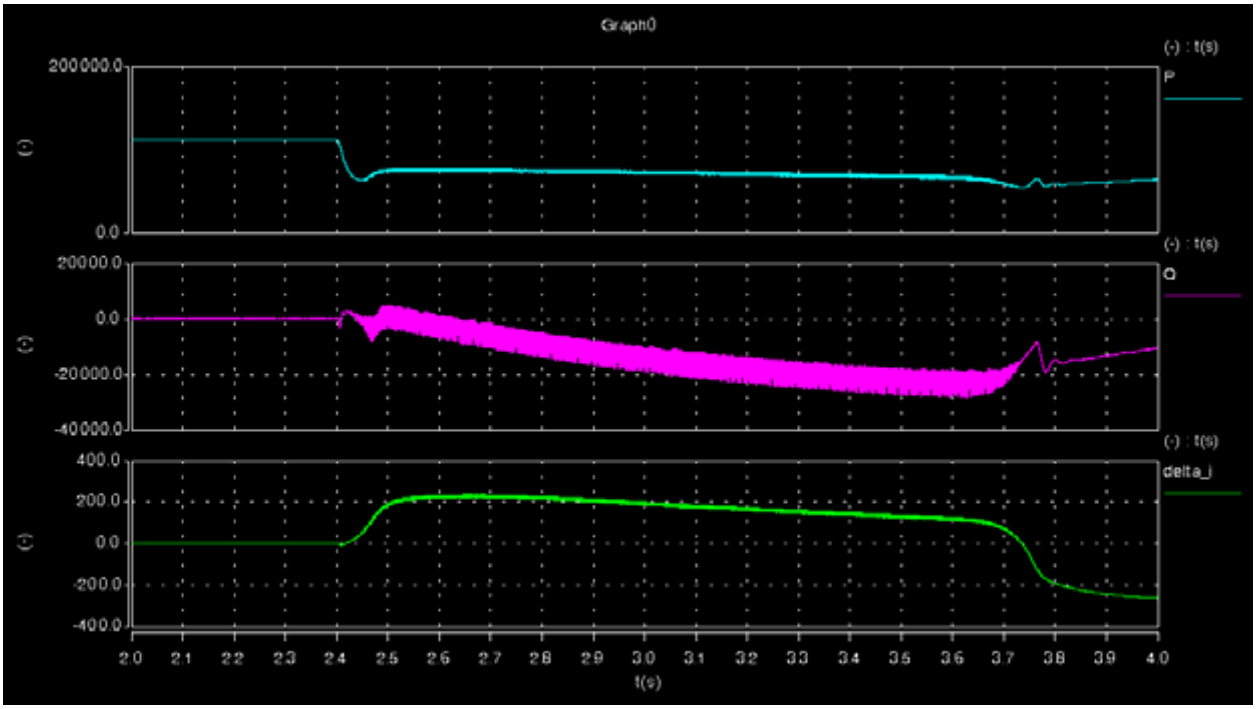


Figure 2-31(b). Simulation results with frequency feedback scheme (Qf=5, 100kW)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

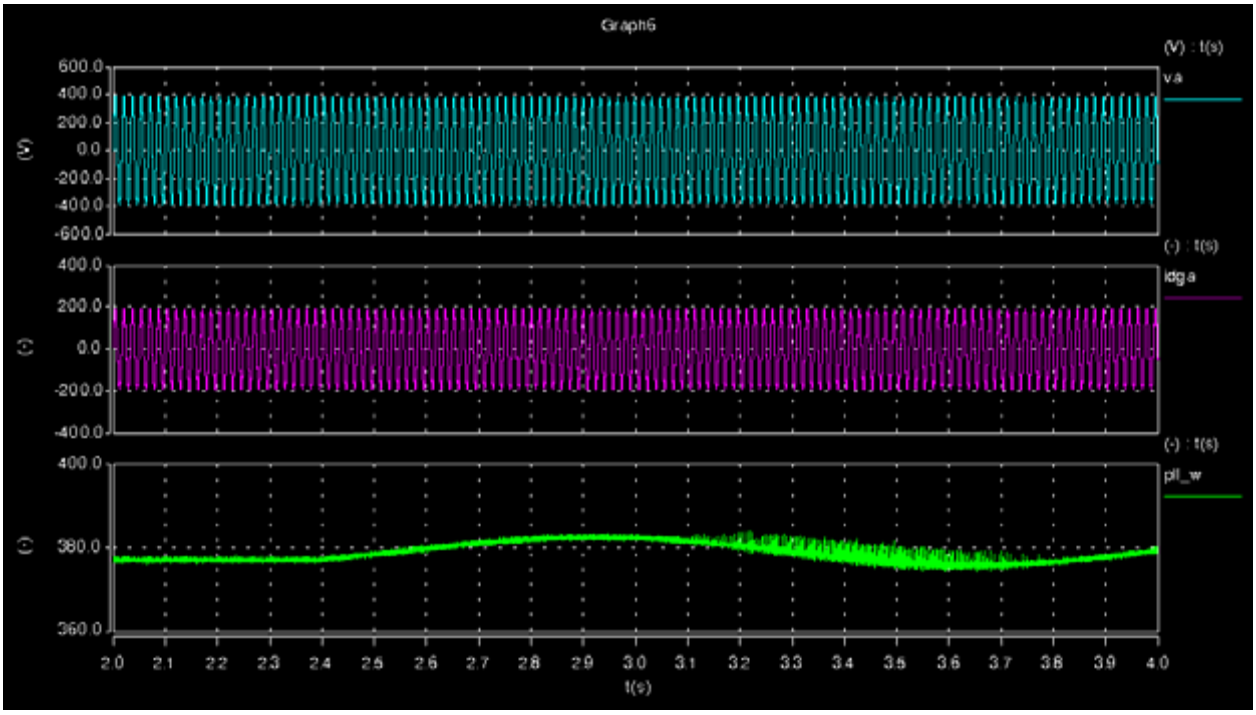


Figure 2-32(a). Simulation results with frequency feedback scheme 1 (Qf=1.8, 100kW, gain 1/10)

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

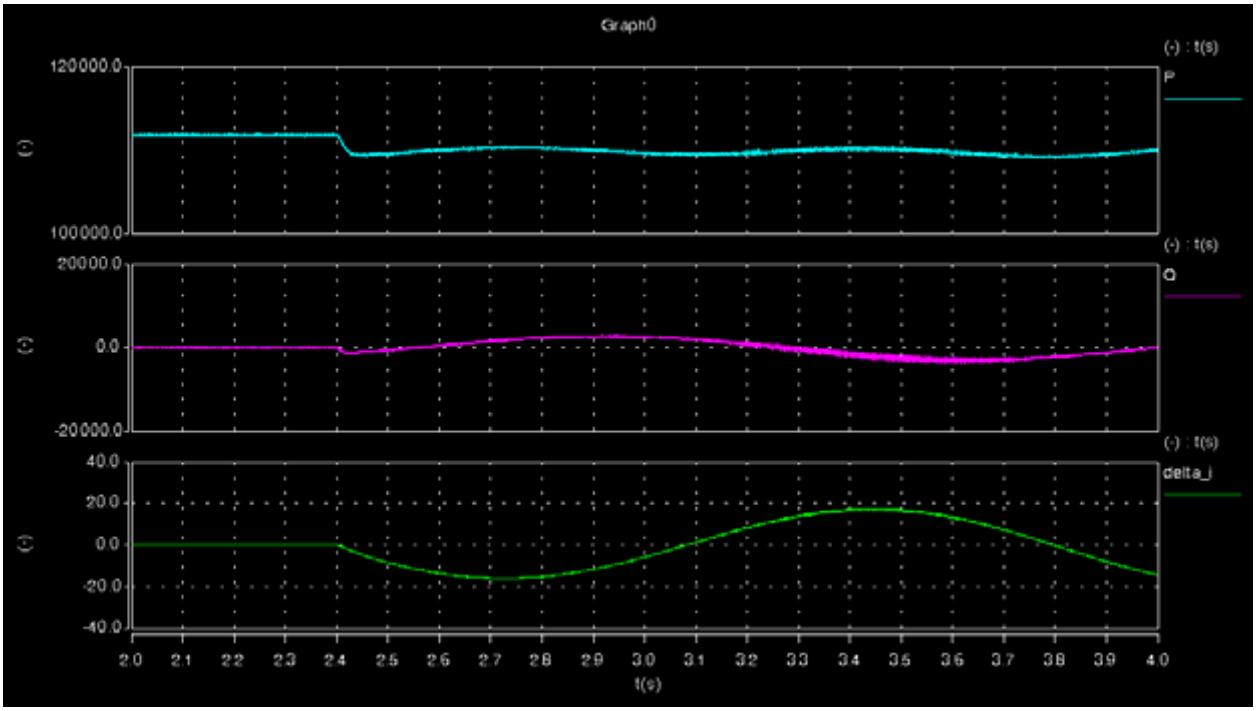


Figure 2-32(b) Simulation results with frequency feedback scheme 1 (Qf=1.8, 100kW, gain 1/10)

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: Δi from the AI feedback loop (A))

2.4.3 Performance Evaluation When Grid Connected

The previous section shows a range of islanding cases. In this section, the impact of the anti-islanding schemes on the inverter performance during grid-connected operation will be evaluated. The performance includes power quality, robustness to grid disturbances, and stability.

2.4.3.1 Power Quality. Power quality can be referred by various aspects, such as harmonics (THD), flicker, etc. In this study, only THD is used as the power quality performance index. THD is measured when the inverter system operates in steady state at different power levels. At each power level, three cases are simulated, one is without AI enabled (NoAI), one is with the voltage scheme (AI-V), and one is with the frequency scheme (AI-F). Table 2-2 shows the recorded THD for all cases. Here, the simulation system is greatly simplified from the real world in that the grid is represented by a voltage source behind an impedance (5%). Therefore, there are no ambient harmonics. Besides, all parameters, including load, are symmetric and balanced. However, even if it is simplified, it is still useful for comparison purposes because all cases are with the same grid and load conditions.

Table 2-2 shows no noticeable difference among the cases without AI (No AI), with the voltage scheme (AI-V), and with the frequency scheme (AI-F). In some cases, the results with AI look better than without AI, but it is so small that it can be considered as numerically at no difference. If there is a reason for the better THD with AI, the reason could be that the AI feedback injection acts like a random noise that results in a better overall harmonics spectrum. This, however, needs further proof in theory or in experiment.

Table 2-2 THD Comparison.

AI	Power (kW)	THD-v	THD-i
No AI	100	0.096%	1.769%
AI-V	100	0.099%	1.752%
AI-F	100	0.089%	1.742%
No AI	66	0.117%	2.918%
AI-V	66	0.132%	2.923%
AI-F	66	0.104%	2.900%
No AI	33	0.367%	5.809%
AI-V	33	0.388%	5.862%
AI-F	33	0.355%	5.778%

Comparing the power quality performance of the proposed schemes with other schemes, such as Sandia Frequency Scheme (SFS) (waveform chopping at zero crossing), the proposed schemes practically have no negative impact on THD performance. This is obviously a significant advantage over many other schemes.

Figures 2-33 and 2-34 show the current waveforms with different schemes under 100%, and 33% power levels, respectively.

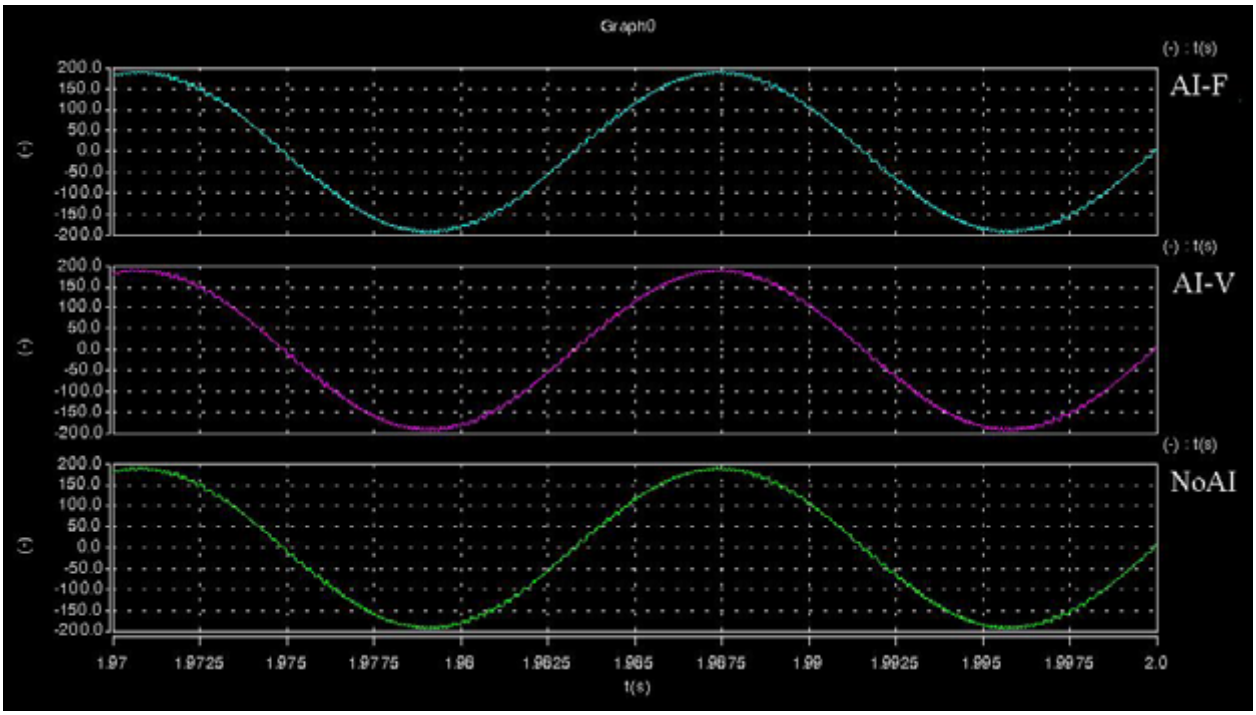


Figure 2-33(a)- Waveforms with 100kW Inverter output

(a) Inverter output current

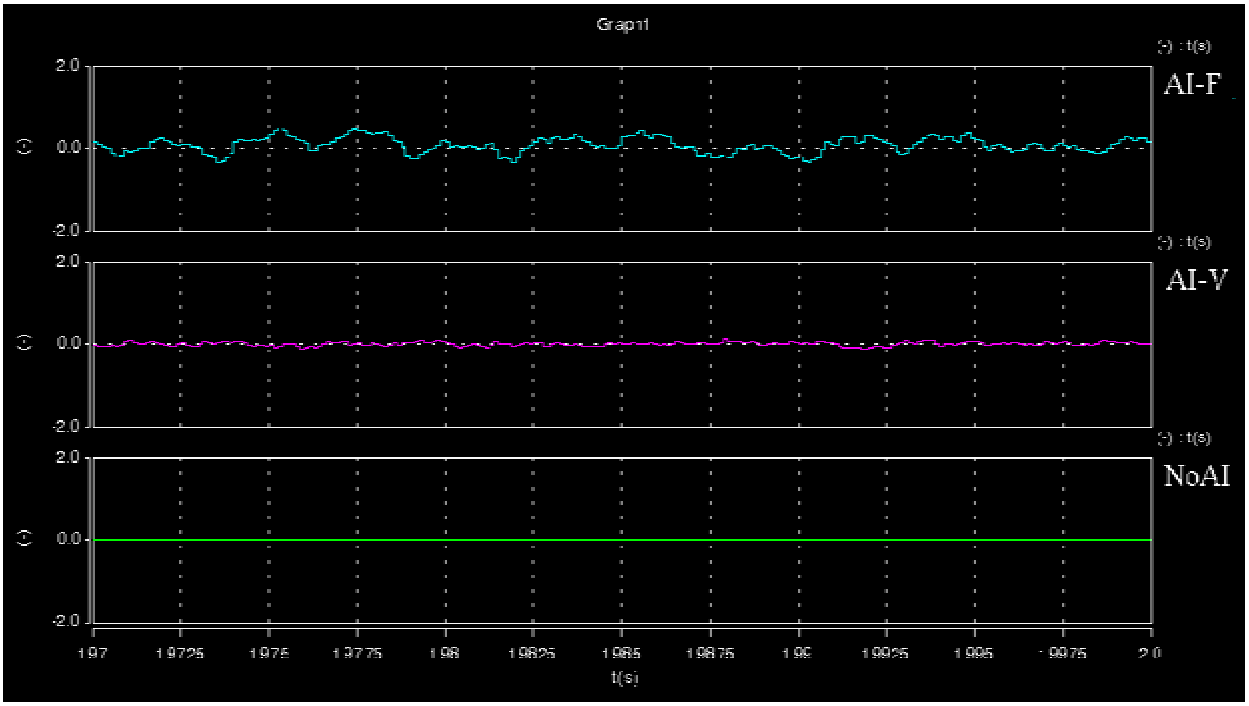


Figure 2-33(b) Waveforms with 100kW Inverter output

(b) Δi from the AI feedback loop

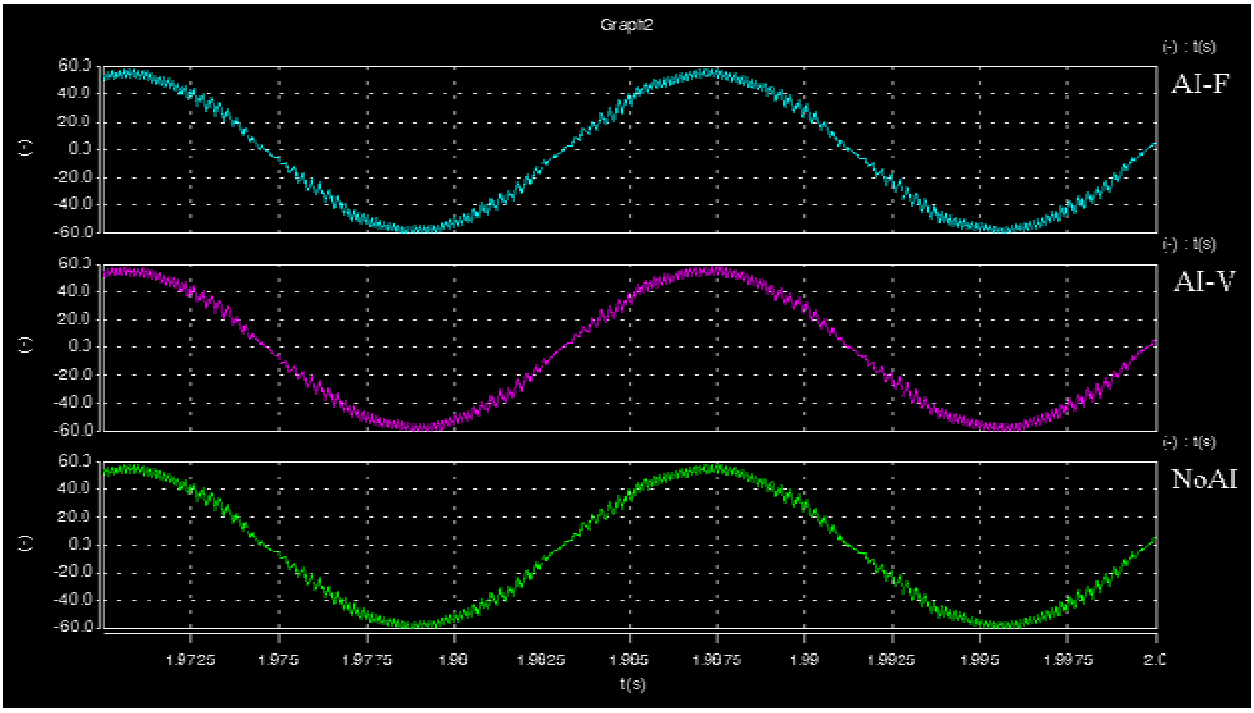


Figure 2-34(a) Waveforms with 33kW Inverter output

(a) Inverter output current

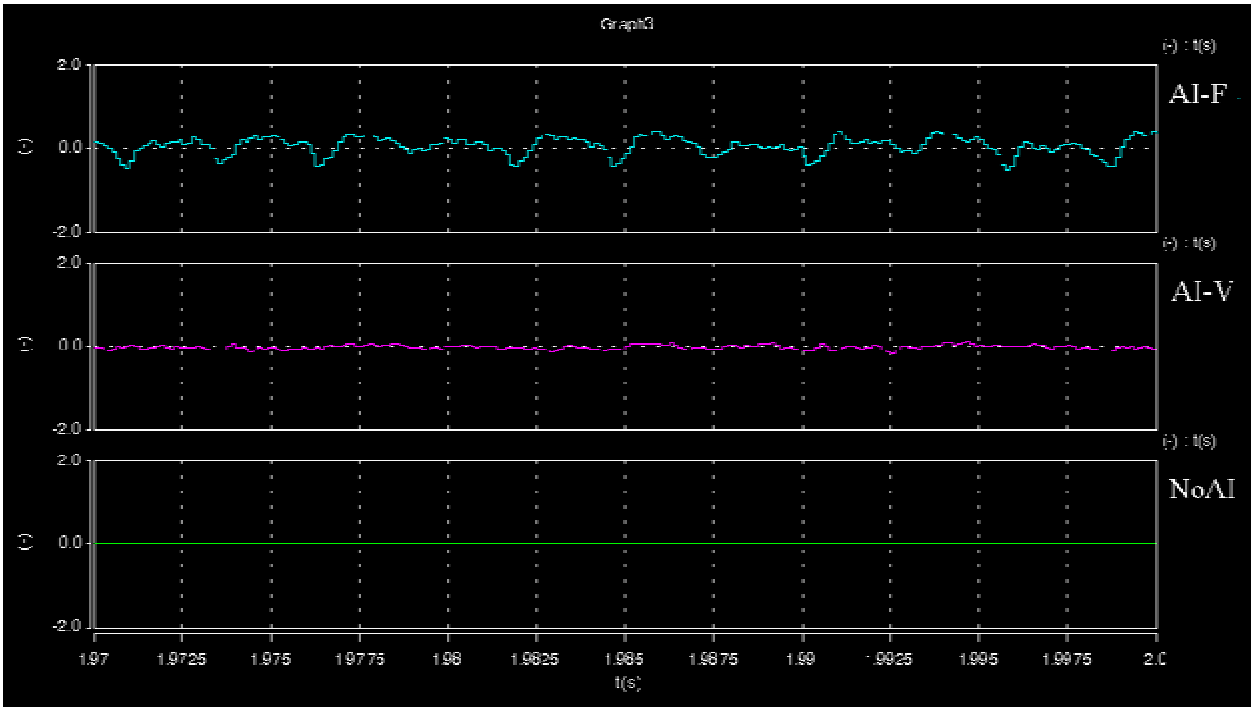


Figure 2-34(b) Waveforms with 33kW Inverter output

(b) Δi from the AI feedback loop

2.4.3.2 Grid Disturbances. Another performance index for evaluating an anti-islanding scheme is robustness for grid disturbances. There are two dimensions to the robustness issue: 1) the anti-islanding scheme should not adversely affect inverter performance during the grid disturbances, and 2) the scheme should not cause false trips for grid disturbances that do not constitute islanding. In the following simulations, the schemes are evaluated under two typical grid disturbances, low-voltage-ride-through event and power step transient. The performance is compared against the case without anti-islanding control.

It is demonstrated that the proposed schemes are robust and resilient to grid disturbances for the situations tested. However, it is not a very complete evaluation. To further validate the performance, a more comprehensive evaluation would be in order, for example, the impact on dynamic stability.

Low-Voltage-Ride-Through (LVRT)

Due to its increasing penetration, distributed generation is becoming an integral part of the overall power generation in the grid. As a result, the grid is becoming more reliant on the DGs, and DG behaviors will have a more significant impact on the grid. Therefore, in some standards, there is a requirement that the DG must stay on the grid when there is a large abnormal grid event. The event may cause the voltage to be lower than the normal ranges for an extended period. This is very difficult for any passive schemes to differentiate the disturbance event from the actual islanding because the schemes will only see and trip on the under voltage condition.

The evaluation conducted here is to demonstrate that the proposed schemes will not cause adverse impact on the low-voltage-ride-through event. Yet, when actual islanding event occurs, the schemes will differentiate the islanding event from the low-voltage-ride-through event.

Figure 2-35 shows the base case (no AI enabled) of the low-voltage-ride-through event. Figures 2-36 and 2-37 show the low-voltage-ride-through event with the voltage and the frequency schemes enabled, respectively. It can be seen that, the voltage scheme responded dynamically to some extent, comparing Figure 2-35(a) and Figure 2-36(a). However, its response does not cause any perceivable issue. In essence, the frequency scheme has no impact at all, comparing Figure 2-35(a) and Figure 2-37(a).

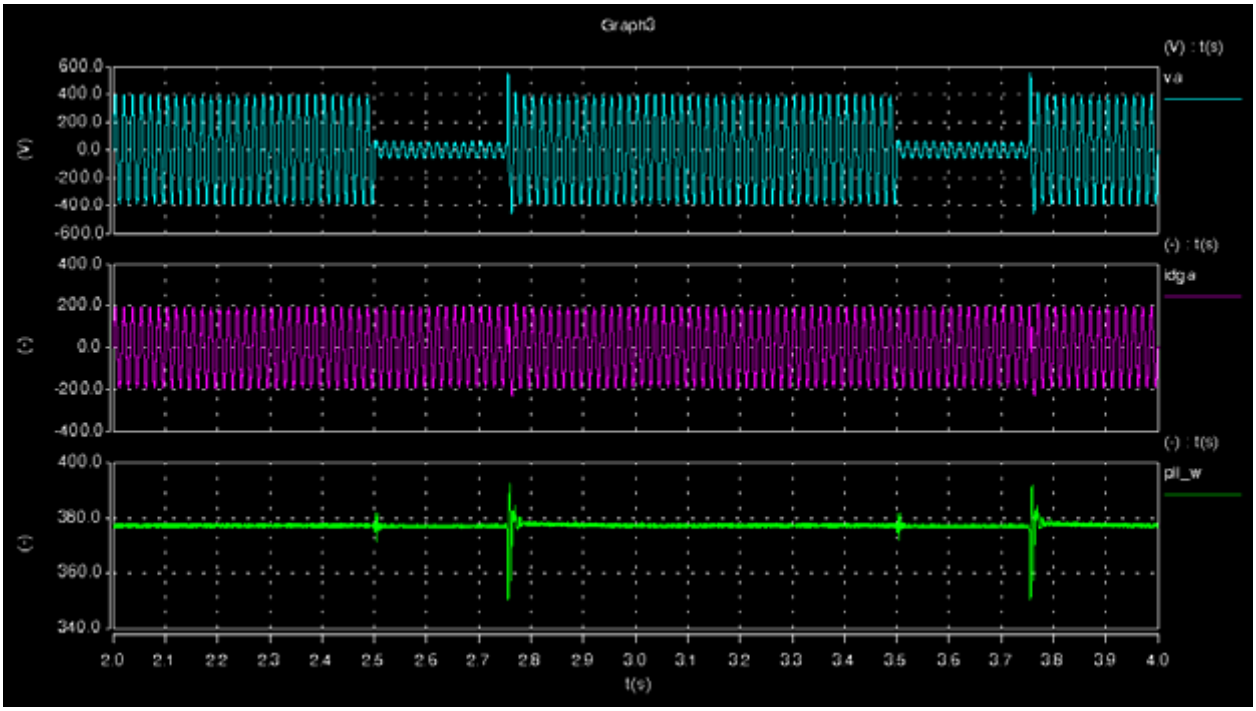


Figure 2-35(a) Inverter low-voltage-ride-through waveforms without AI

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

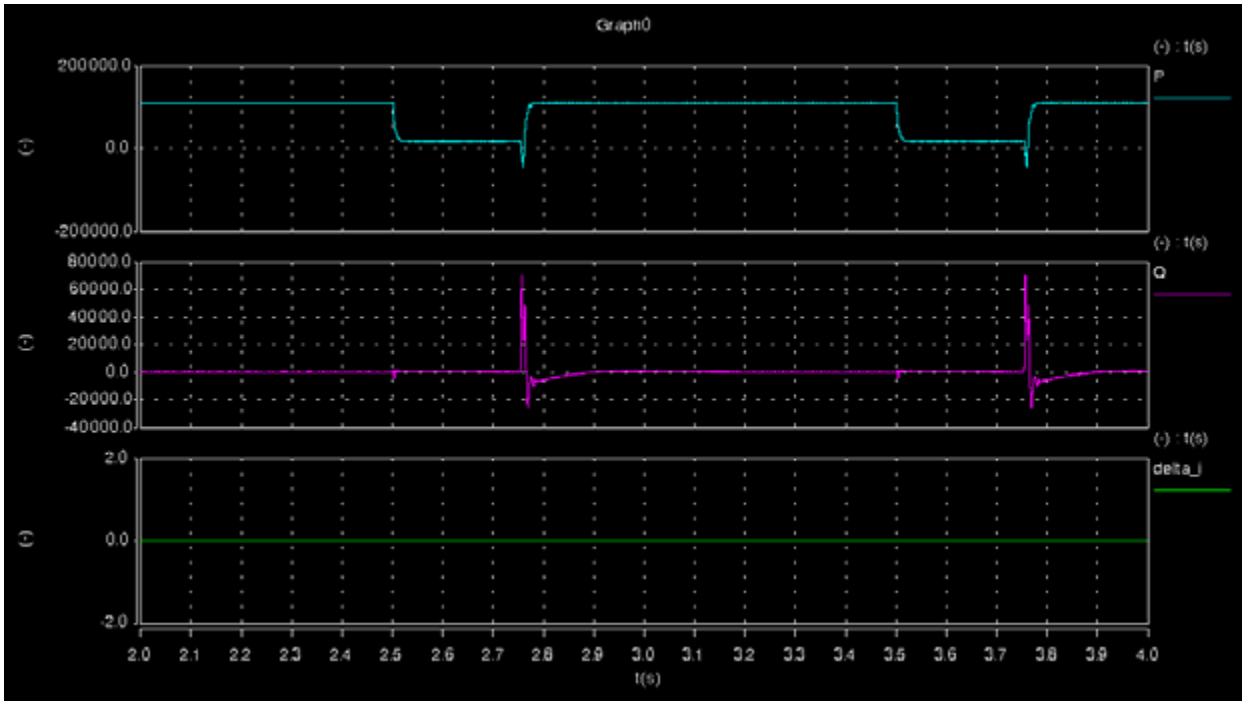


Figure 2-35(b) Inverter low-voltage-ride-through waveforms without AI

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: delta_i from the AI feedback loop (A)).

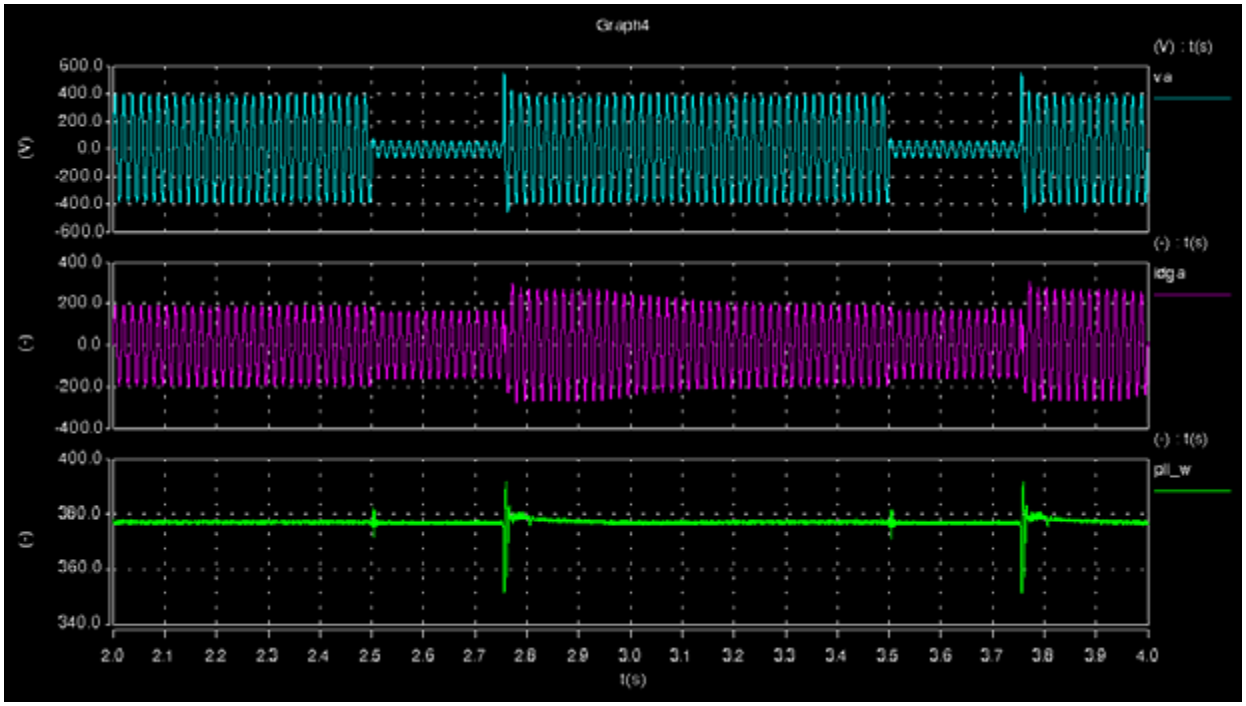


Figure 2-36(a) Inverter low-voltage-ride-through waveforms with voltage scheme

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s)).

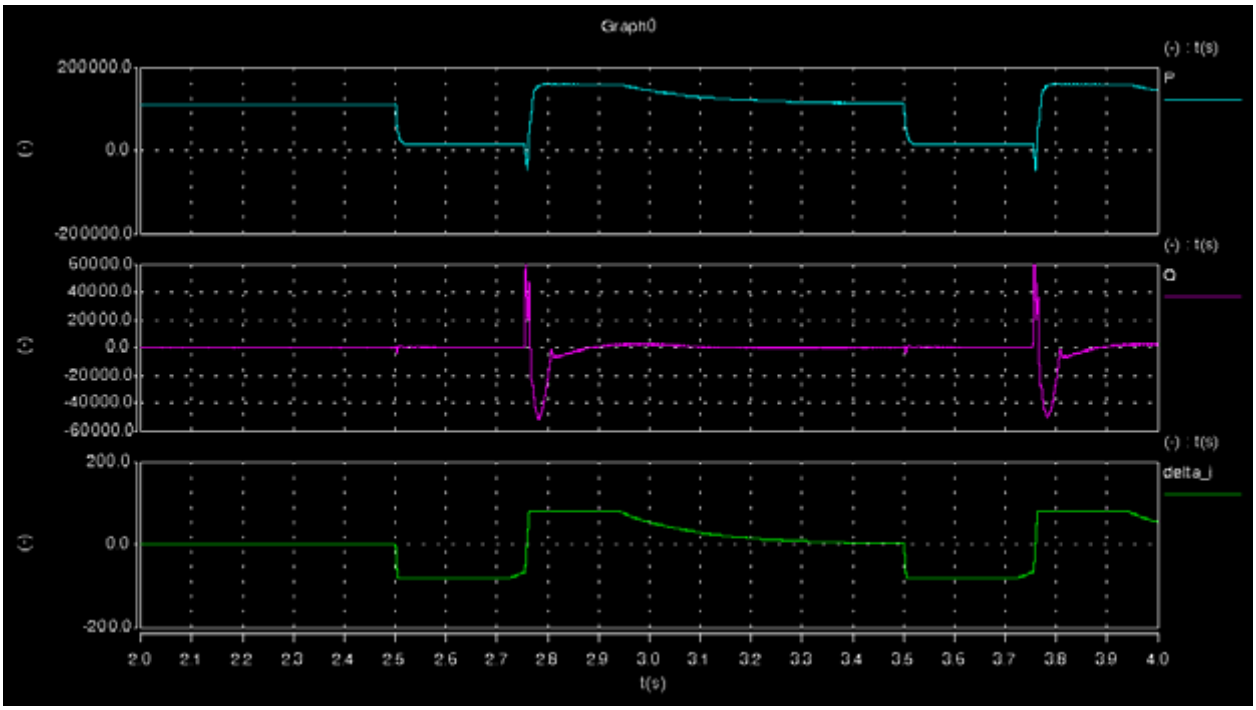


Figure 2-36(b) Inverter low-voltage-ride-through waveforms with voltage scheme

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: delta_i from the AI feedback loop (A)).

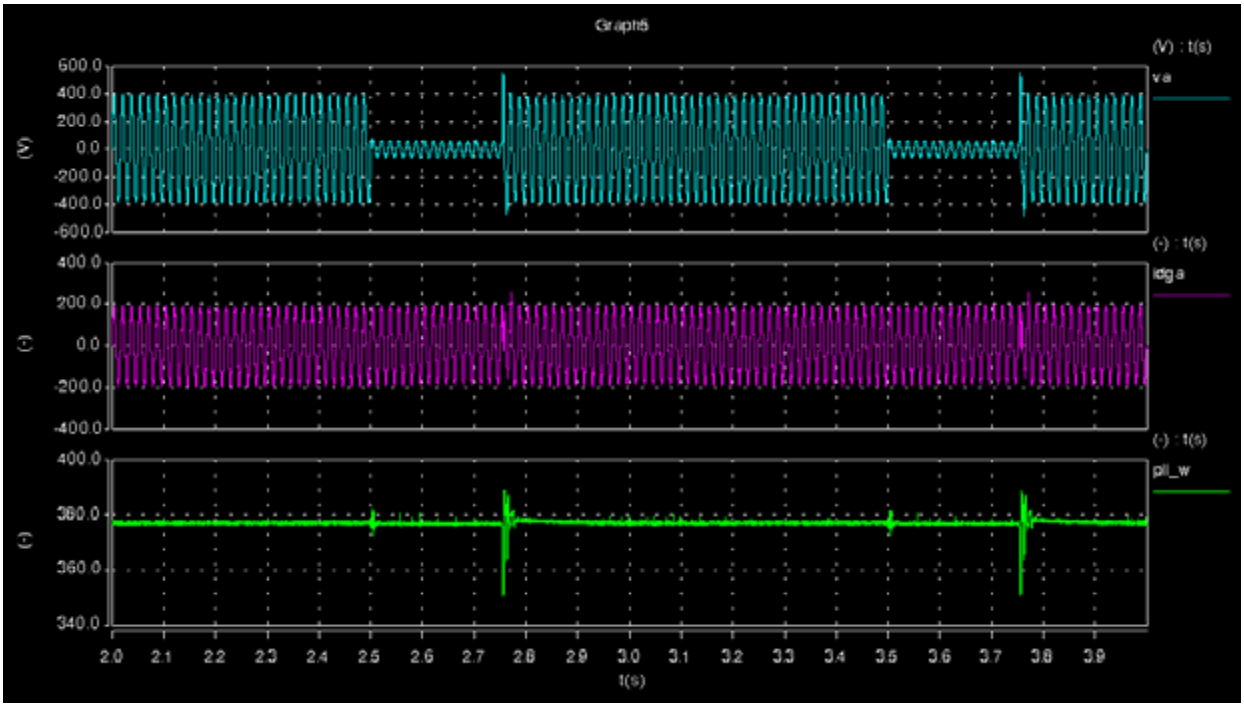


Figure 2-37(a) Inverter low-voltage-ride-through waveform with frequency scheme

(a) (top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

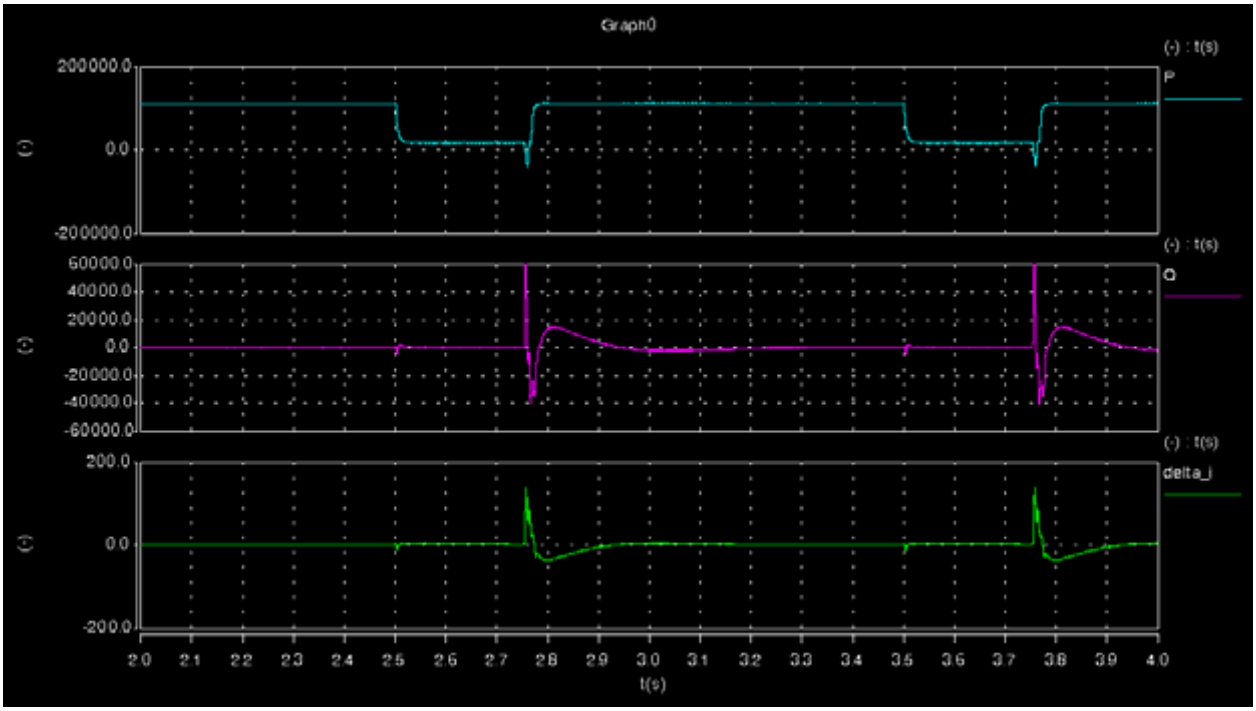


Figure 2-37(b) Inverter low-voltage-ride-through waveform with frequency scheme

(b) (top: inverter output active power (W); middle: inverter output reactive power (Var); bottom: delta_i from the AI feedback loop (A))

For further comparison, Figure 2-38 shows both LVRT event and islanding event in one simulation, under the condition of without AI control and with AI control (frequency scheme), respectively. The system is undertaking a LVRT event from 1.6s to 3.0s. Both cases (with and without AI) have not much difference in dynamics. This means, the AI control does not cause any aggravation of the under-voltage event. At 3.1s, the grid is disconnected to cause an islanding event. The case without AI cannot detect the islanding event (the power mismatch is near zero), while the case with the AI control can successfully detect it by driving the frequency away, as shown in Figure 2-38(b).

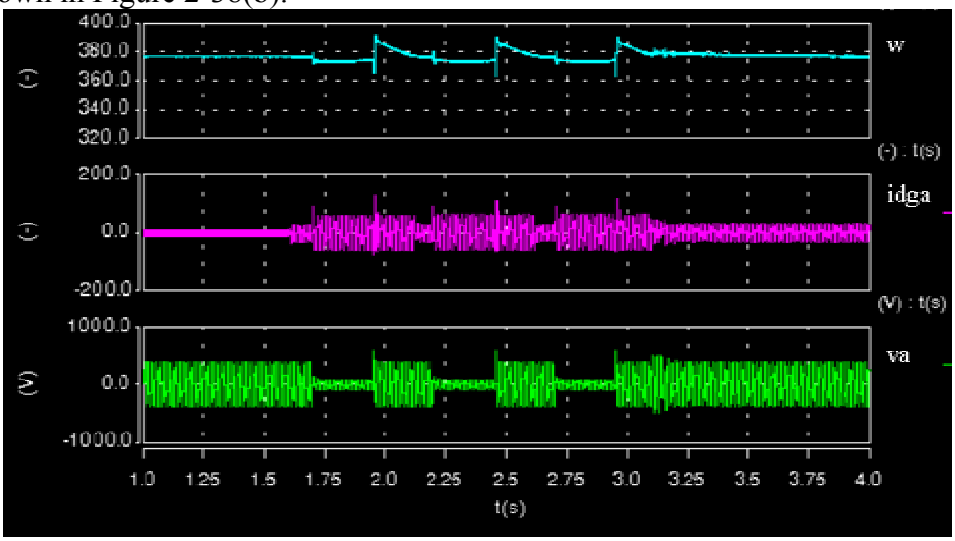


Figure 2-38(a) Comparison between with and without AI under LVRT and islanding events

(a) Without AI control

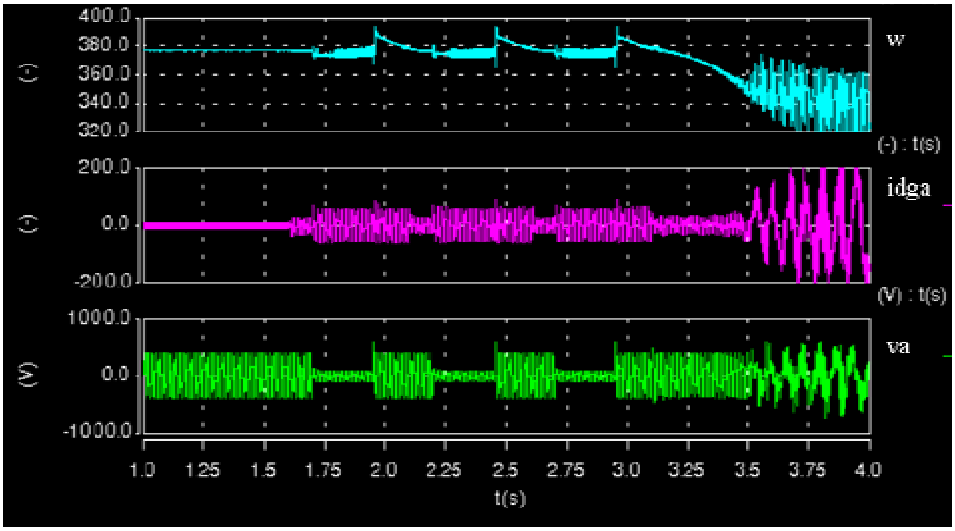


Figure 2-38(b) Comparison between with and without AI under LVRT and islanding events

(b) With AI control (Frequency scheme)

The low-voltage-ride-through requirement indicates that simple application of under- and over-voltage tripping may not result in adequate discrimination between islanding and grid disturbances. This further implies that under/over voltage is not appropriate for islanding protection. Dedicated anti-islanding protection is needed, such as the GE AI schemes.

Power Step

Another disturbance event is the DG-output-power-step-transient response. The inverter current reference steps from 25% to 100% of the rated. This step change may cause voltage disturbance due to finite grid impedance. The simulation results indicate that the event is even more benign than the low–voltage-ride-through event with the proposed schemes. Figures 2-39 through 2-41 show the results without AI, with the voltage scheme, and with the frequency scheme, respectively. Results showed virtually no difference..

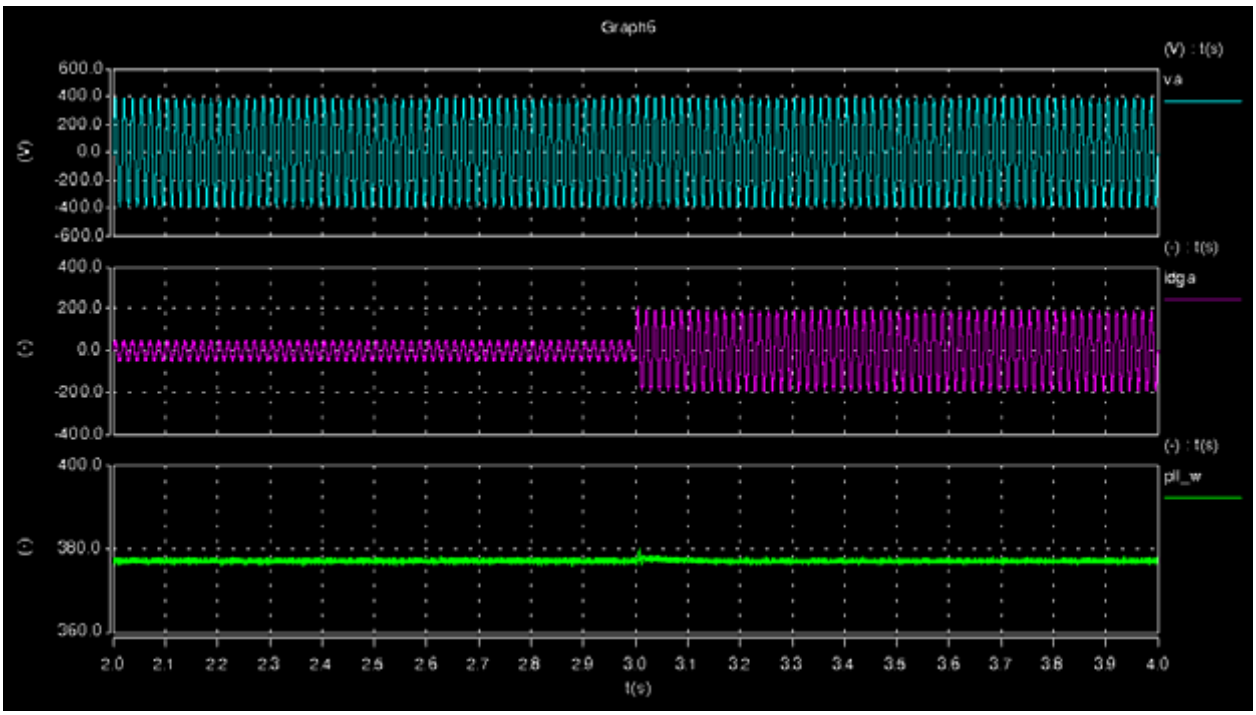


Figure 2-39. Power step transient response without AI

(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

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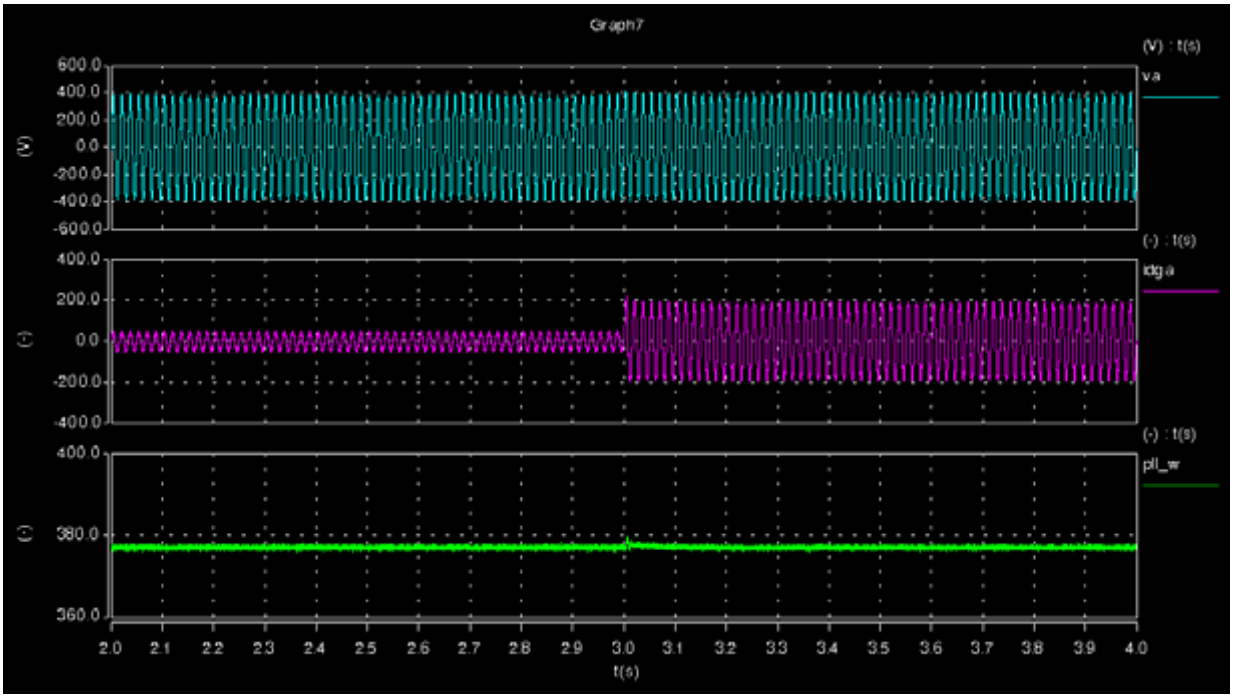


Figure 2-40. Power step transient response with voltage scheme

(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))**.**

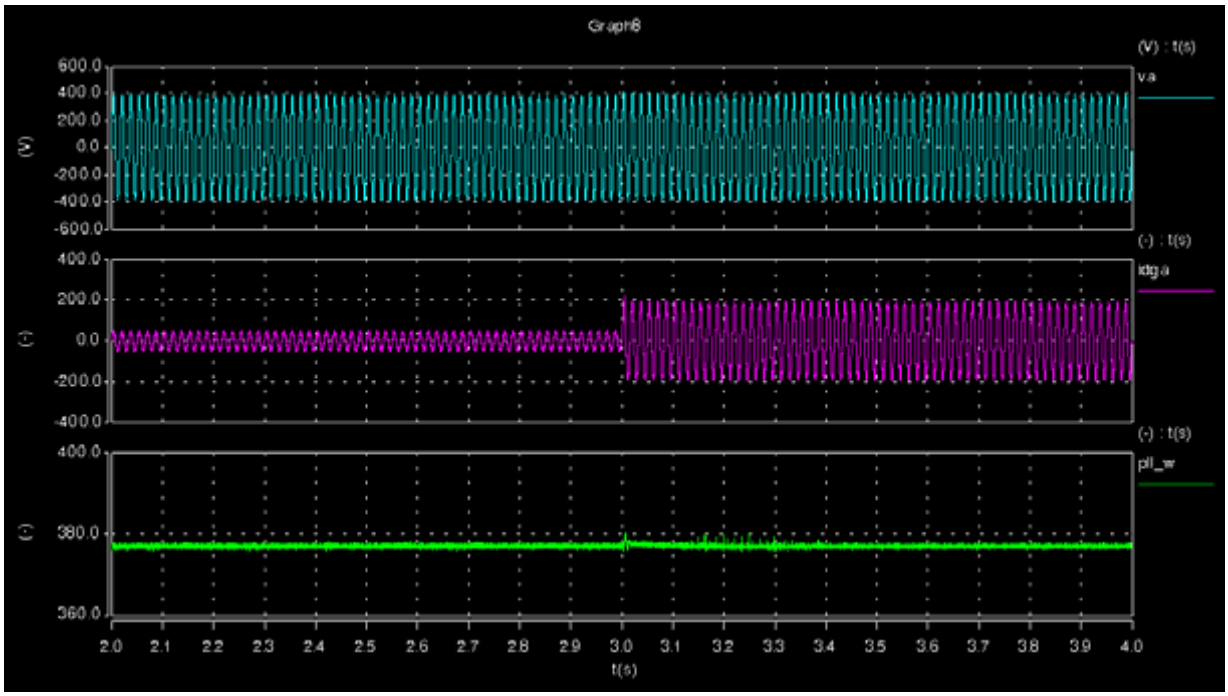


Figure 2-41. Power step transient response with frequency scheme

(top: inverter output voltage (V); middle: inverter output current (A); bottom: inverter measured frequency (rad/s))

2.4.3.3 Stability.There have been concerns over the impact on stability caused by positive feedback schemes, since the grid is not an infinite source. With a finite grid impedance, the voltage at the DG terminal is not an ideal voltage source. Conceptually, if the positive feedback is strong enough, the inverter could destabilize the local system, including the inverter and the load. Therefore, the stability bounds of the positive feedback schemes have always been in question.

Here only local stability is investigated. The local system includes the inverter, the RLC load, and the simplified grid. Two factors will affect the stability. One is the positive feedback loop gain. The other is the grid impedance. Here, assuming the positive feedback loop gain has been optimized for anti-islanding control. Only grid impedance variation is considered.

Usually, the grid impedance looking into the point of common coupling (PCC) (the grid impedance includes the distribution transformer), is about 10% or less, on the rated power base of the DG. In some very weak systems, the impedance could be as great as 20%, which is about the practical bound. However, in some extreme cases, the equivalent grid impedance could be unusually high. Figure 2-42 shows one application scenario of a remote plant (11MVA load) supplied by on-site DG (10MVA) for base load. Due to reliability and other reasons, the plant may want to connect to the grid, but there is no existing service connection for the plant. Then, a new load service is provided for the plant, but, for economic reasons, the plant only contracts for a connection capacity equal to the difference between the load and the on-side DG capacity. In this case, the utility might install a 1 MVA distribution transformer. The grid impedance, including the transformer impedance, secondary service cable, and the impedance of the primary distribution feeder, might be 10% on the 1MVA base of the interconnection capacity. Then the equivalent grid impedance looking from the plant is 100% on the DGs 10MVA rating base. This is an extreme, but practical case. However, it illustrates that the grid impedance could be very high, depending on application.

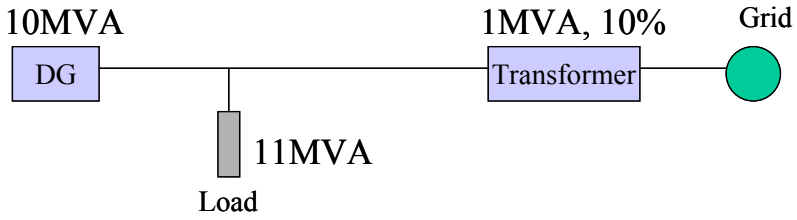


Figure 2-42. Application scenario with 100% grid impedance

The case with 100% grid impedance has been simulated, as shown in Figure 2-43 and Figure 2-44 for the voltage and frequency schemes, respectively. The anti-islanding control is enabled at 1.4s for both cases, while the grid is connected. It can be seen that the system is being destabilized by the AI control with growing oscillations of voltage and frequency.

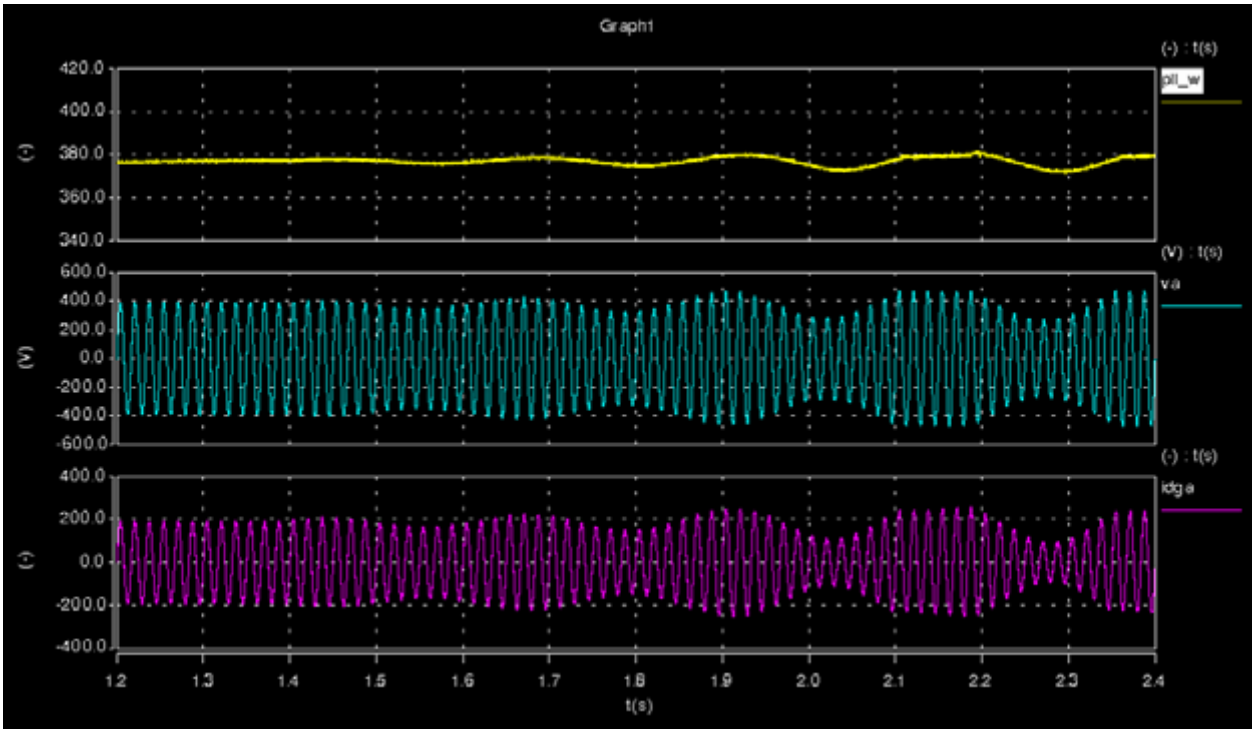


Figure 2-43. Instability caused by voltage scheme with 100% grid impedance

(top: inverter measured frequency (rad/s); middle: inverter voltage (V); bottom: inverter current (A))

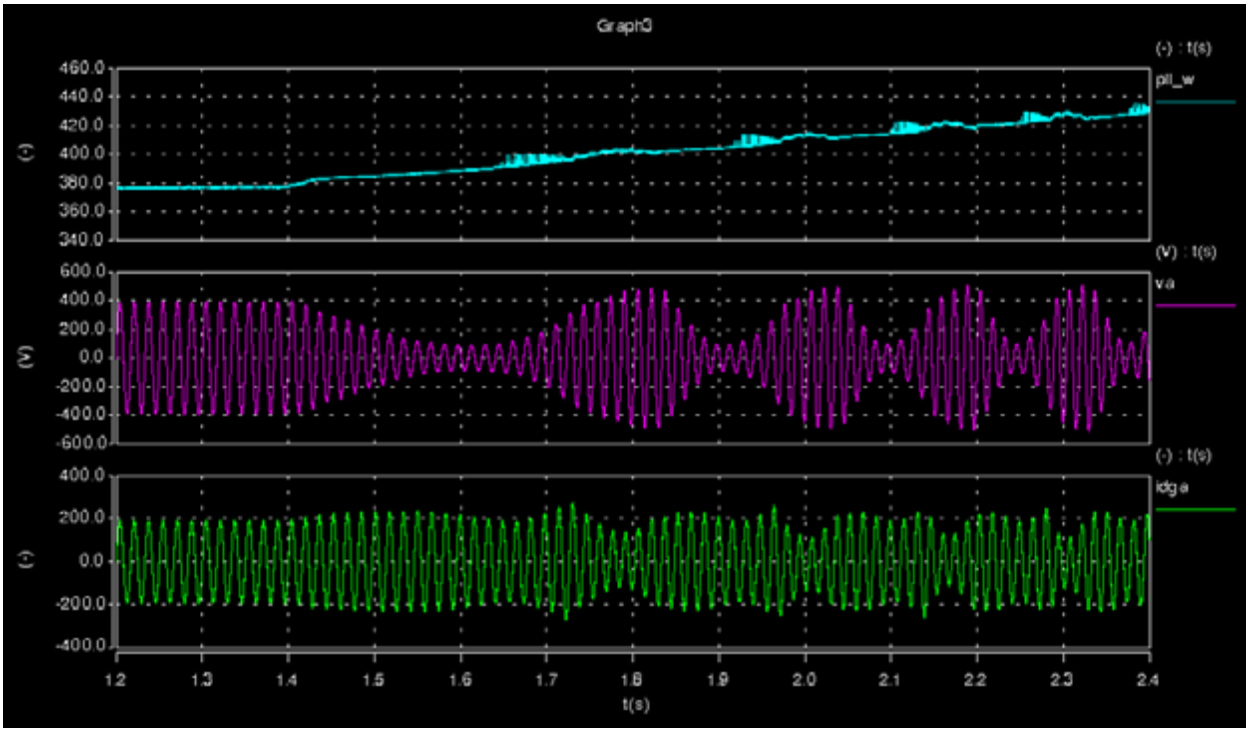
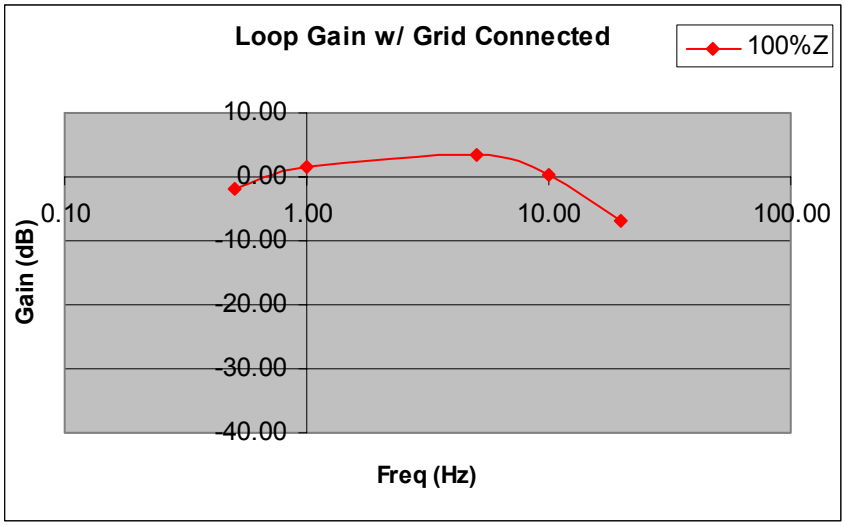


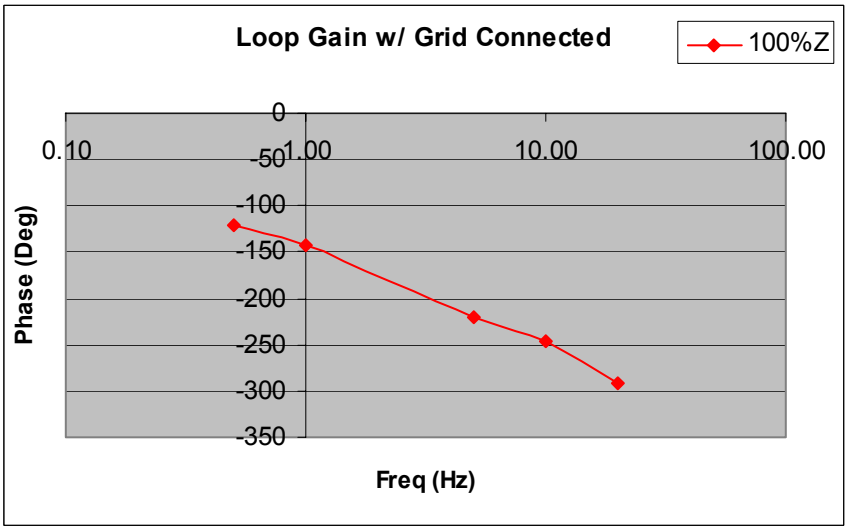
Figure 2-44. Instability caused by frequency scheme with 100% grid impedance

(top: inverter measured frequency (rad/s); middle: inverter voltage (V); bottom: inverter current (A))

The Bode plot of the loop gain with 100% grid impedance is also generated for the voltage scheme, as shown in Figure 2-45. The loop gain shows that the system is unstable because when the gain is across 0dB, the phase is lagging more than 180 degrees. That is why, once the anti-islanding function is enabled, the system becomes oscillatory and eventually goes unstable.



(a) Gain



(b) Phase

Figure 2-45. Voltage scheme loop gain Bode plots with 100% grid impedance

2.4.4 Simulation Results for Single-Phase Inverter

The implementation for a single-phase inverter was also simulated. Figure 2-46 shows the inverter output voltage and its frequency. The frequency drops rapidly after islanding. Meanwhile, the voltage is also dropping because the current magnitude is also impacted by the anti-islanding control, thus causing active power mismatch to result in the voltage change. This scheme has little impact on the power quality because there is no characteristic harmonic injection. Compared with other schemes that use characteristic harmonic distortion, such as zero

crossing chopping, asymmetrical waveforms, etc., the proposed scheme is advantageous in terms of both effectiveness and power quality.

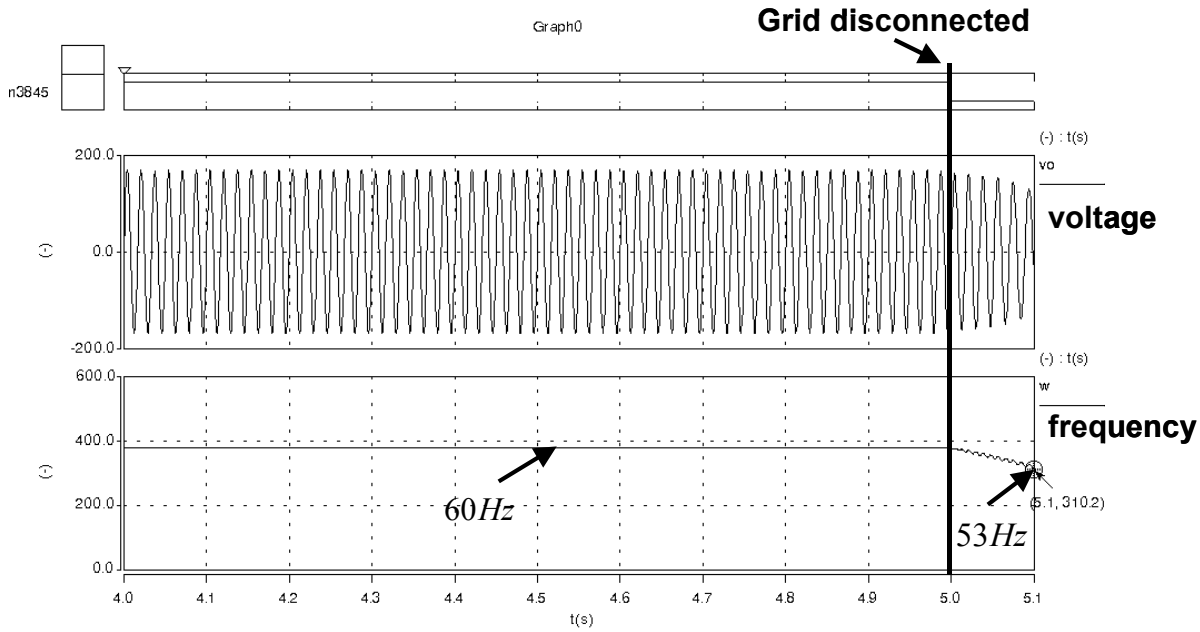


Figure 2-46. Simulation results of the frequency scheme for single-phase inverter

2.5 Summary

This chapter proposes a family of active anti-islanding schemes based on positive feedback and DQ implementation concepts. The proposed schemes have been studied in considerable detail.

Both switching models and average models are developed for a grid-connected three-phase inverter. The models were used for design and evaluation study.

Based on the control theory concept of loop gain, a frequency-domain analysis of the proposed schemes has been presented. The frequency-domain analysis has provided not only insights into the schemes, but also has provided design guideline for the schemes. The dominant factors and worst-case conditions have been identified and analyzed.

Time-domain simulations based on switching models using the inverter production code have been conducted. The time-domain simulations have validated the proposed schemes. Furthermore, the performance of the schemes has also been evaluated for such aspects as power quality, grid disturbance, and power step transient. The stability issue of the positive feedback schemes has been discussed.

In summary, the proposed schemes have no non-detection zone, have negligible power quality impact, have minimal implementation cost (software code only), and are very robust to grid disturbances.

3 Anti-Islanding Testing for Inverter-Based DG

3.1 Introduction

The primary goal of the testing is to validate experimentally the effectiveness of the proposed GE anti-islanding schemes, including the voltage scheme and the frequency scheme.

The second objective is to conduct parametric evaluation of the schemes with respect to different control settings and load conditions, including the controller gains, load power levels, load quality factors.

The recommendations will be made to IEEE P1547.1 based on the lessons learned from the testing.

The tests were conducted at both GE Lab and NREL Lab. In GE Lab, an actual utility was used. At the NREL Lab, a simulated utility was used. With the simulated utility, testing under abnormal utility conditions can be conducted.

3.1.1 Inverter Description

The inverter is based on a GE drive product platform. The platform has been used for different motor drives with different ratings and applications. Currently, the same platform is being converted to grid-connected inverters for use with fuel cells, Sterling engines, wind turbines, etc., distributed generations. The platform design is scalable, with available ratings from 38kW to 1445kW. The inverter chosen for the testing is rated at 145kW with 1.5kHz switching frequency. In the testing, 8kHz switching frequency was used. Therefore, the operational power should be de-rated to be lower than 145kW.

Some key features of the inverter are listed below:

- IGBT Devices
- Heat Pipe Technology for Device Cooling
- Coated Preformed Laminated Bus Assemblies
- Integral DC thru Bus on Common Bus Fed Inverters
- Independent Door Lock & Lockout on each Panel
- 32 bit DSP Single Processor
- Choice of LAN Interfaces

A typical interior and exterior looking of the platform is shown in Figure 3-1.

(a) Exterior **(b) Interior**

Figure 3-1. GE grid-connected inverter product platform

3.1.2 Test System Description

In order to test the inverter functionality, a high voltage DC bus is needed. The high voltage DC bus can be obtained from a high voltage DC power supply, an active rectifier, or a diode rectifier. Among those, a diode rectifier approach was chosen due to its low cost. In the testing, two 480VAC feeds are needed. One is used as the input to the diode rectifier to represent prime mover of a DG system. The other 480VAC is used as a grid. To obtain a sufficient DC bus voltage, a transformer is needed at the diode rectifier input. In addition, a pre-charge circuit is added to start up the DC bus voltage before starting the inverter. The output of the inverter is connected to the grid and load as defined in the testing standards.

Figure 3-2 shows the overall test system. The rectangle frame indicates the cabinet has all components packaged within.

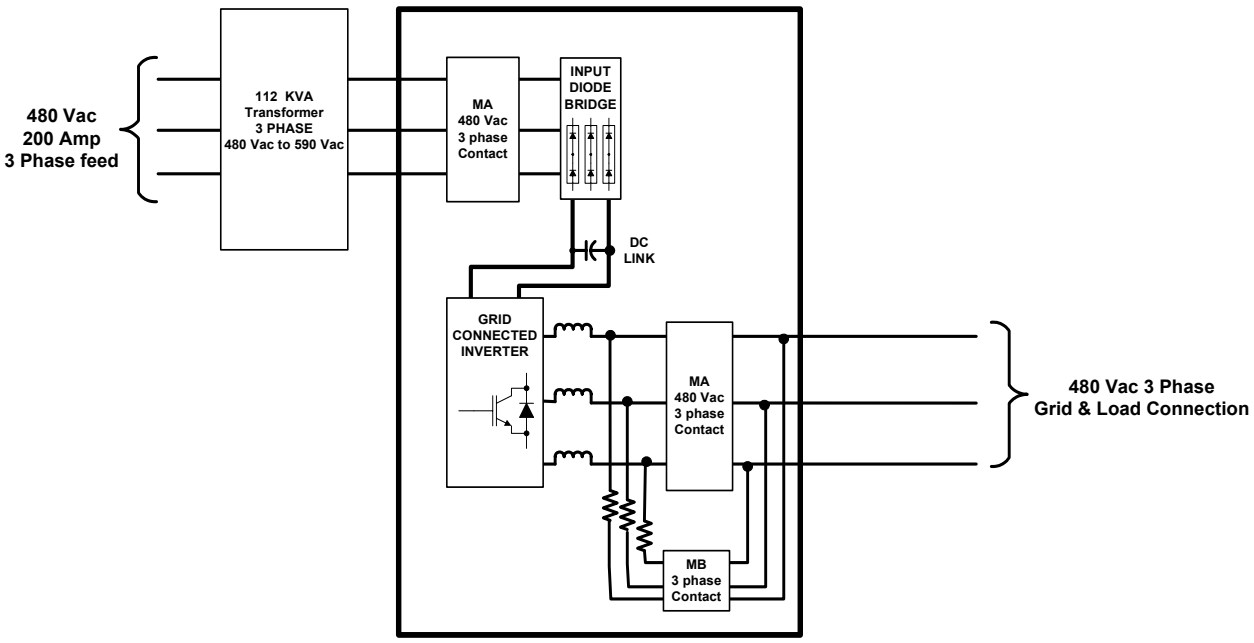


Figure 3-2. The inverter test package

3.2 Testing Results

For all tests, the system is configured as in Figure 3-3, islanding test protocol defined in IEEE P1547.1. The EUT (equipment under test) refers to the overall inverter system in Figure 3-2.

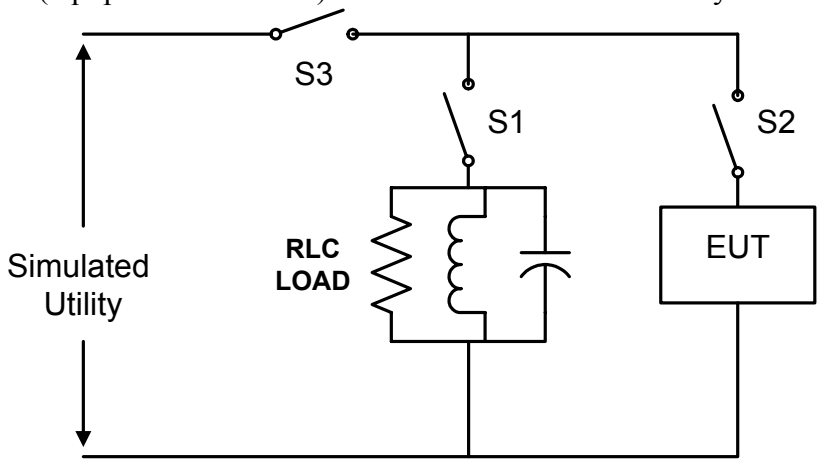


Figure 3-3. Unintentional islanding testing protocol

3.2.1 Test Procedure

1. Turn on the switch S3 to make utility line available.
2. Turn on the switch S1 to connect the load. Load must be made available before connecting the EUT in order to avoid back feed to the simulated utility. The RLC load is adjusted to provide a quality factor Qf of 1.0 (when Qf is equal to 1.0, the following applies $Q_L = Q_C = 1.0 \times P_R$).

3. After utility is available, turn on switch S2 to connect the inverter system. Set the inverter output to match the load power by monitoring the grid current to be zero or near zero within measurement error.
4. After operating in steady state (for more than 1 minute), record all applicable settings of the inverter (AI gain settings, output power, power factor) and the load power (kW, kVar_L, kVar_C).
5. Turn off switch S3 to initiate unintentional islanding.
6. Record the time between the opening of switch S3 and when the inverter ceases to energize the RLC load. In this test, inverter will cease to energize by shutting down itself.
7. The test is repeated with the reactive load (either capacitive or inductive) adjusted in 1% increments or the reactive power output of the EUT adjusted in 1% increments from 95% to 105% of the initial balanced load component value. If unit shutdown times are still increasing at the 95% or 105% points, additional 1% increments shall be taken until trip times begin decreasing.
8. Repeat steps 1-7 at two other different power levels.
9. Repeat steps 1-8 for all three anti-islanding schemes. The first one is voltage scheme only, the second one is frequency scheme only, and the third one is the combined voltage and frequency scheme.

3.2.2 Test Results

The results shown below are obtained from the GE lab test, as well as from the NREL lab test.

At each test condition, a test without anti-islanding schemes was conducted first. The inverter is easily running for more than 10 seconds, in some cases, even indefinitely until manual shut down. Figure 3-4 shows the test results obtained from the NREL lab. Figure 3-5 shows the results from the GE lab. Both have anti-islanding control disabled. After the inverter and the load were islanded, certain load step transient was applied to investigate how the island system voltage and frequency respond to the transient. It was found that a significant load step transient is required to cause voltage or frequency trip. This is further proof that an island can be easily sustained. Special measures to deal with the issue are required to ensure safety of the DG applications.

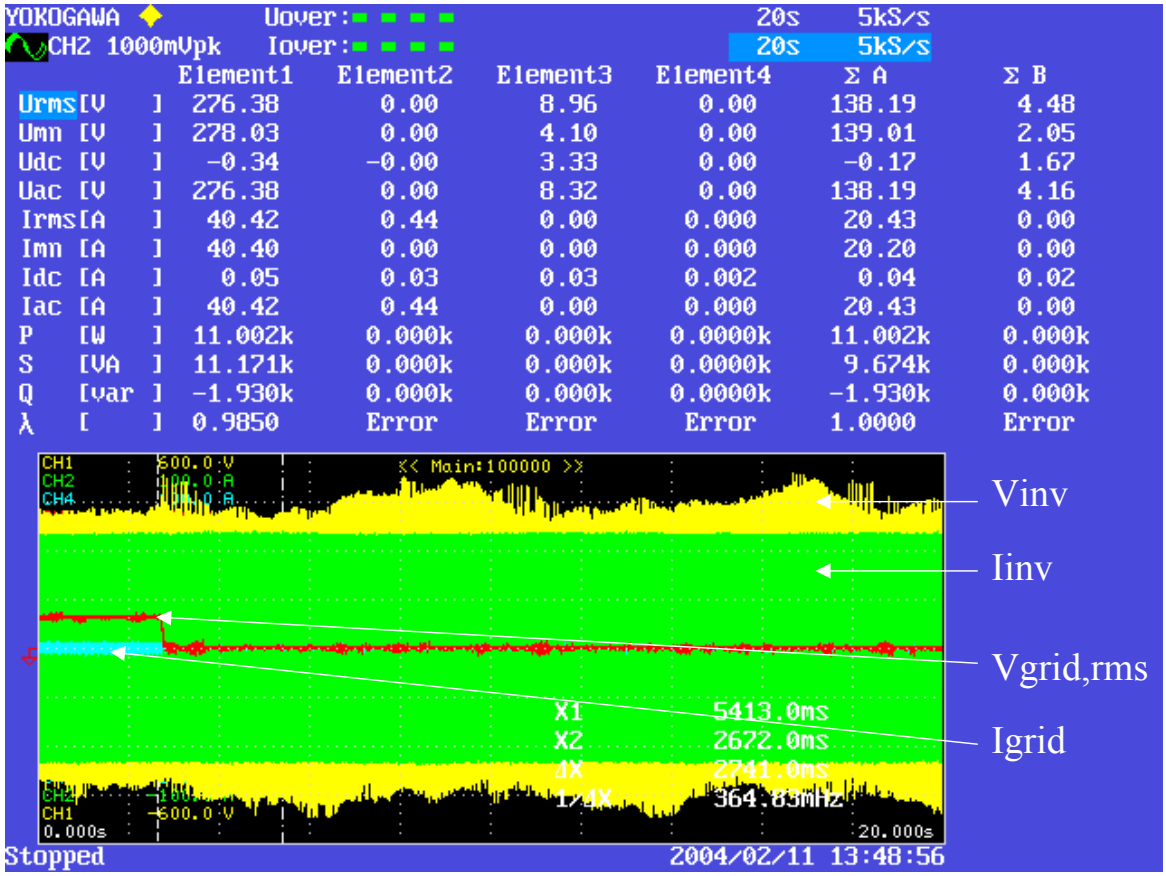


Figure 3-4. NREL lab test results without anti-islanding control

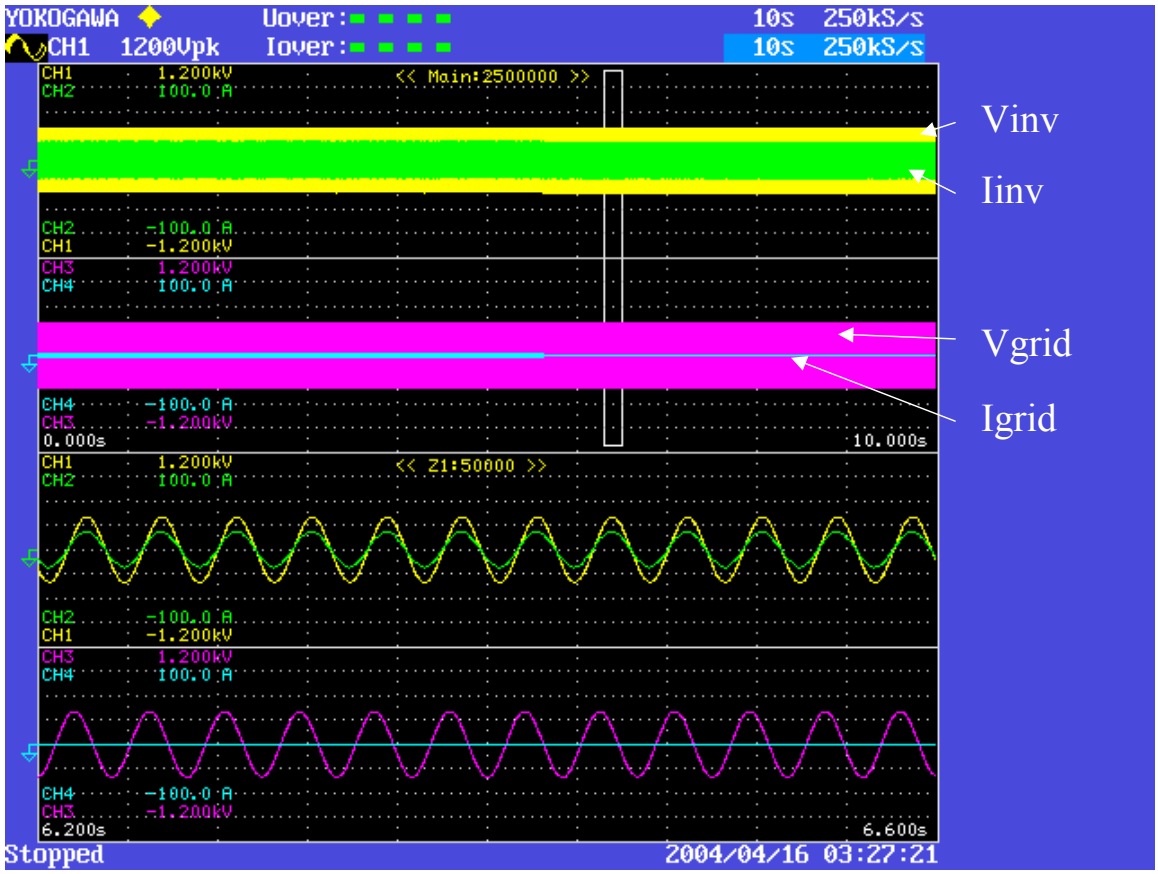


Figure 3-5. GE lab test results without anti-islanding control

Following the test without AI, an anti-islanding scheme then enabled. This way, the effectiveness of the scheme can be clearly demonstrated. In total, three different schemes were tested.

3.2.2.1 Voltage Scheme. Table 3-1 shows the results obtained from the test at NREL lab.

Table 3-1 NREL lab test results.

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Voltage	10	10	10.9	0.76	OV
Voltage	33	35.6	35.6	0.13	OV
Voltage	42	43.4	47.1	0.31	UV

Three different power levels were tested. Three tests were performed at each power level, and the results are repeatable. L and C were tuned so that the net current flow to the utility is minimal. As a result, Quality factor is not exactly at 1.0. One observation from this testing is that the tripping time has no correlation to the power level. From the simulation and analysis conducted earlier, the lower power level should result in higher anti-islanding loop gain, thus better detection capability. However, this is not observed in the testing, under the assumption that faster tripping time indicates better detection.

Figure 3-6 shows the test waveforms of the voltage scheme.

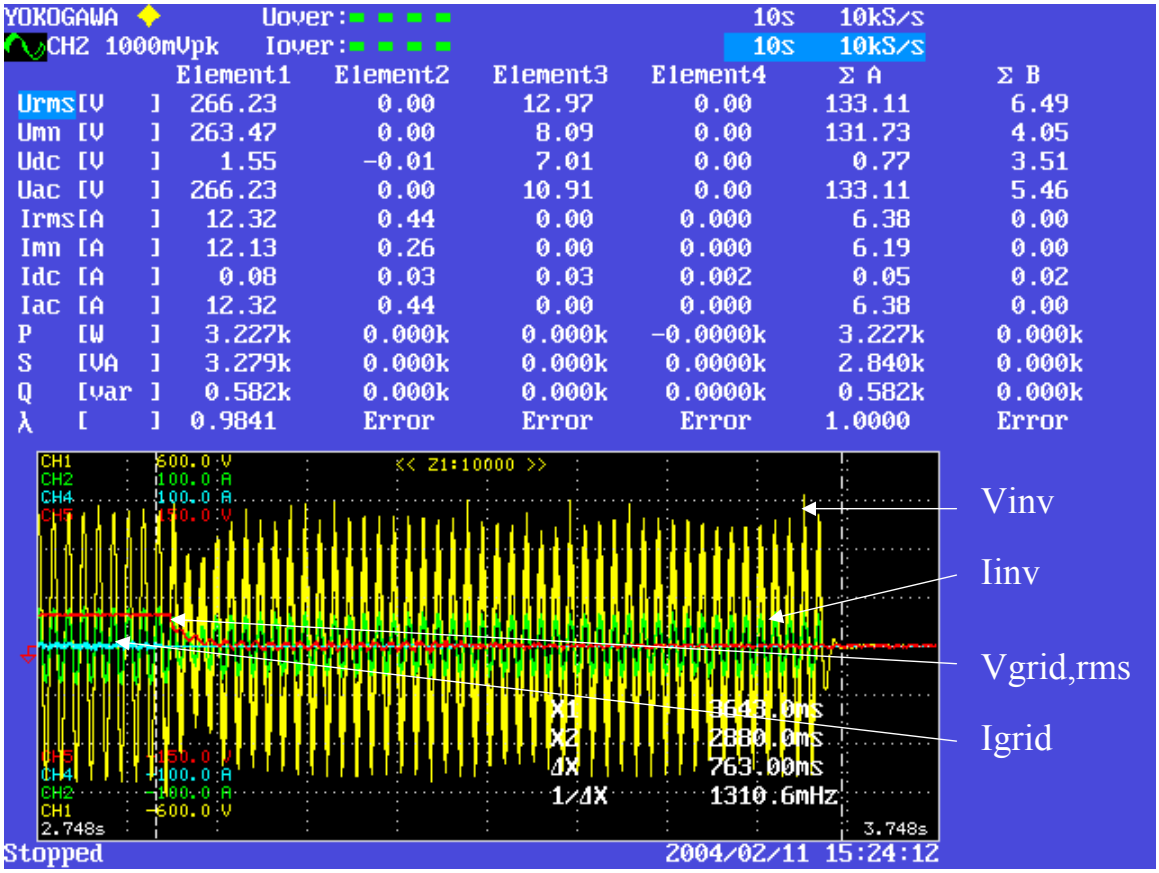


Figure 3-6. NREL lab test results with voltage anti-islanding scheme

3.2.2.2 Frequency Scheme. Table 3-2 shows the test results obtained from the testing at GE lab, since no sufficient test data was obtained from NREL lab testing for the frequency scheme.

Table 3-2 GE lab test results

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Frequency	10	27	27	1.3	UV
Frequency	15	27	27	1.5	UV
Frequency	20	27	27	1.6	OV

Three different power levels were tested. Since L and C are kept constant, effective load quality factors are different with different power levels.

Figure 3-7 shows the test results of the frequency scheme. It can be seen that the frequency drifts away after islanding. However, in this case, the over voltage protection tripped before frequency protection.

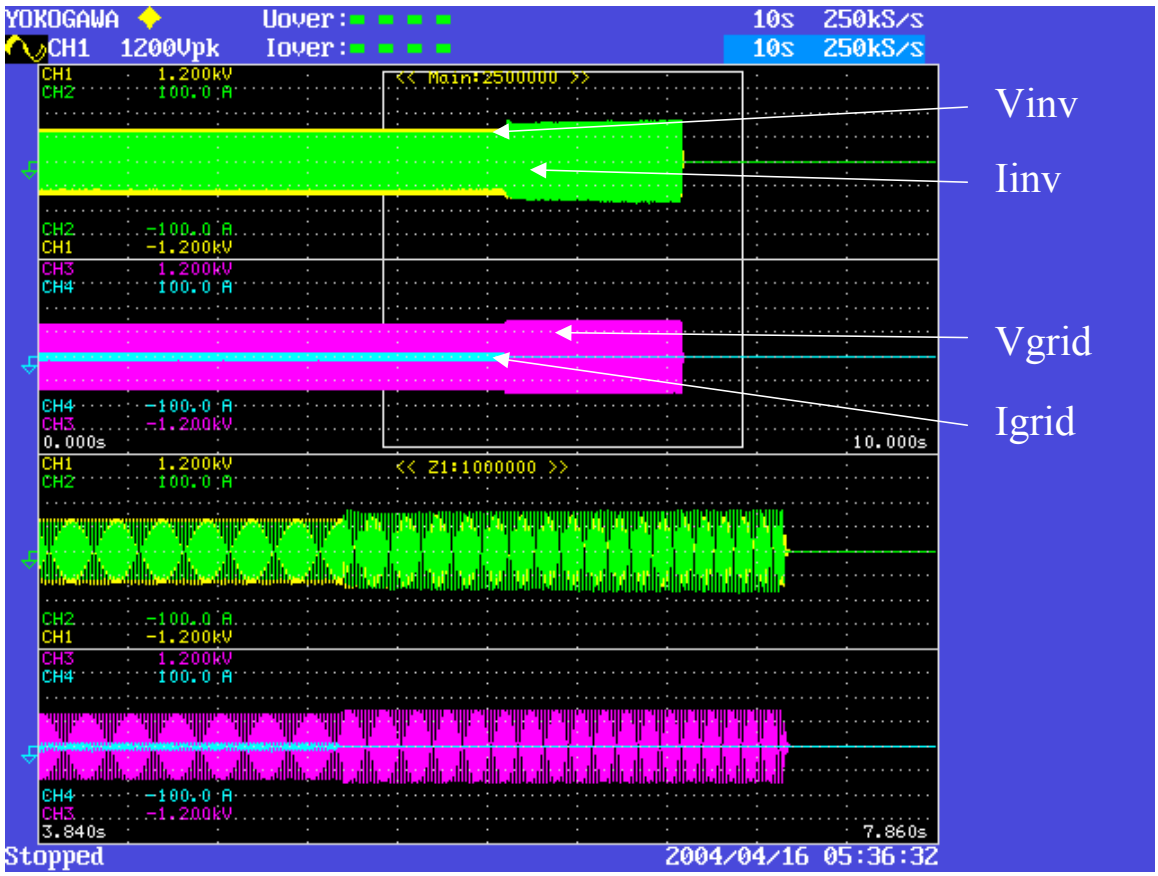


Figure 3-7. GE lab test results with frequency anti-islanding scheme

3.2.2.3 Combined Voltage and Frequency Scheme. Table 3-3 shows the test results for the combined voltage and frequency scheme. The results are obtained from the testing at NREL lab.

Table 3-3 NREL lab test results

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Combined	10.8	10	11.2	0.8	UV
Combined	33	35.6	35.6	1.5	UF
Combined	40	40	46.8	0.4	UV

It is found that the combined scheme has slower tripping time than the voltage scheme alone, but has faster tripping time than the frequency scheme alone. This indicates some interaction between the voltage and frequency schemes.

3.2.2.4 Gain Variation Effect. Tables 3-4 and 3-5 show gain variation effect on the voltage and frequency scheme, respectively. The results are obtained from the testing at NREL lab. With the gain reduced to a certain level, the positive feedback will not be effective, that is, the loop gain becomes below 0 dB, thus, the islanded system may maintain stability if there is close power matching. This indicates that even though a positive feedback control is employed, there is a critical gain, below which the positive feedback control will fail to detect unintentional islanding, and resulting in certain non-detection zones.

Table 3-4 Voltage scheme gain variation test results

Gain_V	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
10	42	43.4	47.1	0.31	UV
1	42	37.5	45	0.36	UV
0.2	42	37.5	45	>10	

Table 3-5 Frequency scheme gain variation test results

Gain_F	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
100	20	27	27	1.6	UF
60	20	27	27	7	UF
10	20	27	27	>10	

3.2.2.5 Low-Voltage-Ride-Through Test. Besides the anti-islanding test, the low-voltage-ride-through test was also conducted. The test procedure of the low-voltage-ride-through is different from the anti-islanding test. Basically, the simulated utility is programmed to be momentarily at low-voltage for a certain period of time, and then recovered to nominal. A delay of the anti-islanding protection is set to be longer than the low-voltage period. This way, the anti-islanding protection will not react to the low-voltage event.

During the low-voltage-ride-through test, however, the inverter trips quickly after the low-voltage event. The delay set in the anti-islanding control code block was not effective since a faster trip initiated by the inverter IGBT bridge was triggered. It was also tested that without anti-islanding control, the inverter still tripped under the low voltage event. The trip was basically a protection of the inverter IGBT bridge.

The scenario was analyzed later. Because of the unregulated DC bus, the inverter system is operating as a constant power source, rather than a constant current source. As a result, a low-voltage event at the utility side of the inverter AC output will cause large current, thus high voltage (Ldi/dt) at the inverter bridge. This high voltage will cause over-voltage protection of the IGBT bridge. This scenario has been simulated in Saber using the same topology as in the testing. A previous report [1] has shown in simulation that the inverter has low voltage ride through capability because the DC bus is an ideal source, thereby the inverter is able to be regulated as an ideal current source. As a conclusion, in order to have low-voltage -ride through capability, the inverter must be designed as a constant current source, not a constant power source. During the low-voltage event, the power feeding to the inverter from the DC bus must be controlled, for example, a crow-bar, so that the inverter can maintain constant current under low AC voltage.

Figure 3-8 shows test results of the abnormal utility condition.

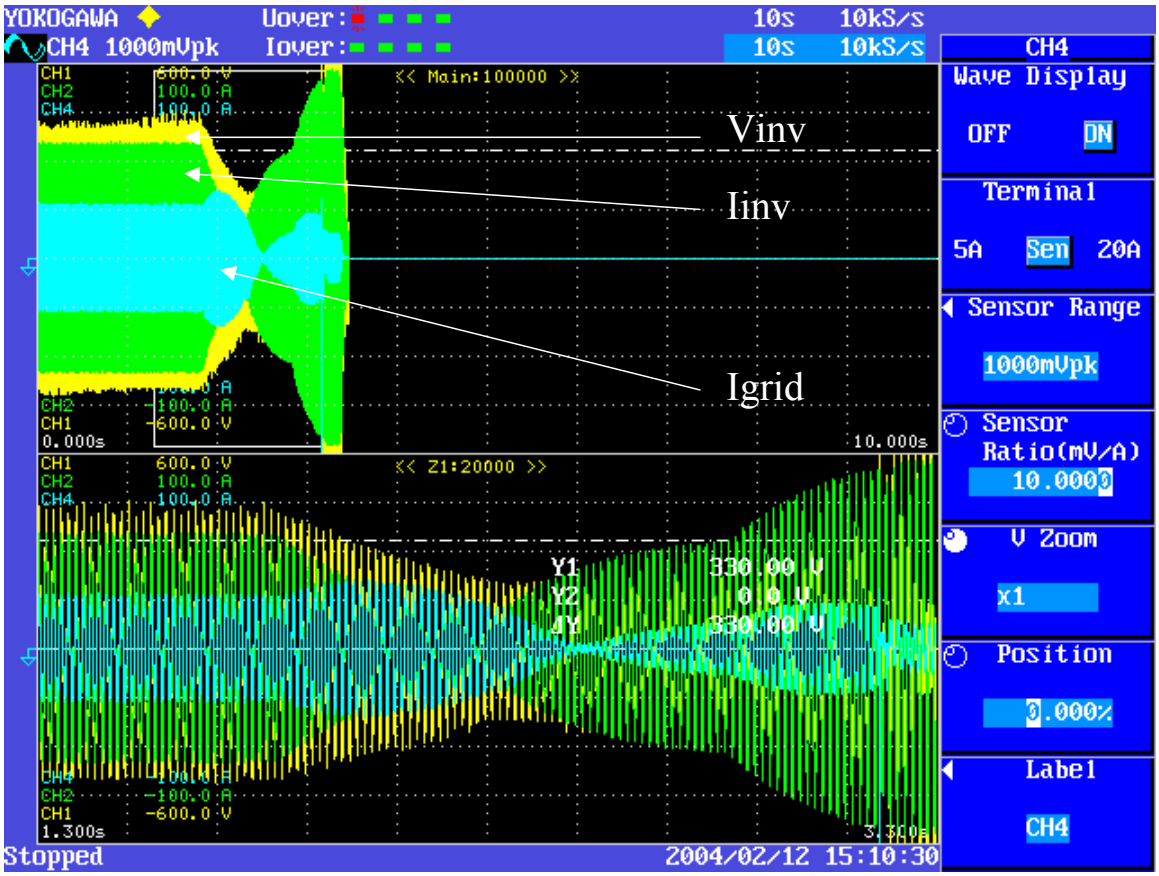


Figure 3-8. Test results with abnormal utility condition.

3.3 Summary

3.3.1 Findings

Below are some findings from the test.

1. If there are no anti-islanding measures, the inverter will run indefinitely in some cases.
2. With the recommended anti-islanding parameter settings, the schemes work successfully (trip within 2 seconds) under all conditions, including worst-case generation/load balance as defined in testing standards.
3. The testing results are repeatable under a fixed condition and parameter setting.
4. The effectiveness of the schemes is not correlated with the tripping time. Intuitively, more effective means faster response and tripping time. However, this is not always observed in the testing. In some cases, given a better detection condition, for example, a higher anti-islanding positive feedback gain, or a lower load quality factor, the anti-islanding control should work more effectively. However, the tripping time is longer in some cases. To make a conclusion from the observations, more testing is needed.
5. When both voltage and frequency schemes are enabled, the tripping time is not faster, or the scheme is not more effective. It indicates some interaction between the two schemes. When applying the schemes, it is recommended to use one scheme so that the performance is more predictable. For the combined scheme, more study and tests are needed for better understanding of the interactions.

6. The THD measurement results indicate that no any degradation effect resulted from the anti-islanding schemes.
7. Besides the anti-islanding testing, low voltage ride through testing was also attempted. It is found that, given the configuration of an unregulated DC bus obtained from a diode rectifier, the inverter is not able to ride through a low voltage event, regardless whether or not the anti-islanding is enabled. In order to have low voltage ride through capability, the DC bus voltage must be regulated so that the inverter can be operated as a constant current source.

3.3.2 Recommendations

The anti-islanding tests at GE and NREL labs are still very preliminary. More structured tests are needed in order to draw some conclusions. It is still believed that the tripping time is an index of effectiveness of the schemes. In order to find the correlation between the parameters and the tripping time, more fine tuned tests are necessary to find the maximum tripping time under each condition.

The test procedures defined in P1547.1 are not always followed due to limited equipment capabilities, for example, load incremental variations, non-back feeding simulated utility, measurement accuracy. Alternative testing procedures should be explored and verified as equivalency.

4 Anti-Islanding Control for Machine-Based DG

4.1 Synchronous Machine and Power System Modeling

Synchronous generators can be analyzed conveniently using the Park's transformation, which results in a time-invariant nonlinear system. A linearized model can be obtained from the time-invariant model at a steady-state operating point. In the event that the system experiences a small perturbation, the linearized power system models can be used with advantage for both analysis and controller design. Such a linear design on a nonlinear system generally provides asymptotic stability over a small region about the equilibrium point and is appropriate for the dynamic stability problem where the primary concern is providing damping following small disturbances.

The mathematical model of a synchronous machine along with various control strategies has been well documented in the literature [6]. For completeness, the model of a machine used in the analysis is reported here again in detail. The overall control block diagram of the machine model is shown in Figure 4-1. The most noticeable feature here is that when the generator is connected to the grid, the main task of the generator is to maintain its real and reactive power output as a typical DG operational mode (in some cases, instead of reactive power, power factor regulation is used). The regulation of the real power is achieved through a feed-forward controller applied to the governor while the regulation of the reactive power is carried out through a feedback PI (Proportional-Integral) controller cascaded with the exciter.

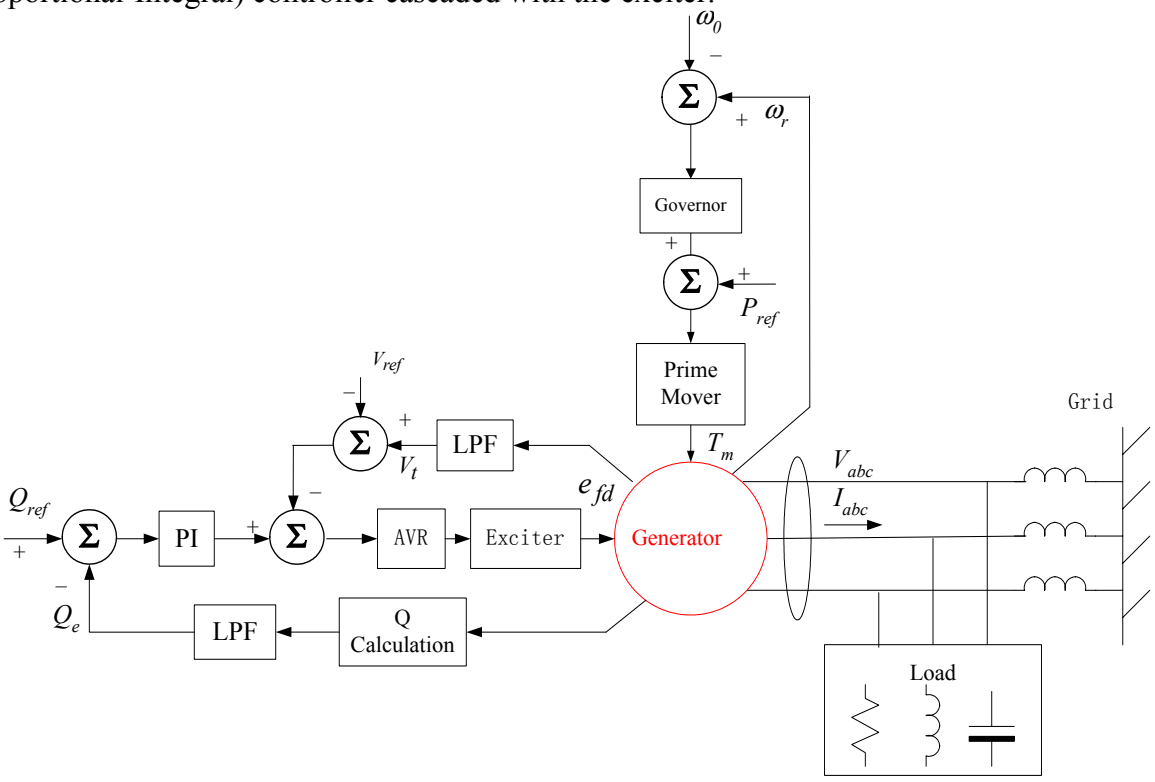


Figure 4-1.Synchronous generator system and its control block diagram

4.1.1 Synchronous Generator Model for Islanding Studies

The dynamics of the synchronous machine can be described by a set of nonlinear differential equations. Typically, the states can be associated with each machine's armature currents, rotor currents resolved through the Park's equations, rotor dynamics, automatic voltage regulator (AVR,) and the turbine-governor dynamics.

In developing the model of a synchronous machine for islanding studies, the following assumptions were made. The worst-case islanding is when the power mismatch is small and the system is operating under steady-state conditions before islanding. This provides solid justification for the following assumptions:

- The air gap flux is distributed sinusoidally along the air gap.
- Magnetic hysteresis is negligible.
- Magnetic saturation effects are neglected.

After simplifications, the following set of equations of the machine model can be obtained.

Voltage equations

$$u_d = p\Psi_d - \Psi_q \omega_r - R_a i_d \tag{4.1}$$

$$u_q = p\Psi_q + \Psi_d \omega_r - R_a i_q \tag{4.2}$$

$$e_{fd} = p\Psi_{fd} + R_{fd} i_{fd} \tag{4.3}$$

$$0 = p\Psi_{1d} + R_{1d} i_{1d} \tag{4.4}$$

$$0 = p\Psi_{1q} + R_{1q} i_{1q} \tag{4.5}$$

Flux linkage equations

$$\Psi_d = -(L_{ad} + L_l) i_d + L_{ad} i_{fd} + L_{ad} i_{1d} \tag{4.6}$$

$$\Psi_q = -(L_{aq} + L_l) i_q + L_{aq} i_{1q} \tag{4.7}$$

$$\Psi_{fd} = (L_{ad} + L_{fd}) i_{fd} + L_{ad} i_{1d} - L_{ad} i_d \tag{4.8}$$

$$\Psi_{1d} = L_{ad} i_{fd} + (L_{1d} + L_{ad} i_{fd}) i_{1d} - L_{ad} i_d \tag{4.9}$$

$$\Psi_{1q} = (L_{1q} + L_{aq}) i_{1q} - L_{aq} i_q \tag{4.10}$$

Air-gap torque

$$T_e = \Psi_d i_q - \Psi_q i_d \tag{4.11}$$

Here the flux is denoted by Ψ. Inductance by L, and terminal voltage is expressed in the D-Q frame [6]. Generally, in case of synchronous machines, the prime mover and other essential mechanical assemblies are mounted on the same shaft. Based on the period involved, it is a good approximation to assume the rotor mass as a rigid body. Hence, for the islanding studies, the following differential equations are used to represent the synchronous machine rotor dynamics.

$$\frac{d^2\delta}{dt} = \frac{1}{2\mathrm{H}}(Tm - Te) \tag{4.12}$$

$$\frac{d\delta}{dt} = \omega_r - \omega_0 \tag{4.13}$$

where:

i_d and i_q are direct-axis and quadrature-axis currents of the generator;

u_d and u_q are direct-axis and quadrature-axis voltage of the generator;

i_{fd} is field winding current of the generator;

e_{fd} is field voltage applied to the generator;

i_{1d} and i_{1q} are direct-axis and quadrature-axis damper winding currents of the generator;

R_a is stator winding resistance of the generator;

R_{fd} is field resistance of the generator;

R_{1d} and R_{1q} are damper winding resistance of the generator;

L_l is stator winding inductance of the generator;

L_{fd} is field leakage inductance of the generator;

L_{1d} and, L_{1q} are direct and quadrature leakage inductance of the generator;

L_{ad} and L_{aq} are direct and quadrature magnetizing inductance of the generator;

ω_r is rotating speed of the generator;

δ is power angle of the generator;

T_m is mechanical torque of the generator;

T_e is electromagnetic torque of the generator;

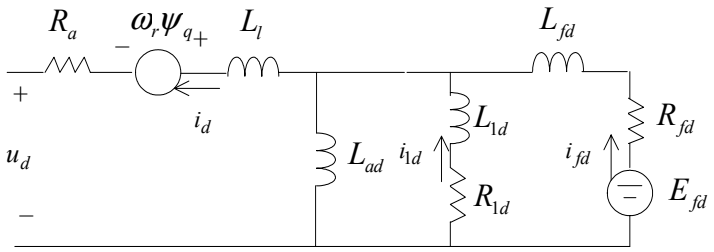
H is inertia constant of the generator;

Ψ_d and Ψ_q are direct and quadrature flux linkage of the generator;

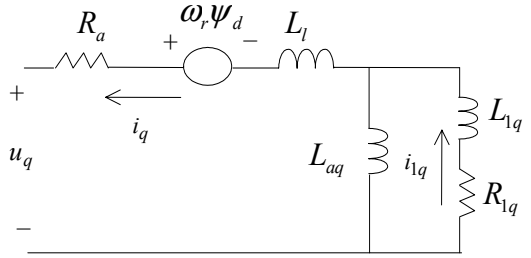
Ψ_{fd} is field winding flux linkage of the generator;

Ψ_{1d} and Ψ_{1q} are direct and quadrature damper winding flux linkage of the generator.

Based on equations (4.1 through 4.13), an equivalent circuit of the synchronous machine can be developed as shown in the Figure 4.2.



(a) d-axis equivalent circuit



(b) q-axis equivalent circuit

Figure 4-2. Synchronous generator d- and q-axis equivalent circuits

4.1.2 Excitation System Model and Reactive Power Regulation

Most generators are equipped with an Automatic Voltage Regulator (AVR). These devices maintain the terminal voltage of the generator at a specified value by modulating the field voltage and hence the field current to supply the required reactive power to the load. However, as a distributed generation, the voltage regulation is prohibited by IEEE 1547, unless special agreements are made. A common operation mode for DG is reactive power (or power factor) regulation.

The exciter systems widely used for synchronous machines are commonly subdivided into the 4 different categories. More detailed aspects of modeling an excitation system for simulation studies can be found in [7]. For simplicity of analysis in the period involved, the excitation system here is represented as a tuned PI controller with a necessary lag circuit. The parameters of the circuit model are approximated from the aggregate response of terminal voltage of a generator. Figure 4-3 shows the model of the excitation system used for the machine simulation. A feedback PI controller is cascaded with the exciter to regulate the reactive power of the machine. Therefore, when the grid is connected, the reactive power output of the machine will follow the desired reference value. The parameters of the PI controller are given in the Appendix of this report.

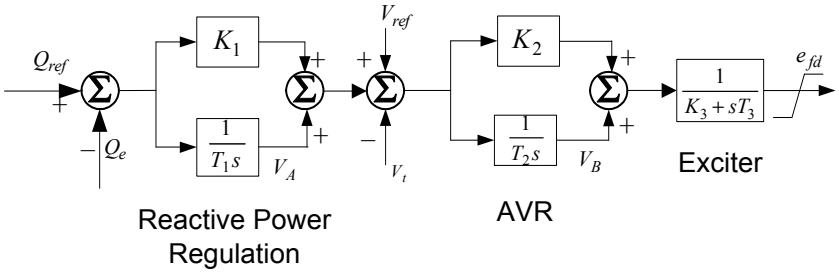


Figure 4-3. Control block diagram of excitation system

The description of the reactive power regulator and the exciter is given by

$$\dot{V}_A = (Q_{ref} - Q_e)/T_1 \tag{4.14}$$

$$\dot{V}_B = [V_{ref} - V_t + V_A + K_1(Q_{ref} - Q_e)]/T_2 \tag{4.15}$$

$$\dot{e}_{fd} = [V_B - K_3 e_{fd} + K_2(V_{ref} - V_t + V_A + K_1(Q_{ref} - Q_e))]/T_3 \tag{4.16}$$

where:

V_A and V_B are the intermediate variables indicated in Figure 4-3;

K_1, K_2 and K_3 are constant in the controller;

T_1, T_2 and T_3 are time constant in the controller;

Q_{ref} is the reference value of the reactive power;

Q_e is the reactive power output of the generator;

V_{ref} is the reference for the terminal voltage;

V_t is the terminal voltage of the generator;

e_{fd} is the field voltage as the input to the generator.

4.1.3 Governor Model and Active Power Regulation

The governor system consists of a prime mover and provides the necessary mechanical power required by the generator. The governor is represented by a droop function with P_{ref} input and the prime mover is described by a lag function. Figure 4-4 shows the typical representation of a governor and the real power regulation for these islanding studies:

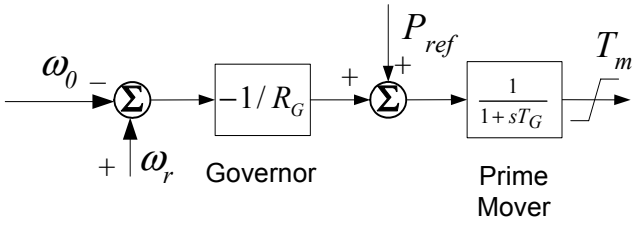


Figure 4-4 Control block diagram of governor

The governor dynamics is (including the prime mover)

$$\dot{T}_m = \frac{1}{T_G}\left(P_{ref} + \frac{\omega_0 - \omega_r}{R_G} - T_m\right) \tag{4.17}$$

where:

T_G is the time constant of the prime mover of the generator;

R_G is the governor droop.

4.1.4 RLC Load Model and Induction Motor Load Model

Load characteristics have an important influence on the dynamical behavior of the generator when it is islanded. The modeling of actual loads is complicated because a typical load bus is composed of a large number of devices such as fluorescent and incandescent lamps, refrigerators, heaters, compressors, motors, furnaces, and so on. Based on a considerable amount of simplification, two types of the loads are most often investigated in the islanding studies: a RLC load and an induction motor load.

The RLC load is as simple as the aggregation of a resistor, an inductor, and a capacitor in parallel. While such a load can represent the steady-state fundamental frequency characteristics of an actual load, this type of model is not a realistic representation of a load because the dynamic and non-fundamental characteristics of actual loads are not accurately simulated. Given the terminal voltage, the current through the resistance, inductance and the capacitance is determined by the following equations.

$$\frac{d}{dt}\begin{pmatrix} i_{dL} \\ i_{qL} \end{pmatrix} = \frac{1}{L}\begin{pmatrix} u_d \\ u_q \end{pmatrix} + \omega\begin{pmatrix} i_{qL} \\ -i_{dL} \end{pmatrix} \tag{4.18}$$

$$\frac{d}{dt}\begin{pmatrix} u_{dC} \\ u_{qC} \end{pmatrix} = \omega\begin{pmatrix} u_q \\ -u_d \end{pmatrix} + \frac{1}{C}\begin{pmatrix} i_{dc} \\ i_{qc} \end{pmatrix} \tag{4.19}$$

$$\begin{pmatrix} i_{dR} \\ i_{qR} \end{pmatrix} = 1/R\begin{pmatrix} u_d \\ u_q \end{pmatrix} \tag{4.20}$$

where:

i_{dR} i_{qR}, i_{dL} i_{qL} and i_{dC} i_{qC} are the d-axis and q-axis currents through the load resistance, inductance and capacitance, respectively.

u_d u_q are d-axis and q-axis terminal voltage.

R, L, and C are the value of load resistance, capacitance and inductance, respectively.

The RLC load equivalent circuit in DQ is shown in Figure 4-5.

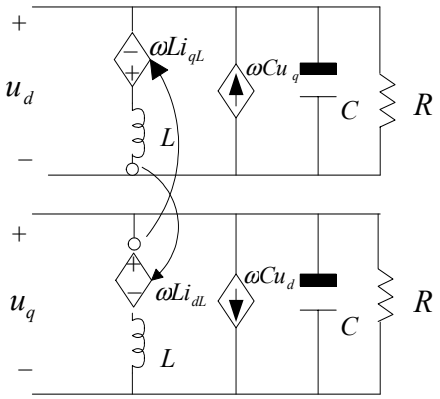


Figure 4-5. DQ equivalent circuit model of RLC load

Typically, motors consume 20% to 70% of the total energy supplied by a feeder. Therefore, the dynamics attributable to motors are usually the most significant aspects of dynamic characteristics of the overall system load. Motor loads, however, vary largely in characteristics due to different applications. The motor load used in the simulation studies described in this report is a compromise; it is intended to represent a general population of motors ranging in types from those in small residential/industrial applications to large motors. The default motor load uses only a single-cage representation. This is adequate for dynamic stability studies where damping of oscillations, rather than stalling of motors and motor starting, is the focus.

The induction motor to be studied is represented by a standard single-cage model with the transient variations of its rotor flux linkage handled explicitly. The motor can be described by performance-based parameters or equivalent circuit parameters. The driven load is characterized by the inertia constant H_m of the combined motor-load rotor and the exponent D, relating driven load to its speed. The detailed modeling of the motor load can be found in [8]. The dynamics of the induction motor is described by

$$\dot{e}_{dm} = -\frac{1}{T_0^{'}}(e_{dm} + (X_{sm} - X_{sm}^{'})i_{qm}) + p\theta_r e_{qm} \tag{4.21}$$

$$\dot{e}_{qm} = -\frac{1}{T_0^{'}}(e_{qm} - (X_{sm} - X_{sm}^{'})i_{dm}) - p\theta_r e_{dm} \tag{4.22}$$

$$2H_m\dot{\omega}_m = (e_{qm}i_{qm} + e_{dm}i_{dm}) - T_{norm}(\frac{\omega_m}{\omega_0})^D \tag{4.23}$$

where:

e_{dm}, e_{qm} are D-axis and q-axis components of the motor transient stator voltage;

i_{dm}, i_{qm} are D-axis and q-axis components of the motor transient stator current;

X_{sm} is the motor synchronous inductance;

X'_{sm} is the motor transient inductance;

H_m is inertia constant of the motor;

D is load model exponent of the motor;

T_{norm} is normal value of mechanical torque of the motor;

ω_m is rotating speed of the motor.

Figure 4-6 shows the DQ equivalent circuit of the induction motor.

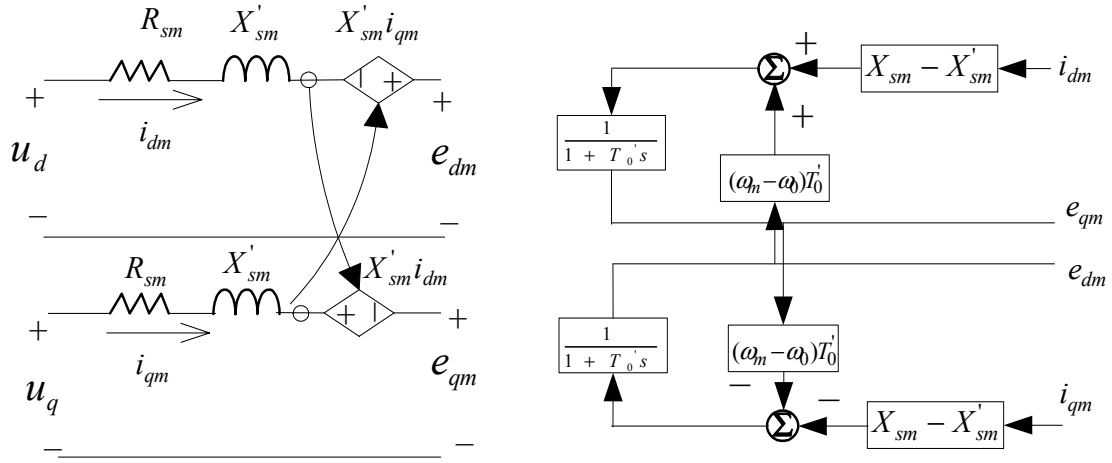


Figure 4-6. DQ equivalent circuit model of induction motor

4.1.5 Grid Model

Since the synchronous machine is connected to an infinite bus, the d-q terminal voltage of the machine is constrained by the grid voltage, described in DQ frame below:

$$\begin{pmatrix} u_d \\ u_q \end{pmatrix} = R_e \begin{pmatrix} i_{dgrid} \\ i_{qgrid} \end{pmatrix} + L_e \begin{pmatrix} \dot{i}_{dgrid} \\ \dot{i}_{qgrid} \end{pmatrix} - \omega L_e \begin{pmatrix} i_{qgrid} \\ -i_{dgrid} \end{pmatrix} + V^{\infty} \begin{pmatrix} \sin(\delta + \alpha) \\ \cos(\delta + \alpha) \end{pmatrix} \tag{4.24}$$

where:

R_e and L_e are the grid resistance and inductance respectively

V^{∞} is the rms value of the bus voltage and α is its phase angle

i_{dgrid} and i_{qgrid} are the d-axis and q-axis currents flowing into the grid

Figure 4-7 shows the grid DQ equivalent circuit.

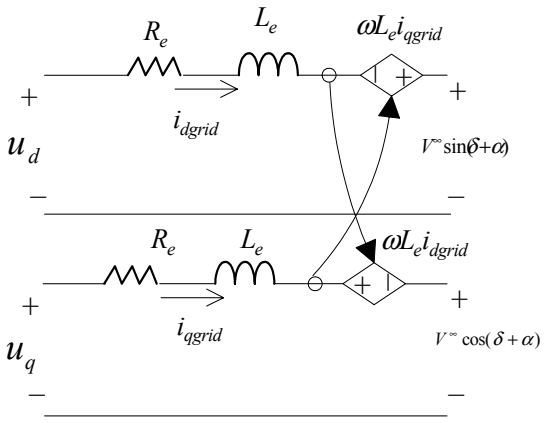


Figure 4-7. DQ equivalent circuit model of grid

System Small-Signal Modeling

In the preceding section, we have developed the equivalent DQ circuit model for the generator, load and the grid respectively. The equivalent circuit of the overall system to be studied can be easily obtained by combining those components together. One circuit model of such a system consisting of the DG, the RLC load, and the grid is shown in Figure 4-8. This equivalent circuit is highly nonlinear and cross-coupled. If the perturbation applied to the power system is small, the linearized model, also called small-signal model, can be obtained by linearizing the equations from (4.1) to (4.24) around an operation point. Therefore, the highly nonlinear model can be greatly simplified and the dynamical characteristics of the power system can be approximately analyzed from the small-signal model.

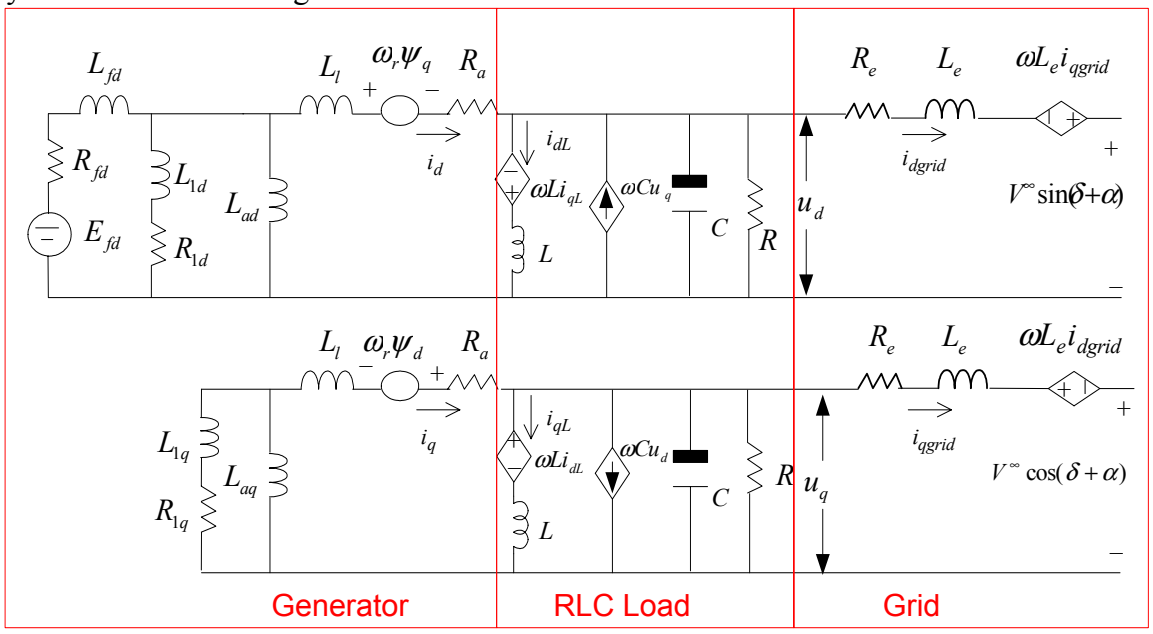


Figure 4-8 DQ equivalent circuit model of the overall system

4.2 Anti-islanding Concept and Implementation

Although the positive feedback concept has been successfully used for the inverter-based DG for anti-islanding protection, the application of the concept to synchronous machine has not yet been explored extensively. Typically, a rotating-machine-based DG is characterized by higher inertia, longer time constants than an inverter-based DG. Due to these factors, the machine and the inverter-based DG respond in fundamentally different ways.
In support of the design and implementation, both frequency-domain and the time-domain analysis are conducted to provide the insights into the characteristics of the proposed schemes.

4.2.1 Implementation of the Active/Reactive Power Schemes

The positive feedback for the synchronous machine comes in two different ways, denoted as active power AI scheme and reactive power AI scheme, because the feedback modifies the active power and reactive power references, respectively. The structures of the active and reactive power AI scheme are shown in Figure 4-9. The active power AI compensator takes the variations in the frequency as input to modify the active power reference to the DG. The reactive power AI compensator uses the variation in the voltage magnitude to change the reactive power reference.

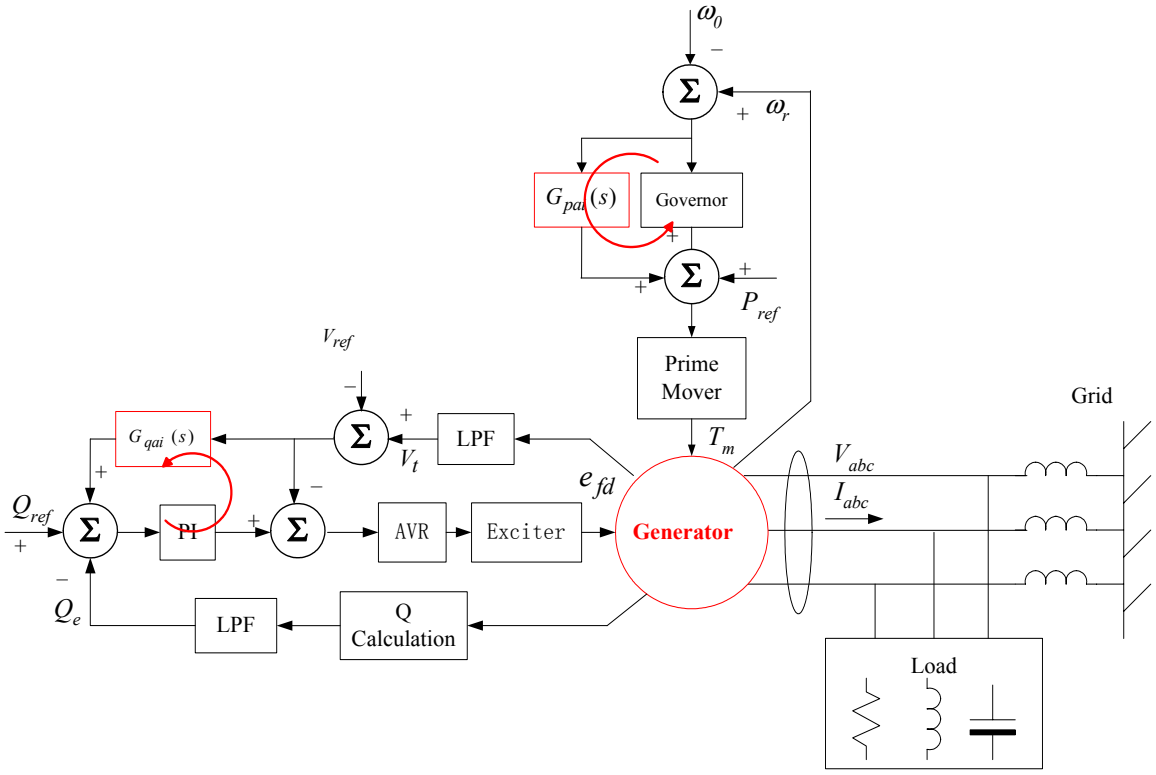


Figure 4-9 Schematic of the machine with the AI compensators

The AI compensators both consist of a washout filter and a proportional gain. The washout filter is designed to ensure that the AI compensators only react to the transient of the frequency/voltage, but not causing any DC steady-state error. When there is a voltage or frequency variation, the responses of the AI loop will amplify the voltage or frequency variation in the same direction. Therefore, the loops are called positive feedback. The mechanism can be further illustrated below.

When there is a generator terminal voltage variation, for instance, voltage increases slightly, the reactive power reference will be increased due to the reactive power AI loop, which will lead to a boosted voltage reference, thus causing the terminal voltage to further increase. When properly designed, the effect of the reactive power AI loop is insignificant when the grid is connected because the grid will regulate the terminal voltage magnitude. Once grid is lost, the reactive power AI loop becomes dominant and drives the voltage away from nominal.
A similar mechanism applies to the frequency. When there is a generator speed (frequency) variation, e.g. frequency increases slightly (due to under loading), the active power reference will be increased due to the active power AI loop, which will further generate a greater mechanical torque (resulting in more under loaded), causing higher speed (frequency). When properly designed, the mechanism will create this instability only in an islanded system, and cause a frequency relay to trip.

In summary, the main idea is that the active/reactive power AI compensators have a dominant effect in the frequency/voltage oscillations when the grid connection is lost. But, with a proper design, these destabilization effects are negligible, when the machine is connected to the grid.

4.2.2 Design Guideline Based on Frequency-Domain Analysis

The basic principles of the positive feedback for islanding detection have been introduced. This section will emphasize the design and implementation of the AI compensator. In order to illustrate the design guideline, a loop gain concept is used. MATLAB is used for the following frequency-domain analysis.

The loop gains of the active and reactive AI loops can be measured by breaking the loops, shown in Figure 4-10, where p_{in} and p_{out} are at the breaking point for the active power loop, while q_{in} and q_{out} are for the reactive power loop.

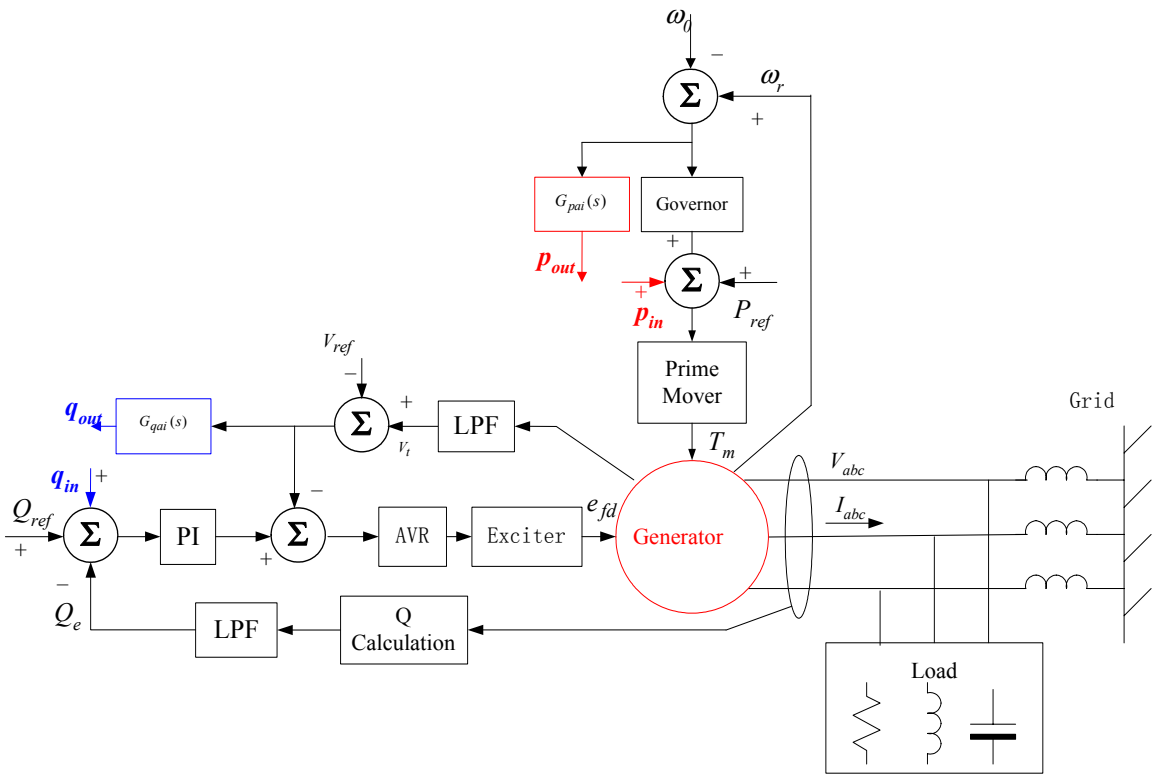


Figure 4-10. Schematic of the machine with the AI loops opened

The loop gain is defined as the small-signal transfer function from the perturbation signal p_{in} (or q_{in}) to the output p_{out} (or q_{out}). Therefore, the active power loop gain is given by

$$T_p(s) = \frac{p_{out}}{p_{in}} \tag{4.25}$$

Similarly, the reactive power AI loop gain is defined as the small signal transfer function from the perturbation signal from q_{in} to the output q_{out}.

$$T_q(s) = \frac{q_{out}}{q_{in}} \tag{4.26}$$

From the loop gain, the system dynamics can be characterized by, for example, the stability margins. For anti-islanding control, criterion for the design principles are:

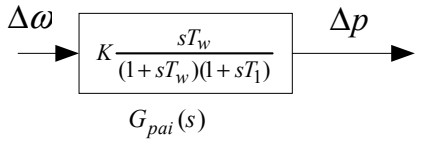
1. When the grid is connected, the loop gain should indicate a stable system, i.e., the peak of the AI loop gain must be less than 0dB. The lower the loop gain is below 0dB, the less impact the AI loop will have on the DG's normal grid-connected operation.

2. When the grid is disconnected, the loop gain should indicate an unstable system, i.e., the peak of the AI loop gain must be greater than 0dB, while the phase is lagging more than 180 degrees. The unstable system will ensure that the islanded system can be detected even when there is 100% active and reactive power matching. The higher the loop gain, the more quickly the island voltage or frequency will move outside the normal operational windows to trigger voltage or frequency protection. However, the gain should not be too high to ensure

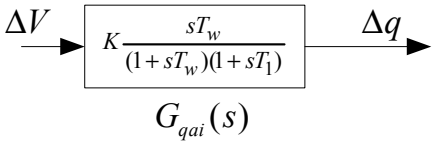
that criterion (1) is met. Basically, criterion (1) sets the upper bound of the loop gain, while criterion (2) sets the lower bound of the loop gain.

If both criteria are satisfied, the AI compensator will amplify the frequency/voltage transients when the machine is islanded but with minimal effect on the frequency/voltage dynamics when the grid is connected.

Figure 4-11 shows the formula of the active/reactive power AI compensator.



(a) Active power AI compensator



(b) Reactive power AI compensator

Figure 4-11. Active and reactive AI compensators

The AI compensator basically consists of a washout filter, a gain, and a first-order filter. The crucial step in the design is to determine the setting for the active/reactive power AI compensator. The critical settings include:

(1) The corner frequency of the washout filter, T_W

(2) The gain, K

(3) The low pass filter corner frequency T_1

The washout function serves as a high-pass filter, with a time constant Tw to allow signals with frequency higher than 1/Tw to pass. For the signal with a frequency lower than 1/Tw, especially for a DC signal, it will be attenuated by the washout filter. This is to minimize the AI loop impact on the steady-state regulation. The low pass filter corner frequency T1 is set to attenuate high-frequency noise. The combined washout filter and the low-pass filter constitute a band-pass filter. The selection of gain, K is a compromise between the high enough gain to ensure islanding detection quickly and the low enough gain to have minimal impact on the DG under the grid-connected conditions. The gain selection should leave certain margins for both grid-connected and islanded conditions.

4.2.3 Practical Design Considerations

The basic criteria for the AI design have been discussed. However, the parametric design of the AI compensator is still an issue since the active/reactive power loop gains may vary with the different load conditions. In order to ensure that the AI control is effective under all circumstances, the AI compensator must be designed under the worst-case situation. The critical gain can only be approximately determined after the study of a range of different load conditions. Consequently, the impact of the various passive and motor load conditions on the loop gains must also be examined. The preliminary study concludes that the situations important to this AI

scheme design are those where the grid impedance is high or there is a high penetration of induction motor load.
After the worst cases have been identified, the active and reactive power AI compensators are chosen as in (4.27) and (4.28), respectively.

$$\frac{\Delta p}{\Delta \omega} = \frac{61.1s}{(1+0.32s)(1+0.29s)} \tag{4.27}$$

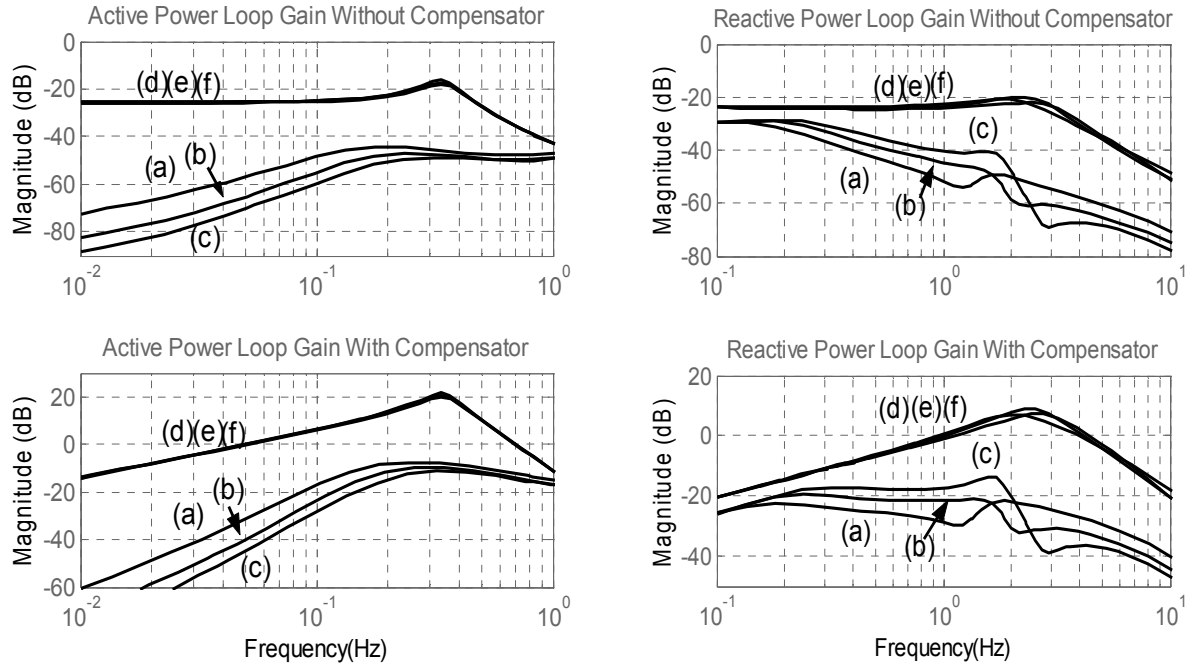
$$\frac{\Delta q}{\Delta V} = \frac{2.41s}{(1+0.048s)(1+0.016s)} \tag{4.28}$$

When the analysis of the loop gains are carried out in the following, it is assumed that

1. The power output of the machine and the local load are closely matched.
2. The machine operates at a power factor of 1.0 (due to the choice of the RLC load with unity power factor)
3. The loss of the grid is caused by the tripping of the utility breaker at a moment when the system is operating at steady state.

With these assumptions, the impact of four different factors (power level, load quality factor, motor load and grid impedance) on the proposed AI schemes is investigated.

4.2.3.1Power Level**.** In order to examine the impact of the different power level on the loop gain, the generator active power, which matches the active power of the RLC load (with Q_f =1.8), is varied from 30% to 90%. The Bode plots of the loop gains under different power levels are shown in Figure 4-12.



(i) Active power loop gains **(ii) Reactive power loop gains**

Figure 4-12. Loop gains with different generator output power

((a) (b) (c) Grid-connected 30% power; 60% power; 90% power, (d) (e) (f) Grid-disconnected 30% power; 60% power; 90% power)

Without any compensator, both the active power and reactive power loop gains are much less than 0dB, under both grid connected [cases (a)(b)(c)] and islanded conditions [cases (d)(e)(f)]. The gain below 0dB even when the grid is disconnected [cases (d)(e)(f)] implies that the isolated DG and load system is stable, and thus can be islanded. Results are consistent with the time-domain simulation results in a later section that show, without any compensator, the islanding can be easily sustained.

The loop gains difference between grid-connected [(a)(b)(c)] and islanded [(d)(e)(f)] is due to the system structural change. One has a grid with relatively low impedance. The islanded system has no grid connected, or, equivalently, a grid with infinite impedance.

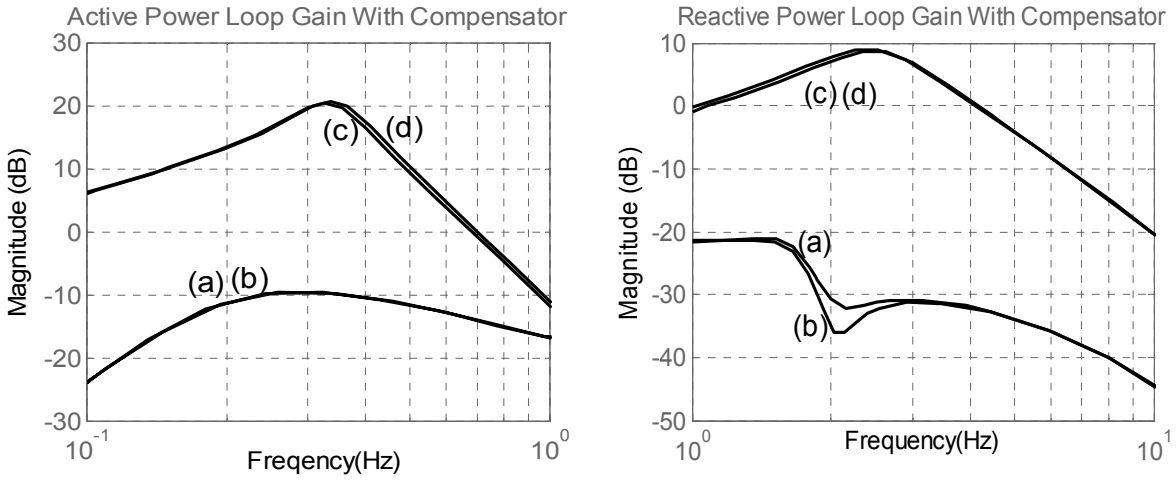
After being compensated, both the active power and reactive power loop gains are reshaped (The bottom two figures in Figure 4-12). The compensator design should be such that, the grid-connected loop gains [cases (a)(b)(c)] are below 0dB in order to keep the system stable, while the islanded loop gains [cases (d)(e)(f)] are above 0dB in order for effective anti-islanding detection. For the purpose of illustration, the peak value of the open loop gain is denoted as G_p and the corresponding frequency is called F_p .Basically G_p and F_p together determine the dynamic characteristics of the AI control. From the design point of view, the larger F_p and G_p , the stronger dynamics of the islanded system. However, there are some fundamental limits on the maxima of G_p and F_p . For the active power AI scheme [Figure 4-12 (i) bottom figure], the limit on F_p is due to the inertia of the DG. In this design, F_p under the grid-disconnected condition is about 0.3Hz. This small F_p indicates the slow response of the active power AI scheme to the loss of the grid. In order to overcome the slow response due to small F_p , a high gain G_p is necessary so that the frequency can be effectively driven out of the normal range for a given time. However, a high gain may potentially cause the DG instability, which sets the upper bound of the loop gain.

From the Bode plot shown in Figure 4-12 (ii) bottom figure, it can be seen that the F_p of the reactive power AI loop gain is around 2.5Hz. In this case, the gain G_p can be lower than the gain for the active power loop gain. This indicates that the reactive power AI scheme can respond faster than the active power AI scheme.

Another observation is that, once the rotating-machine-based DG is islanded, the difference in the loop gain due to the different power levels is insignificant while the previous study has shown that the loop gain of an inverter-based DG is very sensitive to the load power level.

4.2.3.2 Quality Factor**.** The loop gains with the different quality factors, Q_f =0.0 and Q_f =1.8, are compared with each other in Figure 4-13. The quality factor of a RLC load is defined as the ratio of the reactive power stored in the load inductor or capacitor to real power consumed by the resistor. For a load with fixed active power, the different quality factors imply varying the reactive power of the load, i.e., inductance and capacitance. Usually, a load with the quality factor of 1.8 is considered an extreme case for the islanding study. From Figure 4-13, it can be seen that the loop gains vary little with different quality factors for both grid-connected [(a)(b)] and islanded [(c)(d)] conditions. This is again quite different from the case in the inverter-based DG. The fundamental reason is the inertia difference. Generally, Q_f represents the load inertia.

The machine-based DG has large inertia and dominates the overall DG/load system inertia. As a result, different Qf makes little difference in the system dynamics.



(i) Active power loops **(ii) Reactive power loop gains**

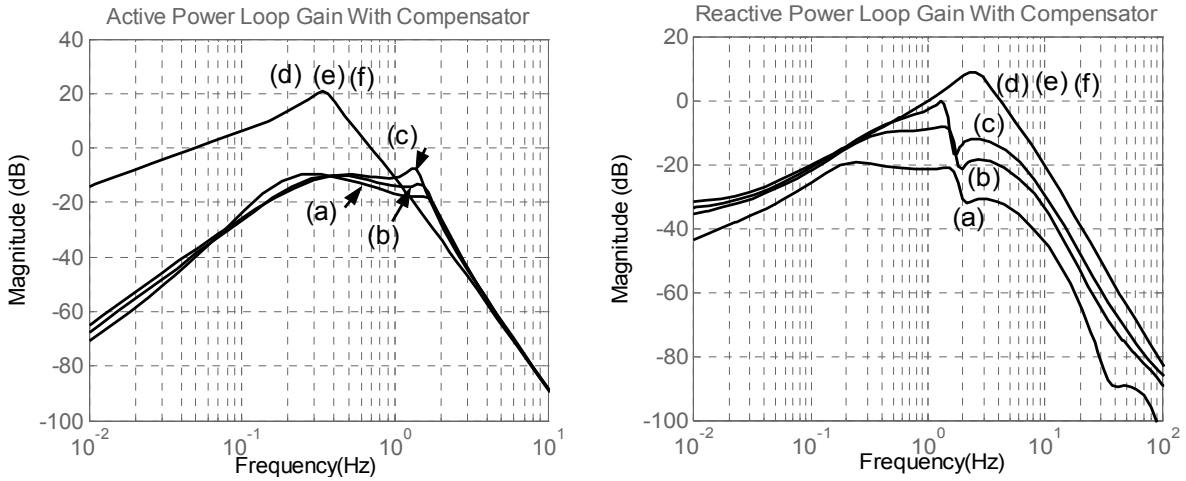
Figure 4-13. Loop gains with different quality factors

[(a) (b) Grid-connected Q_f =0.0 and Q_f =1.8, (c)(d) Grid-disconnected Q_f =0.0 and Q_f =1.8]

4.2.3.3 Grid Impedance. The impact of the AI scheme on the grid stability is also investigated. With different grid impedance, especially high grid impedance (weak grid), the AI schemes may cause stability issue (islanding is actually a special case with infinite grid impedance). Therefore, it is necessary to investigate its impact and specify its application limits.

The active and reactive power AI loop gains have been evaluated for the varying grid impedance from 5% to 40% (on the base of the DG power rating), as shown in Figure 4-14. It can be seen that the grid-connected active/reactive power AI loop gains [cases (a)(b)(c)] increase with the increasing grid impedance. When the grid impedance is approaching 40% (a rare but possible case), the system becomes marginally stable. Another observation is that the reactive power loop gains are more sensitive to the grid impedance than the active power loop gains.

As far as grid impedance is concerned, islanding is actually a special case that has infinite grid impedance. Between the infinite grid impedance (islanded) and finite grid impedance (grid-connected), the active anti-islanding controls always have certain design room by choosing appropriate gain so that their loop gains are separated by 0dB. The higher the grid impedance, however, will result in less design margins. Without sufficient margins, the system may risk instability.



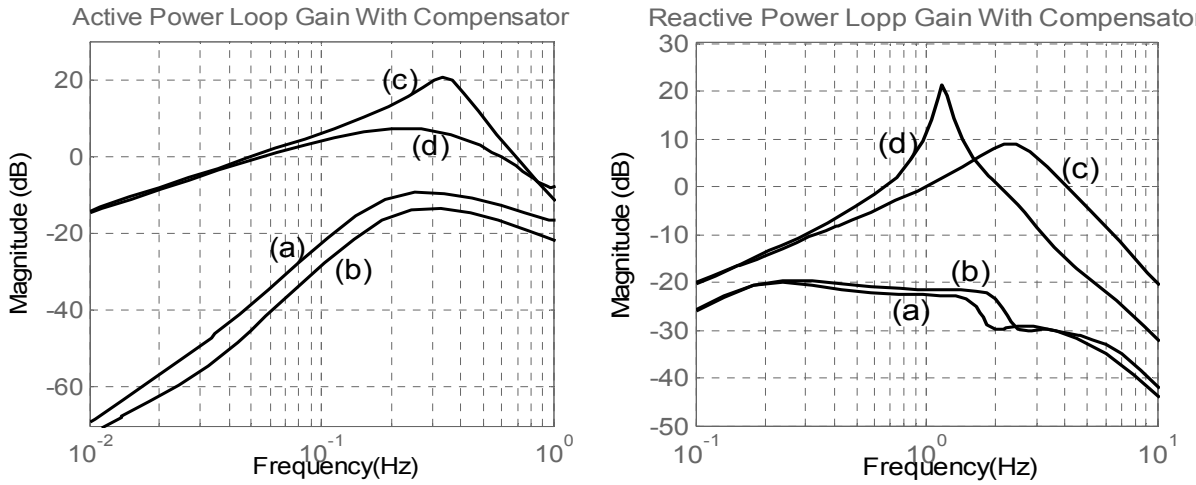
(i) Active power loop gains **(ii) Reactive power loop gains**

Figure 4-14. Loop gains with different grid impedance

[(a) (b) (c) Grid-connected Xe=0.05 p.u.; Xe=0.2 p.u.; Xe=0.4 p.u. (d)(e)(f) Grid-disconnected Xe=0.05 p.u.; Xe=0.2 p.u.; Xe=0.4 p.u.]

4.2.3.4 Motor Load. Induction motors constitute major part of the distribution load. Studies [8] show that the most important sensitivity influencing the system dynamics is the percentage of motors in a feeder. Variations in the motor inertia and impedances are not as great an influence on the system dynamics as the percentage of motors. The effects of the motor load on active/reactive power loop gains are evaluated when the load is composed of an induction motor (H=0.5MW/MVA, Power Rating=150kVA, comparable to the generator rating) and a capacitor for power factor correction.

Figure 4-15 shows the loop gains comparison between RLC load and motor load (with capacitor), both at unity power factor with the same power level. It can be seen that the active power loop gain of the induction motor load [Figure 4-15 (i) ((b)(d)] is lower than the loop gain with the RLC load [Figure 4-15 (i) ((a)(c)]. It implies that the dynamics of the islanded system is slowed down by the induction motor load. In contrast, the reactive power AI scheme is still very effective with the motor load, shown in Fig. 4-15 (ii). It indicates that, the motor load is a worse case than RLC load for the active power scheme. For reactive power scheme, however, the motor load is easier to detect than RLC load.



(i) Compensated active power loop gains **(ii) Compensated reactive power loop gains**

Figure 4-15. Loop gains with RLC and motor load

[(a) (c) Grid-connected/disconnected RLC load(P=0.54 p.u. and Q_f =1.8) (b) (d) Grid-connected/disconnected motor load(P=0.54 p.u., Q=0.34 p.u. and C=600μF)]

4.2.4 Summary

In this section, we have investigated the dependence of the AI loop gains on various factors such as power output of the DG, quality factor, grid impedance, and motor loads. The effectiveness of both schemes is insensitive to power level and quality factor. The active power scheme is less effective with motor load than with RLC load, while the reactive power scheme is effective for both load conditions. When grid connected, the reactive power scheme is more sensitive to the grid impedance than the active power scheme. With the higher grid impedance, the stability margin of the reactive power scheme is reducing quicker than the active power scheme.

4.3 Performance Evaluation with Time-Domain Simulations

In the preceding section, the basic principles and design guidelines of the proposed two anti-islanding schemes have been discussed. In this section, time-domain simulations are carried out using PSCAD to validate the proposed schemes and to evaluate their effectiveness. The parameters of the DG and the load used in the simulations are given in the Appendix. The system used in the simulation consists of the grid, the synchronous generator, and the RLC, or motor loads. A constant voltage source behind impedance is used to represent the grid. The local load and the DG are closely balanced. The loss of the grid is due to the trip of a utility breaker at steady-state and this is considered the worst case for islanding detection.
The performance of the AI schemes is evaluated for both a static load and the induction machine load. For all islanding simulations, the grid is disconnected at t=1s.

4.3.1 Performance Evaluation With RLC Load

4.3.1.1 Case 1: Baseline without AI Scheme**.** Before evaluating the performance of the proposed AI schemes, a baseline case without any AI schemes is simulated, shown in both Figure 4-16 and 4-17. The DG is operating at 88kW (60% of its rated power). The RLC load is 88kW with quality factor Qf=1.8. Since the load and the DG are closely matched, the island can be sustained

after the loss of the grid, because the variation in the frequency and the terminal voltage is so small that any passive scheme may not detect the islanding.

4.3.1.2 Case 2: Active Power Scheme with Qf=1.8. The same DG output and load conditions, but with the active power AI scheme enabled, have been simulated. The simulation results are shown in Figure 4-16 (case 2). After the grid disconnection at t=1s, the frequency drifts quickly (within 2s) to go out of normal ranges [Figure 4-16(b)], while the voltage magnitude almost remains unchanged [Figure 4-16(a)]. Therefore, the active power AI scheme dominates the frequency dynamics, but has little effect on excitation (voltage) dynamics. Figure 4.16(c) shows the field voltage dynamics after islanding. Figure 4-16(d) shows the AI compensator output.

4.3.1.3 Case 3: Reactive Power Scheme with Qf=1.8. Figure 4-17 shows that simulation results with the reactive power scheme is enabled. It can be seen that after islanding, the frequency [Figure 4-17(b)] and the terminal voltage [Figure 4-17(a)] oscillate away quickly. The changes in frequency are caused by the fluctuating active power of the load when the terminal voltage is varying. In this case, the detection of the islanding can be triggered by either under/over frequency or an under/over voltage relay. Figure 4-17(c) shows the field voltage, which is saturated at 2 p.u., but the scheme is still effective.

4.3.1.4 Case 4: Active Power Scheme with Qf=0.0. Figure 4-16 also shows the simulation results for a resistive load only (Q_f=0) (case 4), and with the active power AI scheme enabled. Compared with the simulation results for the load with Q_f=1.8 (case 2), the difference between the variations in the frequency and terminal voltage is negligible. This is well consistent with the analysis in the frequency domain.

4.3.1.5 Case 5: Reactive Power Scheme with Qf=0.0. Figure 4-17 shows the simulation results for a resistive load only (Q_f=0) (case 5), and with the reactive power AI scheme also enabled. Compared with the simulation results for the load of (Q_f=1.8) (case 3), the variations in the frequency [Figure 4-17(b)] and the terminal voltage [Figure 4-17(a)] magnitude are only slightly different. It indicates that Q_f has only a little impact on the reactive power AI scheme. This is also consistent with the analysis in the frequency domain.

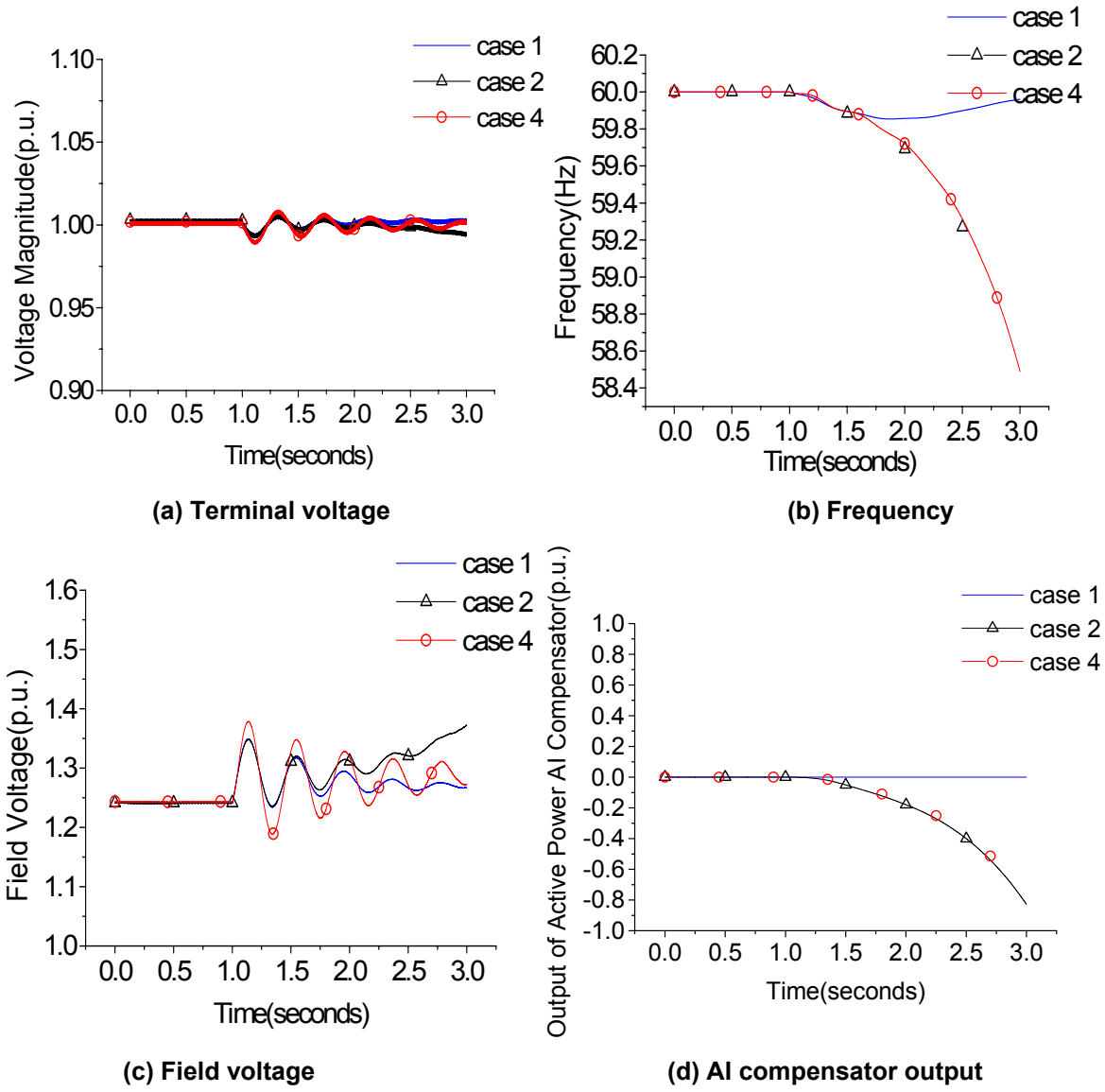


Figure 4-16. Simulation results of the active power scheme in response to islanding at 1s

(Case 1: baseline without AI scheme P=88kW and Q_f=1.8; Case 2: active power AI scheme with P=88kW and Q_f=1.8; Case 4: active power AI scheme with P=88kW and Q_f=0.0)

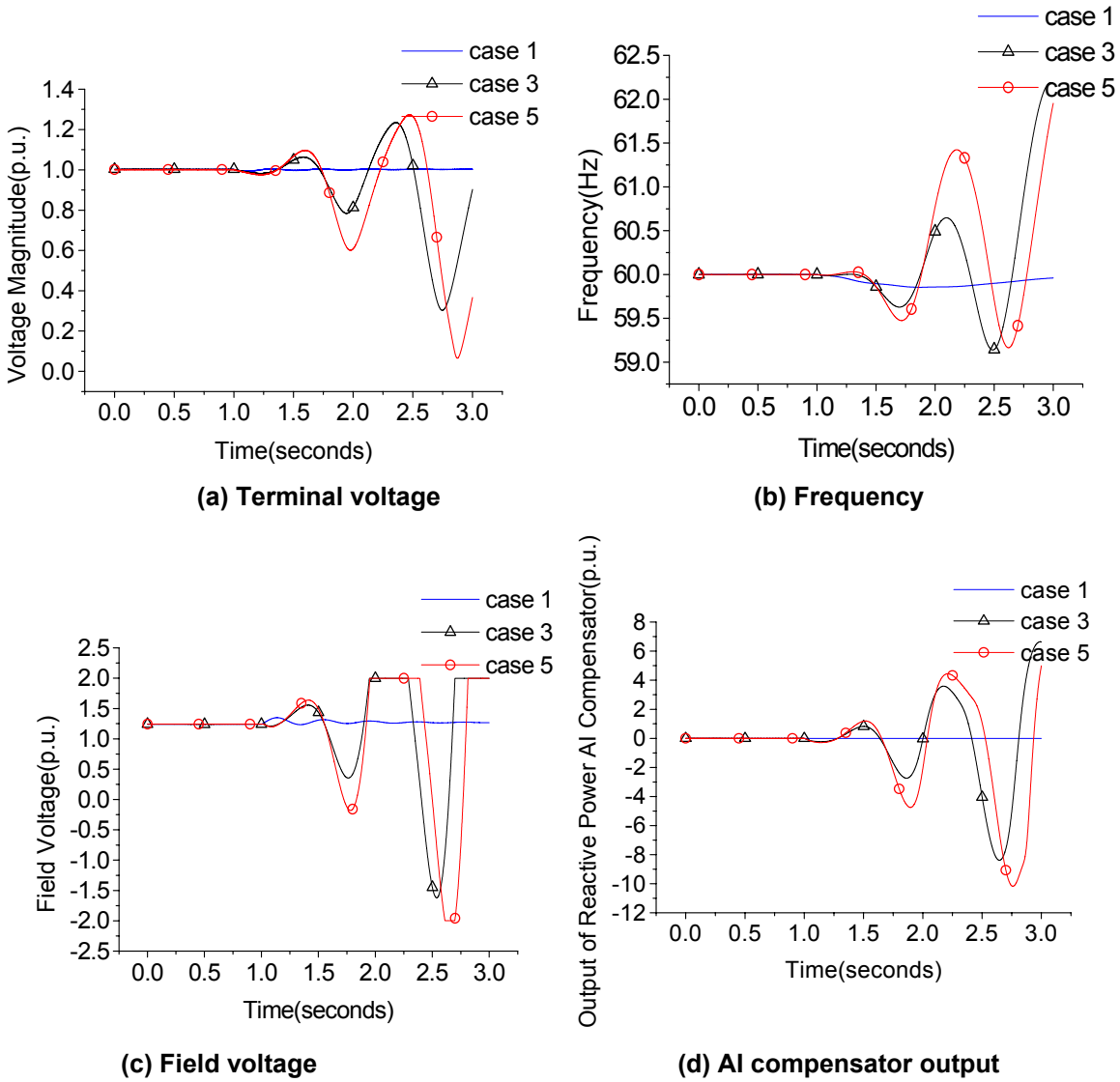


Figure 4-17. Simulation results of the reactive power scheme in response to islanding at 1s

(Case 1: baseline without AI scheme P=88kW and Q_f=1.8; Case 3: reactive power AI scheme with P=88kW and Q_f=1.8; Case 5: reactive power AI scheme with P=88kW and Q_f=0.0)

4.3.2 Performance Evaluation with Induction Motor Load

As indicated in the previous section, motors form a major portion of system loads. Hence, it is important to investigate the motor load impact on the islanding protection. In this study, a generic induction motor is modeled to represent a general population of motors ranging in types from those in small residential/industrial applications to large motors. Studies [8] show that the most important sensitivity influencing the system dynamics is the percentage of motors at the load bus. Variations in the motor inertia and impedances are not as great an influence on the system dynamics as the percentage of motors. Here, the extreme case with 100% penetration of induction motor load (H=0.5MW/MVA, Power Rating=150kVA) is simulated to evaluate its

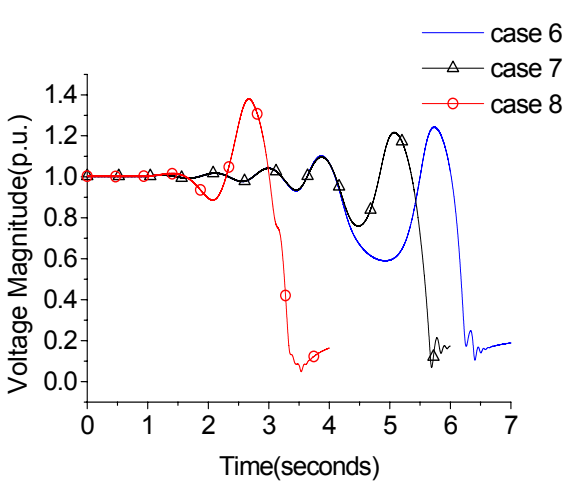
impact on the performance of the AI schemes. In the simulation, a capacitor is connected in parallel to the motor to compensate the reactive power of the induction motor.

4.3.2.1 Case 6: Baseline without AI Scheme and with Induction Motor Load. Before evaluating the performance of the proposed AI scheme for the induction motor load, a baseline case without any AI scheme is simulated, shown in Figure 4-18 (case 6). Since the power mismatch between the generator output and the motor load is very small, the initial oscillation of the islanded system is small and slow. However, the islanded system drastically changes its behavior after approximately 3 seconds of islanding. The voltage magnitude continues to drop so that the islanding cannot be sustained indefinitely.

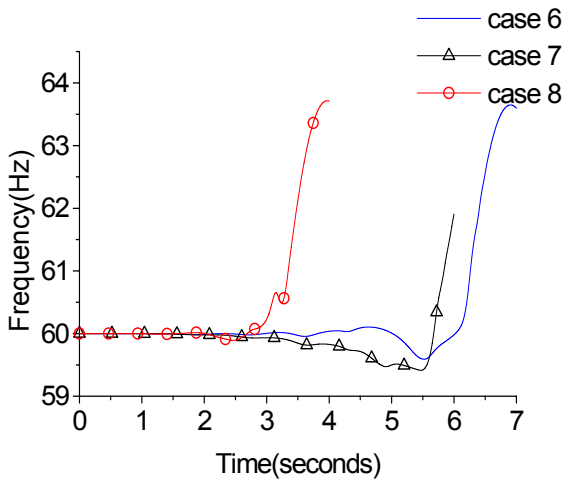
Although the islanded system with the motor load seems to be unstable eventually, the detection of the islanding within 2 seconds is still difficult with the motor load due to its slow response in the first few seconds.

4.3.2.2 Case 7: Active Power AI Scheme with Induction Motor Load. The same conditions have been simulated except that the active power scheme is enabled and the simulation results are also shown in Figure 4-18 (case 7). Compared with the previous simulation results for RLC load, active power AI scheme for the induction motor is not as effective as for the RLC load. In this case, actually, it fails to detect the islanding within a 2-second time window because the voltage and frequency are still within the normal ranges. This is consistent with the frequency-domain analysis.

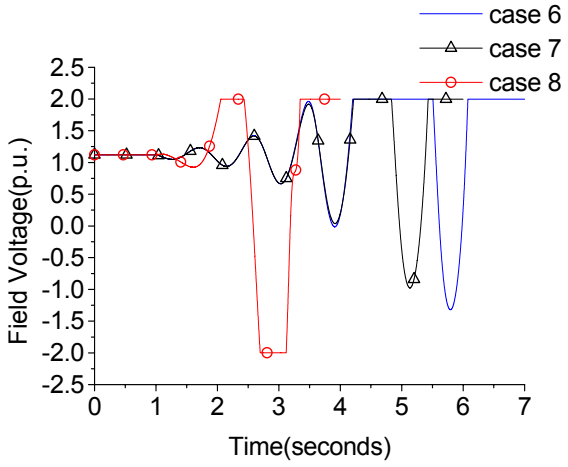
4.3.2.3 Case 8: Reactive Power AI Scheme with Induction Motor Load. The same conditions have been simulated except that the reactive power scheme is enabled and the simulation results are shown in Figure 4-18 (case 8). In this case, the voltage magnitude oscillates dramatically due to the reactive power AI scheme. The islanding can be easily detected by an over-voltage relay. The frequency also drifts away quickly. It concludes that the reactive power scheme is more effective for motor load than the active power scheme. The same conclusion is drawn in the frequency-domain analysis.



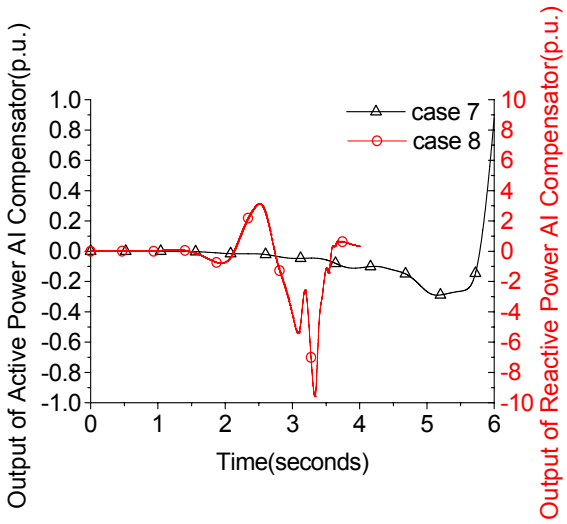
(a) Voltage magnitude



(b) Frequency



(c) Field voltage



(d) AI compensator output

Figure 4-18. Simulation results with the induction motor load in response to islanding at 1s

(Case 6: baseline without any AI scheme for the Induction motor load; Case 7: active power AI scheme for the induction motor load; Case 8: reactive power AI scheme for the induction motor load)

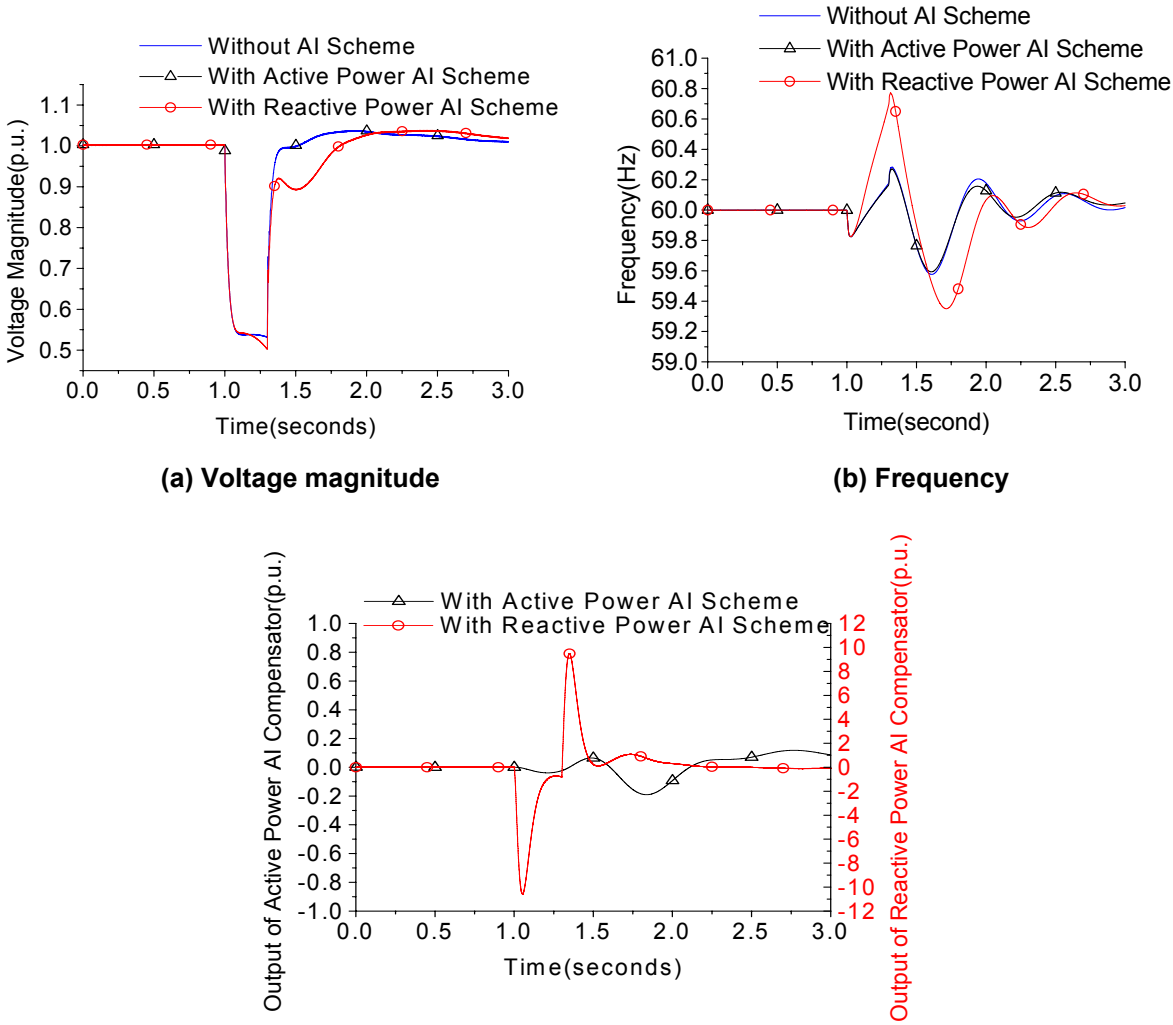
4.3.3 Performance Evaluation When the Grid is Connected

In the preceding section, the anti-islanding control performance of the active power and reactive power AI schemes have been demonstrated. Another major issue related to the performance of the AI schemes is the potential impact on the DG's normal operation under the grid-connected conditions. The following study will simulate a range of situations including oscillation in the

grid frequency, a low voltage event and high grid impedance to investigate whether the proposed AI schemes have a significant impact or not.

4.3.3.1 Grid Disturbances**.** A robust anti-islanding scheme must distinguish between the actual loss of the grid and a grid disturbance. With increasing penetration, distributed generation may become an integral part of the overall power generation system. Therefore, an unexpected tripping-off line from the DG may cause severe impact on the system reliability and stability. One of those disturbances is a transient-low-voltage-event. For some reasons (fault or startup of large motors), the voltage could be lower than the normal ranges for an extended period of time. This is a very difficult situation for any passive schemes to differentiate between the disturbance and the actual islanding.

In the following simulations, the active power and reactive power AI schemes are evaluated under a typical low-voltage-ride-through event. The performance is compared against the case without any AI scheme. A three-phase fault is applied at the high-voltage side of the distribution transformer at t=1s and lasts about 0.3 seconds. The responses of the frequency and voltage from the simulations are shown in Figure 4-19. It is demonstrated that the active power AI scheme is robust and resilient to this low-voltage event. But the impact of the reactive power AI scheme has some negative effect, exaggerating the event when the DG is subjected to a low-voltage event. If widely deployed, this could compromise grid voltage stability following faults.



(a) Voltage magnitude

(b) Frequency

(c) AI compensator output

Figure 4-19. Simulation results of the generator response to a three-phase fault

4.3.3.1 Grid Impedances. There have been concerns over the stability impact caused by the positive feedback schemes, since the grid is not an ideal voltage source. Conceptually, if the gain of the positive feedback is too high or the grid is too weak, the DG may not operate stably due to the AI schemes. Therefore, there always has been the question of what are the stability bounds of the positive feedback schemes. Here the discussion only focuses on the strength of the grid. In the following simulation, the active power and reactive power AI schemes are evaluated under extremely high grid impedance. The case with active power AI scheme has been simulated with a grid impedance Xe=0.5 p.u. (on the base of the DG power rating) and the AI scheme is enabled at t=1.0s. Here the grid is always connected even after 1s. As shown in Figure 4-20(a), the system is dynamically stable when the active power AI scheme is enabled. The case with reactive power AI scheme has been simulated with a grid impedance Xe=0.50 p.u. and the reactive power AI scheme is enabled at t=1.0s. As shown in Figure 4-20(b), the system is dynamically unstable when the reactive power AI scheme is enabled. The high grid impedance causes the reactive power AI loop gain approaches 0dB, thus losing stability margins.

In order to maintain stability (especially transient stability, which imposes more margin requirement than small-signal stability), the design with sufficient margin is necessary. Therefore, for a given design, an upper bound of grid impedance must be specified as an application note, when applying the positive feedback AI schemes.

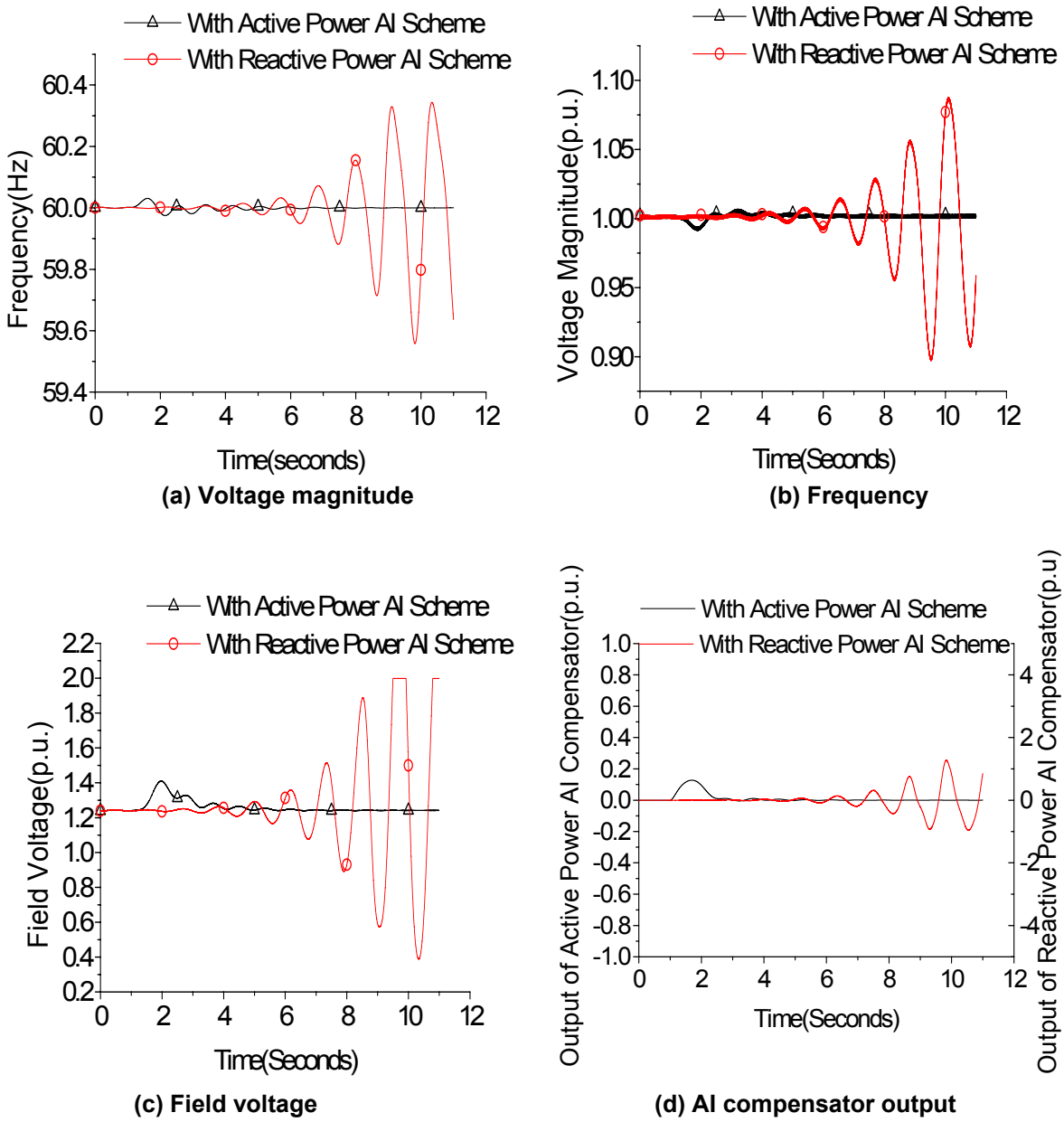
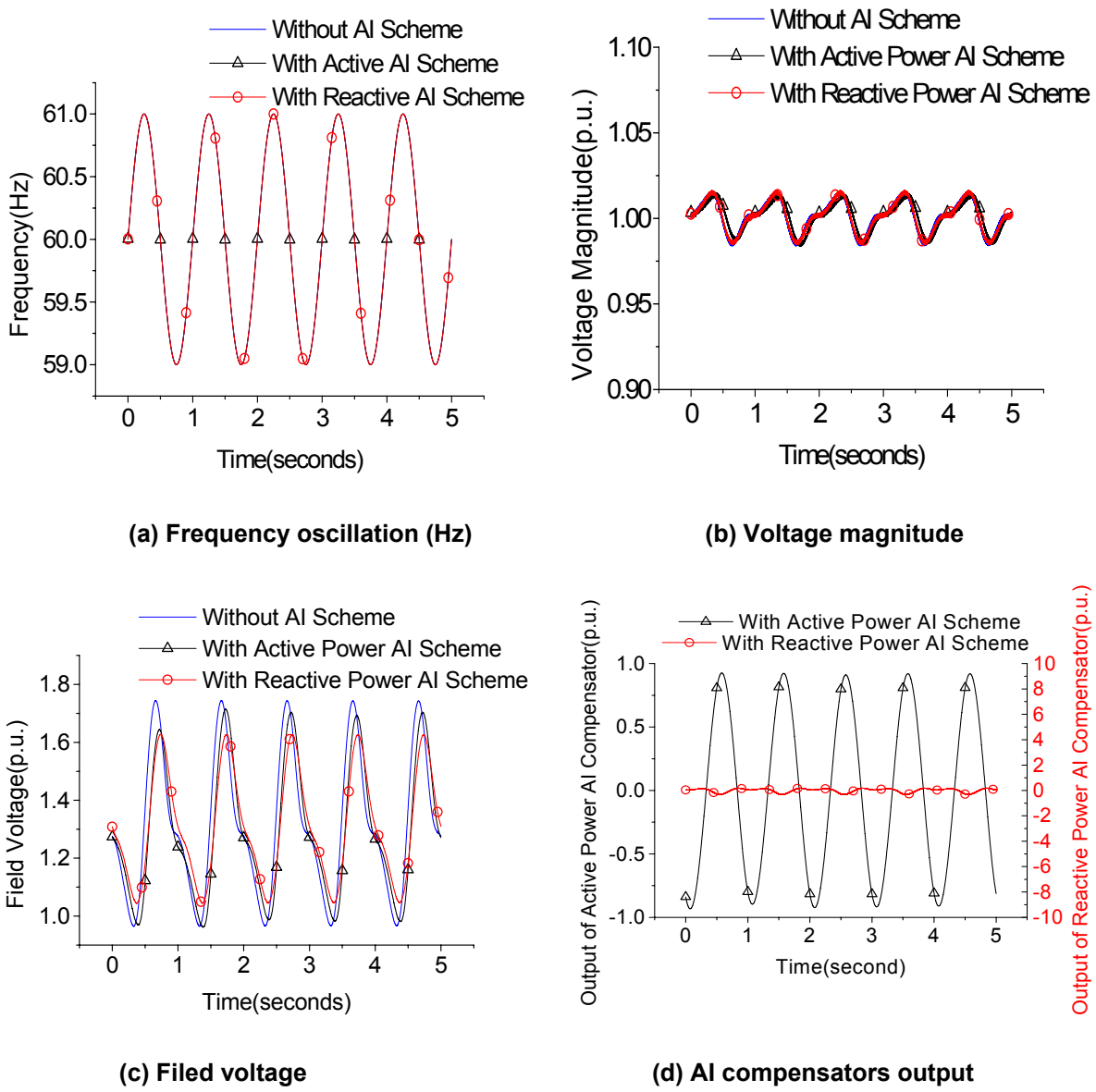


Figure 4-20. Simulation results with high grid impedance

4.3.3.2 Grid Frequency Oscillations.

Another disturbance event to test the performance of the new proposed schemes is a fluctuation in the grid frequency. This variation in the frequency may be attributed to some severe disturbances (faults or loss of a transmission line) occurring in the high-voltage level of the grid. Usually due to the large inertia of the power system, the rate of change of frequency is very low.

One rare case simulated here is that the frequency oscillates between 59Hz and 61Hz at frequency of 1Hz. The simulation results with active/reactive power AI scheme enabled are shown in Figure 4-21. Even tested by so large variations in the frequency, there is little negative impact caused by the active/reactive power AI schemes.



(a) Frequency oscillation (Hz) **(b) Voltage magnitude**

(c) Filed voltage **(d) AI compensators output**

Figure 4-21. Simulation results of the generator response to the grid frequency oscillation

4.4 Summary

This chapter has proposed two new anti-islanding (AI) control schemes, namely active power AI scheme and reactive power AI scheme for synchronous machine-based distributed generations. These DGs include engine generators (diesel, natural gas, biomass, hydrogen) and gas turbines. Detailed discussions and simulation studies, including theoretical analysis and the design guidelines for the new AI schemes, have been covered.

The positive feedback created by the active/reactive power AI compensator will drive the frequency/voltage to be out of the normal ranges once the DG is islanded. One of the outstanding features is that the proposed schemes can show discrimination between actual islanding and other non-islanding disturbances. This is very hard for any passive scheme to achieve. Since the new schemes are designed as part of the DG control, the cost to implement the schemes is basically negligible.

In the first part of this chapter, the characteristics and modeling of the power system using Park's transformation has been covered in considerable details. After that, the positive feedback concept with the principles of the applications has been introduced. With the frequency-domain analysis in MATLAB, the effectiveness of the new active/reactive power AI schemes has been evaluated over a wide range of load conditions. The preliminary study concludes that the reactive power AI scheme is more effective than the active power AI scheme. But the reactive power AI scheme is more likely to cause the DG to be unstable when the grid impedance is very high (very weak grid). The frequency-domain analysis conducted in MATLAB has been validated by the illustrative time-domain simulations conducted in PSCAD. The time-domain simulation also implies that the reactive power AI scheme has a slightly adverse effect when the DG is subjected to a low voltage event.
The preliminary study has discovered the following findings:

1. Without any active schemes, both the RLC load and induction motor load can be islanded for more than 2 seconds without being detected.
2. Both active power and reactive power AI schemes are very effective for RLC load, i.e. detecting islanding within 2.0 seconds even when the power is closely matched between the generation and the load.
3. The impact of different power levels is very insignificant. That is, for a given scheme, it works at full power as well as at partial power.
4. The impact of different quality factor Qf is also insignificant. That is, for a given scheme, it works as effective with a high Qf load as with a low Qf load. This indicates that for synchronous machine based DG anti-islanding testing, a resonant tank (RLC) load is not necessary.[2]
5. Substantial differences in performance were observed for the same anti-islanding scheme (e.g., active power AI scheme) with RLC load and induction motor load. Because induction motors form a large portion of actual loads, these results raise concern that passive load may not be adequate to evaluate the effectiveness of certain AI schemes.
6. The reactive power AI scheme is superior to the active power AI scheme due to its high effectiveness for a high penetration of motor loads. However, the nominal operation of the DG equipped with the reactive power AI scheme can be affected more adversely by the grid impedance and voltage disturbances.

In summary, the new proposed AI schemes for synchronous machine-based DGs are highly reliable, robust to other non-islanding disturbances and easy for implementation.

[2] Latest IEEE P1547.1 testing standard draft is considering to use a simplified load other than RLC resonant tank for testing synchronous machine unintentional islanding protection function.

5 Facility Microgrid

5.1 Introduction

During the past several decades, the North American power grid infrastructure has evolved into four large interconnected networks that are continuously regulated by sophisticated power flow control equipment. These grids are robust to most perturbations, yet their vulnerability is still evident given the magnitude of the August 14, 2003 blackout. Actions need to be taken to reduce stress and congestion on the country's overtaxed transmission and distribution system. Incremental changes to the current grid infrastructure will not achieve the reliability needed in a digital society. New infrastructures or operational concepts need to be explored.

In the DOE's vision of the future electric power infrastructure, "GRID 2030" [9], microgrids (also termed as minigrids in some references) are identified as one of the three major technical cornerstones. Microgrids are envisioned as local power networks that use distributed energy resources and manage the local energy supply and demand. While they would typically operate connected to a national bulk power transmission and distribution system, they would have the ability to pull themselves off the grid and function in an island mode when necessary, thereby increasing the reliability to the local load.

Microgrids are receiving a considerable amount of interests from the power industry partly because of their business and technical structure that shows promise as a means to take full advantage of distributed generations.
Concepts for microgrids fall into two general categories:

- Systems intended to always be operated isolated from a large utility grid
- Systems normally connected to a larger grid.

Conceptually, the isolated microgrid is like a scaled-down version of a large-scale utility grid. Many of the technical requirements are the same. However, there are still distinguishing features mainly due to non-conventional generations contemplated for the anticipated microgrid applications. These features include power electronic interfaces for distributed generation, and intermittent nature of some generation; for example, wind and solar power. In order to supply reliable and quality power, the microgrid must have mechanisms to regulate voltage and frequency in response to changes in customer loads and in response to system disturbances. The penetration of DG in an isolated microgrid is by definition, 100%– all power comes from the distributed generation within the microgrid.

For the grid-connected microgrid, the distinction from the isolated microgrid is the integration and interactions between the microgrid and the bulk grid. The penetration of DG for the grid-connected microgrid could approach or even exceed 100%. The microgrid would be designed and operated such that it presents the appearance of a single, predictable, and orderly load or generator to the bulk grid at the point of interconnection. This arrangement provides several potential advantages for all of the stakeholders:

- DG owners may be able to rate and operate their generation more economically, by being able to export (and import) power to the microgrid.

- The local customers may be able to have continued service (possibly at a reduced level) when connection to the host utility is lost.
- The microgrid could be controlled in such a fashion as to be an active asset to bulk system reliability (for example by providing spinning reserve or black start services, to name two.)
- The host utility may be able to depend on the microgrid to serve local customers in such a fashion that substation and bulk power infrastructure need not be rated (or expanded) to meet the entire load, as if the DG were not present. (This last point is a major, legitimate obstacle to DG.)

The business and regulatory environment presently does not favor (or allow) for multiparty microgrids – those in which power and services are exchanged between third parties over regulated power distribution infrastructure. In fact, in many jurisdictions, interchange of power between adjacent properties, not involving public utility infrastructure, is illegal as a violation of the monopoly franchise granted to the utility. The result of this environment is that individual entities, such as industrial or institutional facilities represent the first generation of microgrids. The entities that turn to DG for their power needs are the 'first adopters' from which industry understanding and best practice can evolve for microgrids. The explorations of microgrids in this report are focused on these single business entity microgrids. For clarity, we have termed this more narrowly defined structure a "facility microgrid".

In this chapter, three key issues associated with facility microgrids are investigated, and they are:
- Facility microgrids with multiple DGs unintentional islanding protection
- Facility microgrids response to bulk grid disturbances
- Facility microgrids intentional islanding.

5.2 Technical Issues

5.2.1 The Definition of Microgrids

Forming a definition for microgrids in the industry has been a difficult and elusive endeavor. Most agree that important elements in the definition of microgrids include geographically co-located power generation sources, energy storage elements, and end-use loads. However, opinions differ concerning the aggregated generation capacity that should be contained within the power system, and whether there should be a single point of common coupling to the main grid, or multiple coupling points. For the sake of this report, our definition is that microgrids are power systems where generation elements are co-located with loads, regardless of the aggregated generation capacity or the grid interconnection. This definition covers a large application space of microgrids ranging from remote rural electrification and residential/community power networks, to commercial, industrial, municipality, hospitals, campuses, and military base power grids. The requirements for each application will also vary largely. Some applications are mainly focused on cost of electricity, e.g., peak shaving. Some applications are focused on local resources usage, e.g., renewables like wind, solar, biomass. Some applications are mainly focused on energy reliability/security, therefore, sophisticated generation and load controls are required.

5.2.2 Interconnectivity

The complexity of the interconnection between a microgrid and the main grid will be affected by the types of power generation elements in the microgrid, the number and location of points of interconnection to the main grid, and the penetration level of microgrid systems to the main grid.

5.2.2.1 Power Generation Types. For a microgrid using conventional generations, such as natural gas or diesel reciprocating engine-driven generators, the system design and engineering is relatively well understood. For many emerging microgrids using alternative energy, such as fuel cells, photovoltaics, microturbines, etc., the system design and integration with the main grid becomes a challenging task mainly due to the lack of experience with those non-conventional generation types.

5.2.2.2 Points of Interconnection. Currently, most grid-connected microgrids have a single point of interconnection with the bulk grid. The interconnection requirements are relatively well defined for the single interconnection point. However, large-scale microgrids and microgrids seeking grid-connected reliability through redundancy may require multiple interconnection points. The coordination of the control and protection will become more complicated as the number of interconnection points increases.

The location of the point of interconnection can also have an impact on the design and performance of a microgrid. If the microgrid is in a remote area, as is the case with some villages and industrial plants for example, the grid can be weak in the sense that voltage and frequency regulation are not tight. In these situations, transient dynamics in the grid can have a significant impact on the system voltage regulation and stability. Additional difficulties can arise when microgrids are connected to a secondary grid network or a spot network. In these situations, the control and protection algorithms will be much more complicated than when connecting to a radial distribution system.

5.2.2.3 Penetration Level, System events such as lightning strikes, equipment failures, and downed power lines are commonplace in the bulk grid. Microgrids are typically expected to respond to these events by tripping offline to protect themselves until the grid recovers. However, if the bulk grid is populated with a multitude of microgrids where several of these entities are net power exporters to the bulk grid, this response behavior could be detrimental. Ideally, the bulk grid would expect the microgrids to cope with, and help recover, from system events. One aspect of this challenging requirement is referred to as low-voltage-ride-through (LVRT) capability. This capability would not only maintain high availability for the microgrids, but would also demonstrate “good citizenship” with the bulk grid by enhancing resiliency.

5.2.3 Intentional Islanding

Although grid-connected microgrids can be designed with the capability for isolated operation, the transition between grid-parallel and stand alone operation can be a challenging task. In some cases, the microgrids will be expected to shut down once the main grid is lost, and then start back up to continue to supply the local loads. The power outage to the local loads could last between seconds and minutes depending on the black-start time of the generation assets within the

microgrids. In many cases, however, a disruption or transient impact to the loads within the microgrids will not be acceptable. For these systems, a seamless transition control is needed. This transition process is called intentional islanding. To prevent the large voltage and frequency transients that follow the loss of the main grid, the intentional islanding control must be capable of maintaining voltage and frequency regulation while exhibiting fast transient disturbance rejection qualities. The DGs must be able to support transient and temporary currents, which are far in excess of the connected load demand, due to magnetizing inrush and motor dynamics. Intentional islanding will be one of the most significant challenges for making grid-connected microgrids an attractive solution for high-reliability customers.

5.3 Objectives

In most applications, multiple distributed generations will be used in a facility microgrid. Similar to the requirement for a single DG, the facility microgrid is required to detect unintentional islanding and isolate itself from the host utility at the point of common coupling. Most anti-islanding protection and control schemes are developed and tested for a single DG, isolated from other DGs. When multiple DGs operate in parallel, the interactions and effects on the overall detection at PCC are not fully investigated. One example is the impedance detection scheme. The scheme requires a current signal injection, terminal voltage measurement, and then calculating the impedance. The islanding can be detected by monitoring the impedance changes. When multiple DGs with the same scheme operate in parallel, the measured voltage may be diluted to result in no impedance change under islanding condition. To avoid this, all DGs should be synchronized with their injection signals. Synchronizing the injection signals may be, however, impractical for two reasons: 1) it discourages plug-and-play autonomous operation approach due to the synchronization link, and 2). unless the DGs are from the same vendor, the injection signals for different DGs will be different at frequencies or magnitudes, which make the dilution effect to be more unpredictable.

Active anti-islanding control is another approach commonly used for DG. The interaction among the multiple DGs with active anti-islanding control is not fully explored. Therefore, the first objective is to investigate the interaction and effectiveness of the anti-islanding protection for multiple DGs with proposed GE active anti-islanding controls. The cases with both multiple inverter-based DGs and multiple machine-based DGs will be investigated. Recommendations of applying the GE schemes to multiple DGs will be made.

The facility microgrid will normally be connected to the host utility (macrogrid, or Area EPS). Depending on the design and operation philosophy, as well as the contractual arrangement with the host utility, the facility microgrid is most likely to rely on the host grid for a portion of its power, with the balance being generated by the DG imbedded in the microgrid. One issue of the facility microgrids is that they will be subject to host utility disturbances. The response of the facility microgrid will in turn affect the host utility dynamics. The second objective is to explore these dynamics.

One of the most attractive aspects of a facility microgrid is the potential for the facility to separate, or island, from the grid. In the simplest sense, this provides a higher level of reliability for the facility than can be obtained from reliance on the grid alone. This extra reliability is often the primary motivation for considering individual applications of DG, and it easily expands to

the microgrid. In order to realize these potential benefits, the DGs in the microgrid must have, at the least, additional controls. The third objective is to investigate the facility microgrid system intentional islanding behaviors and control strategies.

5.4 Facility Microgrid Unintentional Islanding Protection

Typically, a facility microgrid will have multiple distributed generators. The unintentional islanding protection developed for a single DG may not work properly with multiple DGs operating in parallel. This section will investigate the effectiveness of the active anti-islanding control that is developed for a single DG, when applied to multiple DGs. The combination of multiple DGs includes: multiple inverter-based DGs, multiple machine-based DGs, and multiple inverter- and machine-based DGs.

5.4.1 Multiple Inverter-Based Distributed Generations

There are two typical schemes used for inverter-based DG, as discussed in Chapter 2. One is active voltage scheme, the other is active frequency scheme.

For demonstration and simplification, two inverter-based DGs with same ratings are used to illustrate the effect of multiple DGs parallel operation. The conclusion drawn from the study can be extended to more than two DGs, and with different ratings.

The studies are carried out in PSCAD. The overall system includes two inverters with impedance between RLC load and grid with impedance.

Prior to the islanding, the inverters total output is well balanced by the load. i.e., zero power exchange with the utility. This constitutes the worst case for islanding detection, although in most practical cases, islanding occurs after faults. Seven cases, as defined in Table 5.1, were simulated. Figure 5-1 shows the simulation results.

Table 5-1 Case Studies for inverter-based DGs

	DG1		DG2		Line Impedance between DG	
	Voltage Scheme	Frequency Scheme	Voltage Scheme	Frequency Scheme	Resist. (p.u.)	Induct. (p.u.)
Case 1					0.0	0.0
Case 2	Enabled	Enabled			0.0	0.0
Case 3	Enabled			Enabled	0.0	0.0
Case 4	Enabled		Enabled		0.0	0.0
Case 5		Enabled		Enabled	0.0	0.0
Case 6	Enabled		Enabled		0.0	0.2
Case 7		Enabled		Enabled	0.0	0.2

Case 1 is the base case. Both inverters have no active anti-islanding control enabled. It can be seen from Figure 5-1 that the voltage and frequency stay within nominal ranges after islanding.

In Case 2, only one DG has active anti-islanding control. The other DG has no anti-islanding control. Figure 5-1 shows that the voltage and frequency are also within nominal ranges after islanding. That means, the overall system, including the DG with anti-islanding control, will fail the unintentional islanding detection within the required time.

In Case 3, one DG has only the voltage scheme, the other DG has only the frequency scheme. The detection is also failed.

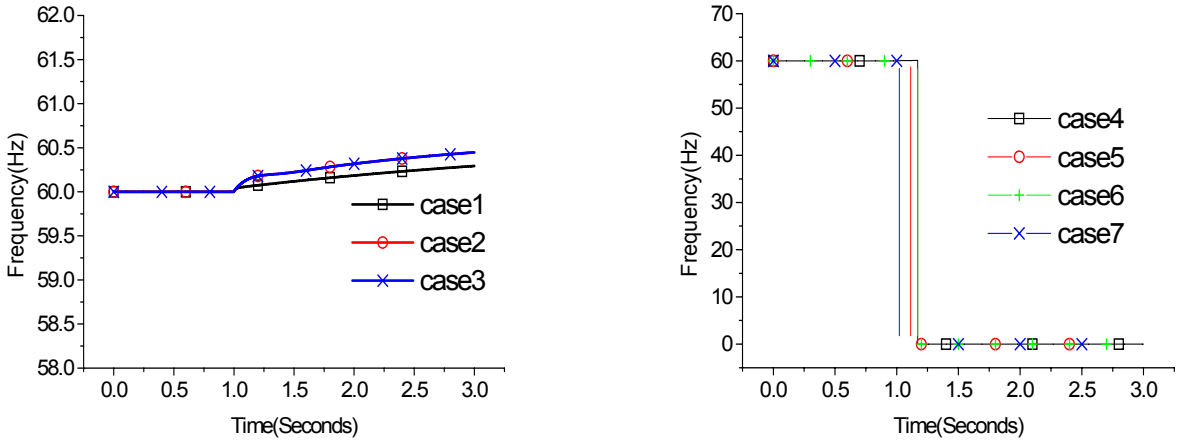
In Case 4, both DGs have the same voltage scheme and the unintentional islanding can be successfully detected.

In Case 5, both DGs have the same frequency scheme and the unintentional islanding can be successfully detected.

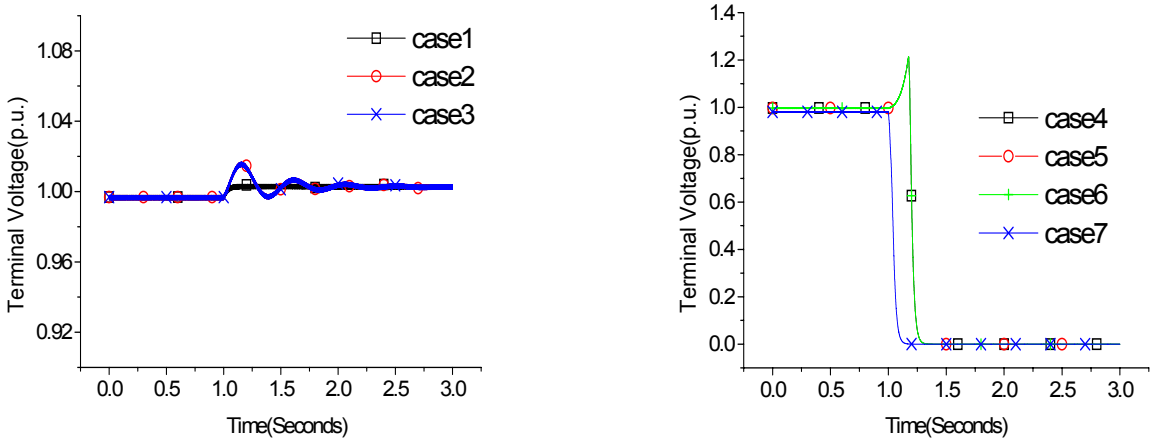
Case 6 and 7 are similar to Case 4 and 5, respectively, except that there is an impedance between the two DGs point of common coupling. For Case 1 through 5, the two DG are directly connected at their terminals without any impedance in between.

The takeaways from the simulations are:

- When both DGs are equipped with the same anti-islanding control, the unintentional islanding can be detected successfully.
- When multiple DGs with the active anti-islanding control operate in parallel, the impedance (up to 0.2 pu simulated) between the DGs terminals has little effect on the schemes. This indicates the geographical separation of the DGs within a microgrid is insignificant as far as the active anti-islanding protection is concerned.
- Even though each scheme works for a single DG, the unintentional islanding detection may fail when some DGs have no active anti-islanding control, or use different schemes. This phenomenon can be analyzed and explained using Middlebrook Extra Element Theorem [10]. Detailed analysis is not presented in this report. The basic concept is that, one DG's active anti-islanding control loop gain can be reduced by another DG that has no active anti-islanding control. If the loop gain is reduced significantly enough, the anti-islanding control becomes ineffective, thus the overall parallel DGs are not able to detect the islanding.



(a) Frequency (Hz) in response to the islanding at t=1.0s



(b) Terminal voltage (p.u.) in response to the islanding at t=1.0s

Figure 5-1. Simulation results in PSCAD for two inverter-based DG system

5.4.2 Multiple Machine-Based Distributed Generations

Figure 5-2 shows the anti-islanding controls for a synchronous-machine-based-distributed generation. There are two schemes that can be implemented for machine-based DG, as discussed in Chapter 4. One is active power scheme, programmed as part of the governor control. The other is reactive power scheme, programmed as part of the excitation control.

Similar to inverter case studies, two machine-based DGs are used to illustrate the effect of multiple-machine DGs parallel operation. The simulations were carried out in PSCAD. Table 5.2 shows the simulation cases. Figure 5-2 shows the simulation results for all cases.

Table 5-2. Case Studies for machine-based DG

	DG1		DG2	
	Active Power Scheme	Reactive Power Scheme	Active Power Scheme	Reactive Power Scheme
Case1				
Case2	Enabled			
Case3		Enabled		
Case 4	Enabled		Enabled	
Case 5		Enabled		Enabled

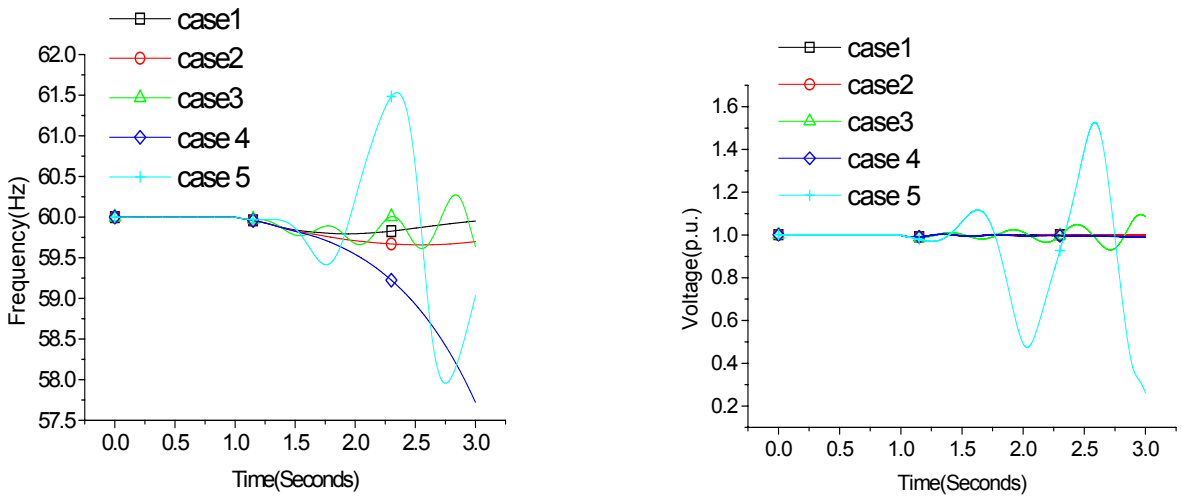


Figure 5-2. Simulation results in PSCAD for the interconnection of two machine-based DG systems

(a) Frequency in response to the islanding (b) Terminal voltage in response to the islanding

The takeaways from the simulations:

- Similar to the case with inverter-based DGs, when both machine-based DGs are equipped with the same anti-islanding control, the unintentional islanding can be detected successfully, as in Cases 4 and 5.

- Also similar to the case with inverter-based DG, even though each scheme works for single DG, the unintentional islanding detection may fail when some DG does not have the same active anti-islanding control, as in Cases 2 and 3.

5.4.3 Multiple Inverter-Based and Machine-Based Distributed Generations

The mixture of inverter-based DG and machine-based DG presents a design challenge for any anti-islanding scheme. With the penetration of distributed resources continuously increasing, this situation will become common, and the performance of the AI protection must be tested in this context. This mixture condition has not yet been explored extensively. First of all, the interactions between inverter-based DG and machine-based DG in the island are unknown. Secondly, existing active anti-islanding schemes have been developed assuming either machine-based DG only or inverter-based DG only. The schemes for machine-based DG and inverter-based DG are not necessarily compatible due to their different mechanisms. The distinct feature of active schemes is a positive feedback that breaks down the active and/or reactive power balance to cause voltage and/or frequency trips. This mechanism must be preserved and unaffected when multiple DGs with different types and power ratings are operating in parallel. Based on this principle, the most effective combination is to have the inverter apply the frequency scheme, and machine apply the reactive power scheme. This combination will lead to effective islanding detection. The other combinations are not as effective, as indicated by simulation studies. Figure 5-3 shows the simulation results with the inverter equipped with the frequency scheme, and the machine equipped with the reactive power scheme. Once islanded, both frequency and voltage of the inverter/machine/load system drift away quickly, so that under/over frequency/voltage relay will detect the islanding.

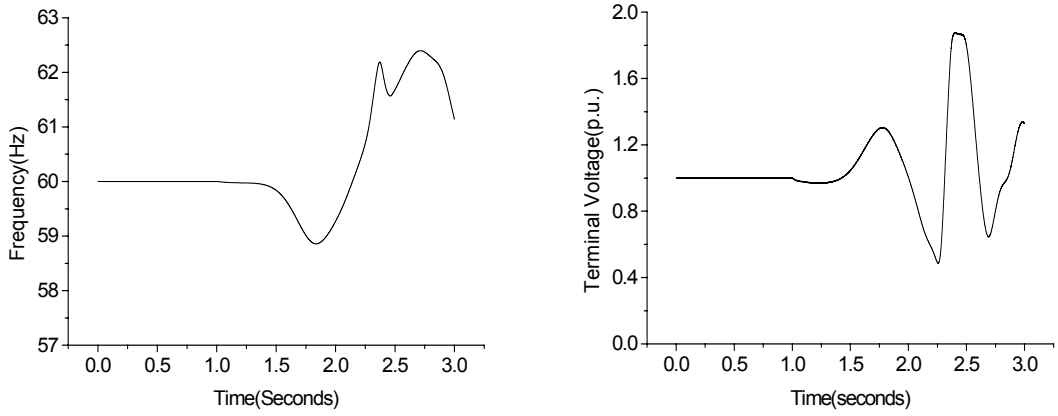


Figure 5-3. Islanded system frequency and voltage with mixed inverter and machine DGs

5.4.4 Summary

This chapter has investigated the performance of the active anti-islanding schemes when applied to multiple DGs. Three combinations of the DGs have been studied, including multiple inverter-based DGs, multiple machine-based DGs, and the mixture of the inverter- and machine-based DGs. The effective strategies that ensure islanding detection have been identified. The strategies are depicted below:

1. If a facility microgrid is comprised of only the inverter-based DGs, the anti-islanding schemes applied to every DG should be the same, either the active voltage AI scheme or the active frequency AI scheme. By doing so, they can be designed and operated independently. No communication link is needed.

2. If only the machine-based DGs are present in an island, each DG should be designed with the same AI scheme, either the active power AI scheme or the reactive power AI scheme. This way, they can be designed and operated independently

3. .If the inverter-based DGs are mixed with machine-based DGs, each inverter-based DG should be equipped with the active frequency AI scheme while each machine-based DG should be equipped with the reactive power AI scheme. With this combination, the DGs can be designed and operated independently.

Beyond the context of planned microgrid applications, these results raise substantial concern regarding the current DG anti-islanding performance and qualification testing standards specified in IEEE 1547 and UL 1741, when multiple DGs are installed to an Area EPS circuit. Both of these standards provide for testing of anti-islanding performance on a single-unit basis. The results just described imply that, unless the anti-islanding protections of the separate DGs are compatible and coordinated, the current standards do not protect the grid and its customers from potentially damaging and dangerous islanding situations.

5.5 Facility Microgrid Fault Event Case Studies

The facility microgrid will normally be connected to the host utility (macrogrid, or Area EPS). Depending on the design and operation philosophy, as well as the contractual arrangement with the host utility, the facility microgrid is most likely to rely on the host grid for a portion of its power, with the balance being generated by the DG imbedded in the microgrid. One class of dynamic impact of immediate concern is the potential for microgrids to alter the local dynamics of a specific subsystem or distribution feeder. This becomes a concern when there is a significant penetration of the microgrids relative to the total load power on that feeder.

5.5.1 Facility Microgrid System Description

A relatively simple facility with a variety of loads and DG was used for investigation of facility microgrid dynamic behaviors.

A one-line diagram of the system, showing the loads, DGs, and power flow for the base condition is shown in Figure 5-4. It includes most basic distribution system components expected to be important for investigation of fundamental frequency performance issues

The facility has a main 13.8kV service bus, with multiple laterals serving individual blocks of load. The loads are a variety of motors, with different dynamic characteristics. The facility connects to a host utility at a point-of-common coupling (PCC) at 115kV. The 115kV system is greatly simplified, with two equivalent lines leading to an equivalent hub node. Two individual 6 MVA DGs are connected to main facility bus through individual transformers. The model, while simple, is suitable for investigation of the performance of microgrid applications.

The line and transformer impedances for the system are shown in Figure 5-5. In the figure, reactances appear below the line and are given on a 100 MVA base. Each bus is labeled with a name, node number, the initial voltage in p.u., and the initial voltage in kV. Circles with 'm' are motors.

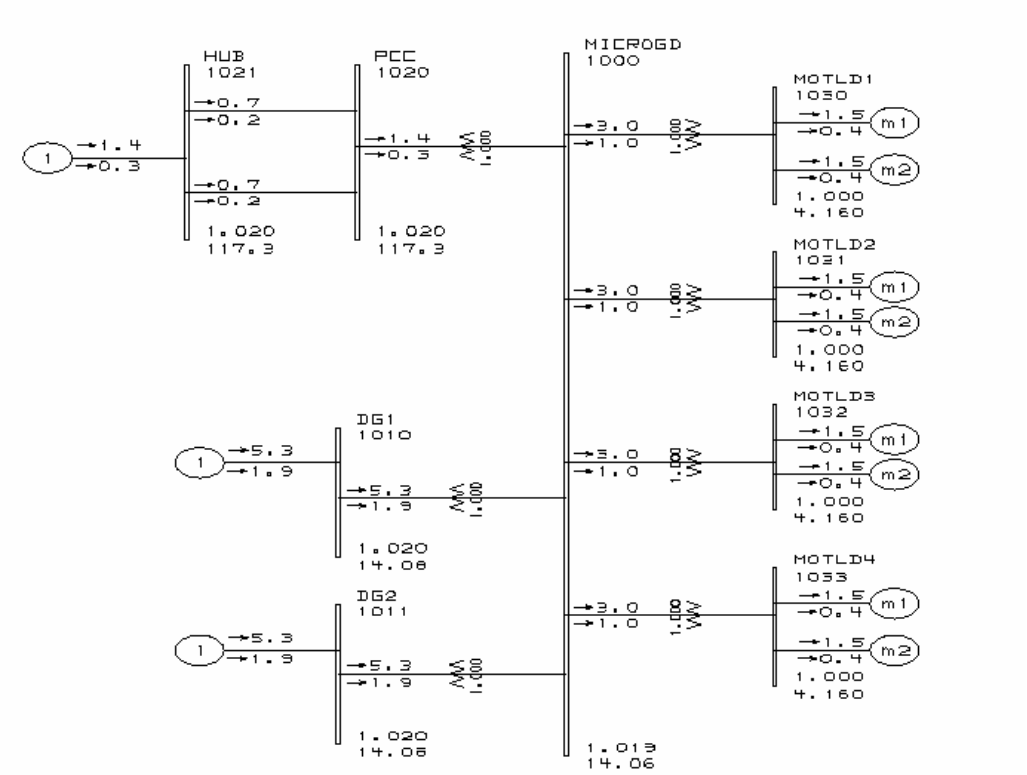


Figure 5-4. One-line diagram of the facility microgrid – active and reactive power flows

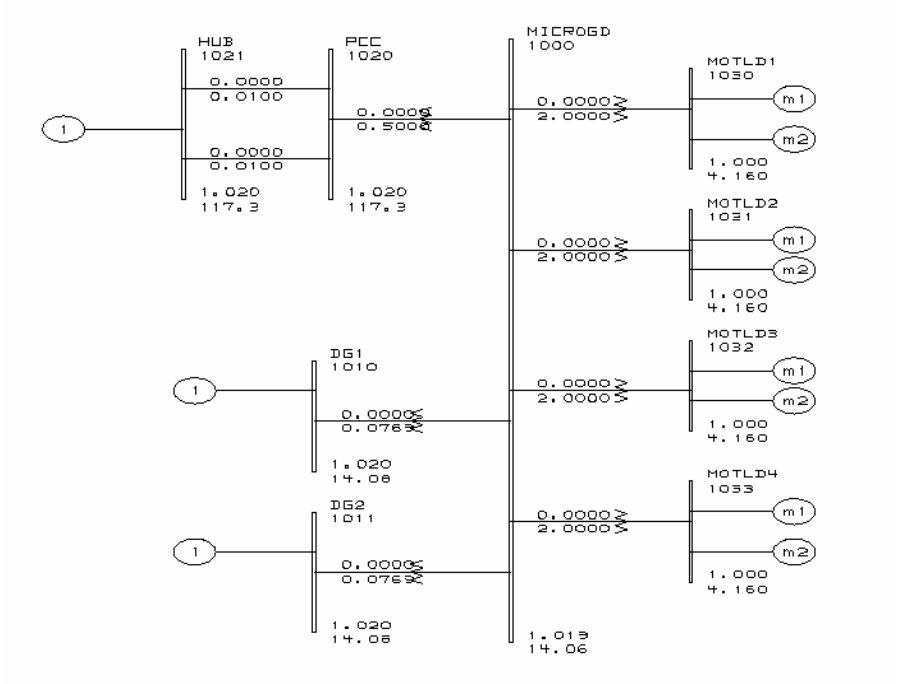


Figure 5-5. One-line diagram of the facility microgrid – network impedance

5.5.2 Case Studies

The initial condition for disturbances studied here is with some power imported, as shown in Figure 5-4. In this case, about 10% (1.4 MW) of the facility power is imported.
Figures 5-6, 5-7, 5-8, and 5-9 show the response of the facility microgrid to a fault on the host system. The event simulated is a fault at the midpoint of one of the two 115kV lines from the point of common coupling to the system equivalent hub. The fault is cleared by removal of the faulted line, which leaves the connection of the microgrid to the host system weakened.
Each of the four figures shows a different system variable for this event. In each figure, there are five traces showing different DG technologies and controls. In the context of this chapter and the next chapter, the active anti-islanding controls discussed in the previous chapter are not used for the DGs.
For each figure the five traces correspond to:

- Dark Blue: No DGs, only loads are presented in the facility.
- Pink: Inverter-based DG with full controls (voltage and frequency regulation with droop).
- Red: Machine-based DG with full controls (conventional voltage regulator/excitation and frequency regulation/governor, both with droop)
- Light Blue: Inverter-based DG with power dispatch (passive) mode (no voltage and frequency regulation)
- Purple: Machine-based DG with power dispatch (passive) mode (no voltage and frequency regulation).

Figure 5-6 shows the voltage at the motor loads within the facility. Figure 5-7 shows the active power exchange between the facility microgrid and the host macrogrid. Figure 5-8 shows the speed of some of the motors in the facility. Figure 5-9 shows the current drawn by the loads.

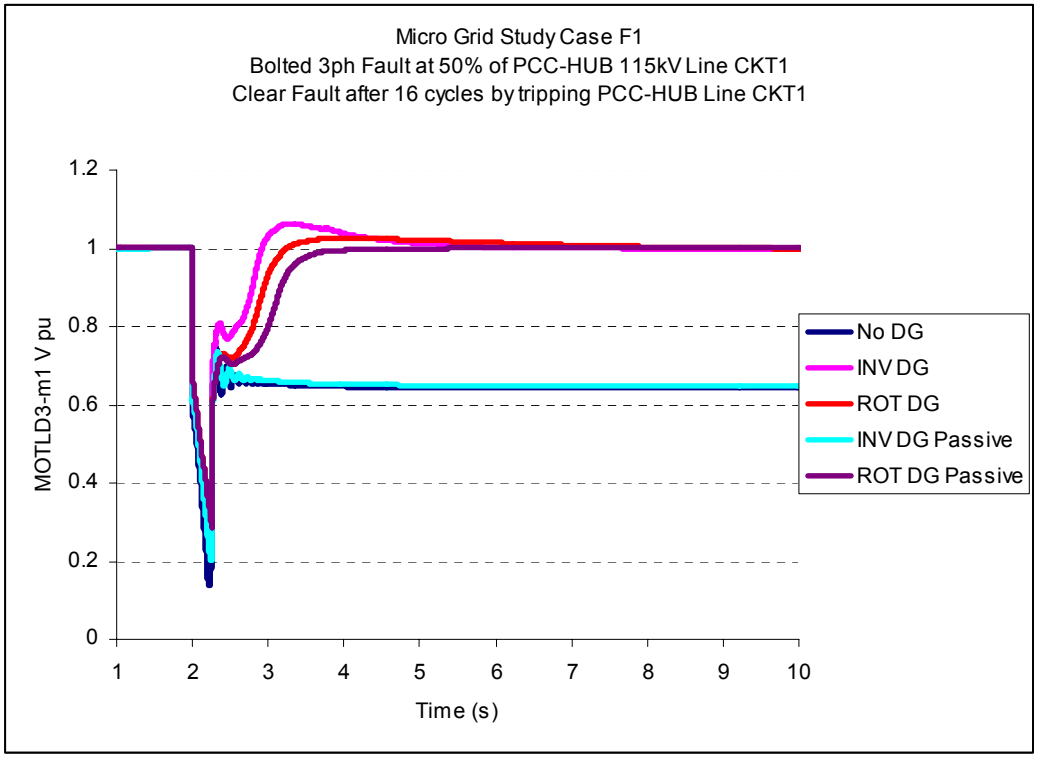


Figure 5-6. Microgrid load bus voltage – following non-islanding grid disturbance

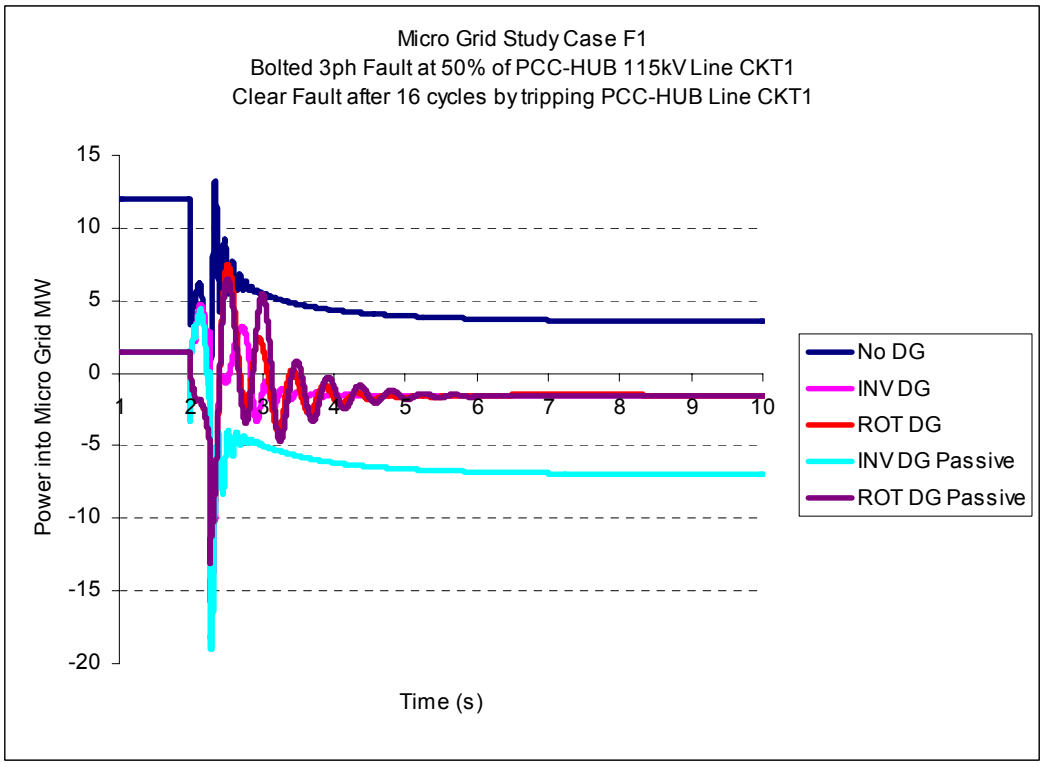


Figure 5-7. Active power into microgrid – following non-islanding grid disturbance

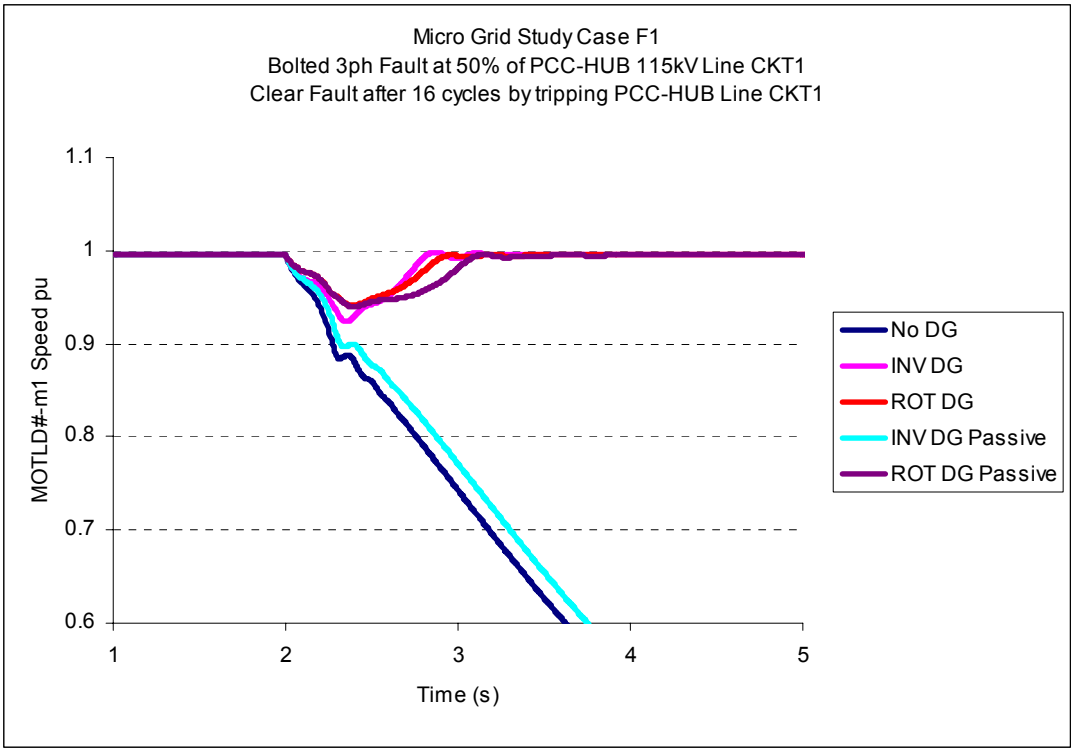


Figure 5-8. Microgrid load motor speed – following non-islanding grid disturbance

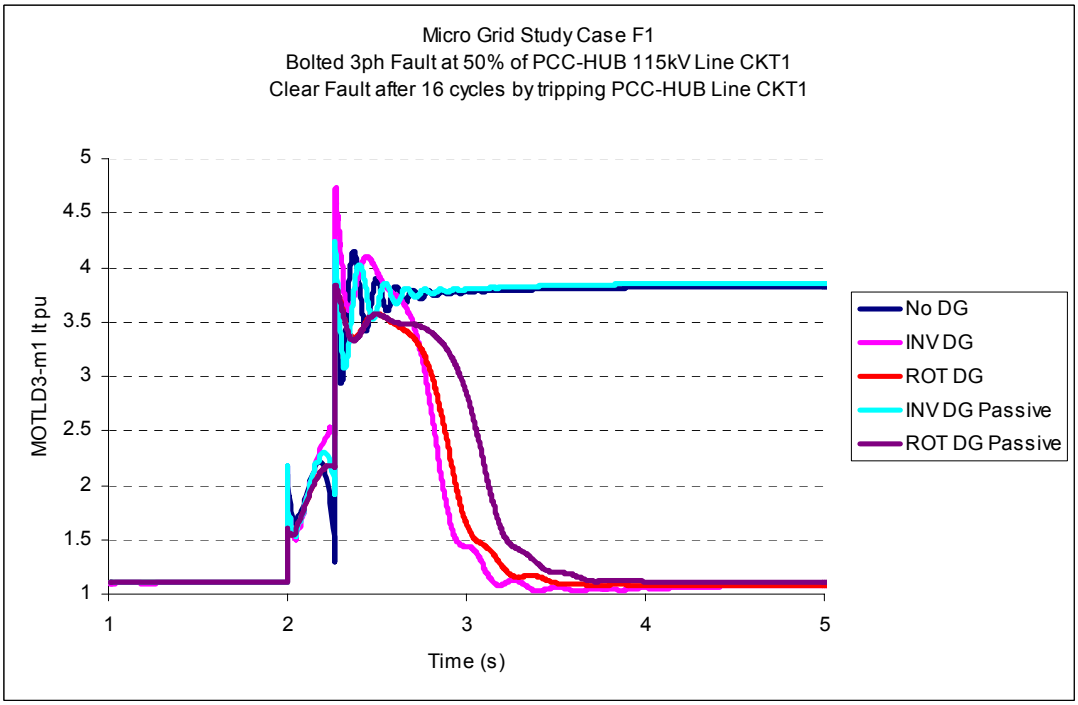


Figure 5-9. Microgrid load current – following non-islanding grid disturbance

5.5.3 Observations

There are a number of observations to be made from these cases:

- The most important observation is that the behavior of the system is significantly different for each set of assumptions. The cases with no DG and with the power dispatch (passive) mode inverter-based DG fail to recover from the fault – that is, the load in the facility is disrupted, and the facility would likely trip some or all of its load and DG. The collapse of the motor speed is graphic evidence of the failed recovery – the motors have stalled and in the process have collapsed the voltage. As a result of the collapsed voltage, the motors cannot restart, and so neither can the voltage recover.

- This failed recovery is not only disruptive to the microgrid load, it is also disruptive to the host grid. This is evident in the high currents drawn after the load stalls. This could cause false trips of protective relaying, and possibly result in outage of other customers on the host grid. Addition of controls (voltage and frequency droop regulation mode) for both types of DG allows a successful recovery, and all parties benefit.

- The presence of DG in the microgrid with appropriate controls can be beneficial to both the microgrid (DG owner) and to the grid. (The No DG case failed.)

- The machine-based DG with dispatch mode was more benign than the inverter-based DG with dispatch mode. This may be due to the inherent mechanical (and magnetic) inertia of the machine that may make recovery naturally friendlier. Conversely, the best performance results from the inverter-based DG with full control (voltage and frequency regulation). ('Best performance', based on fastest recovery to normal voltage and speed). This is not surprising in that the inverter-based technologies are more controllable and are more dependent on good control – these are different faces of the same nature of the equipment.

5.6 Facility Microgrid Intentional Islanding Case Studies

5.6.1 Intentional Islanding Needs

One of the most attractive aspects of a facility microgrid is the potential for the facility to separate, or island, from the grid. Although the microgrid can be designed with the capability for isolated operation, the transition between grid-parallel and standalone operation can be a challenging task. In most applications, the microgrid will be expected to shut down once the main grid is lost, and then start back up to continue to supply the local loads. The power outage to the local loads could last between seconds and minutes depending on the black-start time of the generation assets within the microgrids. In some cases, however, a disruption or transient impact to the loads within the microgrids will not be acceptable. For these systems, a seamless transition control is needed. This transition process is called intentional islanding. Although islanding allows the microgrid to recover, the microgrid will be exposed to voltage deviations caused by grid faults before islanding can be accomplished. Therefore, a grid-connected microgrid cannot be viewed as a means of providing disturbance-free performance, but a microgrid can provide a means to improve power supply availability for critical loads. Loads subject to transient voltage disturbances, e.g., a data center, will still need a UPS (uninterruptible power supply device) to ride grid disturbances, but the amount of energy storage in the UPS can be reduced if this load is supplied by a microgrid.

Intentional islanding can be pre-planned or unplanned. Unplanned intentional islanding imposes much greater challenges than pre-planned intentional islanding. First of all, the loss of the main grid must still be detected, the same functionality as unintentional islanding protection. Secondly, to prevent the large voltage and frequency transients that follow the loss of the main grid, the intentional islanding must be capable of maintaining voltage and frequency regulation while exhibiting fast transient disturbance rejection qualities. Thirdly, the islanded system will impose very large transient currents on its generation due to magnetic inrush when the microgrid is isolated from the faulted grid. (These highly distorted currents are not simulated in the power frequency simulations discussed here, but need to be addressed when an actual microgrid is designed.)

Different levels of power balance (power import/export from the bulk grid) impose different challenges for unplanned intentional islanding. The case with closer power balance (minimal power import/export) is a worse case for loss of grid detection, but is a better case for smooth transition from grid-connected to islanded mode. The case with large power imbalance (large power import/export at PCC), however, is a better case for loss of grid detection, but a worse case for transition due to large transient.

The ability of a microgrid to survive loss of connection to the host utility depends on a number of factors. The microgrid must have sufficient dynamic regulating capability to be able to tolerate the change in both active and reactive power flow that will result from loss of the utility tie. This means at least some of the DGs must have both voltage and frequency regulation functions. If the microgrid imports power from the main grid, once islanded, not all of the load within the facility can be supplied. In this case, non-essential load (can be pre-defined) must be disconnected to allow for continued secure operation of the remaining critical load. The ability to differentiate between critical and non-critical load is a major reliability consideration and potential advantage in a facility microgrid.

5.6.2 Case Studies

This section examines the facility microgrid behavior under islanding events. The events are unplanned and followed by system faults that cause loss of main grid. These kinds of events are most common. The facility microgrid system is the same as in Chapter 3.

Figures 5-10 through 5-14 show the response of the facility microgrid to faults at the PCC that result in trip of the microgrid from the host system. The events simulated are faults at the terminal 115kV PCC cleared by removal of the microgrid main transformer. In one pair of cases, the fault is bolted (i.e., has no fault impedance) and is therefore, more severe than the second pair of cases, in which some fault impedance is assumed.

Each of the five figures show a different system variable for this pair of events. In each figure, there are four traces. For each figure the four traces correspond to:

- Dark Blue: Inverter DG for bolted 3-phase fault
- Pink: Rotating DG for bolted 3-phase fault

- Red: Inverter DG for impedance fault
- Light Blue Rotating DG for impedance fault

As noted above, voltage and frequency regulation are a prerequisite for islanded operation. The cases with power dispatch mode are not studied in this Chapter. Thus, only cases with full control are considered. The two fault events are intended to illustrate that having these controls is a necessary condition, it may not be sufficient to assure successful islanding. The dynamics of tripping from grid connection to islanded operation can be very important.

Figure 5-10 shows the voltage at the motor loads within the facility. Figure 5-11 shows the main bus voltages with the facility microgrid. Figure 5-12 shows the reactive power output of one of the DGs in the facility. Figure 5-13 shows the active power output of one of the DGs in the facility. Figure 5-14 shows the currents delivered by one of the DGs in the facility.

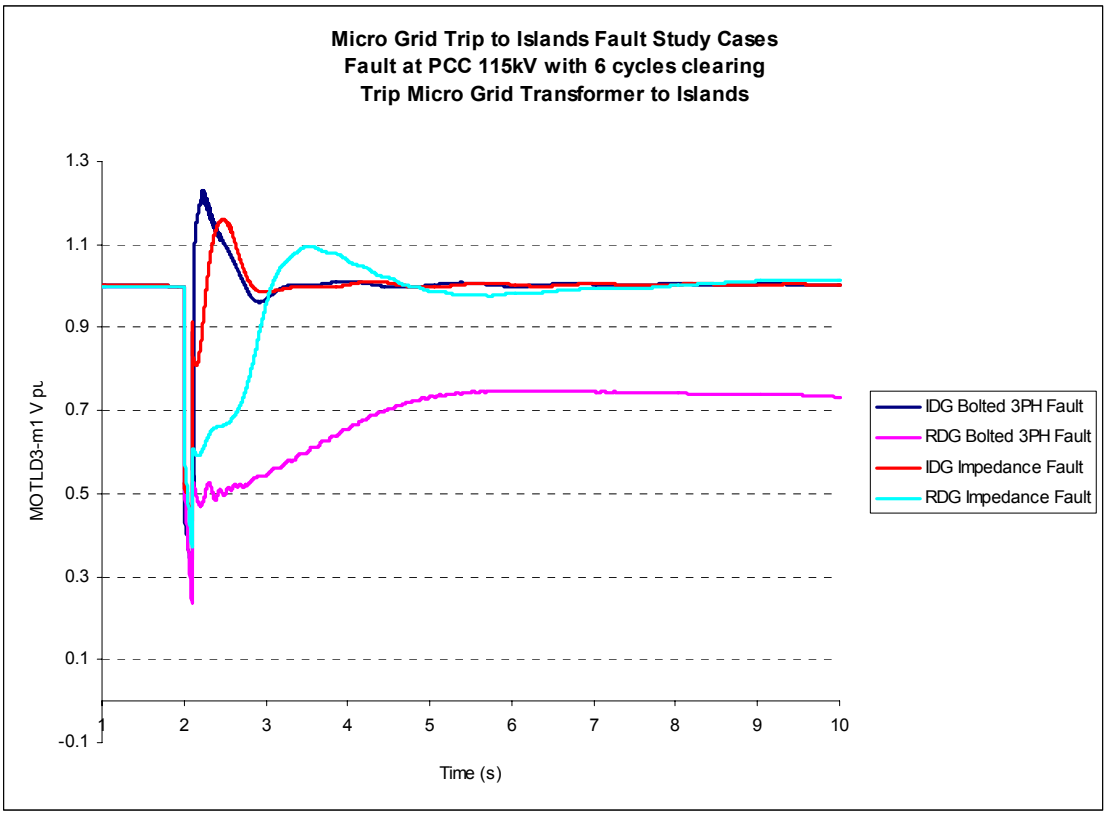


Figure 5-10. Microgrid load voltage – following grid disturbance and trip to island

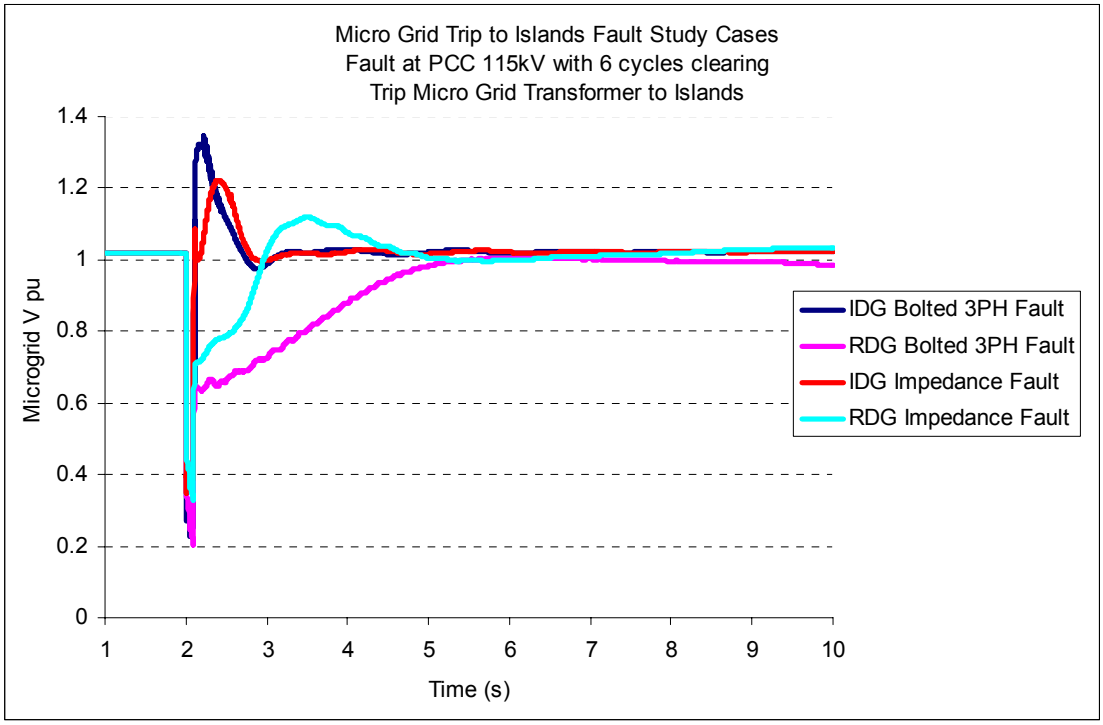


Figure 5-11. Microgrid main bus voltage – grid disturbance and trip to island

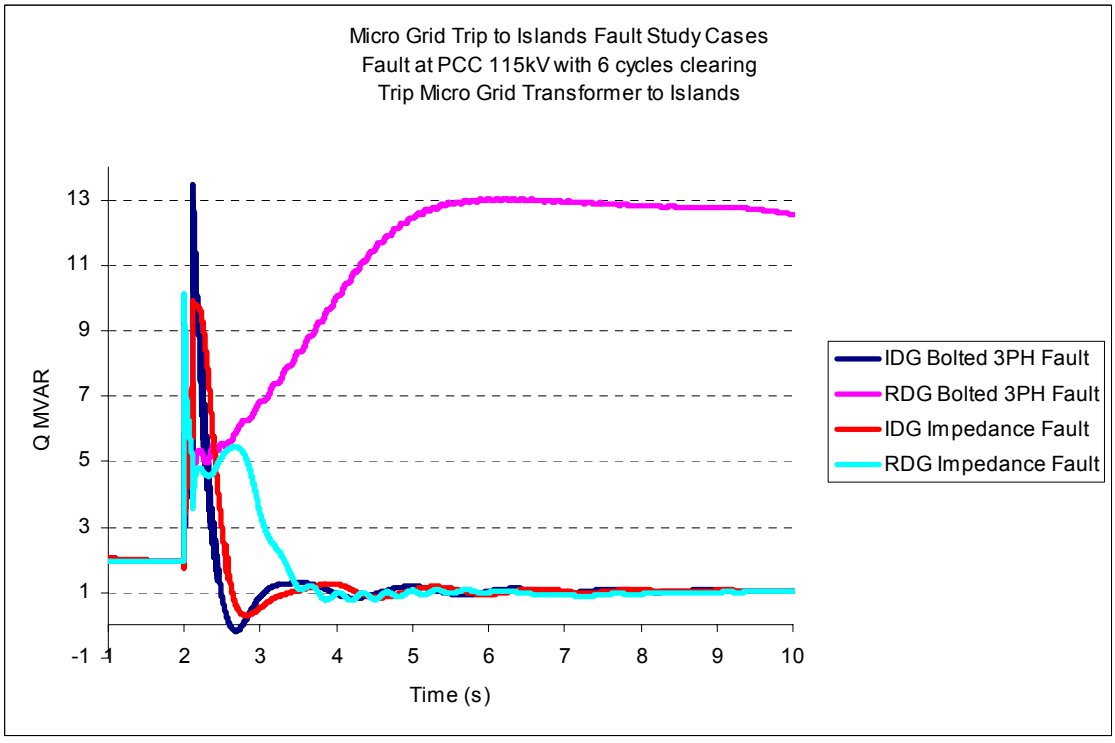


Figure 5-12. Microgrid DG reactive power output – grid disturbance and trip to island

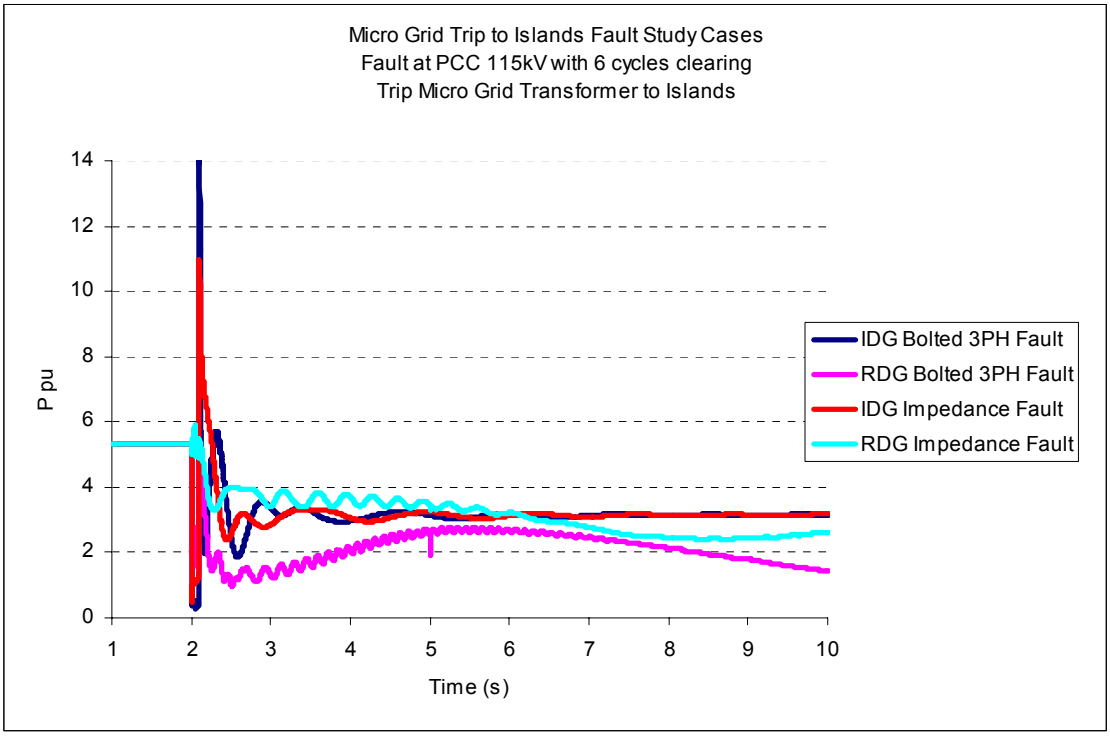


Figure 5-13. Microgrid DG active power output – grid disturbance and trip to island

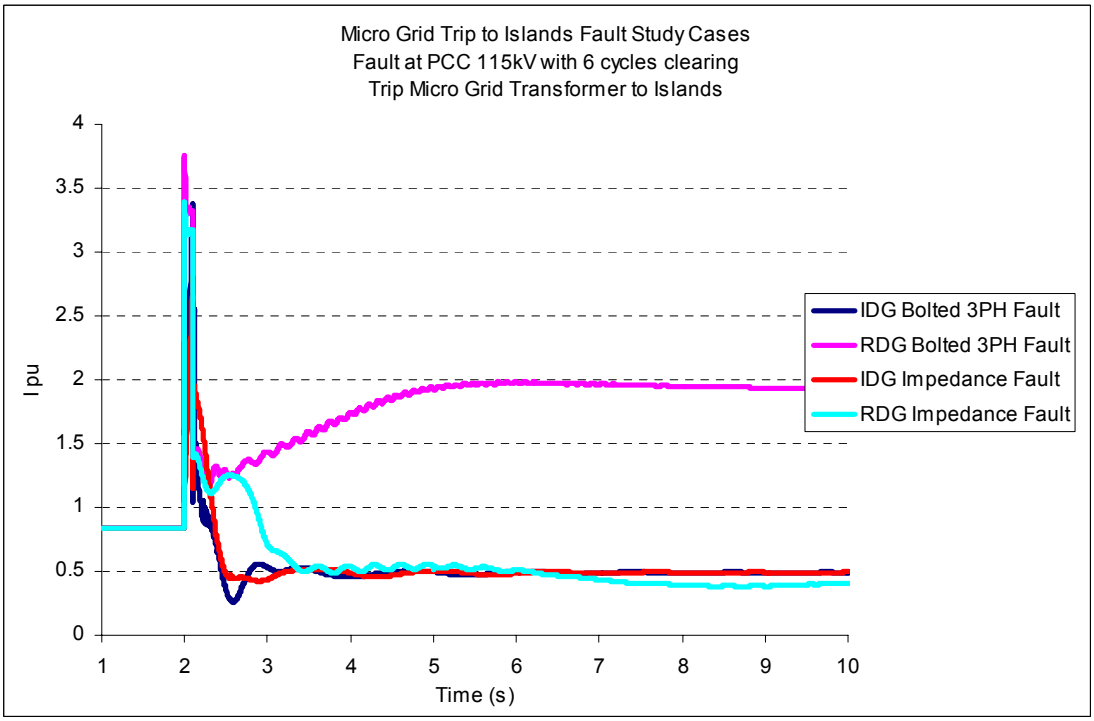


Figure 5-14. Microgrid DG current– grid disturbance and trip to island

5.6.3 Observations

There are a number of observations to be made from these cases.

First, and most important, is that for this particular microgrid, not all of the load within the facility can be served when the microgrid trips to islanded operation. In all of these cases, roughly half of the load in the facility is tripped. This non-essential load is disconnected to allow for continued secure operation of the remaining critical load. This is a major reliability consideration and potential advantage in a facility microgrid: the ability to differentiate between critical and non-critical load. In these cases, facility microgrid control disconnects the non-essential load after the transformer circuit breaker opens, creating the island. The transient swings of the system variables reflect the dynamics of the loads responding to the fault and their interaction with the DG controls.

Second, the microgrid fails to tolerate the dynamics associated with the trip to an island for one case: that is with a very severe fault and the machine-based DG. In this case, the motor recovery fails in a fashion similar to that in failed recovery cases discussed in the previous chapter. In these cases, the faster response of the inverter based DG with very aggressive controls allows for a better recovery. However, this simulation was somewhat idealized; an inverter-based DG might not be able to sustain the temporary overcurrents seen in this case unless it is specially rated for this duty.

This particular comparison is illustrative mainly in the sense that it is clear that different responses will have a major impact on the success (and therefore viability) of the island.
One might be tempted to conclude from this example that inverter based DGs are superior for islanded operation. However, other experience shows that inverter based DGs are generally more sensitive to voltage dips that result from faults and are more likely to trip in response to such stimulus. Inverters, unless over designed, have very limited overcurrent capability. The thermal time-constants of solid state power electronic devices are very short, compared to the copper windings of a rotating generator. Unless these devices are selected so that they normally operate well below their maximum allowable temperatures, overcurrents must necessarily be limited by either tripping or limitation of output current via control action. Limitation of current output by a DG in a recovering system, where loads demand more current than the DG can supply, will result in voltage collapse.

There are several necessary conditions for a DG to support microgrid islanding, which are:
The DG must not trip in response to the initiating disturbance.
The load in the island must not exceed the capability of the DG in the islanded microgrid. If exceeded, non-critical load shedding schemes should be incorporated so that the islanded microgrid can support critical load.
Having enough capability is not sufficient alone: The DGs must have the necessary dynamic response to survive the disturbances that cause the trip to island, and survive the dynamic behavior of the loads following islanding, including inrush currents drawn by transformers and motors (which may be highly distorted), and reacceleration of motors and their mechanical loads.

5.7 Summary

5.7.1 Findings

This Chapter has investigated three key issues facing facility microgrids, and they are:

- Facility microgrid with multiple DGs unintentional islanding protection

- Facility microgrid response to bulk grid disturbances
- Facility microgrid intentional islanding.

One category of recent advancements in unintentional islanding protection are the active anti-islanding controls. The active schemes were developed for single DG, inverter or machine based. Previously, their performance when applied to multiple DGs was not well understood. The first part of the report has attempted to gain an in-depth understanding of these new AI schemes. The recommendations are summarized below:

- For a facility microgrid with only inverter-based DGs, all DGs should be equipped with the same anti-islanding control, either active voltage scheme, or active frequency scheme, or both schemes are enabled.
- For a facility microgrid with only machine-based DGs, all DGs should be equipped with the same anti-islanding control, either active power scheme, or reactive power scheme, or both schemes are enabled.
- For a facility microgrid with mixed inverter- and machine-based DGs, all inverter-based DGs should be equipped with active frequency scheme, all machine-based DGs should be equipped with reactive power scheme.

If the recommendations are not followed, the facility microgrid may risk unintentional islanding, unless other means or design changes are provided. These results are also relevant to the performance of multiple DGs, not in a planned microgrid, connected to an Area EPS circuit. Despite meeting accepted performance requirements and tests, based on the performance of individual DG units in isolation, desired anti-islanding performance may not be realized. This poses a potential risk to safety and exposes utility and customer equipment to possibly damaging conditions.

Obviously, the DGs with active anti-islanding control will not allow seamless transition from grid-parallel to islanded operation. In this case, the microgrid has to shut down, disconnect from main grid, then start up as needed, to supply local load. For microgrid applications requiring seamless transition, other means for loss of main grid detection need to be explored.

The chapter also studies the facility microgrids dynamics in response to bulk grid disturbances. The major takeaways are summarized below:

- The dynamic behaviors of the facility microgrid are significantly different for different cases. The cases with no DG and with the dispatch mode inverter-based DG fail to recover from the fault – that is, the load in the facility is disrupted, and the facility would likely trip some or all of its load and DG.

- This failed recovery is not only disruptive to the microgrid load, it is also disruptive to the host grid. This is evident in the high currents drawn after the load stalls. This could cause false trips of protective relaying, and possibly result in outage of other customers on the host grid. Addition of controls (voltage and frequency droop regulation mode) for both types of DG allows a successful recovery, and all parties benefit.

- The presence of DG in the microgrid with appropriate controls can be beneficial to both the microgrid (DG owner) and to the grid. (The No DG case failed.)

- The machine-based DG with dispatch mode was more benign than the inverter-based DG with dispatch mode. This may be due to the inherent mechanical (and magnetic) inertia of the machine that may make recovery naturally friendlier. Conversely, the best performance (based on fastest recovery to normal voltage and speed) results from the inverter-based DG with full control (voltage and frequency regulation). This is not surprising since the inverter-based technologies are more controllable and are more dependent on good control – these are different faces of the same nature of the equipment.

Finally, the Chapter studies the facility microgrids intentional islanding behaviors. The major observations are summarized below:

- For the studied facility microgrid, not all of the load within the facility can be served when the microgrid trips to islanded operation. In all of these cases, roughly half of the load in the facility is tripped. This non-essential load is disconnected to allow for continued secure operation of the remaining critical load. This is a major reliability consideration and potential advantage in a facility microgrid: the ability to differentiate between critical and non-critical load. In these cases, facility microgrid control disconnects the non-essential load after the transformer circuit breaker opens, creating the island. The transient swings of the system variables reflect the dynamics of the loads responding to the fault and their interaction with the DG controls.

- The microgrid fails to tolerate the dynamics associated with the trip to an island in the one case of a very severe fault and the machine-based DG. In this case, the motor recovery. In these cases, the faster response of the inverter-based DG with very aggressive controls and with sufficient overcurrent capability allows for a better recovery.

5.7.2 Future Work

Generally, facility microgrids are more technically and economically viable than other microgrid applications. To make facility microgrids more practical and attractive, one key issue is autonomous operation that needs to be further explored. In order to have autonomous operation, a facility microgrid should be designed such that it is adaptive to both grid-connected and islanded conditions with minimum load interruption. This requires a system-level design optimization, including system-level controls (autonomous or self-reconfigurable), energy storage deployment/optimization to deal with transients and slow response of prime movers, intelligent load shedding strategies, etc.

Another issue of critical importance is the identified problem of incompatible active anti-islanding controls, which may not work together to provide the necessary performance. This issue extends beyond the narrow context of microgrids to include DG applications in general. Current industry standards appear to be inadequate to provide critical system protection in the future as DG penetration increases and multiple DGs on a feeder become a routine situation.

There is an urgent need to further study and define this issue, and recommend changes to standards to achieve the required protection.

6 Summary

This report summarizes the detailed study and development of new GE anti-islanding controls for two classes of DGs. One is inverter-interfaced, the other is synchronous machine-interfaced. These two types of interfaces cover most distributed generations, including photovoltaics, fuel cells, variable speed engines (microturbines, sterling engines), small wind turbines with direction conversion, batteries, engine generators (diesel, natural gas, biomass, hydrogen) and small gas turbines.

The accomplishments of the work include:

1. Proposed a family of new anti-islanding schemes that feature no non-detection zone (NDZ), have minimum power quality impact, low cost implementation (software code only), and robust to grid disturbances

2. Provided design guideline of the proposed schemes

3. Evaluated and validated the proposed schemes under practical application conditions

4. Demonstrated that the schemes work for multiple inverters, multiple machines, and mixed inverter and machine-based DGs. Results indicate some schemes, though working efficiently for a single DG, may be ineffective for multiple DGs.

5. Experimentally tested and validated the schemes

6. The report has also addressed several key issues of facility microgrid applications.

7 Appendix

7.1 Synchronous Machine Data

The data for the generator used in the simulation studies is obtained from [17].

Machine rating: 150 kW.

Machine rated voltage (line-to-line RMS): 480V.

Inertia Constant : H =2.00 MW/MVA

Machine Reactance values (in pu):

Xd=10.823 pu ; Xq=5.325 pu; X'd=0.863 pu ; X''d= 0.258 pu ; X''q=0.304 pu ;

Time constant value (in pu):

T'd0=2.11s; T"d0=0.0227s; T"q0=0.176s; Xl=0.0892 pu; Ra=0.22 pu.

Load Parameters (100 % of Load):

R=1.536 ohms

L=2.26354 [mH]

C=3.108295 [mF]

For the system with voltage and frequency control

Exciter Data:

K_1=0.0625 pu; T_1=100 pu;

K_2=33 pu; K_2=0.02 sec;

K_3=1.0 pu; K_2=0.0159 sec.

Governor Data:

T_G=1.0 sec;

R_G=5% pu.

7.2 Induction Motor Data

The data for the induction motor used in the simulation studies is obtained from [15].

Stator winding resistance R_a= 0.0068 pu;

Stator leakage inductance L_1= 0.1 pu;

Magnetizing inductance L_m= 3.4 pu;

Synchronous inductance L_s= 3.5 pu;

Rotor resistance R_2=0.018 pu;

Rotor leakage inductance L_2=0.07 pu;

Inertia constant H=0.5 MW/MVA

Load model exponent D=2 pu;

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