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High-Throughput Approaches to Optimization of Crystal Silicon Surface Passivation and Heterojunction Solar Cells

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HIGH-THROUGHPUT APPROACHES TO OPTIMIZATION OF CRYSTAL SILICON SURFACE PASSIVATION AND HETEROJUNCTION SOLAR CELLS

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ABSTRACT

We use a high-throughput (combinatorial) hot-wire chemical vapor deposition system to passivate the crystal silicon surface and to grow heterojunction silicon solar cells. We study the effectiveness of crystal surface treatments by atomic H or/and NH_x radicals, followed by the growth of thin hydrogenated amorphous silicon (a-Si:H) films. Treatment and layer properties such as times, thicknesses and gas mixtures can be continuously graded, creating a two-dimensional sample with each variable varying in one direction. This results in high-throughput optimization of the processes. Effective carrier lifetime is measured by photoconductive decay to evaluate the effectiveness of the surface passivation by surface treatments. The effective carrier lifetime increases from about 5 µs without passivation to about 24 µs with an optimized surface treatment and thickness a-Si:H on single-sided c-Si. Transmission electron microscopy reveals that a-Si:H, a mixed phase, or epitaxial growth of thin-film Si depending upon the surface treatment. Improvement in effective carrier lifetime correlates to with an immediate a-Si:H growth on c-Si, rather than a mixed phase and epitaxial Si growth. We have obtained an efficiency of 13.4% on a non-textured single-sided heterojunction solar cell on a p-type CZ-Si processed with optimized surface treatment.

INTRODUCTION

Surface passivation of c-Si is a critical process for many applications, especially heterojunction solar cells. The surface states often act as recombination centers for the charge carriers. The reduction of excess carrier loss at the c-Si surface, which is the part of heterojunction of an a-Si/c-Si solar cell, is one of the key issues to improve the device performances [1]. Hydrogenated amorphous silicon (a-Si:H) has been widely used for thin-film photovoltaic [2] and many other applications. It has unique properties of high H content and higher bandgap than c-Si. Therefore, it is a promising candidate for surface passivation to c-Si than other traditional dielectrics such as SiO_2 and Si_3N_4. Sanyo's HIT structure cell [3] proves that a thin a-Si:H layer not only effectively passivates the c-Si surface but also can be part of junction layer. However, direct deposition of a-Si:H on a hydrophobic c-Si surface often leads to a mixed phase or epitaxial Si growth with some degree of structure defects, especially by hot-wire chemical vapor deposition (HWCVD) [4]. This epi-Si-like growth has prevented us from achieving a better surface passivation and heterojunction. A high-throughput (combinatorial) hot-wire chemical vapor deposition system [5] is an ideal tool to study thin-film Si growth on c-Si. We believe that surface treatments before a-Si:H deposition can lead to a sharp transition from c-Si to a-Si:H and a better heterojunction for solar cell. In this paper, we will demonstrate how we use this powerful combinatorial tool to screen many surface treatments and successfully lead to the sharp transition, which improves the effective carrier lifetime and solar cell performance.

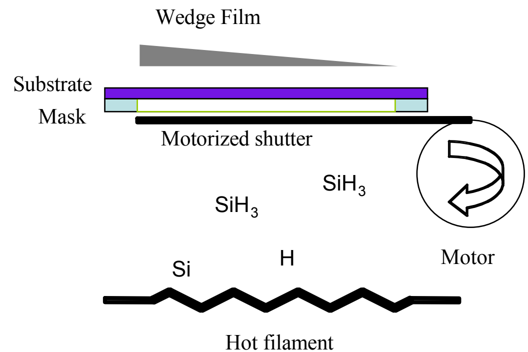

Figure 1. Schematic of high-throughput HWCVD of making thickness grading film with a mask and a motorized shutter which is very close to the surface of the substrate.

EXPERIMENTAL

A final 5% HF dipped clean c-Si substrate is loaded into a high-throughput HWCVD system for surface treatments, thin-film Si growth, or junction depositions. Figure 1 shows the schematics of the high-throughput HWCVD system and the mechanism of making thickness-graded film. The detail description of the system has been published elsewhere [5]. The substrate temperature is set at 250°C for surface passivation study and 200°C for heterojunction solar cells. In HWCVD [6], a hot tungsten filament (~2050°C) acts as a thermal source to decompose the process gases. We use, as an example, H_2 for the surface treatment and pure SiH_4 for the thin-film Si layer. When H_2 passes through the hot filament, it decomposes into H atoms. Therefore, the effects of chemical treatment by atomic H on the surface of c-Si can be rapidly examined using a physical mask. When SiH_4 flows through the hot filament, it decomposes into Si and H atoms. These atoms then collide with SiH_4 in the chamber to form SiH_3, and other radicals to grow an

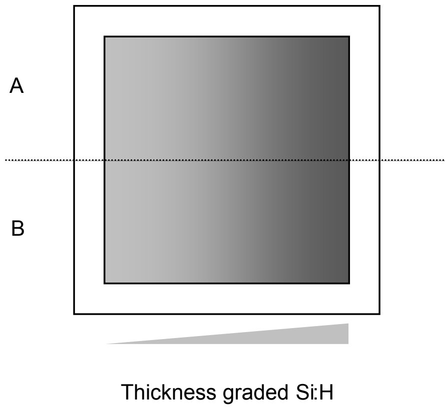

Figure 2. Schematic of high-throughput approach method 1: a direct comparison of two variables and the effect of a thickness graded film.

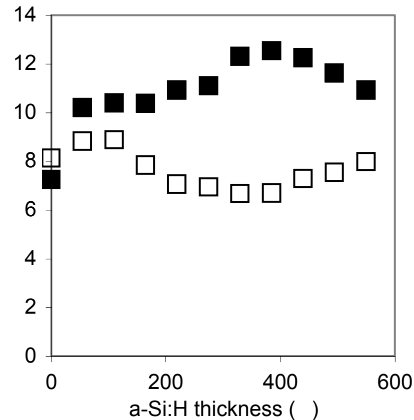

Figure 3. Effects of the surface treatments with (squares) and without (diamonds) atomic H on the effective carrier lifetime as a function of a-Si:H thickness (varied from 5 to 60 nm).

a-Si:H film. We used 20 sccm of SiH_4 and at 9 mTorr. To make thickness graded a-Si:H film, a moving shutter which is very close to the surface of the substrate was added to the system. The variation of the thickness can be controlled by the speed of shutter, the deposition rate, and deposition time.

AMORPHOUS SI SURFACE PASSIVATION

We show here two high-throughput approaches to study the effects of surface treatments and thickness variations on crystal silicon surface passivation. The first approach (method 1) is to apply a surface treatment such as atomic H labeled as in A and no treatment as in B to the part of the c-Si substrate using a mask for a fixed time and then deposit a thickness-graded a-Si:H on the entire sample. Figure 2 shows the schematic of method 1 approach. In practice, it is very useful to directly compare two different surface treatments because the treatments are done on the same c-Si and most our daily task is to try to find the difference between two variables. Actually the high-throughput system is able to compare up to ten variables on a single substrate. This is achieved by using a set of physical masks inside the chamber and a substrate manipulator. This approach is a very efficient tool for screening.

Figure 3 shows the photoconductive decay lifetime [7] as a function of two surface treatments and a-Si:H film thickness. The thickness is calculated from deposition rate on glass substrate times the deposition time. In this sample, the half of the c-Si substrate is exposed to the atomic H for 3 min with a H_2 flow rate of 70 sccm and 25 mTorr. A physical mask with 25 x 50 mm opening is used. Then, we switch to a 50 x 50 mm opening mask, and grow a thickness graded a-Si:H. The effective minority carrier lifetime is probed on the upper region A in figure 2 with atomic H treatment (open squares in figure 3) and the bottom region B in figure 2 without the treatment (solid squares in figure 3) at various locations of different a-Si:H thicknesses. The a-Si:H thickness varies from 55 to 600 Å.

The experiment data shows an interesting result that the effective lifetime in general is higher without the atomic H treatment in comparison to the one with the treatment. We will explain this finding later. With increasing a-Si:H thickness, the changes in lifetime is between 6.5 and 9 μs with H treatment. However, there is an increase of lifetime from 7 to 13 μs with increasing a-Si:H thickness without the atomic H treatment. The thickness at the highest lifetime is about 400 Å. The lifetime on the bare c-Si wafer without any surface treatment and a-Si:H is about 6 μs. This value serves as our baseline of a non-passivated surface.

Our second approach (method 2) is to apply a continuously varied time of a surface treatment such as atomic NH_3 + H_2 to the sample, rotate the sample 90°, and then deposit a continuously thickness-graded a-Si:H on the entire sample. This approach creates a three-dimensional plot, two variables and one result, on a single substrate and is a very powerful tool for detail process optimization. Figure 4 shows the schematics of the method 2. The continuous variation is achieved by a motorized shutter, which is placed very close to the substrate surface in the deposition system. The heated substrate can be xyz positioned and rotate 360° relative to the mask.

Figure 5 shows the effective lifetime as a function of time in our best surface treatment with H_2 + NH_3 before a-Si:H deposition in the x-axis and a-Si:H thickness in the y-axis. The numbers inside the matrix represent lifetimes in μs and only selective locations on the substrate were measured. In method 2, both variables are continuously varied as described in the Figure 4. In Fig. 5, the thinnest a-Si:H layer is along the bottom edge. For a short surface treatments time (5 s), the measured lifetime shows an increases and then slightly decrease (the left most column) as increase of a-Si:H thickness. This result shows a similar trend as in Figure 3 that certain thickness of a-Si:H is needed to enhance lifetime. However, the

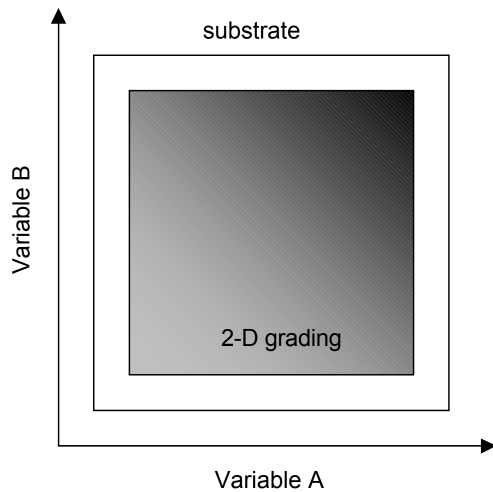

Figure 4. Schematic of high-throughput approach method 2. A three dimensional plot on a single substrate: two variables and a result.

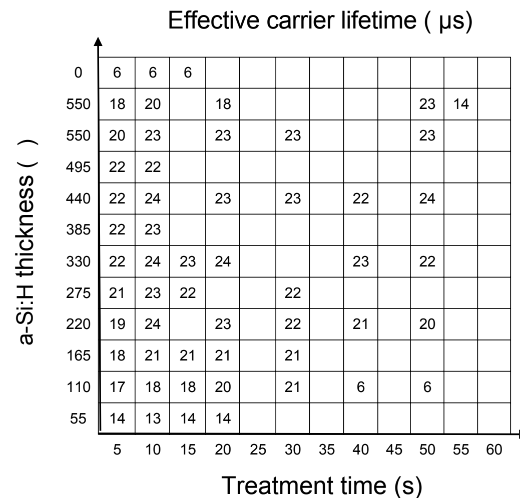

Figure 5. Effective carrier lifetime as a function of a-Si:H thickness (varied from 5 to 55 nm) and surface treatment time (varied from 0 to 60 s) with $H_2 + NH_3$.

lifetime does not increase appreciably for a constantly small a-Si:H thickness of 55 Å. This result points out an important fact that the surface treatment alone is not adequate to passivate the interface. With the help of an a-Si:H layer, lifetime after surface treatment with $H_2 + NH_3$ is much higher than the results in Figure 3. Lifetime reached 24 μs with $H_2 + NH_3$ treatment compared to 13 μs in the sample without atomic H treatment with 400 Å a-Si:H thicknesses. However, after closer examinations of the results in Figure 5, we realize the significance of the surface treatment in which one can achieve a high lifetime in the c-Si with a much thinner a-Si:H. In Figure 3, the optimum thickness for a-Si:H is about 400 Å without a surface treatment. However, in Figure 5, we only need about 100 Å with a surface treatment of $H_2 + NH_3$.

Hydrogenated amorphous silicon films content, in general, about 10 at.% hydrogen and has a mobility bandgap of 1.8 eV which is higher than 1.1 eV of c-Si. When a-Si:H are deposited on c-Si as surface passivation layers, it, in principle, forms a heterojunction because of the difference in bandgap just like other dielectrics such as SiO_2 and Si_3N_4 but at much lower temperature. The electric field at the interface pushes back the free carriers back into the bulk of Si and prevents the excess carrier loss. The H will help to passivate Si dangling bonds at the surface to reduce the defects that act as a recombination center for the carriers. The H inside a-Si:H can move to the interface to further improve the surface passivation as other advantages over traditional dielectrics. We examine the interface between grown thin-film Si and c-Si by transmission electron microscopy (TEM) at above surface treatment conditions to explain the lifetime measurement results.

Figure 6 shows TEM images of a-Si:H and c-Si interfaces at three surface treatments. Figure 6a is the interface with atomic H treatment. It shows an intermediate layer with a rough surface and epi-Si growth with structure defects and then a-Si:H layer. This result suggests that atomic H creates an undesired intermediate layer before a-Si:H growth. This damaged rough surface creates more surface defect states such that it did not improve the effective carrier lifetime as shown in Figure 3. This intermediate layer dominates the loss of carriers and makes the later growth of a-Si:H useless. Figure 6b shows the interface without atomic H treatment. It also shows an intermediate layer but much smooth surface and a good epi-Si like layer appears immediately on the surface of c-Si. It eventually breaks down into a-Si:H as the thickness increases. In this case, the intermediate layer has less effect on the carrier loss compared to the first case. The thickness dependence of effective lifetime on a-Si:H thickness in Figure 3 (solid squares) can be explained by simply treating the intermediated layer as perfect c-Si. The actual thickness of a-Si:H shall be corrected by subtracting from the epi-Si thickness. Figure 6c is the interface with $H_2 + NH_3$ treatment. In this image, there is no apparent intermediate layer! It shows a smooth and immediate transition from c-Si to a-Si:H. The c-Si surface is well passivated by a-Si:H and results in the best lifetime as shown in Figure 5. We conclude that the improvement in effective lifetime well correlates to an immediate a-Si:H growth on c-Si and surface treatment can be a key.

HETEROJUNCTION SOLAR CELLS WITH SURFACE PASSIVATION

In a-Si:H and c-Si heterojunction solar cells process, we face the same challenge to grow an immediate a-Si:H on c-Si because the above facts of growing intermediate layer. We have reported the effect of various intermediate layers on the performance of HJ solar cell [4]. We found that immediate a-Si:H growth of n-type emitter yields the

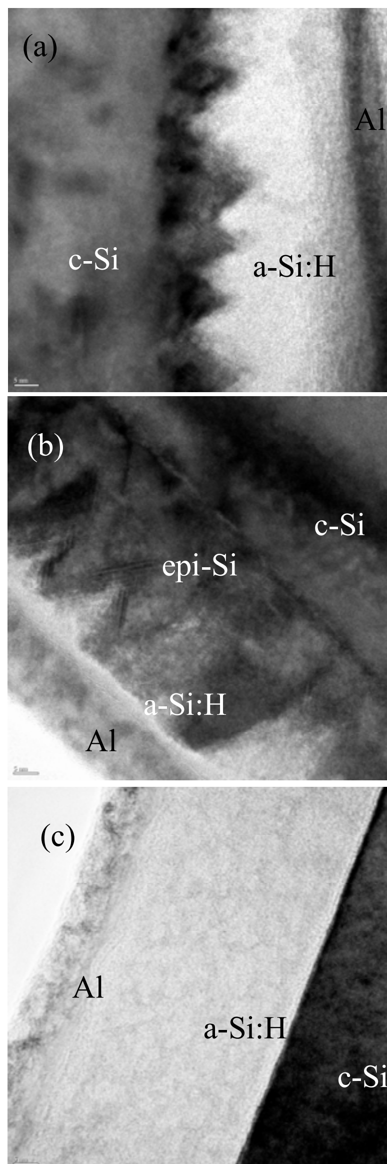

Figure 6. TEM images of different c-Si and a-Si:H interfaces. 6a: with atomic H treatment. 6b: no atomic H treatment. 6c: with NH_3+H_2 surface treatment. All sample has Al cap for the TEM sample preparation.

best cell performance. We can achieve the immediate a-Si:H growth by deposited the film at lower substrate temperature (100°C). However, here, we show other approach to achieving the high-performance of cell at the condition that the intermediate layer (epi-Si) often grows without chemical surface treatment.

We compared JV characteristics of two solar cells: one with a typical NH_3+H_2 surface treatment and other with an optimized treatment before forming n-type emitter. We used a non-textured (100) p-type CZ- Si with resistivity of 1.2 Ω-cm and about 400 µm thick. The cell area is 1 cm^2. The preparation of n-type emitter and wafer properties were published elsewhere [8]. The cell result with typical chemical treatment indicates that a direct transfer of the recipe from surface passivation to a-Si:H heterojunction is not straight forward. The JV curve under light shows an "S" shape near the open circuit voltage (V_{oc}). The cell basically did not work! The result suggests it is possible that NH_3+H_2 surface treatment creates a very thin SiN_x layer which is not sensitive to the lifetime measurement but a barrier to the heterojunction. We are able to achieve a high-performance HJ cell by re-adjusting the mixture of NH_3+H_2 flow rate and process conditions. The cell has a better JV characteristics and an efficiency of 13.4% with V_{oc} greater than 0.60 V, short circuit current density of 31.0 mA/cm^2, and fill factor of 0.72. This cell demonstrates the importance of chemical surface treatment although our best efficiency on the same type c-Si is at 14.9%.

SUMMARY

In summary, we show a detail application of the high-throughput HWCVD technique to the c-Si surface passivation and heterojunction solar cells study. With this powerful tool, we quickly screen the surface treatment variables and optimize the a-Si:H thickness. We conclude that the best surface passivation is achieved with an immediate growth of a-Si:H on c-Si with the aid of a proper chemical surface treatment. We also fabricate the high-performance heterojunction crystalline silicon solar cells based on the optimized surface passivation.

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REFERENCES

1. T. Wang, Q. Wang, M. Page, and T. Ciszek, Thin Solid Films, **430**, 261 (2003).
2. J. Yang and S. Guha, Mat. Res. Soc. Proc, **557**, 239 (1999).
3. H. Sakata, T. Nakai, T. Baba, M. Taguchi, S. Tsuge, K. Uchihashi, and S. Kiyama, Conference Record, the 28th IEEE PVSC, Anchorage, p.7 (2000).
4. T. H. Wang, Q. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, C. W. Teplin, X. Z. Wu, and H. M. Branz, in *Proceedings of the 19th EUPVSEC Conference*, edited by Paris, France 2004), to be published, (2004).
5. Q. Wang, L. R. Tessler, H. Moutinho, B. To, J. Perkins, D. Han, D. Ginley, and H. M. Branz, Mat. Res. Soc. Proc., **762** p. A9.1. 2003.
6. B. P. Nelson, Q. Wang, E. Iwaniczko, A. H. Mahan, and R. S. Crandall, Mat. Res. Soc. Proc., **507** p. 927. 1998.
7. R. K. Ahrenkiel and S. Johnston, Solar Energy Materials and Solar Cells, **55**, 59 (1998).
8. Q. Wang, M. Page, Y. Xu, E. Iwaniczko, E. Williams, and T. Wang, Thin Solid Films, **430**, 208 (2003).

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