Conference Paper

Excess Dark Currents and Transients in Thin-Film CdTe Solar Cells: Implications for Cell Stability and Encapsulation of Scribe Lines and Cell Ends in Modules

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EXCESS DARK CURRENTS AND TRANSIENTS IN THIN-FILM CdTe SOLAR CELLS: IMPLICATIONS FOR CELL STABILITY AND ENCAPSULATION OF SCRIBE LINES AND CELL ENDS IN MODULES

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ABSTRACT

We have isolated a non-linear, metastable, shunt-path failure mechanism located at the CdS/CdTe cell edge. In such cases, most performance loss, usually erratic, can be associated with the shunt path. We studied these shunt paths using dark current-transients and infrared (ir) imaging and find only one shunt path per cell and only at the cell corner wall, even in badly degraded cells. The effect on diminishing the cell's efficiency far exceeds what would be expected from the cell's linear shunt-resistance value. We propose that current transients and ir imaging be used as a "fingerprint" of the source and magnitude of excess currents to evaluate the contribution of scribe-line edges and cell ends in thin-film module performance and degradation due to environmental stress. Protection afforded by, or contamination due to, new or currently used encapsulants can then be evaluated.

INTRODUCTION

Monolithic large-area modules based on thin-film (T-F) a-Si, CIGS, and CdTe have been on the market for a number of years. Most module structures have series-connected cells, each delineated by a set of three scribe lines that form the series interconnect. T-F module active-area performance is always below the active-area performance of cells made with correspondingly processed materials. The most commonly cited cause for this reduced performance is series resistance, due to the sheet resistivities of the transparent conducting oxides used for one of the contacts and the interconnect resistance.

Here, we report on another, probably greater, loss mechanism that we have found in the CdS/CdTe T-F mesa-cell structure, namely, non-linear shunt paths at the cell edge, that can contribute to reduced initial performance loss as well as much of the degradation seen after stress [1,2]. Non-linear shunt paths reported here require two-dimensional (2-D) device modeling and are akin to, but much more devastating than the micro-nonuniformities reported in [3] that involve small micro-regions containing "weak diodes" that reside away from the cell edge. Our metastable, "very shunted, very weak" micro-diode regions appear at corners and probably at cusps, where the junction interfaces must intersect the surface at the cell edge where they are exposed to the effects of the environment, surface diffusion, and electromigration.

These shunt paths are induced with the application of bias voltage and accelerated by temperature and humidity. The loss in performance due to these shunt paths far exceeds what 2-D discrete circuit-element device modeling would predict when only a simple linear shunt resistor is used to represent the defect. Smaller conductive shunt paths, by inference, must exist at cusps and grain-boundary corners along edges caused by the physical chipping during the scribing procedure. These can become more conductive with stress.

At the sharp points on which a shunt is located, and especially at the cell corner where, additionally, localized electric-field enhancement can also occur, we observe significant and often times sporadic degradation. We use light and dark current-voltage (I-V) curves, dark-current transients [4]. and thermal imaging in the 3-5-μm wavelength range to identify these shunt losses. We propose that effects of humidity on cell ends and scribelines, with and without EVA or with new encapsulants, as well as edge-passivation processes, can be effectively screened for detrimental chemical reactions using the transients described in this paper.

The effect of metastable shunt paths and dark-current transients has been well documented in the a-Si T-F system [5]. Similar large excess dark currents and unsteady, minute-long, dark-current transients were found in CdTe cells [1,4]. Transients, measured by changing the voltage bias in a stepwise fashion, provide an ideal method to quantify the contribution of shunt paths. Excess dark currents on non-margined cells, i.e., cells with no border region between the back contact and the cell edge, were compared to currents on margined cells having a mm-wide border between the back contact and edge. Detailed descriptions of the margining process are given in these proceedings [2]. Cell preparation is described in [6]. The back contact for cells used in this study was graphite dag coated with a conductive Ag paste.

CURRENT TRANSIENTS

Ideally, dark currents are controlled by temperature-dependent carrier generation in reverse bias, and recombination in forward bias. In these cases, stepwise changes in bias produce either abrupt or smooth, steadily growing or decaying, current transients that occur as gap-state occupancy adjusts to the new bias condition. This type of normal transient current behavior for a margined cell before stress results in a smooth small
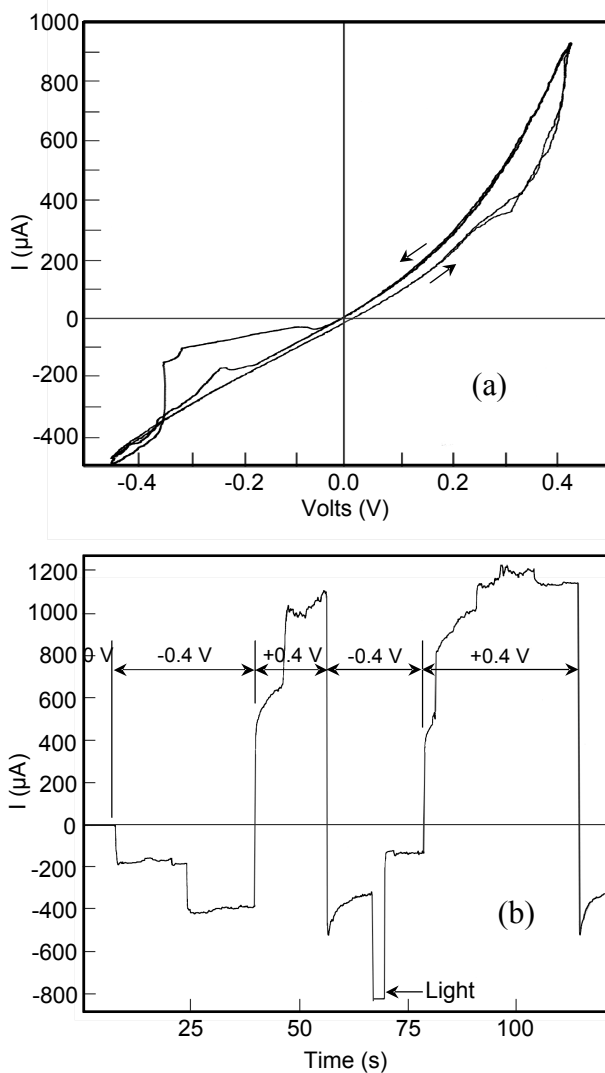
the I-V voltage sweep can be better studied by monitoring the transient behavior in the current due to stepwise changes in voltage. Figure 1b shows that switching between -0.4 and + 0.4 volt bias at 25°C produces large, minute-long current transients that contain the 200-μA step seen in Fig. 1a. One of the incremental changes in the current transient does turn off as the bias voltage sweeps through zero to the opposite sign. The short exposure to light at 65 s will also diminish the reverse bias to the shunt path and has the effect of turning it off. Sometimes, the shunt path was conductive enough to decrease the overall cell efficiency below 4.5%.

These are discrete shunt current paths as identified by the step-wise increases in forward- and reverse-bias currents. It appears that a trapping or localized heating process at the shunt path may be modulating the conducting on-state. The sum of the shunt currents at -0.4 V is -0.4 mA, which corresponds to 1000 ohms. As shunting worsens, discontinuous changes become larger. At T = 90°C, these transient currents are similar in size, but the large steps are absent as though they switched immediately when the voltage was changed to the conducting "on-state," and the trap-like or localized heating transient is absent.

THERMAL IMAGING AND CURRENT-VOLTAGE

IR camera imaging studies were used before to produce temperature profiles caused by heat generated at point shunt paths in T-F CIGS cells [6]. Viewing the T-F directly was shown to be far more sensitive than viewing from the glass side. The film-side thermal image in the 3-5 μm wavelength range of CdTe cell is shown in Fig. 2; The left-hand image shows the exact location of the large excess current shunt: The T rise is about 10 times the camera sensitivity and estimated to be about 1°C. The image was taken with a now, much larger, total shunt leakage current of 1.5 mA at a reverse bias of 0.45 V at 25°C. This corresponds to a dark resistance of about 300 ohms. The right-hand image was taken after removing with a razor blade a small piece of the corner containing the shunt. That procedure increased cell efficiency from 4.23% to 9.0% and reduced the reverse current to a mere 0.0009 mA at the 0.45 V reverse bias, unequivocally identifying that corner as the source of this cell's shunt loss. This result has been found on many of our shunted cells.

Fig. 1a. Erratic, shunted dark I-V for a non-margined, 0.778 cm^2, CdTe cell @ 25°C after stress; 1b. huge, abrupt, forward-current transient steps of 0.2 to 0.3 mA from voltage switching between -0.4 and + 0.4 volts @ 25°C. Note: a discrete shunt path turns on at 24, 48, and 82 s while voltage is constant; the short exposure to light at 65 s has the effect of turning off the shunt while at -0.4 V.

hysteresis loop in the forward bias dark I-V curve [1]. Also documented is the dark current transient at 90°C for a voltage bias switched from -0.3 V to + 0.3 V and back to -0.3 V. A reverse bias of -0.3 V produces a very temperature-dependent current density: 20 nA/cm^2 at 90°C and only 0.65 nA/cm^2 at 25°C. That cell had an initial efficiency of 12.5% and dark currents measured before stress.

For a non-margined cell with the same process steps as for the cell noted above, Fig. 1a shows an unstable, erratic dark I-V behavior during the 4-min voltage sweep cycles at 25°C. Voltage stress during measurement induces shunt path steps as large as 200 μA as the reverse bias increases to 0.4 V causing the large hysteresis loops. This cell also started at 12.5% efficiency, but was stressed for 1225 h at 100°C and one-sun exposure in open-circuit. This metastable shunt- path behavior in
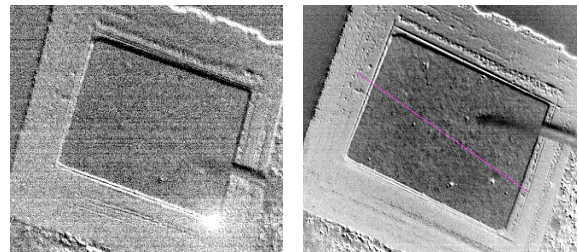

Fig. 2. Thermal-image difference taken for cell #177D: (left) The reverse-bias image at -1.5 mA @ -0.45 V minus the zero-bias image. The light spot in the lower-right corner is the biggest heat source. (right) The reverse-bias image at -0.0009 mA @ -0.45 V minus the zero-bias image after removing that corner. Other contrasts are due to camera vibration.

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The position and electrical characteristics of the cell with and without the shuntpath are now known precisely. When the joule heating is large enough to see with this camera, we find them at a corner of the rectangular electrode. The effect of the removal of the shunted sub-mm^2 triangular corner (seen in Fig. 2 right) on cell performance can now be evaluated. Figure 3. shows the light and dark I-V performance before and after the removal of the shunted corner. Before removal of the shunt, Fig. 3 shows the devastating effect that this geometrically small shunt-path (apparently 300 ohms) has. Its removal results in greatly enhanced performance, with the shunt current reduced a thousand fold. Nearly all of the shunt current flows through one shunt path or group of shunt paths within the same small area.
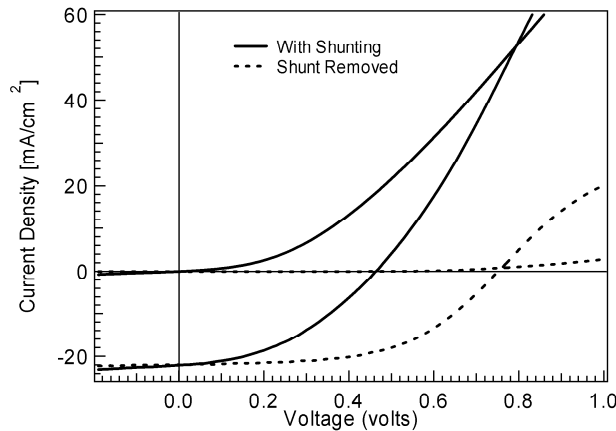

Fig. 3. Light and dark I-V performance; before and after scribing off the small piece of the defective corner.

More careful consideration shows the loss in performance far exceeds what a shunt of this resistance would be expected to produce. The encircled circuit elements at the left in Fig. 4 show the equivalent circuit required to model the I-V performance of a normal, undegraded CdTe cell that includes a back-contact diode, D_{Back}, opposing the main junction diode, D_{Front}. The right-hand circle shows the circuit elements required to model the effects of the non-linear shunt. Initially, discrete circuit-element modeling with PSpice included the normal diode area producing 20-mA light current plus the small shunted diode area with only a linear 300-ohm shunt resistor (R_{SH2}) to simulate the shunt resistance and a series resistance (R_{Sheet}) to simulate the sheet resistance of the SnO_2. This configuration showed no effect on open-circuit voltage (V_{oc}) and only a small effect on the fill factor (ff). The large reduction in V_{oc} and ff implies that this shunt path must be non-linear, i.e., an exceedingly leaky diode (D_{Weak}) must be added in parallel to the shunt resistor to simulate the defective corner's micro defect. We show this in the encircled circuit elements at the left in Fig. 4. Using this circuit approach, we can model these I-V curves with PSpice.

This defect has such a profound effect on the entire cell I-V because both junctions within the small defect area (the main front-junction that controls V_{oc} and ff and the back barrier-junction that is the cause of roll-over and crossover) intersect the cell wall and are very vulnerable to contamination, especially at this sharp corner. The

geometrical electric-field enhancement of junction and bias fields that lie in that exposed cell wall surface at this corner can only make matters worse. The enhanced field at a corner increases the current loss through the shunt path.
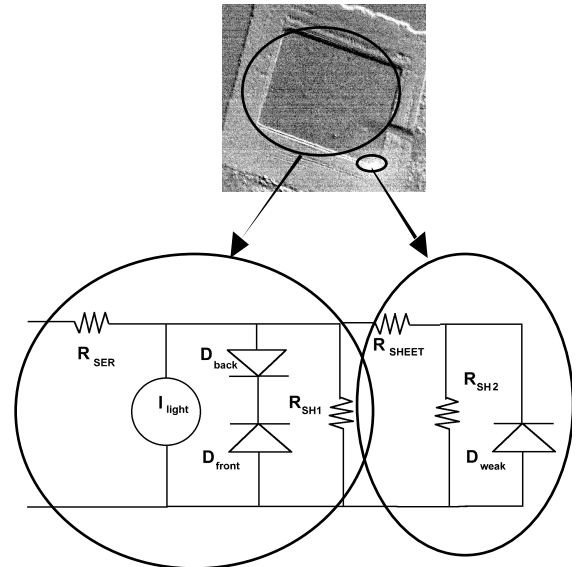

Fig. 4 Equivalent circuit depicting unshunted cell area (left) and corner containing the non-linear shunt path (a parallel combination of a shunt resistor and weak diode in series with a connecting series resistor RSheet that takes into account the effect of the CTO sheet resistance (right).

Ag, used in our CdTe contact, is known to be prone to electromigration [7], and the linear portion of the metastable shunt behavior may be the connecting and severing of small Ag tendrills on the exposed edge. The fact that humidity also accelerates shunting may be explained by envoking wet-electromigration [7]. The shunt paths in this report are turned on with a positive or negative voltage bias and turned off with a reduced or zero bias. It has been suggested that shunt transients in CdTe are due to Cu ion migration forming similar filaments [4]. We see that more is involved. Within the small shunt defect area, both the front and the back junction intersect the cell wall, exposing them to environmental stress and contamination from Ag electromigration, which diminishes the quality of both junctions. Lower V_{oc} and lower ff are caused by the compromised front junction and the diminished crossover behavior caused by the compromised back contact. This small area degrades the entire cell's I-V performance.

We also see evidence with ir imaging that these shunt losses are occurring at the scribe lines and cell ends in CdS/CdTe modules placed in the dark under forward bias; see Fig. 5. The edge wall of the CdS/CdTe cell's mesa-structure used in this study can be compared to the edge wall of the back metal scribe lines of the series-interconnect region between cells and the cell ends of a full-sized module. Cusps and corners are the inevitable result of scribing with a razor or a laser. Bead-blast procedures are often used to isolate the module cell area at the edges, leaving the cell ends in a very ragged edge. Indeed, almost any T-F polycrystalline module has warm spots on edges and scribe lines when viewed with an ir

camera while forward bias is applied in the dark. Mechanical and/or laser scribing are used to define interconnects, again leading to exposed cell walls.
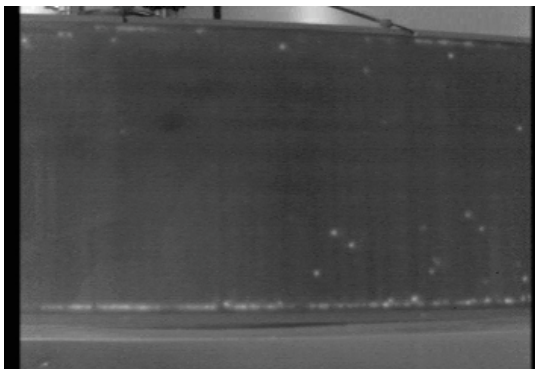

Fig. 5. IR image of a CdTe module forward biased to V_{oc} in the dark.

The effects of humidity on cell edges and scribe-lines, with and without EVA and with new encapsulants, can be effectively screened at the cell level for detrimental chemical reactions. Suitable water-vapor dielectric barriers may have the added effect of reducing the electric field at the cusps and corners present in scribed cells.

Figure 6 shows the preliminary results of encapsulation studies. Non-margined and margined EVA encapsulated cells are stressed, along with a margined non- encapsulated cell. We see lamination loss on the two laminated cells at time = 0. No evidence of shunt-path formation is seen in any current transients up to 750 h. In addition to the initial loss, laminated cells degrade faster. More cells must be put into test, other encapsulants investigated, and stress conditions involving humidity added.
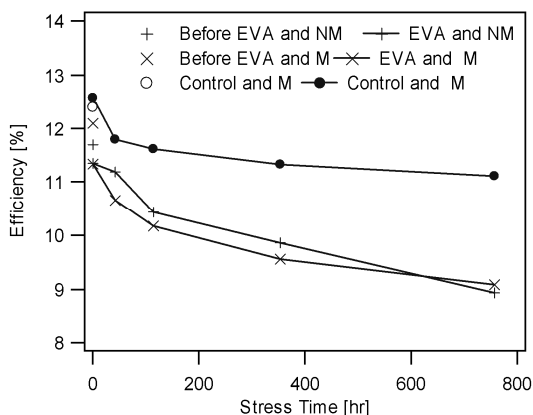

Fig. 6. Performance of EVA-laminated, non-margined (NM) and margined (M) cells with stress time at 100°C and one-sun exposure in open-circuit.

CONCLUSIONS

We have isolated a non-linear, metastable, shunt-path failure mechanism located at the CdS/CdTe cell edge using dark-current transients and ir imaging and find only one shunt path per cell and only at the cell corner wall, even in badly degraded cells. They are induced by voltage and accelerated by temperature and humidity. The effect on diminishing the cell's efficiency far exceeds what would be expected from the cell's linear shunt-resistance value. To model the observed performance change, we must include a very weak diode in parallel with the shunt path, to fully describe how this small defect area can influence the entire cell. Exposure of the diode's front and back junctions at corners and edges makes it very vulnerable to environmental attack and electromigration. We are beginning to test encapsulated cells and preliminary results show EVA causes a lamination loss and an increased rate of degradation. Ultimate module efficiencies may be limited by this type of shunt path.

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