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Technical Report

Grid-Connected Inverter Anti-Islanding Test Results for General Electric Inverter-Based Interconnection Technology

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Executive Summary

One concern about the installation and operation of distributed generation on the electric power system is islanding. Islanding is defined in Institute of Electrical and Electronics Engineers (IEEE) Standard 1547 as:

> a condition in which a portion of an Area Electric Power System (EPS) is energized solely by one or more Local EPSs through the associated point of common coupling (PCC) while that portion of the Area EPS is electrically separated from the rest of the Area EPS. [E1]

Typically, distributed generation manufacturers incorporate anti-islanding functionality into their equipment to ensure it detects electrical islands and disconnects from the electric power system properly.

This report summarizes the anti-islanding testing results of an inverter-based interface for distributed generation. The testing was conducted at the General Electric (GE) Research Laboratory and the National Renewable Energy Laboratory Distributed Energy Resources Test Facility.

The objectives of the testing were to:

- Perform experimental validation of the effectiveness (determined by the time needed to detect and isolate distributed resource equipment from the grid) of proposed GE anti-islanding schemes
- Perform parametric evaluation of the GE anti-islanding schemes with respect to control settings and load conditions, including controller gains, load power levels, and load quality factors
- Develop recommendations for the IEEE P1547.1 working group
- Explore low-voltage ride-through characteristics.

Findings of the testing included:

- Using a matched load, the inverter can be islanded (more than 2 seconds) without any anti-islanding measures activated. In some cases, depending on load match and quality factor, the inverter can run on indefinitely.
- With the recommended anti-islanding parameter settings, the schemes work successfully (trip within 2 seconds) under all tested conditions, including worst-case generation/load balance as defined in the IEEE P1547.1 testing standard [E2].
- The anti-islanding testing results were repeatable under fixed conditions and parameter settings.

- The predicted effectiveness of the voltage and combined schemes did not correlate with load level. It was predicted the schemes would react more quickly at low loading conditions. However, this was not always observed in testing. More testing is needed to draw conclusions from the observations.
- When both voltage and frequency anti-islanding schemes were enabled, tripping time was not faster. This indicates there is some interaction between the schemes. It is recommended that only one scheme be used so performance is more predictable. More study and tests are needed for a better understanding of interactions in combined schemes.
- When a positive feedback control is employed, there is a critical gain below which the positive feedback control will fail to detect unintentional islanding and result in certain non-detection zone.
- Given the configuration of an unregulated DC bus obtained from a diode rectifier, the inverter is not able to ride through a low-voltage event on the utility grid, regardless of whether anti-islanding is enabled. To have low-voltage ride-through capability, the DC bus voltage must be regulated so that the inverter can be operated as a constant current source. Because of issues found during this testing, it is recommended the testing be repeated over a larger range of conditions.

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1 Introduction

1.1 Objectives

The testing covered in this report had several objectives. The primary objective was to validate the effectiveness of proposed General Electric (GE) anti-islanding schemes. The schemes are described fully in "Study and Development of Anti-Islanding Control for Grid-Connected Inverters" [1]. Effectiveness was determined by the speed with which a scheme detected and ceased to energize the electric power system.

The secondary objectives were to:

1. Conduct parametric evaluation of the schemes with respect to control settings and load conditions, including controller gains, load power levels, and load quality factors
2. Examine the ability of the distributed resource to ride through a low-voltage condition on the utility grid.

Based on the lessons learned from testing, recommendations will be made to the Institute of Electrical and Electronics Engineers (IEEE) P1547.1 [2] working group.

1.2 Inverter Description

The inverter is based on a GE motor drive product platform. The platform has been used for motor drives with different ratings and applications. The same platform is being converted to grid-connected inverters for use with fuel cells, Sterling engines, wind turbines, and other distributed generation. The platform design is scalable, with available ratings of 38–1,445 kW. The inverter chosen for testing was rated 145 kW with 1.5 kHz switching frequency. In the testing, 8 kHz switching frequency was used. Therefore, the operational power was derated to be less than 145 kW.

Some key features of the inverter are:

- Insulated gate bipolar transistor devices
- Heat pipe technology for device cooling
- Coated, pre-formed, laminated bus assemblies
- Integral DC thru bus on common bus-fed inverters
- Independent door lock and lockout on each panel
- 32-bit digital signal processor
- Choice of local area network interfaces.

A typical platform interior and exterior are shown in Figure 1.

(a) Exterior (b) Interior

Figure 1. GE grid-connected inverter product platform

1.3 Test System Description

The tests were conducted at the GE Research Laboratory and the National Renewable Energy Laboratory (NREL) Distributed Energy Resources Test Facility. At the GE laboratory, the inverter output operated in parallel with an actual utility; at the NREL laboratory, a simulated utility was used. The simulated utility allowed testing under abnormal utility conditions. Information about the equipment used in testing can be found in "Testing of GE Universal Interconnection Device" [3].

Both laboratories used a high-voltage DC bus for the inverter input power. A high-voltage DC bus can be obtained from a high-voltage DC power supply, an active rectifier, or a diode rectifier. For this experiment, a diode rectifier was chosen because of its low cost. In the testing, two 480-VAC feeds were used. One was used as the input to the diode rectifier to represent the prime mover of a distributed generation system, and the other was used as a grid. To obtain sufficient DC bus voltage, a transformer was used at the diode rectifier input. Also, a pre-charge circuit was added to start the DC bus voltage before starting the inverter. The output of the inverter was connected with the grid and load as defined in IEEE P1547.1 Draft 5.1 [2].

Figure 2 shows the overall test system. The rectangle frame indicates the cabinet, which has all components packaged within. The interconnection system consisted of the grid-connect inverter and output contactors.

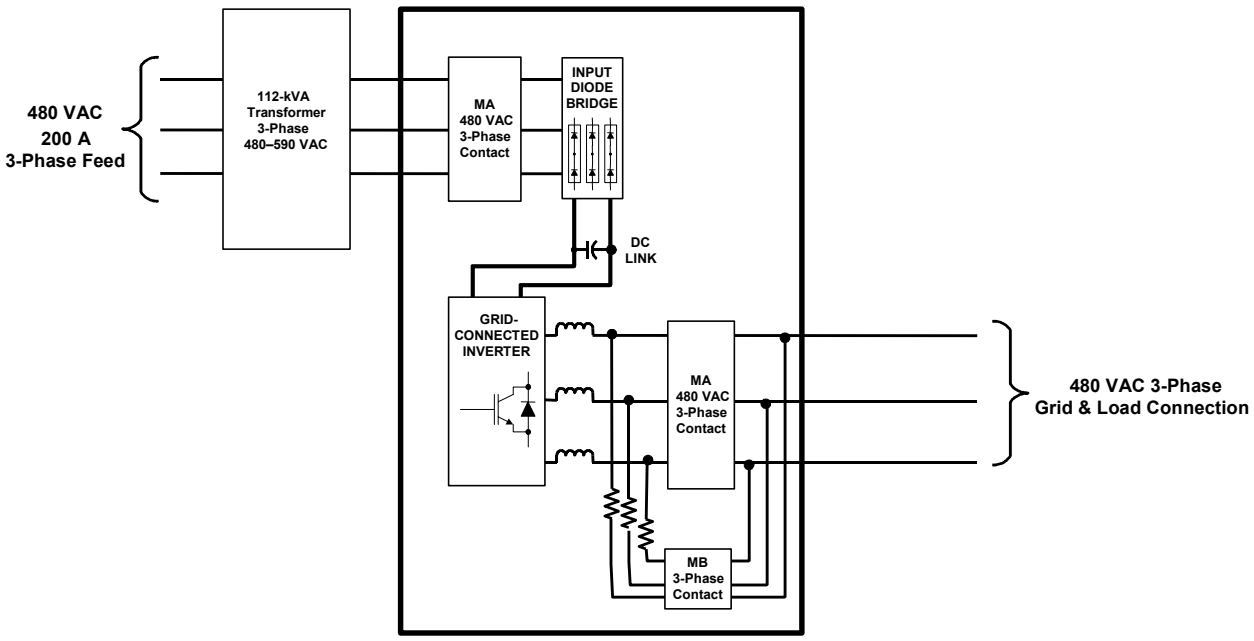

Figure 2. The inverter test package

1.4 Anti-Islanding Schemes

Unintentional islanding of distributed generation may result in power quality issues, interference with grid protection devices, equipment damage, and personnel safety hazards. A comprehensive survey of anti-islanding schemes indicated that existing solutions are too expensive (e.g., transfer trip), not secure (e.g., non-detection zone), or cause power quality degradation (waveform distortion) [1].

To overcome these problems, GE proposed a family of anti-islanding controls that is low-cost (only software code as part of inverter controls), certain (no non-detection zone), and robust to grid disturbances (low-voltage ride-through capability) and has negligible power quality effect (no intentional waveform distortion).

The proposed GE anti-islanding schemes are based on two concepts: positive feedback and DQ implementation (i.e., Park's transformation from ABC stationary coordinates to DQ coordinates). Positive feedback allows for secure detection of the island. The positive feedback, however, must be designed carefully so normal grid-connected operation, especially on a weak grid, is not affected by it. DQ implementation allows for the generation of a family of schemes that can be implemented. One benefit of DQ implementation is that, with its smooth signal injection, it leads to minimum waveform distortion compared with schemes that use a zero-crossing approach.

Two typical schemes are defined: the voltage scheme and the frequency scheme. Because of positive feedback in DQ implementation, the inverter, once islanded, will drive voltage or frequency out of nominal ranges so under/over voltage/frequency relay protection can be tripped. Combined with time-delay settings of under/over voltage/frequency, the proposed anti-islanding schemes can successfully ride through temporary low voltage without false trip yet detect islanding once the grid is actually lost. Traditional under/over voltage/frequency protection cannot reliably achieve both low-voltage ride-through and anti-islanding protection.

Detailed descriptions of the schemes and study results can be found in an earlier report [1].

2 Testing Results

For all tests, the system is configured as in Figure 3 and the islanding test protocol defined in IEEE P1547.1 [2]. EUT (equipment under test) refers to the interconnection system that consists of the inverter, controls, and output contactors.

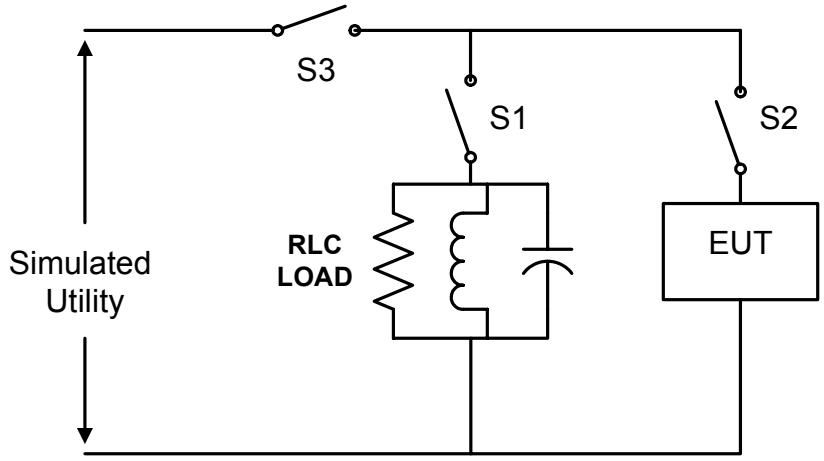

Figure 3. Unintentional islanding test protocol

2.1 Test Procedure[1]

1. Turn on switch S3 to make the utility line available.
2. Turn on switch S1 to connect the load. Load must be made available before connecting the equipment under test to avoid backfeed to the simulated utility. The RLC load is adjusted to provide a quality factor (Q_f) of 1.0. (When the quality factor is equal to 1.0, the following applies: $Q_L = Q_C = 1.0 \times P_R$.)
3. After the utility is available, turn on switch S2 to connect the inverter system. Set the inverter output to match the load power by monitoring the grid current at zero or near zero within measurement error.
4. After operating in steady state (for more than 1 minute), record all applicable settings of the inverter (e.g., anti-islanding gain, output power, and power factor) and the load power (e.g., kilowatts, kVar_L, and kVar_C). Utility or simulated utility voltage/frequency/current should also be recorded.
5. Open switch S3 to initiate islanding.
6. Record the time between the opening of switch S3 and when the inverter ceases to energize the RLC load. In this test, the inverter will cease to energize by shutting itself down.

[1] The test procedure is different from the one listed in P1547.1 D5.1 because of equipment limitation (e.g., no backfeed). In this test, the load is applied before connecting the equipment under test. In the GE laboratory, the load cannot be varied, so output power was adjusted.

7. Repeat steps 1–6 at two other power levels.
8. Repeat steps 1–7 for all three anti-islanding schemes. The first is voltage scheme only, the second is frequency scheme only, and the third one is the combined voltage and frequency scheme.

2.2 Test Results

Before testing was conducted, total harmonic distortion measurements were made with an anti-islanding scheme active and with it inactive. These tests showed there was no measurable difference when an anti-islanding scheme was active.

The results shown below are from the GE and NREL laboratory tests. For each condition, a test was conducted first without any anti-islanding schemes. Without any active anti-islanding schemes, the inverter can run on for more than 10 seconds and, in some cases, would run on indefinitely until it was manually shut down.

Figure 4 shows the test results from the NREL laboratory; Figure 5 shows the results from the GE laboratory. Both have anti-islanding control disabled. After the inverter and load were islanded, certain load-step transients were applied to investigate how the island system voltage and frequency responded to the transient. Small load-change increments (up to 250 W) did not affect the island. A significant load-step transient (a few percentage points of total load) was required to cause voltage or frequency trip. This shows that an island can be sustained even with a slightly variable load. Special measures are required to ensure the safety of distributed generation applications.

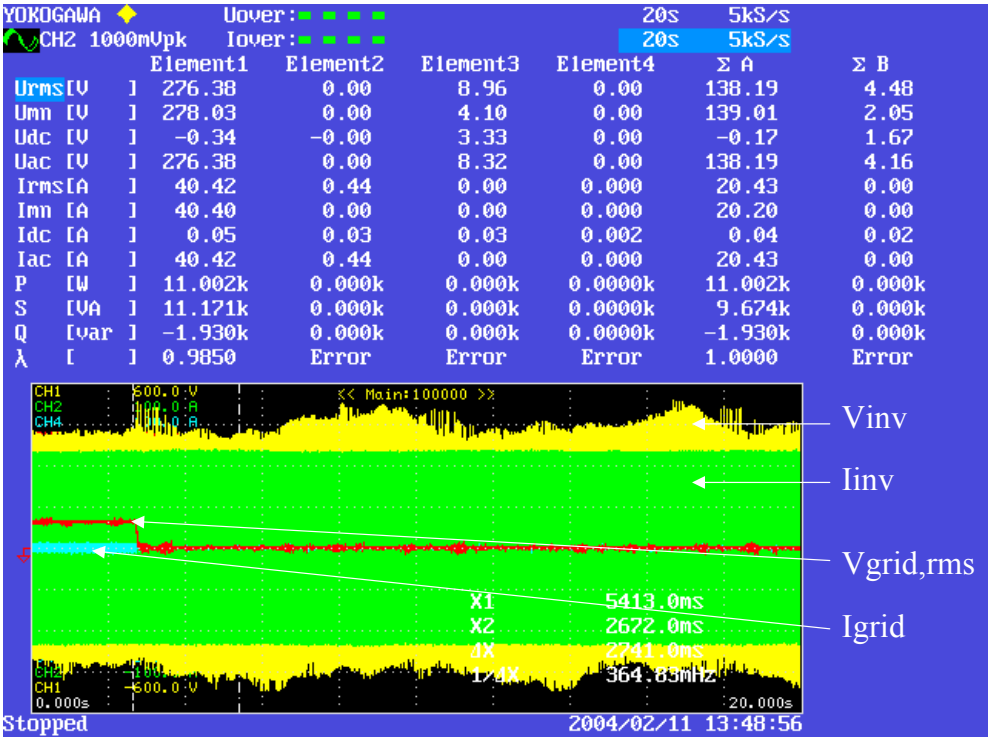

Figure 4. NREL laboratory test results without anti-islanding control

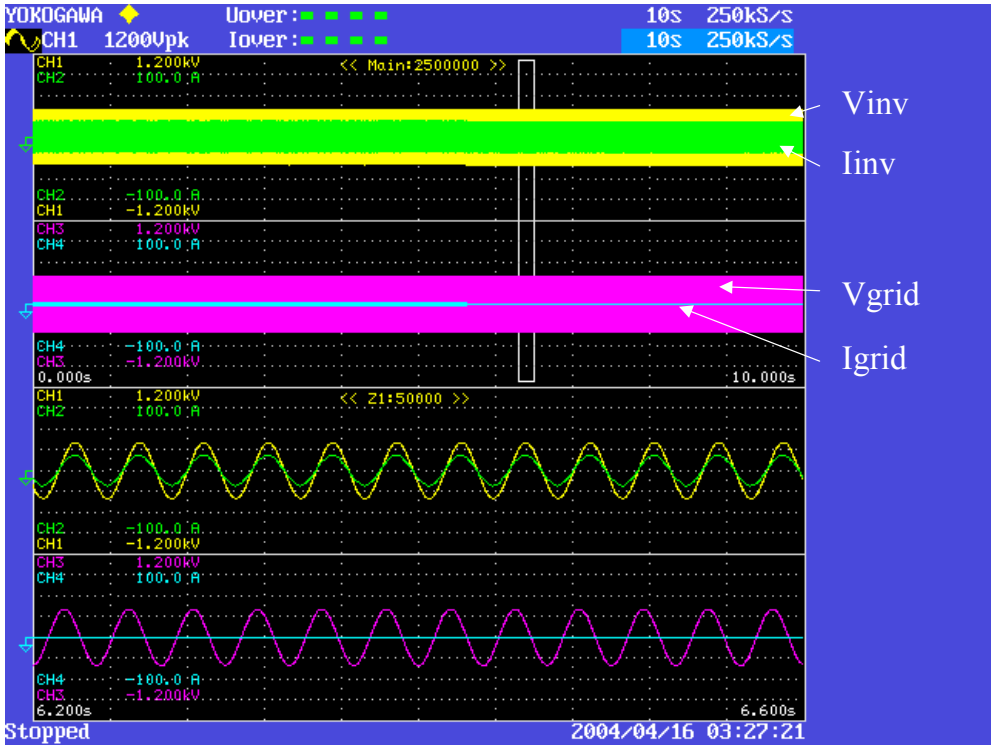

Figure 5. GE laboratory test results without anti-islanding control

After the test without anti-islanding, an anti-islanding scheme was enabled to demonstrate its effectiveness. Three schemes were tested.

2.2.1 Voltage Scheme

Three power levels were tested with the voltage scheme enabled. Table 1 shows the results of the test at the NREL laboratory.

Table 1. NREL Laboratory Test Results With Voltage Scheme

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Voltage	10	10	10.9	0.76	OV
Voltage	33	35.6	35.6	0.13	OV
Voltage	42	43.4	47.1	0.31	UV

Three tests were performed at each power level, and the results are repeatable. L and C were tuned so that net current flow to the utility was minimal.

One observation from testing was that tripping time had no correlation with power level. Based on the simulation and analysis conducted earlier [1], a lower power level should result in higher anti-islanding loop gain and, thus, better detection capability. However, this was not observed in testing.

To develop the correlation of power level and tripping time, more tests are needed. Further tests also need to tune the RLC to find the maximum tripping time. Figure 6 shows a representative test tripping in 0.76 seconds at 10 kW.

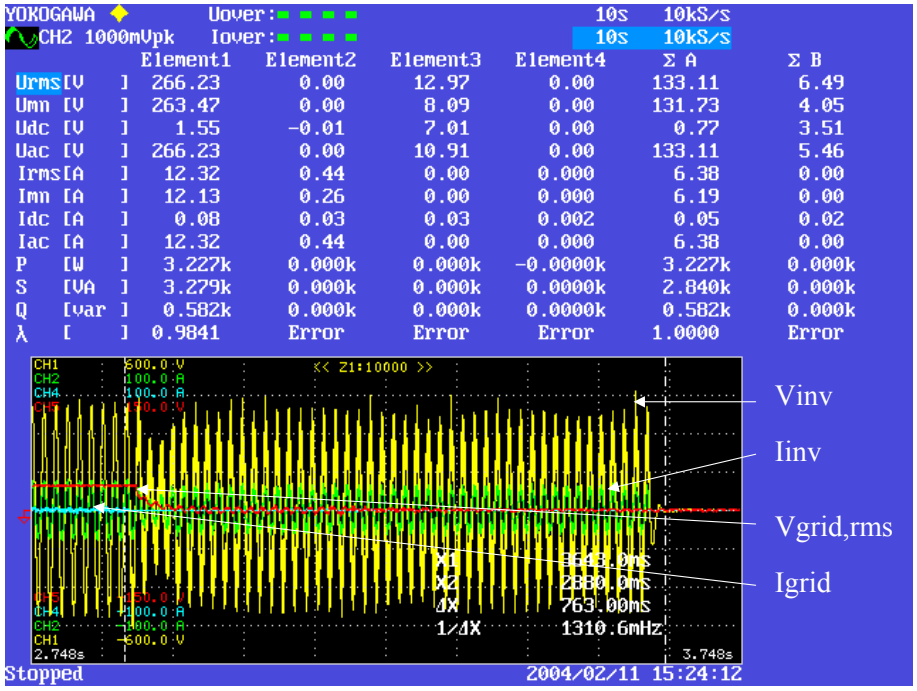

Figure 6. NREL laboratory test results with voltage anti-islanding scheme

2.2.2 Frequency Scheme

Table 2 shows test results from the GE laboratory. Insufficient test data were obtained from NREL testing because of time limitations.

Table 2. GE Laboratory Test Results With Frequency Scheme

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Frequency	10	27	27	1.3	UV
Frequency	15	27	27	1.5	UV
Frequency	20	27	27	1.6	OV

Three power levels were tested. Because L and C were kept constant, effective load quality factors were different with different power levels. Because power level and quality factor vary, the correlation between tripping time and power level or quality factor could not be generated. Future testing should try to keep the quality factor constant.

Figure 7 shows the test results of frequency scheme. The frequency drifts after islanding. However, in this case, the overvoltage protection tripped before frequency protection.

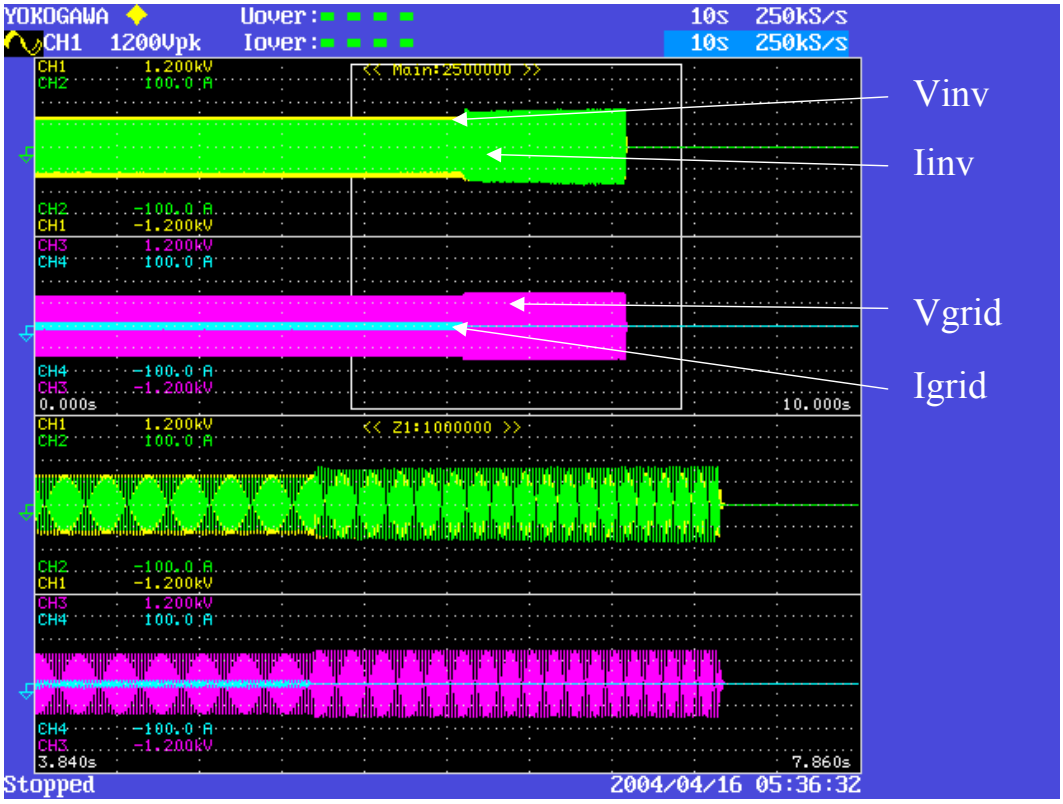

Figure 7. GE laboratory test results with frequency anti-islanding scheme

2.2.3 Combined Voltage and Frequency Scheme

Table 3 shows the test results for the combined voltage and frequency scheme. The results are from testing at the NREL laboratory.

Table 3. NREL Laboratory Test Results

Scheme	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
Combined	10.8	10	11.2	0.8	UV
Combined	33	35.6	35.6	1.5	UF
Combined	40	40	46.8	0.4	UV

It was found that the combined scheme had a slower tripping time than the voltage scheme but a faster tripping time than the frequency scheme. This indicates some interaction between the voltage and frequency schemes.

2.2.4 Gain Variation Effect

Tables 4 and 5 show gain variation effects on the voltage and frequency schemes. The results are from testing at the NREL laboratory.

With the gain reduced to a certain level, the positive feedback will not be effective, i.e., the loop gain drops below 0 dB and, thus, the islanded system may maintain stability if there is close power matching. This indicates that even if a positive feedback control is employed, there is a critical gain below which the positive feedback control will fail to detect unintentional islanding and result in certain non-detection zone.

Table 4. Voltage Scheme Gain Variation Test Results

Gain_V	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
10	42	43.4	47.1	0.31	UV
1	42	37.5	45	0.36	UV
0.2	42	37.5	45	>10	

Table 5. Frequency Scheme Gain Variation Test Results

Gain_F	R (kW)	L (kVar)	C (kVar)	Trip Time (s)	Trip On
100	20	27	27	1.6	UF
60	20	27	27	7	UF
10	20	27	27	>10	

2.2.5 Low-Voltage Ride-Through Test

A low-voltage ride-through test was also conducted. The procedure for the low-voltage ride-through test was different from that of the anti-islanding tests. The simulated utility was programmed to go momentarily to a low voltage and then recover to nominal voltage. The delay of the anti-islanding protection was set longer than the low-voltage period. The anti-islanding protection therefore would not react to the low-voltage event.

During the low-voltage ride-through test, however, the inverter tripped quickly after the low-voltage event. Increasing the delay setting in the anti-islanding control code did not allow the inverter to ride through the low voltage, and a fast trip was initiated by the inverter insulated gate bipolar transistor bridge. It was also tested without anti-islanding control. The inverter still tripped under the low-voltage event. The trip was caused by the self-protection of the inverter insulated gate bipolar transistor bridge.

The scenario was analyzed later. Because of the unregulated DC bus, the inverter system operated as a constant power source rather than a constant current source. As a result, a low-voltage event at the utility side of the inverter AC output caused large current, thus high voltage (Ldi/dt) at the inverter bridge. This high voltage initiated the overvoltage protection of the insulated gate bipolar transistor bridge because of the built in self-protection.

This scenario was simulated in Saber using the same topology as in the testing. A previous report [1] showed that, in simulation, the inverter has low-voltage ride-through capability when the DC bus is modeled as an ideal source. Therefore, the inverter can be regulated as an ideal current source.

To have low-voltage ride-through capability, the inverter must be designed, built, and verified as a constant current source, not a constant power source. During the low-voltage event, the power feeding the inverter from the DC bus must be controlled (e.g., using a crow bar) so the inverter can maintain constant current under low AC voltage. Figure 8 shows test results of the abnormal utility condition.

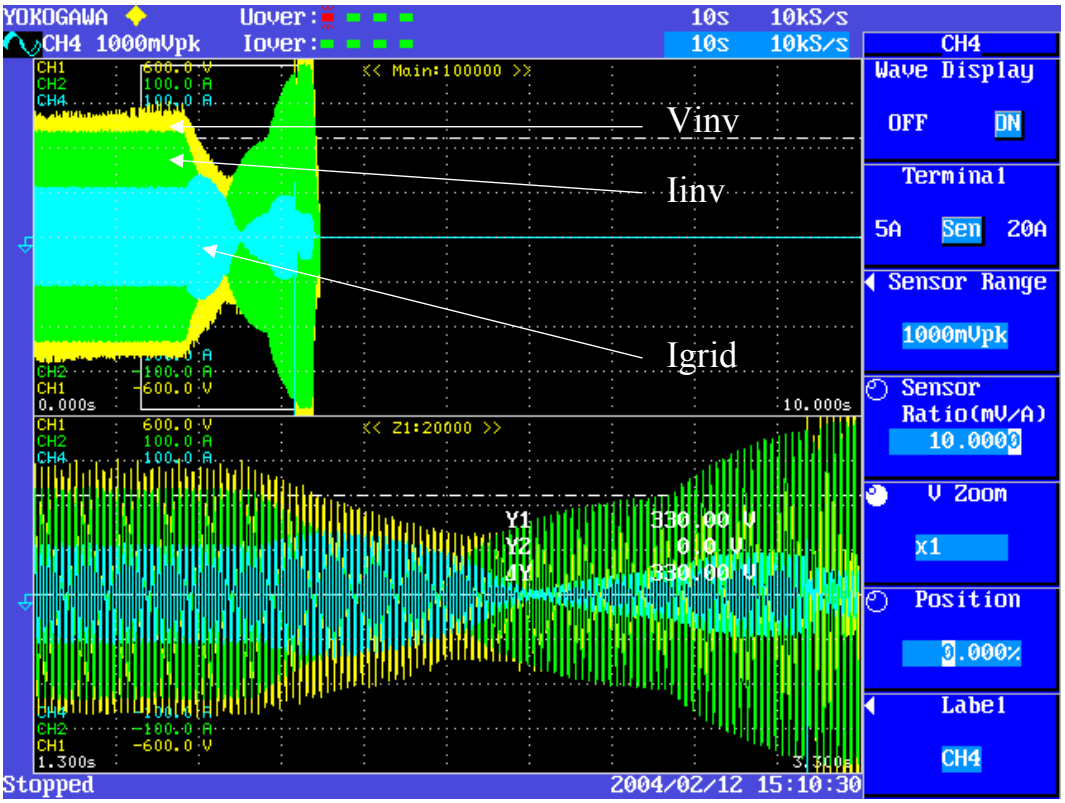

Figure 8. Test results with abnormal utility condition

3 Summary

The test results evaluated the effectiveness of the proposed inverter-based interface from GE.

3.1 Findings

- Using a matched load, the inverter can be islanded (more than 2 seconds) without any anti-islanding measures activated. In some cases, depending on load match and quality factor, the inverter can run on indefinitely.
- With the recommended anti-islanding parameter settings, the schemes work successfully (trip within 2 seconds) under all tested conditions, including worst-case generation/load balance as defined in the IEEE P1547.1 testing standard.
- The anti-islanding test results were repeatable under fixed conditions and parameter settings.
- The predicted effectiveness of the voltage and combined schemes did not correlate with load level. It was predicted the schemes would react more quickly at low loading conditions. However, this was not always observed in testing. More testing is needed to draw conclusions from these observations.
- When both voltage and frequency anti-islanding schemes are enabled, tripping time is not faster. This indicates there is some interaction between the schemes. When applying schemes, it is recommended one scheme be used so performance is more predictable. For the combined scheme, more study and tests are needed for better understanding of interactions.
- When a positive feedback control is employed, there is a critical gain below which the positive feedback control will fail to detect unintentional islanding and result in certain non-detection zone.
- Given the configuration of an unregulated DC bus obtained from a diode rectifier, the inverter cannot ride through a low-voltage event on the utility grid, regardless of whether anti-islanding is enabled. To have low-voltage ride-through capability, the DC bus voltage must be regulated so the inverter can be operated as a constant current source. Because of issues found during testing, it is recommended this testing be repeated over a larger range of conditions.

3.2 Recommendations

The anti-islanding tests at the GE and NREL laboratories were designed to evaluate the effectiveness of an interconnection system and proposed protection schemes based on IEEE 1547 requirements. Tripping time was used to determine the effectiveness of schemes. Although testing could show whether schemes were effective, more fine-tuned tests are necessary to find the maximum tripping time under each condition and the correlation between parameters and tripping time.

The test procedures defined in P1547.1 were not always followed because of limited equipment capabilities (e.g., load incremental variations and non-backfeeding simulated utility). Although P1547.1 allows for alternative testing procedures, the procedures used for this study should be further explored and verified as equivalent.

4 References

[E1] "1547-2003 IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems."

[E2] "IEEE P1547.1 Draft Standard for Conformance Tests Procedures for Equipment Interconnecting Distributed Resources With Electric Power Systems." Draft 5.1, 2004.

[1] Ye, Z.; Walling, R.; Garces, L.; Zhou, R.; Li, L.; Wang, T. "Study and Development of Anti-Islanding Control for Grid-Connected Inverters." NREL/SR-560-36243. Golden, CO: National Renewable Energy Laboratory, May 2004. Available at http://www.nrel.gov/docs/fy04osti/36243.pdf.

[2] "IEEE P1547.1 Draft Standard for Conformance Tests Procedures for Equipment Interconnecting Distributed Resources With Electric Power Systems." Draft 5.1, 2004.

[3] Ye, Z.; Finney, D.; Zhou, R.; Dame, M.; Premerlani, B.; Kroposki, B.; Englebretson, S. "Testing of GE Universal Interconnection Device." NREL/TP-560-34676. Golden, CO: National Renewable Energy Laboratory, August 2003. Available at http://www.nrel.gov/docs/fy03osti/34676.pdf.

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13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*

This report covers testing of General Electric-proposed anti-islanding schemes. The objectives were to: 1) Validate the effectiveness of the proposed anti-islanding schemes; 2) Conduct parametric evaluation of the schemes with respect to control settings and load conditions, including controller gains, load power levels, and load quality factors; and 3) Examine the ability of the distributed resource to ride through a low-voltage condition on the utility grid.

15. SUBJECT TERMS
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