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Hydrogenated Amorphous Silicon Emitter and Back-Surface-Field Contacts for Crystalline Silicon Solar Cells

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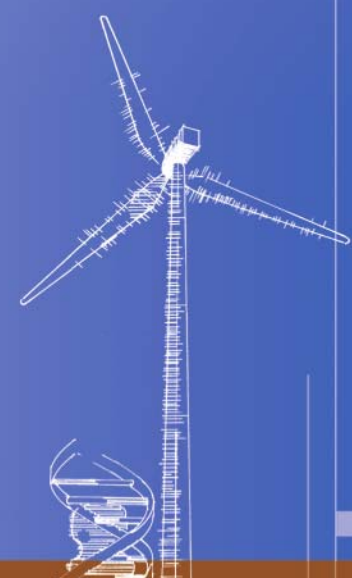

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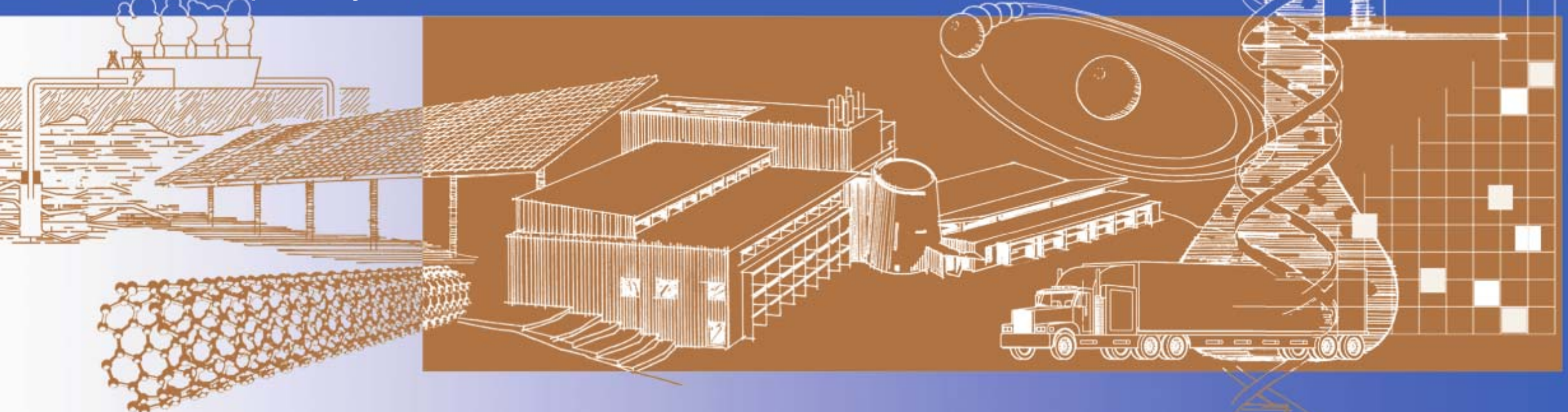

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Hydrogenated Amorphous Silicon Emitter and Back-Surface-Field Contacts for Crystalline Silicon Solar Cells

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ABSTRACT

Thin hydrogenated amorphous silicon (a-Si:H) layers deposited by hot-wire chemical vapor deposition (HWCVD) are investigated as emitters and back-surface-field (BSF) contacts to make silicon heterojunction solar cells on p-type crystalline silicon wafers. A common requirement for excellent emitter and BSF quality is minimization of interface recombination. Best results require immediate a-Si:H deposition and an abrupt and flat interface to the c-Si substrate. We obtain record 16.9% and 14.8% efficiencies on p-type planar float-zone (FZ) and Czochralski (CZ) silicon substrates, respectively, with HWCVD a-Si:H(n) emitters and Al-BSF contacts. Initial efforts with p-type HWCVD Si thin films as the BSF have yielded 12.5% efficiency on p-type CZ-Si.

1. Objectives

The a-Si:H/c-Si heterojunction (SHJ) solar cell [1,2] solves problems of high-temperature (>600ºC) device processing, because a-Si:H deposited below 250ºC can be used as the junction emitter and the back-contact BSF. The minority- carrier lifetime of a c-Si wafer is strongly affected by its thermal history, because of various defect-impurity mechanisms such as H-O centers, B-O complexes, thermal donors, and metal-dopant pairs. Commonly used lifetime enhancement techniques like P-gettering and H-passivation from SiN_x:H imposes difficult constraints on the temperature sequences used in the other silicon photovoltaic device processing steps. With the current industry trend toward thinner wafers or ribbons, wafer bowing caused by high-temperature metal back-contact processes is also a problem. If device-quality poly-Si thin-films on inexpensive, low-temperature substrates are achieved, low-temperature device processing will be essential. Our immediate goal is to extend to other materials and techniques the successes SHJ technology has enjoyed through plasma-enhanced chemical vapor deposition (PECVD) of a-Si:H on n-type c-Si substrates [3].

2. Technical Approach

We use HWCVD to deposit low-temperature hydrogenated silicon thin films as the emitter and BSF layers on p-type c-Si wafers. High-resolution transmission election microscopy (HRTEM) is a key post-deposition diagnostic tool and real-time spectroscopic ellipsometry (RTSE) [4] is employed to monitor thin-film properties such as crystallinity, thickness, and surface roughness during deposition. HWCVD could prove superior to the commonly used PECVD for SHJ solar cells because of simplicity of the system, reduced ion bombardment, low powder formation, and high densities of atomic hydrogen (H) generation that may passivate the wafer interface region. The device fabrication process is detailed elsewhere [5].

3. Results and Accomplishments

The crystallinity of the deposited Si layer is found to be very sensitive to the deposition temperature and crystal orientation of the substrate. Crystallinity, in turn, affects an SHJ solar cell's performance dramatically. In one set of experiments, RTSE clearly indicates epitaxial growth up to 30 nm in thickness on a (100) substrate at 200 C. On a (111) substrate at the same temperature, however, RTSE shows the film to be essentially a-Si as soon as the deposition starts. When the substrate temperature is higher, epitaxial growth can also be observed on (111) substrates. In Fig. 1, one can see that epitaxy persists for ~15 nm at 375 C on a (111) wafer, encompassing the i-layer (5 nm) and extending well into the n-layer. As a result, the open-circuit voltage (V_{oc}) of this device is only 487 mV. When we lower the substrate temperature to 100 C for both the i- and n-layer deposition, abrupt amorphous silicon growth is obtained, even on a (100) wafer, and a V_{oc} greater than 620 mV is obtained. Due to this tendency to grow epitaxial Si at higher HWCVD temperatures, V_{oc} decreases with increasing emitter deposition temperature. Figure 2 illustrates V_{oc} as a function of the i- and n-layer deposition temperatures (same for both layers) for 1.0 and 0.4 cm (111) substrates.

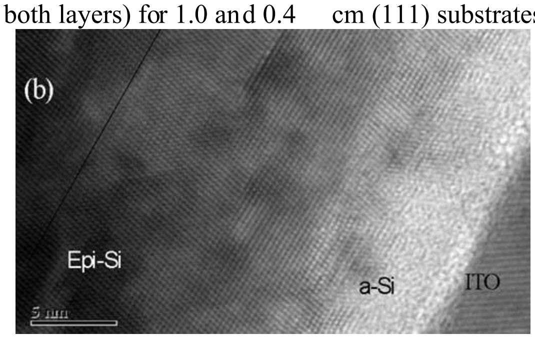

Fig. 1. Cross-sectional HRTEM image of Si deposition on a (111) wafer at 375 C. Line shows the wafer surface.

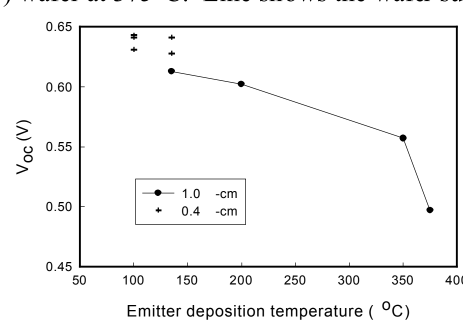

Fig. 2. V_{oc} vs. the i- and n-layer T.

The best voltage is obtained at substrate temperatures of 100º to 150°C. When an epitaxial film grows through the intrinsic layer and into the doped layer, V_{oc} is limited to 600 mV or lower, depending on the a-Si/c-Si interface roughness and quality of the epitaxy [6]. With carefully chosen conditions to avoid epitaxial growth, we have achieved V_{oc} values as high as 640 mV on p-type CZ-Si.

Using the optimized material for the a-Si:H emitter and Al-BSF, we consistently obtain high-performance SHJ devices on untextured substrates, as shown in Table 1. One of the solar cells (16C) was independentaly verified by NREL's Measurements & Characterization Division to have 16.9% efficiency (Fig. 3), the highest ever reported for a planar SHJ cell. Table 1 suggests slightly higher efficiencies due to calibration and spectral differences.

Table 1. 1-cm^2 SHJ solar cell results with the ITO/ a-Si:H(n)/c-Si(p)/Al-BSF structure (XT-10 solar simulator)

ID	V_{oc} (V)	J_{sc} (mA/cm^2)	F.F. (%)	Eff. (%)	Substrate (planar surface)
16B	0.640	33.55	79.4	17.1	FZ (100) p 1.0 ·cm
16C	0.644	33.70	78.5	17.0	FZ (100) p 1.0 ·cm
19A	0.638	33.37	78.6	16.7	FZ (100) p 1.0 ·cm
19B	0.639	33.10	76.5	16.2	FZ (100) p 1.0 ·cm
20B	0.639	33.55	78.9	16.9	FZ (100) p 1.0 ·cm
59A	0.641	32.56	78.5	16.4	FZ (100) p 0.6 ·cm
59B	0.644	32.72	79.9	16.8	FZ (100) p 0.6 ·cm
59C	0.646	32.90	79.7	16.9	FZ (100) p 0.6 ·cm
28B	0.612	30.87	78.3	14.8	CZ (100) p 1.2 ·cm

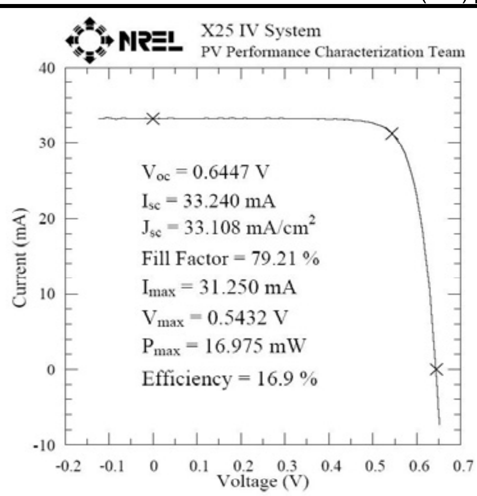

Fig. 3. Independently verified I-V curve of solar cell 16C.

To realize an entirely low-temperature SHJ device process, a thin-film silicon BSF with excellent minority-carrier passivation and majority-carrier conduction would be ideal. However, the large offset in the valence bands between c-Si(p) and a normal a-Si:H(p) often blocks the majority carriers (holes) from flowing to the back terminal, and can lead to undesired contact barriers. Good double-sided SHJ p-type cells have not been reported. By optimizing the silicon layer deposition conditions, we are able to obtain 12.5% (Table 2) efficiency using entirely low-temperature HWCVD Si deposition processes on a planar p-type CZ Si wafer. Further improvements are expected in electron passivation and hole conduction for higher performance.

Table 2. Performance of a 1-cm^2, double-sided, planar SHJ solar cell on a (100) CZ-Si(p) wafer (XT-10 solar simulator)

V_{oc} (V)	J_{sc} (mA/cm^2)	F.F. (%)	Eff. (%)
0.595	30.32	69.0	12.5

4. Conclusions

Effective passivation for both emitter and BSF layers can be obtained with immediate a-Si:H deposition and an abrupt and flat interface to the crystalline silicon (c-Si) substrate. This is accomplished by low-temperature deposition (<150ºC) of the thin silicon layers. A record efficiency of 16.9% for planar SHJ solar cells is achieved using screen-printed Al-BSF on untextured FZ-Si. Good performance (12.5%) is also achieved by a double-sided heterojunction structure on p-type CZ-Si for the first time. We expect still better performance when we incorporate high-efficiency features such as surface texturing and double-layer antireflection coating, and we continue to improve the heterojunction BSF.

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