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EVOLUTION OF CdS/CdTe DEVICE PERFORMANCE DURING Cu DIFFUSION

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ABSTRACT

Cu diffusion from a ZnTe:Cu/Ti back contact onto CdS/CdTe thin-film solar cells is studied. We find if Cu diffusion is insufficient, the entire CdTe layer is depleted. However, if Cu diffusion is excessive, the depletion width can become too narrow to provide optimum current collection. This analysis suggests that most contact processes used for CdS/CdTe devices are optimized (often unknowingly) to result in a depletion width that extends just far enough into the CdTe to yield the highest possible field in the region where light absorption occurs. Analysis of the samples with very high Cu concentration also suggests that Cu doping of CdS may affect carrier collection from the CdS.

INTRODUCTION

Understanding effects that diffusion of contact constituents into CdTe and CdS have on the operation and stability of CdS/CdTe thin-film photovoltaic (PV) solar cells remains an important area of study. Previous research has shown that a significant amount of Cu enters the CdTe layer during the 400°C CdCl₂ treatment, followed by additional Cu diffusion during either graphite/HgTe:Cu paste or ZnTe:Cu contact processes [1,2]. Although it is generally believed that too much Cu diffusion from the contact is detrimental to device stability, it has also been shown that acceptor formation in CdTe, required for high performance, is also linked to Cu diffusion.

Previous studies have shown that the use of a ZnTe:Cu contact interface layer can produce not only high-performance CdS/CdTe devices, but also allows for controlled diffusion of Cu. In earlier studies, this amount of Cu diffusion was increased from very low concentrations (consistent with uncontacted devices) to concentrations consistent with devices demonstrating optimum performance. These studies showed that device performance improved with decreasing depletion (space-charge) width in the CdTe. The reduction in depletion width is expected from increasing CdTe acceptor concentration.

In this work, we extend the study of Cu diffusion to include CdS/CdTe devices expected to have considerably more Cu than required for optimum performance. This is accomplished by using a ZnTe:Cu contact layer containing more Cu than used previously, by making this layer thicker, and depositing it at higher temperatures. These parameters combine to produce higher Cu concentrations in both the CdTe and CdS, allowing operational characteristics consistent with excessive Cu to be studied.

EXPERIMENTAL

The CdS/CdTe material used in this study was produced by vapor-transport deposition (VTD) outside of NREL [3]. CdS and CdTe layers were ~0.3 and ~4 μm thick, respectively. The ZnTe:Cu/Ti contact was produced at NREL as follows: Samples were placed into a multi-source vacuum processing chamber and preheated for 120 min. to the contact-fabrication temperature (samples were maintained at the substrate temperature throughout the contacting process). Substrate temperature was controlled using a resistive heater at constant voltages of 0, 20, 24, 28, 30, 32, 34, or 36 Volts, corresponding to temperatures of ~25°, ~200°, ~240°, ~280°, ~300°, ~320°, ~340°, or ~360°C, respectively. Substrate temperature was calibrated using an Al reference sample with an embedded thermocouple. Prior to ZnTe:Cu deposition, ion-beam milling was performed with a 3-cm Kaufman-type ion gun, operating at a beam energy and current of 500 eV and 6 mA, respectively, and operated using UHP-grade Ar at a chamber pressure of 2x10⁻⁵ torr. A 1-μm thick ZnTe:Cu layer (~9 at.% Cu, measured with electron microprobe) was deposited by r.f. sputter deposition, followed by d.c. sputter deposition of ~0.5 μm Ti. To ensure that any parameters linked to Ti diffusion were comparable for samples with different ZnTe:Cu deposition temperatures, the time interval between completion of ZnTe:Cu and Ti deposition was varied to assure that the heater temperature at the start of Ti deposition was fixed at ~185°C. Following deposition and sample cooling, a pattern of four individual 0.25-cm² cells were defined photolithographically on each sample. Cell definition was by two-step chemical etching, first using TFT Ti Etchant (Transene Co. Inc., Rowley, MA) to remove the Ti, followed by an aqueous solution containing 39% FeCl₃ to remove the ZnTe:Cu and CdTe. Following photoresist removal, unwanted areas were mechanically removed, and a perimeter contact to the SnO₂ layer was formed with ultrasonically soldered In.

Electrical analysis included light and dark current-voltage (LIV/DIV) measurements using an XT-10 solar simulator adjusted to approximate Global AM1.5 current from a CdS/CdTe reference cell. Capacitance-voltage (C-V) measurements were performed using an HP 4274 LCR meter at a frequency of 100 kHz. Voltage-dependent quantum efficiency (QE[V]) measurements were performed at a chopping frequency of 159 Hz, for both white-light bias (tungsten lamp set to produce a device current of ~1-sun) and dark bias configurations. Bias voltages used were -0.5, 0, 0.2, 0.4, and 0.6 volts.

The same devices used for the above electrical analyses were also used for compositional analysis (secondary ion mass spectrometry, SIMS) following chemical removal of the Ti layer with the TFT etchant. SIMS was performed from the contacted side of the devices using a Cameca IMS-3F instrument tuned for a mass resolution ($M/\Delta M$) of ~ 4000 to allow for separation of $^{63}\text{Cu}^+$ from $^{126}\text{Te}^{2+}$ species.

Near-field scanning optical microscopy (NSOM) measurements incorporated an atomic-force microscope (AFM) using a probe tip that emits 635-nm light within a 50-100-nm spot [4]. For NSOM studies, the thickness of the ZnTe:Cu was reduced to 50-200 nm, and the Ti layer was selectively patterned using photolithography [4].

RESULTS AND DISCUSSION

Figure 1 shows SIMS depth profiles of Cu for devices contacted at various heater voltages. As observed previously [5], higher contact temperature leads to increased Cu incorporation into the CdS layer. This study also reveals a systematic increase in Cu concentration in the CdTe layer with heater voltage. This trend may have been present in the earlier work, but is here more obvious due to thicker ZnTe:Cu layers and/or higher contact temperatures. Figure 1 also indicates the devices produced at 30 and 32 volts (near optimum conditions) have very similar compositional profiles, whereas devices contacted at 24 volts have lower Cu concentrations, and devices contacted at 34-36 volts have noticeably higher Cu concentrations.

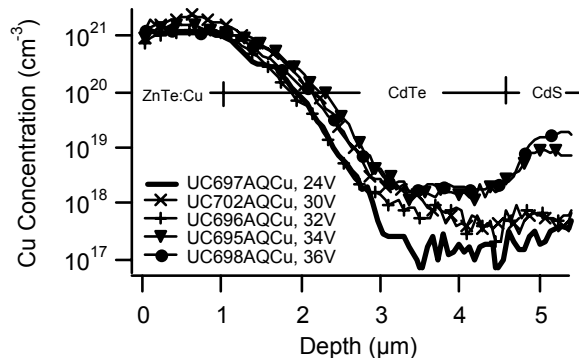


Figure 1. Quantified, high-resolution SIMS depth profiles of Cu concentration in CdTe/CdS devices contacted at various heater voltages. Figure shows approximate location of layer interfaces. Analysis is performed from the CdTe side of device.

LIV/DIV measurements indicate that optimum device performance (shown on Figure 2) results for heater voltages of ~ 30 -32 Volts. Further, because losses in voltage, fill factor and current are similar for devices contacted at lower (Fig. 2a) or higher (Fig. 2b) temperatures, LIV/DIV alone is a poor indicator of Cu concentration. Also, because increased Cu concentration with contact temperature is observed in both the CdTe and CdS layers, this analysis does not indicate if Cu in one or the other layer dominates performance changes. Nevertheless, Figure 1 together with Figure 2 clearly indicate that devices with either insufficient or excessive Cu concentration produce non-optimum performance.

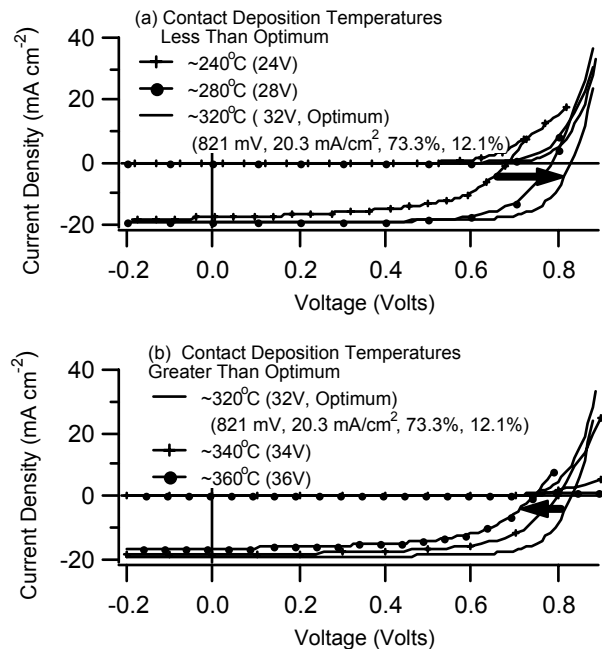


Figure 2. LIV/DIV of devices produced for this study that are expected to contain (a) insufficient or (b) excessive Cu. Optimum LIV values were measured at NREL using the X25 Simulator. Arrows show change in V_{oc} with increasing heater temperature.

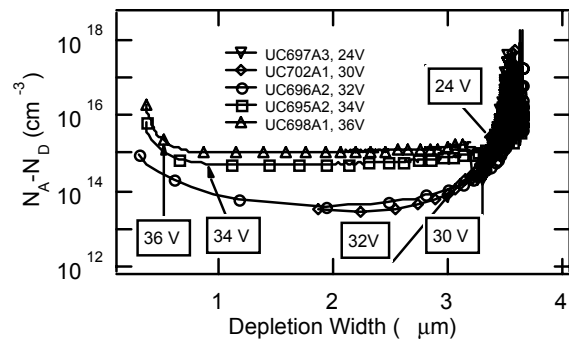


Figure 3. C-V analysis of CdS/CdTe devices contacted at various temperatures. Arrows indicate location of depletion width at zero bias for devices contacted at stated heater voltages.

C-V analysis (Figure 3) provides additional insight into how the contact affects the electrical properties of the device. Key points revealed are: 1) The depletion width decreases systematically with increasing contact temperature. This would be consistent with incorporation of Cu increasing the net defect concentration ($N_A - N_D$) in the CdTe. 2) Devices contacted at higher than optimum temperatures (34 and 36 volts) show significant increase in $N_A - N_D$ (from $5 \times 10^{13} \text{ cm}^{-3}$ to $\sim 1 \times 10^{15} \text{ cm}^{-3}$). This suggests that the considerable increased Cu concentration observed in Figure 1 at high contact temperature translates into increased net defect concentration in the CdTe. 3) Contact deposition at 34 and 36 volts also show a significant reduction in depletion width at zero-bias (from $\sim 3 \mu\text{m}$ to $< 1 \mu\text{m}$). This reduction is due partly to increased net defect concentration in the CdTe, but may be impacted by the requirement of space-charge neutrality following Cu compensation of CdS donors (to be discussed below). The

depletion width for these devices is so narrow that photo-generated carriers may increasingly be created outside the space-charge region in forward bias, and voltage-dependent collection ($J_L[V]$) should be observed. 4) Although the depletion width at zero bias for the optimum device (32 V) is relatively wide, it reduces significantly in forward bias so that at +0.6 V (about the maximum-power point for this device) the depletion width is similar to devices with much more Cu. Therefore, this device also could show $J_L[V]$.

To investigate if effects of $J_L[V]$ are limiting device performance, QE[V] analysis was performed on three devices contacted at heater voltages of 24 V, 32 V, and 36 V (i.e., insufficient, optimum, and excessive Cu, respectively). In all cases, QE[V] results were scaled so that each QE curve integrates to the appropriate device current (at the stated bias voltage) as measured under standard conditions at NREL. Figure 4 shows a comparison of the devices measured without voltage or light bias. This comparison reveals that the device with insufficient Cu demonstrates relatively uniform collection across its responsive range, as expected from a fully depleted device. In contrast, the device produced with excessive Cu shows reduction primarily in its red response, consistent with the depletion width being too narrow. Interestingly, the band edge of this device also shows a slight increase. As suggested from C-V analysis, the device produced near optimum conditions also shows some reduction in its red response, but not as severe as for the device with excessive Cu. QE response from the CdS shows very slightly reduced collection for the sample with insufficient Cu.

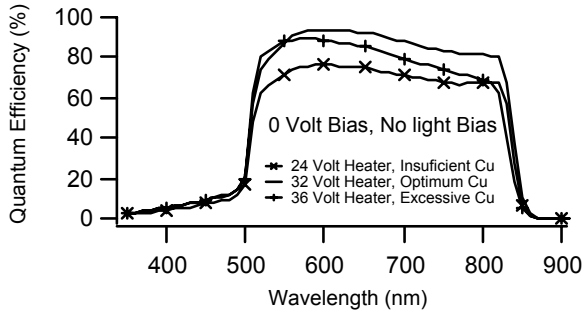


Figure 4. QE[V] analysis of CdS/CdTe/ZnTe:Cu/Ti devices measured with no light bias and 0 volts voltage bias.

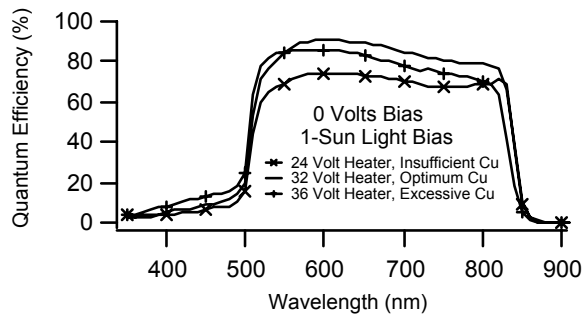


Figure 5. QE[V] analysis of CdS/CdTe/ZnTe:Cu/Ti devices measured with ~1-sun light bias and 0 Volts voltage bias.

Figure 5 shows the same three devices measured without voltage bias, but now adding ~1-sun white-light bias during the QE measurement. Results in the CdTe responsive range (500-850 nm) are similar to measurements

performed without light bias. However, the CdS region (350-500 nm) now shows a more pronounced increase in response with increasing contact temperature.

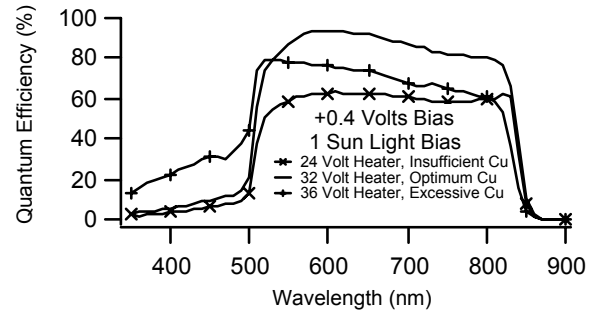


Figure 6. QE[V] analysis of CdS/CdTe/ZnTe:Cu/Ti devices measured with ~1-sun light bias and +0.4 Volts voltage bias.

Figure 6 compares the same three devices measured using both white-light bias and +0.4 volts bias (forward bias). Although not shown, the +0.4 volts bias reduces the spectral response from the CdTe region for samples containing insufficient or excessive Cu. Both these reductions are expected because of insufficient field strength within the depletion width (low Cu) and insufficient depletion width (high Cu). The spectral response for the optimum device is not altered appreciably by the +0.4 volts bias. We suggest this is because the depletion width remains sufficiently wide and the field sufficiently strong as the device enters forward bias conditions. Indeed, we propose this is an underlying criterion for many "optimum" contact processes. An important remaining feature of Figure 6 is the apparent increase in response from the CdS spectral region for the sample with excessive Cu.

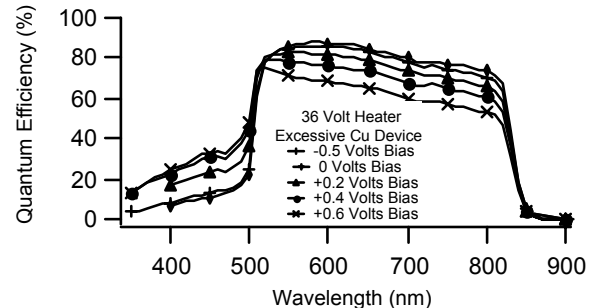


Figure 7. QE(V) analysis of CdS/CdTe/ZnTe:Cu/Ti devices with measured with ~1-sun light bias and stated voltage bias.

The apparent increased CdS response under forward-, light-bias measurement conditions is illustrated more clearly in Figure 7, where a full set of voltage-bias conditions (1-Sun white-light bias) are shown for the sample containing excessive Cu. The figure shows a systematic decrease in response for the CdTe spectral region with forward bias voltage. We suggest this reduction is due to the depletion width being too narrow to collect all the current (i.e., forward bias reduces already poor collection). In contrast, the CdS region shows a systematic *increase* in spectral response for forward-bias conditions.

Changes in CdS spectral response under various bias conditions have been studied historically in Cu_xS/CdS devices [6,7], and more recently in CdS/CdTe devices [8,9]. While our results also reveal changes in the apparent

response from the CdS region, some interesting differences exist. The most significant difference may be that enhanced CdS response is observed for white-light bias at a chopping frequency of 159 Hz. The small increase in CdS response shown in Figure 5, and the larger increase shown in Figures 6 and 7 implies, for high contact temperatures, Cu may compensate donors in CdS, forming a more intrinsic material and allowing the formation of a stronger drift field within the CdS. Indeed, using these assumptions, preliminary modeling using AMPS-1D suggests that moderate collection of carriers from light absorbed in the CdS appears possible (i.e., QE of ~20% at 400 nm). Alternatively, Cu could be passivating interface recombination pathways, enhancing minority-carrier transport at the CdS/CdTe interface.

In addition to providing insight into how the junction evolves in a CdS/CdTe device during back contacting, the previous analysis suggests that, for low Cu concentration, it may be possible to collect light incident from the back of the device (because the device is completely depleted, a drift field will be present near the back contact). In addition to demonstrating device response from backside illumination (note the ZnTe:Cu is transparent to light >550 nm), depletion-width control has also allowed the use of NSOM to spatially map collection near grain boundaries at the back of the device.

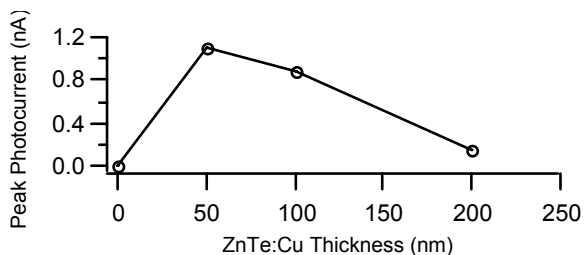


Figure 8. Peak NSOM-generated photocurrent from a CdS/CdTe/ZnTe:Cu/Ti device, measured as a function of ZnTe:Cu thickness.

Figure 8 shows that the highest NSOM photocurrent is produced when the ZnTe:Cu layer is only about 50 nm thick. This is also consistent with previous EBIC analysis that indicated an enhanced field near the back contact for devices with 50-nm ZnTe:Cu contact layers [3]. Figure 8 also shows the NSOM-generated device current decreases as the ZnTe:Cu layer thickness increases. Because the ZnTe:Cu layer ($E_g = 2.25$ eV) is transparent to the NSOM illumination source (1.95 eV), the systematic current reduction for ZnTe:Cu thickness > 50 nm is not due to absorption in the thicker ZnTe:Cu. Rather, we conclude Cu diffusion from the thicker ZnTe:Cu layers produces more acceptors in the CdTe, and these cause the outer edge of the space-charge layer to move away from the back surface, producing a non-depleted region (i.e., higher recombination) where the NSOM illumination is generating most of its carriers. Collection could be limited further by a potential barrier at the back contact forming a second depletion layer. The field of this second depletion layer would be in the opposite direction of the main junction field, causing electrons to drift away from the main junction.

NSOM analysis using a 50-nm-thick ZnTe:Cu film (as described above) is shown in Figure 9. In this figure, a comparison of the resulting AFM images (left side) and

NSOM images (right side) suggests, for this structure, collection is enhanced near grain boundaries. Further discussion of this NSOM analysis is presented elsewhere [4].

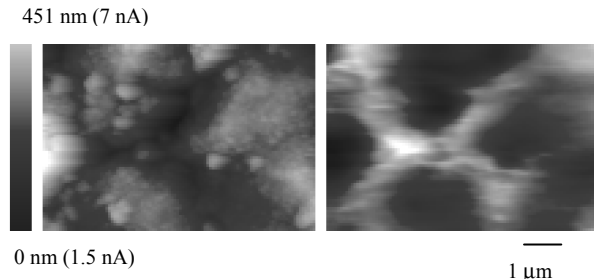


Figure 9. Left: AFM image of polycrystalline CdTe/CdTe/ZnTe:Cu solar cell. Right: NSOM image of the same region.

CONCLUSIONS

This study has shown that a CdS/CdTe PV device undergoes significant changes during formation of a back contact that uses a ZnTe:Cu contact interface layer. These changes not only involve formation of low-resistance barriers at the CdTe/ZnTe:Cu and ZnTe:Cu/metal interfaces, but also considerable changes in the net defect level within the CdTe bulk. This work also shows the CdS layer of a CdTe/CdTe device undergoes significant changes when sufficient Cu is allowed to diffuse into it at high temperatures. Specifically, changes in the apparent spectral response are revealed when the CdS contains sufficient Cu. Although these changes are similar to those reported by others, some interesting differences exist. At this time, we are investigating if these observations can be used to benefit the overall performance of thin-film CdS/CdTe devices.

ACKNOWLEDGEMENTS

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