August 2004 • NREL/CP-520-36669

Conference Paper

Toward Better Understanding and Improved Performance of Silicon Heterojunction Solar Cells

Preprint

T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz, and Q. Wang
National Renewable Energy Laboratory

V. Yelundur and A. Rohatgi
Georgia Institute of Technology

G. Bunea and A. Terao
SunPower Corporation

To be presented at the 14th Workshop on Crystalline Silicon Solar Cells and Modules
Winter Park, Colorado
August 8–11, 2004

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

NOTICE

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: mailto:reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Toward Better Understanding and Improved Performance of Silicon Heterojunction Solar Cells

T.H. Wang[1], M.R. Page[1], E. Iwaniczko[1], D.H. Levi[1], Y. Yan[1], H.M. Branz[1]
V. Yelundur[2], A. Rohatgi[2], G. Bunea[3], A. Terao[3], and Q. Wang[1]
[1]National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401
[2]Georgia Institute of Technology, 777 Atlantic Dr., Atlanta, GA 30332
[3]SunPower Corporation, 430 Indio Way, Sunnyvale, CA 94085

Abstract

The double-sided silicon heterojunction (SHJ) solar cell is more appropriate for n-type crystal silicon (c-Si) wafers than for p-type c-Si wafers because there is a larger band offset to the valence band edge of hydrogenated amorphous silicon than to the conduction band edge. Thin intrinsic and doped hydrogenated amorphous silicon (a-Si:H) double layers by hot-wire chemical vapor deposition (HWCVD) are investigated as passivation layers, emitters, and back-surface-field (BSF) contacts to both p- and n-type wafers. Passivation quality is studied by characterizing the SHJ solar cells and by photoconductive decay (PCD) minority-carrier lifetime measurements. The crystal-amorphous heterointerface is studied with real-time spectroscopic ellipsometry (RTSE) and high-resolution transmission electron microscopy (HRTEM) to detect phase change and material evolution, with a focus on better understanding the factors determining passivation effectiveness. A common feature in effective passivation, emitter, and BSF layers is immediate a-Si:H deposition and an abrupt and flat interface to the c-Si substrate. In this case, good wafer passivation or an excellent heterojunction is obtained, with a low interface recombination velocity (S) or a high open-circuit voltage (V_{oc}). V_{oc} greater than 640 mV, S less than 15 cm/sec, and efficiency of 14.8% have been achieved on polished p-type Czochralski-grown (CZ) Si wafers. Collaboration between NREL and Georgia Tech resulted in a 15.7%-efficient HWCVD-deposited SHJ cell on non-textured FZ-Si with a screen-printed Al back surface field (BSF), the highest reported HWCVD SHJ cell. Collaboration between NREL and SunPower demonstrated that HWCVD a-Si:H passivation can be better than the conventional oxides, with a low surface recombination velocity of 42 cm/sec on textured n-type FZ-Si.

1. Introduction

The most important material property for photovoltaic (PV) silicon, minority carrier lifetime, is strongly affected by the thermal history of the silicon substrate because of various defect-impurity mechanisms such as H-O centers, B-O complexes, thermal donors, and metal-dopant pairs. Ulyashin et al. [1] demonstrated that significant enhancement in minority carrier lifetime can be achieved by thermally annealing silicon substrates in N_2 at 450ºC for 20 min; increases of 200%, 150%, and 200% in lifetime were seen for CZ-Si, FZ-Si, and multicrystalline silicon, respectively. Schultz et al. [2] showed that by lowering the normal 1050ºC oxidation for 1 hour to 800ºC for 4 hours, the dramatic lifetime degradation of 65% by 1050ºC oxidation was cut to 5% loss only for multicrystalline silicon, highlighting the potential advantages of low-temperature processing. Various lifetime enhancement techniques like P-gettering and H-passivation from SiN_x:H which are commonly used for PV

silicon impose difficult constraints on the temperature sequences used in the other device processing steps. If polycrystalline thin-film silicon on inexpensive, low-temperature substrates is achieved, low-temperature device processing will be essential. With the current industry trend toward thinner wafers or ribbons, wafer bowing caused by high-temperature metal back contact is a great concern. The a-Si:H/c-Si heterojunction solar cell is a good solution to these problems because a-Si:H deposited below 250ºC can be used as the junction emitter, the passivation layer, and the full contact BSF. The simple planar structure of the SHJ may also help control processing costs.

2. Status of silicon heterojunction solar cells

The SHJ solar cell grew out of research on a stacked amorphous/crystalline silicon cell design by Hamakawa et al. [3,4] in 1983. In 1990, a more advanced silicon heterojunction device structure was developed by Sanyo as the Heterojunction with Intrinsic Thin-layer (HIT) cell, with a doped a-Si(doped)/μc-Si(undoped)/crystalline Si structure [5]. In 1991, Sanyo changed their μc-Si:H undoped layer to a-Si:H [6]. According to Taguchi et al [7], in the normal a-S:H/c-Si heterojunction cells, the open-circuit voltage (V_{oc}) and fill factor were lower than those of conventional diffused solar cells. These poor properties are a result of the recombination process throughout the depletion region at the a-Si/c-Si heterojunction. Moreover, doped a-Si layers have mid-gap state densities above 10^{18} cm^{-3} [8] that would increase dark tunneling leakage currents. This tunneling process is suppressed by inserting the intrinsic a-Si:H spacer which contains only 10^{15} to 10^{16} cm^{-3} of midgap defect levels. With this intrinsic a-Si:H spacer, a V_{oc} of 600 mV and 1-cm^2-cell efficiency of 14.8% was soon demonstrated on an n-type CZ-Si wafer [9]. Sanyo then successfully applied the HIT structure to the backside of the cell as a back surface field (BSF) layer. By using the HIT structure on both sides of the cell with a highly reflective metal as the back electrode and by optimizing other conditions, they obtained an open-circuit voltage of 644 mV and an efficiency of 20% for an aperture area of 1 cm^2 [9]. In late 1997, Sanyo started mass production and have since achieved laboratory cell efficiency of 21.3% on 100-cm^2 cell area and an open-circuit voltage of 714 mV. The production cell and module efficiencies are 19.5%, and 17%, respectively. These results are for n-type CZ-Si after refinements to their process that include reduced H-plasma damage, low-temperature screen-printed metal grids of 2-mm spacing, and steps to upgrade minority carrier lifetime of the wafers [10].

Inspired by the outstanding performance of the HIT cells, dozens of research groups [11, 12] throughout the world have been trying to duplicate Sanyo's results with only partial success so far, due to insufficient understanding of the heterointerface and lack of open literature about critical surface pretreatments and other process steps. In addition, because p-type silicon is a more common PV material, SHJ cells on p-type c-Si are more popular than on n-type. But it has been difficult to achieve high efficiency with double-sided HIT cells on p-type c-Si. Nevertheless, with a high-temperature BSF (such as alloyed Al or diffused B), SHJ cells based on p-type c-Si have been encouraging. For example, on a textured p-type CZ-Si with an Al-BSF, Tucci et al. [13] made a 17% efficient 2.25-cm^2 SHJ solar cell with a V_{oc} of 600 mV by using a $CrSi_2$ thin layer to enhance the emitter conductance. A 1-cm^2 cell that is 15.9% efficient with a V_{oc} of 612 mV has also been reported on textured p-type CZ-Si with a boron-diffused BSF [14].

To understand why SHJ cells have been problematic, it is essential to carefully consider the impacts of heterojunction band offsets. The literature consensus is that there is a larger band offset (~0.45 eV) at the valence band edges and a smaller band offset (~0.15 eV) at the conduction band edges [e.g., 15] reflecting the small difference (~0.15 eV) in electron affinity (distance from the conduction band edge to the vacuum level) between c-Si (~4.05 eV) and a-Si:H (~3.90 eV). With this information, we may construct a schematic band diagram as shown in Figure 1, in which the left/right diagram is for the n-type/p-type c-Si based HIT structure respectively and the plus/minus signs (+/-) represent positively/negatively charged dangling bond (DB) defects accordingly.

Sanyo's double-sided HIT cell on n-type CZ-Si uses a total thickness of only 10 nm of a-Si:H(p/i) as the emitter and a slightly thicker 20 nm of a-Si:H(i/n) as the BSF. At the front junction, the larger valence band offset results in a potential well in which minority carrier holes can be trapped, preventing efficient photo-generated carrier transport. Pure thermionic emission is unlikely to provide enough transport for the holes due to the high barrier. However, the trapped holes may be able to tunnel across the thin a-Si:H(i) layer into the a-Si(p) layer, possibly with some thermal and trap assistance. On the backside, the large valence band offset and thicker i-layer provide a back surface "mirror" for holes. This Si:H(i/n) stack does not much hinder electron transport because the offset in the conduction band edges is small. Thus the a-Si:H(i/n) provides an excellent back contact with adequate majority carrier electron transport and excellent passivation repelling minority carrier holes from the back contact.

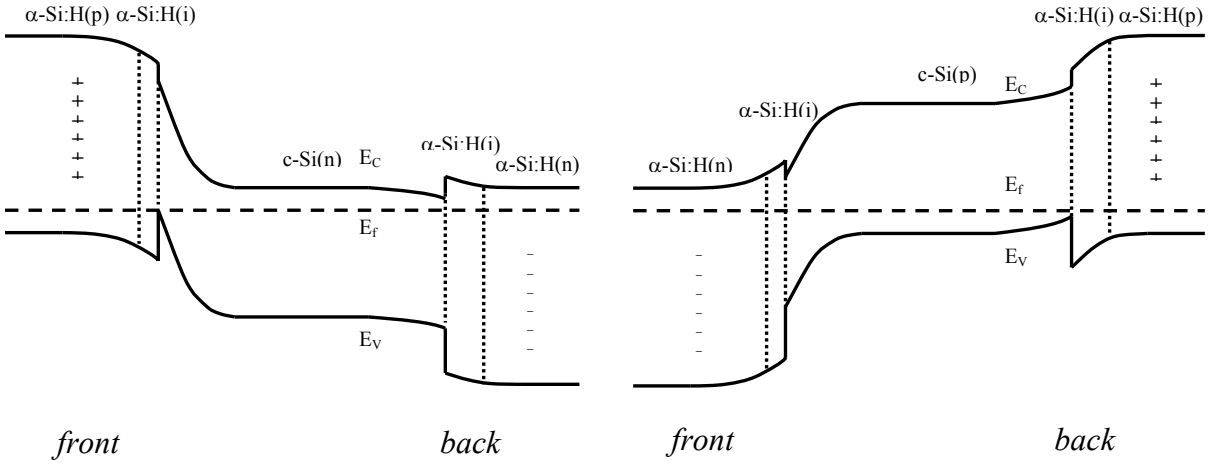

Figure 1. Schematic band diagram of double-sided HIT: on n-type c-Si (left) and on p-type c-Si (right).

We can apply this understanding of the heterojunction band offsets to a p-type c-Si based double-sided HIT cell with an a-Si:H(n/i) emitter on the front surface and with a-Si:H(i/p) as the BSF contact on the back surface. The minority carrier electron collection will be impeded by only a small barrier created by the small band offset in the conduction band edges. Minority carrier collection should thus be even easier than in the n-type c-Si based HIT cell, although the built-in voltage (from the vacuum level bending) at the front junction is comparable to a c-Si homojunction but much less than the a-Si(p/i) on c-Si(n) case. On the backside, however, the small conduction band offset provides a much less

effective mirror for the minority carrier electrons. Worse, the larger offset in the valence band edges would present a large barrier for majority carrier holes to flow through to the back contact unless one sacrifices passivation by using a thinner or no i-layer to use trap-assisted tunneling. An alternative is to use a-SiC:H [16] or other alloys with bigger conduction band offsets to c-Si as the BSF for p-type c-Si. If, indeed, the band offset is much larger in the valence band edges than in the conduction band edges then: (1) a-Si(n/i) will be a good emitter for p-type c-Si with a built-in voltage comparable to a silicon homojunction; (2) a-Si(p/i) with a very thin i-layer will be a very good emitter for n-type c-Si with a higher built-in voltage than a silicon homojunction; (3) a-Si(i/p) is a poor BSF for p-type c-Si; and (4) a-Si(i/n) is an ideal BSF for n-type c-Si.

All the amorphous layers in the better performing heterojunction cells reported so far have been deposited by plasma-enhanced chemical vapor deposition (PECVD). Obtaining high performance of such cells by HWCVD, in which precursor gases (e.g., silane) are decomposed by a hot W filament at about 2000°C, has been a challenge [17, 18]. However, HWCVD could prove superior to PECVD for silicon heterojunction solar cells because of higher deposition rates, reduced ion bombardment of the base wafer, and high densities of atomic hydrogen (H) generation that may passivate the wafer interface region.

3. Collaborative research at NREL, Georgia Tech, and SunPower

For the reasons discussed above, we began our silicon heterojunction solar cell work at NREL with an a-Si(n/i) emitter on Al-BSF p-type c-Si, even though a completely low-temperature heterojunction process is the ultimate goal. We focus on emitter and BSF optimization with effective interface passivation. With a more complete understanding and control of the HWCVD heterointerfaces, we can apply them to other types of devices including a double-sided HIT structure.

One problem that HWCVD presents is a tendency to grow epitaxial silicon on clean c-Si substrates [19], even at temperatures as low as 200°C. In high-efficiency heterojunction solar cells, a thin (~5 nm) intrinsic hydrogenated a-Si:H layer must be interposed between the base wafer and the heavily doped emitter, as discussed above. If epitaxy extends through the i-layer, the defective interface will be contacted by the doped a-Si:H which is a much less effective passivant than the intrinsic layer. Partial epitaxy, highly defective epitaxy, or a mixed phase i-layer can all cause detrimental high dark currents, because the a-Si/c-Si interface area or defect density will be large. The additional dark-current path through inadequately passivated interface states leads to a low V_{oc}. Therefore, V_{oc} and the interface recombination velocity (S) are important indicators of the effectiveness of an a-Si:H/c-Si heterointerface. Our earlier HWCVD effort yielded 13% efficiency and a V_{oc} of merely 580 mV [18]. After careful interface studies, we achieved V_{oc} over 640 mV [20], S below 15 cm/sec, and efficiency of 14.8% on p-type CZ-Si with no surface texturing and single layer anti-reflection coating (ARC). Collaboration with Georgia Tech has resulted in a 15.7% cell on non-textured p-type FZ-Si with a Georgia Tech screen-printed Al-BSF and single layer ARC. This is believed to be the highest reported efficiency for a HWCVD silicon heterojunction cell [21]. We expect still better performance when we incorporate surface texturing and double-layer ARC. Working with SunPower Corp's randomly textured FZ-Si samples, we obtain a surface recombination velocity of 42 cm/sec, lower than the value of 52

cm/sec by high-temperature oxidation followed by forming gas annealing.

3.1. *Effect of crystallinity in Si layer*

The crystallinity of the deposited Si layer is found to be very sensitive to the crystal orientation of the substrate. In one set of experiments, RTSE clearly indicates epitaxial growth up to 30 nm in thickness on a (100) substrate at 250°C. On a (111) substrate at the same temperature, however, RTSE shows the film to be essentially a-Si as soon as the deposition starts. When the substrate temperature is higher, epitaxial growth can also be observed on (111) substrates. In Figure 2a, the single-crystal silicon characteristic peaks at 3.38 eV and 4.25 eV in the imaginary part of the pseudo-dielectric function, $\langle\varepsilon_2\rangle$, calculated directly from the measured parameter Ψ and Δ by RTSE, persists for 1.5 min (~15 nm) at 500°C on a (111) wafer, enduring the i-layer (5 nm) and extending well into the n-layer. This is confirmed by the HRTEM image of Figure 2b. As a result, the V_{oc} of this device is only 487 mV.

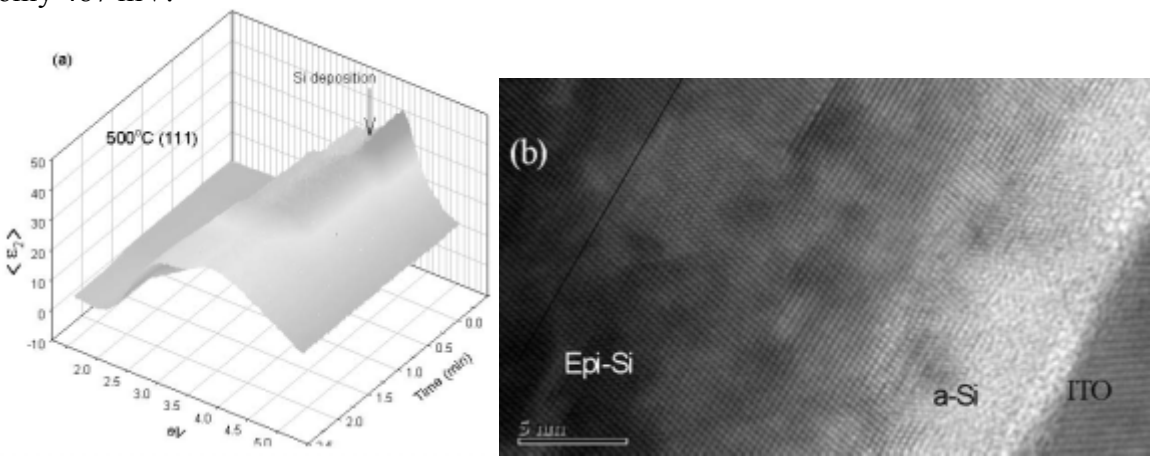

Figure 2. Si deposition on a (111) wafer at 500°C: (a) $\langle\varepsilon_2\rangle$ evolution. Arrow shows start of growth; (b) HRTEM image. Line shows the wafer surface.

As shown in Figure 3, when we lowered the substrate temperature to 100°C for both the i- and n-layer deposition, abrupt amorphous silicon growth is obtained, even on a (100) wafer. A V_{oc} of 628 mV is obtained on this device. Because of the tendency to grow epitaxial Si at higher HWCVD temperatures, V_{oc} decreases with increasing emitter deposition temperature. Figure 4 is a plot of V_{oc} as a function of the i- and n-layer deposition temperatures (same for both layers) for 1.0 and 0.4 Ω·cm (111) substrates. The best voltage is obtained for substrate temperatures of 100 to 150°C. Once an epitaxial film is grown through the intrinsic layer and into the doped layer because of too high a deposition temperature, V_{oc} is limited to 600 mV or lower, depending on the a-Si/c-Si interface roughness and quality of the epitaxy. With carefully chosen conditions to avoid epitaxial growth, we have achieved V_{oc} exceeding 640 mV on p-type CZ-Si.

The beneficial effect of an abrupt interface is shown in interface recombination velocity S. Figure 5 shows the S value as a function of i-layer deposition temperature, for passivations with the n-layer temperature fixed at 300ºC(*). Reducing the i-layer temperature reduces S as Si epitaxy is suppressed. (*The higher n-layer temperature is used for dopant

activation in this case. In our solar cell process, activation is accomplished during the 30-min thermal ITO evaporation step at about 200ºC.)

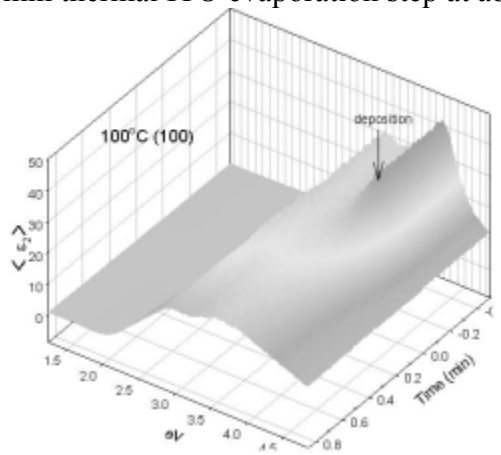

Figure 3. $\langle\varepsilon_2\rangle$ for 100°C on (111).

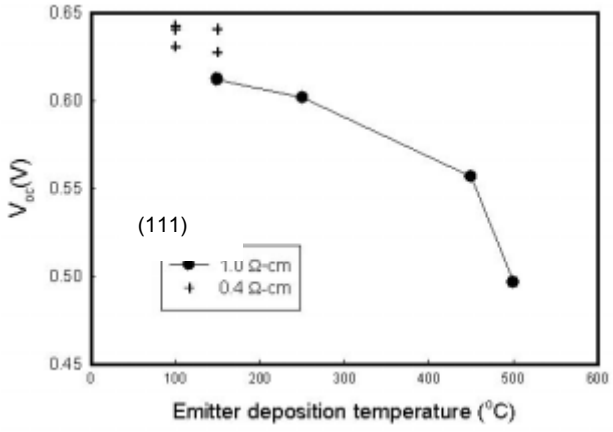

Figure 4. V_{oc} vs. the i- and n-layer T.

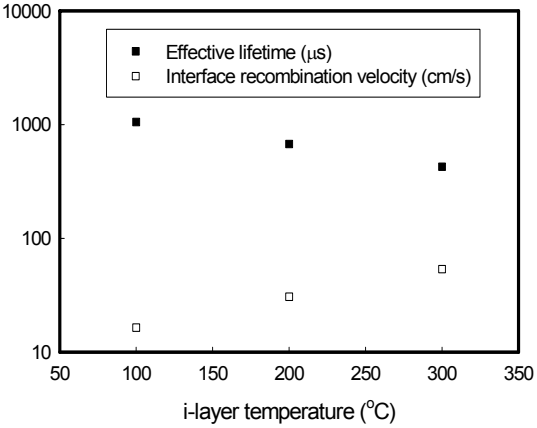

Figure 5. S vs. i-layer T (n-layer T = 300ºC)

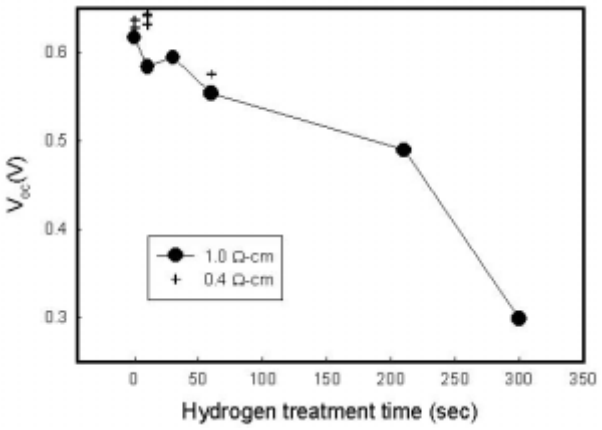

Figure 6. V_{oc} vs. H pre-treatment

3.2.*Hot-wire pre-treatment with H_2*

Short atomic H pre-treatment with hydrogen gas (H_2) cracked by the hot wire may etch any residual surface silicon oxide, clean the silicon surface, or passivate defects in the base wafer. However, from HRTEM and RTSE, we find that prolonged H pre-treatment actually damages the c-Si surface, resulting in a rough interface and partial epitaxy. As summarized in Figure 6, V_{oc} decreases as H pre-treatment gets longer. From Figure 6, very little or no H pre-treatment is better to maintain a low density of interface states. This is especially true on textured wafers. On a 200-μm thick, randomly textured, n-type FZ-Si wafers, 287Å of oxide formed by dry oxidation and forming gas annealed at SunPower resulted in an effective lifetime of 193 μs (S=52 cm/sec) at $1.3x10^{16}cm^{-3}$ carrier density, as measured with a Sinton transient photoconductive decay measurement system. After stripping the oxide in hydrofluoric acid and depositing a symmetric a-Si(n/i)/c-Si/a-Si(i/n) structure (with no H pre-treatment), we obtain 238 μs effective lifetime (S=42 μs) at the same injection level after optimizing the deposition conditions. Table 1 shows the effect of H pre-treatment duration and i/n-layer thickness on the effective lifetime. It is shown that

any H pre-treatment seems to lower the effective lifetime or increase the S value.

Table 1. Effect of H_2 treatment and i/n-layer growth time (in seconds) on effective lifetime

H_2 at 100°C	i-layer at 100°C	n-layer at 300°C	Effective lifetime (μs)
10	10	210	136.8
10	30	210	92.5
10	10	420	95.5
10	10	315	133.9
5	15	210	136.6
0	10	210	237.9
20	10	210	122.0

4. Summary

If the valence band offset is larger than the conduction band offset, a-Si(n/i) and a-Si(p/i) can be good emitters for p-type c-Si and n-type c-Si wafers, respectively. However, although a-Si(i/n) will be an excellent back contact for n-type c-Si, a-Si(i/p) will make a poor back contact to p-type c-Si. The large valence band offset at the c-Si(p)/a-Si(i/p) interface will present a large barrier to hole collection and the small conduction band offset will provide an inadequate minority carrier mirror.

A common feature in effective passivation, emitter, and BSF layers is immediate a-Si:H deposition and an abrupt and flat interface to the crystalline silicon (c-Si) substrate. In this case, good wafer passivation or an excellent heterojunction is obtained with a low interface recombination velocity or a high V_{oc}. Reduced V_{oc} or increased S is found whenever the heterointerface is not abrupt and flat. Wafers at higher temperature and with (100) orientation are more likely to lead to deleterious epitaxial growth than those at lower temperature or with (111) orientation. A short (10 s) H_2 treatment with the hot wire prior to the a-Si:H film deposition may improve carrier transport across the interface, but prolonged treatment can damage the c-Si surface, leading to a rough interface with partial epitaxy, reduced V_{oc}, and higher S. Textured c-Si surface is especially adversely affected by H_2 treatment. With these findings, V_{oc} greater than 640 mV, S less than 15 cm/sec, and efficiency over 15.0% have been achieved on polished p-type Czochralski-grown (CZ) Si wafers. Collaboration between NREL and Georgia Tech produced an SHJ cell with efficiency above 15.7% on non-textured FZ-Si with a screen-printed Al-BSF. This is the highest reported efficiency for an HWCVD-deposited silicon heterojunction cell. We expect still better performance when we incorporate surface texturing and double-layer ARC. A collaboration between NREL and SunPower demonstrated a low surface recombination velocity of 42 cm/sec on textured n-type FZ-Si by a-Si:H passivation.

Acknowledgements

The authors would like to thank Charles Teplin, Yueqin Xu, Scott Ward, Anna Duda, Richard Ahrenkiel, Steve Johnston, Richard Crandall, and Daniel Friedman for their valuable

technical assistance and discussions. This work is supported by U.S. DOE under Contract #DE-AC36-99G010337.

References

[1] A. Ulyashin, R. Bilyalov, A. Brück, M. Scherff, R. Job, W. Fahrner, J. Poortmans, *Proceedings CD of the 3rd World Conf. PV Energy Conv.*, 4p-A8-69, Osaka, Japan, May 11-18, 2003

[2] O. Shultz, S.W. Glunz, J.C. Goldschmidt, H. Lautenschlager, A. Leimenstoll, E. Schneiderlöchner, G.P. Willeke, *19th European PV Solar Energy Conf.,* 2DO.3.2, Paris, France, June 7-11, 2004

[3] K. Okuda, H. Okamoto, Y. Hamakawa, *Jap. J. Appl. Phys.,* Vol. 22 No. 9 (1983) L605

[4] Y. Hamakawa, H. Okamoto; K. Okuda, *United States Patent 4,496,788,* January 29, 1985

[5] M. Iwamoto, K. Minami, T. Yamaoki, *United States Patent 5,066,340,* November 19, 1991

[6] S. Noguchi; H. Iwata, K. Sano, *United States Patent 5,213,628,* May 25, 1993

[7] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sakata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama, and O. Oota, *Prog. Photovolt: Res. Appl*. 2000; **8**: 503-513

[8] K. Pierz, W. Fuhs and H. Mell, *J. Non-Cryst Solids*; **114 (**1989) 651

[9] T. Sawada, N. Terada, S. Tsuge, T. Baba, T. Takahama, K. Wakisaka, S. Tsuda, S. Nakano, *Proceedings of the 1st World Conf. PV Energy Conv.*, Hawaii, 1994, 1219

[10] M. Tanaka, S. Okamoto, S. Tsuge and S. Kiyama, *Proceedings CD of the 3rd World Conf. PV Energy Conv.*, Osaka, May 11-18, 2003

[11] N. Jensen, R.M. Hausner, R.B. Bergmann, J.H. Werner, and U. Rau, *Prog. Photovolt: Res. Appl.* 2002; **10**:1-13

[12] F. Roca, J. Cárabe, A. Jäger-Waldau, *19th European PV Solar Energy Conf.,* Paris, France, June 7-11, 2004

[13] M. Tucci, G. de Sasere, *J. Non-Cryst. Solids*, Vol. 338-340 (2004) 663

[14] M.L.D. Scherff, A. Froitzheim, W. R. Fahrner, *19th European PV Solar Energy Conf.,* June 7-11, 2004, Paris, France

[15] M. Sebastiani, C. RiGaspare, G. Capellini, C. Bittencourt, F. Evangelisti, *Phys. Rev. Lett.* **75** (1995) 3352

[16] M. Cuniot and N. Lequeux, *Philosophical Magazine B*, **64,** 6 (1991) 723

[17] C. Mukherjee, U. Weber, H. Seitz, B. Schroder, *Thin Solid Films,* **395 (**2001**)** 310

[18] Q. Wang, M.R. Page, Y. Xu, E. Iwaniczko, E. Williams, T.H. Wang, *Thin Solid Films*, **430** (2003) 208

[19] J. Thiesen, E. Iwaniczko, K.M. Jones, A. Mahan, R. Crandall, *Appl. Phys. Lett.,* **75** (1999) 992

[20] T.H. Wang, Q. Wang, E. Iwaniczko, M.R. Page, D.H. Levi, Y. Yan, C.W. Teplin, Y. Xu, X.Z. Wu, and H.M. Branz, *19th European PV Solar Energy Conf.,* 2CV.3.54, Paris, France, June 7-11, 2004

[21] M.R. Page, E. Iwaniczko, Q. Wang, D. Levi, Y. Yan, H.M. Branz, V. Yulundur, A. Rohatgi, and T.H. Wang, This Workshop, Winter Park, CO, August 8-11, 2004

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
August 2004	Conference Paper	

4. TITLE AND SUBTITLE
Toward Better Understanding and Improved Performance of Silicon Heterojunction Solar Cells: Preprint

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, G. Bunea, A. Terao, and Q. Wang

5d. PROJECT NUMBER
NREL/CP-520-36669

5e. TASK NUMBER
PVP4.4101

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/CP-520-36669

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words)*
The double-sided silicon heterojunction (SHJ) solar cell is more appropriate for n-type crystal silicon (c-Si) wafers than for p-type c-Si wafers because there is a larger band offset to the valence band edge of hydrogenated amorphous silicon than to the conduction band edge. Thin intrinsic and doped hydrogenated amorphous silicon (a Si:H) double layers by hot-wire chemical vapor deposition (HWCVD) are investigated as passivation layers, emitters, and back-surface-field (BSF) contacts to both p- and n-type wafers. Passivation quality is studied by characterizing the SHJ solar cells and by photoconductive decay (PCD) minority-carrier lifetime measurements. The crystal-amorphous heterointerface is studied with real-time spectroscopic ellipsometry (RTSE) and high-resolution transmission electron microscopy (HRTEM) to detect phase change and material evolution, with a focus on better understanding the factors determining passivation effectiveness. A common feature in effective passivation, emitter, and BSF layers is immediate a-Si:H deposition and an abrupt and flat interface to the c-Si substrate. In this case, good wafer passivation or an excellent heterojunction is obtained, with a low interface recombination velocity (S) or a high open-circuit voltage (Voc). Voc greater than 640 mV, S less than 15 cm/sec, and efficiency of 14.8% have been achieved on polished p type Czochralski-grown (CZ) Si wafers. Collaboration between NREL and Georgia Tech resulted in a 15.7%-efficient HWCVD-deposited SHJ cell on non-textured FZ-Si with a screen-printed Al back surface field (BSF), the highest reported HWCVD SHJ cell. Collaboration between NREL and SunPower demonstrated that HWCVD a-Si:H passivation can be better than the conventional oxides, with a low surface recombination velocity of 42 cm/sec on textured n-type FZ-Si.

15. SUBJECT TERMS
PV; photovoltaics; solar cells; crystalline silicon; materials and processes; module; impurities; device process; crystal growth; defect; passivation; microelectronics

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			19b. TELEPONE NUMBER (*Include area code)*
Unclassified	Unclassified	Unclassified	UL		