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Subcontractor Report

Large-Scale PV Module Manufacturing Using Ultra-Thin Polycrystalline Silicon Solar Cells

Annual Subcontract Report
1 April 2002–30 September 2003

J. Wohlgemuth and S.P. Shea
BP Solar
Frederick, Maryland

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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NREL Technical Monitor: R.L. Mitchell

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PREFACE

This Annual Technical Progress Report covers the work performed by BP Solar for the period April 1, 2002 to September 30, 2003 under DOE/NREL Subcontract # ZDO-2-30628-03 entitled "Large-Scale PV Module Manufacturing Using Ultra thin Silicon Solar Cells". This is the first Annual Technical Report for this subcontract. The subcontract is scheduled to run from April 1, 2002 to November 30, 2005.

The following personnel at BP Solar have contributed to the technical efforts covered in this report.

Dinesh Amin	Fiore Artigliere
James Cliber	Roger Clark
Mark Conway	Joseph Creager
Danny Cunningham	Paul Garvison
George Kelly	Shaun Kendle
Bonnie Kinsey	Timothy Koval
Mohan Narayanan	Andy Nguyen
Jean Posbic	William Poulin
Paul Schneider	Jay Shaner
Stephen Shea	George Winstead
John Wohlgemuth	Murray Bennett
Haibin Yu	Jim Newton

BP Solar has been supported by subcontracts at the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI), and the Physics Department at North Carolina State University.

ARRI staff that worked on the subcontract included:

Heather Beardsley	Raul Fernandez

NCSU worked on the subcontract was performed under the direction of Professor Gerald Lucovsky.

EXECUTIVE SUMMARY

The major objectives of this program are to continue the advancement of BP Solar polycrystalline silicon manufacturing technology. The Program includes work in the following areas.

- Efforts in the casting area to increase ingot size, improve ingot material quality, and improve handling of silicon feedstock as it is loaded into the casting stations.
- Developing wire saws to slice 100 μm thick silicon wafers on 200 μm centers.
- Developing equipment for demounting and subsequent handling of very thin silicon wafers.
- Developing cell processes using 100 μm thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%.
- Expanding existing in-line manufacturing data reporting systems to provide active process control.
- Establishing a 50 MW (annual nominal capacity) green-field Mega-plant factory model template based on this new thin polycrystalline silicon technology.
- Facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar grade silicon feedstock.

ACCOMPLISHMENTS

During the first year of the program there were significant accomplishments in each of the task areas.

As part of the feedstock task a review of materials requirements and a ranking of material types were completed. Materials were ranked for use in casting based on minority carrier lifetime, factory yield and the distribution of cell efficiencies. A factory cost module was utilized to rank the types of silicon feedstock based on their cost to produce a watt of finished solar cells. Finally, developmental relationships were established with several feedstock vendors to provide access to lower-cost experimental feedstock sources as they become available.

In the casting area the most significant accomplishment was a demonstration of increasing the ingot size from 240 kg to over 300 kg, a potential means of cost saving. Efforts in support of the process, lead to improvements in yield and reduction in casting cycle time by 14%.

Work in support of the wire saw lead to a reduction in saw room losses by 30%. Development efforts have validated the use of an alternate cutting material better suited for use on ultra-thin wafers.

In the area of wire saw demounting, ARRI reviewed a number of potential approaches to wire saw demounting and selected hot water soak with subsequent wet wafer cassetting as the best option. ARRI then built several generations of prototype wet wafer cassetting equipment. The latest version successfully destacked water rinsed and slurry coated wafers. In addition, commercial equipment has been identified that may be adaptable to PV manufacturing. Preliminary trials of that equipment using today's thicker wafers were reasonably successful.

ARRI also completed an evaluation of wafer handling techniques to improve yields in the current technology and to identify handling techniques for ultra-thin wafers and cells. ARRI selected two approaches, electrostatics and air levitation. For the electrostatic technology, they procured prototype equipment and demonstrated its ability to handle dry wafers and cells without full surface metallization. For air levitation ARRI designed and built several prototypes. These prototypes successfully handled dry and wet wafers and cells with and without metallization.

In the cell area BP Solar completed implementation of silicon nitride process in all three BP Solar screen print factories and achieved greater than 14% average cell efficiency. In addition a chemical texturing process was developed that resulted in a greater than 4% increase in module efficiency on experimental lots.

In the module assembly area BP Solar implemented a robust, cost-effective, laminated-in protective by-pass diodes for large area PV modules and developed a cost-reduced, junction box to replace two earlier models. In preparation for module assembly with ultra-thin cells, a dynamic load test has been developed that breaks cells susceptible to field failure, but does not damage normal cells.

Finally, in the area of Monitoring and Control, BP Solar completed a full-factory manufacturing data reporting system in Frederick. This system allows continuous access to real time production data.

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1.0 INTRODUCTION

The goal of BP Solar's Crystalline PVMaT program is to improve the present Polycrystalline Silicon manufacturing facility to reduce cost, improve efficiency and increase production capacity. Key components of the program are:

- Increasing ingot size;
- Improving ingot material quality;
- Improving material handling;
- Developing wire saws to slice 100 μm thick silicon wafers on 200 μm centers;
- Developing equipment for demounting and subsequent handling of very thin silicon wafers;
- Developing cell processes using 100 μm thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%;
- Expanding existing in-line manufacturing data reporting systems to provide active process control;
- Establishing a 50 MW (annual nominal capacity) green-field Mega plant factory model template based on this new thin polycrystalline silicon technology; and
- Facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar grade silicon feedstock

These goals are to be achieved while improving the already high reliability of today's crystalline silicon modules.

Two subcontractors are supporting BP Solar in this effort:

1. Automation and Robotics Research Institute of the University of Texas at Arlington to assist BP Solar in developing equipment for automated handling and demounting of ultra-thin wire saw wafers.
2. North Carolina State University to support BP Solar in characterizing the effect of trapped charge at the silicon/AR coating interface and in determining how to improve the passivation of BP Solar cast polycrystalline silicon solar cells.

The baseline for this PVMaT program is the polycrystalline process and production line as it existed at the conclusion of BP Solar's previous PVMaT Contract NREL # ZAX-8-17647-05 entitled "PVMAT Improvements in the BP Solar PV Module Manufacturing Technology". [1, 2] This baseline is described in more detail in Section 2.0.

The rationale behind this program was to identify specific areas in the baseline process where improvements in handling, process control or the process itself could significantly reduce cost, increase efficiency and/or improve capacity. The realization that feedstock silicon is becoming an increasing larger percentage of the overall cost lead to the incorporation of efforts to significantly reduce wafer thickness and to work with selected silicon feedstock manufacturers to secure a source of solar specific lower-cost solar-grade silicon feedstock.

BP Solar has identified two external vendors, who have provided large capacity casting stations for the expansion of the BP Solar Frederick casting facility. Material quality from these stations was shown to be equivalent to that made in the BP Solar baseline stations. Efforts during this program include increasing the ingot size and improving the material quality.

The development in the wire saw technology is to reduce wafer thickness in order to reduce cost and increase even further the number of wafers/cm of brick that can be cut, thereby reducing the amount of silicon necessary per watt of modules produced.

Work on cell processing is designed to increase the average cell efficiency to 15.4% (at Standard Test Conditions) for ultra-thin wafers while improving process control and reducing the overall module manufacturing cost. Areas of investigation include passivated AR coating, edge isolation, surface texturing, and selective emitter diffusion. In addition, those processes that are not compatible with processing of ultra-thin cells will be identified and modified.

Wafer and cell handling will become more critical as the thickness decreasing. ARRI is assisting BP Solar in identifying approaches to handling of ultra-thin wafers throughout the production line. During the first year particular emphasis will paid to developing approaches to demounting ultra-thin wafers from the wire saw.

Improved measurement and control during processing should lead to improved yields and higher average cell efficiency. Three specific areas in the plant have been identified, where additional inline measurements are expected to significantly improve control of the process.

The first year's efforts will be discussed in detail in Section 3.0.

2.0 BASELINE PROCESS

BP Solar's Crystalline Silicon Technology is based on use of cast polycrystalline silicon wafers. The process flow at the end of NREL Contract # ZAX-8-17647-05 is shown in Table 1.

Table 1
Cast Polycrystalline Silicon Process Sequence

Casting
Of
240 Kg Brick Ingots

Wire Saw Wafering

Cell Process
(All Print with Al BSF & PECVD SiN AR)

Module Assembly
(XY Positioning)

Lamination
(Fast Cure EVA)

Finishing

The various segments of BP Solar's module manufacturing process as practiced at the beginning of this PVMaT program are described below.

Casting
BP Solar has purchased directional solidification equipment specifically designed for photovoltaics. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semi-crystalline silicon ingot. The size of the cast ingot yields 25 – 12.5 cm by 12.5 cm bricks.

Wafering
During the previous PVMaT Programs BP Solar developed wire saw technology for cutting large area polycrystalline wafers and improved the performance by reducing the wire saw pitch to 450 microns with no loss in downstream yield, by separating and recycling the components of the wire saw cutting slurry, and by re-tooling older saws to increase their capacity by 40%.

Cell Process
The cell process sequence is based on the use of Thick Film Paste (TFP) metallization, where a commercially available screen-printed silver paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps include: diffusion, firing of the front and back print pastes and PECVD deposition of a SiN antireflective (AR) coating.

During the previous PVMaT Program, BP Solar developed the cost effective PECVD Silicon nitride process. This process has now been implemented on all BP Solar screen print production lines.

Module Assembly
The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. BP Solar uses automated machines to perform the tabbing operation. Tabbed cells are then soldered into strings using equipment developed in the previous PVMaT program.

Module Lamination
The module construction consists of a low iron, tempered glass superstrate, EVA encapsulant and a Tedlar back sheet. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

3.0 PVMAT PROGRAM EFFORTS

The following sections detail the progress made during this year.

3.1 Silicon Feedstock Development

In this task, BP Solar is investigating the use of a wider variety of off-grade silicon feedstock and identifying strategic sources of solar-specific lower-cost solar-grade silicon feedstock. BP Solar completed a survey of the available lower-cost solar grade silicon feedstock material.

This effort included evaluation of all commercial participants in the feedstock industry in terms of:

- Commercial capacity
- Technologies
- Intellectual property
- Personnel
- Interest in participating in PV feedstock development

Some of the results of that study are detailed below:

A variety of silicon feedstock sources is used in the production of wafers for photovoltaic (PV) applications. "The selection and processing of silicon for crystal growth represents the first and most important step in obtaining the highest possible device efficiencies. The quality of the selection and processing sets an upper limit on the performance of the final device. Very few, if any, options exist to convert poor quality base material into material worthy of cell processing."[3]
The technical performance of feedstock depends on three characteristics:

1. The types of impurities and their overall level in the silicon:
   - Higher levels of impurities lead to lower solar cell conversion efficiency for both mono and multi-crystalline processes.
   - All silicon growth processes tend to remove impurities from the source silicon by a process of impurity segregation, which concentrates impurities in the remaining molten silicon as the crystal solidifies.
   - This segregation process concentrates impurities in the "top cuts" from cast multicrystalline ingots, in the "tails" of monocrystalline Czochralski (CZ) boules, and in the "pot scrap" left in the ceramic crucible at the end of a CZ growth run. These sources of silicon are therefore fundamentally inferior to "intrinsic" silicon, the very high purity product used as feedstock in the semiconductor industry.

2. The surface morphology and the size distribution of the silicon feedstock pieces:
   - Feedstock with very rough surfaces or with closed pores is hard to keep clean.
   - Feedstock with pieces less than about 2 cm is difficult to melt in the heritage Solarex casting process, but is acceptable in mono crystal pulling and in the current generation of BPSolar casting furnaces.
   - In the heritage Solarex casting process, smaller piece sizes produce ingots that are more difficult to cut.
   - Powder silicon is difficult to handle and easily contaminated.

3. Whether or not the material requires further cleaning or other processing before going into the PV process line:
    - Pot scrap silicon, for example, frequently comes with adhered pieces of ceramic, which must be removed, and the pieces re-cleaned, before further processing.
    - Brokered silicon generally must be re-cleaned before use because of its variable and generally unknown provenance.
    - Powder silicon cannot be used directly in the crystal growth processes, but must first be agglomerated so that it stays in place and melts effectively, as well as to segregate impurities.

The PV industry has traditionally depended on "off-grade" feedstock that did not meet the needs of the semiconductor industry. Much of this feedstock consisted of high purity, "intrinsic" silicon that did not meet the surface finish requirements of the semiconductor industry. Another important source of silicon was the "Tops and Tails" of single crystal, CZ ingots that did not meet the semiconductor industry's requirements for wafers. Some of this material has always come directly from the vendors to the semiconductor industry. Some is sold to brokers for resale to the PV industry.

The DynCorp study points out that, "since all silicon residues represent some form of waste material from the semiconductor industry, generalizations regarding usability are difficult to make and entail significant risk. For example, although the PV industry generally considers tops/tails silicon as a class of usable residue, usability in practice depends solely on the composition of a particular shipment of material."[4]

In addition, because the PV industry to-date has been based on semiconductor industry byproducts, the availability of feedstock has fluctuated with cycles in that industry. Through the mid-1990's, the cost of off-grade intrinsic silicon and of single crystal tops and tails was between $15/kg and $20/kg. Changes in the semiconductor industry then led to their using some of the tops and tails and some wafers that were formerly scrapped. This phenomenon, combined with the growth of the PV industry, led to a reduction in the availability of PV feedstock. PV manufacturers, out of necessity, continued to run by learning to use pot scrap silicon, which was initially available at very low prices.

The transition to pot scrap feedstock led to a dramatic, short-term decrease cost for silicon feedstock. However, pot scrap silicon has poorer yields, and produces less efficient solar cells than can be made from intrinsic or tops and tails feedstock. As more manufacturers began to use pot scrap, the price rose. At the same time, the poor yields from pot scrap meant that other sources of good feedstock were competitive with pot scrap even at prices above $20/kg. During the late 1990's, this led PV manufacturers back to a mix of feedstock dominated again by off-grade semiconductor intrinsic and tops and tails. This transition was facilitated by a downturn in the semiconductor industry, which lead to significant over capacity in polysilicon feedstock.

Silicon Performance

A fundamental measure of quality for cast multicrystalline or for CZ silicon is minority carrier lifetime. Carrier lifetime is directly related to solar cell short circuit current. Material types can be ranked in order of their lifetimes.

Intrinsic Silicon is clearly the best material in terms of brick lifetime. "Small Piece", which is also an intrinsic material is next. Material that needs to be cleaned before further processing falls in the middle of the group, and material that is expected to have high impurity content falls toward the bottom.

"Recycle" is slab material that has been cut from the sides and bottoms of cast ingots as the ingots are cut down into bricks prior to wafering. The quality of recycle tends to reflect the quality of the original starting material. That is, recycled material from ingots cast using intrinsic silicon will be nearly as good

as the original intrinsic, while recycled material from pot scrap will be roughly the same quality or a little better than the original pot scrap.

Final solar cell performance has been shown previously to correlate well with lifetime measurements taken at the brick level.

Another measure of Silicon quality is the overall factory yield. Factory yield is defined as the number of good tested Watts at module test per kilogram of raw silicon into the process, (W/kg). This definition includes both mechanical losses and losses due to cells or modules that fail minimum efficiency criteria at final test. Materials such as pot scrap and Tops and Tails must be sorted and resistivity typed before being used, reducing the overall yield. In addition, the process yields are lower through the casting, wafering and cell lines for pot scrap because of both higher mechanical and electrical losses. Remarkably, overall factory yields can differ by more than a factor of two between low-quality feedstock, like pot scrap, and prime intrinsic polysilicon.

Another way to look at performance is to look at the distributions of efficiencies for finished cells. Again, there is a large difference in the higher efficiency populations for high quality material versus pot scrap. In addition, the distributions obtained from low quality material are more variable than those from high quality material are.

The overall impact of silicon quality on cost can be calculated using factory standard cost models. As one example, the cost per Watt at the cell level is dramatically higher for pot scrap than it is for Intrinsic Silicon, even when the raw material cost for pot scrap is half that of Intrinsic.

In addition, because of the lower average efficiency and the lower yield of off-grade silicon, fewer Watts can be produced from the same number of solar cells. Lower efficiency product is also often sold at a discount with respect to higher efficiency product. Combining the cost and revenue numbers gives the average variable margin, which again is substantially higher for Intrinsic Silicon compared to pot scrap.

The finished model may be used to make quantitative decisions on the cost effectiveness of various silicon feedstocks.

The cost model discussed above has been used to evaluate a number of different feedstock sources. Details of specific source types from specific manufacturers are proprietary.

In general, the model demonstrates that reduction of feedstock purity is virtually never cost effective, nor is purchase of feedstock lots through brokers. The former suffers yield losses that more than offset any cost advantage, while the latter requires substantial engineering effort for small lot qualification and even then suffers from significant process variability.

In contrast, for the new-generation casting stations, process yields for high-purity silicon are essentially independent of piece size or morphology. This flexibility allows marginal cost reductions to be achieved by several vendors in ways that are specific to their particular processes. Adequate supplies of cost-effective feedstock are available for at least the next several years. During that time, it is expected that new sources of lower-cost feedstock will become available because of development efforts now underway by a number of existing and potential new suppliers.

We have established development relationships with several potential vendors for advanced, low-cost feedstock. Near the end of the first contract year, we had received sample material from two of these vendors, with larger quantities to be available in the second year after completion of the first set of tests.

3.2 Casting Development

In this task, BP Solar is investigating improvements in the casting process in order to increase ingot size, improve material quality and improve material handling. BP Solar has designed and demonstrated a prototype casting station that can increase the cast ingot weight to 300 kg. Additionally BP Solar was working to optimize the casting process through modifications to the release coating and the dopant species.

BPSolar, working with different manufacturers of polysilicon feedstock, has identified several forms that result in lower cost material into the casting process, as described above. A cost model was developed and used to evaluate these different feedstock sources. Details of specific source types from specific manufacturers are proprietary.

Piece size and surface morphology vary widely for feedstocks both across vendors and within the offerings of a single vendor. Casting and downstream process yields depend essentially only on material purity, and not on piece size or surface morphology. We have found material purity to be sufficient for each of the vendors now supplying feedstock to BPSolar.

The standard charge size for the latest BPSolar casting stations is 240 kg. We have made charges from silicon feedstock as small as 2 mm in diameter up to pieces of variable shape up to 10 kg or more. The only issue that has arisen has been difficulty in packing a full charge of the larger pieces into the crucible. In all cases, the full charge can be obtained by intermixing larger and smaller piece size material.

We plan to increase charge size to 300 kg. Constraints on this increase are:

- Packing of silicon pieces – We have demonstrated that the present crucibles will hold up to 350 kg of very small, uniform beads. We do not see a problem with achieving 300 kg charge sizes with an appropriately chosen mix of larger and smaller pieces.
- Crucible strength – The larger charge size will exert significantly higher pressure on the crucible when the charge is molten. However, both of the large station designs include external support for the crucible. They are expected to be sufficiently robust to handle the higher pressure.
- Crucible size – Cannot be changed without substantial reengineering of both the stations and the crucible, but not necessary for 300 kg charge.
- Crucible recharge after melt – Can be done with some reengineering of the existing stations, but not necessary to achieve 300 kg charge.
- Hot Zone – BPSolar presently has two different types of large casting station. In both types, the hot zone may be too short to allow good control of ingot freeze-out as the charge size increases and the ingot becomes taller.
- Sizing – This constraint has been removed by the recent purchase of band saws, capable of cutting the taller ingots.

Because of these considerations, no station redesign was necessary to begin work on casting 300 kg charges in the existing large-format casting stations at BPSolar. There is some risk that the present design will not allow sufficient control of the freeze-out process to ensure uniform material quality throughout the ingot. This risk will be evaluated by thermal modeling coupled with conservative experimental approaches to the larger ingot size.

We have purchased a thermal modeling package with a dedicated high-speed computer system for this work.

Yield Improvement and Cycle Time Reduction

Casting yield in the new casting facility has been quite high, but there was initially a high incidence of cracks after sizing the large ingots into bricks. There are presently two different casting station models running in the new building, from two different manufacturers. We will refer to these as Type A and Type B stations. The incidence of cracks from the Type A stations was higher than that from the Type B stations in general. In addition, the degree of cracking in the Type A station material depended on the way in which the ingots were cut into bricks, while this was not the case for the Type B station material.

A crack reduction program was been initiated on the Type A stations incorporating suggestions from the manufacturer. Several different variations on the casting program were tried on one station, one of which successfully reduced the incidence of cracking by as much as half, but with some increase in the overall cycle time.

A separate program was then undertaken to reduce the cycle time. This work was driven by thermal modeling followed by experiments designed using the model results. The most robust version of the program was implemented in production, reducing the overall casting cycle time by 14%.

The original ceramic release coating recipes were supplied by the two casting station manufacturers. A program was undertaken to establish as single coating method that was appropriate for both station types. This was successfully implemented in production as well.

Reduced Oxygen/Carbon Trial

A program has recently begun to better understand the role of oxygen and carbon in material performance.

A 70 kg ingot was purchased from another manufacturer. Four 125mm x 125mm bricks were cut from the ingot. The brick length was approx. 190mm. Average minority carrier lifetime of the brick was 5.0 microseconds using the microwave photoconductive decay method. Samples will be prepared in according to an ASTM procedure defining sample preparation, (2 mm thick with polished surfaces to ensure measurement accuracy). The samples will be measured using an FTIR spectrometer calibrated with a float zone standard.

One of the bricks will be notched for wafer trace ability and processed in the cell line. The performance will be compared against a control brick.

3.3 Thin Slicing of Silicon Wafers

In this task, BP Solar is developing a process to slice silicon wafers of 100 μm thickness on 200 μm centers.

Modeling Work

BP Solar proposes to use thinner wafers in order to reduce silicon consumption and cost. In order to estimate the impact of doing this, we modeled the effect of cell thickness on performance using PC1D software. For most of the material parameters, (for instance band gap) we simply used the values supplied with the model. We also used the incident light spectrum supplied with the program. For a small number of parameters, such as bulk lifetime and surface recombination velocities, we used parameters appropriate to our material or device. Specifically, we used the model to make estimates of the effects of varying wafer thickness, bulk silicon lifetime and front surface texturing and their interactions

We currently make our cells on wafers that are 230 microns thick. As shown in Figure 1 below, efficiency increases as wafer thickness decreases. Peak short circuit current occurs at a thickness of about 70

microns. Open circuit voltage and, to a much smaller extent, fill factor, increase monotonically as thickness decreases. At our target thickness of 100 microns, there is an efficiency improvement of 3.8%, of which 2.7% comes from I_{sc} gains, and most of the rest from V_{oc} improvements.

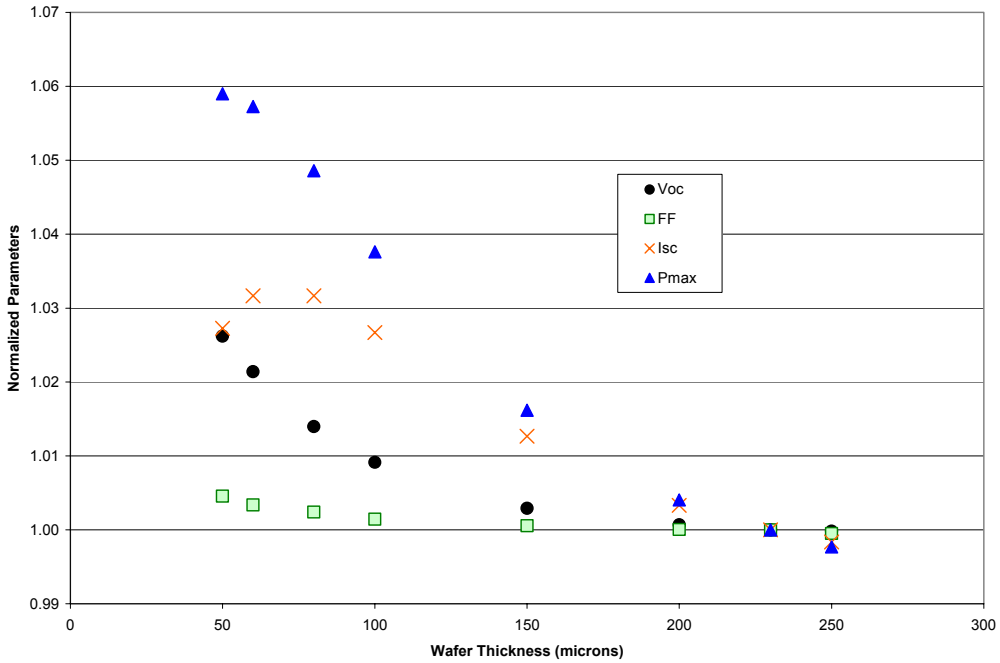

Figure 1: Normalized cell parameters (V_{oc}, FF, I_{sc} and P_{max}) as a function of wafer thickness

Improving bulk silicon lifetime, by impurity reduction, improvements in crystal structure, or by other means has a slightly greater impact (about 3%) on 100-micron wafers than on our current wafers. This is shown in Figure 2.

We propose to increase current by texturing the front surface of the cell. The PC1D program allows one to model the texture in terms of two parameters, facet angle and height, as shown in Figure 3.

The facet height has almost no effect on current, only about 0.1% over the range of .05 – 5 microns. However, facet angle has a significant effect, as shown in Figure 4.

If facet angles of greater than or equal to 50 degrees can be accomplished, then currents gains of 2% or greater are predicted.

A cell made on a 100-micron wafer with appropriate front surface texturing could be 5% more efficient than our current cells made on 230-micron wafers. Most of the gain comes from higher short circuit currents. A smaller gain in Voc occurs because of using thinner cells.

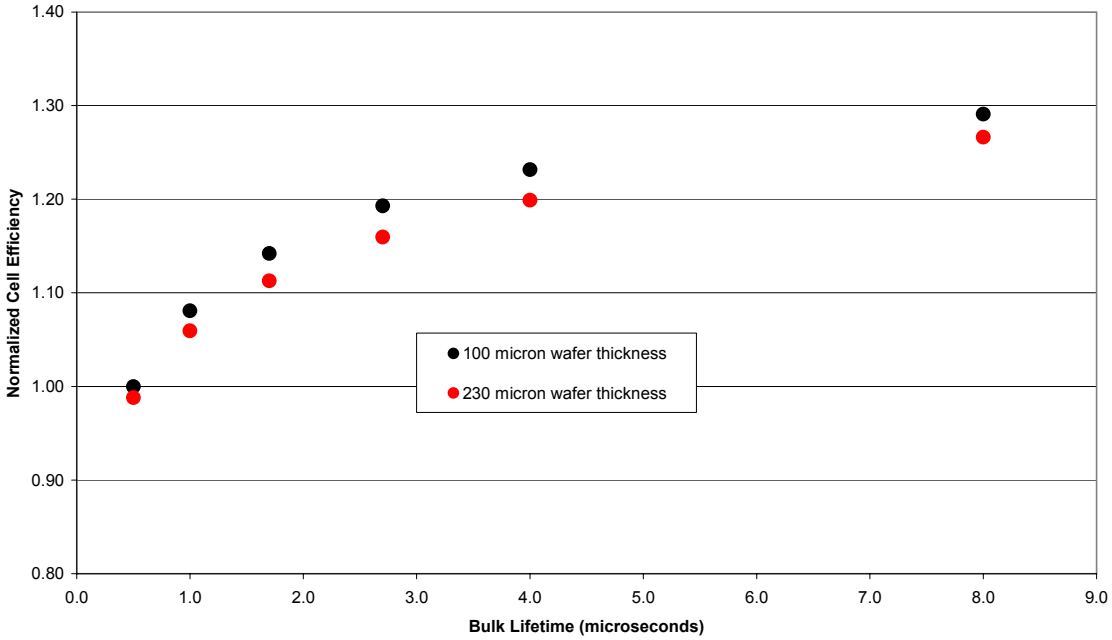

Figure 2: Effect of bulk lifetime on efficiency: for 100 micron and 230 micron thick cells

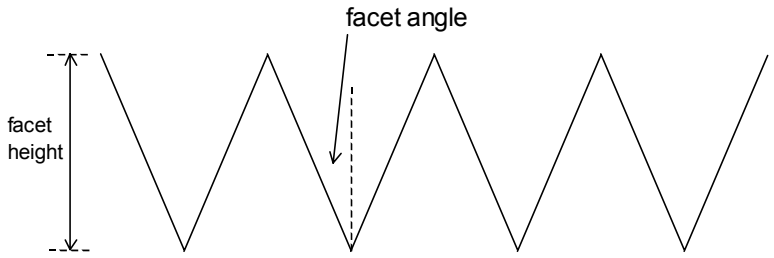

Figure 3: Parameters used in PC1D to characterize surface texture.

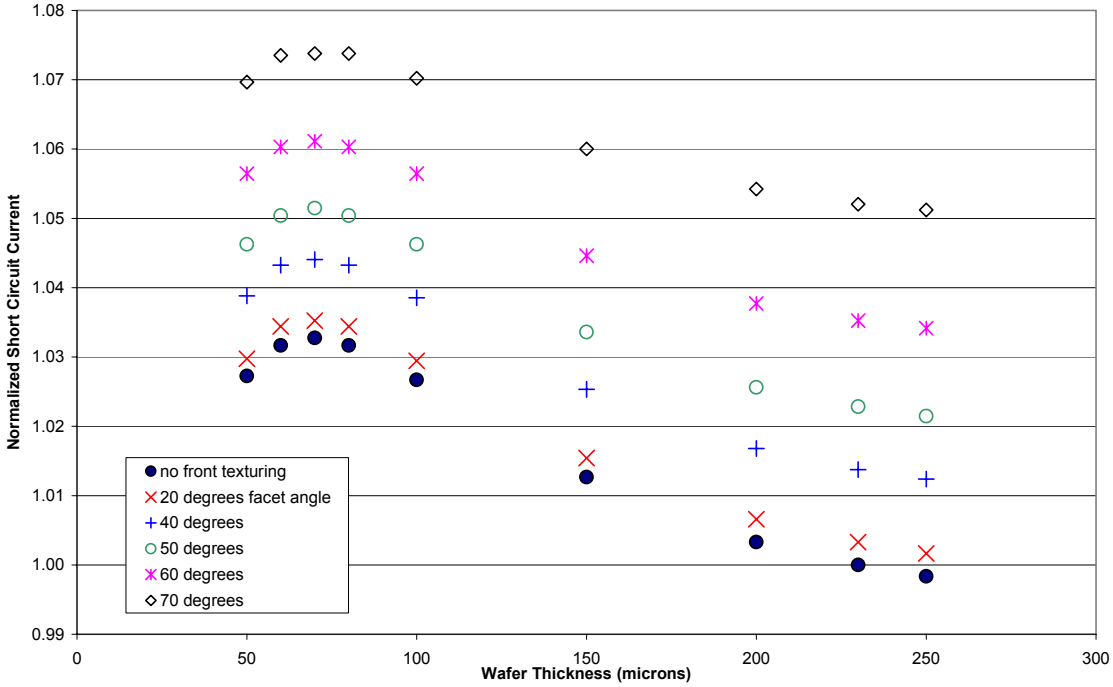

Figure 4: Short circuit current as a function of wafer thickness for a series of facet angles

Cutting Media

To cut thin wafers and save kerf material we need to modify the cutting media to reduce the surface damage while maintaining a reasonable cutting speed. We have begun an evaluation of the science and technology of cutting (particularly silicon). The three materials most often utilized for silicon cutting and polishing are silicon carbide, alumina and polycrystalline diamond. BP Solar wire sawing has always used only silicon carbide as a cutting material.

In the media-texturing business, the technology has transformed from use of alumina and silicon carbide to mixtures of those, to diamond to mixtures of diamond and alumina. The corresponding change in defect size has been from 5 microns to 0.2 microns, while concurrent changes to the other process parameters have maintained similar material removal rates. With 0.2 micron surface damage, the present defect etch could most likely be eliminated. This would save material (at least 25 microns of silicon from every wafer) and eliminate one of the major yield loss steps for ultra-thin wafers.

While polycrystalline diamond is more expensive than silicon carbide, it is also more readily recycled/reused in the process. We have identified a partner to work with in the development of this cutting material.

Initial trials at BP Solar were not successful, as the trial slurry did not cut as effectively as anticipated. Following these tests, the vendor performed a number of bench-top laboratory trials to investigate the impact of slurry variations on cutting efficiency.

Based on the results of the bench-top tests, further full-scale trials were carried out on a large saw. While the results were significantly better, and several full-size runs were cut to completion, the surface finish of

the resulting wafers was not acceptable. The vendor is presently conducting additional bench-top tests prior to another round of full-size tests later this year.

Another potential vendor of conventional slurry has proposed a joint development effort in 2004 specifically designed to achieve the goal of cutting thinner wafers (down to as thin as 100 microns), while facilitating separation of the finished wafers during the demounting process (discussed further below).

Yield and Cost Improvements

BP Solar has worked with an outside vendor to implement wire saw slurry recycling. This system is now operational. In addition to providing a more consistent slurry quality, the system will result in substantial cost savings in 2003 and beyond.

A major initiative was undertaken to improve yields in the saw area. This work will be discussed below in the section on process control. The initiative resulted in a reduction of loss in the wire saw area by over 30%.

3.4 Wafer Demounting and Handling

In this task, BP Solar is developing processes and equipment for demounting and subsequent handling of very thin silicon wafers.

3.4.1 Commercial Systems

BP Solar is developing a method to automate wafer handling after wire sawing. The objective is to develop a process and equipment able to:

1) Accept wafers directly from the wire saw,
2) Clean the residual oil-based slurry in a timely fashion,
3) Detach the wafers automatically from the wire sawn wafer comb and
4) Cassette the detached wafers automatically into cassettes for the next stage of manufacturing.

The method being developed includes two separate, consecutive systems: Post wire saw Clean and Detach system (PCD system) and wafer Singulation, Inspection & Cassetting (WSIC) system.

Two sawn wafer combs were tested. The experimental PCD system accepted sawn wafers directly from the wire saw while still attached to the mounting beam and with slurry still in between the wafers. This test used solvent cleaner to remove slurry from deep inside the wire saw grooves. The cleaner is different from the solvent currently used. The current solvent needs hours to clean a wafer comb. The new solvent cleaner was poured over the comb of wafers. Fresh cleaner penetrated deeply into the wire saw grooves, loosening and removing the residual slurry. At room temperature, the process of removing slurry was very rapid (<15 minutes), consuming less than one gallon of cleaner.

Immediately following the application of the cleaner, the wafer comb was rinsed with clean tap water. The rinse process successfully removed residual cleaner. To detach wafers from the beam, the cleaned wafer comb was soaked in hot tap water. In a short period, the epoxy bond softened, and wafers were released from the beam.

The detached wafers were processed with a WSIC system designed for semiconductor applications. This system has less than desired hourly output capacity for solar applications. However, this system was able

to process solar wafers. No visual damage occurred to the wafers during the cleaning and detachment processes.

A single chamber PCD system design was proposed. The chamber is sealed and vented and houses the entire PCD process of cleaning, rinsing and detaching. We are still experimenting with the possibility of using aqueous cleaner for PCD. A new WSIC system is being designed to meet solar production hourly output requirements. Preliminary cost-benefit analysis was conducted. It shows the method being developed could minimize manual handling, improve productivity, lower labor cost, and consequently reduce wafer cost.

3.4.2 ARRI Development

3.4.2.1 Wire Saw Comb Wafer Demount

Introduction & Scope
This activity focuses on the study of automation techniques for separating wafers from the wire saw comb, plus potential integration with automated cassetting. It addresses current thickness wafers, for which there is immediate applicability, and it considers its eventual use with ultra-thin technology.

Three main factors motivate this study:

- Increase throughput; current (2002) water soak method is lengthy
- Reduce yield losses due to fractures with manual handling
- Potential integration as one-step wire saw to cassetting (no soaks); this would have a significant impact on front-end wafer processing cycle time

Solution Approaches
Wire saw comb demounting entails the release of wafers after the sawing process from the glass or epoxy bar substrate, to which they remain held by a thin strip of epoxy.

Two types of approaches arise in this context – one based on simultaneous detachment of wafer clusters from the substrate, which are then fed into singulation equipment in coin stacks, and one where entire mounting bars are loaded into a machine and wafers are individually detached prior to cassette placement.

Potential techniques have been identified and are listed below for each category in increasing order of ease /feasibility.

(a) Simultaneous detachment

- *Epoxy-less clamping on wire saw machine carrier*: Eliminate epoxy and clamp a single brick onto the metal carrier through the sidewalls. Halfway through the cutting process, clamp the cut side of the brick by the side and finish cut. There is a potential issue with vibration-induced breakage at the brick-carrier interface.
- *Horizontal cutting motion integrated within wire saw machine*: Immediately after wire saw has cut through the brick, move brick carrier forward or backward by 1 mm to use the wires to "cut" the wafers from the root. This motion would have to be retrofitted into the machine. A basket to catch the wafers as they are separated from the carrier is also required.
- *Ultrasonic epoxy bond weakening*: use ultrasonic energy to dislodge wafers from the comb.
- *Hot wire / wire saw cutting of entire brick after removed from wire saw machine*: Use a wire saw or hot wire method to slice through the carrier-brick interface after the wire saw process.
- *Use of existing wires to assist with singulation*: leave the wires on the brick prior to unloading them from the machine (the wires are one-time use only). This entails bonding the wires on

each side of each brick to a metal or plastic strip, then cutting them. This feature may be used both to detach wafers from the carrier as well as help singulate them into cassettes.

- *Formulated polar solvent soak to accelerate epoxy bond weakening*: Introduce a polar solvent bath after the cleaner soak to weaken epoxy bond.
- *Higher temperature water soak to accelerate epoxy bond weakening*: place comb in high temperature (60-70 C) water bath, which would neutralize the epoxy bond to the point where wafers can fall on their own weight. Water could be specially formulated with solvent such that both processes can be merged into a single one.

(b) Individual detachment

- *Water jet cutting*: direct a stream of small-diameter, high-pressure water jet at the wafer-substrate interface to break the epoxy bond and allow wafer to be singulated from the stack (by an applicable pick-and-place method).
- *Laser cutting*: direct a high-intensity laser beam at the wafer-substrate interface to break the epoxy bond and allow wafer to be singulated from the stack (by an applicable pick-and-place method).
- *Mechanical detachment*: detach wafers from comb by direct application of traction or lifting forces on the wafer surface using an appropriate pick-and-place, with or without epoxy weakening pre-soak.

Current Technique

Currently the following steps are followed:

- Entire sawn brick (complete with full carrier) is submerged in a static tank with cleaner solvent for 1.5 to 3 hours (depending on solvent freshness) to remove slurry.
- Sawn comb is transported to demounting area where it is submerged in a warm water bath (40 – 50 ºC) for an additional 15 minutes.
- Clumps of wafers roughly 1" thick are manually dislodged from the comb and singulated into cassettes.

Preliminary Analysis

The epoxy supplier reported that the current formulation is designed to release fully when soaked in water at 90 ºC within minutes; the supplier also confirms that gravity detachment (with submerged wafers, zero impact over a short distance) is a viable simultaneous removal method, performed by other customers.

The initial BP Solar water soak process (in place at the beginning of this study, 2002) was using low average soak temperatures because immersion of wafers took place in static steel tanks without insulation or hot-water recirculation capability; this led to relatively long soaks and incomplete epoxy release.

The new BP Solar-implemented enhanced water soak process (Spring 03) is using tanks with a hot water supply; water is kept at 40-50 ºC for operator comfort, which is well below the recommended 90 ºC, but this has proven adequate for epoxy release. The soak is performed relatively fast (10-15 minutes).

Conclusion: epoxy release can take place with a fast and very inexpensive water soak process. Given that the complication and expense of every single alternative method for wire saw comb demount exceeds the water soak process by orders of magnitude, ARRI recommended the use of said conventional release method, and has concentrated automating the still necessary wet wafer demounting process.

Automated Wet Wafer Demounting

It is appealing to feed a sawn comb directly from the wire saw station into a cassetting machine, particularly if the warm water soak and possibly even the solvent soak can be eliminated. It can be assumed that removal of the slurry is unimportant at this step since it can be easily incorporated into the post-cassetting cleaning process. It can also be assumed, from the information in the previous section, that a ready means to weaken the epoxy bond exists; this reduces this problem entirely to one of "wet wafer handling" or, more specifically, "wet wafer coin stack singulation."

An approach investigated and partially tested by ARRI is to use the vacuum/shearing coin stack demount method on wafers still on the saw comb. In this configuration, the carrier would be placed horizontally; a warm water bath, covering only the bottom half of the wafers would still be used to weaken the epoxy bond. To keep wafers from listing as they become detached from the comb prior to mechanical removal, soft-walled side clamps would be necessary.

This method would rely on the ability of vacuum to hold on to the wafer against a film of wire saw slurry, and on the availability of a suitable vacuum pump resistant to slurry ingestion; preliminary testing of the latest ARRI demounting prototype at the BP Solar facilities shows promise with this approach. Further detail on the ARRI automation prototypes is found in the following section.

It is possible, but has not yet been tested, that a method such as electrostatic chucking would be preferable to vacuum for wafer acquisition. Further information on electrostatic means of wafer holding is found in section 3.4.2.

Prototyping Work at ARRI

ARRI has investigated multiple methods for automated wet wafer demounting. The combination of vacuum / shearing has been consistently identified as the most promising for this particular scenario. Throughout phase I, ARRI has built no fewer than five generations of prototypes to achieve wet wafer coin stack demounting. The following items have been identified as most relevant to the success of the process:

- A special vacuum pump design is necessary to cope with minor fluid ingestion. Certain makes of venturi pumps can be easily modified for operation in this environment by removal of a cleaning filter.
- The vacuum cup material found to be optimal in terms of friction (soft silicone) is also compromised by presence of solvent; contact with a solvent must be avoided or minimized by thorough rinsing with water to prevent warping and loss of sealing. However, contact with the wire saw slurry has no deleterious effect on this vacuum cup material.
- The maximum shearing speed between wafers is limited by the high interfacial traction forces present, to a point where a single manipulator will not be able to perform both the singulation and cassette placement functions fast enough. However, with a "hand-over" operation after peeling the wafer from the stack, it is possible to achieve cycle times comparable to human handling (between 2 and 3 seconds per wafer).
- It has been found necessary to have a counter-rotating brush for most effective separation of the wafer.

The Generation 1 prototype is shown in Figures 5 and 6. Figure 5 shows that standard vacuum cups (without drawing vacuum) are used to impart friction upon the face of the wafer. Rotary actuator provides gripping action once the wafer has been pulled up and the surface has been exposed. Figure 6 shows a close-up of the material bins. One bin contains the wet wafer stack and the other an old-style BP Solar cassette. Each bin can be filled with fluid to simulate wet processing conditions. The presence of standing fluid has not proven critical in the operation of the various singulation prototypes.

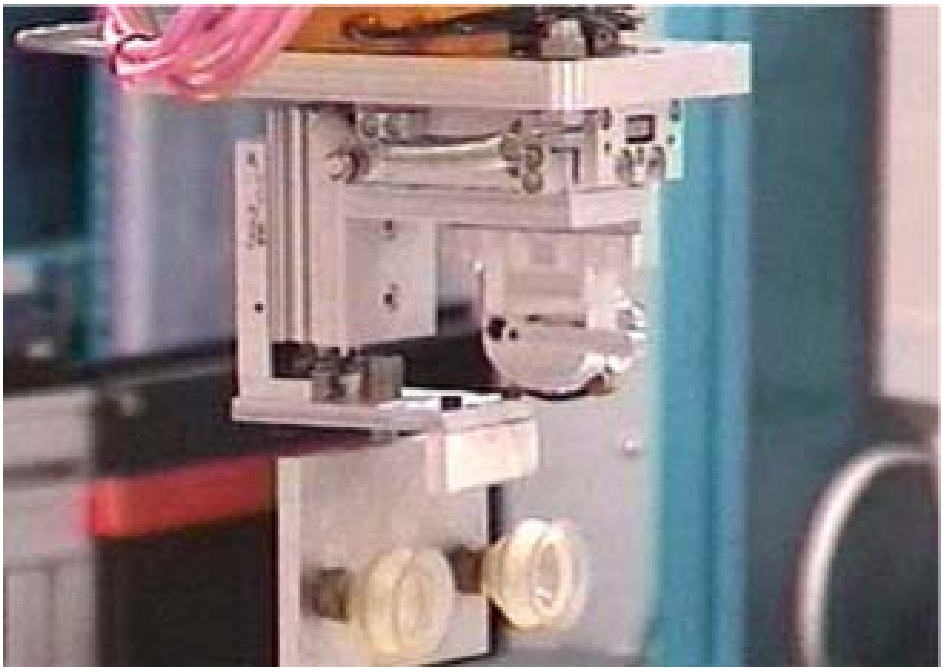

Figure 5: Generation 1 wet wafer demounting prototype

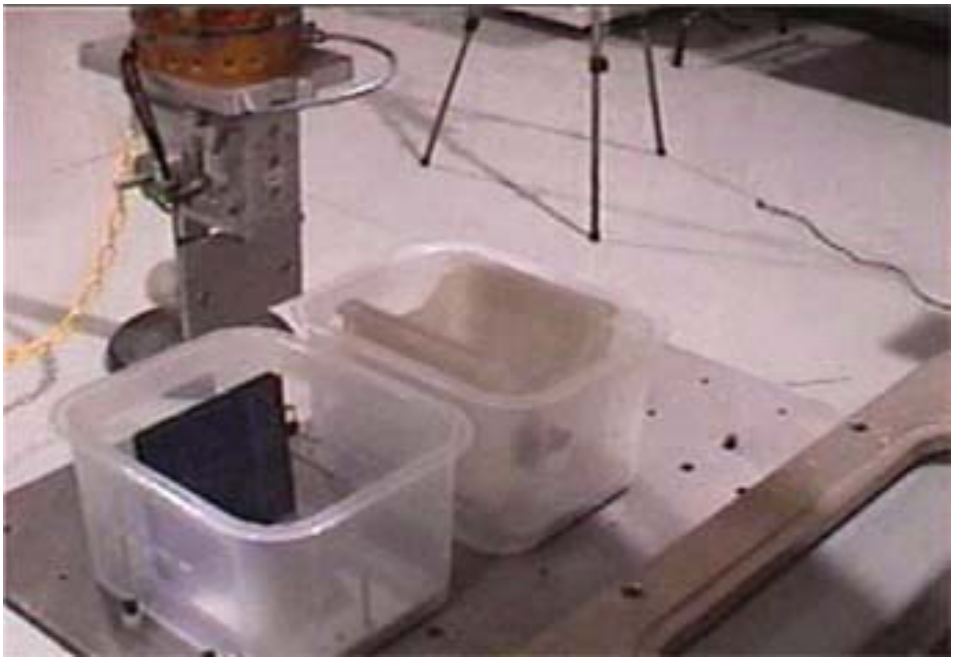

Figure 6: Material bins of the Generation 1 wet wafer-demounting prototype

In Generation 2 a counter rotating roller and an end-effector with active vacuum were added as shown in Figures 7 and 8.

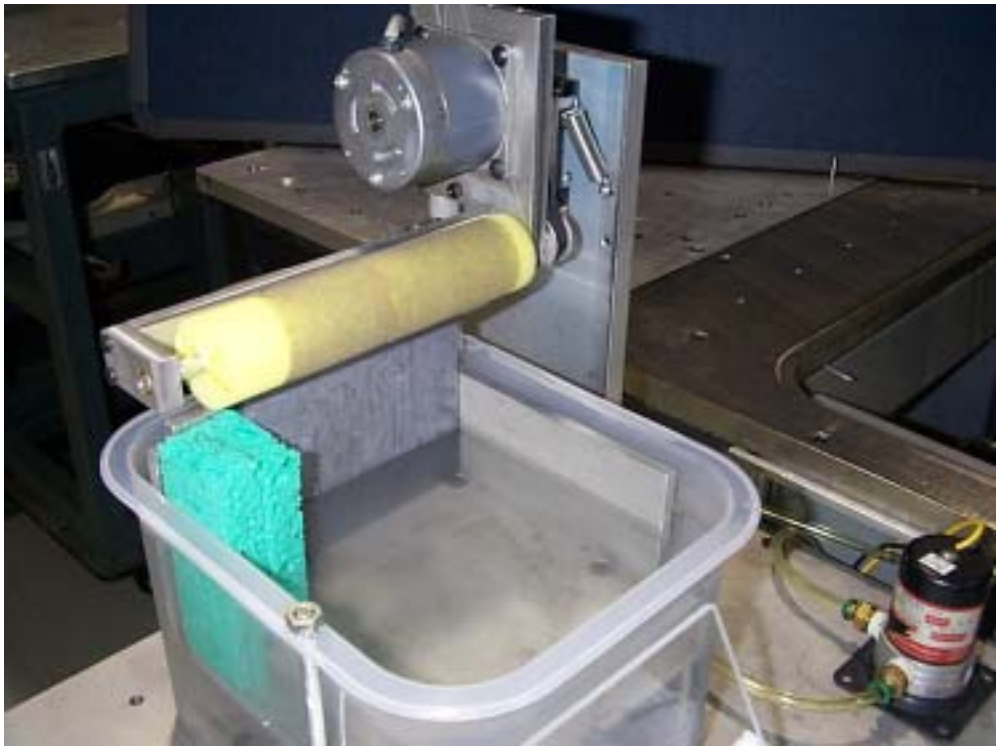

Figure 7: Generation 3 prototype with counter-rotating roller introduced to help wafer singulation

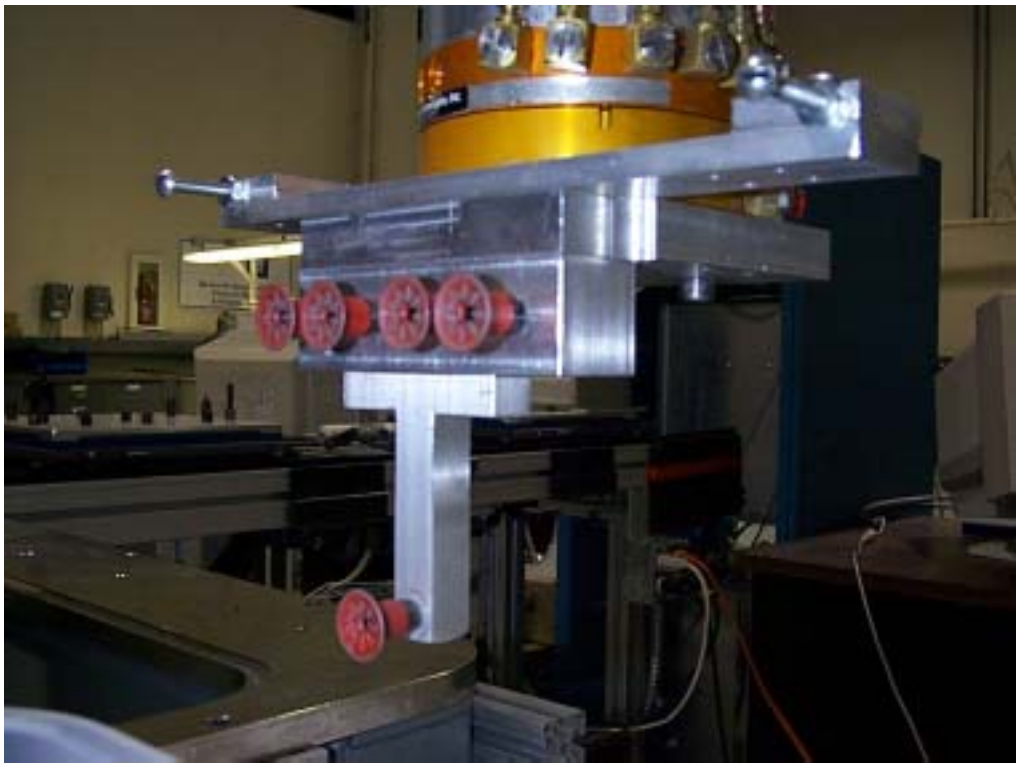

Figure 8: Generation 3 prototype with end-effector with active vacuum cups

Generation 4 used a horizontal coin stack arrangement. It incorporated a pneumatic slide, which did not provide the necessary speed control for wafer separation. This prototype also included a stepping motor for raising the coin stack against the horizontal actuator. These features are shown in Figures 9 and 10.

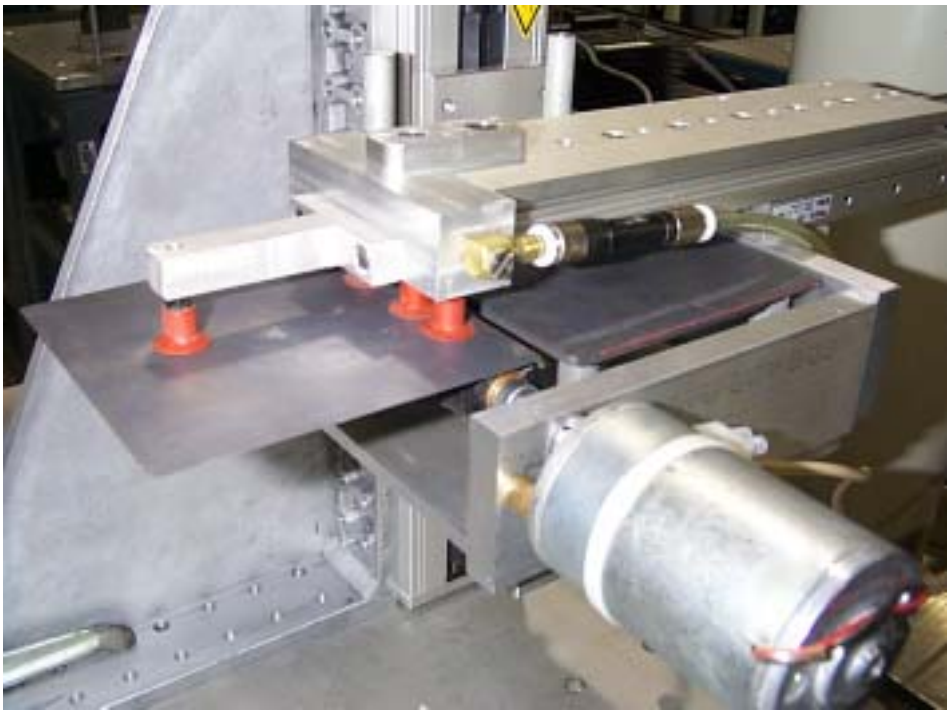

Figure 9: Generation 4 prototype with horizontal coin stack arrangement

Figure 10: Generation 4 prototype, overall view with step-motor stage for raising the coin stack

The Generation 5 prototype incorporated a servomotor as a substitute for the pneumatic horizontal drive. The servomotor allows profiling of the displacement as the wafer is peeled from the stack. It is shown in Figure 11.

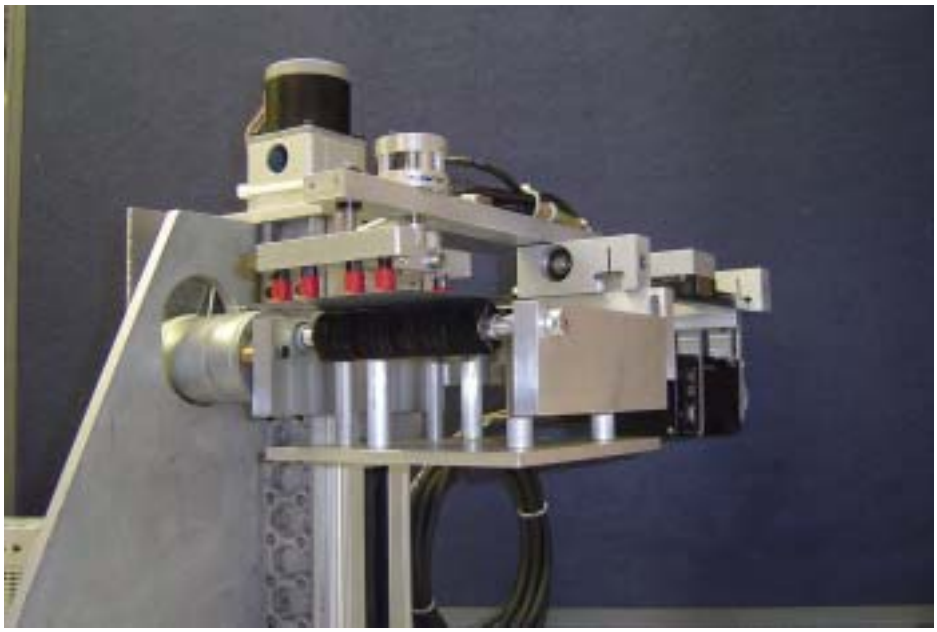

Figure 11: Generation 5 prototype

The last generation prototype developed by ARRI was packaged for stand-alone operation and transported to BP Solar for testing. Testing was performed to validate the vacuum/shearing approach for wet wafer singulation.

Singulation of wafers coming out of the current water cleaning process was unsuccessful; the problem was traced to excessive amounts of solvent present in the water which contribute to warping of the vacuum cup edges, thus losing their ability to sustain vacuum.

The prototype was successfully demonstrated, however, with wafers that had been individually flushed with water and thus were free of solvent (vacuum held with no problems). It is possible that the enhanced performance could have happened because the water cleaning also removed any traces of slurry, but ARRI believes the reason for working better was the availability of a strong vacuum hold.

Additional testing was performed with wafers soaked in slurry exactly as they come out of the wire saw machine (carefully demounted by hand). The intent was to see if the machine could singulate wafers that had not been exposed to solvent and that were heavily drenched in slurry. The prototype was successful in demounting under these conditions. Virtually no slurry ingestion into the vacuum system was observed, presumably due to the heavy viscosity of the fluid. Performance of the vacuum cups in peeling wafers from the stack was satisfactory; although the slurry might have lowered the traction from the vacuum cups, it also works to diminish interfacial frictional forces.

In conclusion the successful demounting of slurry-soaked wafers by the vacuum/shear method suggests the possibility of a one-step process from wire saw to cassetting, avoiding both the solvent and wafer

soaks as currently performed at BP Solar. A solvent soak would still be needed but could be effectively implemented on cassetted wafers. Based on this initial success, ARRI recommends the evaluation of direct-from-wire saw wafer demounting as a Phase II activity.

3.4.2.2 Evaluation of NZCP Handling Techniques

Introduction & Scope

This activity focuses on the study of wafer handling techniques that impart minimal ("near-zero contact pressure" or NZCP) on the wafer. Its ultimate objective is to address ultra-thin wafer technology, though some concepts are immediately applicable to current thickness wafers.

Two main factors motivate this study:

- Eventual migration to ultra-thin wafers
- Yield losses with current thickness wafers

Solution Approaches

The traditional technologies used for wafer handling are conventional vacuum cups and parallel grippers. Vacuum handling, due to its simplicity, is preferred in nearly all operations where contact with the wafer surface is acceptable. The current vacuum systems are, in fact, unsophisticated in that they are not designed for stress minimization, and use standard off-the-shelf spring-loaded compliance devices. The technologies investigated during this study extend from conventional but optimized vacuum systems to approaches that have no commercial embodiment. Those studied were:

- Electrostatic chucking
- Electrostatic levitation
- Acoustic levitation
- Air levitation
- Light-touch finger/vacuum
- Adhesives

Preliminary Analysis

The main critical factor in handling fragile wafers is reducing localized stresses – achieving the most even distribution possible of forces. That is, a near-zero contact *pressure* – and not near-zero contact *force*, is sought. The second critical factor is to minimize, or if possible and sufficiently economical, avoid altogether surface contact.

Electrostatic handling holds much promise as an NZCP wafer handling method. Electrostatic *levitation* has been achieved mainly at the research level. It should be investigated further for critical non-contact operations; it is discussed in more detail in the next section. The electrostatic *chucking* (contact) method is already in use in semiconductor manufacturing, and is explained in more detail. Chucks with special surface designs can also minimize surface contact.

Air levitation is possible and has been previously investigated under prior PVMaT work. A new version has been devised based on diffuser principle, generating vacuum on the part by imparting a high-speed, radial-flow jet on the center of the wafer. Biasing the jet strength can impart motion, although the present work has concentrated on single wafer acquisition rather than transport. This work has been successful and a detailed report is included.

Acoustic levitation can potentially suspend but not acquire wafers; as such, it has only limited potential.

Light-touch finger/vacuum is based on conventional technology; its best application is in employing FEA to establish optimal distribution of cups for minimal stress.

The adhesive method difficult to implement, and is potentially unsuitable due to surface contamination.

Electrostatic Levitation

An electrostatic manipulator can handle thin wafers in a contact-less manner using the "Direct Electrostatic Levitation and Propulsion (DELP)" technology (developed by Applied Electro-Optics Inc. of Mansfield, Massachusetts). The novel aspect of this manipulator is that it does not distort wafer's shape during the handling process. This is because that the force applied to the wafer is same as that of the wafer's gravity. Furthermore, the force is evenly distributed on a wafer.

When the overlapping area of an electrode and a wafer is large enough compared with the gap between them, to a close degree of approximation, the electrostatic force can be represented as

$$F = \varepsilon A V^2/(2x^2)$$

Where

F: Electrostatic attractive force,
ε: Permittivity,
A: Overlapping area,
V: Voltage applied to electrode,
x: Gap between electrode and wafer.

It is clear from the above equation that the electrostatic force is inversely proportional to the square of the gap between the electrode and a wafer, so it is impossible to achieve a stable levitation without controlling the voltage applied to the electrode. Figure 12 is a schematic diagram of an electrostatic levitation system with one degree-of-freedom. It actively controls the wafer's movement in the vertical direction. The vertical position of the wafer measured by a displacement sensor is fed into a controller as feedback signal. The controller compares the wafer's current position to the reference position, generating a control signal using appropriate control algorithms. The control signal is then amplified by a high voltage amplifier and applied to the electrodes. The effect of this is to modify the force-gap characteristics such that the voltage, and thus the electrostatic force, increases as the gap increases, and vice versa. In the equilibrium position, the electrostatic force is balanced against that of gravity, the wafer is stably suspended under the electrodes at the desired gap.

In a real system, a wafer's movement in the following five degrees-of-freedom is controlled:

1) Movement in horizontal plane (2 degrees-of –freedom),
2) Movement in vertical direction,
3) Pitching and,
4) Rolling.

The movement in horizontal plane can be passively restricted either by mechanical stoppers or by lateral force. The remaining three degrees are actively controlled by the method described above.

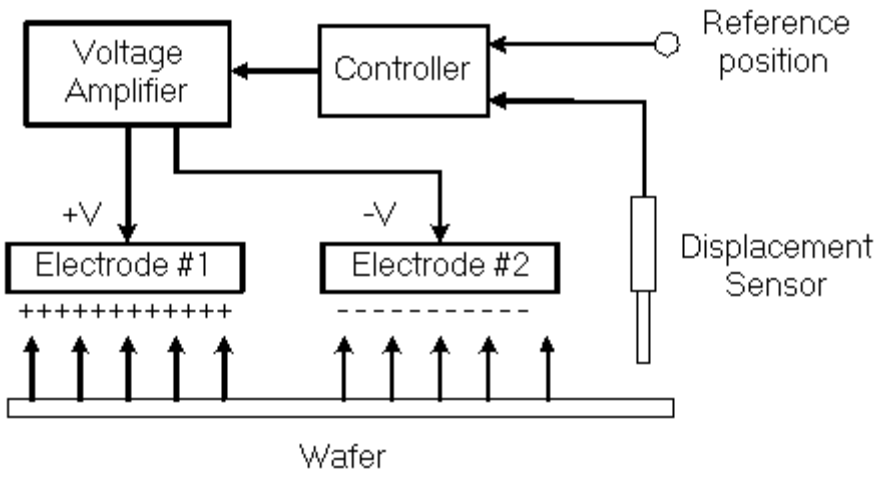

Figure 12: Single degree-of-freedom electrostatic levitation system

Figure 13 shows a point-to-point wafer handling system using electrostatic levitation technology. The wafer being transported is a standard 12-inch diameter single crystal silicon wafer, which is suspended under the levitation unit with a 400 microns gap. The levitation unit is mounted on a linear stage, which is driven by pressurized air.

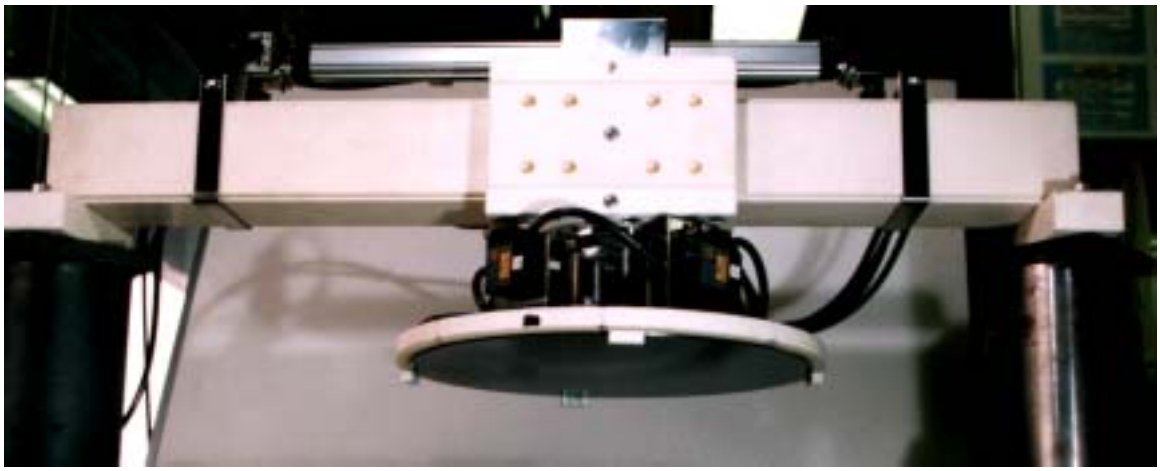

Figure 13: Electrostatic Wafer Levitation Device

Electrostatic Chuck

Based on promising preliminary work, ARRI has purchased a custom-designed and fabricated electrostatic chuck. Unlike the work described in the previous section, this full-contact method does not employ position feedback to maintain an air-gap with the wafer. As such, it is considerably less complex and expensive. Proper design of the chucking surface can minimize contact area. Test results on this device are forthcoming as soon as the test item is available to ARRI.

Air Levitation

Three prototypes have been produced and evaluated. All are based on the principle of generating a horizontal stream of high-velocity air over the surface of the wafer to produce a vacuum; the air-stream is rendered horizontal either by direct impingement on the wafer or by the action of a flow-diverting valve.

Two of the designs are non-contact, with the wafer levitating as if on an “upside-down” air table, and the third exerts minimal contact to stabilize its horizontal motion. Figures 14, 15 and 16 show pictures of the three prototypes tested (valves, where used, are shown in their extended position for visibility).

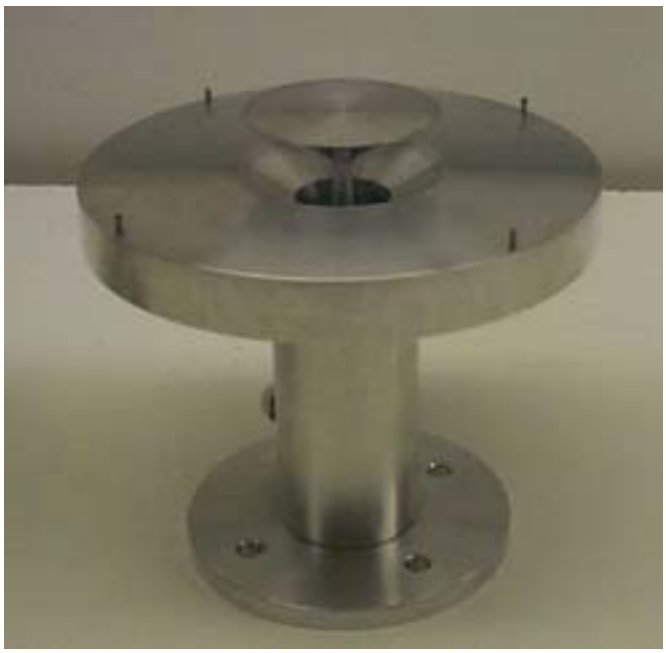

Figure 14: Non-contact valve nozzle design

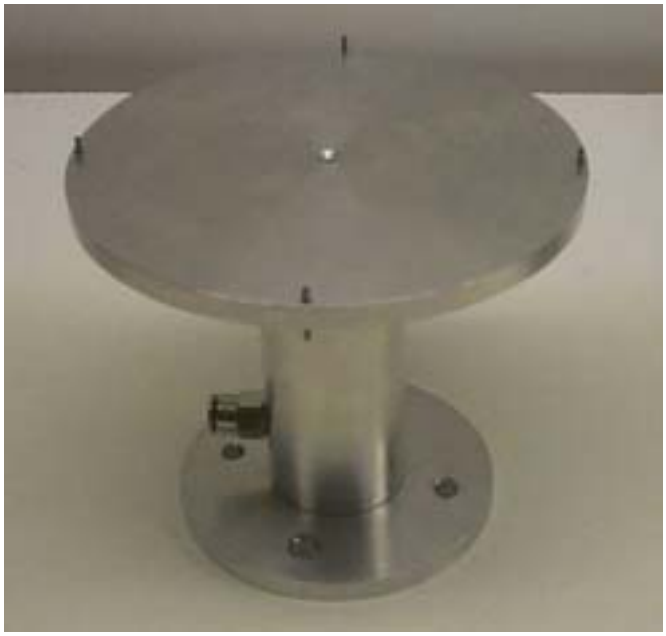

Figure 15: Non-contact valve diffuser design

Figure 16: Low-contact valve diffuser design

The prototypes depicted above were tested in a robotic cell to perform dry coin stack wafer acquisition. The tests were very successful, illustrating the suitability of these devices. Figure 17 below depicts the basic test setup.

In order to evaluate the performance of the three nozzles, a series of tests were conducted. These tests involved the flow rate, noise output, and the lift capacity. The three nozzles exhibited similar behavior in that 8 psi was around the minimum pressure to lift the wafer off a surface and 9.2 psi produced an acceptable amount of lift to firmly hold the wafer in place. In the first test, the flow rate in standard liters per minute was measured. It was observed that the nozzle design yielded approximately twice the flow rate as the diffuser.

Table 2: Flow Rate of air levitation prototypes

	Diffuser	Contact Nozzle	Non-contact Nozzle
8.0 psi	**35 L/min**	**61 L/min**	**64 L/min**
9.2 psi	**37 L/min**	**67 L/min**	**68 L/min**

These values compare favorably with the consumption of a typical vacuum pump for a wafer pickup application, which averages about 140 SLPM.

The second criterion evaluated was the noise output. First, the background noise was measured. Next, the noise for each design was measured. The recorded values are the differences between the two. Measurements were taken one foot from the outer circumference of the flange.

Table 3: Noise Output of air levitation prototypes

	Diffuser	Contact Nozzle	Non-contact Nozzle
8.0 psi	**+2.5db**	**+0.5db**	**+2db**
9.2 psi	**+4.5db**	**+1.0db**	**+2db**

The third criterion evaluated was the lifting force generated by each nozzle. A small ceramic plate had additional standard weights added (nickels) until the weight could no longer be lifted.

Table 4: Lifting Force of air levitation prototypes

	Diffuser	Contact Nozzle	**Non-contact Nozzle**
10 psi	**1.1 ± .05 oz**	**3.4 ± .05 oz**	**3.7 ± .05 oz**

As a final test, the three nozzles were placed on a robotic arm as shown in Figure 17 and were subjected to a stack-to-stack transfer test. The maximum speed of this robot arm was around 45 in/sec horizontally and it was able to move the 250-micron wafers at that speed.

Figure 17: Robotic transfer test of air levitation prototypes

The radial diffuser and nozzles present a promising new approach to handling the wafers. The diffuser consumes less air than the other two but generates the lowest lift. The contact nozzle holds the wafer in place but the contact may not be compatible with some processes. The no-contact nozzle appears to be the best concept because it generates the most lift and consumes roughly the same amount of air as the

contact nozzle. The robotic testing proved that the devices could adapt to a fast horizontal speed. Air consumption is lower than that required for standard vacuum cup systems, runs at lower pressures, and demands no special filtration requirements.

3.5 Cell Process Development

In this task, BP Solar is developing high efficiency cell processes for very thin silicon wafers (with the assistance of North Carolina State University). BP Solar is assessing the compatibility of the process cell and module process equipment to handle 100 μm thick wafers.

3.5.1 Texturing work

Effective surface texturing will be important to provide good light trapping in thinner cell designs. Two different approaches have been investigated:

Reactive Ion Etching (RIE)
Work progressed on the RIE program in cooperation with Gratings, Inc. The decision was taken to complete Task 3, which compared three levels of texture etch, using the silicon nitride-based cell process rather than our standard sequential-fire TiOx baseline process. This was driven by disappointing results in earlier trials as well as the fact that BP Solar was implementing the nitride process worldwide to replace the TiOx process. The wafers were sent to Sydney for diffusion and nitride deposition following the texture etch work done at Gratings.

Sydney diffused the cells in the belt furnace after applying a relatively light doping layer. Previous work had identified this recipe as the best diffusion condition for use with the silicon nitride fire-through metallization sequence. Unfortunately, the cell results were not a good as we had hoped. However, the material utilized in Task 3 was from the top end of a brick that was later identified as being with a region where the material quality was rapidly decreasing as a function of position. The data is presented below, along with photographs of example wafers and finished cells from each of the three groups:

Note the relatively small increase in current even thought the cells appear quite dark to the eye. At present, this effect has not been satisfactorily understood. The largest increase (as a group) was 1.2% relative compared to the controls. In the case of the “under-etched” group, (which appears darkest) the device quality was so poor that we could not measure a meaningful Isc value.

Filename: C:\NewTree\Projects\RIE\PVMaT 2003 Work\Task3\[PvMaT RIE task# 3.xls]Titles & ID *Reference Cell:* 1 clad 60-1
Substrate Unkown Poly *Prepared By:* TDK/BK
3/12/03 3:53 PM *Cell Size (cm^2):* 156

RIE PvMaT Work
Task#3 (HBB SiN)

	--N--	EFFIC (%)	PMAX (WATTS)	ISC (AMPS)	VOC (mV)	FF (%)	RSER (mOHM)	RSH (OHMS)	N FACT.
Unencapsulated results, not corrected for spectral mismatch						*p-values based on a 2-sided t-test w/ df adj. by F-test*			
Controls TiOx		12.04	1.88	4.585	576.8	71.2	9.3	10.0	1.40
Group 1	*--11--*	*(0.19)*	*(0.03)*	*(0.034)*	*(2.2)*	*(0.5)*	*(0.3)*	*(3.3)*	*(0.06)*
Etch #1 "over etched" SiN		12.15	1.90	4.642	572.1	71.5	7.8	60.9	1.41
Group 2	*--8--*	*(0.16)*	*(0.02)*	*(0.021)*	*(2.7)*	*(0.8)*	*(0.3)*	*(20.1)*	*(0.07)*
	Delta:	0.10	0.02	0.057	-4.7	0.3	-1.5	50.9	0.02
	Delta%:	**0.8%**	**0.8%**	**1.2%**	**-0.8%**	**0.4%**	**-16.0%**	**510.8%**	**1.2%**
	p-value:	.23	.23	.00 *	.00 *	.31	.00 *	.00 *	.60
Etch #2 "medium etched" SiN		12.01	1.88	4.582	568.9	72.0	7.8	57.0	1.38
Group 3	*--11--*	*(0.12)*	*(0.02)*	*(0.033)*	*(1.7)*	*(0.5)*	*(0.1)*	*(17.2)*	*(0.04)*
	Delta:	-0.03	0.00	-0.003	-7.9	0.8	-1.6	47.1	-0.02
	Delta%:	**-0.3%**	**-0.3%**	**-0.1%**	**-1.4%**	**1.2%**	**-16.8%**	**471.9%**	**-1.4%**
	p-value:	.64	.64	.85	.00 *	.00 *	.00 *	.00 *	.38
Etch #3 "under etched" SiN		10.54	1.65	4.189	553.1	71.0	7.4	51.0	1.50
Group 4	*--10--*	*(0.31)*	*(0.05)*	*(0.095)*	*(3.0)*	*(0.9)*	*(0.3)*	*(27.2)*	*(0.09)*
	Delta:	-1.51	-0.24	-0.395	-23.7	-0.1	-1.9	41.0	0.10
	Delta%:	**-12.5%**	**-12.5%**	**-8.6%**	**-4.1%**	**-0.2%**	**-20.7%**	**411.5%**	**7.3%**
	p-value:	.00 *	.00 *	.00 *	.00 *	.70	.00 *	.00 *	.00 *

Table 5: RIE Etch conditions Trial Results

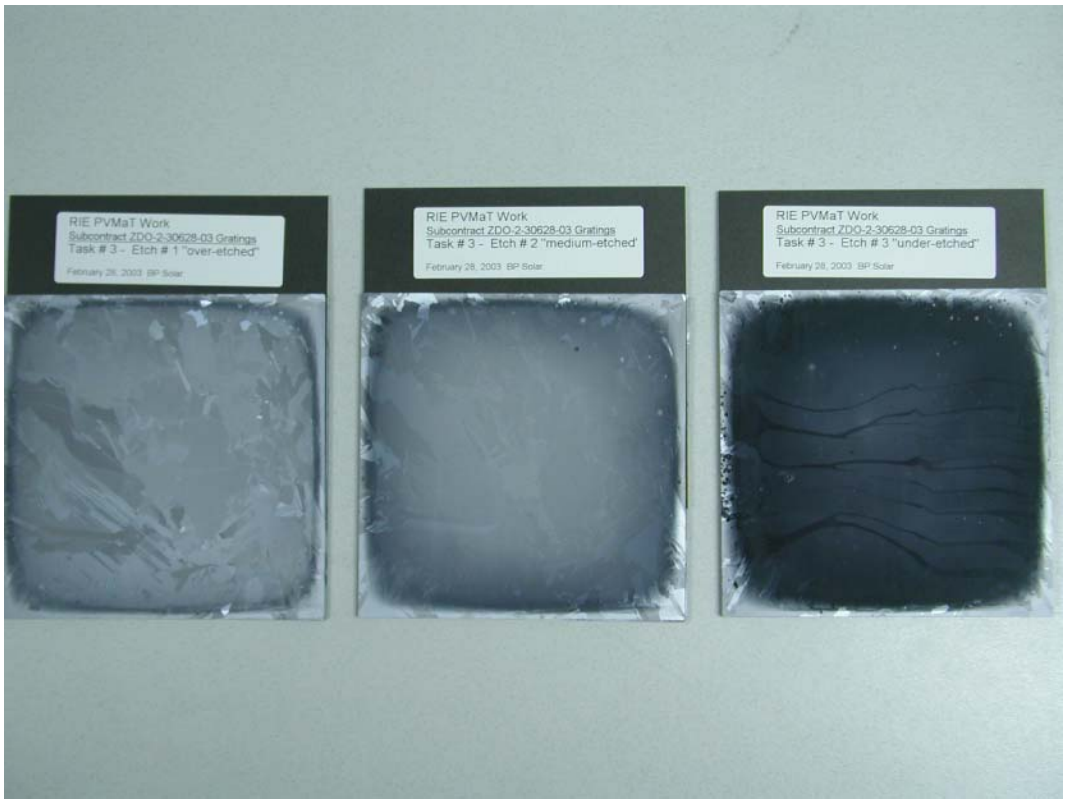

Figure 18: RIE Etch Conditions Trail Results

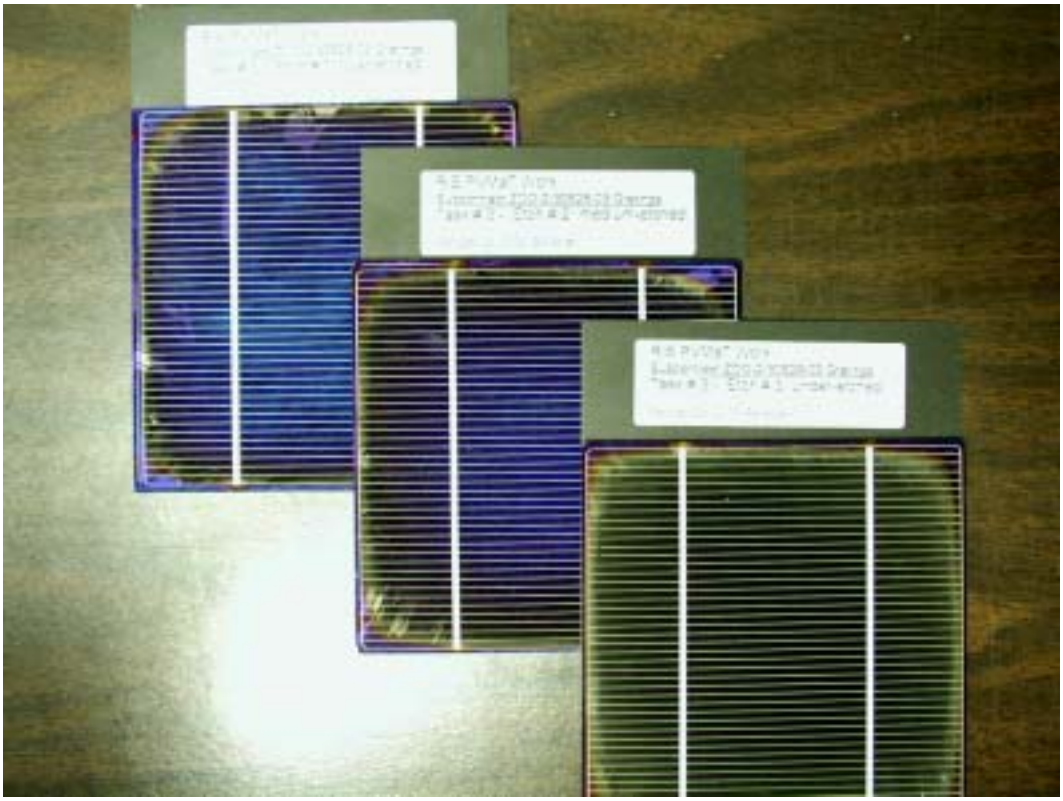

Figure 19: RIE Etch Conditions Trial – Finished Cells

Chemical Iso-Texture

Cell processing of wafers textured using an "Iso" chemical process was completed along with a matched set of control wafers. The surface texturing was analyzed using Scanning electron Microscopy, as shown in Figure 20. The cell process sequence included: iso chem. texturing, emitter diffusion (55 Ω/sq), edge isolation by plasma etching, PECVD-SiN deposition, screen print of front and back contacts and fire in an IR-furnace. The cell results showed a significant increase in the short circuit current density and cell conversion efficiency as shown in Figures 21 and 22. The cell parameters are presented in Table 6.

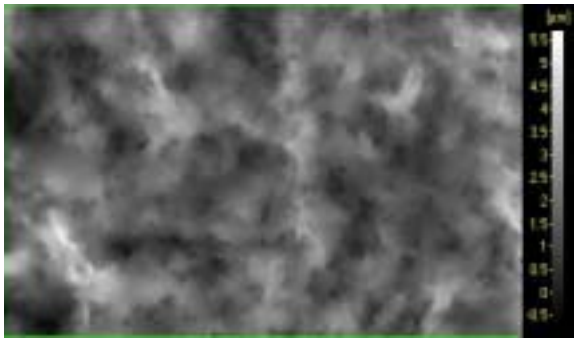

Figure 20: Height topography of an isotropic textured wafer area of app. 60×30 μm². The 3 dimensional surfaces were calculated from 2 electron microscope images taken at different angles.

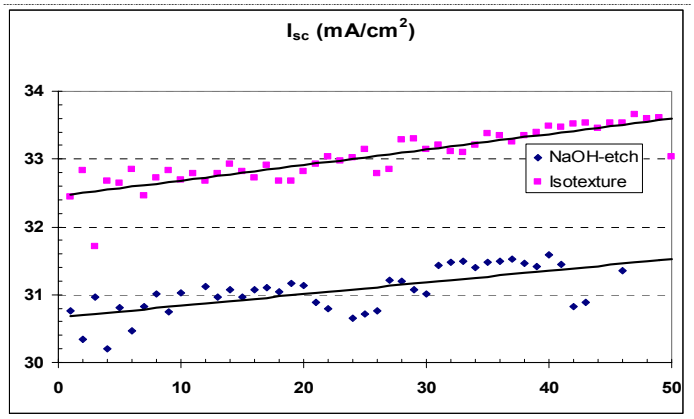

Figure 21: J_{sc} of neighbouring iso textured and alkaline etched wafers. The gain due to the texture is in the range of 2 mA/cm².

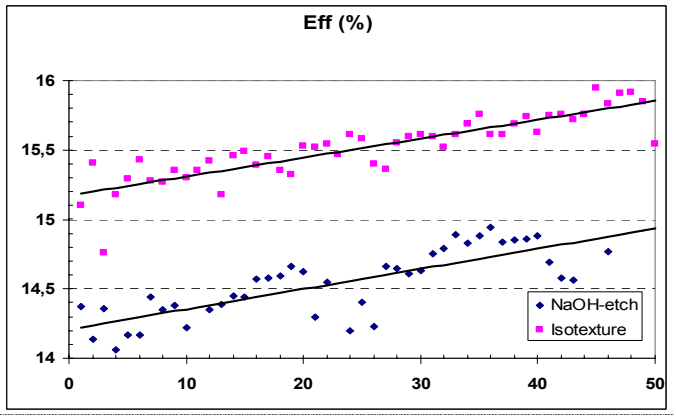

Figure 22: Performance of neighbouring iso textured and alkaline etched wafers. The gain due to the texture is in the range of 1 % absolute.

Table 6: I-V characteristics of the best 36 cells from Figures 21 and 22. There is an absolute gain of 2 mA/cm² in J_{SC} and 1 % in efficiency

	FF	**J_{sc}**	**V_{oc}**	**Eff.**
	%	**mA/cm²**	**mV**	**%**
NaOH	76.3	31.2	615.9	14.6
Iso texture	76.6	33.2	614.1	15.6
Gain	0.3	**2.0**	-1.8	**1.0**

Detailed characterization of these cells was also completed. The spectral response data (as shown in Figure 23) indicates that the quantum efficiency of the iso chemical textured cells improved in the shorter wavelength region.

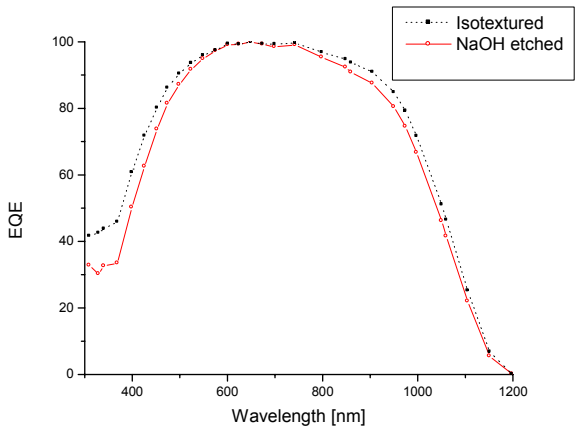

Figure 23: Comparison of EQE of the iso chemically textured cell and the control cell

Two modules were made – one with the iso chemical textured cells and the other with the baseline control cells. As can be seen from Fig. 24, the textured module has a darker and more homogeneous appearance when compared to the control module. Module measurements indicate that there is still a gain in I_{sc} of 4.2 % and power of 4.8 % relative (as shown in Table 7).

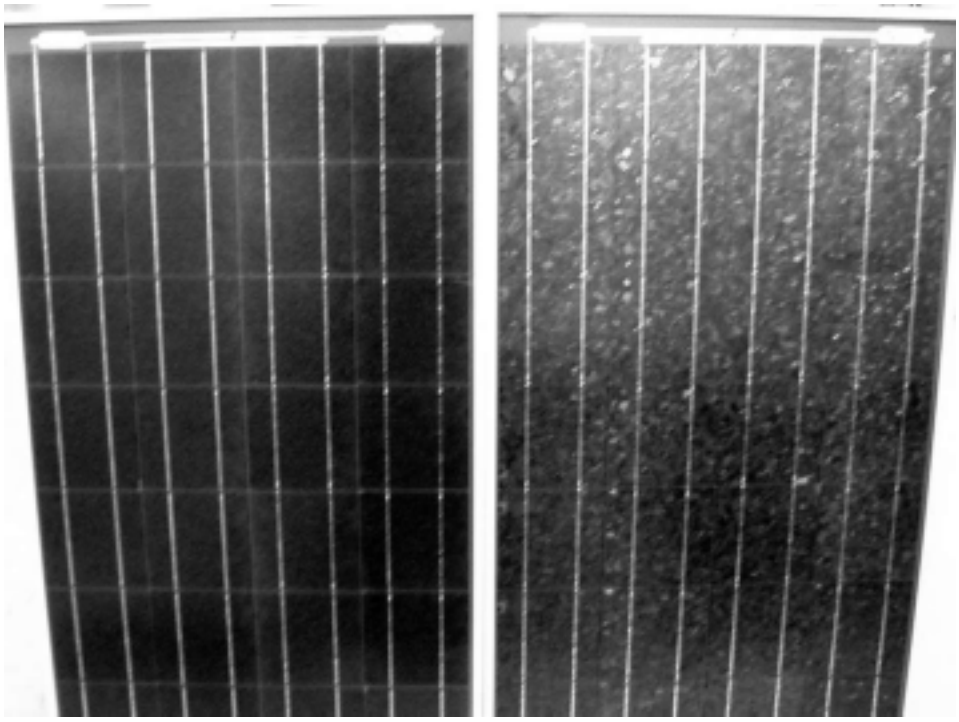

Figure 24: 36 cell modules made of neighbouring wafers. Left: iso textured (86.5 Watt); Right: NaOH etched. (82.5 Watt), a 4.8 % relative increase in efficiency

Table 7: I-V characteristics of the 2 modules shown in Fig. 24 and the calculated values of the cells.

Module	**FF**	**I_{SC}**	**V_{OC}**	**P**
	%	**A**	**V**	**W**
NaOH	74.5	4.98	22.2	82.5
Iso textured	75.0	5.19	22.4	86.5
CELL	**FF**	**J_{SC}**	**V_{OC}**	**Eff.**
	%	**mA/cm²**	**mV**	**%**
NaOH	74.5	31.9	616.7	14.7
Iso textured	75.0	33.2	622.2	15.4
GAIN [%]	**0.6**	**4.2**	**0.9**	**4.8**

3.5.2 Silicon Nitride High Efficiency Process Development

The objective of this work was to increase the performance of the BP Solar cell lines from an average cell efficiency of 12.8% to an average of 14.5% by replacing the existing, TiOx-based anti-reflection coating process with a silicon nitride-based process. The new process uses a PECVD silicon nitride coating and subsequent fire-through metallization step to provide significant bulk and surface passivation of the solar cell, resulting in the increased efficiency. This process had been previously installed in the Tat-BPSolar facility in Bangalore, India. The installations in Sydney and Frederick used different equipment set, with in-line, remote plasma deposition equipment instead of the batch-style, direct plasma equipment used in Bangalore.

A comprehensive cost of ownership (CoO) model showed that the operational cost of the new equipment would be significantly better than that of the older equipment, as long as the performance was equivalent for the two equipment sets.

Details of this work have been extensively reported in the monthly contract reports. The equipment in Sydney has been in operation since September 2002. The Frederick equipment was started up in August 2003. The first 80,000 cells produced in Frederick had an average efficiency of 14.46% at the cell test level. Photographs of the new silicon nitride building in Frederick and the equipment are shown below in Figures 25 and 26.

3.5.3 Passivating AR Coatings

This current program is a continuation of previously funded research collaborations between BP Solar and NC State University. The previous 2-year program established a mechanism for the enhanced photovoltaic response of polycrystalline silicon solar cells that was associated with interface passivation that occurred during the processing of silicon nitride anti-reflection coatings. This work indicated that the enhancement does not derive from a transport of H-atoms from the hydrogenated Si_3N_4 layer into the poly-silicon film as had previously proposed. Instead, it was shown that the enhancement derived from a thin interfacial SiO_2 layer between the polycrystalline silicon and non-crystalline Si_3N_4 layer. This

interfacial layer reduces surface recombination at interfaces between poly silicon and Si_3N_4 in essentially the same way that it improves the performance of silicon metal oxide semiconductor, MOS, devices.

Figure 25: New Building for Silicon Nitride Deposition – Frederick

Figure 26: Loading End of In-line Silicon Nitride Equipment - Frederick

The current research builds on previously funded work. Studies on metal-oxide-semiconductor, MOS, devices have demonstrated fixed positive charge of approximately $8x10^{11}$ cm^{-2} at the internal dielectric interface between SiO_2 and Si_3N_4. This charge produces band bending in the poly silicon that is in the wrong direction for efficiently carrier collection from the n-region of the solar cell. Studies of MOS devices with alternative dielectric materials, such as Al_2O_3, ZrO_2, Ta_2O_5 and Zr and Hf silicates have indicated that the sign and concentration of fixed charge at the internal interface between an ultra-thin, ~0.6 nm, surface passivation layer of SiO_2, and an alternative dielectric can be controlled, and actually changed from positive to negative through alloying. The proposed research will investigate the effect of internal charge on collection of minority carrier holes. By controlling the thickness of the alternative dielectrics, these layers can also act as anti-reflection films.

The fixed charge is negative for Al_2O_3, and positive for all of the other oxides and silicates indicated above. The specific proposal is to engineer a multi-layer dielectric in which an interfacial SiO_2 layer is used to form the low defect density interface, and either an Al_2O_3, or Al_2O_3-alloy (e.g., with ZrO_2) is used to control the internal dielectric space charge, optimizing it for the photovoltaic application.

Research Objectives

The objectives of the current task are three in number.

i) To develop remote plasma processing for separate and independent control of silicon-dielectric interfaces, and bulk dielectric films for second generation anti-reflection coatings for polycrystalline silicon solar cells;
ii) To develop a capability for deposition of hafnium oxide and hafnium silicate alloys for substrates up to three inches in diameter; and
iii) To build on the results of the previous phase, and develop an atomic scale understanding of bonding at silicon-dielectric interfaces that is optimized for solar cell performance.

Progress Report

(a) Relaxation of interfacial bond stress at silicon-dielectric Interfaces

Based on research performed under ONR and SRC sponsorship, it has been demonstrated that the SiO_x layer self-organizes to minimize bonding and thermally induced strain across the poly silicon dielectric interface. This reduces defects and defect generation under device operation, and is an important factor that must be integrated into anti-reflection coatings on photovoltaics (see Fig. 27). In particular, advanced anti-reflection coatings must be comprised of composite dielectrics, similar to the Si3N4 anti-reflection coatings that contain a thin SiO_2 interfacial layer to control interfacial defects and a thicker film to provide spectroscopically controlled reflectance.

(b) Advanced dielectrics for anti-reflection coatings

A new capability has been developed in our processing facility to incorporate mixed dielectric alloys comprised of Al_2O_3 and HfO_2 or ZrO_2 alloyed with SiO_2. Proceeding in this way, the fixed charge at an internal interface between a superficially thin SiO_2 interfacial layer, and the bulk dielectric anti-reflecting film can be controlled continuously from negative (Al_2O_3) to positive HfO_2 or ZrO_2 while providing the controlled optical reflectance. Figures 28 and 29 are obtained from the analysis of capacitance-voltage traces obtained on metal-oxide-semiconductor devices, and indicate a range of control from approximately $-7.5\pm1x10^{12}$ to $+5x10^{12}$ unit charges/square centimeter. This is sufficient to swing the surface potential of the surface of the silicon photovoltaic device from hole to electron accumulation, and therefore control the surface recombination of photo-generated minority carriers over a range compatible with optimized photovoltaic performance.

Plans for the Next Year

During the next year of the program, multi-layer dielectric films will be integrated into PV devices to order to evaluate changes the short-wavelength response due control of the to the surface recombination velocity at the surface of the device. P-N and N-P solar cell structures will be studied in order to quantify the relationship between spectral response and collection of photo-generated minority carriers.

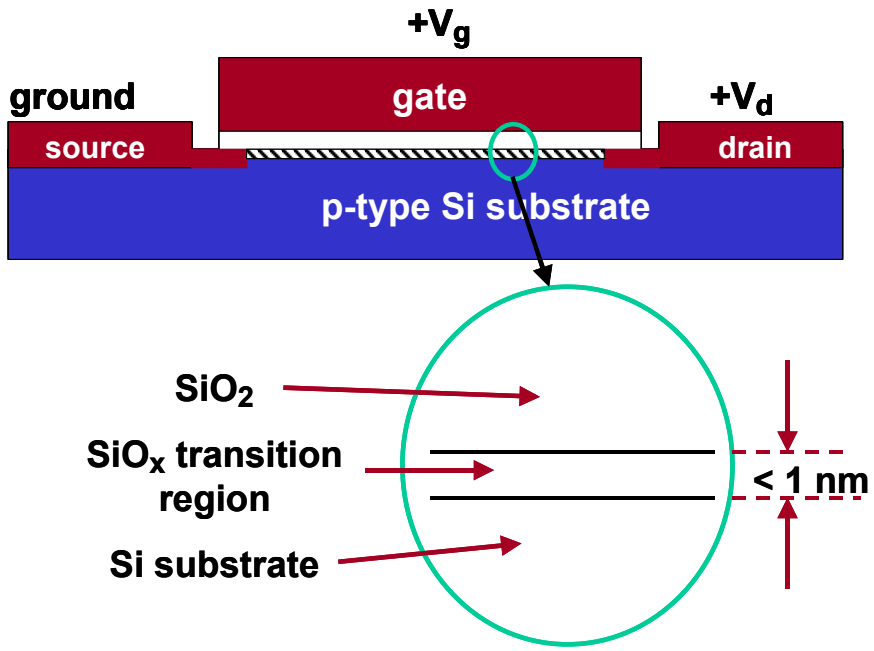

Figure 27: Composite dielectric in a field effect transistor. This same bi-layer dielectric structure forms the basis for advanced anti-reflection coatings in PV devices.

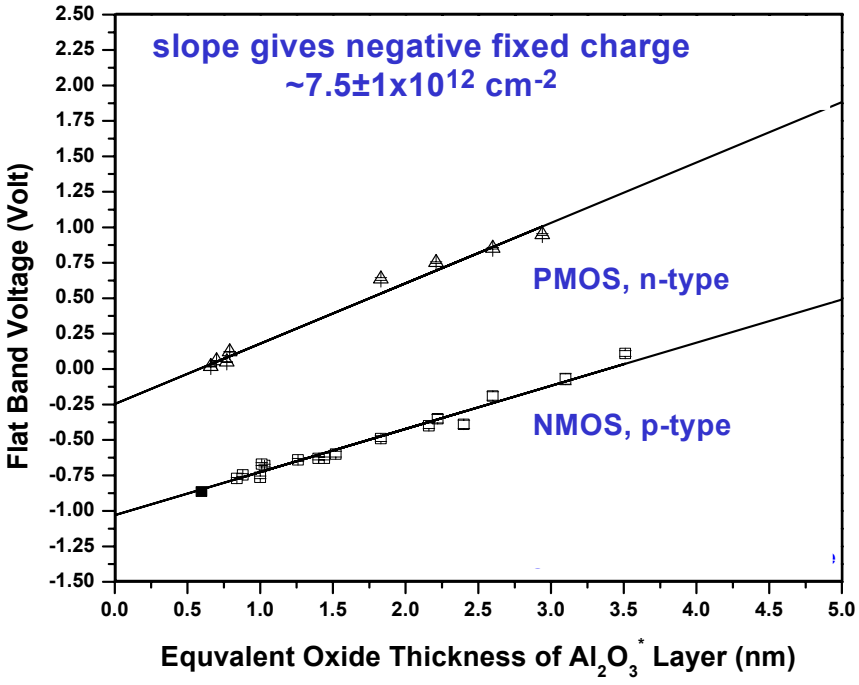

Figure 28: Capacitance-voltage plot of an Al_2O_3 MOS device. The slope of these plots corresponds to a fixed negative charge level of approximately -7.5+/-1x10^{12} cm^{-2}

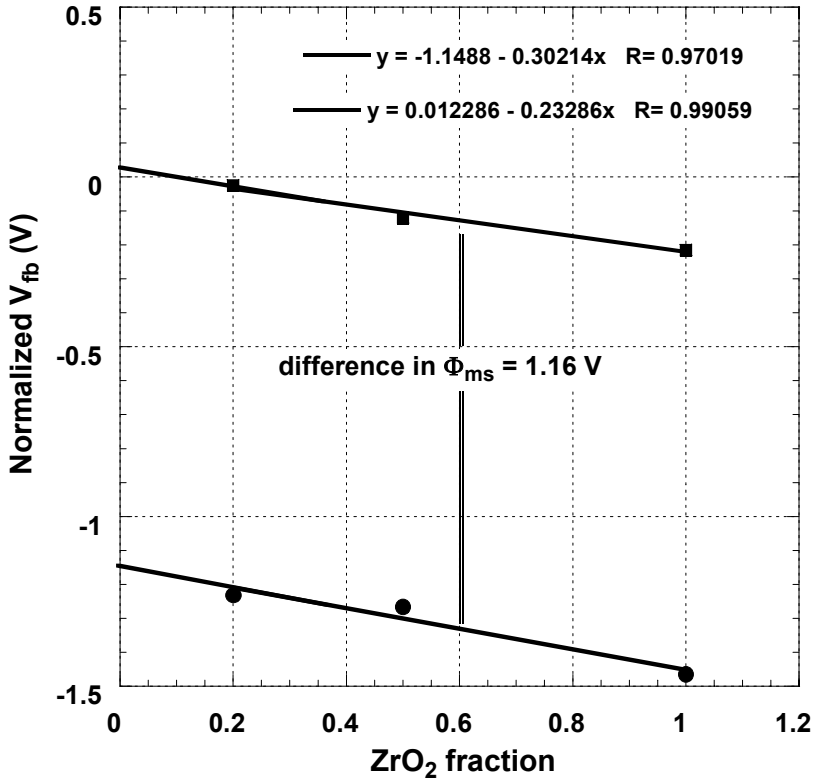

Figure 29: Capacitance-voltage plot of a ZrO_2 MOS device. The values of normalized flat band voltages of this plot indicate a range of control of fixed positive charge extending from the mid 10^{10} cm^{-2} level to approximately 5x10^{12} cm^{-2}.

3.6 Module Assembly

In this task, BP Solar is developing and demonstrating a module assembly process and the equipment suitable for very thin solar cells. This task is expected to result in an assembly process capable of producing framed, terminated PV modules using very thin cells at an overall yield exceeding 98%.

3.6.1 Laminated Diodes

Incorporation of bypass diodes is necessary in all but the smallest 12-volt modules. As cells get larger, the diodes must be able to carry the extra current produced by the larger cells. As modules get larger the number of diodes increases as a diode is required for every 12 to 24 cells, depending on the reverse behavior of the cell type. Indeed use of higher efficiency cells usually means fewer cells per diode.

When most modules had 36 cells, it was easy to build two strings of 18 cells and have each string protected by a diode in the junction box. Today most modules have more cells (typically 72) and the trend is away from junction boxes toward quick connectors. In this case, the added diodes require extra penetrations into the laminate, attachment of the diodes and potting within a small junction box. These processes are not readily automated so add significant labor to the module cost.

A laminated diode eliminates these external diode mounts and extra parts and the steps required to protect them from corrosion, and simplifies the circuitry. The laminated diode assembly consists of surface mount type Schottky diodes pre-assembled with copper strips coated with silver. The cell matrix is connected to this laminated diode assembly, and the whole assembly is then encapsulated between the glass and the back sheet as routinely done on current PV laminates. The external diode connections are no longer required. This means a total elimination of enclosures and encapsulant filling.

This concept is not new, as BP Solar (then Solarex) produced several hundred modules with laminated diodes in the mid-1990's. One such system with 144 MSX-240 modules has been operating in California for more than 5 years. A field trip to the California site was conducted in order to evaluate the performance of the laminated diodes. The system is shown in Figure 30.

Figure 30: Array of 144 MSX 240 Modules on Trackers in California

All 144 MSX 240 modules were visually inspected for cracks, burn marks and flaws. All were in good condition with no cracks, burn marks or delaminations observed. Each section of the system was producing the AC output power expected for the solar conditions that day.

An IR camera was used to inspect every module. During normal operation, (with modules free of shadowing) there was no indication that any of the bypass diodes were turned-on. Further observation was taken on the effect of shading the module. Figure 31 was taken without any shading. Figure 32 shows the activation of the diode after shading one cell of the module. The red dot showing the increased heat of the diode, function is proper. After removal of the shading, the diode returned to the state shown in Figure 31 in 30 seconds. This process was repeated on 20 randomly selected modules, all with the same result. Shading times were varied from 1 to 10 minutes.

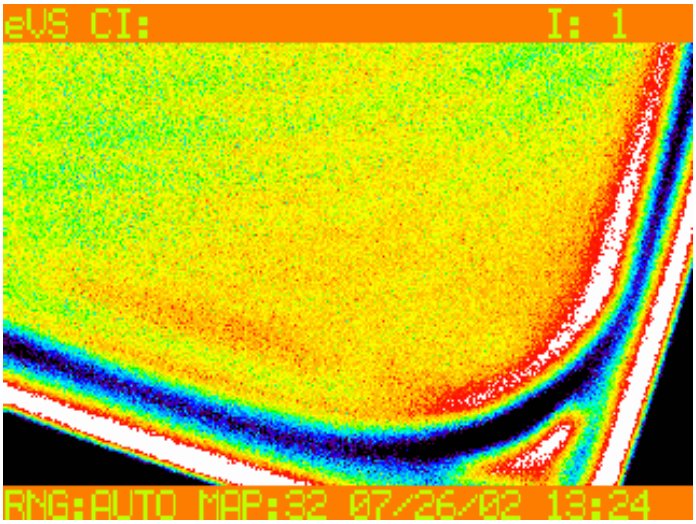

Figure 31: IR Image of By-Pass Diode with No Shading

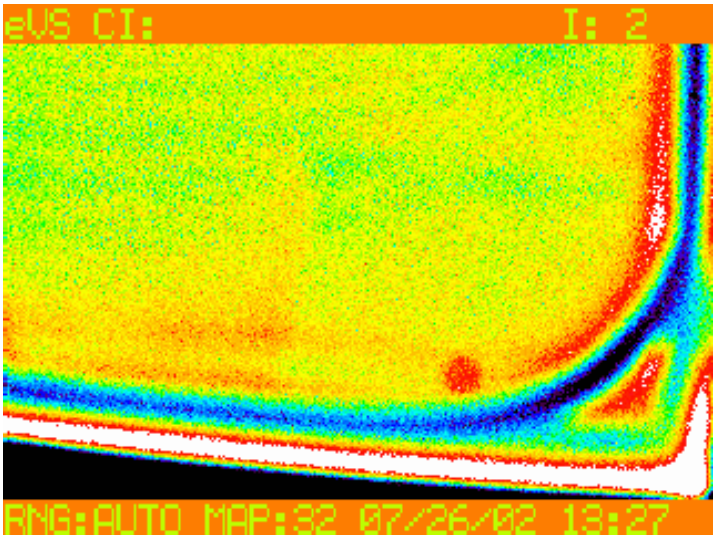

Figure 32: IR of By-Pass Diode Image with Shading

After an installation period of five plus years, all modules (MSX 240) seem to be functioning properly in regards to diode operation. Visually, there were no flaws such as cracking, delaminations or burn marks

found. There aren't any signs of overheated diodes or cells within the modules. In all cases, the diodes returned to normal (the off-state) within 30 seconds after shading was removed.

In the past incorporation of chip diodes into the laminate has not been easy to accomplish because chip diodes tended not to be capable of carrying as much current as was necessary and it was difficult to correctly heat sink them. Recently high current chip diodes have become available at reasonable cost. In addition, circuit board type bus bars and heat sinks are available commercially.

A preliminary module design was developed using chip diodes mounted on circuit boards. Sample modules were then fabricated. These samples were subjected to and successfully passed the following tests.

1. **Internal Qualification (for a 25-year warranty)**
   Five hundred (500) Thermal Cycles (-40 to + 85° C)
   1250-hour Damp Heat (85° C, 85% RH)
   50 Thermal Cycles and 10 Humidity-Freeze Cycles
2. **External Certifications**
   IEC61215 certified at Arizona State University (ASU)
   Safety Class II 1,000V (Cut test and High Voltage test) certified at TUV
   UL safety certified to 1703
3. **Other Tests**
   Impulse Voltage test at TUV
   IEEE1262 - Bypass Diode Thermal Test at ASU

The BP5170S module was selected as a pilot run candidate due to the complexity of its cell matrix layout. The present design requires six diodes and three small potted junction boxes for each 72-cell module. Two pilot run trials were successfully conducted at two major BP Solar manufacturing sites: Madrid (Spain) and Frederick (USA). The laminated diode boards functioned properly in the pilot run samples and no performance deviations were recorded. A saving of 5 minutes in the assembly line was achieved.

Approximately 2,000 BP5170S units with laminated diode boards have now been built in the Frederick plant. It will be implemented in full production in the 3rd quarter 2003.

Module Terminations:
Presently BP Solar produces modules with two different junction boxes. One was the heritage Solarex box and the other was the heritage BP Solar box. After the merger, an initial effort to eliminate one box was halted due to dissatisfaction among customers of that box. Each of these boxes has its advantages and disadvantages. The biggest disadvantage is the cost of having two separate parts and all of the associated hardware. So the second part of the module electrical termination program will be to design, qualify and implement a new junction box to replace the two now in use.

The differences between the two boxes are summarized in Table 8. The question then becomes which of these properties should be incorporated into the new hybrid box. To answer this question we utilized a survey of Distributors, Dealers and large customers. A list of the most important features requested for the box is given below.

Table 8: Comparison of Two BP Solar Junction Boxes

Property	**BP Heritage**	**Solarex heritage**
NEMA IP Rating	IP65	IP54
Lid type	Hinged flip lid	Tuck and screw lid
Adhesive area	Small	Large
Output holes	Smaller PG13.5 holes	4 punch-outs for PG 13.5 or ½"
Electrical terminations	Adel or Wago	Bussman 6 terminal strip
Ability to attach to frame	No	Yes

Junction Box Features Selected in Customer Survey

- Box not taller than the frame
- Knockouts for cables and conduits
- At least 2 extra screws over the minimum necessary
- Ability to attach to frame
- The results were almost evenly divided between requesting IP65 and IP54
- Hinged lid

Based on this analysis a preliminary design of a new junction box was completed. The design meets all of the survey selections including being able to offer the same box with or without a gasket to meet either IP65 or IP54. The initial cost analysis of the new design indicated a cost savings of between $750,000 and $1,000,000 a year at today's volume.

The proposed new junction box design combines the best features of both "heritage" j-boxes presently used. These key features include:

Solarex (SPJB) j-box:

- Accepts both English and metric size conduit fittings and cable glands. (This is important because FM approval for hazardous locations requires use of "listed" fittings, and only the English sizes meet this criterion.)
- Solid bottom to the box, which prevents accidental damage to the back sheet by screwdrivers during installation
- Provision for easy application of correct amount of adhesive (RTV) for bonding to the back sheet
- Provision for screws to attach the j-box to the module frame, and posts to allow installation of our small charge regulator (SRX6) within the j-box

BP Solar (GSM) j-box:

- Hinged lid, with captive screws to eliminate potential for dropping or losing these parts during installation
- Provision for lid gasket, which can provide IP65 rating when desired
- Accepts lowest-cost terminal block available to meet requirements for current, voltage and wire size ratings

A three-dimensional CAD model of the proposed box has been used to generate stereo lithography (SLA) prototype parts. These parts have been reviewed with key sales personnel in all regions to fine-tune the desired features. All perceived issues have been addressed in the latest version of the design.

Initial discussions with the injection-molding vendor have been completed; to assure that the box can be produced economically. These discussions led to several minor changes in the design from the original concept. Price quotes for the j-box and the mold have now been received.

3.6.2 Interconnection Issues

One of our approaches to making modules with ultra-thin cells is to modify our conventional robot machinery to improve performance. Interconnect soldering of thin crystalline silicon solar cells has been investigated with modifications to robot soldering resistance weld heads and tips. The orientation of the weld head had been changed to increase solder joint surface area and reduce pressure per unit area. Frequency of unacceptable low interconnect pull test values was reduced. Silicon breakage caused by pressure of the interconnect ribbon and solder weld tip was reduced.

A second approach to making modules with ultra-thin cells is to accomplish the interconnection using conductive adhesives without the stresses of conventional soldering. A designed experiment was conducted to evaluate the effects of adhesive joint size, number of joints of adhesive, treated or untreated bond area. The response variable was device fill factor or series resistance. Single cell modules, each with interconnection ribbons and busses connected to the control (soldered) structure and the test (adhesive) structure were used for accurate comparisons. The results are given in the table below.

Table 9: Conductive Adhesive Attachment Results

DOE for Epoxy Joints Cell #	Run number	Epoxy Joint Count per Bus Ribbon	Epoxy Joint Size in mm	Burnished (1 is, 0 not)	Average Delta FF
301…	3	4	1	0	-1.8%
201…	2	4	4	0	-1.1%
601…	6	4	4	0	-0.5%
701…	7	12	4	0	-1.0%
801…	8	4	1	1	-5.8%
101…	1	12	1	1	-2.0%
501…	5	12	1	1	-6.7%
401…	4	12	4	1	-2.4%

The best results were virtually identical to the soldered controls. After further experiments, the best candidates will be subjected to environmental testing.

3.6.3 Cell Breakage Phenomena in PV Modules

As module reliability problems due to cell breakage could become a significant limiting factor in the development of thinner cell, larger cell, and larger module products, it becomes critical to understand cell breakage phenomena in more detail.

Furthermore, recent factory and field data indicates that mechanical/thermal stresses in PV modules may be a significant factor in generating solar cell breakage and accompanying power losses. This appears to be especially true in larger modules with cells, which have suffered damage due to the automated tabbing and stringing equipment during module assembly.

To understand the breakage phenomena better, experiments are under development to evaluate the performance of various module types and sizes under mechanical stresses expected in module shipping/handling, and wind/snow loading, combined with the stresses expected due to thermal cycling. Characterization of the modules is done using IR scanning for broken cells and measurement of power losses before and after stresses have been imposed. This effort is intended to develop a knowledge base for future development work.

Cyclic Wind Load

To simulate multiple wind load cycles, a cycling wind load chamber has been constructed that can alternate positive and negative loads at pressures between 0 and 50 psf. This apparatus effectively allows us to resurrect the older IEEE 1262 cyclic wind load test, which has been abandoned in recent years so is no longer done as part of the module design qualification process.

To date, we have found that significant cell breakage can occur in larger modules when multiple cycles are applied. This breakage does not occur significantly when only a single or a few wind load cycles (as in the IEEE 1215 sequence) are applied. From this we can conclude that there is a fatigue process occurring within the solar cells. When breakage does occur, it is most prevalent near the module center, where the glass deflection is the greatest.

Future work will include analysis of the stresses on the cells during this testing and characterization of the behavior of different cell types under this cycling regime. Empirical data on brittle fracture of materials will be used in this evaluation. Work is also underway to determine the frequency of winds at or above various threshold wind speeds in order to reestablish an appropriate cyclic wind load test standard. Finally, modules stressed using these tests methods will be subjected to thermal cycling to determine if there is interaction between the two stresses in terms of the ultimate power losses expected.

Shipping Damage

Product packaging must meet a set of defined standards in order to be considered acceptable by shipping firms. The most generally accepted set of standards are those defined and maintained by the International Shipping and Transportation Association (ISTA). There are different standards established for different sizes and weights of packaging and different shipping methods. For PV modules, two shipping standards have been identified: ISTA 2D for individually packed modules and ISTA 3E for palletized modules. Both these tests subject the packaged product to significant shock and vibration stresses, with the 2D protocol being significantly more severe than the 3E. BPSolar has been testing and certifying products to the ISTA criteria for several years, but internal damage to cells has not been an evaluation criteria.

Tests have been performed to ISTA 2D for individually packaged products. Cell breakage has been observed due to the shock and vibration experienced in these tests.

Future work will include a set of experiments to determine which portions of the shipping tests cause the cell damage and to evaluate packaging changes that are needed to reduce cell breakage. ISTA 3E will also be performed to quantify any issues with the palletized load packaging.

3.7 In-Line Process Control

In this task, BP Solar is incorporating active feedback from one manufacturing process into the in-line MES system. BP Solar has completed an assessment of crack detection methods for application to very thin wafers.

Crack Detection Summary

Wafer breakage during processing is a very high cost issue. This is particularly true when wafers fail during one of the print steps, generally resulting in several minutes of downtime while the operator cleans up the scattered parts and the wet paste. This is also a source of potential contamination. It is believed that wafers frequently fail at the print steps because they come into the process already cracked and the crack then fails when it is stressed during the process step. Wafer cracks can also cause electrical failure at cell or module test.

During the previous contract, ARRI and BP Solar investigated methods for detecting and rejecting cracked wafers before they are processed. An acceptable method would be able to detect cracked wafers or cells at any stage in the manufacturing process, be non-destructive, and be able to perform a 100% test at planned automation rates in excess of 2000 units per hour. Several potential methods and vendors were identified.

Eddy Current Testing

The potential vendor said they were using eddy currents successfully to detect micro cracks in wafers. Eddy current sensing is fast enough for on-line use and less costly than ultrasonic testing. Samples of good and of damaged solar cells were submitted for eddy current testing. Cracks were detectable in bare wafers, but were not reliably detectable in metallized wafers, as signals from the metal itself dominate the response. This approach was dropped as not viable.

Laser-based Ultrasound

This method is based on using a short laser pulse directed at the wafer to cause a sudden rise in temperature of the wafer material. The temperature rise initiates a sudden but minor expansion of the silicon. The acoustic energy released from the expansion can be used to distinguish between elastic or plastic expansion. The strain energy emitted from the cracks will produce acoustic waves having frequencies characteristic of plastic deformation. The technique is fast enough so it can be implemented on-line, is a non-contact approach and can be described as "low-cost."

Cells were sent to test the feasibility of using this approach. The vendor demonstrated that laser-based ultrasound inspection is a viable method for detection of micro-cracks in wafers. The inspection technique involves the use of two lasers. The first laser scans the wafer in 5-mm increments along the *x* and *y* directions to create localized heating of the wafer, which causes the targeted region to expand, emitting acoustic signals. The acoustic emission is measured by the second laser, which takes the place of contact sensors normally used in acoustic emission sensing.

A third crack detection approach was proposed by another vendor, and a prototype system jointly developed by the vendor and ARRI. The prototype system was tested first at ARRI. Some further development was done to harden the system for extensive testing, and the next round of testing was then done at BPSolar.

While the testing at ARRI was successful in discriminating known cracked wafers from intact ones, the testing at BPSolar revealed some issues with calibration and repeatability. Further development was then undertaken by the prospective vendor and the system demonstrated again at their site.

Between the second and the third trials, the vendor had reengineered the detection method considerably. The resulting prototype appeared, in principle, to be more robust and potentially less prone to calibration drift and external noise than the original concept machine.

During the development period, BPSolar had placed orders for various pieces of automated handling equipment for several cell lines. The initial concept for the wafer crack detection system was that it would be integrated with these and similar automated handling systems in order to provide real-time feedback on wafer breakage. Two issues emerged during the wafer crack system development. First, it was not clear that the system, as finally conceived, could be small and light enough to integrate into the handling tools of our automated handling systems. Second, the vendors of these automated handling systems were willing to guarantee such low rates of breakage that the value of in-line wafer crack detection would be much diminished.

Development work was therefore halted after demonstration of the new prototype at the vendor. The detection method appears feasible on a laboratory scale, and it may be useful to purchase a similar unit for experimental-scale work in the future. However, it appears unlikely that the method will prove useful for in-line use in high-volume manufacturing.

MDCS Summary

In late 2002, work was done to finalize the introduction of the MDCS (Manufacturing Data Collection System) on the Assembly line. This completed the rollout of the MDCS system throughout the manufacturing lines in Frederick

An initiative was begun to improve control of yields in the saw area. The team working on this issue identified a need to collect sawing parameters in real time as an aid in identifying conditions that lead to wire breaks during the sawing process. The newer saws collect a large amount of process data during each run, but the data is stored locally on the machine and is difficult to access at all, let alone in real time.

The team reconfigured several machines to facilitate downloading the run data, and are presently collecting run data to determine if there are data signatures that occur in advance of a wire break. If so, the team intends to configure a saw so that the data is monitored by the MES system in real time in order to provide pro-active indications of run conditions that may be leading up to a wire break, thereby allowing intervention prior to a break occurring.

In addition, a series of designed experiments were run to determine the effect of several key process parameters on saw performance. The results of these experiments were used to determine both the optimal run conditions and the parameters we wish to monitor in-line in the future. The result of this work was a reduction by over a factor of two in the incidence of "problem" runs on three specific saws.

The MDCS system now reports saw data in real time to a large-screen display in the saw room. Results are displayed for the present shift, previous shift, previous day, and then charted for the previous 30 days and 90 days, with trend lines applied.

A similar exercise is now underway in the cell line. To date, the process team has identified several areas in which the MDCS system can be used to provide real time process data display and analysis.

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13. ABSTRACT (Maximum 200 words): The goal of BP Solar's Crystalline PVMaT program is to improve the present polycrystalline silicon manufacturing facility to reduce cost, improve efficiency, and increase production capacity. Key components of the program are: increasing ingot size; improving ingot material quality; improving material handling; developing wire saws to slice 100-μm-thick silicon wafers on 200-μm centers; developing equipment for demounting and subsequent handling of very thin silicon wafers; developing cell processes using 100-μm-thick silicon wafers that produce encapsulated cells with efficiencies of at least 15.4% at an overall yield exceeding 95%; expanding existing in-line manufacturing data reporting systems to provide active process control; establishing a 50 MW (annual nominal capacity) green-field Mega plant factory model template based on this new thin polycrystalline silicon technology; and facilitating an increase in the silicon feedstock industry's production capacity for lower-cost solar-grade silicon feedstock.

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