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Subcontractor Report

Lab to Large Scale Transition for Non-Vacuum Thin Film CIGS Solar Cells

Phase I Annual Technical Report
1 August 2002–31 July 2003

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1.0 BACKGROUND

The purpose of the Thin-Film Photovoltaics Partnership Program (TFPPP) is to accelerate the progress of thin film solar cells and module development as well as to address mid and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust modules of 15% aperture-area efficiency. Furthermore, this research is directed at making progress toward this objective by achieving interim goals in thin film module efficiencies; cell and module processing; cell and module reliability and the necessary fundamental research needed to build the technology base that support these key areas. Participation in the National R&D Teams is paramount to the success of this project. The DOE/NREL/NCPV strategy in undertaking this R&D effort is to maintain the good coupling between laboratory results from fundamental materials and processes research to manufacturing R&D, pilot-line operation, and early entry of advanced thin-film PV products to the ever-growing marketplace worldwide.

The purpose of this subcontract, as part of the R&D Partners category is to, (i) identify the challenges that ISET may face in the process of making a 'Lab to Large Scale' transition for its ink based non-vacuum process in production of thin film CIGS solar cells and modules, (ii) develop workable solutions for these challenges such that they can readily be implemented in a large-scale processing line for CIGS modules.

1.1 INTRODUCTION

The primary objective of this research is to streamline ISET's ink based non-vacuum process for fabricating efficient CIGS modules at a lower cost of module production of << $1.0/watt. To achieve this objective, ISET focuses R&D efforts on investigating topics that directly impact the ultimate cost of processing CIGS modules. These topics of concern include (i) module output and therefore the solar cell and the module efficiency, (ii) overall process yield – which requires developing a process that offers a very high degree of repeatability for every manufacturing step, and finally (iii) a process approach that maximizes the utilization of the materials used.

In accordance with the above, this report will cover activity during Phase I in the investigation of methods for low-cost manufacturing and process development. Specific tasks cover four broad areas: (1) solar cell efficiency (2) process control (3) module integration and (4) enhanced material utilization by recycling unused materials.

Table I . Overview of Phase One Tasks

1	Solar Cell Efficiency Improvement	This is the primary task of the contract. In this task we aim to improve the efficiency of the CIGS solar cells by grading the composition of the absorber layer by surface modification to achieve gallium rich wider bandgap layers near the photoactive junction. This approach will increase the cell efficiency by increasing the open circuit voltage.
2	Process Improvement and Control	This task will aim to develop an insight into the kinetics of reduction and selenization steps of ISET's non-vacuum process. Data will be collected with the goal of improving the process conditions and designing reduction and selenization furnaces capable of processing larger area substrates.
3	Module Integration	This task will evaluate issues unique to module formation. Monolithic integration schemes using the 'orthogonal scribe' approach will be developed and optimized. Different inks and printing techniques will be evaluated for front contact deposition.
4	Recycling	This task will be to increase material's usage and to minimize waste. This task will have significant cost and environmental impact.

1.2 CELL EFFICIENCY IMPROVEMENT BY SURFACE MODIFICATION

Photovoltaic module output is determined by the cell efficiency. We focus on increasing the open-circuit voltage and the overall conversion efficiency by modifying CIGS solar cells using an overall non-vacuum approach.

Building on our current ink based fabrication methods, we turn our attention to producing graded layers of the $Cu(In,Ga)Se_2$ solar cell absorber by surface modification at the junction interface. The objective is to grade the solar cell absorber layer via gallium surface treatments. Briefly, gallium alloying makes it easier to produce higher open-circuit voltages and when spiked in atomic ratios of Ga/(In+Ga) of 25% to 30%, groups worldwide using vacuum techniques have been able to produce solar cell efficiencies approaching 20% (effective bandgap 1.1 – 1.2 eV).

1.2.1 Current Problems in Gallium Distribution

It is well known that the addition of gallium to the CIS structure opens up the bandgap and increases the V_{OC} of the resulting cell. At ISET, past efficiency and spectral response results had indicated that in spite of adding Ga to the absorber layer, we were not getting the full benefit of it in increasing the open circuit voltage. SIMS measurements on our samples had indicated that during the conversion process in which the Cu-In-Ga alloy was converted to CIGS, the gallium is accumulating at the rear of the absorber layer nearing the Mo interface (Figure 1) due to the kinetics of the selenization step. Consequently, controlled stoichiometries, which introduce gallium *nearly molecularly* in our ink based deposition appears to be ineffectual at opening up the bandgap of the semiconductor. We are countering the problem of gallium depth-distribution by exploring modification routes. Gallium surface treatments will help us achieve higher cell efficiencies by opening up the material bandgap from otherwise CIS-type laboratory cells during the selenization of nanoparticle metal alloy precursors.

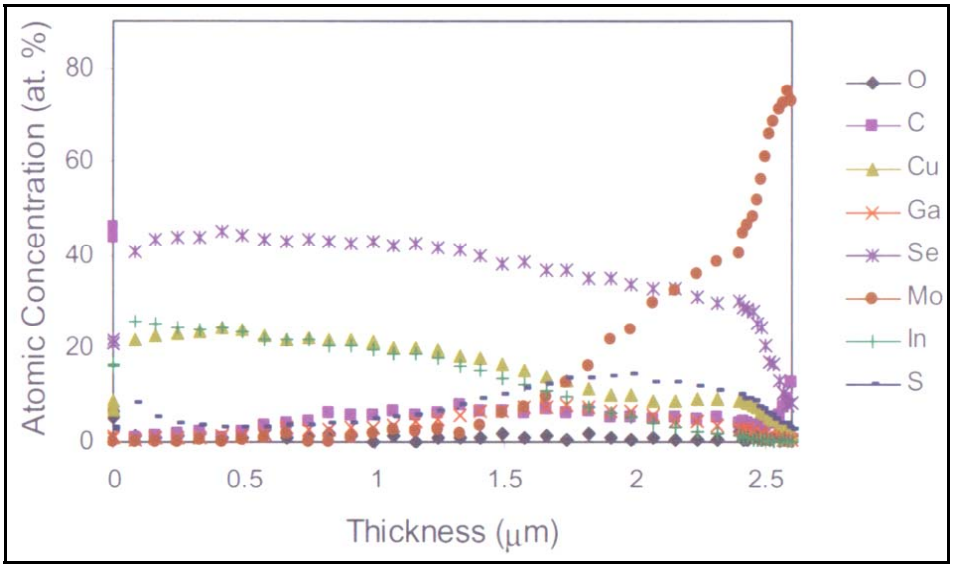

Figure 1. SIMS Depth profile of a CIGS Absorber layer using ISET's ink-based processing scheme involving selenization of nanoparticle precursors.

1.2.2 Surface Modification – Method Development

The general strategy is to form a gallium containing interlayer over the base solar cell material. Through film annealing and gas-solid exchange, we take one of two routes for absorber modification. From the first strategy outlined in Figure 2, we modify an existing selenized film with a very thin coating of a gallium compound and subsequently drive Ga into the lattice at high temperature (as limited by the glass substrate). The second strategy is to modify a film of the reduced metal alloy with a thin layer of a gallium compound prior to carrying out selenization; both

attempts aim to lock-in gallium in the chalcopyrite structure in the near surface region below the junction interface.

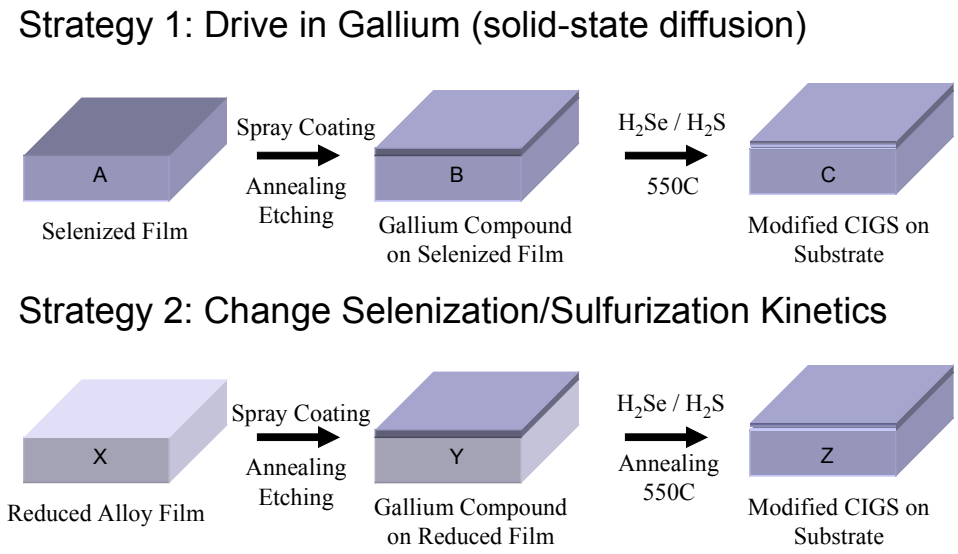

Figure 2. Method Development for surface modification from two distinct routes.

The key challenges in method development for the thin film deposition and growth processing scheme are as follows:

- Developing the modification step
  - Identify a compatible film deposition scheme for a gallium containing interlayer
  - Optimize coating parameters to uniformly deposit an interlayer of a working thickness
  - Identify an annealing treatment for film growth
- Forming the modified chalcopyrite
  - Identify processing parameters (e.g. temperature, time, ambient conditions) to incorporate gallium in the modified absorber
  - Develop the necessary etching procedure to remove unincorporated, extraneous material at the surface
  - Ensure compatibility with the remaining processing steps (CdS by chemical bath and ZnO by CVD) for device fabrication

1.2.3 The Modification Step: Depositing a gallium interlayer

Benefiting from ISET's patented expertise in ink formulation and coating technologies, chemists at ISET developed the necessary ink formulation and dispersion technologies to deposit a host of alternate inorganic coating materials. From the standpoint of ink preparations, the *aqueous* system is limited to dispersion of metal oxides and/or dissolution of metal salts (e.g. chlorides, nitrates and hydroxides). We added additional know-how in *non-aqueous* media to effectively disperse gallium compounds in solvent-based vehicles.

Use of organic solvents also added further capability in dispersing binary and ternary mixtures of copper-indium-gallium alloy metal powders, pure elemental sulfur and selenium powders, allowing us to coat any of a number of inorganic materials with relatively little in the way of capital equipment requirements.

These **ink suspensions** and **solution-based** deposition schemes for the gallium interlayer paved the way for bringing in gallium at the top by non-vacuum approaches.

In the period between April-May 2003, we identified solution-based techniques for depositing gallium thin films by spray deposition onto a variety of substrates. These films are visibly smooth and tenacious (on the order of tens of nm film thickness). This activity led us to a novel low-temperature synthesis of appropriate gallium compounds in solution involving gallium complexes with sulfur in solution. While we were also able to synthesize what appear to be ternary and quaternary compounds of interest, we restricted our attention to optimizing our newly established process for forming thin layers of specific Group III compounds. This new method became our most promising method as a nanostructured coating material for surface modification.

Two complementary surface modification approaches were used to deposit a gallium interlayer. In the first approach, the Cu-In-Ga alloy surface was modified with a Ga source and the sample was selenized under H_2Se to form the modified chalcopyrite film. The rationale behind this approach was that the gallium bound in the compound form at the surface would be inhibited from accumulating at the rear of the absorber layer (as in our standard process) and would be incorporated into the chalcopyrite lattice in the front during selenization. The second approach involved Ga introduction into a preformed chalcopyrite lattice layer by surface treatment followed by annealing. Both approaches were evaluated in parallel during phase I.

1.2.4 Modified chalcopyrite Formation: the Gallium 'Drive-In'

Our attempts to modify selenized films using inks of specific gallium compounds successfully coated the samples with a gallium interlayer, but did not fall into a working thickness range for gallium incorporation and as of the time of this report process conditions have not yet been optimized.

Efforts with our solution-based gallium deposition scheme have delivered some promise in our quest for achieving higher open-circuit voltages by surface treatment. In this method, we start with clear, colorless solutions containing a gallium and sulfur source which are sprayed onto the preformed chalcopyrite layer followed by annealing. We avoid problems of extensive hydrolysis of Ga (III) salts in solution by (i) inducing metal-sulfur complexation in a non-aqueous system followed by (ii) rapid solvent bakeout and thermal decomposition to yield the gallium containing surface layer. We empirically determined temperature-time processing parameters on which clear coated films convert to leave behind a continuous, very thin chalcogenide film. Elemental analysis by X-ray fluorescence in Figure 3 confirms the deposition of gallium and sulfur on our base chalcopyrite material.

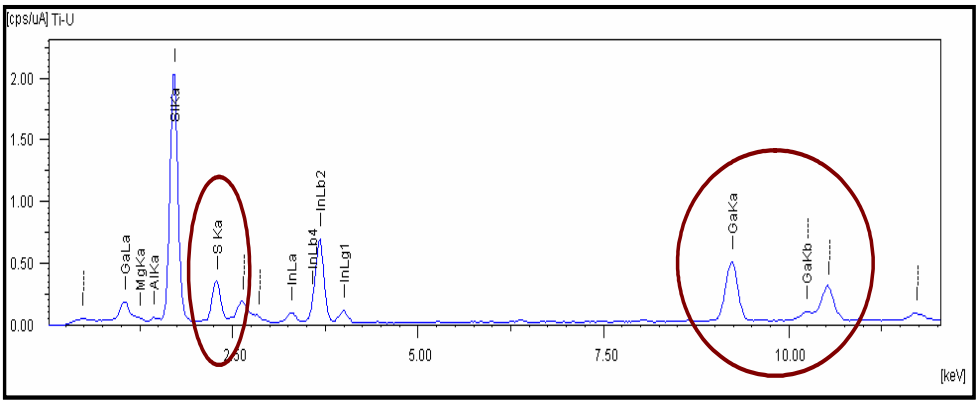

Figure 3. Deposition of gallium and sulfur by surface modification from a novel solution based coating scheme

After fluorescence data upheld our reaction pathway to a gallium interlayer, a thermal analysis scan of our coating solution validated our film-forming annealing treatment which occurs below 300°C. Next, after several rounds of optimizing air-assisted spray coating conditions, we were able to define a set of modification parameters that successfully spiked our films with gallium in just the right range of atomic ratios without degrading the performance of the solar cells relative to sister control samples.

1.2.5 Surface Modification and V_{OC} Enhancement

Once a feasible modification route was defined, we attempted to drive gallium into the lattice chalcopyrite structure. These experiments were carried out at high temperatures between 500-550°C under several ambient conditions including vacuum, inert gas and reactive hydrogen selenide gas. After modifying the surface, a series of single-step annealing experiments under inert ambients showed that we were successful in externally depositing several hundred angstroms of a gallium source in the modified film without causing major losses in current (J_{SC}~30-35 mA/cm^2). This indicated that we had defined a working interlayer thickness range for surface modification.

Despite achieving respectable currents after modification, device efficiencies suffered primarily due to losses in fill factor. We observed selenium deposits on the exhaust of our quartz annealing tubes which signaled that some compensation for the Se loss would likely be necessary if we stood any chance at seeing an increase in the open circuit voltage coming from the external source of gallium.

We introduced a dual-step annealing treatment for the modified chalcopyrite film growth using a small amount of hydrogen selenide gas at the higher temperature. The gallium compound that was deposited at the lower temperature is driven in-situ into the lattice into the absorber layer by solid-state diffusion when heated in hydrogen selenide gas. The result was a first statistically significant Voc jump relative to a control sample representing a voltage increase in the range of **+70-130mV**. As we saw improvement in the cell voltages, currents and fill factors began to suffer.

Our next point of attack is to develop the necessary etching procedure prior to the junction formation. Our thinking is that etching should be necessary to rid the surface of unincorporated material at the surface after modification such as any excess Ga_2S_3, Ga_2Se_3 and/or $CuGaSe_2$ that may be forming at the near surface. We expect that in combination with the established modification route which is producing enhanced open circuit voltages, etching prior to junction formation will assist in stabilizing the current and FF in the devices. We are currently exploring chemical etchants that will prepare a pristine surface after modification. To date, our CIGS surface modification strategy has produced a Voc enhancement of 572mV from a control sample of 450mV which tells us that we are on our way to getting the benefit of gallium in the device. Under the processing conditions employed, the Jsc and FF of these samples have been somewhat lower, resulting in lower overall efficiency. Currently we are optimizing the processing and etching conditions to maintain this high V_{OC} on optimized samples fabricated in our research furnaces.

1.3 PROCESS IMPROVEMENT, CONTROL & RECYCLING ISSUES

In parallel with surface modification experiments, we concentrated efforts on optimizing reduction and selenization steps for process scale-up. By investigating reaction kinetics under our goal of large-scale production, we were able to make changes which have led to both a larger size and quantity of high efficiency solar cells. Our efforts directly impact process throughput and yield capability.

1.3.1 Process Transfer to Large-Area Production Furnaces

During the 2001-2002 timeframe, ISET set up large tube furnaces with the capability of processing large area substrates as large as 5"x 36." These production furnaces became operational in early 2002. We subsequently concentrated our efforts on transferring our existing process from our small research furnaces to the large production furnaces. This involved the optimization of time and temperature conditions for reducing the oxides to alloys and selenizing those alloys to form the CIGS solar cell absorber. We are also optimizing sample size and loading configuration of coated samples to effectively maximize the throughput area in the large furnaces. Currently, coated substrates of typical size 4"x 12" are routinely reduced in the large furnace. Elemental analysis of reduced films by X-ray fluorescence (XRF) confirms good compositional mapping over the larger area processing. Results for the bulk compositions are shown in Figure 4.

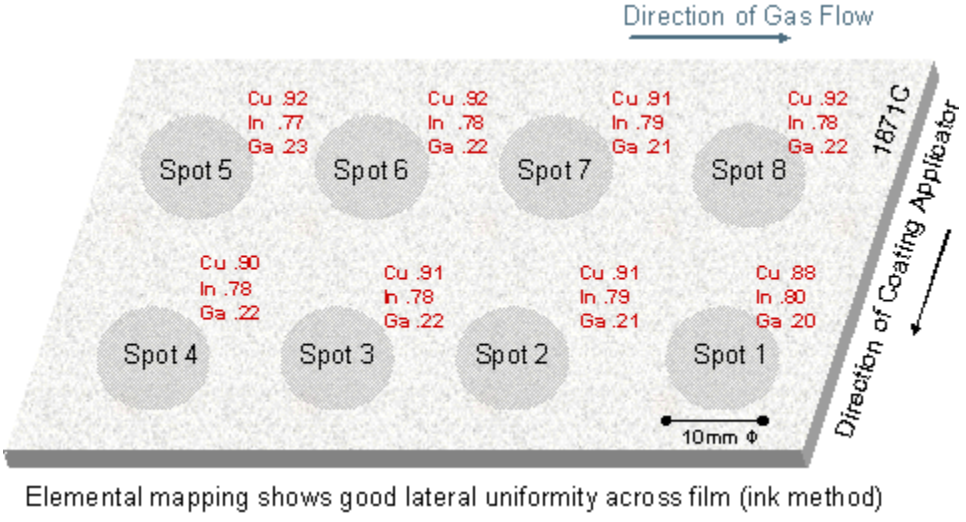

Figure 4. XRF Elemental analysis mapping of a reduced alloy film

With the first set of large reduction and selenization furnaces now in operation, we turned our attention to setting up a second set of production furnaces. As of the time of this report, the second large reduction furnace is operational and qualified while the second selenization furnace is near

operational status. A late stage addition of cooling fans to both sets of production furnaces also increases our throughput due to shortened processing times.

Currently, reduced and selenized samples are processed individually in the middle of the furnace hot zone, on quartz base plates. To increase the amount of cells processed per reduction and selenization runs, a quartz 'boat' was designed to accommodate a larger number of samples per run. The challenge with using these quartz holders has been achieving the level of uniformity that has been optimized in the small research furnaces. Knowledge gained from scaled-up processing in these large furnaces will be essential to designing larger capacity systems, which is a prime goal of this 'lab to large scale' transition effort. If successful, these hardware changes in conjunction with our overall process improvement will increase ISET's installed capacity to well over 50 kW/yr.

1.3.2 Process Improvement and Control in Reduction

To develop insight into the kinetics of the reduction process for achieving complete reduction of nanoparticle oxides with the objective of designing a large scale reduction furnace.

The acquisition of a DTG thermal analyzer (Shimadzu, Japan) was used to help us understand the kinetics of the metal oxide reduction process. With information on the reduction profiles of the individual Cu-In-Ga oxides, the temperature ramp and soak profile was tailored to simulate individual oxide reductions, as well as exothermic aided reductions. Our thermal data led to a change in the way the mixed oxide film is heated during the reduction profile. Employed in the large area reduction furnace, these new profiles produced devices with efficiencies exceeding 12.0% under simulated AM 1.5 illumination.

Figure 5 illustrates an I-V curve for a solar cell fabricated in the large area reduction furnace while still carrying out selenization in the small research selenization furnace as a control.

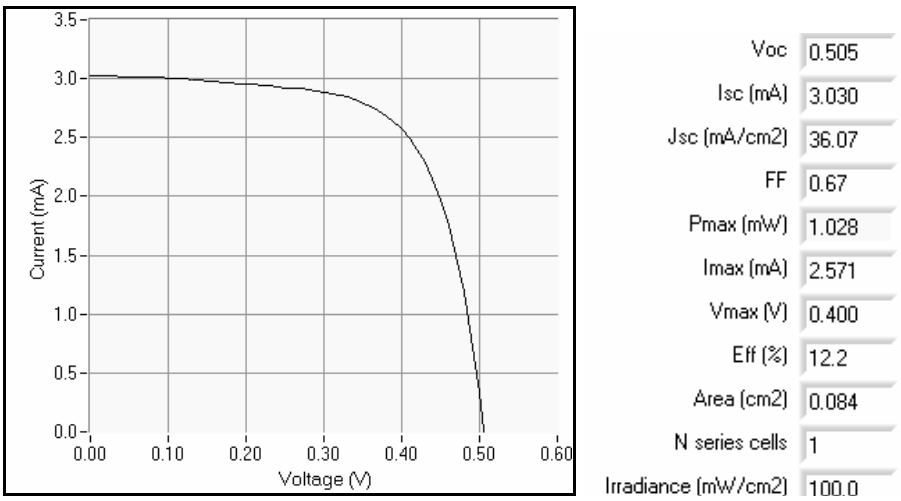

Figure 5. I-V curve of a CIGS solar cell produced in the large area reduction furnace and selenized in a small research furnace. Sample is tested under AM1.5 illumination.

Several process control issues arose during the initial testing of the large area reduction furnace. The increased size and capacity of the large furnace increases the probability for leaks. It is well known that during the reduction of metal oxides to their respective alloys, the reaction is sensitive to trace amounts of oxygen or oxygen bearing vapor/gas phase impurities.

With this sensitivity in mind, an *oxygen trap* was added to the hydrogen and nitrogen gas inlet manifold. Additionally, a moisture detector was added as an in-line process monitor to detect the presence and quantity of H_2O in the tube during reduction runs. These issues ultimately led to a design of a recirculation system. This system is designed to re-circulate the internal gases, while siphoning out both H_2O and oxygen. The gas within the tube furnace is fed through a liquid nitrogen cold trap, which freezes passing H_2O molecules. The gas is then fed through a moisture/oxygen trap, and then fed back into the tube furnace at a high rate. The high speed movement of gas increases the rate and degree of reduction of the Cu-In-Ga oxide films and it may allow us to process a large number of substrates simultaneously. A schematic of the recirculation system is shown in Figure 5 which illustrates the above mentioned improvements in process design in the large area reduction furnace.

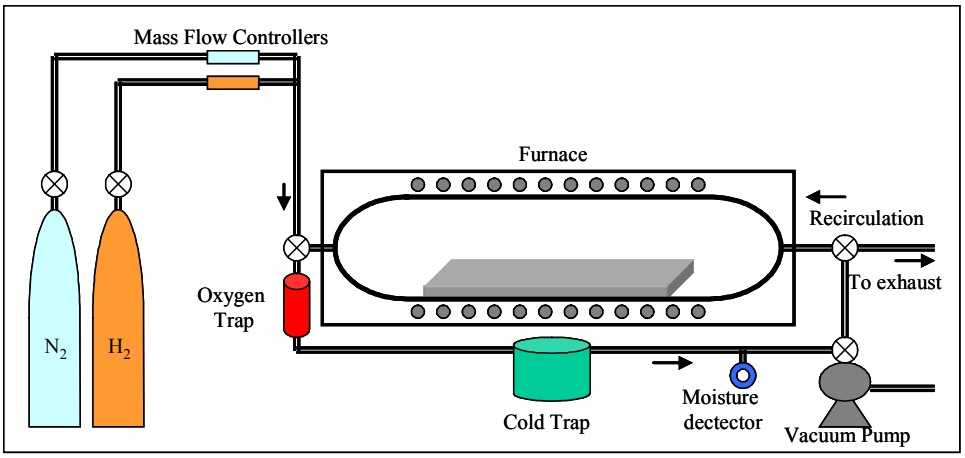

Figure 6. Schematic of recirculation system in the large area reduction furnace.

1.3.3 Process Improvement and Control in Selenization

To develop insight into the kinetics of the selenization process of metal alloy precursors with the objective of designing a large scale selenization furnace.

Efforts for process improvement are also underway to define process conditions in the large area selenization furnaces. Due to slightly different constructions of the small research furnace compared to the large area production furnaces, the existing temperature-time profiles needed to be altered to achieve high efficiency CIGS solar cells.

As of late 2002, the selenization process on reduced films was done under flowing H_2Se gas. This process was extremely wasteful, as less than 1% of the H_2Se that flowed over the sample during the reaction was used in the gas-solid conversion. Specific issues with sample non-uniformity during selenization arose when the gas flux was not uniform over the surface of the sample. Being mindful of specific tasks outlined in phase one of this project, we switched from selenization under flowing conditions to static conditions, thereby minimizing H2Se gas waste. Selenization is now carried out in a heated chamber filled with a known concentration of H_2Se without any gas flow. In addition to minimizing unnecessary waste of H_2Se, the static process results in more uniform samples after selenization. The change to static conditions is a process improvement that has also opened the door to using a high-capacity sample holder for increasing throughput. Currently, optimization of selenization conditions is underway to successfully carry out the selenization conversion using a rack holder for processing multiple substrates simultaneously. Additionally, we have discovered that selenization in a sub-atmospheric ambient using static H_2Se gas mixtures have produced high efficiency devices in the large area furnaces. Figure 7 illustrates an I-V curve for a solar cell fabricated in both

of the large area reduction and selenization furnaces under optimized static selenization conditions.

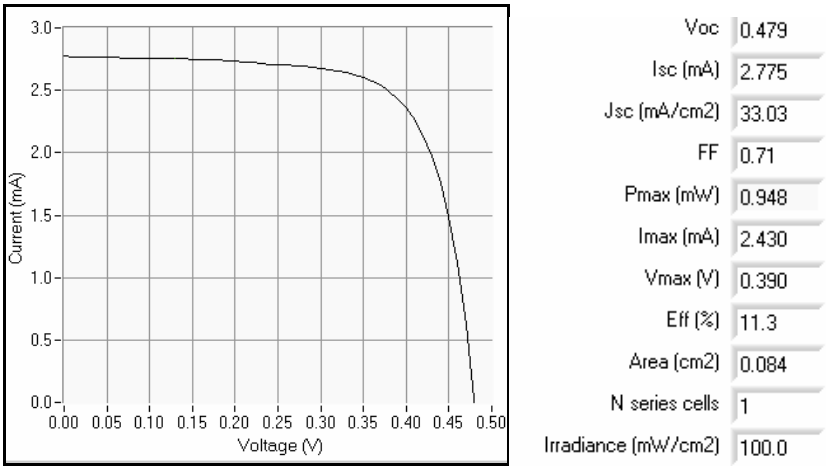

Figure 7. I-V curve of a CIGS solar cell produced in the large area reduction and selenization furnaces. Sample is tested under AM1.5 illumination.

With both of the large area furnaces qualified to yield efficient devices, the next step in our scale-up was to minimize H_2Se gas usage by recycling unused hydrogen selenide gas. Figure 8 illustrates a schematic for a H_2Se recycling system that was added to the existing large area furnace setup. In this configuration, the total unused hydrogen selenide, which has been cut down under static conditions, can be trapped and reused.

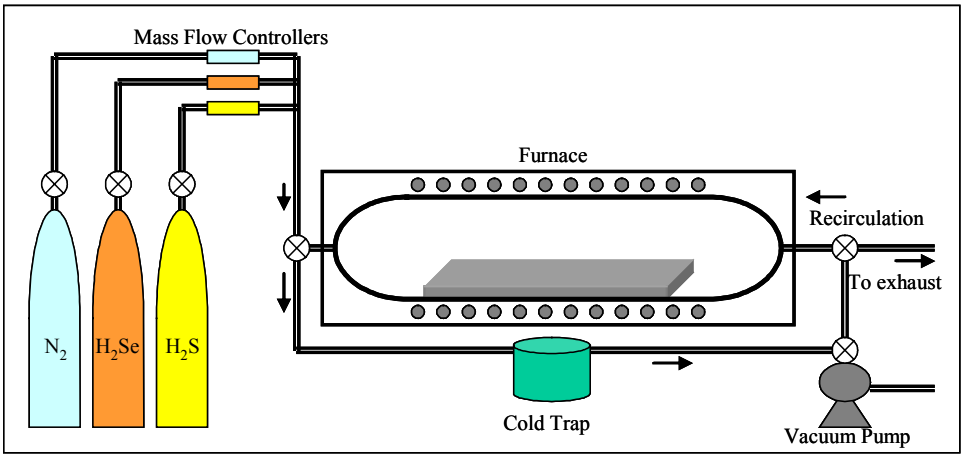

Figure 8. Schematic of recirculation system in the large area selenization furnace.

The static approach to selenization was further explored by adding post-sulfurization using hydrogen sulfide gas to the selenization routine.

Changes were made in the time, temperature and reactant concentrations throughout various parts of this step, enabling an improvement in device efficiency. Figure 9 shows an I-V curve for a solar cell fabricated which was reduced in the large area reduction furnace, followed by an optimized selenization/sulfurization profile in the large area selenization furnace.

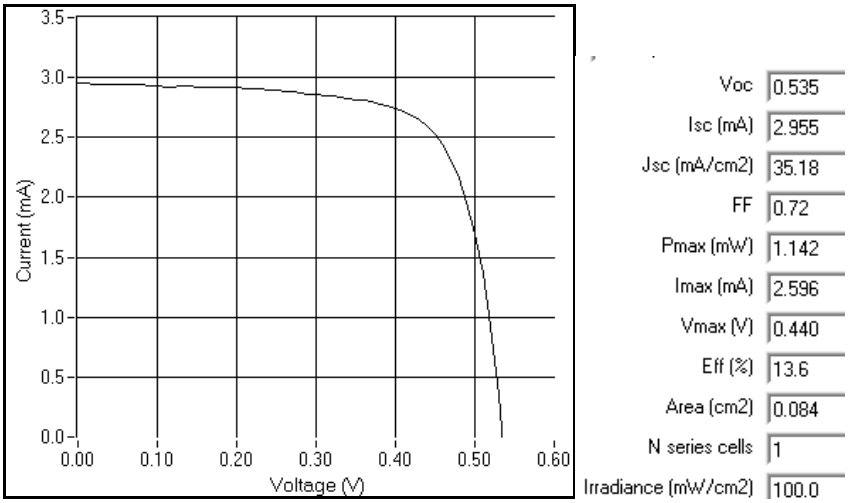

Figure 9. I-V curve of a CIGSS solar cell produced in the large area furnaces with optimized selenization/sulfurization profile. Sample is tested under AM1.5 illumination.

1.4 MODULE INTEGRATION

Monolithic integration of individual solar cells to form modules is a challenge that is not present in lab scale cell fabrication, but is unique and essential to large scale manufacturing. Hence in our current effort to address issues related to 'lab to large scale' transition of ISET's CIGS technology, addressing this aspect has been given high priority.

1.4.1 Depositing Top Contacts

During Phase I, our goal was to identify non vacuum methods for depositing top contacts on fabricated CIGS solar cells. Initially we decided to use screen printing to deposit the top contacts. The primary focus of this effort was to identify an appropriate conducting ink that could be screen printed onto the window layer to form the top contact for the module integration. Unlike silicon, top contacts on CIGS solar cells cannot be processed above 200°C as that will destroy the photoactive junction. This implies that the inks must be polymer/epoxy-based and must be curable below 200°C. In addition to our temperature limitation, a successful ink should meet two criteria. First, it should exhibit minimal contact resistance in contact with the TCO layer. Second, it should have

minimal resistive losses for current conduction within the silver grid pattern.

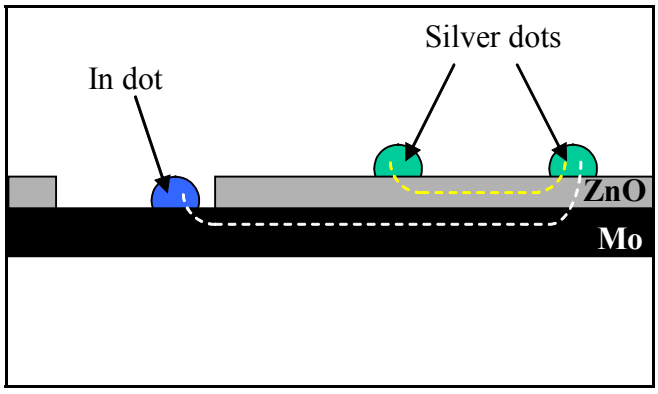

Figure 10. Schematic of a 'dot test' for evaluation of contact resistance between the ink and the ZnO layer.

Specifications of commercial products list bulk and/or sheet resistivity which strictly pertains only to the second criteria above. Therefore to test the contact resistance of these inks with ISET's TCO, several vendors of commercial screen printable silver inks were contacted and samples were procured for testing.

Figure 10 shows a schematic of the samples prepared for testing contact resistance. A ZnO layer was coated onto a metallized Mo coated glass substrate. Dots of silver ink were placed on the Zinc Oxide layer and cured per specification schedule provided by the manufacturers. An indium dot was placed on the exposed Mo section to simulate the back contact in a typical cell. Resistances were measured between silver dots and also between silver dots and the indium dot.

Thin dotted lines in Figure 10 show the most likely current path during the 'dot tests.' In the above configuration the Mo layer and the In/Mo interface are highly conducting and the ZnO layer is also very conducting. The Mo/ZnO interface should also exhibit minimal resistance and in any case, is factored out when comparing samples with dots on similarly prepared substrates. Therefore, any measured resistance derives primarily from the resistance of the junction between the silver dot and the ZnO.

Figure 11 shows the results of contact resistance measurements with inks from several different vendors. The data point at Ink 0 actually represents the resistance measured on a sample prepared by evaporating silver dots by e-beam evaporation in a configuration similar to the ink dot samples. This data are provided for comparison purposes.

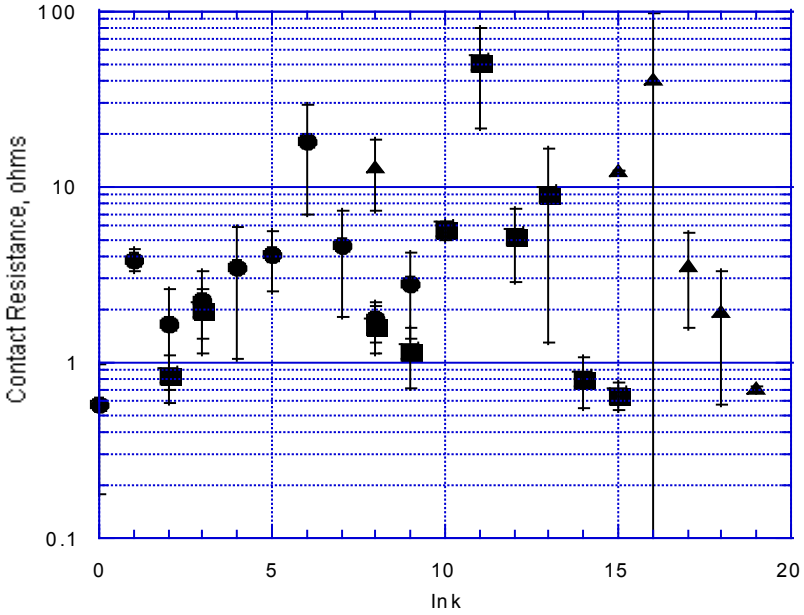

Figure 11. Results of contact resistance measurements ('dot tests') on several different screen-printable silver inks on ISET's ZnO.

The above data indicates that even though these inks have been cured at temperatures below 200°C, for several of them, their contact resistance is within an order of magnitude from industry standards.

Subsequent to dot tests, those inks that displayed the lowest contact resistance were screen printed onto CIGS solar cells made on flexible moly foils. These cells had a total area of approximately 15 cm^2. Smaller test cells that did not require top contacts (that is, where the top TCO conductivity was sufficiently high) were also scribed near the large cell for comparative evaluation. Figure 11 shows the I-V curves of a typical small and large cell. The small cell data is without the silver grid where the large cell was measured with the screen printed top silver grid.

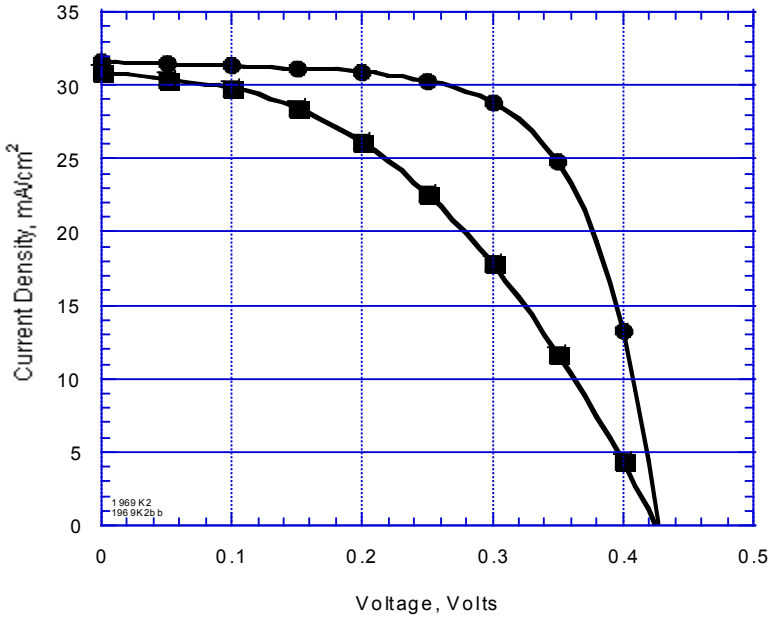

Figure 12. I-V curve of a large area cell (squares) and a small area cell (dots). The areas are large cell: 15.3 cm^2 and small cell: 0.084 cm^2.

As seen in Figure 12, the V_{OC} and the J_{SC} are similar for both cells. The overall efficiency of the larger cell is lower than that of the smaller cell because it has a lower fill factor. The fill factor is lower due to the greater series resistance due to the contacts in the larger cell as compared to the smaller cell where the current collection is over a smaller area directly through the top TCO. Similar results have been obtained with inks purchased from several vendors. Currently talks are underway with the technical personnel of these vendors to identify ways to further reduce the contact resistance. Options being explored include doping, optimizing the rheology and composition of the inks, identifying methods of preparing the surface before contact deposition and determining optimal curing conditions for the contacts. Further reduction of contact resistance along with the "orthogonal scribe" approach will be the focus of this task in Phase II and III for module integration.

1.5 FUTURE TASKS

Continuing research efforts will focus on building up main tasks outlined in this report. We will focus on surface modification strategies to improve the solar cell efficiency by increasing open-circuit voltages to achieve 15% cell efficiency. We will push to make CIGS solar cells with screen-printed contacts and carry over the process to produce monolithically integrated modules with printed contacts.

1.6 PHASE I SUMMARY

The overall philosophy of this work is to carry out R & D in areas that directly impact the cost of production of modules in a manufacturing plant such as module power output i.e. watts/ft^2, overall process yield and materials utilization. To make the non-vacuum process suitable for large scale production, we address key issues in a complete module fabrication process and collect the necessary data so that the *Lab to Production* transition will be made with no surprises. The data and information collected will be used to design scaled up process equipment for large volume production.

Focus on Efficiency

The main focus presented for improving the cell efficiency is to perform the composition gradation on the surface of CIGS absorber layers such that there are Ga rich regions in the front near the junction coming from surface treatments. This Ga profile in the absorber layer may be able to take advantage of both a back surface field reflector (from our selenization scheme) for better current collection and at the same time higher V_{oc}'s from gallium rich regions near the junction resulting in higher efficiency solar cells.

In the first year we evaluated various approaches for gallium surface treatments and narrowed the field to identify a suitable approach for adaptation into a large scale manufacturing of CIGS modules. We have already demonstrated higher cell voltages by surface treatment, and are developing a more elaborate and defined process for surface modification that will take us to our goal of 15% at the cell level. We will continue improving the efficiency of solar cells throughout the entire duration of this contract by way of surface treatments.

Focus on Process Improvement, Control and Recycling

We have initiated kinetics and engineering studies of the reduction and selenization process, effects of temperature, pressure and gas flow regimes leading to a design of production furnaces suitable for processing large area substrates. We have brought online these new larger capacity furnaces, and have transferred our process with optimized profiles to produce high efficiency solar cells using our nanoparticle, ink-based fabrication scheme. Our new larger-capacity design includes the development of a recirculation system for the recycling of gases; sensors, detectors and traps for process control. Our efforts directly impact process throughput and yield capability with higher materials' utilization. We were able to make changes which have led to both a larger size and quantity of high efficiency solar cells.

Focus on Monolithically Integrated Modules

The major challenge lies in finding proper conducting and insulating inks that could be screen printed with the kind of precision that we will need for monolithic integration of modules with *printed* contacts. We identified several commercially-

available inks and are in the process of lowering the contact resistance for monolithic integration that will be the focus of Phase II and III of this contract.

PUBLICATIONS

V. K. Kapur, A. Bansal, P. Le, O. Asensio and N. Shigeoka "Non-Vacuum Processing of CIGS Solar Cells on Flexible Polymer Substrates" Third World Conference on Photovoltaic Energy Conversion Conference Proceedings, Osaka, Japan (2003) in press

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13. ABSTRACT *(Maximum 200 words):* The purpose of this subcontract is to (1) identify the challenges that ISET may face in the process of making a "Lab to Large-Scale" transition for its ink-based non-vacuum process in production of thin-film CIGS solar cells and modules, and (2) develop workable solutions for these challenges such that they can readily be implemented in a large-scale processing line for CIGS modules. The primary objective of this research is to streamline ISET's ink-based non-vacuum process for fabricating efficient CIGS modules at a lower cost of module production of < $1.0/watt. To achieve this objective, ISET focuses R&D efforts on investigating topics that directly impact the ultimate cost of processing CIGS modules. These topics include (i) module output, and therefore, the solar cell and module efficiency, (ii) overall process yield, which requires developing a process that offers a very high degree of repeatability for every manufacturing step, and finally (iii) a process approach that maximizes the utilization of the materials used. In accordance with the above, this report will cover activity during Phase I in the investigation of methods for low-cost manufacturing and process development. Specific tasks cover four broad areas: (1) solar cell efficiency, (2) process control, (3) module integration, and (4) enhanced material utilization by recycling unused materials.

14. SUBJECT TERMS: PV; thin film; solar cell efficiency; non-vacuum process; module; low-cost manufacturing; process control; module integration; enhanced material utilization; chalcopyrite; Cu(In,Ga)Se_2 (CIGS); solid-state diffusion;

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