Advanced Processing of CdTe- and $CuIn_{1-x}Ga_xSe_2$-Based Solar Cells

Final Technical Report
26 May 1998—22 December 2001

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Part I – CdTe

EXECUTIVE SUMMARY

The main task areas addressed by the "CdTe Component" of this project are:
- development of alternative transparent conducting oxides and window layers
- development of simplified processing for the fabrication of CdTe solar cells
- studies of the long term stability of CdTe devices
- development of back contacts/back contact processing methods.

All of the above issues are critical to CdTe technology and offer the opportunity to combine the key aspects of the technology in an attempt to improve our understanding of the CdTe/CdS solar cell. The ultimate goal is the development of a manufacturing friendly technology capable of producing efficient and stable CdTe cells.

During the first two years of this project we reported on the performance of CdTe solar cells fabricated entirely by the CSS process (CdS and CdTe) at temperatures as low as 480°C. Solar cells are now routinely being fabricated in two temperature ranges: (a) 580-620°C and (b) 540-560°C. These conditions were chosen based on performance and reproducibility criteria. Commercial soda lime glass substrates are also routinely being processed, in addition to the borosilicate substrates that continue to serve as "baseline" substrates.

Work on an "all-dry" processing schemes has continued with emphasis being placed on the development of a high throughput vapor-based $CdCl_2$ heat treatment. During the last year of this project the robustness of this process was improved, primarily through increased process control. Considerable progress has been made toward reducing the process time for this heat treatment, with reasonable performance levels.

Long term stability studies have focused on temperature stressing of CdTe cells fabricated using the baseline process, which includes a copper-based back contact (HgTe:Cu powder mixed in graphite paste). This report summarizes the results of this stress experiment, during which all cells were stressed for approximately 3600 hours at temperatures as high as 120°C in a controlled ambient (He).

Work on developing Cu-free back contact options has continued. It has been previously reported that Ni_2P-based back contacts have produced encouraging results. Work on this contact continued and Ni2P-contacted cells were also light soaked for 1330 hours to determine their stability. Some limted work was also carried on the sputtered Sb_2Te_3 option. In general, this approach has not produced the anticipated results obtained by others.

Work on alternative TCO's and window layers has primarily focused on CdO. In this report we summarize results on cells fabricated using CdO in the substrate structure. The effect of "buffer" layers is also discussed, as well as initial results for Cd_2SnO_4 and $CdIn_2O_4$.

Solar cells fabricated under this project are characterized by standard techniques that include light and dark J-V, C-V, C-f, and spectral response measurements. Whenever appropriate junction parameters such as diode factor (A), reverse saturation current (J_O), and background carrier concentration are extracted and used to explain solar cell behavior. Additional analysis such as SEM, XRD, and PL measurements are carried out on as needed basis.

As part of this project the University of South Florida continues to participate in the CdTe National Team activities that include processing and testing of team samples. USF is also participating in the Focus Group established by First Solar Inc.

1.0 INTRODUCTION

This project addresses most of the key CdTe technology areas, with focus on improving the manufacturability and long term stability of this technology. The activities over this three year period include development of simplified processing, study of novel front and back contacts, and long-term stability. This report describes work carried out during the last year of the project. The solar cells discussed below are fabricated by various deposition technologies that include chemical vapor deposition (CVD), chemical bath deposition (CBD), close spaced sublimation (CSS), and rf-sputtering. The devices are routinely evaluated using standard solar cell analytical techniques such as dark and light current-voltage (J-V), spectral response (SR), and capacitance-voltage (C-V) measurements.

2.0 CELL FABRICATION PROCEDURES

A detailed description of the various processes used for the fabrication of CdTe solar cells at USF can also be found elsewhere[1]. A brief description is provided here for completeness. The baseline CdTe solar cells fabricated during this project are of the superstrate configuration:

Corning 7059 glass/SnO$_2$:F/SnO$_2$/CBD-CdS/CSS-CdTe/doped graphite.

Variations to the above structure include the following:

(a) Soda lime glass (typically LOF TEC 15 or 20) is used regularly for CdTe solar cells fabricated at low processing temperatures.
(b) Transparent conductors other than SnO$_2$ include CdO, Cd$_2$SnO$_4$ and ITO. Under a different contract sponsored by the Japanese New Energy and Industrial Technology Development Organization (NEDO) a co-sputtering capability was developed and is dedicated to the deposition of TCOs based on Cd, In, Zn, Sn, and Ga. Some of these are already being incorporated into cells while others are still at the early stages of development/investigation.
(c) The CdS is routinely deposited by either the Chemical Bath Deposition (CBD) process or Close-Spaced Sublimation (CSS). The close-spaced sublimation is a higher throughput process that has manufacturing advantages over CBD.
(d) The CdTe is deposited by CSS, in two temperature regimes depending on the type of glass substrate in use. Maximum processing temperature for soda lime glass substrates is 550°C, and for borosilicate glass is 625°C. In addition to the small area reactors currently available, a large area deposition system is being developed for submodule size substrates (10 x 10 cm^2).
(e) Graphite doped with HgTe:Cu, Cu-free materials or alternative Cu-based methods, such as sputtered Cu$_X$Te, are being used as back contact options.

3.0 ALTERNATIVE WINDOW LAYERS – TRANSPARENT CONDUCTING OXIDES

The area of window layers/transparent conducting oxides (TCOs) deals primarily with studying materials that can serve as effective front contacts for CdTe solar cells in place of the commonly used SnO$_2$, as "buffer" (high resistivity) layers, or as replacements for CdS. Although, SnO$_2$ and CdS have been widely used with very good performance results, the CdTe technology has reached a level where alternative options need to be explored in order to advance the overall device efficiency, improve manufacturability, or possibly improve the long-term stability of CdTe. Work by scientists at NREL has clearly demonstrated the importance of the front contact/window layers for this technology[2]. In this section the results on alternative TCO/window materials and processes are discussed.

3.1 Cadmium Oxide

The electro-optical properties of tin doped cadmium oxide films (CdO:Sn) were presented in a previous report[1]. After demonstrating that both transmission and conductivity were well within the required range for solar cell applications, the focus shifted on incorporating these films in solar cells. The objective is to investigate the potential of this material as a front contact or window layer in CdTe solar cells. Cadmium oxide films were used for solar cell fabrication as window layers or front contacts using various device configurations and process options; these include, low and high temperature CdTe and CdS prepared by CSS and CBD.

3.1.1 CdTe/CdO Devices

Using CdO:Sn as a replacement for CdS could lead to enhanced J_{SC}'s, as the absorption edge of heat-treated CdO:Sn was found to be about 100 nm below that of CdS (approx. 400 vs. 500 nm)[3]. However, CdTe/CdO/SnO$_2$ cells exhibited very low V_{OC}'s (<500 mV), with device characteristics dominated by shunting. Such V_{OC} values are even lower than what is typically obtained for CdTe/SnO$_2$ junctions. This device behavior was initially attributed to problems associated with a highly "defective" CdTe/CdO interface, as a direct result of the high cell processing temperatures. However, devices fabricated by limiting all processing temperatures below <550°C did not result in improved performance. No further analysis or process optimization was pursued as it became apparent that within the current "optimized" parameter space of our cell fabrication procedures CdTe/CdO cells exhibited poor characteristics.

3.1.2 CdO:Sn in Bi-layer Front Contacts

In this section device results with CdO:Sn/high ρ bi-layer structures are presented. The high-ρ layer (ρ ≈ 1-3 Ω-cm) is MOCVD SnO$_2$, which is what is used in baseline devices. Devices discussed in this section were fabricated using CBD CdS and high temperature CSS-CdTe (≈ 600°C). The first sets of cells were fabricated in order to determine whether the CdO:Sn films are thermally/chemically stable after being exposed to the various cell fabrication procedures.

Figure 1. The V_{OC} and FF of CdO:Sn/SnO$_2$/CdTe solar cells.

Figure 1 displays the V_{OC} and FF for devices with CdO:Sn deposited to different thicknesses, ranging from no CdO to just under 2000 Å. It is clear that the V_{OC}, which is typically a good indicator of the junction quality, is essentially constant and above 820 mV for all devices fabricated onto CdO:Sn. The FF shows a monotonic decrease for thicknesses below 700-800 Å, while for larger thicknesses it has exceeded the 70% mark. Based on these cell performance characteristics it can be concluded that the properties of CdO:Sn remain unchanged during the cell fabrication process. The decrease in the FF for the small thicknesses is clearly due to an increase in the cell series resistance as displayed in the light J-V for these cells shown in Fig. 2. Devices fabricated without CdO:Sn and with CdO:Sn of 300 Å, are series resistance limited while all other cells exhibit essentially identical series resistances. The device with 1500 Å, exhibits the best overall

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Figure 2. Light J-V of CdO:Sn/SnO₂/CdTe solar cells with varying thickness of CdO.
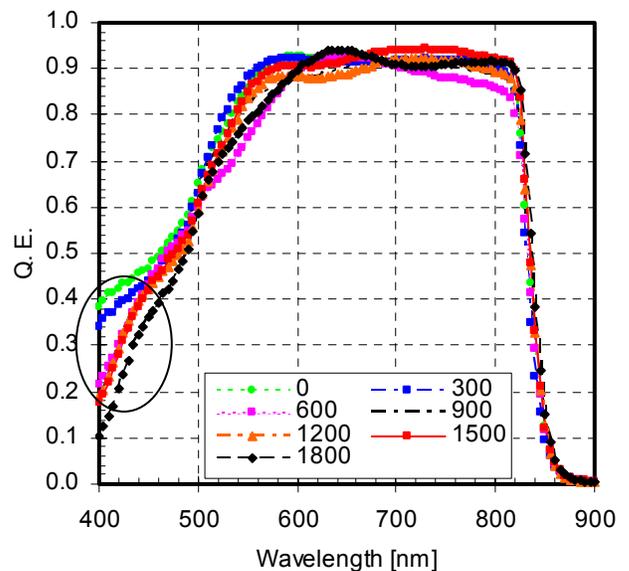
Figure 3. The SR of CdO:Sn/SnO₂/CdTe solar cells (shown in Fig. 2).

characteristics, but this behavior is not believed to be associated with the CdO:Sn thickness. It should be noted that the cells displayed in Fig. 2 are the best devices from Fig. 1, while Fig. 1 contains results for at least four cells per thickness.

The SR of the cells from Fig. 2 is shown in Fig 3. Essentially, all devices exhibit similar QE. The small decrease observed at short wavelengths (region marked with a circle) for all cells with CdO:Sn of 600 Å or thicker, is due to increased absorption in CdO. Variations in the 500-600 nm range could be related to the interfacial $CdS_{1-x}Te_x$ layer. The rest of the observed variations are due to variations in film thicknesses leading to shifts in the interference peaks.

3.1.3 CdO:Sn in all CSS CdTe/CdS Cells

After utilizing CdO in baseline devices (CBD-CdS/CSS-CdTe) a series of all-CSS cells (CSS-CdS/CSS-CdTe) were fabricated. The most significant processing difference between the two types of cells is the substrate deposition temperature of CdS (>500°C for CSS vs. 80-90°C for CBD). This results in different nucleation mechanisms for the two processes, yielding films with different grain structure, orientation, and density. The impurity content of the films is also expected to vary significantly due to the nature of the processes themselves but also the fact that the CSS-CdS is 99.999% pure while the CBD films are deposited form sources with 98.5% purity. Depending on the deposition conditions CSS-CdS can contain O_2 (sometimes in the form of CdO). Depositing CSS-CdS in the presence of O_2 has been found to improve solar cell performance[4]. The CdO:Sn films are not expected to be affected by the CSS-CDS deposition process, since they have exhibited no significant changes after deposition of CVD SnO_2 (i.e. CdO:Sn/SnO_2) a process that takes place at high temperatures (>450°C) and O_2 ambient.

With most deposition parameters fixed to reproduce previously determined "optimum" film properties, the thicknesses of both the SnO_2 (undoped) and CdO were varied in order to optimize the thicknesses of the CdO:Sn/SnO2 bilayer structure. The results are shown in Figs. 4 and 5, where the FF and V_{OC} as a function of the CdO and SnO_2 thicknesses are shown.

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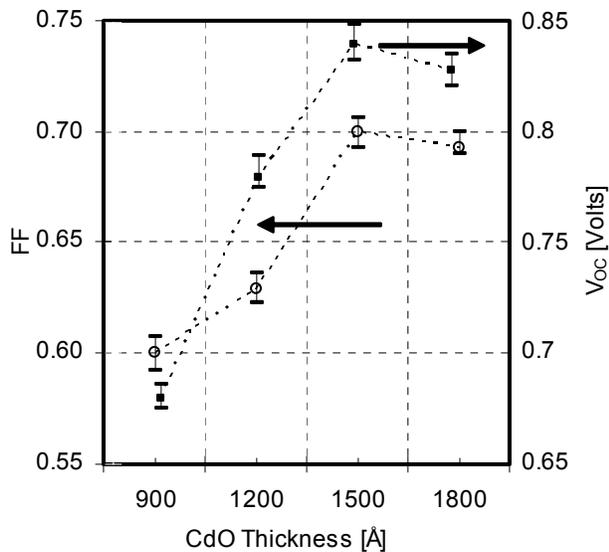
Figure 4. The V_{OC} and FF of all-CSS CdTe devices as a function of the CdO thickness
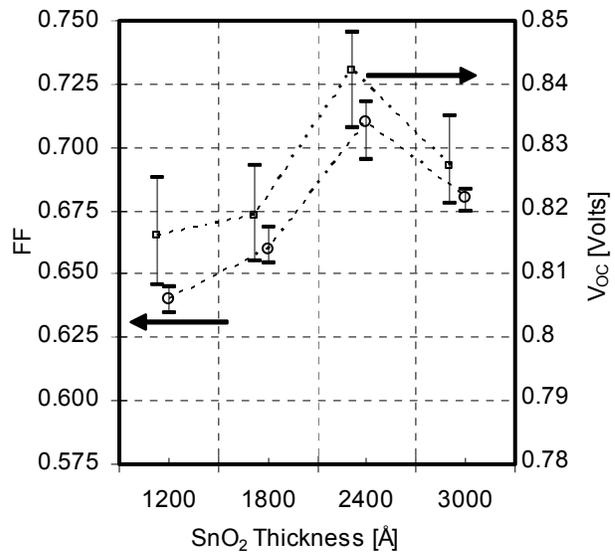
Figure 5. The V_{OC} and FF of all-CSS CdTe devices as a function of the SnO$_2$ thickness

The data shown in Fig. 4 (V_{OC} and FF vs. CdO:Sn Thickness) cover thicknesses in the same range as the devices shown in Fig. 1 (<2000 Å). However, comparing the results in the two figures (1 vs. 4), two distinct differences can be identified: (a) the performance for all-CSS devices begins to drop off at large thicknesses than the CBD-CdS devices (approximately 1500 Å vs. 800 Å), and (b) in the case of all CSS devices the V_{OC} follows the FF unlike the CBD-CdS cells where the V_{OC} remained essentially constant. The device characteristics in the case of Fig. 4 were not limited due to large series resistances, but rather due to "shunting". Only a speculative explanation can be given at this time as no additional analysis has been performed to further investigate the properties of these layers and interfaces. It is possible that as the CdO thickness is decreased, the nucleation process of the CSS-CdS is modified affecting the structural properties of the CSS-CdS and resulting in more pinholes. It should be noted that to-date, the CSS-CdS films cannot be used to the same small thicknesses as the CBD-CdS due to the difficulty in depositing these films pinhole free at small thicknesses (<900-1000Å).

Figure 5 shows the effect of the "buffer" layer thickness (in this case CVD SnO$_2$) on the V_{OC} and FF; the bars in the graph show highest, lowest, and average values based on at least three cells. The device structure is: CdO:Sn/SnO$_2$/CSS-CdS/CdTe. The thickness of the CdO was fixed at approximately 1500 Å based on the results of Fig. 4. The thickness for the CSS-CdS was also fixed, but as it will be indicated below it varied in at least one instance. These data supports the need for a "buffer" layer, in this particular case with a thickness of at least 2000 Å, in order to sustain higher V_{OC}'s and FF's. The devices with the thickest SnO$_2$ exhibited a drop in both V_{OC} and FF. This is believed to be associated with a smaller CdS thickness for this cell and not the "buffer" layer thickness. The SR data of the best cells of Fig. 5 are shown in Fig. 6. It is clear from the short wavelength response that the device with the buffer layer of 3000 Å, also has the thinnest CdS. Based on these results one can conclude that both the CdS and buffer layer thickness can be optimized (minimized) for optimum performance. The difficulty with CSS-CdS films remains the fact that they cannot be deposited to the same small thicknesses as the CBD-CdS.

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The light I-V the best cell fabricated to-date based on a CdO front contact is shown in Fig. 7. The V_{OC}, FF and J_{SC} were 850 mV, 75.0% and 23.7 mA/cm^2 respectively. The J_{SC} was calculated from the SR shown in Fig. 8.
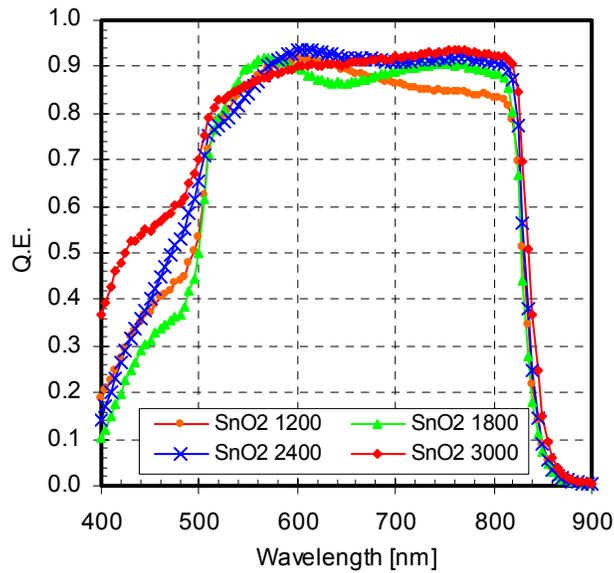
Figure 6. The SR of CdO:Sn/SnO$_2$/CSS-CdS/CdTe cells (shown in Fig. 5)
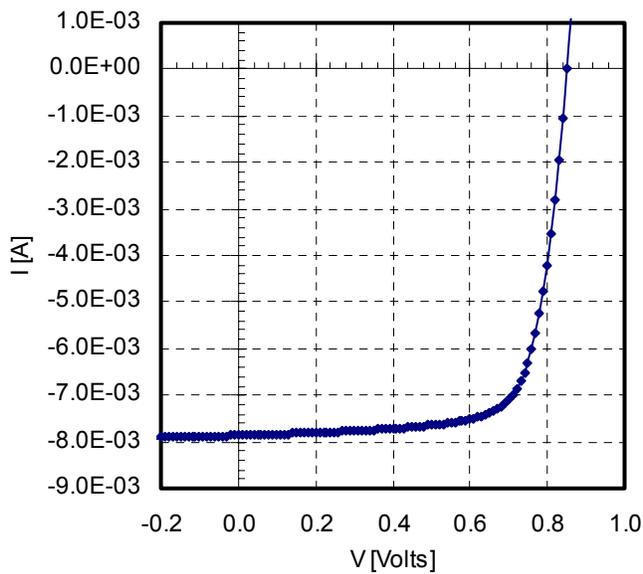
Figure 7. Light I-V of best CdTe cell fabricated with CdO as the front contact.
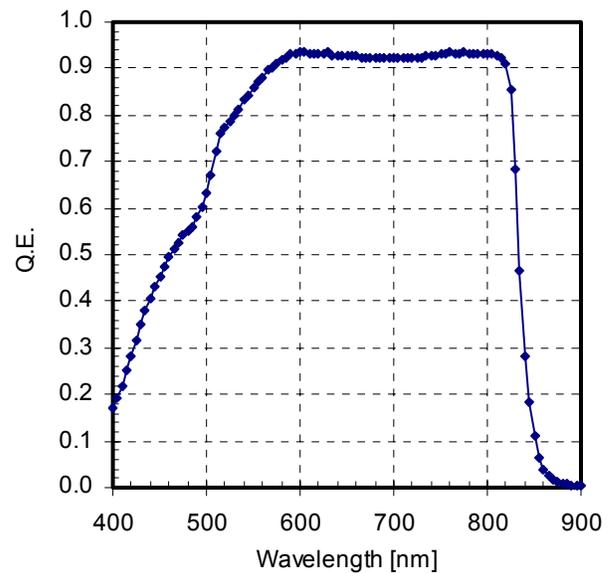
Figure 8. The SR of the device shown in Fig. 7.

3.1.4 CdO Sheet Resistance

The effect of the substrate (i.e. $CdO/SnO_2/CdS$) on the performance of the cells discussed in the above sections is summarized in Fig. 9 where the influence of the resistance (R_{SHEET}) on the FF is shown.   The data include representative devices from all the various device structures fabricated and discussed above. As already mentioned in a previous section replacing CdS with CdO produced very poor results, and such devices are not included in Fig. 9. The data has been divided in three regions (I, II and III) based on the FF (above and below 70%) and R_{SHEET} (above and below 20 $\Omega/\square$). The device performance (specifically the FF) in these regions is significantly affected by the characteristics of the $CdO/SnO_2/CdS$ substrate as follows:

Region I: FF > 70% - R_{SHEET} < 20 $\Omega/\square$

In this region the devices were fabricated with CdO sufficiently thick (at least 600 Å) to achieve low enough sheet resistance; it should be noted that over 50% of the devices in this range had a sheet resistance less than 10 $\Omega/\square$. In addition to the minimum CdO thickness requirement, all cells in this region also met minimum thickness requirements for the undoped SnO_2 and/or CdS films. Either one or both of these layers had to be sufficiently thick in order to maintain the FF above the 70% level. The minimum thickness of the CdS varied depending on the method of deposition (CSS vs. CBD).

Figure 9. The dependence of the FF on R_{SHEET} for CdO-based solar cells.

Region II: FF < 70% - R_{SHEET} < 20 $\Omega/\square$

In this region the CdO thickness is the same as region I above, however, the undoped SnO_2 layer or the CdS were not thick enough, and the FF dropped to values below 70%, and in some extreme cases below 60%.

Region III: FF < 70% - R_{SHEET} > 20 $\Omega/\square$

The limiting factor in this range is the sheet resistance of the CdO, regardless of the thicknesses of the other two films.

3.2   Ternary Transparent Conducting Oxides

Under a different contract sponsored by NEDO (Japan) a co-sputtering (RF) capability for the deposition of TCO's has been developed. Among the first materials under investigation are Cd_2SnO_4 and $CdIn_2O_4$. Co-sputtering offers flexibility in the preparation of these materials in that their composition (stoichiometry) can be varied. In most cases these variations were on the order of a few percent around the stoichiometric composition, i.e. Cd/Sn=2.0 for Cd_2SnO_4 and Cd/In=0.5 for $CdIn_2O_4$. The ratios are simply varied by controlling the deposition rates. Film thickness and composition is very uniform over a deposition area of approximately 6 x 6 cm^2, as a result of using substrate rotation, and adjusting the angle between the sputtering sources and the substrate. A significant difference in the deposition of these two materials is the fact that

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Cd_2SnO_4 is deposited from the binary oxides (SnO_2 and CdO) while $CdIn_2O_4$ is deposited by reactive sputtering of metallic targets (Cd and In) in an O_2 ambient.

The approach taken under this effort is to first establish film deposition conditions that produce TCOs with reasonable electrical and optical performance prior to incorporating them into cell structures. Only a few solar cells have been fabricated to-date using Cd_2SnO_4, with most of the work at this point being focused on material properties. No devices have been fabricated on $CdIn_2O_4$ yet, as this material is still at the early stages of investigation.

3.2.1 Cadmium Stannate (Cd_2SnO_4)

Cadmium stannate was selected as the first material option based on the promising results obtained at NREL[2]. As mentioned above, Cd_2SnO_4 was prepared by RF magnetron co-sputtering from CdO and SnO_2 targets. Most depositions were carried out at room temperature; unless otherwise stated all results discussed in this section are for room substrate deposition temperature. The typical ambient was 100% Ar, introduced after obtaining a background pressure in the range of 10^{-6} Torr. The process was initially calibrated using EDS to determine film composition. Once the film composition was reproducibly controlled the Cd/Sn ration was varied and the properties of the films investigated. X-ray diffraction was also used to investigate the structural properties of the films.

3.2.1.1 Composition vs. Electro-Optical/Structural Properties

Figure 10 shows the resistivity of Cd_2SnO_4 films deposited with Cd/Sn ratios ranging from approximately 1.50 to 2.4. As the data indicates a minimum resistivity is obtained for "Cd-rich" conditions. The lower resistivity is believed to be due to Cd interstitials. It has been suggested that excess Cd conditions can lead to an increase in Cd interstitials therefore affecting the material's resisivity[5].

The results shown in Fig. 10 were for films deposited at room temperature but subsequently annealed. Room-temperature as-deposited films were found to be amorphous and resistive, therefore heat treatments were employed to further improve their properties. Figure 11 shows the XRD spectra for as-deposited and heat-treated Cd_2SnO_4 films. As the data shows the films are initially amorphous but begin to crystallize at annealing temperatures of

Figure 10. The resistivity of Cd_2SnO_4 films as a function of the Cd/Sn ratio.

approximately 525°C, where the (222) peak begins to appear. At 550°C additional orientations appear, but the (222) direction dominates and is the preferred orientation. Higher temperatures up to and including 700°C were also used, but it was determined that the films begun to decompose as indicated in Fig. 12. Here the XRD spectrum of a film annealed at 700°C is shown, where a SnO_2 related peak begins to appear.

Figure 11. XRD spectra for Cd₂SnO₄ films annealed at temperatures ranging from 500 - 550°C.
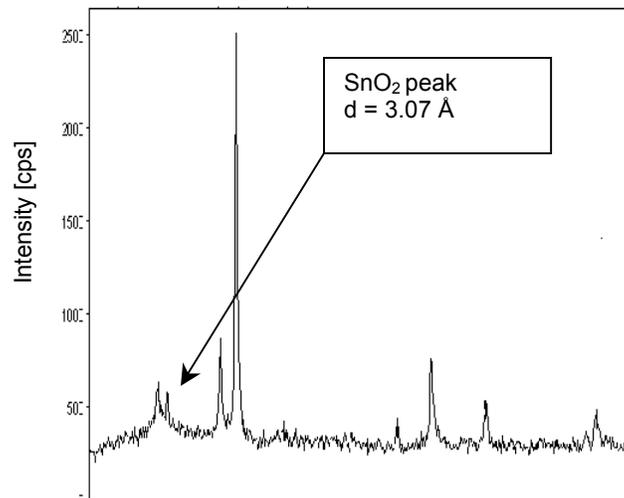
Figure 12. XRD pattern for Cd₂SnO₄ annealed at 700°C showing the appearance of a SnO₂ phase.

3.2.1.2 Solar Cells

Solar cell fabrication using Cd_2SnO_4 as the front contact is still at the early stages. However, the first sets of devices made using this material have produced some interesting results. Table I shows the performance of the best devices from three substrates where the thickness of the Cd_2SnO_4 was varied as indicated. The V_{OC}'s have exceeded 800 mV, and the FFs are approaching 70%. These quantities are below the best values that can be obtained using bi-layers of SnO_2 as the front contact. However, the key difference in the cells listed in table 1 is that they are fabricated without a resistive layer (i.e. $Cd_2SnO_4/CdS/CdTe$). The reason for the relatively high V_{OC}'s and FF's in the absence of a resistive layer will require further study, but based on the structural/electrical properties of Cd_2SnO_4 one may tentatively conclude: (a) although a "buffer" layer is not deposited, it is possible that such resistive layer forms at the Cd_2SnO_4/CdS interface as a result of a reaction between these two films during the fabrication process. However, since it was previously found that heat-treating Cd_2SnO_4 in the presence of CdS enhances its conductivity, this will be ruled out for now[6]. (b) Cd_2SnO_4 films were found to be smoother than CVD SnO_2[6]. This may have aided the CBD-CdS deposition by resulting in more nucleation sites and therefore denser and pinhole free CdS films that can yield high V_{OC} and FF cells.

At this time no significant gain in J_{SC} has been realized as a result of replacing SnO_2 with Cd_2SnO_4, even though the optical transmission of Cd_2SnO_4 has been in general higher than that of SnO_2 (depending on the thickness of the films). The spectral response of the cells listed in table I is shown in Fig. 13. The overall behavior is similar to what is obtained with $SnO_2/CdS/CdTe$ devices with baseline CBD-CDS films, however, a more derailed and accurate study will be carried out to better quantify any gains in J_{SC}. In addition, the thickness of the CdS will be revisited, since it is possible that the smoothness of Cd_2SnO_4 may allow the use of thinner CdS.
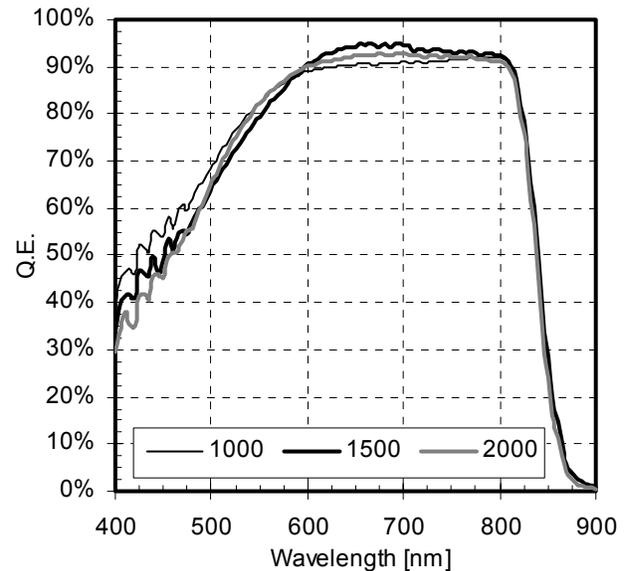
Figure 13. The SR of the Cd_2SnO_4-based cells listed in table 1.

Table 1. Solar cell performance (best devices) for cells fabricated on Cd_2SnO_4 without a high-ρ buffer layer.

Cd_2SnO_4 thickness [Å]	V_{OC} [mV]	J_{SC} [mA]	FF [%]	Efficiency [%]
1000	825	23.56	68.3	13.28
1500	808	23.48	67.3	12.77
2000	821	23.10	69.6	13.20

4.0   IMPROVING MANUFACTURABILITY – DRY PROCESSING

As mentioned earlier one of the objectives of this project is to simplify the cell fabrication processes in order to improve issues associated with large scale high throughput manufacturing. Lower processing temperatures (<550°C), all-CSS devices, and dry processing have been addressed during this project. The following sections discuss results obtained from a vapor-based $CdCl_2$ treatment.

4.1   Vapor Chloride Process description

The vapor $CdCl_2$ process is carried out in a chamber such as the one shown in Fig. 14 below. The process is based on controlling the temperature of two zones (zone 1: $CdCl_2$ and zone 2: substrate), and transposing vapors of $CdCl_2$ over the sample area using a carrier gas. Three different ambient gases (carrier gases) were used: (a) He, (b) O_2 (mixture of O_2 and He), and (c) H_2 ambient. The total flow rates as well as the partial pressure of O_2 were also varied in certain cases. The ultimate objective is to develop a completely dry cell fabrication process, while maintaining state of the art performance. Currently, "wet" steps in the baseline cell fabrication procedure include the CBD CdS, $CdCl_2$ post-deposition heat-treatment, and CdTe surface etch (bromine or nitric/phosphoric solution).
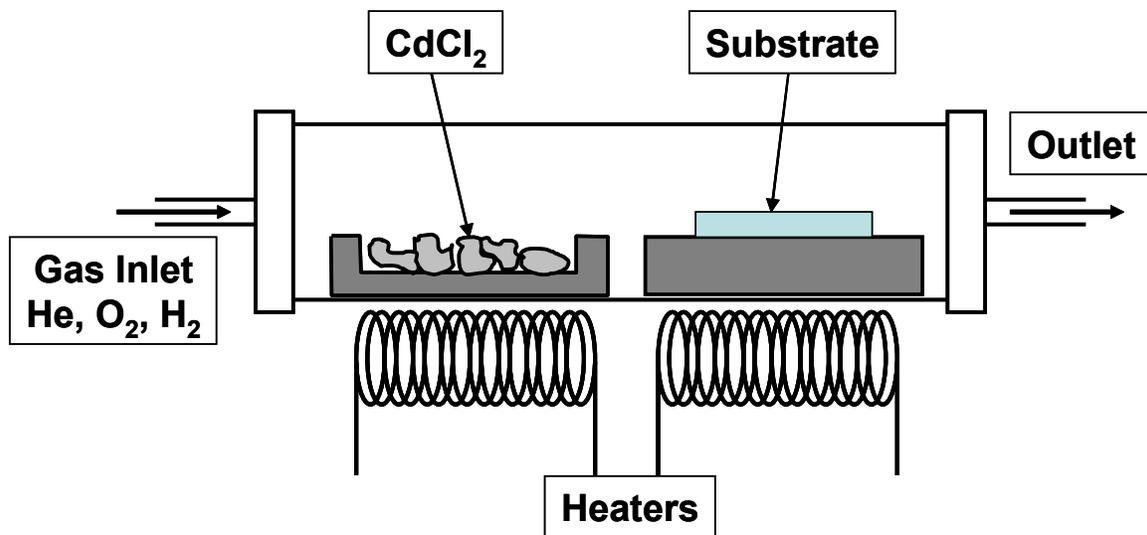
Figure 14. The Vapor CdCl$_2$ treatment apparatus used during this project.

Previous work on the vapor $CdCl_2$ treatment produced encouraging results in terms of cell performance, but reproducibility was often a challenge. One of the additional precautions taken in recent work in this area was to maintain the gas flow through the annealing chamber at all times in order to minimize exposure of $CdCl_2$, which is hygroscopic, to moisture, and instead of using $CdCl_2$ powder the powder was pressed into pellets.

Since the objective is to eventually develop a "dry" fabrication process it would be desirable to eliminate any $CdCl_2$ residue from the CdTe surface after the $CdCl_2$ treatment. A series of samples vapor-treated at temperatures in the range of 360-400°C was analyzed using EDS to determine whether significant amounts of chlorine (Cl) remain on the surface of the CdTe following the vapor treatment process. The temperature range includes the to-date optimum temperatures. The results are summarized in table 2, where it is apparent that significant

amounts of Cl (therefore $CdCl_2$) are found on the surface of the CdTe. Higher annealing temperatures did not show any Cl but cell performance in those cases was limited (see section below).

Table 2. Amount of Chlorine found on the surface of CdTe after the vapor $CdCl_2$ process.

Annealing Temperature [ºC]	Chlorine Concentration [%]
360	17.0
370	18.0
380	23.0
400	4.3

4.1.2   High Throughput Processing – Short Annealing Times

The deposition of the semiconductors can vary depending on the method of deposition, however, in the case of a vapor transport process or CSS this can be done in a few minutes. The $CdCl_2$ treatment process is a time consuming fabrication step. Typically the $CdCl_2$ is applied to the CdTe surface, the structure is then heat treated and subsequently the $CdCl_2$ residue if any, must be removed. The vapor treatment has the potential of combining all these steps into a single process, but the duration of the heat treatment is still relatively long (up to 30 minutes in some cases). In this section results from work on shortening the duration of the vapor $CdCl_2$ treatment by using higher annealing temperatures are presented.

Figure 15 shows results for high temperature vapor treatments processed for 1, 2, and 3 minutes. The data displayed show average, high, and low values from up to 8 cells from two substrates per experiment. The two data sets represent annealing temperatures below 500ºC - (approx. 480ºC) indicated by the triangles, and above 500ºC (approx. 520ºC) indicated by the square symbols. The reason for the approximate temperatures is due to the fact that due to the fast heating rates and short annealing times, the temperature controllers do no settle in time at the desired temperatures, but tend to oscillate (this is an issue that needs to be addressed in future work). It should also be noted that the cells shown in Fig. 15 have not been exposed to any wet processing following the vapor heat treatment (i.e. no bromine or nitric/phosphoric acid
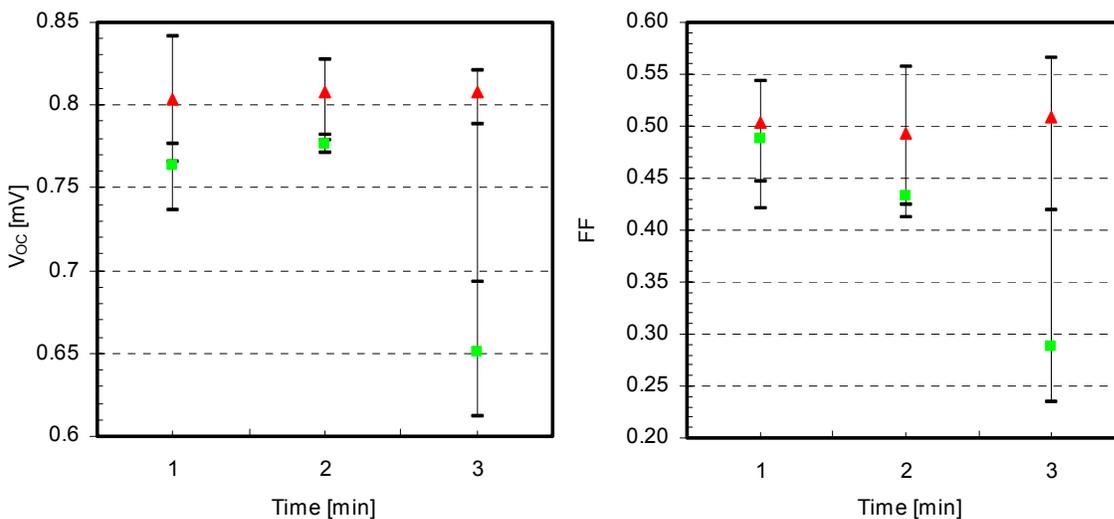
Figure 15.   The V_{OC} and FF for CdTe cells vapor treated at high annealing temperatures for times less than 5 minutes.

etches). The most important result from these experiments is the high V_{OC}'s obtained for both annealing temperatures for 1 minute treatment times. In general the shorter annealing times appear to yield better performance, with the lower of the two temperatures being overall superior. Nevertheless the results exhibit significant variations at this time, partly due to the difficulty in controlling the temperatures as mentioned above.

4.1.3 The Effect of H_2 Ambient

The use of oxygen during the $CdCl_2$ treatment has been shown to be beneficial to device performance [1]. However, the use of O_2 could lead to the formation of surface oxides which could have a detrimental effect on the back contact formation, especially if one is to eliminate the treatment (wet etch) of the CdTe prior to the application of the back contact. Inert ambient such as He has been previously investigated with limited success; cell performance was always limited compared to devices processed in the presence of O_2. During this phase of the project H_2 was also used as the ambient gas during the vapor $CdCl_2$ treatment; the typical ambient was a mixture of He and H_2 in order to be able to vary the partial pressure of H_2. One of the concerns in using H_2 during this process, especially at high temperatures, is the fact that H_2 can react with SnO_2 reducing it to Sn. However, in order for this reaction to take place the H_2 would have to diffuse through the CdTe and CdS first. Table 3 lists some of the better devices obtained from vapor treated CdTe cells in the presence of H_2. The duration of the heat treatment was less than 1 minute. The V_{OC} appears to increase with the CdTe thickness. A similar trend was observed in the past for $CdCl_2$ treatments carried out in the presence of O_2. However, in the case of O_2, the variation in V_{OC} was considerably smaller and for the best devices the V_{OC} exceeded 800 mV. These results should be expected as the diffusion of the various species ($CdCl_2$, H_2, and O_2), and therefore their influence on device performance, will be affected by the thickness of the CdTe. However, what is not clear at this time is the effect of H_2 which seems to limit the V_{OC} to values below 800 mV. It is possible that H_2 influences the background doping concentration in CdTe, or has an effect on the CdTe/CdS interface. In the case of O_2, its effect during the $CdCl_2$ treatment has been found to be beneficial by promoting the interdiffusion of CdTe and CdS[7]. Work on the vapor treatment continues with emphasis on eliminating the wet etch and developing a larger area apparatus.

Table 3. The V_{OC} and FF for Solar cells $CdCl_2$ vapor treated in the presence of H_2.

CdTe Thickness [μm]	V_{OC} [mV]	FF [%]
3.6	790	59.42
5.0	758	59.28
6.7	709	59.43

5.0 BACK CONTACTS

Work on back contacts has been primarily focused on Cu-free options. Work on Sb_2Te_3 and Ni_2P was carried out during the first two phases of this project. Unfortunately performance of Sb_2Te_3-contaceted cells remained well below of what has been reported by others[8]. The reasons for this are not clear at this time, and the issue may be revisited in the future. During this phase of the project Cu-free contact work was limited to Ni_2P.

5.1 Ni$_2$P Contacts

After optimizing the process for temperature, ambient, and annealing times, the effect of the Ni$_2$P concentration in the graphite paste was investigated. Figure 16 shows the light J-V for the best cells obtained using the concentrations indicated. None of the J-V data sets suggests the formation of a limiting back barrier, which was often the case for cells contacted with Ni$_2$P and annealed at non-optimum temperatures. The primary difference in the devices of Fig. 16 is in the series resistance, the smallest one being for the device contacted with 25% (by wt.) concentration paste. The general trend shown in Fig. 16 was consistent for additional sets of devices contacted with these concentrations. Previous SIMS analysis of Ni$_2$P-contatced cells indicated that relatively high concentrations of phosphorous were found only within the first 1-2 μm from the CdTe surface, and was

Figure 16. Light J-V of Ni$_2$P-contacted CdTe solar cells.

below the detectable limits in the bulk of the CdTe. It is therefore believed that the variations in series resistance shown in Fig. 16 are associated with this region of the device (i.e. CdTe surface) and not with the bulk CdTe.

5.1.1 Light Soaking Experiments

The primary reason for investigating Cu-free back contact options is due to the belief that Cu is responsible for the observed degradation in CdTe devices. A set of devices contacted with Ni$_2$P
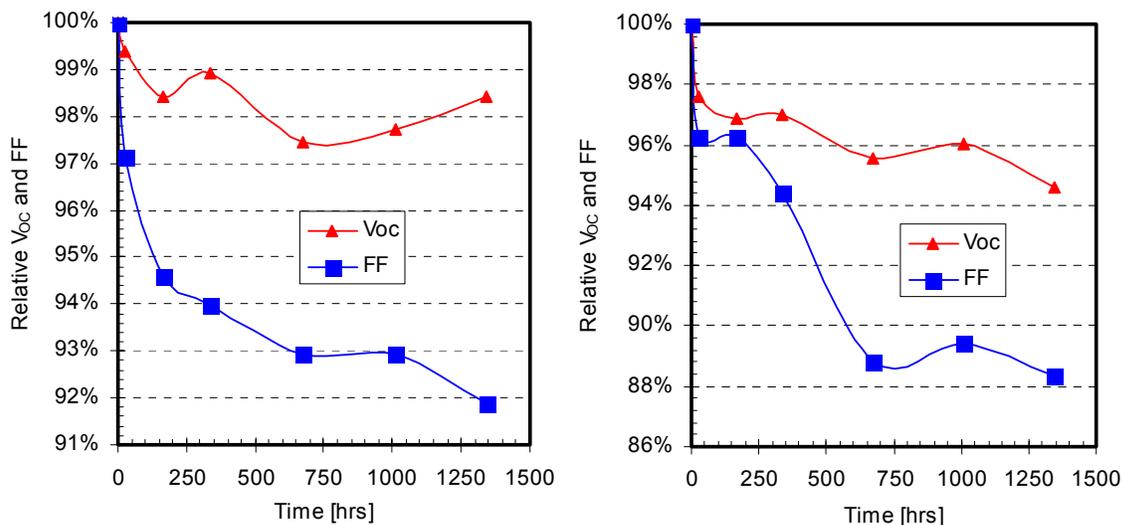
Figure 17. Relative V$_{OC}$ and FF for Ni$_2$P-contacted CdTe cells light soaked at First Solar Inc.

were fabricated at USF and light soaked for over 1300 hours at First Solar. Figure 17 shows the results of this experiment where the relative V_{OC} and FF are shown for two such devices. The device on the left was held at J_{SC} and the device on the right was held at J_{SC} for 1000 hours and then switched to V_{OC}. In general the behavior of both cells is very similar with the V_{OC} remaining within approximately 5% of its initial value while the FF has decreased by approximately 10%. This is not significantly different than behavior observed for cells contacted with Cu-based contacts. The SIMS analysis of the Ni_2P-contacted devices indicated that Cu was present in these devices but to much lower levels than devices contacted with Cu-based contacts[1]; the source of this Cu is most likely the starting materials used for the cell fabrication (i.e. CdTe, graphite, etc.). The fact that the devices in Fig. 17 do exhibit significant degradation suggests that either Cu has to be reduced to levels below those found in the starting materials, or simply the degradation is due to changes in the device not associated with Cu.

6.0   STABILITY STUDIES – TEMPERATURE STRESS EXPERIMENTS

6.1   Experimental/Device Details

During the first phase of this project we initiated a temperature stress study using a small number of solar cells with a primary objective to determine a satisfactory range of temperatures to stress a larger number of devices [1]. Subsequently, a set of CdTe devices were fabricated using our baseline process and stressed at six temperatures: 60, 70, 80, 90, 100, and 120°C. The average starting V_{OC} and ff for all devices used in this study were 840 mV and 72% respectively; three cells were stressed at each temperature. The cells were kept in the dark and at open-circuit conditions. For this experiment we used a vacuum oven, into which heaters were installed to create six independent temperature zones. The oven was evacuated (50 mTorr) and backfilled with He several times and eventually kept at a slightly positive pressure (<5 psi). Additional information on this procedure can also be found in a previous report [1]. The next section summarizes the results obtained after stressing the CdTe devices for approximately 3600 hours.

6.2   Results

Figure 18 summarizes the three-cell *average* change in V_{OC} and ff over 500-hour time intervals. It is clear that the bulk of the degradation occurs during the early stages of the stressing process
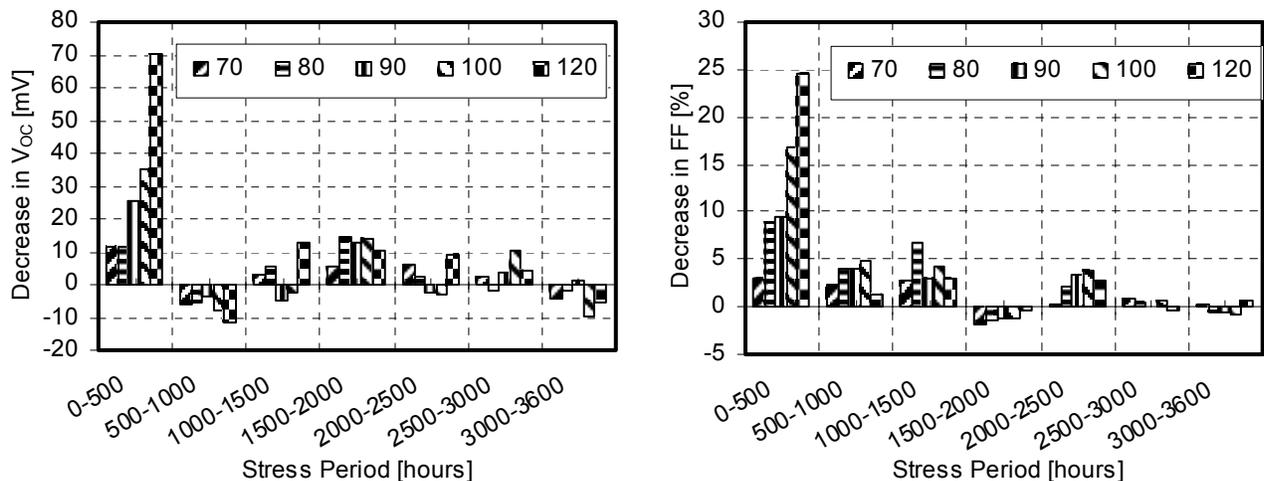
Figure 18. The change in V_{OC} and FF over 500 hour time periods for CdTe cells stressed at temperatures in the range of 70 to 120°C.

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(i.e. within the first 500 hours). Additional changes in both quantities are considerably smaller during subsequent stressing, which includes periods for which solar cell performance seems to partially recover. The V_{OC} seems to recover by approximately 5-15 mV during the 500-1000 hour interval while the ff recovered during the 1500-2000 hour interval. It should be noted that the largest V_{OC} recovery was observed for the cell that exhibited the largest decrease (i.e. 120°C). The opposite is true with regards to the ff, where the largest recovery is for the cells that exhibited the smallest decrease (i.e. 70°C). The data of Fig. 18 are also summarized in tables 4 and 5.

Table 4. V_{OC} changes in 500-hour time intervals.

Stress Interval [Hrs]	0-500	500-1000	1000-1500	1500-2000	2000-2500	2500-3000	3000-3600	Average Change [mV]	Total Change [mV]
70	11.41	-6.17	3.16	5.51	6.21	2.33	-4.01	2.63	18.43
80	11.66	-5.37	5.59	14.64	2.16	-1.68	-2.09	3.56	24.91
90	25.28	-3.84	-4.96	12.98	-2.42	3.38	1.15	4.51	31.58
100	35.31	-7.76	-2.66	13.81	-3.06	10.15	-9.42	5.20	36.38
120	70.19	-11.44	12.82	10.45	9.05	4.28	-5.38	12.85	89.98

Table 5. FF changes in 500-hour time intervals.

Stress Interval [Hrs]	0-500	500-1000	1000-1500	1500-2000	2000-2500	2500-3000	3000-3600	Average Change [%]	Total Change [%]
70	2.91	2.31	2.68	-1.82	0.34	0.79	0.29	1.07	7.50
80	8.74	3.95	6.81	-1.46	2.15	0.40	-0.63	2.85	19.96
90	9.38	3.99	2.94	-1.26	3.44	0.10	-0.58	2.57	18.00
100	16.72	4.80	4.31	-1.31	3.85	0.63	-0.85	4.02	28.15
120	24.60	1.33	2.91	-0.41	2.68	-0.39	0.66	4.48	31.38

The V_{OC} and FF for these cells over the 3600 hour stress period are included in Appendices A1 and A2. In this section data pertained to the lowest, highest and an intermediate temperature (70, 120, and 90°C respectively) are discussed. The trends from these three temperatures are consistent with what was observed for the other two temperatures (80 and 100°C). The results discussed in this report represent the "typical performance" observed at each temperature.

Figure 19 shows J-V data for a cell stressed at 70°C taken at various times during the thermal stressing (left – dark Ln(J)-V, center – light J-V 4th quadrant, right - light J-V). The figure includes J-V data taken at 0, 580, 1260 and 3600 hours. The following section summarizes the changes (qualitatively) observed for the device stressed at 70C.
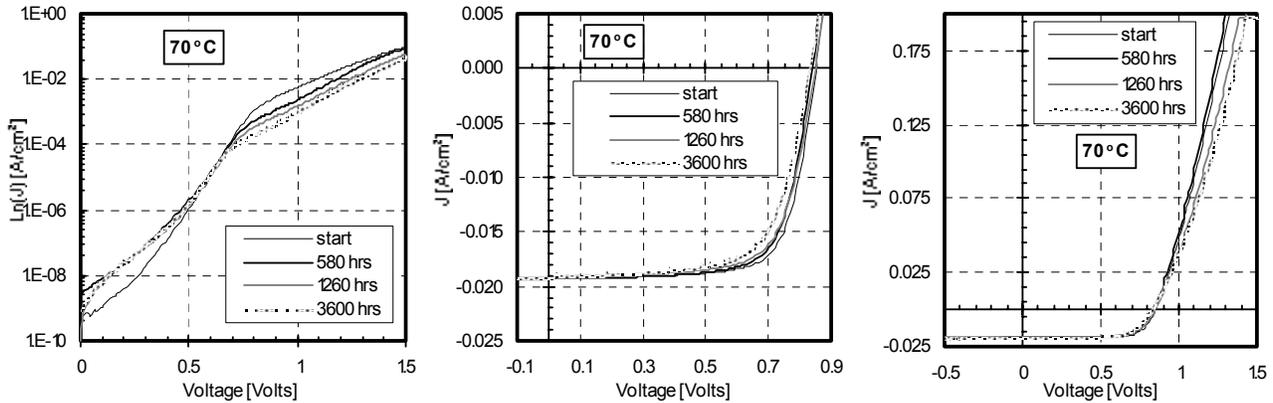
Figure 19. Dark (left) and light (center, right) I-V for a CdTe cell stressed at 70°C.

6.2.1 Dark J-V

The current at low voltages (V<0.7 Volts) increases within the first 580 hours, with subsequent changes being negligible. This increase could be either due to increased "dark" shunting or increased recombination currents. It is therefore suggested that thermal stressing does not affect the main junction characteristics beyond the 500-600 hour interval. At higher voltages (V>0.7 Volts), the dark current decreases (see both ln(J) vs. V and linear characteristics in figs. 19 and 20). This leads to J-V characteristics with a rather large turn-on voltage (see fig. 20) and significant dark light crossover. The crossover does not appear to have a direct impact on device performance (under illumination). In fact, unstressed state-of-the-art devices often exhibit similar behavior. This observed "shift" in the dark J-V may be associated with photoconductivity changes in CdTe or CdS. Another possibility is that a "barrier" exists at the front region of the cell (i.e. CdSTe/CdS, or CdS/SnO$_2$), which increases with stress, and whose effect on the cell J-V is eliminated under illumination. Efforts to model a front barrier using AMPS are consistent with what is empirically observed in the dark, but not under illumination, where the simulated light J-V exhibit an "S-shape" behavior near V$_{OC}$ (note that in fig 19 center/right, the light J-V are consistent with "ohmic" contacts and do not indicate the presence of a barrier).
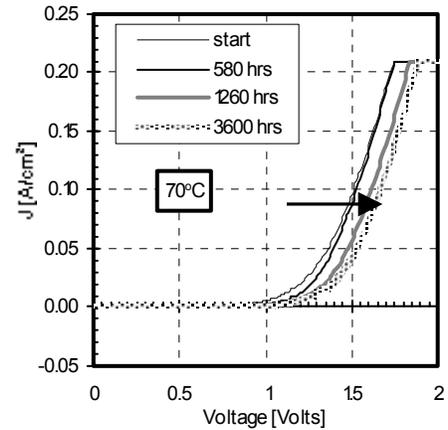
Figure 20. Linear dark J-V of device shown in Fig. 19.

6.2.2 Light J-V

The change in V$_{OC}$ is small but the FF appears to decrease significantly (see tables 4&5). During the early stages of stressing, it was possible to estimate values for J$_O$ and A, and these were used to explain the initial losses in V$_{OC}$ [1]. However the subsequent increase in shunting dominated the J-V and estimation of these parameters was not possible. The light J-V behavior suggests that the lower FF's are caused mainly due to an increase in the series resistance, as indicated by the changes in J-V in the fourth quadrant and at high currents in the first. It should also be noted that no significant decrease in the light shunt resistance was observed.

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In summary, the observed changes (which are typical) in the devices stressed at 70°C take place primarily during the initial stress period (approximately the first 500-600 hours), and appear to be related to the front/main junction region. An increase in the resistivity of the CdTe or CdS is also possible, with no evidence of any degradation or other effects related to the back contact.

6.2.3 Summary for T=90 & T=120°C Stress Temperatures

The data for a typical device stressed at 90°C are shown in fig 21. Qualitatively, the changes are essentially identical to what has been described above for the cells stressed at 70°C. However, as it is clearly evident from tables 4/5 and fig. 21 that quantitatively the observed changes/degradation are larger in this case, for both the dark and light J-V. A key difference between the cells stressed at 70 and 90°C, is that the latter also show signs of "light shunting". The dark and light J-V data for cells stressed at the highest temperature (120°C) are shown in fig 22. In this case it is evident that shunting dominates both the dark and light characteristics of these devices, with nearly 80% of the observed degradation taking place within the first 500 hours.

In addition to the updated performance data and J-V results presented in this report, SIMS results provided in a previous report [1] indicated that the Cu concentration in CdTe increased (slightly). This increase exhibited a spatial dependence; the Cu concentration was higher in the CdTe region close to the CdTe/CdS interface i.e. within the depletion region. Therefore unlike many of the other instances previously reported where the observed degradation in CdTe cells was dominated by degradation of the CdTe/Back contact interface region, in this case the most significant changes point to degradation/changes taking place at the main junction. Copper may still be responsible for these changes as it appears to accumulate in the junction region of these devices.
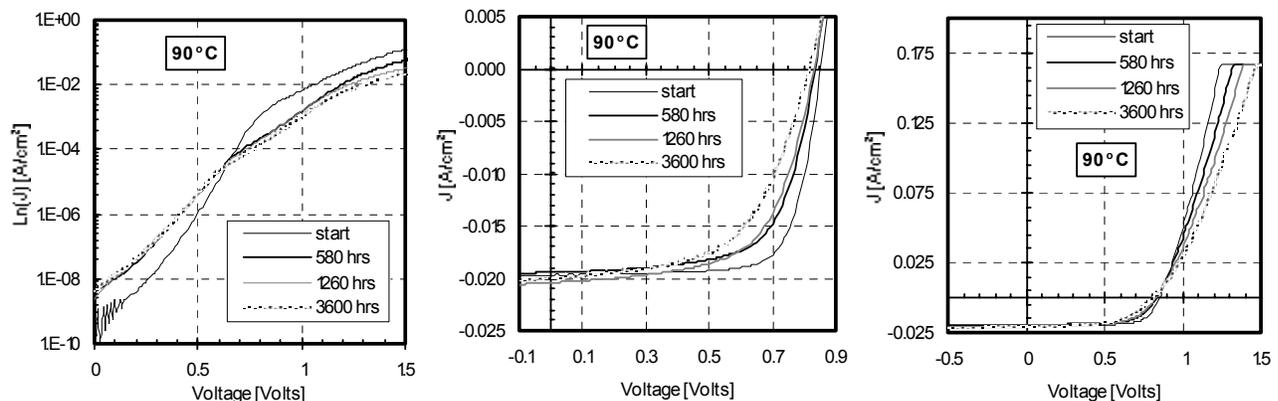
Figure 21. Dark (left) and light (center, right) I-V for a CdTe cell stressed at 90ºC.
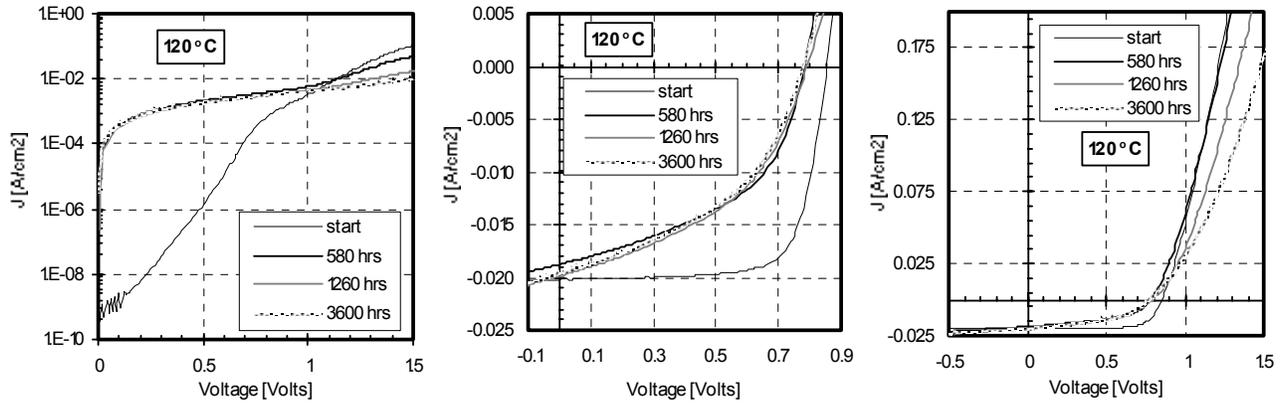
Figure 22. Dark (left) and light (center, right) I-V for a CdTe cell stressed at 120ºC.

PART II - CIGS

EXECUTIVE SUMMARY

This project had as its primary objectives development of improvements in the manufacturability of CIGS devices and development of high band gap alloys for use in tandem structures. Additional objectives included development of improved junction options and contributing to the overall understanding of these materials and devices. All results reported are for two-step, all solid state processing. Loss of cost-share funding resulted in significant scaling back of the tasks, particularly the high band gap alloy work.

Progress has been made in all task areas. State-of-the-art Jsc's have been achieved for both CIGS and CGS. The highest Jsc for CIGS, 41 mA/cm^2, in fact was accomplished with a reactively sputtered ZnO junction replacing the CdS. A major challenge for two-step solid state processing has been effective incorporation of Ga. This issue has been studied extensively using AMPS© simulations and advanced characterization tools such as photocapacitance. Significant advancements have been made in understanding defect formation and the effect of defects on performance. Applying these insights to process modifications has lead to control of Ga-based defects in the interface region of our devices. This has resulted in a one-to-one increase in Voc with band gap and state-of-the art Voc's. However, in accomplishing this objective the defect density in the bulk increased resulting in losses in Jsc. Combining the accomplishments of state-of-the-art Jsc's and Voc's in the same run remains a challenge for the next phase.

Three alternative junction materials, ZnO, In$_2$Se$_3$ and ZnIn$_2$Se$_4$(ZIS) were investigated as potential replacements for CdS. ZnO is deposited by reactive sputtering, while the others are deposited by evaporation, all physical vapor deposition processes. As indicated above, state-of-the-art Jsc's have been achieved with ZnO, though Voc's and FF are about 10% below CdS values. In$_2$Se$_3$ has significant manufacturing advantages because its source materials are the same as CIGS. While reasonable initial performance is achieved, there is a substantial stability problem that seems to be due to reactivity with Cu in our devices. ZIS has about the same performance level as ZnO, and also seems stable. With further work either ZnO or ZIS may catch up to CdS.

Photocapacitance has been developed as an effective tool for characterizing defects. When combined with AMPS simulations significant insights to device performance have resulted. It is becoming clear that the difficulties with attaining proper Ga bonding are associated with use of Se flux. We have learned how to attain good Ga bonding by controlling the flux in both bulk and surface regions, though not simultaneously. Wavelength dependent photocapacitance shows a shift to bulk defects when surface defects are reduced. The challenge for the future is to control defect formation in both regions simultaneously.

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1.0   INTRODUCTION

This project had as its primary objectives development of improvements in the manufacturability of CIGS devices and development of high band gap alloys for use in tandem structures. Additional objectives included development of improved junction options and contributing to the overall understanding of these materials and devices. The loss of EPRI cost sharing at the end of the first year had a major impact on our ability to address all of these objectives adequately. Through discussions with the NREL contract manager the tasks were restructured to reflect the loss in EPRI funding. Much of the high band gap work was discontinued after the first year, but the student working on that task was allowed to finish the subtasks needed to complete his dissertation. Work on the other three tasks was continued into the second and third years, though at a reduced level. In spite of the negative impact of the forced rearrangement progress was made on all task areas. Highlights from each of the areas will be provided below. More in depth and inclusive discussion of each can be found in the quarterly and annual reports.

1.1 Device Fabrication

Details of our deposition process have been described previously [1,9]. We provide a brief description here for convenience. The important features of our process are that it is all-solid-state and does not utilize co-evaporation. Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by sputtering or evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 °C. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. Much of what is presented in the following discussion is for our baseline process. In this process the order of deposition of the precursors is Cu/Ga/(In + Se). Deviations from this procedure will be presented as they arise in the ensuing discussion. Formation of the semiconductor layer takes about one-half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by high ρ/ low ρ ZnO deposited by sputtering.

Because of the very complex nature of these materials we have found it useful to intentionally grade compositions. The locations of the sources relative to the 2" x 2" substrate are shown in figure 1. Each source can be made to vary in deposition rate/time to result in a thickness difference of 5 to 10% from the near edge to the far edge of the substrate. We deposit a 5 x 5 array of cells of area 0.1 cm^2 by using a shadow mask for ZnO deposition. The resulting compositional gradients allow for a richer database and avoid issues associated with run-to-run variables when precise comparisons are necessary. By adjusting our run parameters we can operate in regimes that have both high and low sensitivity to the compositional profiles. This is also useful for avoiding high sensitivity processes that would be unacceptable at a manufacturing level.
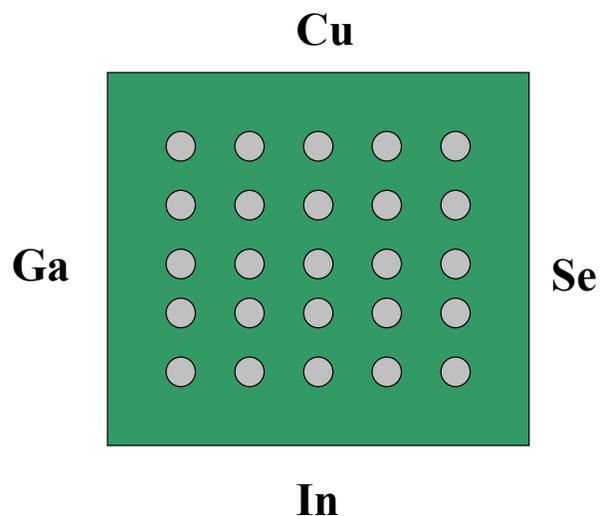
Figure 1. Arrangement of sources around the 2" x 2" substrate.

2.0 RESULTS AND DISCUSSION

2.1 CIGS Processing

The central issue in developing our manufacturing-friendly process has been the proper incorporation of Ga. We have succeeded in utilizing Ga to improve adhesion. We have successfully incorporated small quantities of Ga in our Type I devices with low band gaps to improve performance. And, to a certain extent the bulk Ga in our CGS devices is properly incorporated. What continues as a difficulty is the incorporation of Ga in the space charge region of CIGS devices to effectively raise the band gap to the desired 1.2 eV range. All of our devices have at least 10% Ga, but most of this is not in the space charge region. We have developed techniques for incorporating this amount of Ga in the space charge region with concomitant increases in band gap, but the electronic quality of these layers is always inferior to those with less Ga. We are still trying to determine the fundamental cause of this problem, and have utilized extensive modeling and advanced measurement concepts to assist our efforts. Results from these techniques will be discussed further below along with data on our efforts at Ga control.
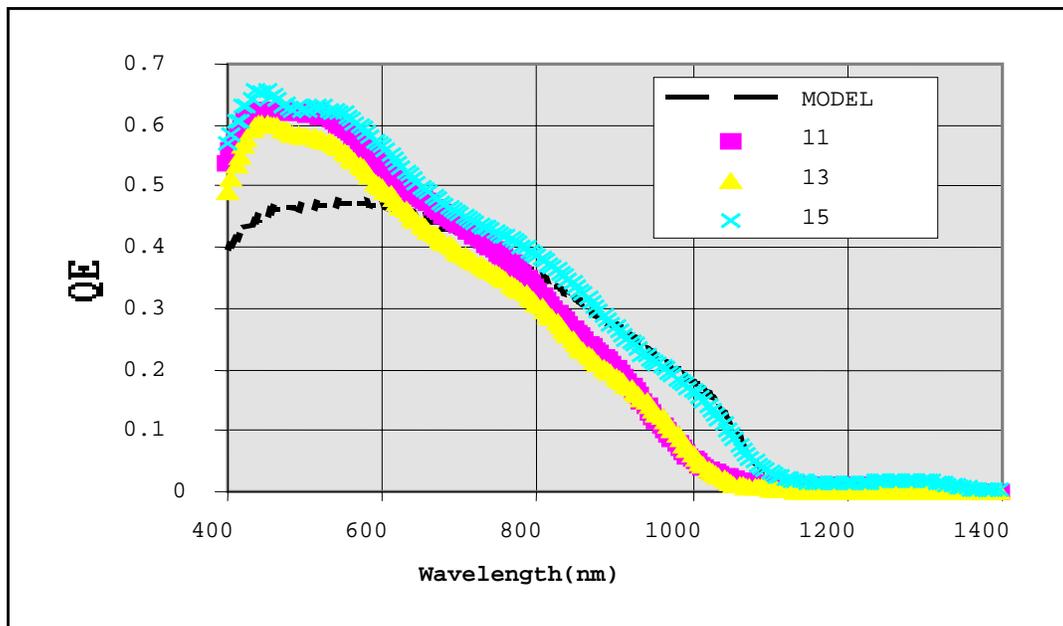
Figure 2. Spectral response for a run with increased Ga in the SC layer.

The nature of the problem is demonstrated in runs in which we force large amounts of Ga into the space charge layer by varying our process sequence. For example, in our standard Type I runs a free layer of Ga is deposited first and then In and Se are added. The proximity of In to the top of the device during the deposition sequence gives it an advantage over Ga in the space charge region. However, in type II devices we deposit In before Ga thus giving Ga the advantage by proximity. This does matter in that Type II devices typically have larger band gaps. Thus, thermodynamics does not have the final word here. Squatter's rights also play a role. Representative spectral responses for a Type II run are shown in figure 2. Referring to figure 1, device 11 is in row 1 column 3, 13 is row 3 column 3, and 15 is row 5 column 3. The band gap shift is in the range 0.15 - 0.2 eV over the 0.95 eV band gap of our Type I devices

indicating significant encroachment of Ga into the space charge layer. The drop in carrier collection, however, is dramatic. In fitting the data with our spectral response model as shown, the resulting parameters were a depletion width of 0.15 microns and negligible diffusion length. The collapse of the diffusion length raises concerns that an inverted band profile might be hurting carrier collection. That is, the tails out to 1300 nm in the QE profiles of these devices could be interpreted as evidence for presence of a low gap region.. If the low gap region were behind a higher gap region, i e, at the rear of the space charge region, this would hurt the collection of minority carriers. Such a situation would also be expected to result in a poor FF, however, the FF for these devices is in the range 0.6 to 0.63 which is reasonable and not indicative of an inverted band profile.

The Voc profile for the run is shown in Fig. 3. Voc's up to 575 mV are observed which is a 100 mV increase over devices with the standard Ga level. This still represents only about half of the voltage increase expected from the band gap shift. Since the evidence suggests that more Ga is near the CdS interface, which is thought to be the main recombination region, suspicion must be cast on Ga as the lifetime reducing agent that is hurting Voc. The bilayer structure hypothesized above, however, could provide a different perspective on voltage behavior. As seen in the figure, Voc favors the central region, especially toward the Se source. This in part suggests a strong role by Se flux in forming the important interface region, but it equally can be interpreted as an aversion to Ga at these high Ga levels.

The difficulties posed above were improved upon with further experimentation. Significant assistance, however, was provided by a combination of AMPS modeling and capacitance measurements. As a result of our ongoing efforts we were able to overcome this problem as shown in figure 4 which shows Voc versus band gap for a more recent Type II run. In this case we cover a range of 70 meV in energy gap, and as shown, we realize a one-one increase in Voc of 70 mV from 490 to 560 mV. The key to success was not letting the defect density increase as Ga was added to increase the band gap . The defect level as measured by our photocapacitance technique is also shown, and as can be seen, it does not increase with increasing band gap. This

Figure 3. Voc profile for a run with increased Ga in the SC layer.
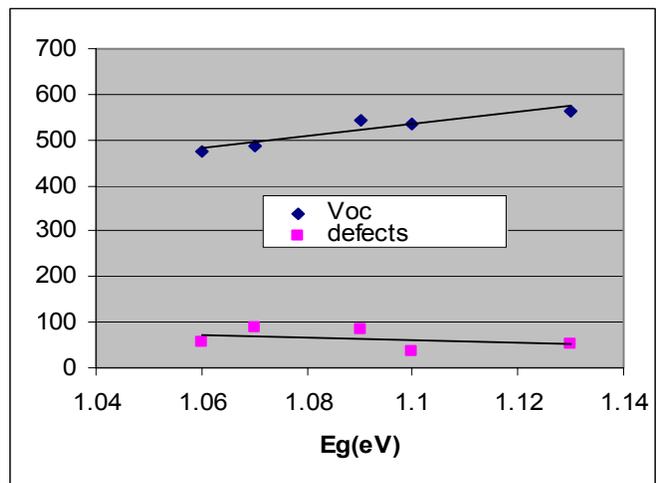
Figure 4. Dependence of Voc and defects on Eg for Type II devices.

result was achieved by understanding the effect of Cu/In ratio combined with Se flux on Ga incorporation. Although this was a big step forward, 560 mV is still too low a Voc for a band gap of 1.13 eV. Clearly there are additional factors affecting Voc that remain to be understood and controlled.

Improving Voc is key to further advances in efficiency. We have achieved state-of-the art Jsc's in low band gap devices, and have demonstrated the ability to do this consistently. After significant effort to further resolve the low Voc problem we felt that we were confronted with a fundamental limitation. The limitation that we suspect is that associated with trying to deposit metallic layers in a chamber that also supports Se deposition. It is common knowledge that once Se deposition is done in a chamber, Se is everywhere. Consequently, for our Type I structures which start with sequential Cu and Ga layer depositions, we became concerned that these metallic layers contained traces of Se from the background flux. We tried mitigating this issue by depositing the metal layers in another Se-free chamber, but we concluded that exposure of these layers to ambient when transferring between chambers had a bigger negative effect on performance than trace Se. To overcome this problem we designed and built a new deposition system that isolates the metal layer depositions from Se. This system became operational during the third year of this project and has been used for complete runs for the past several months. It has become the critical ingredient needed to demonstrate further improvements in our processing approach. Much of the time has been devoted to "bringing the system up". A key component of this is carefully noting any differences between the new and old system as the same process recipes are run in both. There are always lessons to be learned when transferring or scaling-up a process. What we can report thus far is that the new system is working well according to the design principles used. We have accomplished isolation of the metal depositions without exposure to Se or ambient. We also have successfully transferred our Type I process from the old system. What this means is that device performance is comparable for the same process recipe. Also, we are happy to report that the new system provides much greater control over process parameters and excellent reproducibility. These are critical to the detailed experiments that are needed to finish sorting out the key issues associated with Ga incorporation and low Voc's. Preliminary results support our contention that the metal layers were being affected by the environment in the old chamber. However, the mechanisms do not seem to be as simple as we assumed. There also appears to be an effect due to the closed environment of the new chamber. That is, the old chamber is opened before each run and exposed to ambient. The new chamber has a load lock, so, 10-15 runs can be completed without opening. By carefully charting the runs we are observing what appears to be a contamination effect on Jsc associated with the run history after opening the chamber. This is very interesting in that it must be tied into the absence of Se in the metal chamber as well. This is the type of phenomenon that could not be observed in a standard research system, but becomes critical when trying to scale up a research process to manufacturing levels. We are not sure what the final outcome of this new observation will be, but this effort will be continuing under the follow-up project. The capabilities of this new system should allow a final resolution of what can be achieved with the two-step, all solid-state processing approach.

2.2 CGS

This is the task area that was most impacted by the loss in EPRI cost sharing, however, progress was made on some subtask elements. Devices were fabricated with the same two-step, all solid-state processing approach used for CIGS. The bulk properties of the CGS layers exhibited high electronic quality through XRD and SEM/EDS analysis and device performance. We followed the approach that we used with CIGS, to first improve and gain control over Jsc and then move on to Voc. We have achieved a Jsc of 15.2 mA/cm^2 which is close to the ideal of

about 17.6 mA/cm^2, and this was achieved without an AR coating. We have also advanced Voc and FF up to values of 775 mV and 0.6 respectively. While these are approaching the best values reported in the literature, overall performance of CGS is still far below that needed for tandem structures, and all research groups are reporting similar difficulties. While Jsc is reasonably good, Voc, and to a lesser extent FF are far below required performance levels. We have not found traditional materials measurements to be of much help in determining the underpinnings of these shortcomings. They seem to be at the micro-structural, and particularly,

point defect level in CGS, though contact and interface issues are contributing as well. As we have worked to improve Voc, we have observed complex interrelationships among Jsc, Voc and FF. This is thwarting our efforts to improve Voc. Part of the difficulty is that straightforward application of our successful AMPS model for CIGS is not working with CGS. The problem is summarized in figure 5. The "semi-ideal" plot is what might be expected from a straightforward extrapolation from CIGS to CGS. Of particular interest is the high Voc. For a material with a band gap of 1.65 eV it is difficult to simulate the low Voc's that are observed. The "actual" plot of figure 5, with Voc of about 700 mV is a good representation of what is observed experimentally. The low Voc was achieved by using a rather large reverse diode at the back contact. While this produced low Voc and a good fit to the power curve of actual devices, the bend-over at high forward bias is not typical of actual devices. Nevertheless, we further explored this mechanism, and as seen in figure 6, the effect of the back contact energy can be substantial. To follow-up on this we initiated a series of experiments to vary the conditions of back contact formation. We did see effects suggesting that the interfacial region with the Mo was sensitive to the chemical species that was deposited first. We could make Voc worse by manipulating the deposition details in this region, but we did not succeed in making it better before the loss of cost sharing funds caused us to shelve these activities. It is likely that the back contact is part of what's limiting CGS performance. We hope to pick this up again when conditions are more favorable.
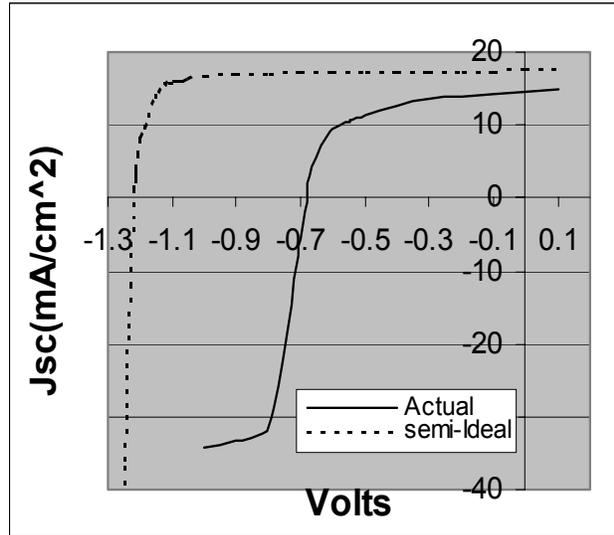
Figure 5. AMPS simulated IV plots for "semi-ideal" and actual CGS.
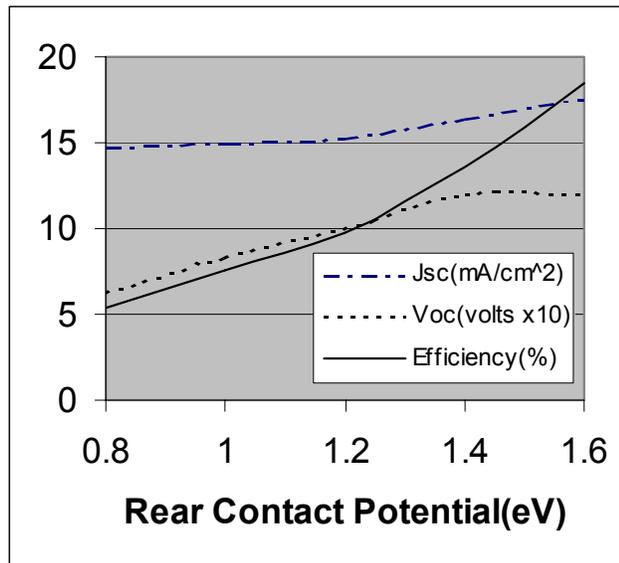
Figure 6. AMPS simulated performance parameters as a function of rear contact potential for CGS.

2.3   Alternative Junction Options

2.3.1   ZnO

There is ongoing interest in simplifying the junction formation process. Of particular interest is eliminating or replacing CBD CdS. The best outcome would be elimination, retaining only a double layer ZnO contact. Since ZnO is commonly deposited by sputtering, an acceptable physical deposition process, this would be a highly desirable outcome from a manufacturing perspective. Thus we and others have been attempting to form suitable junctions with ZnO[10]. The best success has been achieved with CVD ZnO[3], though progress continues with sputter deposition. We have developed a reactive sputtering technique that allows additional control over deposition parameters. Process mechanisms, however, are a bit more complex since a chemical reaction is being controlled at the growth surface. Nevertheless, the ability to separately control Zn and O allows for a richer film growth regime and a larger range of film properties. Our initial results were poor with all parameters inferior to CdS controls. With ongoing improvements, however, we have improved all parameters, particularly Jsc. While Voc and FF values are about 10% low, Jsc's are on a par with CdS devices. A comparison is shown in figure 7. The integrated Jsc for the ZnO device is 41 mA/cm^2 which is the highest that we have achieved. None of the devices have AR coatings.
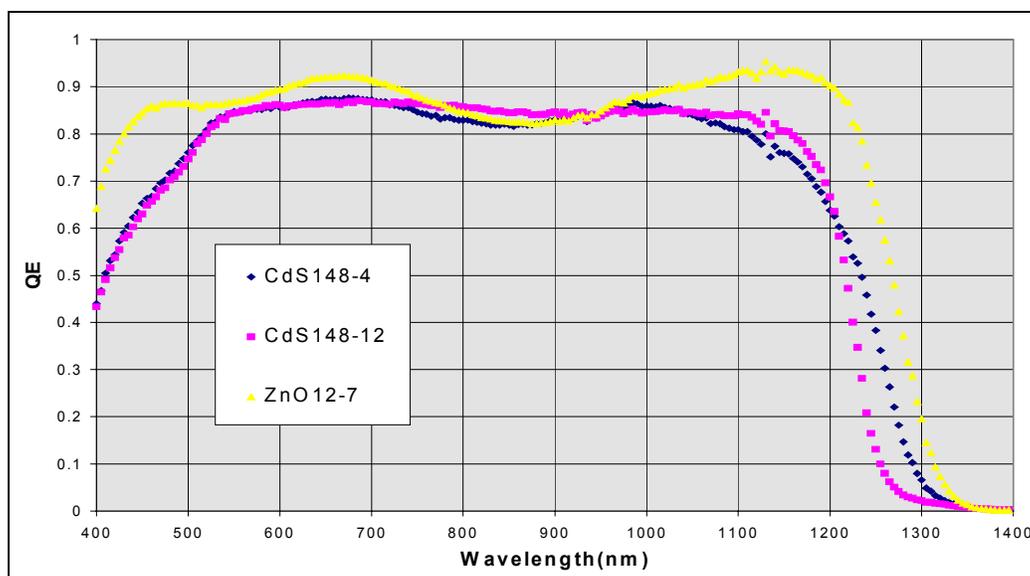
Figure 7. Comparison of QE response for CdS and ZnO devices.

Our analysis indicates that the low Voc and FF values are the result of poor interface properties. In part this is due to chemical and structural differences between ZnO and CdS. But some of the shortfall is likely due to the energetics of the sputtering process itself. While this can be mitigated to some extent, a significant reduction in growth rate is the likely price. Other options have emerged and will be discussed in the following sections. However, the possibilities for ZnO remain open. As we learn more about the nature of the interface from studies with these other materials, we may gain insights to allow a newly guided return to sputtered ZnO.

2.3.2 In$_2$Se$_3$

In$_2$Se$_3$ is a viable candidate for the buffer layer. In addition to its obvious compatibility with CIGS, it has a band gap of 2.3 eV and can be deposited from the same sources as the absorber. There has been some effort to characterize the properties of In$_2$Se$_3$ [12], but relatively little is known. Some success with device performance has also been reported [13], but conclusions have not yet been reached about its potential. We have undertaken an evaluation of In$_2$Se$_3$ buffer layers to help evaluate their potential and to add to our ongoing efforts to understand junction phenomena. In terms of device fabrication we were interested in determining if In$_2$Se$_3$ could be deposited at substrate temperatures of about 200 C, since our standard devices typically degrade if held at temperatures above this level after fabrication. We developed deposition procedures that produced stoichiometric In$_2$Se$_3$ at these temperatures and proceeded to use those procedures to deposit it as a buffer layer on top of CIGS. The devices were completed by depositing the same two-layer ZnO contact as used on our CdS devices. At the time of this study our reactor was processing Type I CIGS devices that had Jsc's in the 35-40 mA/cm^2 range, Voc's of 450 – 525 and FF in the .6 - .7 range. The range in Jsc's and Voc's is due to the band gap of the CIGS that was determined by the details of the run parameters. That is, by controlling the level of Ga in the space charge layer we could vary the band gap that would of course result in tradeoffs between Jsc and Voc. Typical efficiencies for standard CdS devices were in the 10 – 11 % range.

The distributions of Voc and Jsc values for a In$_2$Se$_3$ /CIGS run are shown in figure 8. As can be seen, Voc's are fairly uniform and in the same range as values for CdS devices. Since device areas are about 0.1 cm^2, Jsc's are in the range of 20 mA/cm^2 which is much lower than CdS references. As seen in figure 9, the reduction is Jsc is due to an overall downward shift in the QE spectrum. This was somewhat unexpected in that the buffer layer is at the surface and might be expected to affect Voc and FF more than Jsc which is to first order a bulk property. However, the observed behavior might be explained in terms of voltage redistribution or the influence of interface states.

465	475	485	485	485		1.2	1.6	1.9	1.7	1.4
475	485	485	485	495		1.9	1.6	2.0	1.75	1.9
475	485	485	485	485		1.75	2.05	2.5	2.25	1.75
485	485	485	485	485		1.9	2.15	1.7	2.3	1.6
475	485	485	485	475		2.0	1.8	2.4	2.15	1.4

Figure 8. Voc (left) and Isc (right) values for an array of 25 In$_2$Se$_3$ /CIGS devices.

To properly evaluate In$_2$Se$_3$ it is also necessary to account for other differences in junction formation procedures. In the initial devices such as that above the procedure for handling the absorber was the same. It was removed from the chamber after formation and placed in a second chamber for In$_2$Se$_3$ deposition. Thus it had the same air exposure as reference CdS

devices. To take full advantage of the nature of this buffer, we also left the absorber in place after its formation and deposited the In$_2$Se$_3$ buffer without breaking vacuum. Under this scenario we could also vary the procedure from absorber end to In$_2$Se$_3$ deposition in terms of cool-down time and deposition temperature. We did observe a general improvement in performance with these in-situ procedures, but there were other overriding factors that had to be sorted out.
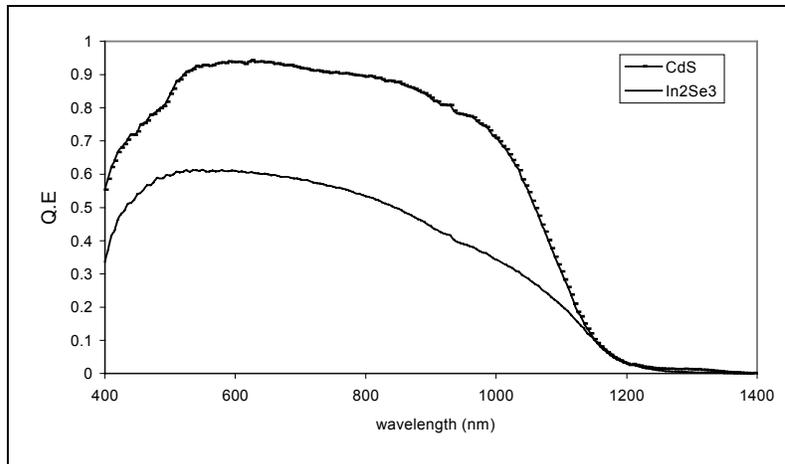
The effect of the electrolyte in the CdS bath on the absorber is always an issue that must be addressed for new buffer layers. We tried the usual range of partial electrolyte experiments and found that effects were present, though limited. The biggest effect was associated with Cd. Treatment with Cd ions (from Cd acetate) improved Jsc but lowered Voc. The change in QE response resulting in the increased Jsc is shown in figure 10. As can be seen, the change is not a simple shift upwards but appears to have elements of improved red response. This suggests influence on the space charge width or diffusion length which are subsurface phenomena.

Figure 9. QE spectral response for In$_2$Se$_3$ /CIGS and CdS/CIGS reference devices.
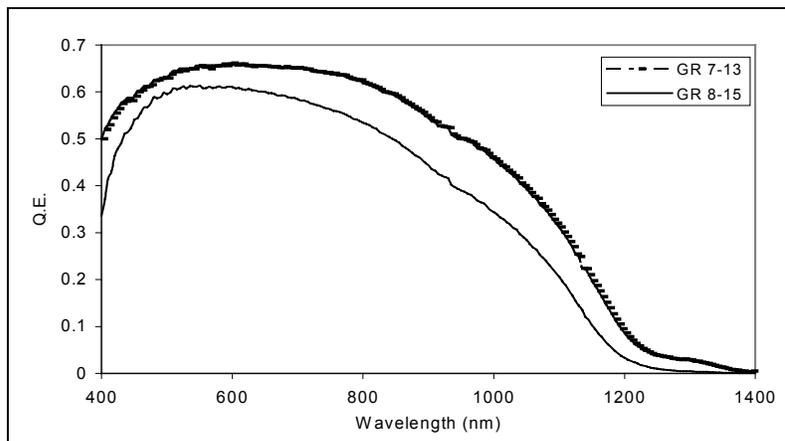
Figure 10. Comparison of spectral response for devices with(GR 8-15) and without(GR 7-13) Cd

Additional experiments were conducted to determine the dependence of performance on In$_2$Se$_3$ thickness and deposition temperature. The dependence of Voc and Jsc on thickness are shown in figure 11. 300 Å seems to be the favored thickness, though this is a limited set of data points, and more would be required to draw conclusions. The dependences of Voc and Jsc on the substrate temperature for In$_2$Se$_3$ deposition are shown in figure 12. The favored temperature is about 200 C. These profiles are similar to what is observed if we do a post deposition anneal on our standard CdS/CIGS devices. Typically we do not find that the anneal improves performance. In cases where it does, however, 200 C seems to be the highest acceptable temperature, and as we go above that performance drops off. Thus the temperature profiles for In$_2$Se$_3$ suggest that the same mechanism is responsible. The profiles are due to mechanisms in the absorber itself rather than to temperature induced influences on the growth of In$_2$Se$_3$. This might be particularly true of the drop-off above 200 C. The rise in performance up to 200 C,
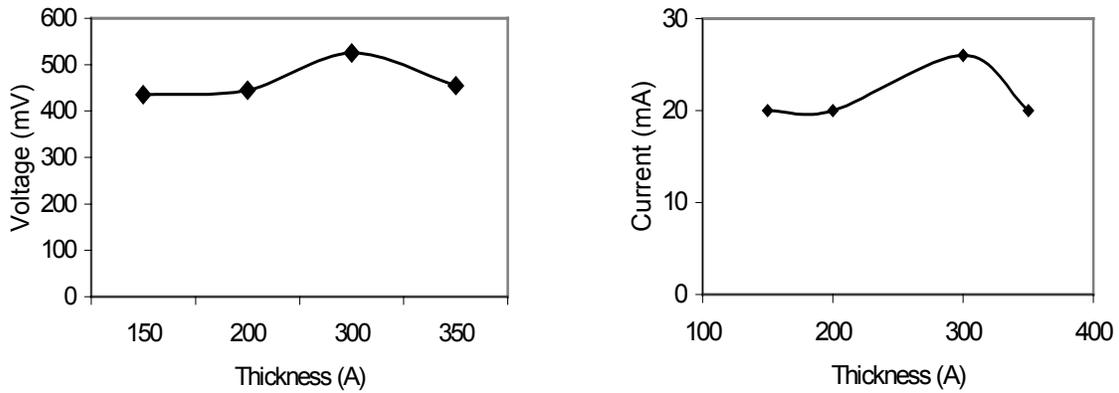
Figure 11. Dependence of Voc and Jsc on In$_2$Se$_3$ layer thickness.
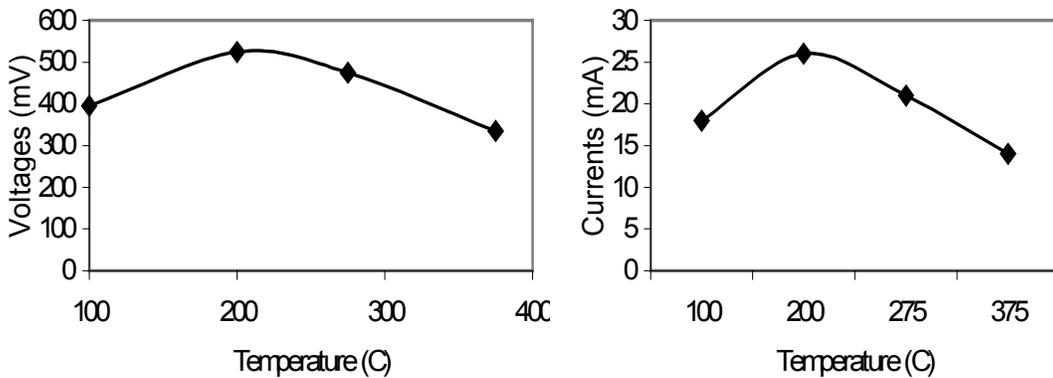
Figure 12. Dependence of Voc and Jsc on substrate deposition temperature for In$_2$Se$_3$.

however, may be In$_2$Se$_3$ growth related. In experiments on glass the properties of In$_2$Se$_3$ were found to be inferior at lower growth temperatures.

As indicated by the Jsc and Voc values in the above plots insights from these experiments have led to improvements in performance. Voc and Jsc profiles for one of our better In$_2$Se$_3$ /CIGS devices are shown in figure 13. The Voc of 525 mV matches the highest value of our CdS reference cells, and while the Jsc's are improved, they are still about 20% below reference cell values.

The Voc profile is plotted in figure 14 relative to the location of the sources for CIGS deposition. Unlike the earlier devices a pattern relative to the sources can now be observed. As can be seen, high Voc's favor low Cu/Group III ratios. The implication is that excess Cu adversely affects the formation and/or performance of the junction region. One possibility that we are considering is the formation of CIS. The band gap of the CIGS absorber for these devices is in the range 1.02-1.05 eV while that of CIS is 0.95 eV. The presence of CIS domains in the space charge region might thus pull down Voc as observed.

While continuing efforts to understand and improve the lower Jsc values we were confronted with what seemed to be persistent instability in device performance. Our standard procedure for CdS buffer layer devices is to measure them right after fabrication without an anneal step. We

475	475	475	475	485
475	485	495	495	495
485	475	505	515	515
485	495	505	515	525
485	495	505	515	515

2.1	2.1	2.4	1.8	1.8
2.1	2.5	1.5	2.0	2.0
2.2	2.7	2.7	2.2	1.9
2.6	3.0	2.9	2.6	2.0
2.5	3.0	2.9	2.8	2.0

Figure 13. Voc and Jsc profiles for an improved In$_2$Se$_3$/CIGS device.

generally find that annealing does not improve performance. The In$_2$Se$_3$ devices were handled in the same way, that is, with no post fabrication anneal.

The results of re-measuring the devices of figure 13 one week later are shown in figure 15. As can be seen, substantial drops in both Voc and Jsc have occurred. This is troubling in light of the fact that our CdS devices seem to be stable. The change in Voc relative to the source locations is shown plotted in figure 16. Note that the orientation is not the same as the above tables. As can be seen, the change to first order seems random and independent of
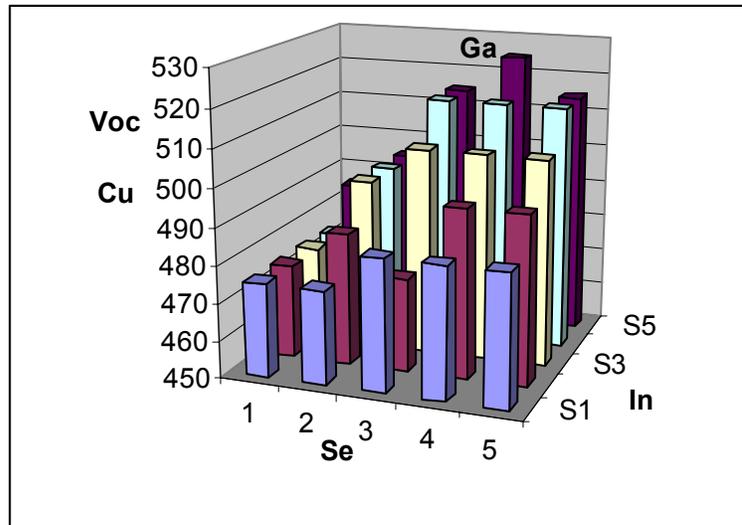
Figure 14. Voc profile for improved In$_2$Se$_3$/CIGS devices.

375	375		255	385
315	415	435	415	365
265		255	375	375
315	355	375	365	345
335	385	355	305	305

1.3	2.0		1.6	1.5
1.4	2.1	2.0	1.8	1.5
1.3		1.3	1.5	1.2
1.8	2.0	2.0	1.7	1.2
2.2	2.4	2.0	1.7	1.3

Figure 15. Performance of In$_2$Se$_3$ buffer layer devices after one week.

location. This is surprising given the reasonably good uniformity of the initial Voc profile. One might expect the effect to be about the same everywhere, or at least favor one of the components suggesting some sort of reaction due to metal stoichiometry. On closer inspection a case might be made for larger change occurring on the In source side. This would be more convincing if the change at position (4, S1) weren't so large.

To better understand these phenomena the devices were submitted to various treatments. These were done also in the hope of eliminating the problem. The effects of light soaking the devices for 10 minutes at one sun intensity are

Figure 16. Profile of the change in Voc after one week.

shown in figure 17. This procedure is commonly used prior to measurement and often produces an enhancement in Voc. As can be seen, the overall effect on both Jsc and Voc is minimal. The small changes observed are likely due to wear and tear on the samples and standard measurement error.

The devices were then annealed at 200 C for 10 minutes in air. The results are shown in figure 18. The anneal resulted in a significant improvement in Voc's, almost back to the original values. However, this was accompanied by furth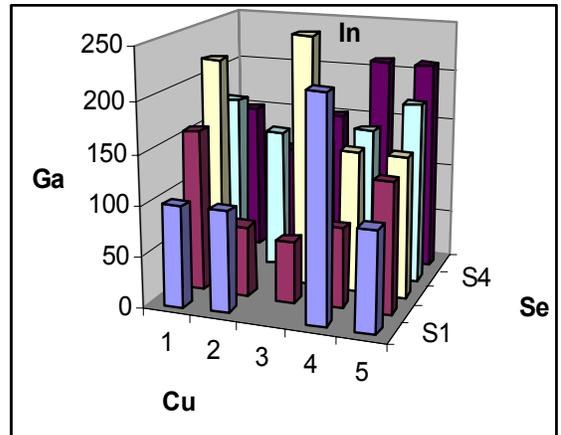er degradation in Jsc values. The results of measuring the sample again a week after the anneal are shown in figure 19. As can be seen, Voc's have all dropped again, and Jsc's continue on a steady degradation path.

These results suggest that two mechanisms are at work. The mechanism that is the dominant control on Voc seems to be reversible, while that leading to ongoing degradation of Jsc is not. In the case of the latter mechanism a plot of the Jsc profile in figure 20 after the anneal step is informative. As can be seen, the biggest losses in Jsc are occurring opposite the Group III sources. This suggests interaction between the In_2Se_3 buffer layer and the absorber. A reasonable hypothesis is that free or improperly bonded Cu on the absorber surface is the source of the problem. There is an ongoing reaction with the In_2Se_3 resulting in the formation of species that impede current flow. Revisiting the above data, it now appears that the 200 C anneal may have accelerated this process while at the same time rejuvenating Voc.

An examination of QE spectra is also helpful in gaining insights to these mechanisms. In figure 21 QE spectra for the initial o and annealed   state of a device are shown. This device is from the Group III - rich corner. As can be seen, in this case the overall current as determined by the integral of the response actually improves a little. However, these spectra were taken without light bias which is significant. As can be seen, after annealing there are two characteristic changes in the features: a strong upward shift in the blue and the appearance of a red tail. The red tail may be evidence for formation of CIS on the surface as suggested above. Also shown in the figure are AMPS simulations for the initial and annealed state. It was found that the red tail could be simulated by converting the top 100 nm from a band gap of 1.07 eV to 0.95 eV. While qualitatively this all seems consistent, there are problems at a quantitative level. Although our devices do have some excess Cu on the surface, it is not apparent that it is enough to form a 100 nm layer of CIS by reacting with the buffer layer.

31

365	345		245	375
315	395	415	415	345
255		255	255	365
305	345	375	375	295
335	355	345	345	295

1.6	1.9		1.5	1.4
1.4	1.9	2.0	1.7	1.2
1.2		1.5	1.4	1.1
1.5	2.0	1.8	1.6	1.3
2.2	2.4	1.9	1.9	1.2

Figure 17. Voc and Isc profiles of In$_2$Se$_3$ devices after light soaking.

445	495	265	465	455
465	485	485	495	465
435	425	455	495	495
475	495	495	495	445
495	505	505	495	485

1.3	1.1	0.5	0.6	0.5
1.3	1.0	0.7	0.6	0.5
0.8	5.5	0.6	0.4	0.4
1.4	0.9	0.6	0.6	0.4
1.9	1.4	0.8	0.8	0.6

Figure 18. Voc and Isc profiles of In$_2$Se$_3$ devices after annealing.

236	381	63	109	279
302	202	291	212	315
277	269	169	276	352
329	362	344	356	268
289	300	360	370	264

0.8	0.8	0.1	0.2	0.3
1.0	0.8	0.6	0.2	0.3
0.8	0.6	0.2	0.2	0.3
0.9	0.7	0.4	0.3	0.2
1.2	0.8	0.7	0.5	0.3

Figure 19. Voc and Isc profiles of In$_2$Se$_3$ devices one week after annealing.

The upward shift in the blue in the QE is also of importance. It was simulated by lowering the electron and hole mobility of the In_2Se_3 layer from 50 to 0.1. This has an effect on the response at high light intensity. That is the QE plot under one sun light bias would indicate lower output which is consistent with IV measurements. Devices away from the Group III – rich area show a more severe downward shift in their QE spectra. The mobility of this region also influences Voc.

We have found through our ongoing efforts to model and simulate CIGS device performance that Jsc is primarily determined by bulk properties. However, there are circumstances that can result in interface influence and sometimes domination of Jsc. On the other hand we find that Voc is primarily determined by interface or near surface phenomena. Only when these are sufficiently subdued are bulk properties a factor. One of the tools that we have used to study Voc phenomena is photocapacitance. We have demonstrated a correlation between Voc and the photocapacitance signal[14], and have used time resolved and wavelength dependent analysis to probe the underlying mechanisms. The technique focuses primarily on space charge layer properties. To first order In_2Se_3 buffer layer devices are expected to have the same SC layer properties as CdS devices. Differences are expected in the In_2Se_3 buffer layer itself. However, the speculated formation of additional layers at the interface due to reaction between Cu and the In_2Se_3 buffer layer provides a target for photocapacitance.

The photocapacitance factor(PCF) which is Clight/Cdark and dark capacitance, Cd, are plotted versus Voc in figure 22. As can be seen, there is no correlation between Voc and PCF.

Figure 20. Jsc profile of of In_2Se_3 buffer layer devices after anneal.
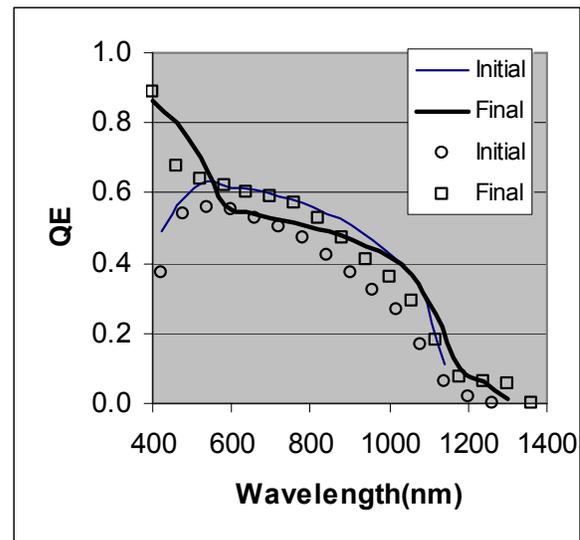
Figure 21. Experimental (symbols) and simulated (lines) QE spectra for In_2Se_3 buffer layer devices in initial and annealed states.

PCF values are usually between 1 and 2, and in this case there are many that are much higher. The dark capacitance, though more well-behaved, also shows no correlation. While not surprising, these results confirm that Voc is dominated by mechanisms other than the space charge layer states that we normally observe.

While not correlated with Voc, the PCF does favor Group III –rich metal ratios as seen in figure 23. A similar propensity was observed for the Jsc degradation mechanism, and as seen in figure 24, there is indeed a correlation. The corresponding plot for dark capacitance is provided in figure 25. This suggests that the dependence for the initial state for the PCF is driven by the dark capacitance. However, the dependence for the annealed state is significantly stronger for the PCF. In all cases an increase in capacitance that would normally correspond to a shrinking
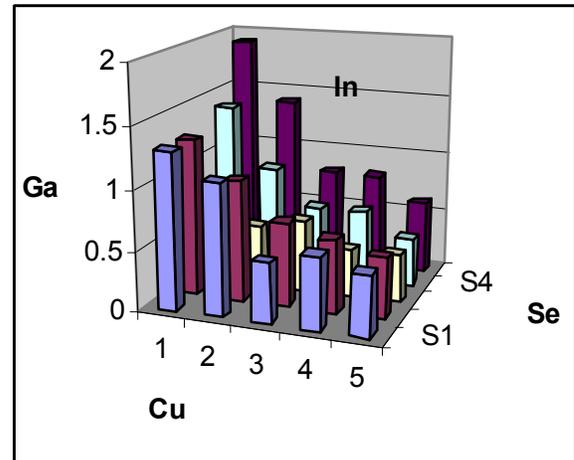
SC width is associated with a higher Jsc. This is opposite of normal behavior and indicates that the capacitance signal is not solely associated with the SC layer. A not unreasonable position is that the capacitance signals are largely controlled by mechanisms in the buffer layer region. This is useful because that is the region that we need to probe to understand the mechanisms associated with instability. What is clear is that as Jsc degrades, so does the PCF. A hypothesis at this point is that the photoconductivity of the buffer layer is controlling current flow. As the transport properties of the buffer layer degrade, proposed to be due to interaction with Cu, current transport through the layer also degrades hurting Jsc. We expect that the photo-mechanism in this case involves dielectric phenomena rather than trapping. Further experiments involving time and wavelength dependent PCF will be required to follow-through on these observations and hypotheses.

Given the above it would seem that the Jsc and Voc mechanisms have their origin in the deposition procedures for the buffer layer. Since In and Se are already present in the absorber, the presence of these in the buffer is not the issue, but rather it must be the manner in which these are combined in forming the buffer layer. As discussed previously, the buffer layers are deposited at 200 C because we have found that temperature sufficient to form stoichiometric In_2Se_3. What we have learned thus far about this stability problem suggests that we try higher deposition temperatures for the buffer layer. This might eliminate the formation of secondary species that affect Voc, though unless we do something else, we might also find significantly reduced Jsc's. To defeat the Jsc mechanism we likely will have to change deposition conditions at the end of absorber formation. We may need lower Cu content than for CdS devices. A combination of these approaches may result in stabilization of these devices that would make In_2Se_3 an attractive replacement for CdS.

Figure 22. Dark capacitance and photocapacitance factor for In_2Se_3 buffer layer devices.
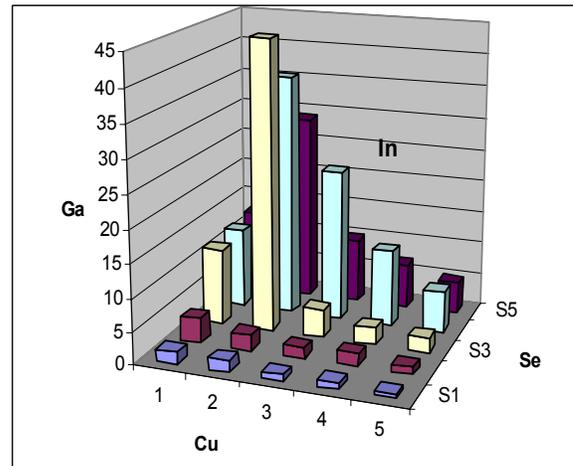
Figure 23. PCF relative to Cu, In, Ga and Se sources.

2.3.3 ZIS

Recently EPV introduced ZIS($ZnIn_2Se_4$) as another potential buffer layer material[15]. After initial evaluation they reported an efficiency of 11.6% that suggested the high potential of this material as a CdS replacement. EPV kindly provided us with sample quantities of the material to use in our ongoing studies of buffer layer phenomena. We were particularly interested in this material in light of the issues raised with In_2Se_3 buffer layers. In particular, this material might provide additional insight to the instability problem and the speculated blame being placed on reactivity with Cu.
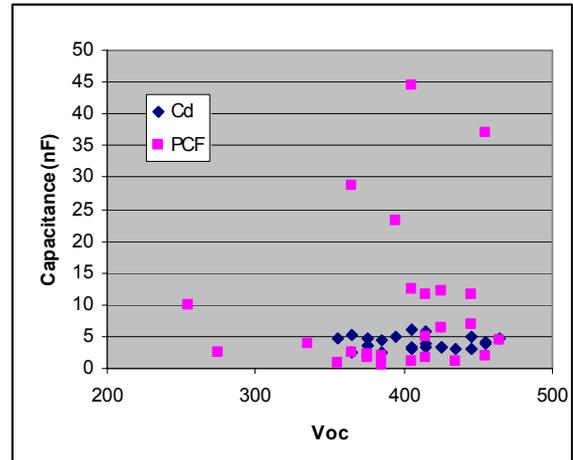
34

ZIS was deposited in the manner prescribed by EPV. An amount was weighed out and placed in an open W boat. The entire amount was then evaporated onto the substrate surface. The deposition rate was held constant at about 0.5 Å/s using a quartz thickness monitor. At the recommended substrate temperature of 200 C we observed fairly uniform output as shown for Voc in figure 26. The Voc's were comparable to CdS controls, but Jsc's were a bit lower. This is similar to the initial evaluation results reported by EPV [15]. Because 200 C is at the high end of the temperature range at which we can safely anneal our devices we tried a lower substrate temperature of 150 C as well. The overall performance was somewhat poorer than at 200 C, but we first were concerned with determining the correct thickness of the ZIS layer. In figure 27 we show Voc and Isc versus ZIS thickness for devices deposited at a substrate temperature of 150 C. Thickness is expressed in terms of the weight of the deposited material. As can be seen, Voc is curiously affected by the thickness indicating a peak at about 27.5 mg. Although an exact calibration was not attempted, this thickness is estimated to be in the typical range of 300 – 500 Å generally used for buffer layers.

Fortunately current shows a similar trend, also peaking at about the same thickness. From experiences with other buffer layers we know that a certain minimum thickness is required, and that beyond that thickness the properties may hold constant and then eventually diminish again as the resistive nature of the buffer layer starts to cause redistribution of voltage. It appears that these same phenomena are at work here, though it is somewhat surprising that Voc would start to drop at increasing thickness.

Figure 24. Dependence of initial and post-annealed Isc on the PCF.
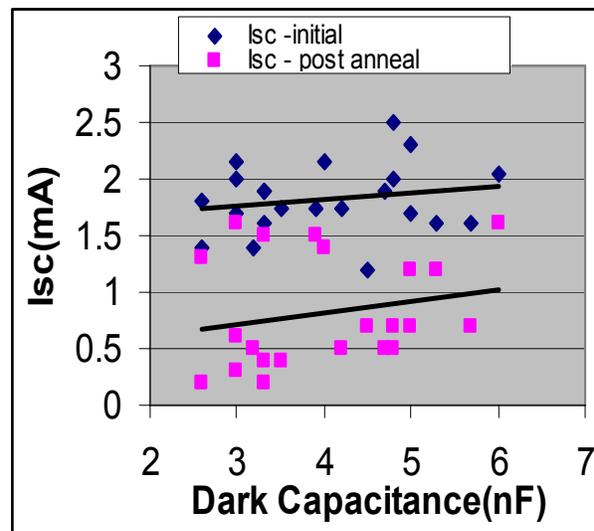
Figure 25. Dependence of initial and post-annealed Isc on the dark capacitance.

Another issue that came to light is the occurrence of abnormally large contact resistance with these devices. Our usual procedure is to do a routine 2-probe initial evaluation of devices right after fabrication and to follow-up with 3-probes for devices of interest. Generally 3-probe measurements merely give a more refined measurement of FF for standard devices. In the case of ZIS buffer layer devices we had difficulty in getting the 3-probe measurement to run. This was determined to be due to high contact resistance with the probes causing the voltage limit of the power supply to be reached. This was puzzling because the same ZnO bilayers were deposited
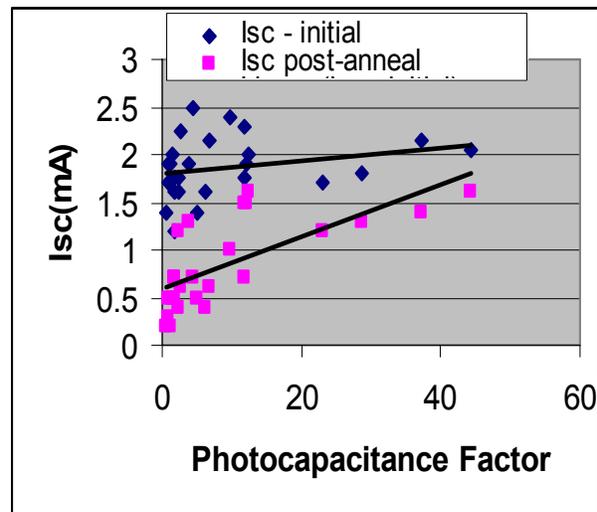
over the ZIS as for our standard CdS devices, and those devices measure normally. After several experiments including leaving out the undoped ZnO layer, varying the ZIS thickness, etc, we are still left with the conclusion that the ZIS layer affects the overlying ZnO layer leading to high contact resistance. This is not a real problem, but only a procedural one. But it nevertheless reminds us of the complexities of these materials and the need for continuing diligence.

Just as the situation above in which ZnO deposited on ZIS behaves differently it is clear that ZIS will behave differently when deposited on various absorbers. All of the results presented here are for our Type II CIGS devices that are more strongly affected by Ga phenomena since they contain more
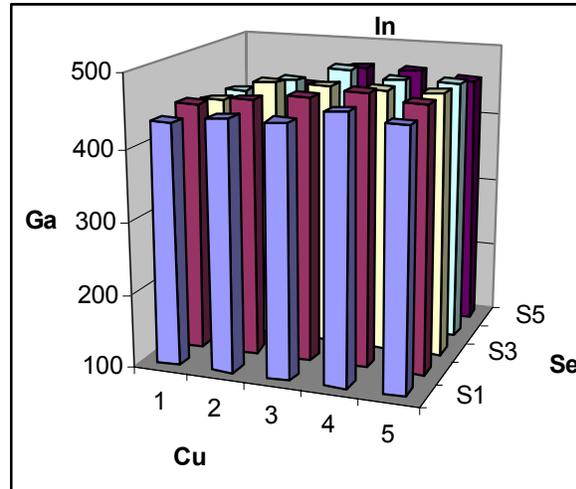
Figure 26. Voc profile for a ZIS buffer layer device for a buffer layer deposition temperature of 200 C.
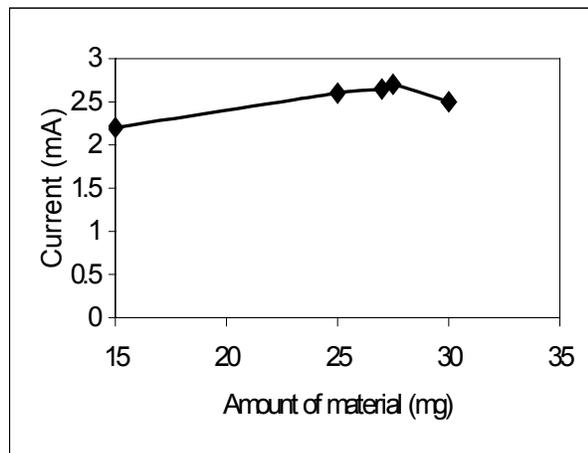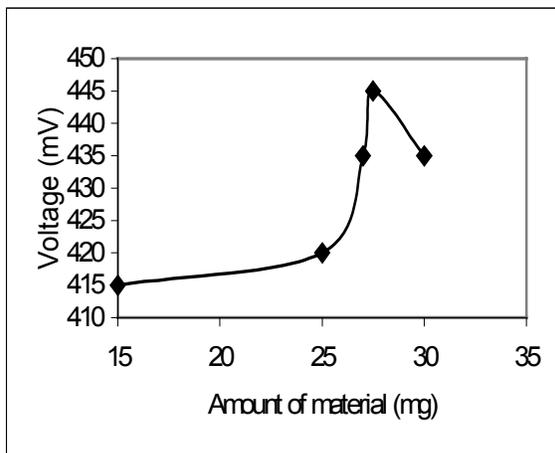
Figure 27. Voc and Isc dependence on ZIS buffer layer thickness for a ZIS deposition temperature of 150 C.

Ga in the space charge layer than our Type I devices. This issue starts to show up when comparing profiles for different ZIS substrate deposition temperatures. In figure 28 we show the Voc profile for a ZIS deposition temperature of 150 C. As can be seen, Voc shows a definite preference for the Group III – rich region at the intersection of the Ga and In sources. This aversion to Cu is similar to what we have reported for In_2Se_3 buffer layer devices and suggests that we might see instabilities similar to those observed for In_2Se_3. However, this is not the case. Thus far ZIS buffer layer devices seem to be stable, though we have not monitored them for an extensive period of time. It is interesting to contrast the profile in figure 28 with that in figure 26 for a ZIS deposition temperature of 200 C. Although we indicated above that the Voc pattern was fairly uniform, a closer look indicates otherwise as seen in figure 29. The average Voc along each column relative to the Ga and Se sources is plotted. As can be seen, in this case there is a definite aversion to Ga. This is not unlike what we observe in CdS devices in which Ga bonding is not optimized. The implication is that this is at least in part an absorber

issue and not solely attributable to ZIS. Thus at the lower substrate temperature of 150 C the ZIS may not form properly and allow intrusion by Cu from the absorber. At 200 C the ZIS forms properly and prohibits interference from Cu. This might suggest that the 150 C devices would be less stable than the 200 C devices. Additional experiments would be required for this determination. The good news nevertheless is that properly deposited ZIS is a viable candidate to replace CBD CdS. The presence of Zn stabilizes it against the Cu attack that In_2Se_3 suffers from, and it is only a bit less straightforward to deposit than In_2Se_3. Its bottom line performance is still somewhat short of CdS, but there is no apparent reason why this cannot be overcome.

Through ongoing studies of these buffer layer materials we are starting to understand the unique role that CdS plays and the specific requirements that must be met by any proposed replacement. For now it continues its hold as the best option just as Mo does for the back contact. We have not, however, uncovered a fundamental reason for its leading performance, so we should continue the pursuit.

2.4 Understanding

Over the course of this project we have looked at a range of materials, including two absorbers, CIGS and CGS, and three alternate buffer layers, ZnO, In_2Se_3 and ZIS. In addition to the standard characterization measurements we have utilized extensive capacitance measurements to probe the effect of defects on performance, and we have employed extensive AMPS simulations to guide and verify our thoughts and ideas. Much of what we have learned and discussed in reports is generic to these materials. However, there is also a large body of knowledge that is associated more specifically with our particular deposition process. Out of this some common themes have emerged. For example, for both absorbers we have achieved state-of-the-art Jsc's, but are still lagging in Voc and FF relative to co-deposition processing. We have argued that Jsc is largely a manifestation of bulk properties, while Voc and FF are largely affected by interface phenomena. These are of course generalizations. Every detail of the deposition process can and often does affect all parameters. Nevertheless, it is appropriate to generalize and conclude that we have not yet mastered the interface properties in our devices. The key question is whether this is a fundamental limitation of the two-step, solid state process, or is it that we have just not yet found the correct pathway? The answer seems to
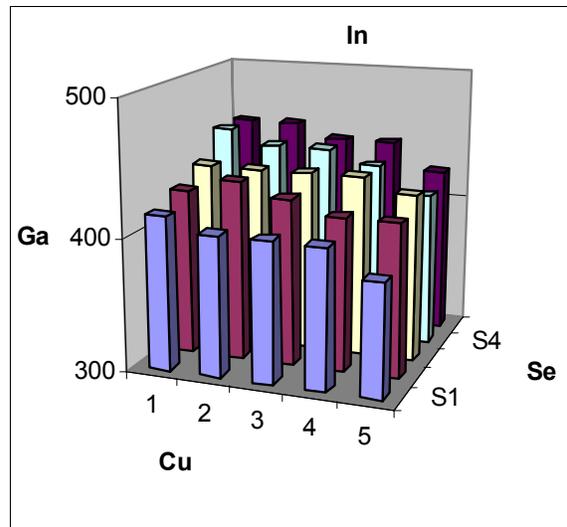

Figure 28. Voc profile for ZIS buffer layer devices for a ZIS buffer layer deposition temperature of 150 C.
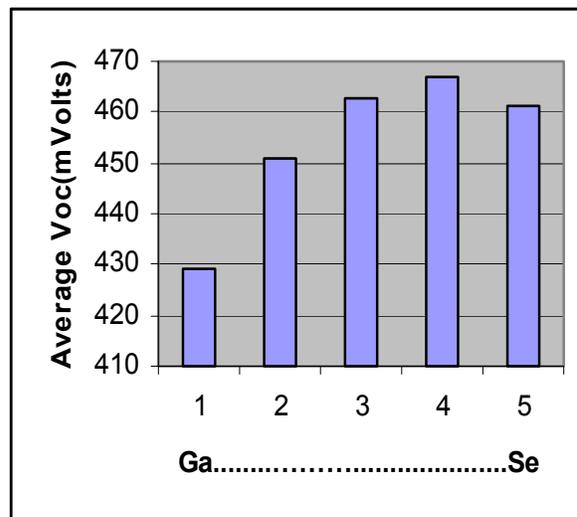

Figure 29. Voc relative to the Ga source for ZIS buffer layer devices with ZIS deposited at 200 C.

lie with use of Se flux as opposed to H_2Se. Since H is not present in the case of co-deposition, its role must be one of proper deliverance of Se to the metal precursor species. As part of a molecule Se is prevented from premature reactions that form unfavorable species in the wrong place. This may not be possible with Se flux. As soon as the Se hits the growth surface, it is free to react as free Se. The overpressure of Se that is needed reflects a low sticking coefficient, though that which does stick reacts at the first opportunity. While we have not identified the exact species that is formed and limits performance, we have made a clear case that it is associated with Ga. *Improperly bonded Ga* is an expression that has been extensively used in our reports. It then seems that errant Ga results from improperly utilized Se. Thus we might conclude that H_2Se simply does a better job of delivering Se to the Ga neighborhood so that it can be properly incorporated into the lattice. Since we have argued that the controlling defective area is the top of the space charge region, we must also include reasons for this in our explanations. Perhaps this is fairly obvious. In order for free and highly reactive Se to penetrate through the entire film it is necessary to provide an overabundance to the growth surface. In such an environment unfavorable Ga species are formed. This does not occur with H_2Se because although Se is available in excess, it is not released from the molecule to form the unsavory species.

With such ideas in mind we have tried all manner of Ga and Se delivery (short of co-deposition) to overcome this limitation. The results of figure 4 in which we achieve a one-one increase in Voc with Eg represent a significant victory in this regard. Ga is bonding properly in the space charge region and near state-of-the-art Voc's are realized. However, in the process of gaining control over the Voc limitation, we added defects that took a toll on Jsc. We can speculate that in this case we didn't over selenize the surface, but paid the price of under selenizing the bulk. In our year 2 Annual Report we show photocapacitance wavelength profiles for devices similar to these that indicate that the controlling defects have indeed moved from the surface into the bulk of the films. While this is generally good for Voc, Jsc and FF suffer, and in fact, these bulk defects can also somewhat lower Voc if surface defects no longer dominate. Somewhere in all of this is a way of controlling both regions together. We have accomplished state-of-the-art properties in both the bulk and surface regions using two-step, all-solid-state processing, but not simultaneously. With further effort and growing insights we expect to develop the process that can put both pieces together, hopefully soon.

Acknowledgements

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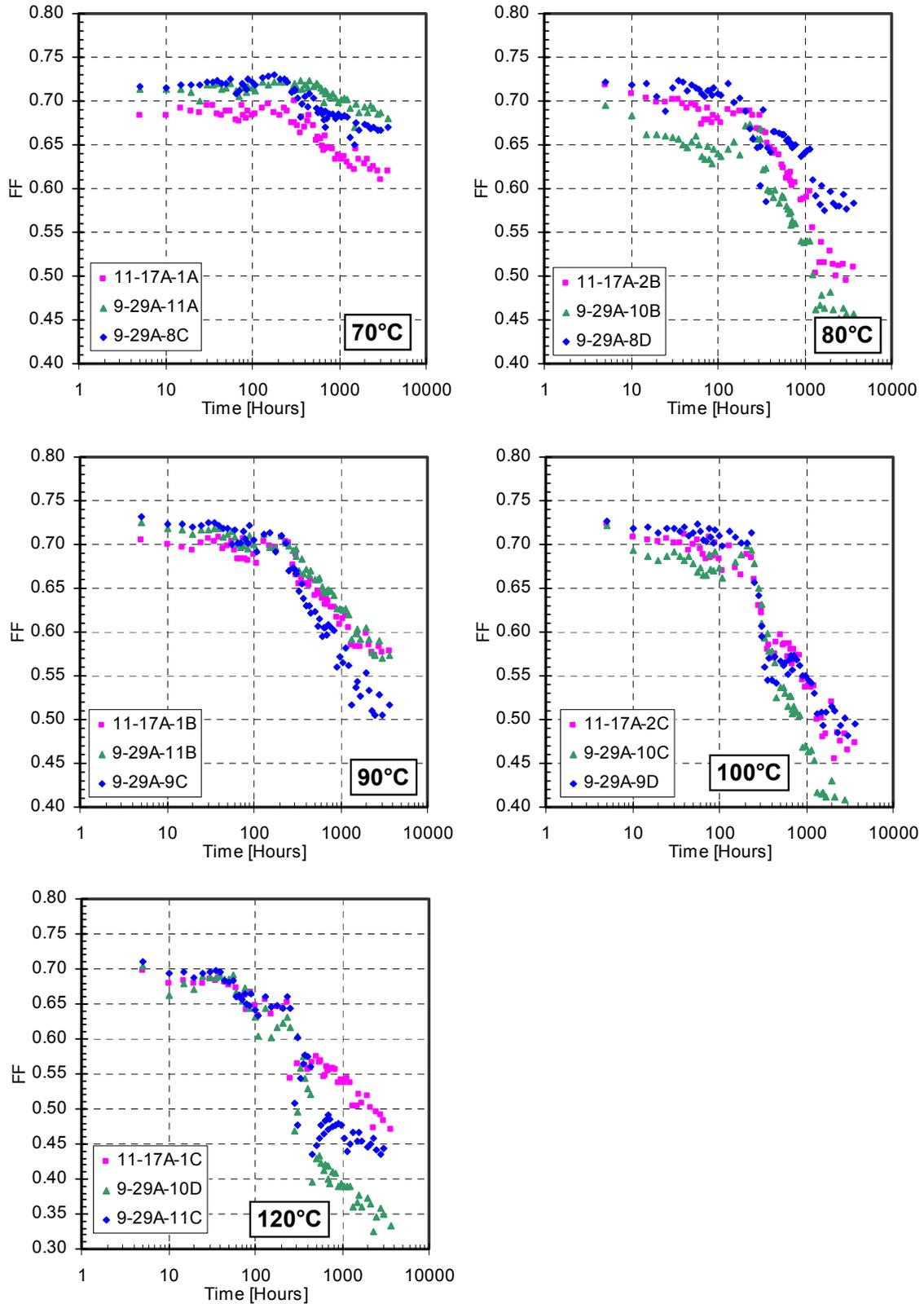
Appendix – A1

V_{OC} of cells stressed at 70, 80, 90, 100, and 120°C for 3600 hours
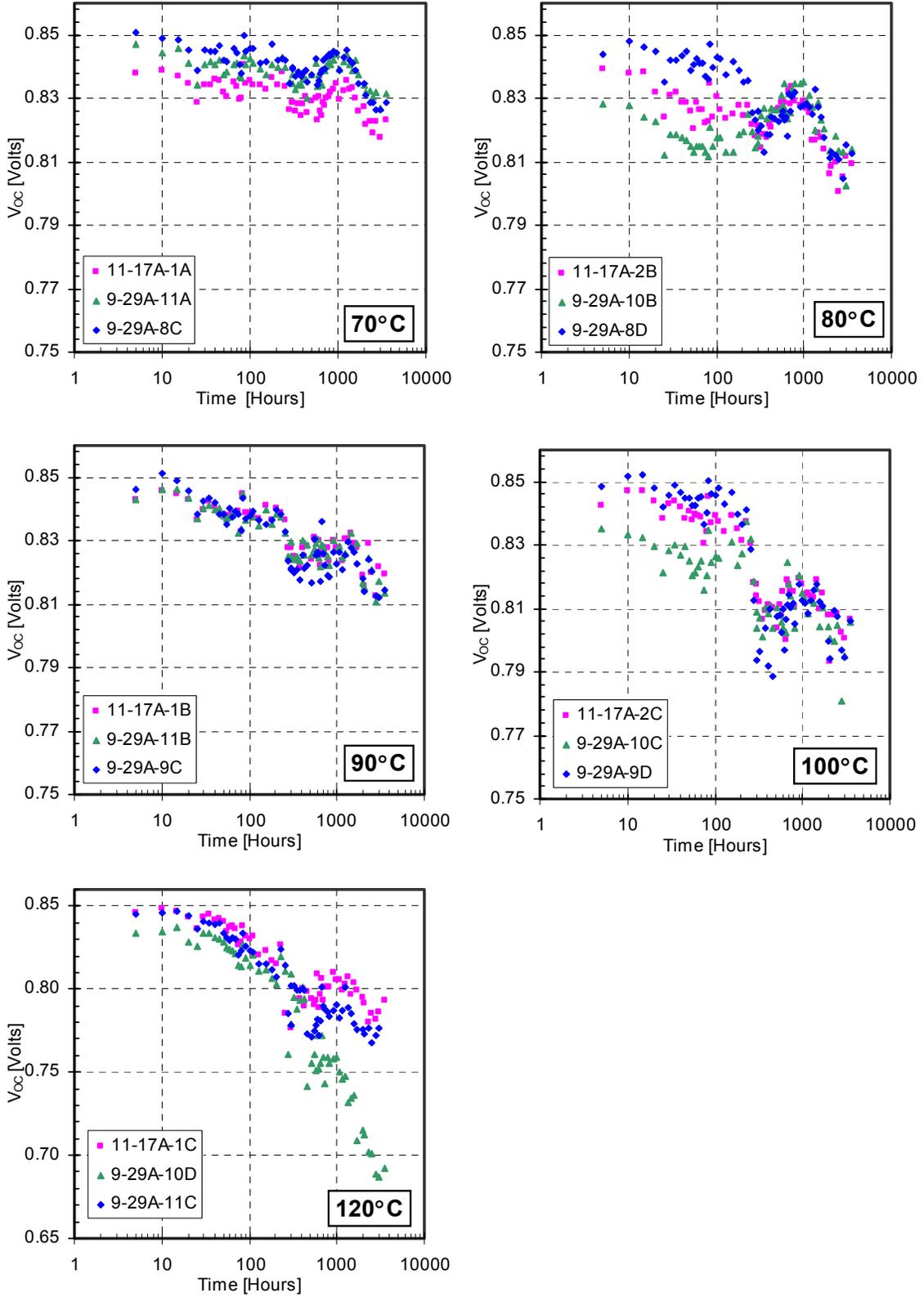
Appendix – A2

FF of cells stressed at 70, 80, 90, 100, and 120°C for 3600 hours

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13. ABSTRACT *(Maximum 200 words)*: This project addresses most of the key CdTe technology areas, with focus on improving the manufacturability and long-term stability of this technology. The activities over this 3-year period include developing simplified processing, studying novel front and back contacts, and improving long-term stability. This report describes work carried out during the last year of the project. The solar cells discussed below are fabricated by various deposition technologies that include chemical vapor deposition, chemical-bath deposition, close-spaced sublimation, and rf-sputtering. The devices are routinely evaluated using standard solar cell analytical techniques such as dark and light current-voltage, spectral response, and capacitance-voltage measurements.

14. SUBJECT TERMS: PV; solar cells; CdTe; long-term stability; chemical vapor deposition (CVD); chemical-bath deposition (CBD); close- spaced sublimation (CSS); rf-sputtering; dark and light current-voltage (J-V); spectral response (SR); capacitance-voltage (C-V) measurements; manufacturability.	15. NUMBER OF PAGES
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