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ABSTRACT

We investigated the electronic properties of ZnO/CdS/CIGS /Mo/SLG polycrystalline thin-film solar cells with compositions ranging from Cu-rich to In(Ga)-rich by deep-level transient spectroscopy (DLTS) and capacitance-voltage (C-V) measurements. This compositional change represents the evolution of the film during growth by the 3-stage process. Two sets (four samples each) of CIGS thin films were prepared with Ga/(In+Ga) ratios of ~0.3 (low Ga) and ~0.6 (high Ga). The Cu/(In+Ga) ratio ranges from 1.24 (Cu-rich) to 0.88 (In(Ga)-rich). The films were treated with NaCN to remove the $Cu_{2-x}Se$ phase where needed. Key results include: (1) For low-Ga devices, DLTS data show that acceptor-like traps dominate in samples where CIGS grains do not go through the Cu-rich to In(Ga)-rich transition, whereas donor-like traps dominate in In(Ga)-rich samples. Therefore, we see a clear transformation of defects from acceptor-like to donor-like traps. The activation energies of these traps range from 0.12 to 0.63 eV. We also observed that NaCN treatment eliminates a deep minority trap in the In(Ga)-rich devices, (2) For high-Ga devices, only majority-carrier traps were detected. These traps again range from shallow to deep, (3) The carrier concentration around the junction and the density of traps decrease as the CIGS becomes more In(Ga)-rich.

INTRODUCTION

$Cu(In,Ga)Se_2$ (CIGS)-based polycrystalline thin-film solar cells are promising for photovoltaic applications. The highest conversion efficiency for small laboratory devices is 19.2% [1]. The four elements of this multinary polycrystalline film can be alloyed to form different CIGS phases as dictated by the pseudo-binary CIS phase diagram [2]. Even though this multiplicity makes the material complicated, CIGS nevertheless tolerates defects and impurities by self-adjusting its chemistry and microstructure. In our laboratory, we are investigating the thin-film growth mechanisms using our so-called "3-stage process" as influenced by the specific dynamics of this process. The electronic properties of thin-film $Cu_xIn_{1-y}Ga_ySe_2$ devices made from films as they transition from Cu-rich to In(Ga)-rich, and for different Ga contents (i.e., different y values), are the subject of this work. Devices made from these films were analyzed using deep-level transient spectroscopy (DLTS) and capacitance-voltage measurements (C-V).

The phase and microstructure evolution of $Cu(In,Ga)Se_2$ from Cu-rich to In(Ga)-rich with the addition of Cu has been discussed in our previous publications (e.g. ref. [3]).

For comparison of our results with previous studies, see references [4,5].

EXPERIMENTAL

The CIGS thin films were deposited on Mo-coated soda lime glass substrates by physical vapor deposition in a multisource bell jar system using the three-stage process (see Figure 1). In this process, a precursor of $(In,Ga)_2Se_3$ is reacted with Cu+Se to produce $Cu(In,Ga)Se_2$ plus $Cu_{2-x}Se$ as a secondary phase, followed by the addition of In+Ga+Se to adjust the composition to slightly Cu-poor.

Our approach is to interrupt the film growth at predetermined points along the film growth pathway. The thin-film samples from which the devices were made are labeled **a** through **d** and are indicated in Figure 1. Sample **a** is Cu-rich and sample **d** is In(Ga)-rich. Thin-film samples **a**-**d** were treated by NaCN for about 5 min to remove the $Cu_{2-x}Se$ secondary phase where needed. Devices were made from these NaCN-treated thin-film samples. CdS was deposited by CBD and ZnO, and the front contacts were deposited by sputtering. Other devices were made from the untreated In(Ga)-rich thin-film sample (which will be referred to as **d**').

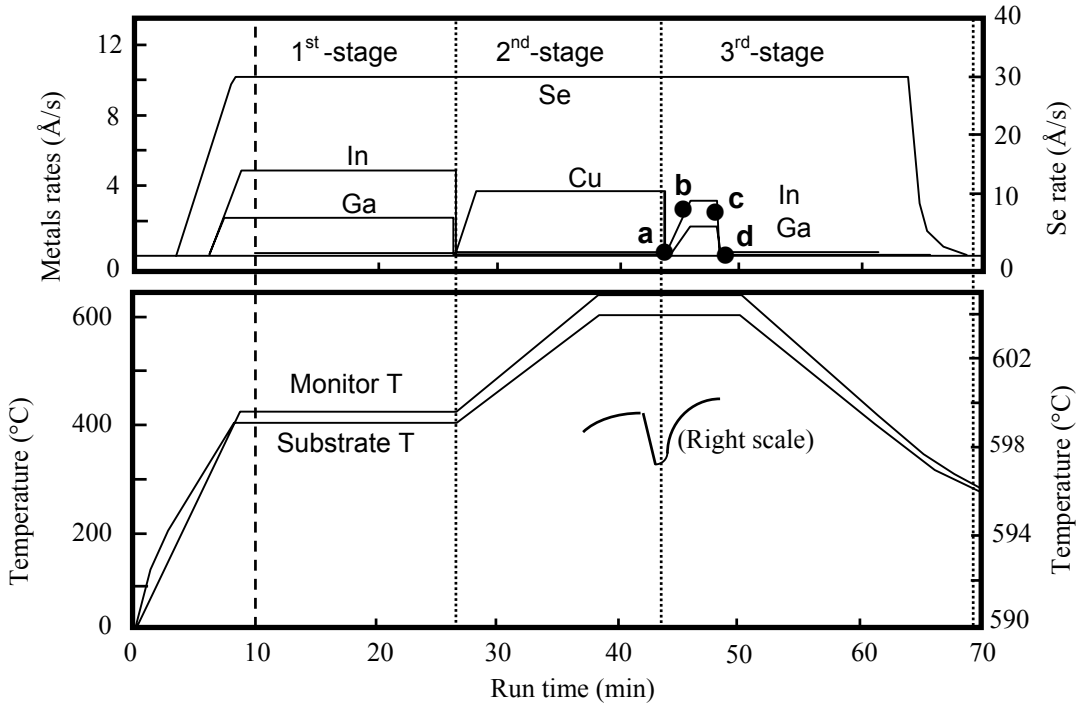


Figure 1. Schematic profile of the "three-stage growth process.

RESULTS AND DISCUSSION

(I) Low Ga Samples

The electronic properties of ZnO/CdS/$Cu_xIn_{1-y}Ga_ySe_2$ (CIGS)/Mo/SLG polycrystalline thin-film solar cells made from samples **a** through **d** (where the film transitions from Cu-rich to In(Ga)-rich) were investigated by DLTS and C-V measurements. For DLTS measurements, carriers are introduced using a bias pulse, changing the electron occupation of a trap. The junction capacitance increases as the electron occupation of the trap increases [6]. In this study, we used the DLTS technique to measure the activation energy (which is approximately the energy distance from the respective band to the trap level) and the trap concentration. The DLTS spectra were measured with a reverse voltage V=-0.4 V, trap-filling pulses of amplitude 0.5 V, and a saturation pulse width of 1 ms. Figure 2a shows the DLTS data for low-Ga (i.e. Ga/(In+Ga)=~30%) samples **a-d'**. For sample **a**, the signal shows a negative peak (at T=~120 K), identifying the shallow defect A_1 as a hole trap with activation energy of 0.12 eV from the valence band. Also, it shows a beginning of a positive peak (at $T \cong 300$ K), identifying a defect D_1 as a deeper electron trap. For sample **b**, the signal shows a negative peak (at $T \cong 210$ K), identifying a defect A_2 as a hole trap with activation energy of 0.28 eV from the valence band. For sample **c**, the signal shows a positive peak (at $T \cong 230$ K), identifying a defect D_2 as an electron trap with activation energy of 0.47 eV from the conduction band. For sample **d**, the signal has two positive peaks (at temperatures of about 120 and 260 K, respectively), identifying the defects D_3 and D_4 as electron traps with activation energies of 0.12 and 0.25 eV, respectively, from the conduction band. For sample **d'**, the signal shows a positive peak (at $T \cong 230$ K), identifying a defect D_5 as an electron trap with activation energy of 0.63 eV from the conduction band. Comparing samples **d** and **d'**, we see that NaCN treatment eliminates a deep minority trap in the In(Ga)-rich devices. The heights of the peaks in Figure 2 are proportional to their respective trap concentration [6]. The traps in samples **a-d'** have densities in the range $6.6 \times 10^{11} - 2.0 \times 10^{14}$ cm^{-3}. The low values of the trap densities may be due to the incomplete filling of the traps.

Figure 3(a) shows the C-V measurements. The average carrier concentrations (N values) were deduced from Figure 3b. These concentrations were found to be: 4.8×10^{16}, 7.5×10^{15}, 4.8×10^{15}, 7.9×10^{16}, and 1.4×10^{16} cm^{-3} (for samples **a**, **b**, **c**, **d**, and **d',** respectively, see Figure 1).

(II) High Ga Samples

Now, consider the high-Ga (i.e., $Ga/(In+Ga) \approx 0.6$) samples **a-d'**. Figures 4 (a) and (b) show the DLTS data and Arrhenius plots for these samples, whereas figure 4(c) shows the C-V data. Some of the traps were seen using a rate window of 20 ms, however to see the other traps, shorter rate windows were used; thus, two DLTS plots are shown in figure 4 (a). All the DLTS peaks for these samples are negative, and therefore belong to majority (or hole) traps. Traps A_3, A_4, A_5, A_6, A_7, A_8, A_9, and A_{10} (figure 4) have activation energies of 0.09, 0.72, 0.07, 0.25, 0.23, 1.17, 0.84, and 0.57 eV, respectively. The activation energies are measured relative to the valence band. The traps have densities in the range of $0.12 - 24 \times 10^{14}$ cm^{-3}. The carrier

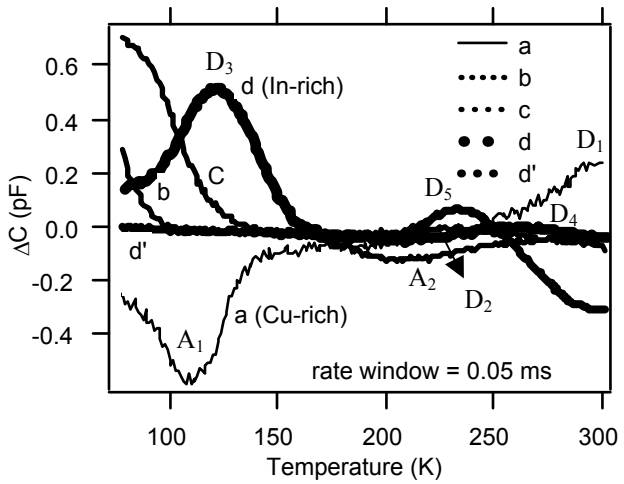


Figure 2a. DLTS data for samples (**a-d'**). (**'**) before NaCN treatment.

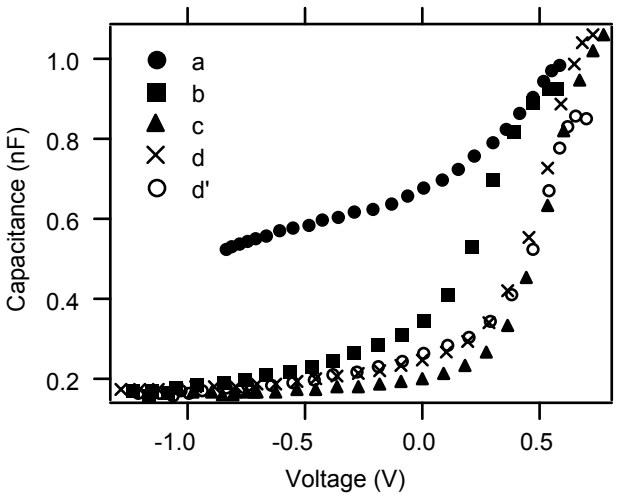


Figure 3a. C-V data for samples **a-d'**.

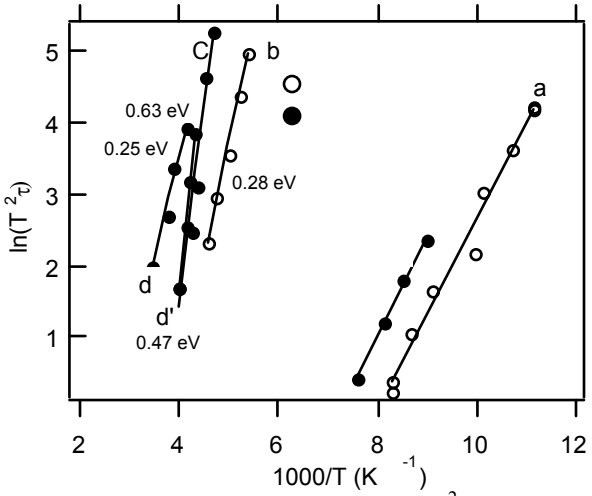


Figure 2b. Arrhenius plots of $\ln(T^2\tau)$ vs. 1000/T for samples (**a-d'**). (T: temperature, τ: time constant).

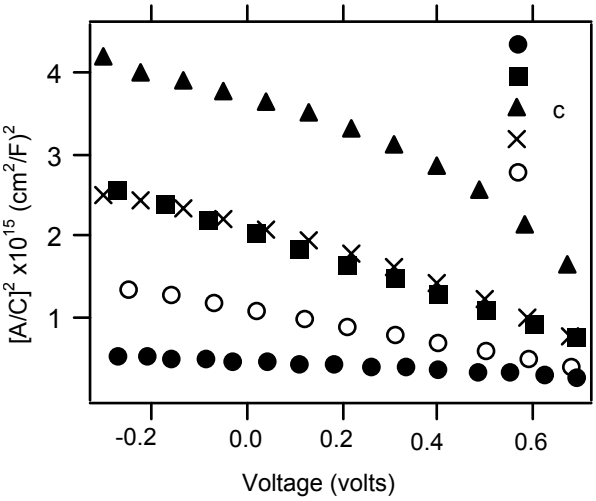


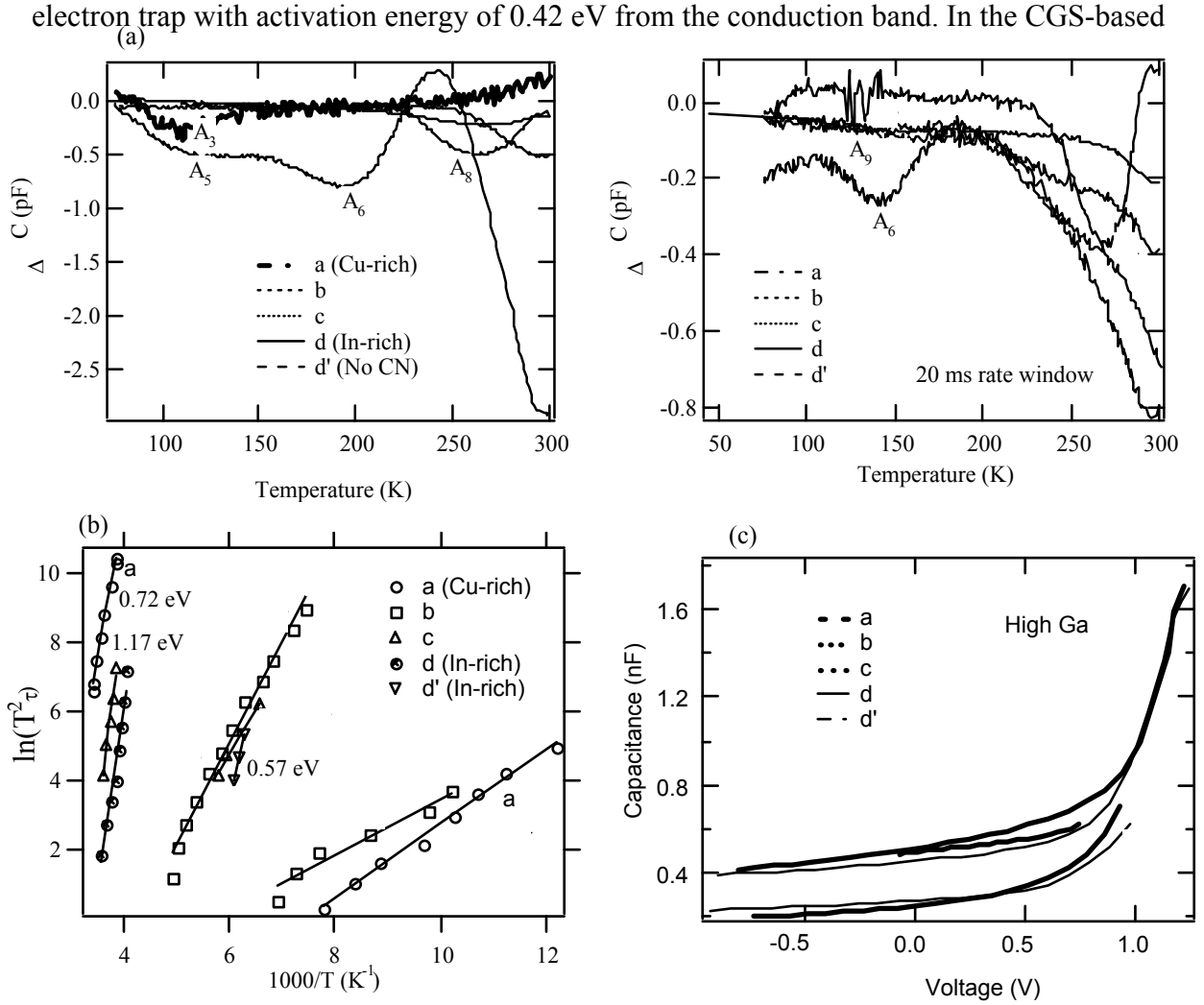
Figure 3b. $[A/C]^2$ vs. applied voltage for samples (**a-d'**). (A: area, C: capacitance)

concentrations around the junction of the cell (from C-V) for samples **a-d** and **d'** are in the range of $0.14 - 4.8 \times 10^{17}$ cm^{-3}. These concentrations are one order of magnitude higher than in the low Ga case. The carrier concentration is the highest for sample **a** and decreases as the film becomes more In(Ga)-rich. This is true for low- and high-Ga cases.

(III) CIS and CGS Samples

We also fabricated CIS- and CGS-based devices and analyzed them using DLTS and C-V. The CIS-based device has a new world-record efficiency of 14.5% [7]. In this device,

we detected a hole trap with activation energy of 0.17 eV from the valence band and another electron trap with activation energy of 0.42 eV from the conduction band. In the CGS-based



Fi.gure 4. (a) DLTS data, (b) Arrhenius plots of ln ($T^2\tau$) vs. 1000/T, and (c) C-V data for high-Ga samples **a-d** and **d'**.

device, which has an efficiency of about 8%, a hole trap with activation energy of 0.22 eV from the valence band was detected.

Figure 5 shows the relative defect density for CGS, and low- and high-Ga devices for the different defect states shown in figures 2 and 4 above. The defect density is the highest for sample **a** and decreases as the film becomes more In(Ga)-rich.

Conclusions

(1) For low-Ga devices, both acceptor-like traps dominate in samples where CIGS grains do not go through the Cu-rich to In(Ga)-rich transition, whereas donor-like traps dominate in In(Ga)-

rich samples. Therefore, we see a clear transformation of defects from acceptor-like to donor-like traps. The activation energies of these traps range from 0.12 to 0.63 eV. We also observed that NaCN treatment eliminates a deep minority trap in the In(Ga)-rich devices. (2) For high-

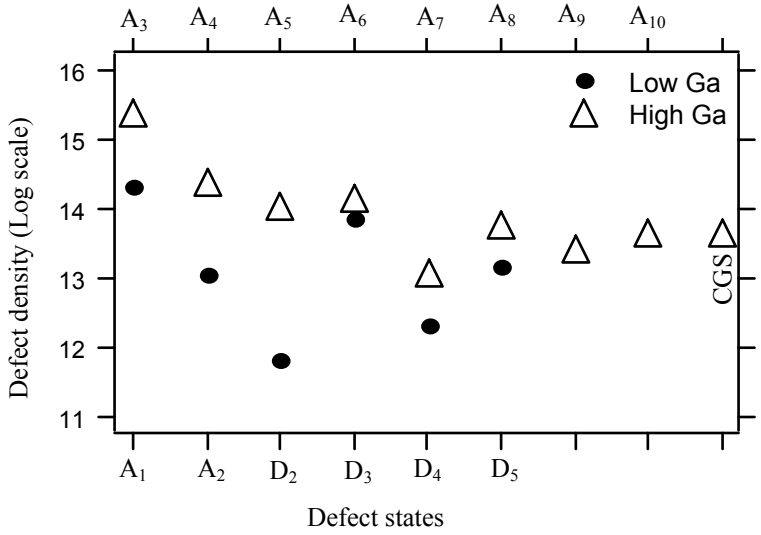


Figure 5. Defect densities (logarithmic scale) for the different defect states shown in figures 2 and 4 above.

Ga devices, only majority-carrier traps were detected. These traps again range from shallow to deep. (3) The carrier concentration and the density of point defects decrease as the CIGS becomes more In(Ga)-rich.

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REFERENCES

1. K. Ramanathan, M. Contreras, C. Perkins, S. Asher, F. Hasoon, J. Keane, D. Young, M. Romero, W. Metzger, R. Noufi, J. Ward, and A. Duda, *Prog. Photovolt: Res. Appl.* **11**, 225 (2003).
2. U.C. Boehnke and G. Kuhn, *J. Mat. Sci.* **22**, 1635 (1987).
3. Jehad AbuShama, R. Noufi, Y. Yan, K. Jones, B. Keyes, P. Dippo, M. Romero, M. Al-Jassim, J. Alleman, and D. Williamson, *Mat. Res. Soc. Symp.* **668**, H7.2.1 (2001).
4. A. Jasenek, U. Rau, V. Nadenau, and H. W. Schock, *J. Appl. Phys.* **87**, 594 (2000).
5. R. Herberholz, M. Igalson, and H. W. Schock, *J. Appl. Phys.* **83**, 321 (1998).
6. D. V. Lang, *J. Appl. Phys.* **45**, 3023 (1974).
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