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Silicon Materials Research on Growth Processes, Impurities, and Defects

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ABSTRACT

Research progress on silicon crystal growth processes for photovoltaic applications and defect and impurity effects on PV performance is presented. Growth processes, in addition to thin-film silicon growth, include techniques for silicon-feedstock generation and a method for rapid, replenished Czochralski growth. We have produced research samples of silicon with low and very high dislocation densities for collaborative research with other institutes, and have also made samples with varying amounts of incorporated nitrogen and oxygen, again, for collaborative studies with university researchers, concerning the effects of these impurities on mechanical strength. Transition-metal doping of silicon for understanding metallic impurity effects on lifetime and cell performance is ongoing.

1. Si Feedstock via Deposition on Tubular Substrates

Under a cooperative research and development agreement (CRADA) between GT Equipment Technologies (GTi) and NREL, we have installed a prototype silane chemical vapor deposition (CVD) reactor made by GTi, as well as the infrastructure facilities, enclosure, sensors, and electronic control for its safe operation with silane. Experiments will begin shortly to demonstrate a process for depositing high-purity silicon feedstock from silane on large tubular substrates instead of conventional thin rod substrates. The larger starting surface area is expected to translate to shorter deposition times.

Figure 1. Silane CVD reactor for Si growth on tubes.

2. Si Feedstock from Phosphorous Industry Wastes

We completed the first phase of an International Science Technology Center (ISTC) collaborative project with the Institute of Physics and Technology, Almaty, Republic of Kazakhstan. In this project, aluminothermic reduction of silica from phosphorus industry wastes yielded silicon powder with phosphorus and boron concentrations 2 ppm and 8-10 ppm, respectively. The calcium content was <0.06 ppm and the aluminum concentration was 7 ppm. Other metal impurities were present at <0.1 ppm. This material provides a good starting point for further upgrading to solar-grade silicon.

In another variant of the process, low-cost and highly reactive silicon alloys were discovered, which produce silane on hydrolysis with acid aqueous solutions under normal environmental conditions and without any catalyst. This method of silane synthesis has the advantages of a simple chemistry of reaction and easy removal of water as the main impurity. It is remarkable that boron, one of the most difficult-to-remove impurities in silicon, is present in the synthesized silane only in trace amounts. Both variants of the reduction process (resulting in silicon or silane-producing silicon alloys) require minimal energy input due to the highly exothermic character of the reactions.

3. A New Process for Replenished Czochralski Growth

To test a new Czochralski (CZ) growth configuration [1] using a continuously replenished shallow melt of small volume as shown in Fig. 2, we've acquired a crystal growth furnace (Fig. 3). Expected benefits of the new process include reduced melt convection, smaller temperature fluctuations, lower oxygen content, lower density of microdefects, smaller variations in microscopic doping density, a tighter resistivity range from ingot top to bottom, relatively constant thermal conditions, higher growth rate (higher productivity), more controllable interface shape, faster turnaround between crystal ingots, minimal loss of feedstock materials if a growth run fails, a deepened periphery to stabilize the shallow melt, and thermal isolation between growth and feed melt compartments.

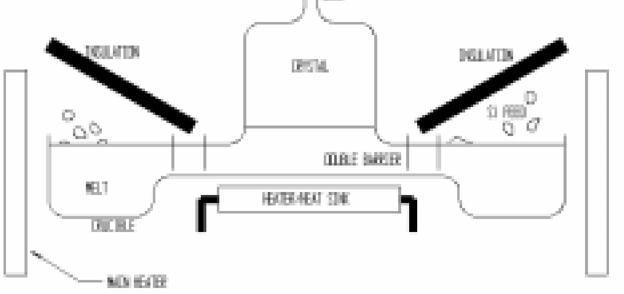

Figure 2. Schematic of a continuous CZ growth configuration.

Figure 3. CZ furnace in the NREL Crystal Growth Labs.

Modeling of the new configuration has begun in collaboration with the State University of New York at Stony Brook. Some preliminary results are shown in Fig. 4. They indicate that the new system can meet the requirements of convection suppression and continuous crystal growth [2].

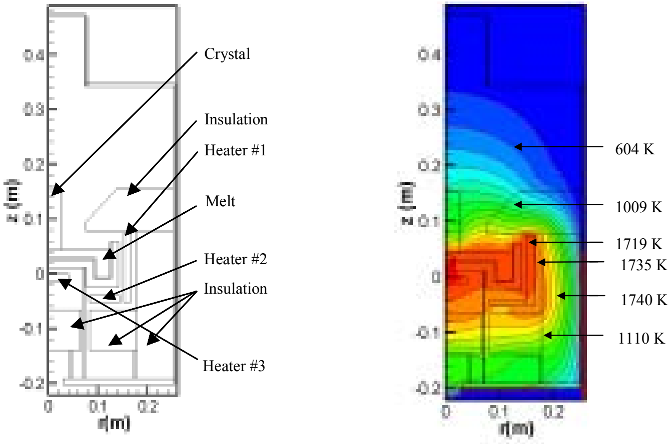

Figure 4. Some preliminary modeling results for the new CZ growth process.

4. Thin-Layer Si Growth by Atmospheric Pressure Iodine Vapor Transport (APIVT)

Direct deposition of large-grain poly-Si thin layers on glass-ceramics substrates

We have developed the APIVT technique to directly deposit large-grain (~20 µm) polycrystalline silicon thin layers at a fast rate (~3 µm/min) at moderate temperatures of about 900ºC on non-silicon substrates such as mullite and Corning LGA-139$^{®}$glass-ceramics. The average grain size obtained by APIVT is about ten times that achievable by a typical chlorosilane CVD process at similar temperatures. With optimized growth conditions, we are able to eliminate gas-phase nucleation that leads to spurious growth in the bulk and on the surface of silicon films. A smoother surface and nearly isotropic growth characteristics are also obtained, as shown in Fig. 5, compared to films grown earlier.

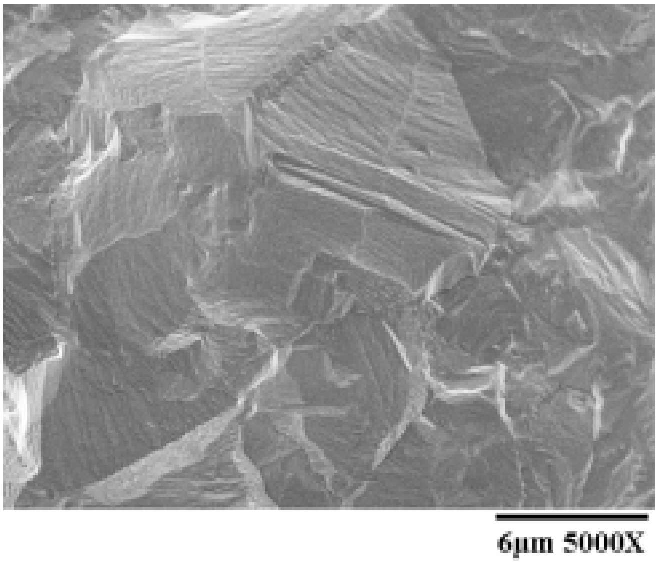

Figure 5. Plan view of recent APIVT growth with smoother surface and more-conformal grain boundaries.

Epitaxial growth on low-cost metallurgical-grade (MG) -Si seeded substrates

Low-cost MG-Si seeded substrates can be made by a variety of means such as the Silicon-on-Ceramics coating process developed many years ago at Honeywell with mullite substrate cost at $< \$6/\mathrm{m}^2$, or stand-alone MG-Si substrates at a material cost of $< \$5/\mathrm{m}^2$ with AstroPower's patented sheet process. Figure 6a shows a 1-mm-wide portion of the surface of a MG-Si film dip-coated on graphite, which has dendritic growth features with grain sizes on the order of hundreds of microns. Epitaxial growth on MG-Si seeded substrates could result in very large grain sizes so that a much less stringent passivation process is needed, as shown in Fig. 6b (0.5 mm in width). The fast and inexpensive APIVT technique achieves silicon epitaxy with relative ease by maintaining a clean interface. In the current experimental system, this is accomplished by heating the substrate to above 1000°C before actual growth starts. During growth, the substrate temperature was lowered to 900°C to minimize impurity contamination from an impure MG-Si substrate. The surface morphology strongly depends

Figure 6. (a) MG-Si film dip-coated on graphite; (b) Large-grain APIVT film grown on an MG-Si substrate.

on orientations of the individual grains and the growth temperature. Higher temperature favors a smoother surface, as usual.

6. Low and High (Mosaic) Dislocation Densities in Si

Multicrystalline silicon exhibits a wide range of dislocation densities grain-to-grain and sometimes within a single grain. Even low densities of dislocations can interact with metal contaminants to compromise photovoltaic (PV) properties. And in the extreme case, there are infamous "bad" regions characterized by unusually high dislocation densities. We have undertaken the task of replicating some of these dislocation situations with pure silicon in the float-zone (FZ) process and will be extending the work to grow samples with both dislocations and controlled transition-metal contamination or doping. The resulting samples are of interest to a number of university research collaborators. Low dislocation density samples are produced by seeding the growth and very gradually tapering to larger diameters to increase dislocation density, as shown in the North Carolina State University (NCSU) topograph of Fig. 7.

Figure 7. X-ray topograph of a dislocated Si crystal.

We were also able to produce pure Si single-crystals of extremely high dislocation density by thermally stressing the crystals in the growth furnace. This leads to a mosaic structure of dislocations forming along low-angle grain-boundary cells, as shown in Fig. 8, with average dislocation densities > 1 x 10^6 cm^{-2}. In addition to their use in PV materials studies, samples such as this are of high interest for broadband radiation detectors in the medical imaging community.

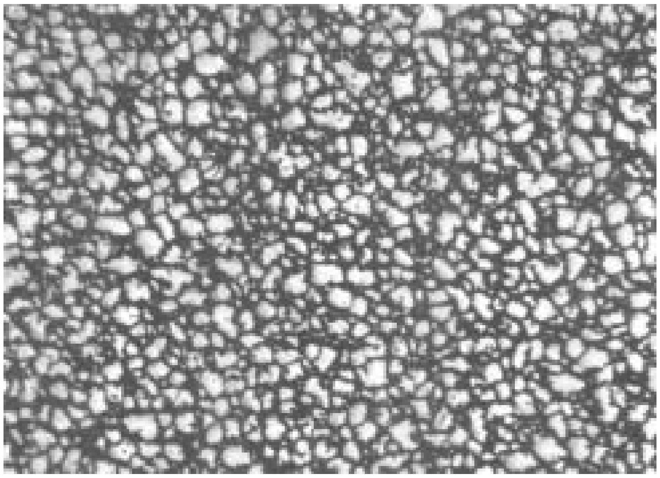

Figure 8. Photomicrograph showing a dislocation-etched, 2-mm-wide region of a pure FZ crystal severely stressed in the growth furnace, leading to a mosaic structure.

7. Impurity Doping Studies in Silicon

Controlled doping is required for a number of materials studies in silicon ranging from transition-metal impurity effects on minority-charge-carrier lifetime and photovoltaic performance to the role oxygen and/or nitrogen play in determining the mechanical strength of silicon wafers. To avoid extraneous impurities from crucibles and heaters, the FZ growth method is preferred. To obtain uniform axial dopant profiles in FZ growth, the equations governing solute redistribution dictate that impurities with segregation coefficient k near 1 must be added continuously during crystal growth, while impurities with k << 1 should be added only at the start of the crystal segment. Dopant sources can be gaseous, liquid, or solid. Gas-phase dopants can be problematic for reasons of toxicity (e.g., diborane, phosphine) or reactivity with the solid growing crystal (e.g., N_2, O_2, CO_2).

We have had success with solid-source doping for low concentrations of O and a range of concentrations of N in dislocation-free FZ growth. The method consists of inserting a solid form of the dopant, for example, a high-purity quartz rod, into the molten zone during growth, as shown in Fig. 9. The surface area of the solid source, melt-zone volume, crystal diameter, and growth rate determine the O concentration. An example follows of simultaneous low O-doping and microdefect generation. A 3-mm-diameter quartz rod inserted about 5 mm into the melt zone of a dislocation-free, swirl-defect-free silicon crystal growing at 4 mm min^{-1} provided about 8 x 10^{16} cm^{-3} O.

Figure 9. Solid-source oxygen doping of a 34-mm-dia., dislocation-free FZ Si crystal using a high-purity quartz rod.

Slowing the growth rate to 2 mm min^{-1} lowered the O concentration slightly to 7 x 10^{16} cm^{-3} and introduced the classic swirl pattern of silicon self-interstitial defects, as shown in Fig. 10 for a Secco-etched wafer from the 2 mm cm^{-3} growth-rate region. These samples are part of a set used in a collaborative SiWEDS (Silicon Wafer Engineering and Defect Science) project with NCSU focused on microdefect/oxygen interactions and wafer mechanical strength.

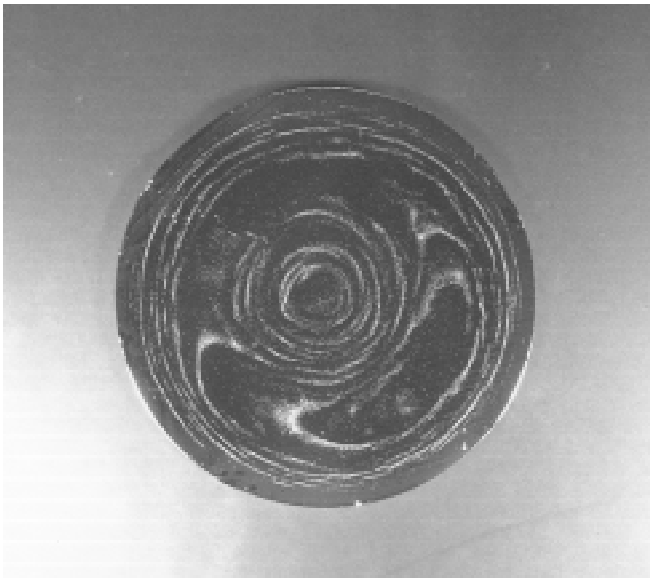

Figure 10. Silicon self-interstitial swirl-defect pattern on a FZ (100) wafer grown at 2 mm min^{-1} with 7 x 10^{16} cm^{-3} O. A companion crystal section grown at 4 mm min^{-1} is swirl-free.

8. Summary and Discussion

Silicon materials research activities are ongoing in the areas of silicon feedstock, new growth processes, thin-layer silicon growth, dislocation and microdefect effects on material performance, and controlled impurity doping studies with O, N, and transition metals, as well as combinations of these with and without defects. Some highlights from each R&D area were presented. Further information can be found at http://www.nrel.gov/silicon.

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[2] C. Wang, H. Zhang, T.H. Wang, and T.F. Ciszek, "A Continuous Czochralski Silicon Crystal Growth System," 14th American Conf. on Crystal Growth and Epitaxy, Seattle, Aug. 4-9, 2002, to be published in J. Crystal Growth.

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