October 2002 • NREL/SR-520-32883

Subcontractor Report

Apollo® Thin Film Process Development: Final Technical Report

April 1998—April 2002

D.W. Cunningham
BP Solar
Fairfield, California

National Renewable Energy Laboratory

1617 Cole Boulevard
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NREL Technical Monitor: Harin S. Ullal

Prepared under Subcontract No. ZAK-7-17619-27

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1. Introduction

The Thin Film PV Partnership program, subcontract ZAK-8-17619-27, was started in May 1998. This report describes the approach and findings of the work performed over this period.

Figure 1. The BP Solar CdTe Thin Film Facility at Fairfield, California

BP Solar first started investigative work on CdTe photovoltaic in 1986. The module product name chosen for the CdTe devices is Apollo®. The deposition method chosen was electro-chemical deposition due to its simplicity and good control of stoichiometric composition (1-2). The window layer used is CdS produced from a chemical bath deposition. Initial work focused on increasing photovoltaic cell size from a few mm^2 to 900 cm^2 (3-5). At BP Solar's Fairfield plant, work is focused on increasing semiconductor deposition to $1m^2$ (6-7). The primary objective of this subcontract is to establish the conditions required for the efficient plating of CdS/CdTe on large area transparent conducting tin oxide coated glass superstrate.

The initial phase concentrates on superstrate sizes up to $0.55m^2$. Later phases will include work on 0.94 m^2 superstrates.

The tasks in this subcontract have been split into four main categories.

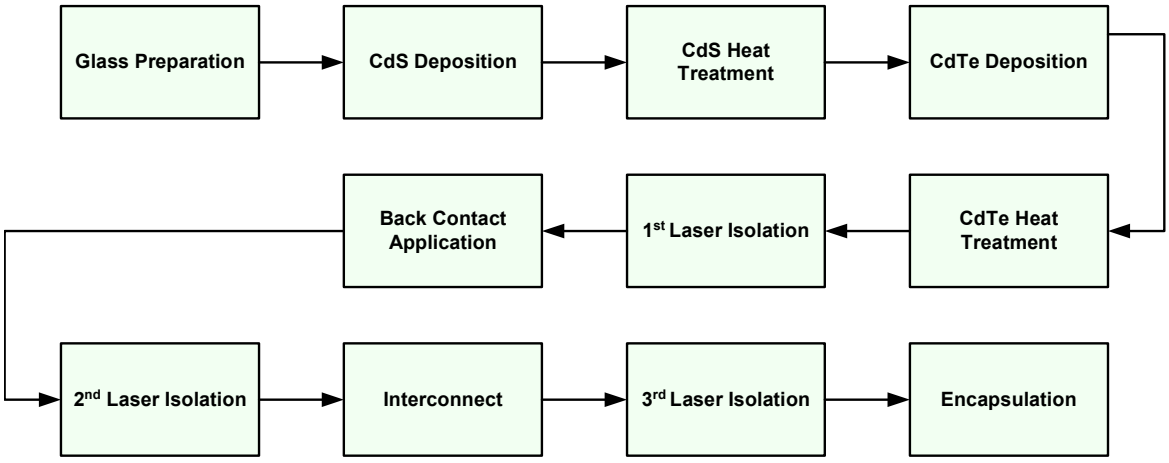
- CdS and CdTe Film Studies.
- Enhanced Laser Processing.
- Outdoor Testing Program for the Apollo® module.
- Production Waste Abatement and Closed Loop Study.

The first task is seen as critical in the characterization of the semiconductor's performance because it defines a baseline for the first devices from the large area reaction chambers. The second task will concentrate on optimization of the high volume laser processing techniques required for production. The third task, outdoor testing, is essential for any new thin film product and not only provides confidence in the device, but also may identify any improved performance over traditional crystalline silicon technology, such as low light level "switch on" effects. The last task is important for the technology since it is based on wet chemical reactions. This builds on work performed under a previous NREL contract # AFF-8-17619-27.

1.1 CdS and CdTe Film Studies

1.1.1 Process Schematic

The schematic shows the process sequence for CdS, CdTe deposition and back contact application.



1.1.2 Reaction Sequences for CdS and CdTe

The BP Solar process for depositing both the cadmium sulphide and cadmium telluride layers is based on solution chemistry reactions. The process principles for these novel reactions have been described in the literature (1,2,8). The attraction of the processes is in the availability of the precursor materials, chiefly various salts of cadmium and tellurium, and the low capital cost of such equipment. The latter is particularly true due to the lack of vacuum and high temperature processes.

Chemical bath deposition of cadmium sulphide

CdS is deposited from an aqueous solution reaction. The reduction/oxidation reaction is as follows:

$$Cd2+(complex)(aq) +(NH2)\ 2CS(aq) +2OH\text{-}(aq) \rightarrow CdS(s) +H2NCN(aq) +2H2O(l)$$

CdS deposited on the non-TCO side or "sunny side" is removed using HCl. The resulting byproduct is $CdCl_2$, which is easily treated/removed in BP Solar's wastewater treatment system.

$$CdS_{(s)} +2HCl_{(aq)} \rightarrow CdCl_{2(aq)} +H_2S_{(g)}\uparrow$$

The H_2S gas is scrubbed using an activated carbon scrubbing system.

Electrochemical deposition of cadmium telluride by potentiostatic control

CdTe is deposited by electrochemical deposition. The cathode in the reaction is a CdS coated TCO coated glass substrate. The TCO substrate is commercially available. The reaction for the reduction of Cd and Te at the TCO/CdS surface is as follows:

$$Cd^{2+}_{(aq)} +HTe0_2{}^{+}_{(aq)} +3H^{+}_{(aq)} +6e^{-} \rightarrow CdTe_{(s)} +2H_20_{(l)}$$

1.1.3 CdS/CdTe Equipment and Operation

The window layer, CdS, is deposited in high volume equipment that has four in line process tanks. The equipment configuration comprises of a pre-clean DI water tank that is used to clean the glass surface, two identical process vessels and a heated DI rinse tank.

The final tank (heated DI) acts to clean and quench the deposition reaction and also aids rapid drying of the glass plate. The two process tanks are worked in parallel and are identical. Process chemicals are supplied from two reservoirs. The first reservoir contains the cadmium compound and chelating agent, aqueous ammonia. The second reservoir contains the thiourea aqueous solution. The metering/mixing of these compounds is computer controlled, as is the sequence in which they are added. This needs to be precise, as the plates must be dipped at the moment the compounds are placed in the tank. Also, the components must be sufficiently mixed to initiate the reaction. A typical reaction time is 15 minutes. The CdS deposition follows an exponential decay, with the fastest deposition rates occurring in the first 5 minutes. After the deposition is complete, the bath waste is sent to the waste treatment and recycling system.

The next step of the CdS process is the removal of residual CdS from the front (or sunny side) of the glass and along the edge. The edge removal is performed so that electrical contact can be made to the tin oxide surface for electroplating. The contact is made on the exposed tin oxide surface on both long (61") edges of the plate.

The excess CdS is removed using HCl. This has been found to be a very efficient method for CdS removal. The reaction is very rapid, affording byproducts of $H_2S_{(g)}$ and $CdCl_{2(aq)}$. Both by products are easily abated and controlled. These abatement technologies were described in detail in BP Solar's DOE funded project that was completed July 1998.

The final CdS process step prior to CdTe deposition is a 400^{o}C heat treatment that recrystallizes the CdS, modifying its band gap.

The CdS reactor is capable of producing eighty, 0.94m^2 plates per deposition run, at a rate of almost 1,000 plates per day.

1.1.4 CdTe Equipment and Operation

The main CdTe production system was designed by BP Solar engineers and built by a manufacturer of specialist electrochemical systems. The system was designed to electroplate forty 0.55m^2 plates or twenty four 0.94m^2 plates simultaneously on a per tank basis. The equipment has a high level of automation with respect to plate handling and control. Each plate has its own potentiostatic controller. The system is modular in nature. The capacity 0.94m^2 tank is replicated eight times in the production train to give the line a 8MW pa. capacity. For each twenty-four plate tank there are two re-circulation pumps which supply tellurium replenished solution to the plating cells. These pumps are standard Teflon based, magnetic drive systems. The computer-controlled potentiostat is used to administer the applied voltage to the cathode plate. It is also used to determine the total charge applied to the plate by integrating the plating current with time. The target charge is 2,500C/sqft and the charge produces approximately 1.8μm thick CdTe film.

Figure 2. Electrochemical Reactor for CdTe Film Deposition

Development of the Apollo CdTe module through the project

While the main part of the report shall concentrate on the technical aspects of semiconductor development and reliability, this section will describe the increases in scale achieved over the project and finish with a bench mark against other thin film technologies.

Figure 3. 0.94m^2 Apollo Glass Laminate

The basic module design comprises of the following components,

- Transparent conductive oxide coated glass: Commercially available, coated float glass.
- Double glass laminate: Both glass sheets are heat strengthened meaning that they comply with ASTM 1048.
- Lamination: The two glass sheets are laminated using a standard solar industry (pump/press) laminator. The adhesive used is fast cure EVA.
- External cables and junction box: Incorporated from standard product BP Solar products.

Figure 3 shows the 0.94m^2 Apollo module as it is at the end of the current subcontract. The 24" by 61", monolithic module is currently the largest thin film module made. BP Solar plans to make two power ranges, 80W nominal and 70W nominal, with plans to introduce a 90W version as the technology is improved and refined. Figure 4 below shows the improvements made in the technology over the period of the project. The increases in size predominantly came from improvements in plating conditions and reductions in the transparent conductive oxide sheet resistance.

Along with the substrate size increases, there have also been significant increases in the device performance. The details of these increases will be described in the main body of the report but a summary of the achievements are shown in the graph below, Figure 5.

Figure 4. Increases in Plate Size in the Apollo Technology

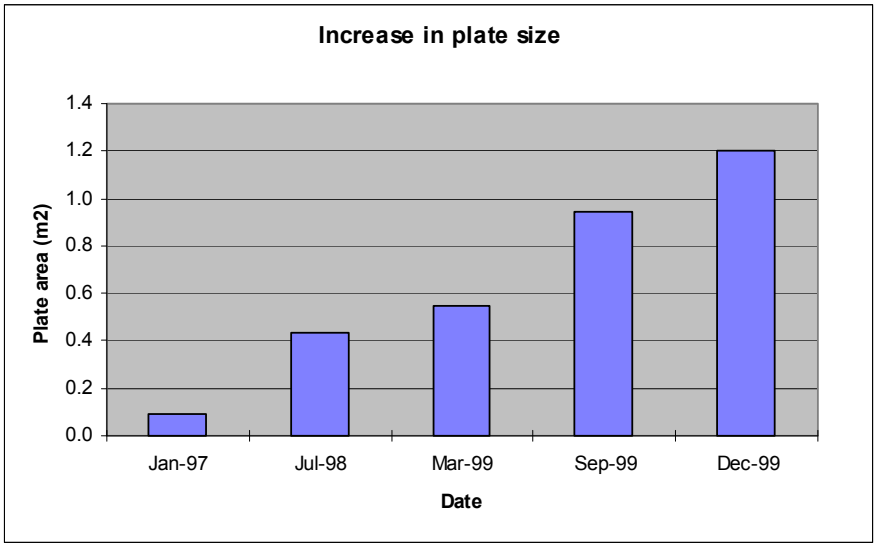
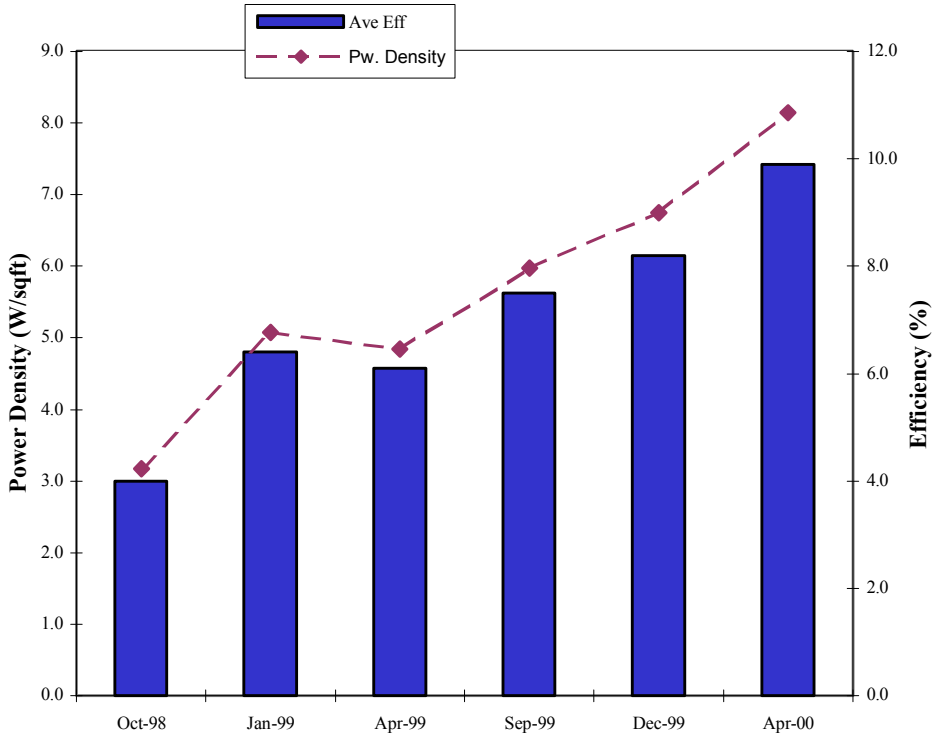


Figure 5. Improvements in the Device Efficiency for Apollo Modules



2. Semiconductor Characterization and Optimization

The semiconductor characterization and optimization section of the subcontract focused on the tin oxide coated substrate, buffer layer studies, CdS optimization and CdTe characterization. In each case, characterization studies were either performed in house or by collaboration with other members of the National CdTe team. Where necessary, external subcontractors were used who had relevant skill sets such as local surface analysis companies or impurity analysis companies.

As described earlier, the BP Solar heterogeneous II-VI device offers a low capex cost route to multi mega-Watt thin film production. The full understanding of the semiconductor properties is essential to promote its full potential and maturity into a manufacturing process.

2.1 Tin Oxide Coated Glass

BP Solar purchases its tin oxide coated glass substrates from a commercial manufacturer. At no point in the project was there felt to be a need to manufacture the material internally. The tin oxide coated glass has two functions in the Apollo process. One of its actions is to behave as a cathode in the electrochemical deposition process. This is essential to the technology. In this case, the electrical properties of the material need to be such that there is not a substantial potential drop through the plate that non-stoichiometric deposition occurs. This becomes the driving force for the selection of plating condition, in particular plating current density and the sheet resistance of the tin oxide. In the early stages of the project, the substrate width was limited to 14". The main limiting factor for this width was the tin oxide sheet resistance. The sheet resistance of the tin coating was 10Ω/sq for the 14" substrate. During the first two thirds of the subcontract, this 0.55m^2 substrate was used.

Considerable effort was placed on large area development during the subcontract. The advantage of breaking the 50W barrier for the finished module power was attractive not just for lower finished module costs (and the economies of scale associated with larger unit modules) but also from a balance of systems point of view. One of the challenges for electroplating large areas is how to overcome potential drop within the conductive transparent oxide (CTO). While potential drops in the contacting connections to the plate are minimal, potential drops in the CTO between the connections can be substantial. If a substantial potential drop occurs in the CTO, then CdTe stoichiometry will vary, favoring Te rich or Cd rich CdTe deposits, depending on the extent of the drop within the plate. The technical team at BP Solar worked with suppliers to obtain CTO films with sheet resistances below 7Ω/sq in order to reduce potential drop in the 61" x 24" plate. Initial results were encouraging, and films were obtained with good composition uniformity. Some of the first plates were fully processed without cutting down to smaller sizes. The results were very encouraging, indicating a good robustness of the process towards large area scale up. The performance of two of the plates was verified at NREL and the results are summarized in Table 1 below.

Table 1. 0.94m^2 Module Measurements Made at NREL

Module Number	Test System	Voc (V)	Isc (A)	FF (%)	Pmax (W)	Cell Eff. (%)
92440041	Spire 240A	44.92	2.476	.607	67.53	7.8
92440041	Outdoors	45.00	2.466	.623	69.08	7.9
92030054	Spire 240A	45.08	2.503	.615	69.43	8.0
92030054	Outdoors	45.19	2.477	.646	72.23	8.3

The electrical configuration of these modules consisted of 57 cells in series. The cell area was 152.3cm^2 giving an active are of 0.868m^2 and a total module area of 0.944m^2. The powers in this table were later surpassed (and are reported later in the document). The results did clearly show that the importance of tin oxide sheet resistance on scaling the electrochemical CdTe process.

2.2 High Resistivity Buffer Layer Studies

Utilization of high resistivity buffer layers has been studied by various groups (9) in industries including amorphous silicon as well as CdTe. They have been shown to reduce shunting of p-layers and back contact materials to the conductive tin oxide. The application of buffer layers with electrodeposited CdTe has not been demonstrated though.

A high resistivity buffer layer has been shown to improve device performance by allowing reduction of the CdS window layer while off setting possible electrical shunting between the CdTe absorber and the transparent conducting oxide. The benefits of this process have been demonstrated by various groups with increased Isc leading to higher efficiencies. Other groups typically use a dry process to apply the CdTe layer (CSS, PVD, etc), which means that the underlying transparent conducting oxide layer does not play a roll in the absorber layer deposition mechanics. In electrochemical deposition, this is not the case as the TCO acts as the cathode during the CdTe formation. Moreover, the ability to deposit CdTe is directly related to the conductivity of the conducting oxide. As a result oxides with high resistivities will not form stoichiometric layers of CdTe by electrochemical deposition.

In Phase 2, the chemical bath deposition of CdS was characterized for its optical and electrical properties. It was shown to have a resistivity in the order of 10^4 ohm.cm. which is three or four orders of magnitude higher than the resistivity of reported oxide buffer layers. This was considered encouraging for a potential compatibility with the electro-deposition process as CdTe can be deposited directly on CdS.

In order to perform evaluation trials, T Gessert's group at NREL made a number of tin oxide films deposited on standard LOF TCO substrates. The TCO sheet resistance was measured at 10 ohm/sq.. The substrate dimensions were 3" x 12" which was the largest size that could be deposited by NREL. The SnO_2 films were deposited via CVD and the

electrical parameters were measured using a four point probe with current source and high impedance voltmeter.

The properties of the tin oxide films deposited at NREL are shown on the following page in Table 2.

Table 2. Resistive Oxide Thickness vs. Sheet Resistance and Bulk Resistivity

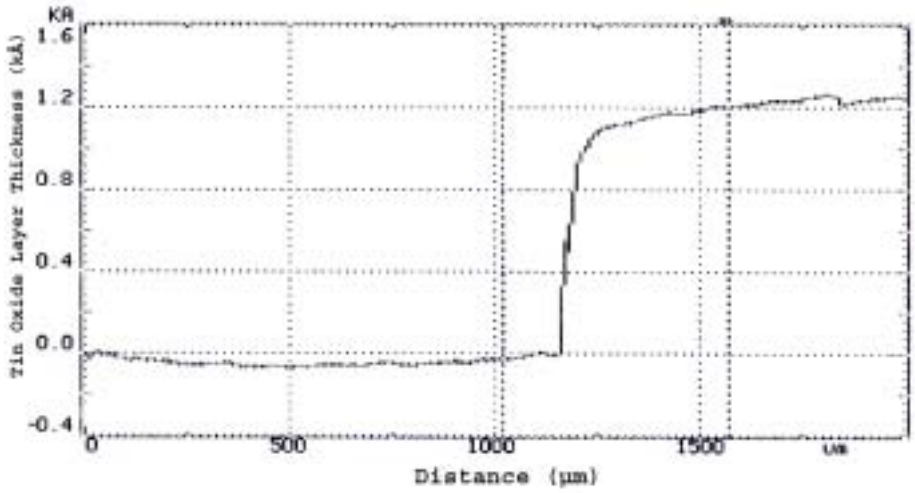
SnO_2 thickness (Å)	Sheet Resistance (Ohm/sq.)	Bulk Resistivity (Ohm.cm.)
500	35,800	0.179
1000	41,650	0.417
2000	31,210	0.624
4000	17,349	0.694
10,000	17,010	n/a

The resistance values for each run were determined from 1sq.in borosilicate glass samples. Variances in the bulk resistivity were seen due to composition and doping differences. The resistivity of the 10,000Å film was difficult to measure due to its thickness. It was estimated that the resistivity value was between 0.6 and 1.0 ohm.cm.

Various organizations have looked at using a buffer layer with amorphous silicon, CIS as well as with CdTe. In the case of CdTe, no data has been forth coming on the compatibility of this type of layer with electroplated CdTe. Electro-deposition of CdTe on a high resistivity tin oxide/CdS film and the subsequent affect on potential drop is not known. What is known is that high potential drops in the cathode can lead to non-stoichiometric CdTe.

Some initial work was performed on small areas through collaborative work with SierraTherm Inc., CA and NREL. Both groups deposited tin oxide by CVD processes. These films were characterized and the resistivity determined by Hall effect and four point probe measurements. Large area deposition (>0.25m^2) was not possible by either group at the time of the test. BP Solar investigated depositing resistive TCO layers of various thickness and compositions by DC sputtering. Using this method of deposition, conformal films of over 1m^2 were made. Four point probe measurements showed resistivities to be in the order of 1 to 10Ω.cm for a 1200Å thick film. Figure 6 shows a surface profilometer step trace of the film. It is worth noting the very smooth surface obtained by this method of deposition. The interfacial high resistance TCO layer has been optimized to reduce potential drop across the plate during CdTe electrodeposition as well as to realize better IV performance of a processed plate/module. High efficiency values reported at the later portions of this report incorporates this interfacial layer, although its thickness and characteristics are unique compared to other interfacial/buffer layers used in PVD/CSS deposited CdTe devices.

Figure 6. Step Profile of Resistive Oxide Film



2.3 CdS Optimization

As described in the introduction the method for CdS window layer formation is by thio-urea reaction with a high pH Cd ion solution. At the beginning of the subcontract, CdS thickness was in the range of 1000Å. By the end of the subcontract, the CdS thickness had been reduced to 500Å. The following section describes the performance of the devices prior to the thickness reductions and the studies undertaken to characterize the CdS film.

CdS Optical properties

The band gap and transmittance measurements are shown for various CdS thickness is in the table below. Note: All depositions on 10 ohm/sq tin oxide coated glass except where stated. Transmittance and band gap were determined for CdS before and after a standard heat treatment of 400^{o}C for 20 minutes in air. Optical measurements were made on an Oriel spectrophotometer using a filtered white light source. The results are shown in Table 3 below.

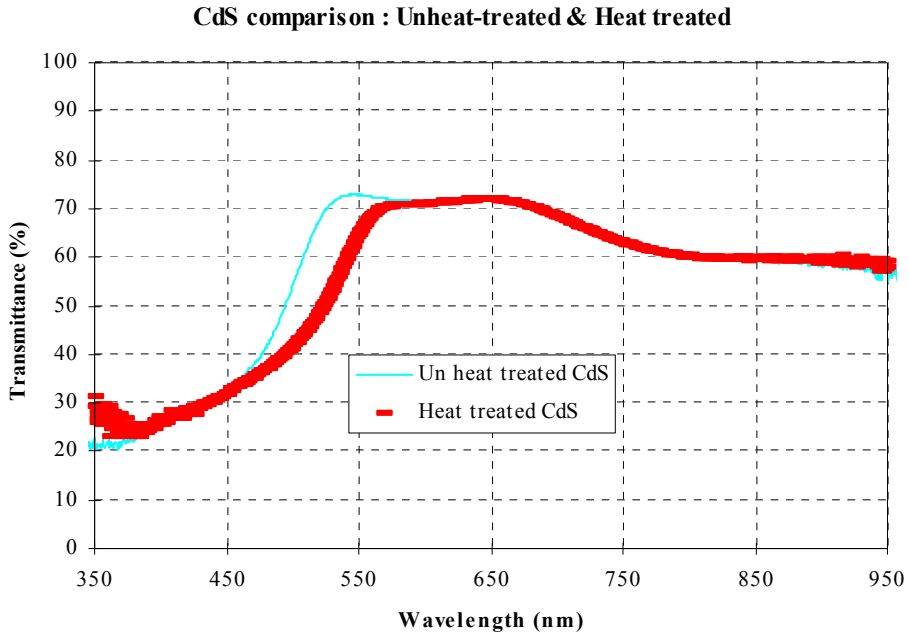
Table 3. Cds Band Gap Studies, Before and After Air Anneal

Sample	Thickness (Å)	Bandgap uCdS (eV)	Transmittance uCdS (%)	Bandgap hCdS (eV)	Transmittance hCdS (%)
C	595	2.42	58		
D	623			2.32	55
E	666			2.28	55
F	679	2.41	57		
G	897			2.26	53

Note: u stands for un-heat treated. h stands for heat treated.

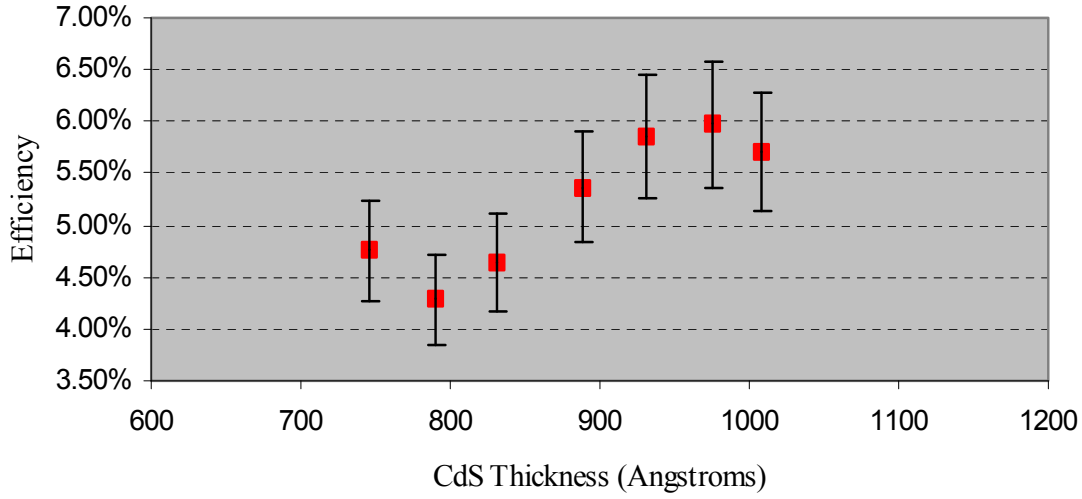
Figure 7 below shows the transmittance change in the CdS film before and after anneal. There is a reduction in transmittance in the 450nm to 550nm range post heat treatment in air. To the eye, the film color changes from yellow to orange/red. It is believed that the transmittance change is a result of the reaction with oxygen and a re-crystallization.

Figure 7. CdS Transmittance Before and After Heat Treatment



During the early stages of the project, a sensitivity study was undertaken to determine to what extent CdS thickness affects efficiency. It can be seen from Figure 8, that there was a significant drop off in performance for CdS thicknesses between 850Å and 900Å.

Figure 8. Effect of CdS Thickness on Efficiency



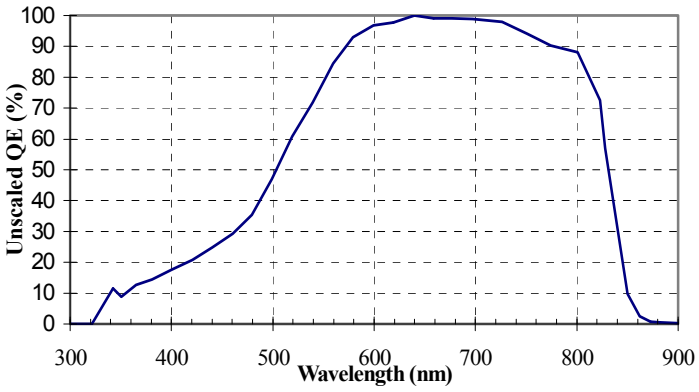
As part of the BP Solar Inc. team effort on semiconductor optimization, work has focused on characterization of the CdS/CdTe crystal structure at various stages of the process. BP has worked with IEC (University of Delaware) and the CdTe group at NREL to determine the physical properties of the films. Various techniques were incorporated including AFM and XRD as well as QE and electrical measurements. The data obtained from this work were used to optimize the semiconductor recrystallisation steps and heat treatments. One important study that was undertaken was an optical loss analysis of the finished device. The aim of this work was to identify the loss mechanism in the device and then prioritize for largest potential gain and compatibility with the existing process. The following section describes the work performed on standard CdS / CdTe cells

2.4 CdS/CdTe Device Loss Analysis

Quantum efficiency measurements and a loss analysis were carried out on typical CdS and CdTe films. The CdS thickness was 1050Å and the CdTe thickness was 1.8microns. These films were deposited on standard Pilkington (LOF) substrates with a sheet resistance of 10Ω/sq.

Loss analysis was carried out at IEC (UOD). Module spectral response was measured by K. Emery of NREL. The spectral response for the Apollo® module measured at NREL is shown in Figure 9.

Figure 9. Apollo® Mini-module QE



The mini module dimension was 645cm^2 and had a glass tedlar configuration. This size and construction was chosen especially for the QE work and is not standard for BP Solar's Apollo® product. Electrical connection was such that a single cell and the whole module could be measured independently if required.

The module electrical parameters that correspond to the above QE are shown in Table 4.

Table 4. Mini Module Electrical Characteristics

Voc:	25.45 V (0.795V/cell)
Jsc:	16.60 mA.cm^{-2}
FF:	0.64
Efficiency:	8.62%

The low Jsc is due to losses in the 400nm to 600nm wavelength range. This can be accounted for in terms of CdS absorption and band gap narrowing due to CdS/CdTe intermixing at the hetero-junction interface.

B McCandless of IEC (UOD) conducted a loss analysis study. A break down of optical losses in the device was made possible as a result of the study. The results are shown in Table 5.

Table 5. Summary of Loss Analysis

Loss mechanism	Wavelength range (nm)	Integrated Photocurrent ($mA.cm^{-2}$)
TCO/glass absorption	300-860	4.0
CdS absorption	300-490	3.0
Cell reflection	300-860	1.3
"Red" carrier collection	650-860	1.0
CdS/Te absorption	490-600	0.8
Unabsorbed red carriers	820-860	0.2

Some of the losses described above are avoidable but inevitable for a cost effective production process. For instance, $5mA.cm^{-2}$ of Jsc is lost due to TCO/ glass absorption and cell reflection. The TCO/glass absorption could be reduced by moving to 1mm thick borosilicate glass instead of float line, 3mm soda lime glass. Equally, the 10Ω/sq. (approx. resistivity $6x10^{-4}$ Ω.cm.) fluorine doped tin oxide could have a higher transmission by using other more transparent oxides. However from a commercial point of view it is felt that gains in these areas, while technically possible, will increase the total cost of the product or reduce the robustness of the final device. Reduction of CdS thickness will reduce the absorption in the 300nm to 490nm range and increase Jsc accordingly. Jsc's as high as $19.7mA.cm^{-2}$ have been demonstrated with CdS thickness of 690nm to 700nm. However, this typically is accompanied by a loss in Voc and FF for the device. It has been shown that resistive buffer layers can be incorporated between the TCO and the window layer to inhibit shunting through pinholes in thin CdS. Utilizing a thin, highly resistive tin oxide or zinc doped tin oxide buffer layer in conjunction with thin CdS has been used successfully to maintain Voc and fill factor while obtaining beneficial increases in Jsc. This could be one route to decreasing the losses from CdS absorption but as yet there is little or no data on how compatible an electrochemical CdTe process is with a highly resistive buffer layer. Work performed by T Gessert's group at NREL has shown that CdS from Fairfield had the following properties. The properties are shown in Table 6.

Table 6. CdS Electrical Properties

Sheet resistance	7.00E+09	ohm/sq.
Resistivity	7.00E+04	ohm.cm.
Mobility	2.86	$cm^2/V.s$
Doping density	3.12E+13	$/cm^3$

Another area of considerable loss is in "red" carrier collection and absorption (total potential gain 1.2mA.cm^{-2}). Grain size for electrodeposited CdTe is small. Typically, CdTe grains average at 0.3 microns, which is normal for low temperature processes. Increasing this grain size will reduce the grain boundary to grain size ratio and improve carrier lifetime and collection. This will be an area the BP Solar team will continue to investigate.

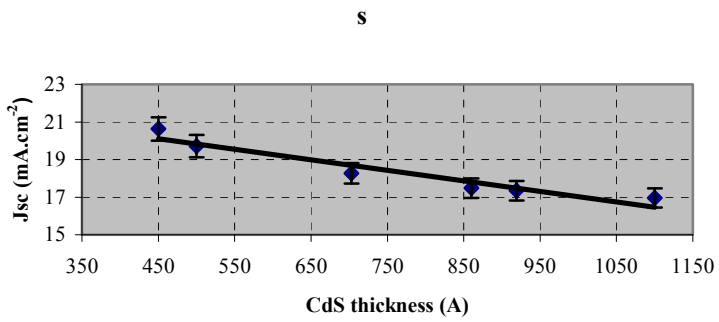
In summary, the loss analysis has helped focus efforts in areas that will increase device performance through Jsc increases. If a Jsc of 20mA.cm^{-2} is used as a target for 0.55m^2 and 0.94m^2 modules, then if the Voc and fill factor illustrated in Table 1 are maintained, then module aperture area efficiencies greater than 10% will be realized.

2.5 Optimization of CdS Window Layer Thickness

A study was performed to determine the relationship of Jsc with CdS thickness to follow on from the optical loss analysis described in the previous section. The loss analysis had shown that approximately 3 to 4 mA.cm^{-2} could be gained from optimization of the CdS properties with the majority of the gain coming from a reduction in the CdS thickness.

The loss analysis had been performed on a mini module that had a 1050Å thick CdS film which gave a corresponding 16.6mA.cm^{-2} Jsc. CdS films were made using a modified chemical bath deposition process which gave CdS films down to 450Å. Figure 10 shows the relationship of CdS thickness with Jsc as the film is reduced and glass substrate, CdTe and back contact films remain constant. From the devices made, quantum efficiency measurements were obtained to ascertain the effect on the blue response to reducing the window layer.

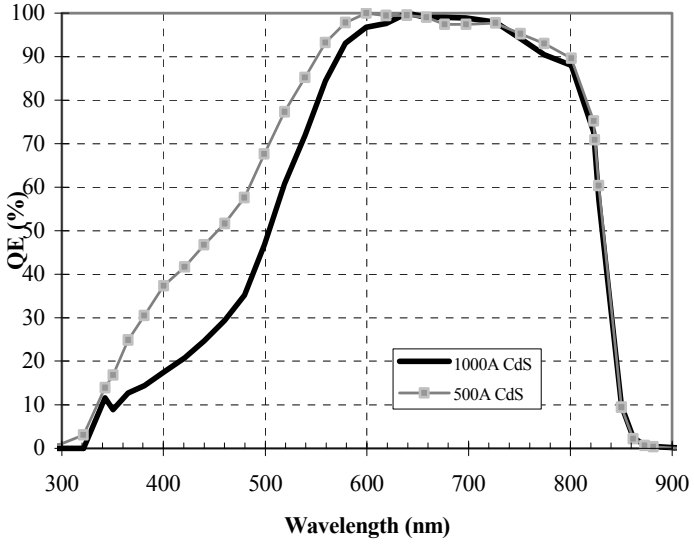
Figure 10. Jsc vs. CdS Thickness



Quantum efficiency (QE) is a good technique for determining the wavelength dependent response for solar cells. Quantum efficiency also helps resolve the spatial response through the device. Knowing the band gap and absorption coefficients of the window and absorber layers, a loss analysis can be performed to determine which semiconductors are limiting performance. The QE shown in Figure 11 shows the response for Apollo®

devices made with different thickness' of CdS window layer. The standard process incorporates a 1000Å CdS layer, which limits the blue response of the device. At 400nm and 500nm, the QE values are 17% and 50% respectively for the standard device. This wavelength range has been shown to be greatly influenced by CdS absorption. A loss analysis showed as much as 6mA.cm^{-2} could be gained in Jsc by reducing the CdS thickness. Typical Jsc values associated with a 1000Å CdS film are in range of 17mA.cm^{-2}. On the basis of this investigation, devices with thinner CdS layers were fabricated. The QE for devices containing a 500Å and 1000Å window layers are compared in Figure 11. Clearly, there is an improved blue response for the thinner window layer. At 400nm and 500nm, QE values of 38% and 69% were measured respectively with essentially no change in the regions relating to the bulk absorber (>600nm). The Jsc values for these devices were in the range of 20.5mA.cm^{-2}, indicating more than 20% increase over the thicker window layer. We believe this is a significant achievement as these Jsc values are currently unprecedented for a commercial size modules. Later in the report, the effect of improved blue response on device results will be discussed in more detail.

Figure 11. QE for Reduced CdS Window Layer vs. Standard Thickness



2.6 Morphology of Electro-deposited CdTe Material

In order to understand the crystallographic detail samples were sent to external laboratories (NREL and IEC) for analysis and quantification of the changes in morphology at various stages of the CdTe process. Of particular interest was the form of the CdTe directly after electro deposition and after subsequent heat treatments. Typically, low temperature depositions of CdTe such as electrochemical, physical vapor deposition, and sputtering afford small grain structures (<1μm). There is a considerable amount of strain incorporated in these films as deposited and the crystal structure has a predominant <111> orientation. Strain relief, is one of the aspects seen in the CdTe film after a 450^{o}C anneal in air, as is a change in orientation of the crystal unit cell (11-13). As well as the orientation change, grain growth can also occur when the heat treatment is performed in the presence of chloride (14-15). In the electrochemical deposition of CdTe, chloride can

be incorporated in the film during the plating process. Initial results confirm that chloride additions can be also performed post deposition, commensurate with other CdTe films.

The two techniques used to investigate the crystal structure were atomic force microscopy (AFM) and x-ray diffraction (XRD). The following data illustrates some of the typical structures seen for the Apollo® films.

Figure 12. AFM of as-Deposited CdTe

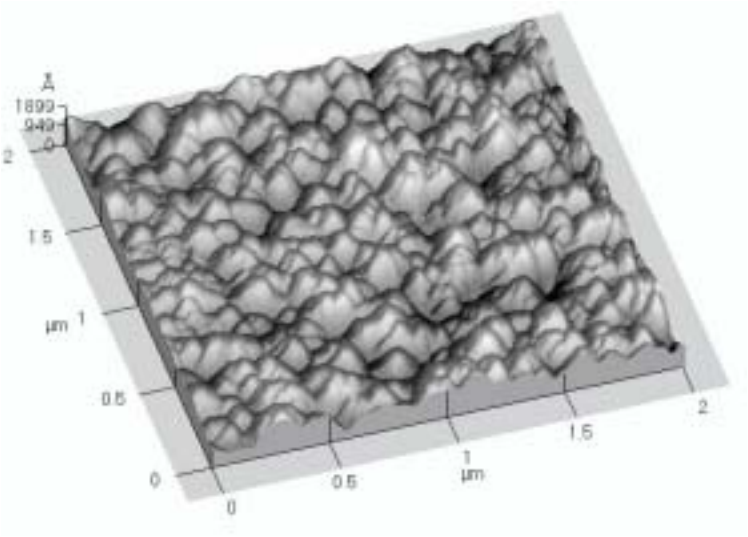


Figure 13. XRD of as-deposited CdTe

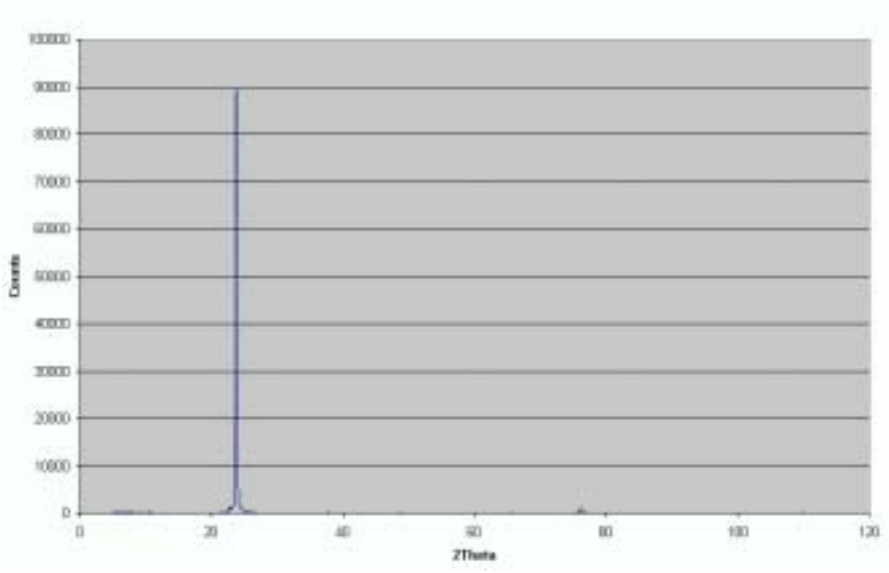


Figure 14. AFM of CdTe Post Air Anneal

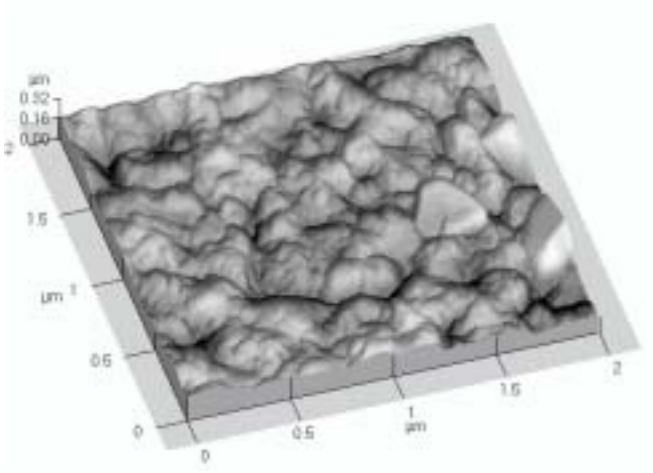


Figure 15. XRD of CdTe Post Air Anneal

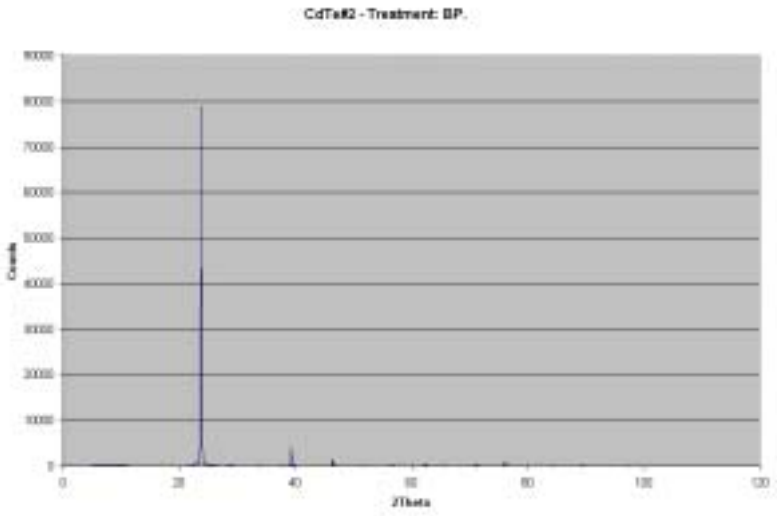


Figure 12 shows the grain structure for as deposited CdTe. The typical grain size is between 0.1µm and 0.2µm. Some grains exhibit faceted faces, which indicate that grain sizes could be smaller than 0.1µm. The XRD data in Figure 13 shows that the grain orientation at this stage was predominantly <111> as normally seen for films at this stage.

Figure 14 shows grain formation after heat treatment in air at 450C. Some grain growth and coalescing of the grain facets was observed. Also, the maximum grain dimension had increased to about 0.4µm from 0.2µm. Figure 15 shows a modest change in the crystal structure.

This data indicates that, while some gain growth occurred, it was not substantial and that the grain structure is held or pinned in some way.

2.7 Comparison of CdTe Films Formed Using Alternative Methods

This section highlights the joint work being performed between BP Solar and IEC (University of Delaware) on the crystallographic differences between CdTe films formed by electro-deposition, physical vapor deposition (PVD), and close space sublimation (CSS). The electrodeposited samples were made at BP Solar. The PVD and CSS samples were made at IEC.

This work was undertaken so that a greater understanding could be obtained as to why device operation of electrodeposited CdS/CdTe solar cells is similar to other devices with considerably different grain structure. This is in spite of the fact that the electrodeposited CdTe films have a thickness of less than 2μm and the lateral grain size is sub-micron. BP Solar has shown that cells made by electro-deposition exhibit aperture area efficiencies of almost 11% at $0.94m^2$ (16). For this reason the approach of the work was to compare CdTe films with similar thicknesses deposited by various methods.

2.8 Comparison of Various CdTe Films

Various techniques were used to compare the CdTe films. The techniques were utilized to not only to obtain morphological data but also gain information on the chemical nature of the surface and bulk of the CdTe films. Atomic force microscopy (AFM) was used to obtain grain size and surface morphology details. Energy dispersive X-ray spectroscopy (EDS) was used for surface chemistry analysis while X-ray diffraction (XRD) and glancing incidence X-ray diffraction (GIXRD) gave crystallographic as well as surface and spatial compositional analysis.

Film analysis was carried out in the as deposited form and in the post heat-treated form. In all cases, post deposition heat treatment was necessary for either grain growth or grain boundary passivation. The extent of recrystallization and grain growth appears to be greatly dependant on the method of film deposition. In all cases, the heat treatment was performed in the presence of chloride ions, either within the films or on the CdTe surface. Details of the three films investigated are shown in Table 7. below.

Table 7. Film Properties of the Three CdTe Films Deposited by Different Methods:

	Electrodeposited	**PVD**	**CSS**
Deposition temperature	70°C	340°C	600°C
Film thickness	1.8 micron	4.0 micron	4.0 micron
As deposited orientation	(111)	(111)	Random
As deposited composition	CdTe	CdTe	CdTe
Post heat treatment orientation	Random or (220)	Random	Random
Post heat treatment oxides	$CdTe0_3$ CdO	$CdTe0_3$ CdO	$CdTe0_3$ CdO

From Table 7, it can be seen that the CdTe deposition temperatures differ significantly between the various methods. For electro deposition and PVD, the lower temperature depositions yield films with predominantly <111> orientation. The high temperature CSS films have a random orientation. On heat treatment in the presence of chloride ions, the electrodeposited and PVD films recrystallize to form random or <220> orientated films. Examples of the XRD patterns are shown in figure 16. These patterns are similar to patterns shown in earlier quarterly reports indicating the emergence of <220> grains as a result of heat treatment.

Figure 16. XRD Patterns as Deposited and Post Heat-Treated for Electrodeposited CdTe

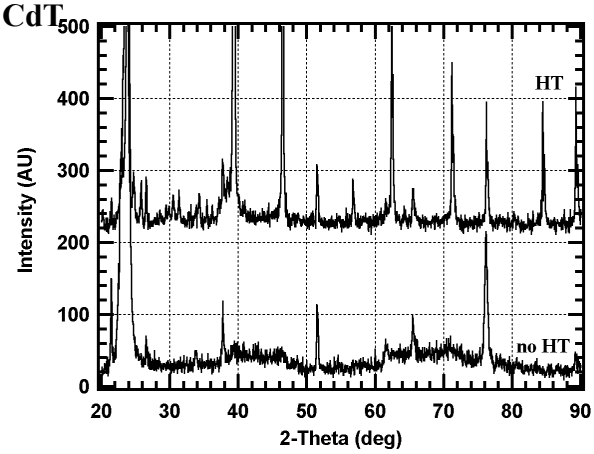


Figure 17. AFM Images of Electrodeposited CdTe

a) As deposited **b) Post heat treatment**

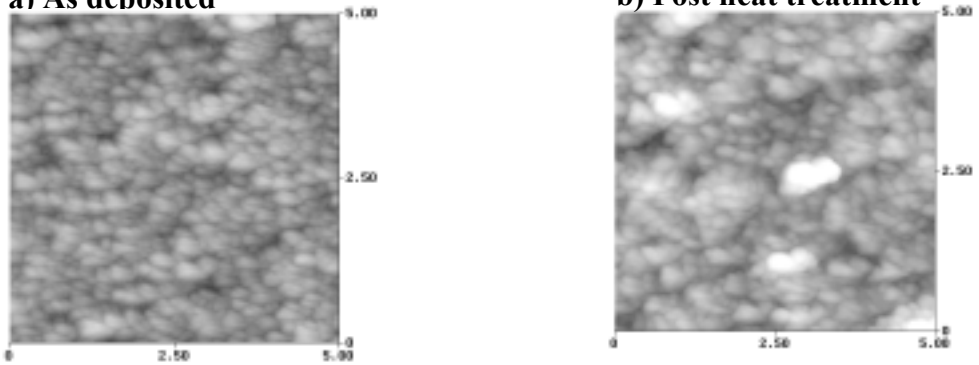


Figure 18. AFM Images of PVD CdTe

a) As deposited **b) Post heat treatment**

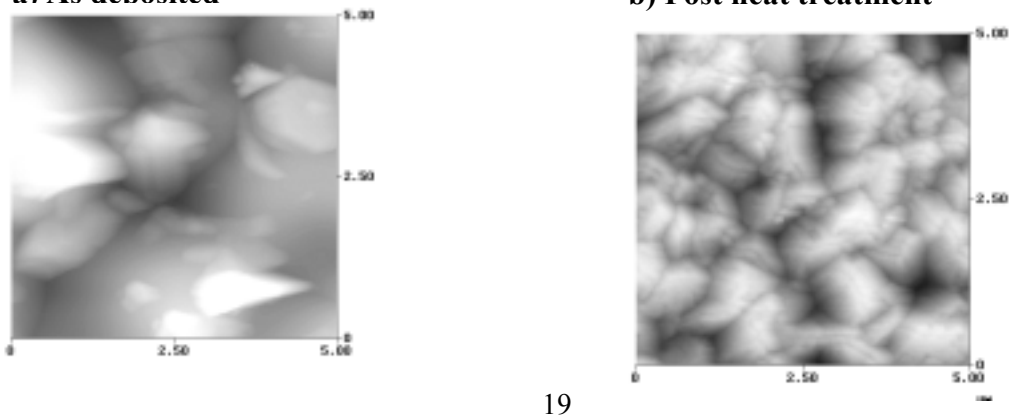
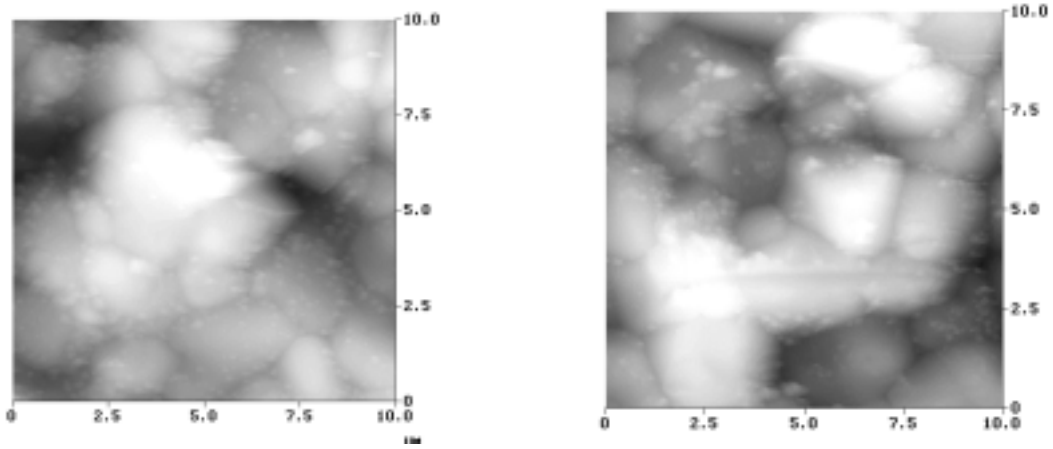


Figure 19. AFM Images of CSS CdTe

a) As deposited **b) Post heat treatment**



From the AFM shown in Figures 17 to 19, it can be seen that only in the case of PVD deposited CdTe does the heat treatment significantly grow grains. In both the electrodeposited and CSS cases the grain size stays relatively unchanged post heat treatment.

Using XRD and GIXRD, various oxide phases were observed post heat treatment. Table 7 highlights the type of oxides present. The X ray techniques show that for the CSS deposited films, the $CdTeO_3$ and CdO give only weak signals present only at the surface of the CdTe. For the PVD films the oxides are present predominantly at the surface, but for the electrodeposited films the oxide species are seen at the surface and penetrating through the bulk. Moreover, we believe that the oxides are probably decorating the abundant grain boundaries as well as the surface. No crystalline phases were detected using XRD.

2.9 Effect of Cd^{2+} Concentration on CdTe Morphology

As part of the thin film partnership program, BP Solar has been investigating the effect of cadmium concentration on CdTe grain size of the as deposited films. The approach for the work is as follows. The CdTe bath electrolyte concentration was adjusted to a target of 90g/l (weight of Cd^{2+} ions per liter of DI water). The actual concentration obtained was 88g/l. All other chemical components of the bath were maintained the same (pH, chloride level, etc.). Chloride level and pH are in the range of 400ppm and 1.6 respectively. With the bath chemistry set, the CdTe deposits were made. The CdTe deposits were sent to IEC (UOD) for AFM and EDAX analysis. AFM was used to determine the grain size and surface roughness. EDAX was used to determine the CdTe compositional ratio. All the plates were processed under normal conditions through the Apollo process. Therefore, IV data was obtained and cross-referenced with the crystallographic/compositional data.

Plating bath Cd^{2+} concentration was further reduced to 77g/l, 57g/l, and 48g/l. Crystallographic properties and CdTe composition was obtained for all concentrations with the exception of the 57g/l solution, where grain structure only was determined.

Figures 20 through to 23. show the grain structure of the CdTe at various concentrations and Table 8 shows the composition of the samples with the exception of the 57g/l solution

The AFM images show grain structure changing significantly with increasing cadmium concentration. The surface of the film appears to be smoother for the lower concentrations becoming significantly rougher as the solution increases in concentration. At this stage, it is difficult to determine the nature of the surface structure. In order to gather more information on the surface structure, IEC performed a selective surface etch. The film surface was modified with two etchants to aid in contrast enhancement so that the grain structure detail could be determined. Two methods were used. The methods are described below.

1) *A grain revealing etch.* This is a topotaxial conversion of CdTe to Cu_xTe by reaction in an aqueous Cu^{2+} solution at a low pH followed by etch in a CN^- solution to remove Cu_xTe.
2) *A cleaning/leveling etch*. This involves a reaction in a $Br:CH_3OH$ solution.

Figure 20. AFM for CdTe Deposited from [48g/l] Solution

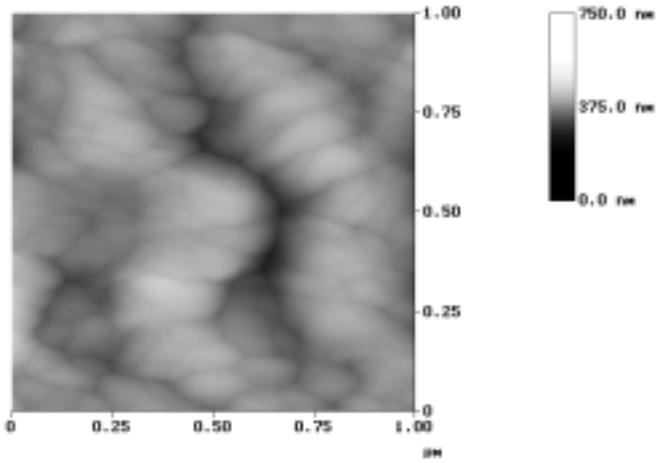


Figure 21. AFM for CdTe Deposited from [57g/l] Solution

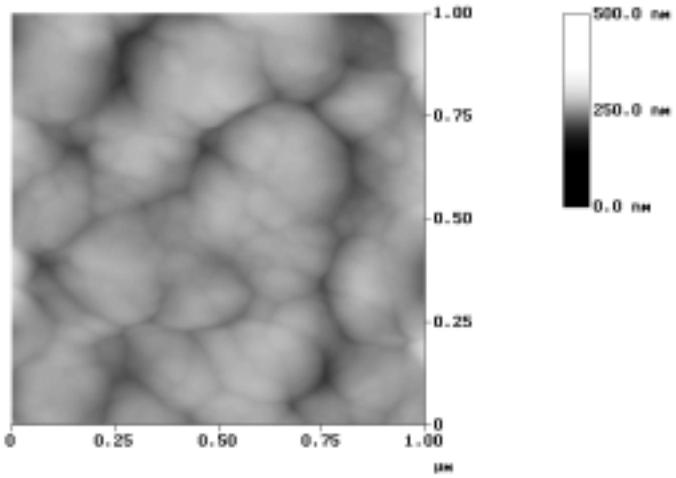


Figure 22. AFM for CdTe Deposited from [77g/l] Solution

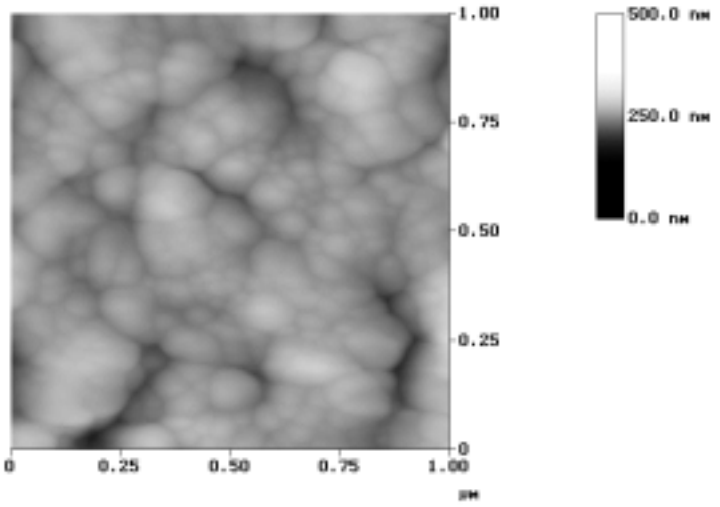


Figure 23. AFM for CdTe Deposited from [88g/l] Solution

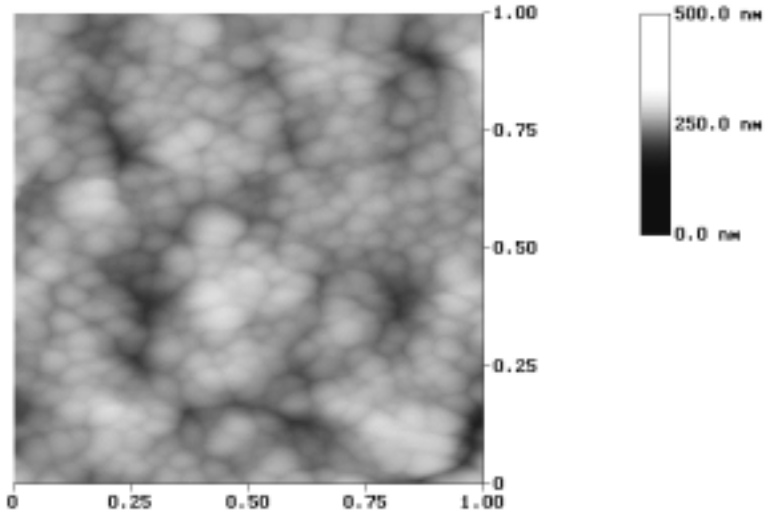


Table 8. EDAX Determination of Cd:Te Composition

Cd conc (g/l)	Cd ratio	Te ratio
48	49%	51%
77	50%	50%
88	49%	51%

Figure 24 and 25 show the effects of the two etches on films formed with high and the low Cd^{2+} bath concentrations.

Figure 24. Highest Cd^{2+} Concentration Deposit After Copper Solution Etch

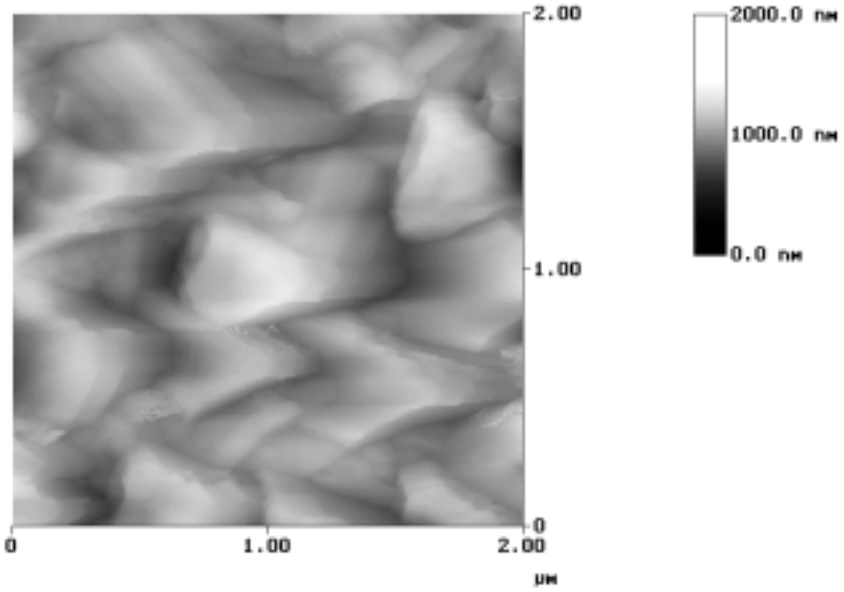
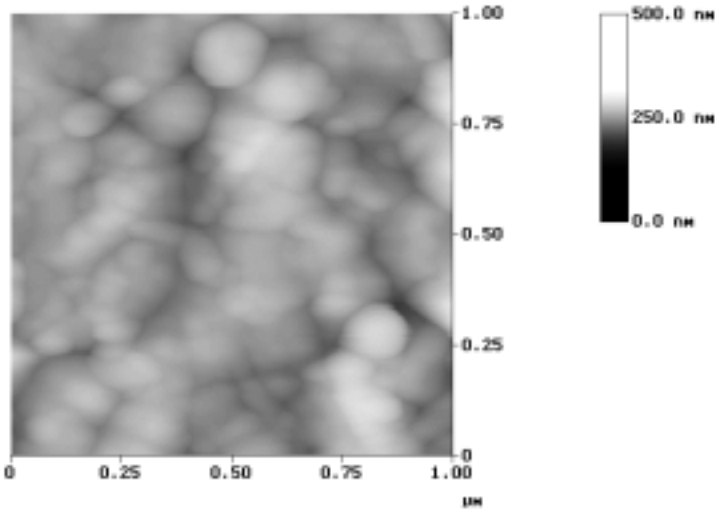


Figure 25. Lower Cd^{2+} Concentration Deposit After Copper Solution Etch

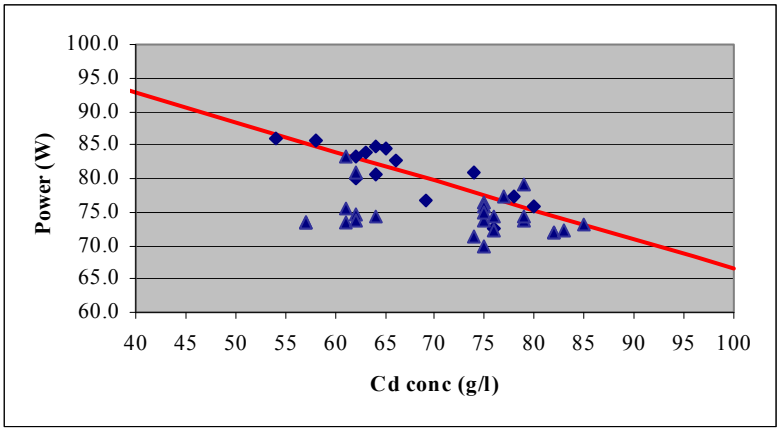


The lower concentration sample, Figure 25, exhibited a broad range of grain sizes, from 0.05 to 0.15 micron. The high concentration sample, Figure 24, reacted very differently to the Cu/CN treatment, yielding unusual etch patterns and bimodal distribution of feature sizes. The smallest features are ~0.05 micron and occur in clusters. The larger features are ~0.25 micron wide and exhibited faceted morphology. The small features on the sample produced from the high, 88g/l, solution appeared to be removed on etching.

Although there appears to be considerable differences in the grain structure of CdTe films grown from different cadmium concentrations, the Cd:Te ratios of the films are remarkably constant (see Table 1.) over the concentration range. This suggests that the most significant factor in determining stoichiometery is potential control during plating and is independent of Cd^{2+} concentration. The electroplating potential was the same for all plating concentrations.

Figure 26. shows the effect of bath electrolyte concentration on IV performance. Each point on the graph represents a daily average power for 24" x 61" plates plotted versus the bath cadmium concentration. The total individual plate sample size was in excess of 100. The red line through the points represents a least squares linear regression fit. It appears from the graph that there is a relationship between bath concentration and power. In the discussion above, the AFM images show significant differences in CdTe surface structure for deposits depending on cadmium concentration. As there were no differences in parameters such as stoichiometery, non-Cd bath components, and intrinsic impurities such as copper, we can assume that the relationship with power is a result of differing crystal structure.

Figure 26. Power Versus Cd^{2+} Concentration in Plating Tank



2.10 Effect of Copper Impurities in the Electroplating Solution

Producing a semiconductor film with low intrinsic impurities is very important for high initial performance and ultimate long-term stability. In chemical deposition processes, extrinsic impurities from material precursors can become incorporated into the semiconductor. This is especially a problem in the CdTe deposition where the precursors such as tellurium oxide are added on a regular basis. Using high purity materials minimizes contamination risk, but it is important to know the sensitivity and hence threshold for common, electro-active impurities such as copper.

A study was under taken where plate performance was determined for various copper concentrations. The graphs below show the effect of copper concentrations from 2ppm (atomic percent in CdTe) to 112ppm. The concentrations were determined by dissolving CdTe directly from the TCO plate using hyper pure nitric acid. This solution was then analyzed using an ICP-AES spectrometer for copper ions. The ICP equipment is accurate to 0.1ppm of copper. The Te peak was used to normalize the copper signal so that the copper concentration could be presented as ppm in CdTe bulk.

Table 9. Projected Effect on Device Power (W) vs. Copper Concentration in CdTe

[Cu]ppm in CdTe	Ave. Power (W)	Change
5	84	100%
10	83	99%
20	82	97%
40	78	93%
60	75	89%
80	71	85%
100	68	81%
150	59	70%
200	51	60%
250	42	50%
350	25	29%
400	16	19%

Figures 27 through 32 show the effect of copper concentration on various electrical parameters for full size CdS/CdTe devices. The data comes from various test runs where the impurity concentrations were determined on a per run basis.

Figure 27 shows the effect of copper concentration on power and cell efficiency. A linear regression (least squares) fit is super-imposed on the data points to emphasize performance trend. For electrochemical deposition systems, it is normal for the steady state copper impurity concentration to be in the order of 10ppm or less. More typically, the impurity is present in a 5ppm ± 5ppm range. Table 9 shows the projected effect on performance at various copper concentrations together with the relative change in power from a baseline concentration of 5ppm. It can be seen that significant losses in performance are not seen until intrinsic copper concentrations above 20ppm are reached. In fact a 50% reduction in power is not observed until 250ppm. It is worth noting that all the copper discussed is in the intrinsic form and homogeneously deposited through the bulk. This is not the case for copper used in back contact applications which is deliberately applied at the rear of the device to act, at least in part, as a p+ ohmic contact. The effect of copper (II) ions in bulk CdTe is what might be expected of this recombination center. As the amount increases there is a drop in Voc and fill factor, which reduces performance. Equally, the shunt resistance decreases while the short circuit current stays relatively unchanged. What is more unexpected is the change in series resistance (Figure 31). This parameter increases with concentration. This could indicate a change in doping density.

Figure 27.

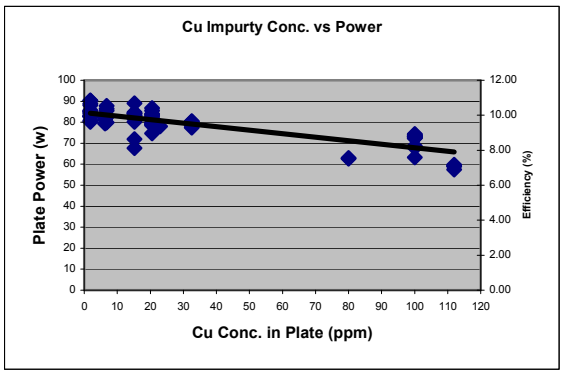


Figure 28.

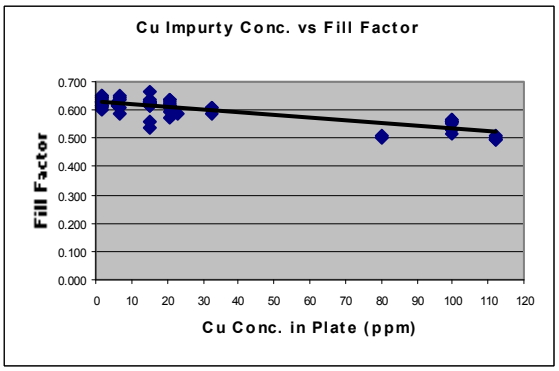


Figure 29.

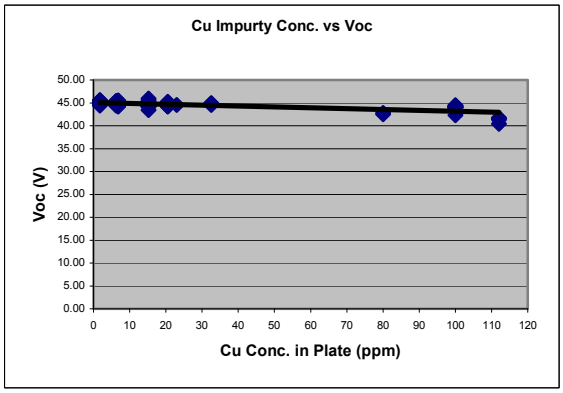


Figure 30.

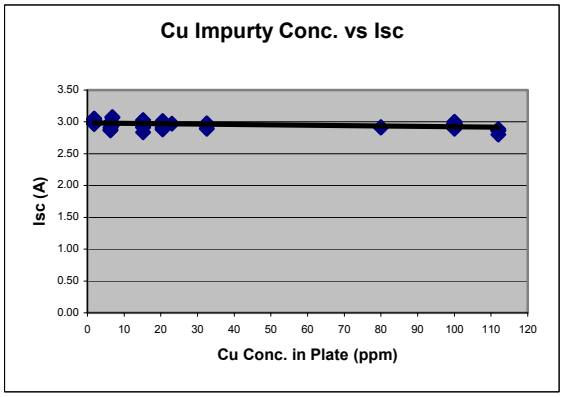


Figure 31.

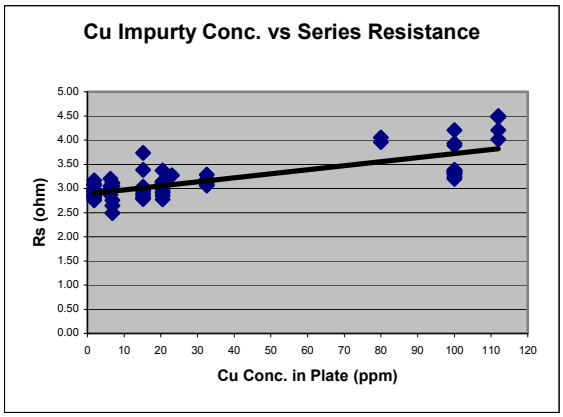
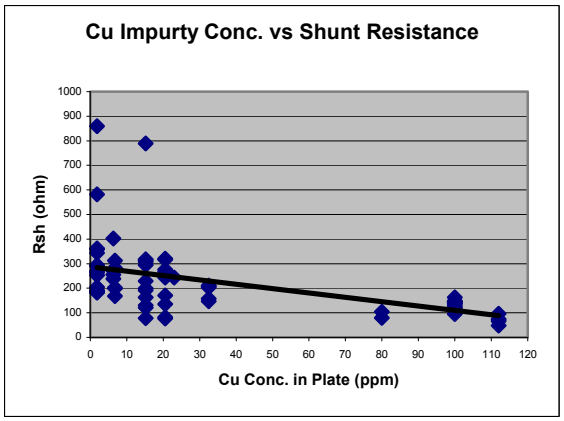


Figure 32.



Copper Partition Coefficient

As described earlier, copper is a contaminant in the deposition of CdTe. While copper can be added to the back contact successfully, if it is present during the electro-deposition process, the performance of the device can be affected adversely. The above data has shown that levels as low as 20ppm (about 8 x 10^{17} atoms Cu per cm^3 of CdTe) can reduce the efficiency. It has been found that copper and other impurities that have a redox potential less negative (versus a standard hydrogen electrode) than cadmium will co-deposit with the CdTe. This is the main mechanism for introduction of impurities into the bulk CdTe during film growth. Another factor defined by the Apollo team, is that ultra small quantities of impurities in the solution can be found at a significantly higher concentration in the CdTe. This concentration effect probably occurs as a result of the significant over potential of many of the electro-active impurities versus $Cd^{2+} + 2e \leftrightarrow Cd$ (E^{θ} = -0.40 vs. NHE) couple. A list of impurities that co-deposit with CdTe, is shown in Table 10.

Table 10. Redox Potential for Various Impurities

Ion	E^{θ}(V) NHE
Zn^{2+}	-0.76
Fe^{2+}	-0.41
Cd^{2+}	-0.4
Pb^{2+}	-0.13
Cu^{2+}	0.34
Hg^{2+}	0.85
Pt^{2+}	1.2

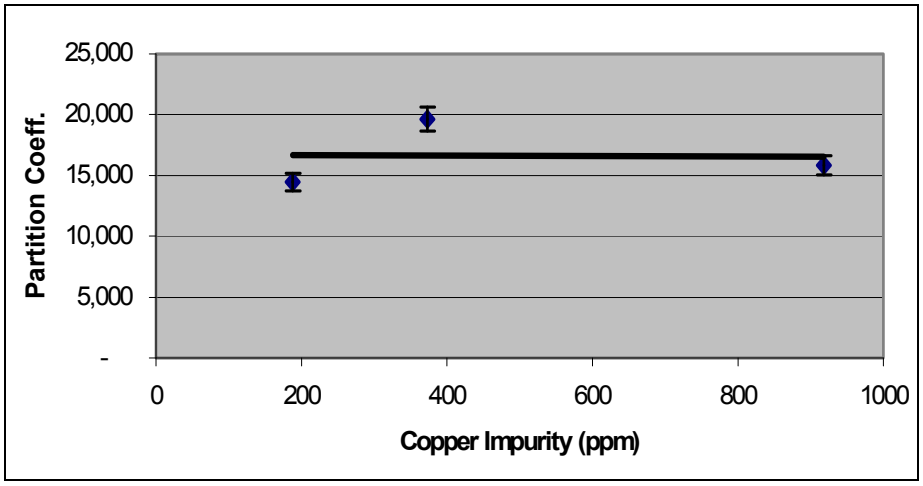
It is interesting to note that although zinc has a more negative potential than cadmium it can be found deposited in CdTe electrochemically. It is thought that this occurs by under potential deposition. The ratio of impurity found in the solution versus the solid is called the partition coefficient. It can be defined by the following equation:

$$\text{Partition coefficient} = \frac{[\text{Impurity}]\text{ppm/CdTe}}{[\text{Impurity}]\text{ppm/solution}}$$

Impurity levels in both the CdTe film and in the $CdSO_4$ plating solution can be determined by ICP-AES. BP Solar used its in-house ICP spectrometer to determine the concentrations in the CdTe and $CdSO_4$ solution. However, in the case of the solution, the concentrations were in the range of tens of ppb (parts per billion). As this level was at the detection limit of the BP equipment, independent confirmation was obtained by outside laboratories (Charles Evans West and Balzas) that utilized ICP-MS (mass spectrometric) equipment. This type of ICP has sensitivity an order of magnitude better than the AES (atomic emission spectroscopy) equipment used at BP.

It can be seen in Figure 33, that the partition coefficient determined at various concentrations is very similar. The significant feature is that the coefficient is in the order of 17,000. This indicates a very low system tolerance to solution borne copper impurities. On the other hand, any impurity introduced into the bath can be removed very rapidly by continual plating. In reality, a ”spike” copper impurity of 200ppm can be reduced to <20ppm by successive plating of approximately 4 runs as long as the source of the copper ions is no longer present in the solution.

Figure 33. Cu Partition Coeff vs. Cu Conc. in CdTe



3. Performance and Reliability

3.1 Device Performance Improvements: 0.55 m^2 Module

As described in the introduction, the initial size of the plate was 0.55m^2. The phase 1 and phase 2 deliverables of the sub-contract were based on this smaller sized module. After initial, CdTe optimization of time and temperature, the aperture area efficiency of the modules were in the 8% range.

Four 0.55m^2 modules were sent to NREL as deliverables during Phase1. The deliverable criterion for Phase 1 was for an active efficiency greater than 8% on a 14” x 61” module.

Table 11 shown below summarizes the results from measurements made at NREL. Spire 240A and outdoor measurements are shown for each module.

Table 11. 0.55m^2 Module Measurements Made at NREL

Module Number	Test System	Voc (V)	Isc (A)	FF (%)	Pmax (W)	Cell Eff. (%)
92030034	Spire 240A	24.7	2.53	0.61	38.2	8.1%
92030034	Outdoors	24.7	2.55	0.63	40.0	8.4%
92030041	Spire 240A	24.4	2.62	0.60	38.2	8.1%
92030041	Outdoors	24.5	2.63	0.63	40.4	8.5%
92030055	Spire 240A	24.8	2.57	0.60	38.4	8.1%
92030055	Outdoors	24.8	2.61	0.62	40.0	8.4%
92080115	Spire 240A	24.6	2.57	0.62	39.5	8.3%
92080115	Outdoors	23.5	2.60	0.62	38.2	8.0%

The cell (aperture) efficiency was calculated from the active area of each cell. The total active area was 153cm^2 per cell with 31 cells in series connection. This gave a total active (aperture) area of 0.474m^2. All modules satisfied the deliverable criteria of >8.0% for Phase 1 of BP Solar's Thin Film PV Partnership program. Two modules were returned to BP Solar and were used as reference modules for performance testing.

One of the major efficiency limiting parameters at that time was the Jsc. From the table above it can be seen that the average Jsc for the measurements was 16.9cm^2. The following section describes the improvements in device performance as a result of decreasing the window layer thickness.

The potential benefits of a reduced window layer were discussed in the previous section. The optical improvement in reducing the window layer thickness from 1000Å to 500Å is seen as an increase in blue response in the 400nm to 500nm range. The increase in Jsc with reduced CdS layer was also shown earlier. It was found that on reducing the CdS layer significantly below 500Å that a loss in Voc and fill factor occurred. This is commensurate with increased shunting from micro pinholes in the CdS layer. One method to reduce the effect of this layer may be to introduce a high resistivity buffer layer between the CdS and conducting oxide film. This is, as yet, not fully proven in the electrochemical deposition process used at Fairfield especially when considering the sensitivity to potential drop that this system has.

A series of devices were made using a CdS film at 500Å. Some typical values for devices incorporating the reduced window layer are shown below in Table 12.

Table 12. Standard Process

Voc (V)	VOC/cELL (V)	Isc (A)	Jsc (mA.cm-2)	Pmax (W)	FF	Efficiency
26.46	0.827	3.19	21.0	54.3	0.64	11.1
26.57	0.830	3.18	20.9	53.3	0.63	10.9
26.22	0.819	3.08	20.3	51.1	0.63	10.5
25.96	0.811	3.09	20.3	50.0	0.62	10.3
26.26	0.820	3.05	20.1	49.0	0.61	10.1
25.89	0.809	3.03	19.9	47.3	0.60	9.7
25.78	0.806	3.02	19.9	46.0	0.59	9.4

Comparing the results with those using the standard process above, the main difference in the performance can be seen as an increase in Jsc. The difference in Voc is due to the latter modules containing 32 series connected cells instead of 31 as in the standard process cells. The increase in Isc relates to a Jsc change from an average of 16.9mA.cm^{-2} for the standard modules (1000Å CdS) shown above, compared to 20.3mA.cm^{-2} for reduced window layer modules. This gain is in line with the gain predicted by the loss analysis.

3.2 Device Performance Improvements: 0.94 m^2 Module

This section describes the effect on device performance transitioning to the larger area 0.94m^2 substrates. The first part describes the early performance of the large area devices and then the performance of these devices incorporating a reduced window layer.

Considerable effort was placed on large area development during this phase. One of the challenges for electroplating large areas is how to overcome potential drop within the conductive transparent oxide (CTO). While potential drops in the contacting connections to the plate are minimal, potential drops in the CTO between the connections can be substantial. If a substantial potential drop occurs in the CTO, then CdTe stoichiometry will vary, favoring Te rich or Cd rich CdTe deposits, depending on the extent of the drop within the plate. The technical team at BP Solar worked with suppliers to obtain CTO films with sheet resistances below 10Ω/sq. in order to reduce potential drop in the 61” x 24” (0.94m^2) plate. Initial results were encouraging, and films were obtained with good composition uniformity. Some of the first plates were fully processed without cutting down to smaller sizes. The results were very encouraging, indicating a good robustness of the process towards large area scale up. The performance of two of the plates was verified at NREL and the results are summarized in Table 13 below.

Table 13. 0.94m^2 Module Measurements Made at NREL

Module Number	Test System	Voc (V)	Isc (A)	FF (%)	Pmax (W)	Cell Eff. (%)
92440041	Spire 240A	44.92	2.476	.607	67.53	7.8
92440041	Outdoors	45.00	2.466	.623	69.08	7.9
92030054	Spire 240A	45.08	2.503	.615	69.43	8.0
92030054	Outdoors	45.19	2.477	.646	72.23	8.3

The electrical configuration of these modules consisted of 57 cells in series. The cell area was 152.3cm^2 giving an active are of 0.868m^2 and a total module area of 0.944m^2. All these dimension measurements, together with the electrical measurements were confirmed at NREL.

Initial results using the reduced window layer process on large area were also encouraging. The results below show typical values for a 500Å CdS film. Compared to the 14" wide substrate Voc and Jsc are only marginally lower for the 24" substrate. Jsc is probably lower due to increased light absorption in the thicker conducting oxide for <10Ω/sq. sheet resistance substrates required for large area deposition. The fill factor was considerably higher for the large area plates due to the lower sheet resistance. Some examples of the large area devices with the reduced window layer are shown below in Table 14.

Table 14. Examples of Large Area Devices with Reduced Window Layer Thickness

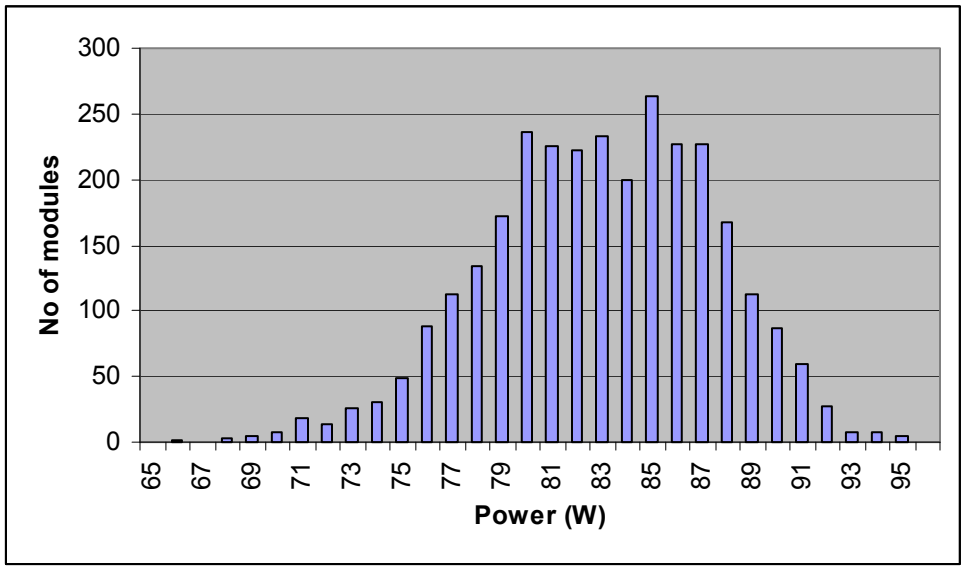
Module Number	Voc (V)	Voc/cell (V)	Isc (A)	Jsc (mA.cm^{-2})	Rs.cm^{-2} (Ω.cm^{-2})	Pmax (W)	FF	Eff. (%)
01010001	46.17	0.810	3.07	20.18	8.08	89.6	0.632	10.3
01010012	46.62	0.818	3.02	19.85	8.17	89.6	0.636	10.3
01010018	46.32	0.813	3.00	19.73	7.54	90.3	0.649	10.4
01010019	46.52	0.816	3.03	19.89	7.60	91.0	0.646	10.5
01010021	46.28	0.812	3.00	19.72	7.63	90.0	0.647	10.3
01010023	46.57	0.817	2.97	19.48	7.66	89.7	0.649	10.3
01010025	46.18	0.810	3.04	19.96	6.24	89.7	0.640	10.3
01190016	45.30	0.795	3.05	20.03	8.25	86.4	0.626	9.9
01190022	46.52	0.816	3.03	19.90	7.84	88.6	0.629	10.2
01190025	46.06	0.808	3.10	20.34	9.20	87.8	0.616	10.1
Average	46.25	0.811	3.03	19.91	7.82	89.26	0.637	10.3

Four modules were sent to NREL for measurement confirmation. These modules were also to be used as primary references by the Apollo® team at Fairfield. NREL measured one of the modules as having an aperture efficiency of 10.6% with a power of 91.5W.

Since this period, NREL has confirmed an 11% aperture efficiency module with a power of 92.5W. The efficiency was higher with only a 1W power increase because of a reduced aperture area, albeit on a full 0.94m^2 substrate.

A typical pre-production power distribution is shown below in Figure 34.

Figure 34. Histogram of Module Power for Apollo 0.94m^2 Product



The average power for this distribution obtained in March 2002, was 82.4W with a standard deviation of 4.6W.

This data shows that the device improvements obtained on 14" wide, 0.55m^2 modules were successfully transferred to the 24" wide, 0.94m2 module design.

3.3 Reliability Testing

This section will describe the work performed by BP Solar in determining module reliability through, indoor light soak testing, outdoor performance testing and environmental stability.

The main areas of work focused on internal light soak of full modules, external performance by establishing grid connected beta sites and small area stressing at IEC (UOD).

3.3.1. Outdoor Testing

Figure 35. Apollo® Grid Connected Array Layout at Fairfield California

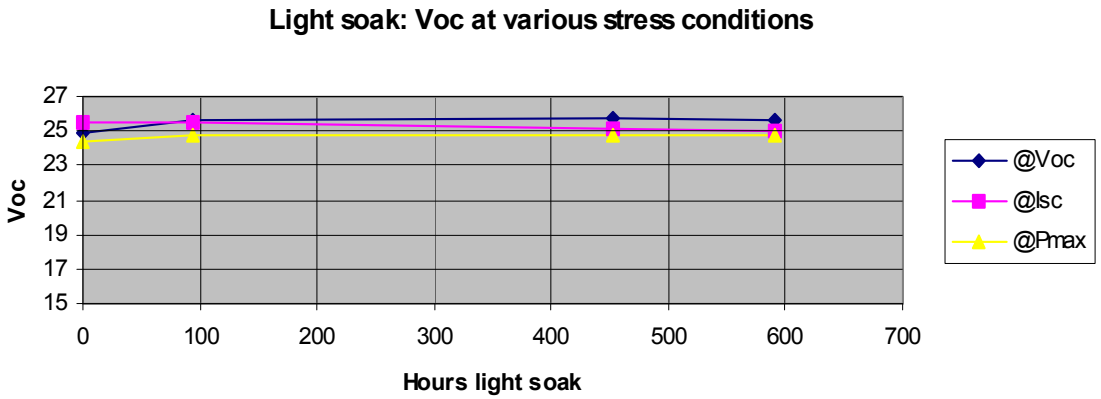
The arrays shown in Figure 35 were established in 1999 to determine the field performance of the Apollo prototype modules

During quarter 2 of phase 2, the BP Solar engineering staff installed the grid-connected system with 14" x 61" modules. A total 48 modules were installed on the system (back ground array). The average power of the new modules was 35W (STC) and therefore, the STC rating for the array becomes 1.68kW. The modules were connected in 4 groups of 12 modules. The DC output from the modules (Vmax and Imax) is logged on a regular basis, every 2 minutes.

In January 2000, a new array was commissioned on the grounds of the Fairfield facility. The array incorporates 60, 0.55m^2 Apollo® modules with an average STC performance of 38W each (foreground array in Figure X). This would give an equivalent array output of 2.28 kW (DC STC) assuming no system/inverter losses. The array is connected to an Omnion 2200 inverter. There are 3 sub arrays of 20 series connected modules. The inverter is bi-polar and a center tap is made between the 10th and 11th module. Each group of 20 modules is connected in parallel and before input is made to the inverter. The DC outputs of the sub arrays is monitored using shunt resistors to determine load current while DC load voltage is measured directly across each sub array. The readings are recorded in a shared data acquisition system (DAS). The DAS is shared with the 1st ground mounted system installed in 1999. Both systems are monitored every two minutes.

Some of the initial data from the newest array is shown in Figure 36.

Figure 36. Light Soak: Voc at Various Stress Conditions



On first appearance it looks as though there was a reduction in performance over the first 5 months of operation. In order to isolate system, module and/or temperature effects, the bottom row of 20 modules was removed and measured internally on a Spire 240A simulator. The results and comparison with pre installation values are shown in the Table 14 below.

Table 15. Spire 240A Measurements for String 1

DATE		Isc	Voc	Rs	Rsh	PMax	FF	Eff
1/12/00	average	2.71	25.2	2.99	219	38.4	0.561	7.87
6/12/00	average	2.71	25.2	2.38	152	39.0	0.570	7.97
Change	average	0%	0%	-21%	-31%	1%	2%	1%

It can be seen that the internal measurements indicate no change in module performance over the last 5 months of operation under load. The modules have been reinstalled and a similar comparison will be made once per quarter.

Out door performance will continued to be monitored over the long term.

3.3.2. Internal Light Soaking

New internal light soak stations were constructed during the project. The light soak stations were constructed to hold five, 0.94m^2 modules per unit. The modules can be held at Voc, Isc or Pmax. The Pmax is set using a simple variable resistor with the load current and load voltage displayed, real time, via a computer interface. The modules are forced cooled in air using a central fan. The lamps are 2kW metal halide and there are 4 lamps per unit. The temperature is monitored for each module and the light intensity is measured for uniformity using a 142cm^2 silicon cell. Average irradiance light soak station is measured using a CdTe reference module (Ref. module calibrated at NREL OTF). Typical light intensity and temperature ranges are shown in Table 16.

Table 16. Light Soak Intensity and Module Temp

Intensity	800$W.m^{-2}$	+/- 5%
Temperature	50C	+/- 5C

The typical electrical parameters, Voc, FF and Rs, for Apollo® modules at various stress conditions are shown in Figure 36. The performance of extended light soak is shown in Figure 38.

Figure 37. Light Soak: Voc at Various Stress Conditions

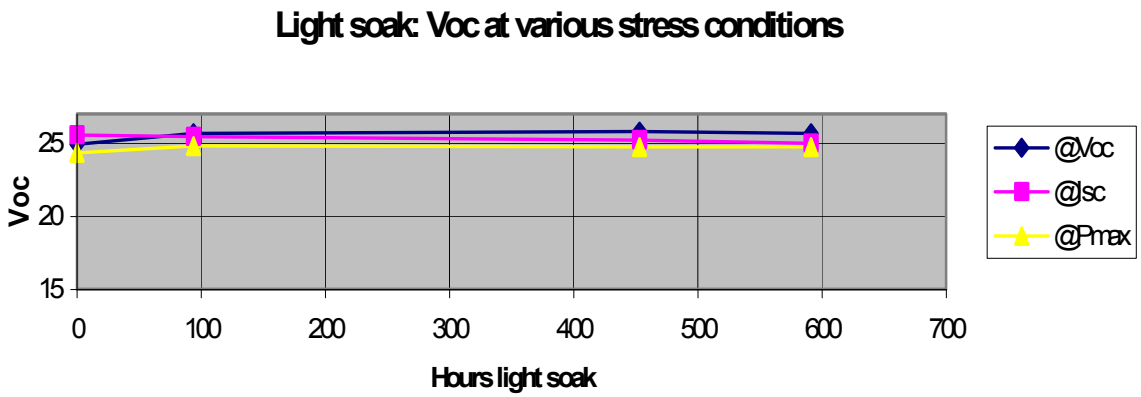
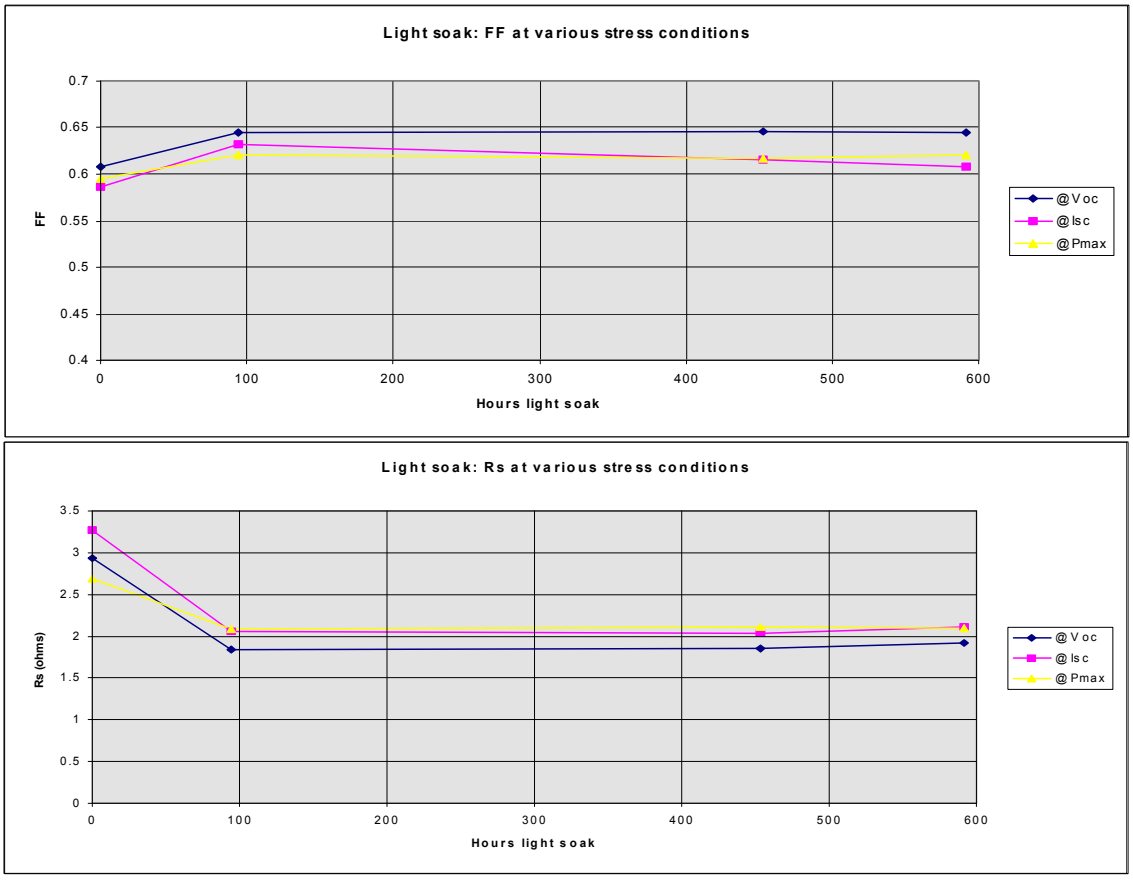


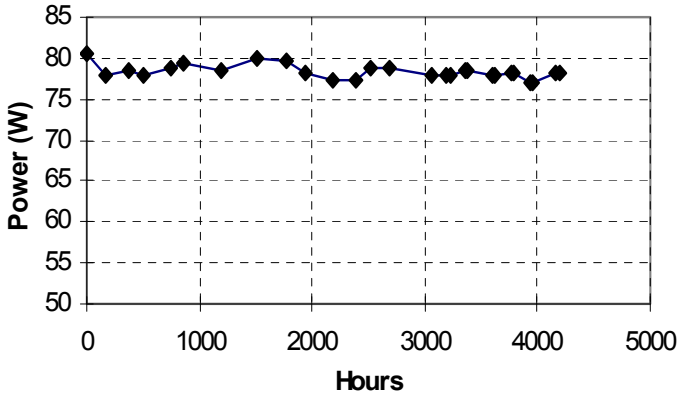
Figure 38. Light Soak: Effect on Fill Factor and Rs. at Various Load Conditions



Module Isc (not shown on a graph) and Voc show good stability at each condition. Fill factor also behaves in a similar fashion at each condition. However, in this case there is a decrease in the module series resistance in the first 100 hours that produced an increase in fill factor by about 5%. This effect is maintained throughout the light soak period. It is believed that this effect is evidence of the existence of traps within the absorber layer. These traps are passivated once the module is illuminated.

Long term exposure (>1500 hours continuous) shows good stability with less than a 4% change over this period. Performance is shown in Figure 39.

Figure 39. Extended Light Soak an Apollo Module

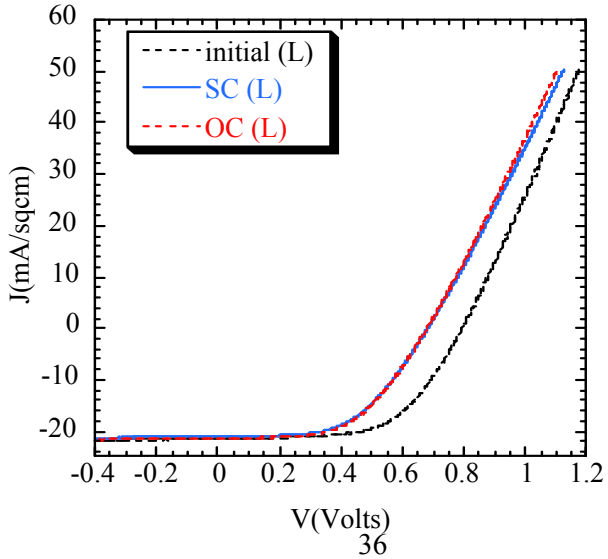


Light soak performance will be used as an important tool to define the effect of process parameters on stability.

3.3.3 Small Scale Stress Testing

Figure 40 shows the light soak performance of a 1cm^2 Apollo® cell on light soak at IEC (UOD) at various test conditions, Voc and Isc. At IEC, the cell was exposed to 100°C at one sun irradiance for 30 days continuous illumination. A small change in Voc was noted post stress. IEC showed this change to be reversible on removing the cell from the stress conditions. By three weeks, Voc had almost completely recovered.

Figure 40. Apollo Device After 30 Days Illumination at Short Circuit and Open Circuit



IEC also exposed cells to light and dark cycling at various temperatures, 25°C and 65°C. In all cases an amount of recovery was observed in the dark portion of the cycling. The temperature, which showed the least amount of change, was the 25°C temperature with light-dark cycling.

This work will be continued under a new DOE contract due to start in the second half of 2002.

4.0 Environmental Aspect for the Apollo Technology

4.1 Waste Treatment Optimization

During the period of the project, BP Solar worked with environmental consultant Radian International to investigate various methods of addressing issues that would effect large-scale production of CdTe panels using essentially an aqueous based process. The areas that were addressed in the project were:

- A feasibility study for close looping the wastewater plant for the production line.
- This included characterizing the composition of the wastewater streams.
- Developing process flow diagrams for the wastewater streams including loadings and concentrations for each leg.
- Defining specifications for an adequate reverse osmosis system.
- Definition of technologies capable of organic material removal and particulate removal.
- Treatment alternatives for the down stream process wastes.

A number of the potential alternatives for treatment of the down stream process wastes were evaluated with real waste solutions. A treat ability test plan was put together to assess the compatibility of the waste from the Apollo line and various technologies. Some of the techniques evaluated were novel, such as high shear membrane treatment and others were more established precipitation followed by filtration. In all cases solution samples were produced that accurately represented waste from various process steps.

One of the conclusions from the activity was that the waste streams are sufficiently complex that the removal of all organic and ionic species to level that could be sent to a reverse osmosis system is very difficult. However, while the goal of a totally close loop system was somewhat elusive, there were a number of knock improvements in the waste treatment systems that lead to operational and economic improvements in the processing of wastewater. In particular ultra-filtration of CdS particulates in from the wastewater lead to a much-extended lifetime for the ionic exchange resins (in fact to a loading that exceeded the manufacturer expectations) before regeneration was required. Also, a novel centrifuge system was specified and identified to remove organics so that the trace cadmium ions could be treated in house using the production ionization system rather than sent out for recycling.

4.2 Cadmium Recycling

BP Solar's approach to cadmium recycling has been one of working with companies that already have the ability to recycle glass coated with cadmium compounds. The philosophy of the companies product stewardship program is one that aims for a cradle-to-cradle approach. What this means is that ultimately we would like to use the same source for disposal and precursor procurement essentially making the mass balance for CdTe zero to the environment at the end of life for the module. This phase of the project was stated in the latter stages of the program and will be continued into the upcoming new PV Partnership program.

5.0 Summary

We consider project ZAK-7-17619-27 to have been a significant success for the Apollo technology. At the start of the project, the films were being deposited on square foot substrates at efficiencies of approximately 6%. The end of the project CdTe films were routinely deposited on areas of 10.1 square feet ($0.94m^2$) with aperture efficiencies of up to 11%. Moreover, this lead to the possibility of prototype products in the 80W and 90W range, a first for any monolithic thin film technology in the photovoltaic industry.

Internal light soaking both on large scale (full modules) and small-scale lead to greater understanding of the light induced behavior of the devices. Out door test beds at Fairfield needed more work than initially anticipated and other, non-module, issues needed to be de-convoluted from the actual system performance.

The environmental section was very useful in refining the best available control technologies used in the plant for abatement. Also, during the project, a product stewardship plan was established for the module placement in the field.

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13. ABSTRACT *(Maximum 200 words):* BP Solar first started investigative work on CdTe photovoltaics in 1986. The module product name chosen for the CdTe devices is Apollo®. The deposition method chosen was electrochemical deposition due to its simplicity and good control of stoichiometric composition. The window layer used is CdS, produced from a chemical-bath deposition. Initial work focused on increasing photovoltaic cell size from a few mm^2 to 900 cm^2. At BP Solar's Fairfield plant, work is focused on increasing semiconductor deposition to 1 m^2. The primary objective of this subcontract is to establish the conditions required for the efficient plating of CdS/CdTe on large-area, transparent conducting tin-oxide-coated glass superstrate. The initial phase concentrates on superstrate sizes up to 0.55 m^2. Later phases will include work on 0.94 m^2 superstrates. The tasks in this subcontract have been split into four main categories.

- CdS and CdTe film studies.
- Enhanced laser processing.
- Outdoor testing program for the Apollo® module.
- Production waste abatement and closed loop study.

14. SUBJECT TERMS: PV; transparent conducting (TCO); tin-oxide-coated glass; enhanced laser processing; monolithic thin films; modules; device performance; cadmium telluride (CdTe); electrochemical deposition; CdS/CdTe plating

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