

Specific PVMat R&D on Siemens Cz Silicon Product Manufacturing

**Final Subcontract Report
June 1998—September 2001**

T.L. Jester
*Siemens Solar Industries
Camarillo, California*



NREL

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

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Contract No. DE-AC36-99-GO10337

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NREL Technical Monitor: R. L. Mitchell

Prepared under Subcontract No. ZAX-8-17647-14



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Preface

This report describes work done by Siemens Solar Industries (SSI) from June 1998 to September 2001 during a three-phase Photovoltaic Manufacturing Technology (PVMaT 5A2) subcontract from DOE/NREL. The work focuses on improvements in the cost per watt of Cz modules and improved PV module manufacturing technology. The focus of the three year program is to implement a 17% efficient, 195 micron cell with a 30% reduction in manufacturing cost. In addition, the program developed a prototype 200 mm diameter cell with low cost module packaging. A final deliverable is a 50% reduction in slurry use through recycling of Silicon Carbide, and a 70% reduction in caustic waste.

Acknowledgments

Many people have contributed to the work under this contract. Thanks are due especially to Rick Mitchell, NREL technical monitor, Bryan Fickett, Greg Mihalik, Jeff Nickerson, Ken Sandland and the engineering staff at SSI.

This work was funded in part by DOE/NREL Subcontract # ZAX-8-17647-14.

Summary

Work focused on reducing the cost per watt of Cz silicon photovoltaic modules under Siemens Solar Industries' DOE/NREL PVMaT 5A2 subcontract is described in this report. Work on cell thickness reduction, the required electrical and mechanical changes to accommodate these thinner cells, larger cells and waste reduction are all described in this annual summary. Table i. shows the results of the program.

Table i. Program Plans and Results

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Thin Cell	16% efficient 125 micron prototype cells Complete	16.5% efficient 195 micron prototype cells Complete	17% efficient 195 micron production cells Complete
200 mm Product	12 " section of ingot sliced into wafers Complete	Prototype cells and modules Complete	4.5 Watt Cell in pilot production Complete
Recycling and Reduction of Chemicals	10% increase of slurry materials recycling and re- use Complete	20% increase of slurry materials recycling and re- use 13% reduction in caustic waste Complete	50% increase of slurry materials recycling and re- use 70% reduction in caustic waste Complete

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Introduction

Program Goals

The Photovoltaic Manufacturing Technology (PVMaT) project is sponsored by the U.S. Department of Energy (DOE) through the National Renewable Energy Laboratory (NREL) in order to assist the photovoltaics industry in improvement of module manufacturing and reduction of module manufacturing cost. The objective of the DOE/NREL PVMaT subcontract with Siemens Solar Industries (SSI) is to continue the advancement of Siemens Solar Industries' photovoltaic manufacturing technology in order to achieve a 30% reduction in module cost per watt at the end of three phases of work. Each phase lasts a year as shown in Table 1. Phase I of this subcontract began in June of 1998, Phase II in June of 1999, and Phase III in June of 2000. The program addresses the reduction in cost per watt with a three part development contract: a significant reduction in wafer thickness from approximately 400 microns at the start of the program to a finished cell thickness of 195 microns at the end of the three years, a significant increase in the size of the cells produced up to 200 mm diameter cells, a significant reduction of 50%, in the use of slurry materials, and 70% reduction in caustic waste.

Table 1. Goals of Siemens Solar Industries' PVMaT 5A2 Subcontract from DOE/NREL

	Phase I 1st Year	Phase II 2nd Year	Phase III 3rd Year
Thin Cell	16% efficient 125 micron prototype cells	16.5% efficient 195 micron prototype cells	17% efficient 195 micron production cells
200 mm Product	12 " section of ingot sliced into wafers	Prototype cells and modules	4.5 Watt Cell in pilot production
Recycling and Reduction of Chemicals	10% increase of slurry materials recycling and re- use	20% increase of slurry materials recycling and re- use 13% reduction in caustic waste	50% increase of slurry materials recycling and re- use 70% reduction in caustic waste

Approach

The first step toward reducing cost in this PVMat 5A2 program at SSI is to reduce wafer thickness. In PVMat 4, cell size was increased to 150 mm in diameter. Large thin wafers have the potential to be the lowest cost wafer as the Cz growth process produces round ingot. Large wafers are the best candidates to make thinner from a cost perspective, however the yield losses at 150 micron thickness have been found to be excessive. For this reason, the approach has been a two step reduction in thickness, from 385 microns to 250 micron cells, and then from 250 microns to 195 micron cells during Phase III.

The cost per watt reduction affected through both the PVMat 5A2 program and other programs at SSI have shown significant progress. Figure 1 shows the \$/Watt reduction for the last three years. The total cost reduction for all three years is over 35% referenced to the start of the program.

About half of the cost to produce a solar module is incurred by the time a wafer is produced, and another 20% is added in the cell processing steps (Figure 2). In large area wafer and cell production, the manufacturing costs are reduced by increasing the area of the wafer, this benefit is compounded as the wafers are made thinner. Siemens Solar Industries has studied, developed and piloted processes for 250 micron thickness cells in both 103 mm and 150 mm sizes. A significant finding in this work has been to improve the efficiency of the cells produced from 14% to over 16.5%. A requirement to control the quality of the ingot produced surfaced as the cell efficiencies became higher and controls were put in place to ensure process optimization in ingot growth.

Figure 3 shows the top cost drivers in dollars per kilowatt. The focus on Silicon Carbide is clear as well as the fact that the thinner, larger cells lower the contribution of each of the other components in dollar per watt costs. The Silicon Carbide cost reduction was targeted at 50% total.

Figure 4 shows the productivity gains in the factory over the phases of the program. Significant reduction in labor has been obtained by making wafers thinner and larger.

The larger cells are made, the lower the potential dollar per watt. SSI has initiated the development and growth of 200 mm ingot to be fabricated into wafers and eventually cells. These larger cells continue to show the best cost structure as it optimizes the watts per kilogram consumed in producing the cells. Module designs for lower cost contribution have been started.

Hazardous waste reduction is attacked in two ways, the largest consumable item aside from polysilicon is Silicon Carbide (SiC) used in the wafer slicing process. This SiC use can be reduced significantly through recycling and re-use. This program approach is well underway at SSI. The largest hazardous waste volume at SSI is the caustic waste generated in the wafer etching processes. The reduction of this waste has been accomplished using subcontractors with extensive environmental compliance

experience such that the solution is driven by best available techniques, lowering operating cost as a secondary motive.

These three areas of focus, thinner cells, larger cells and modules and hazardous waste reduction have the potential of reducing cost by approximately 30% per watt.

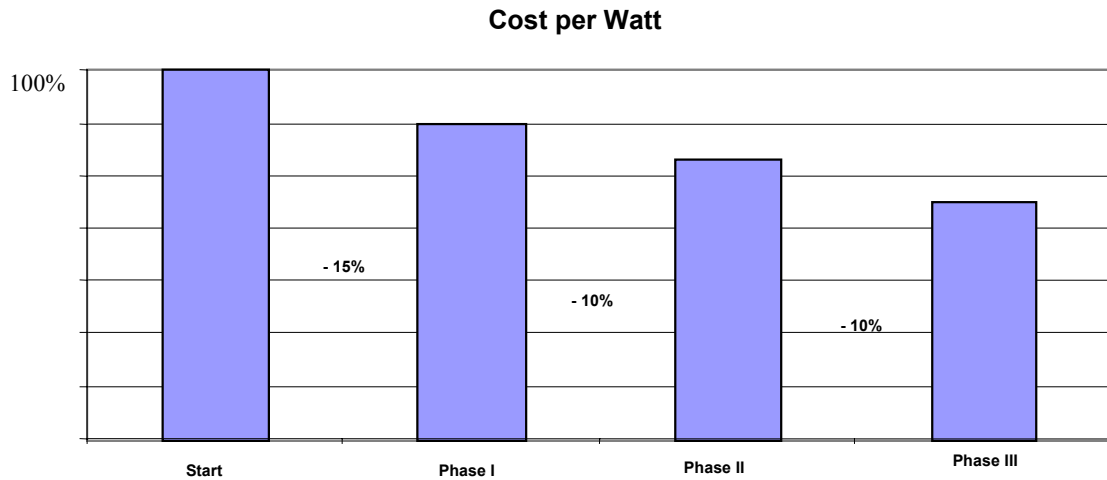


Figure 1. Cost per Watt vs Year

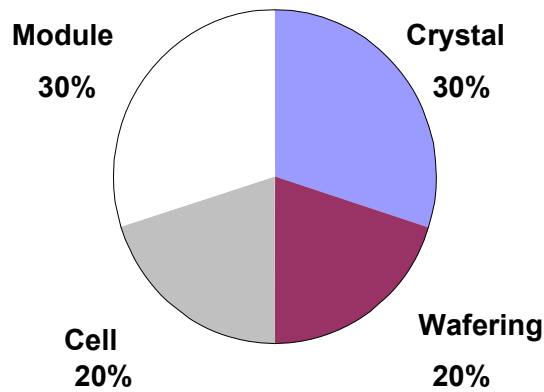


Figure 2. Cost per Watt Category

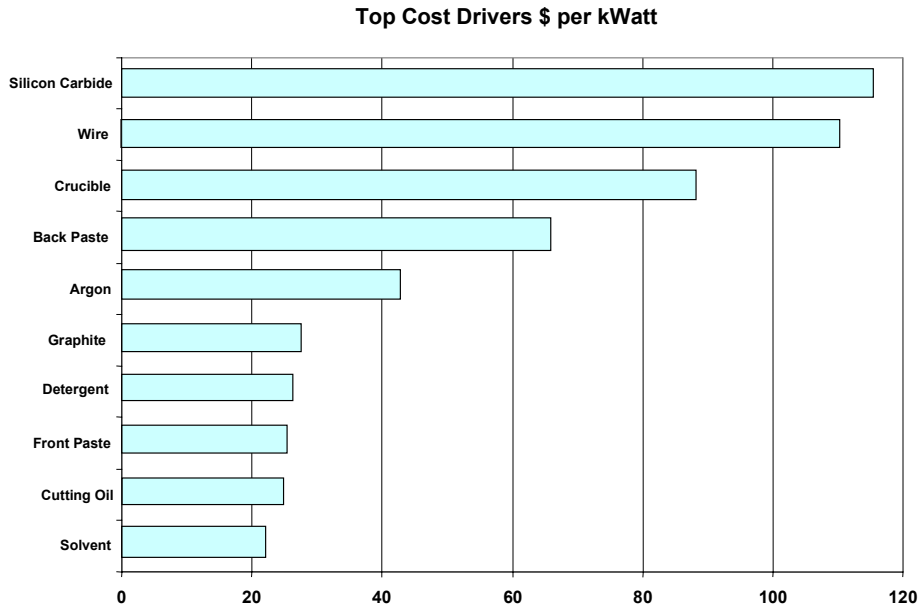


Figure 3. Dollar per kilowatt costs

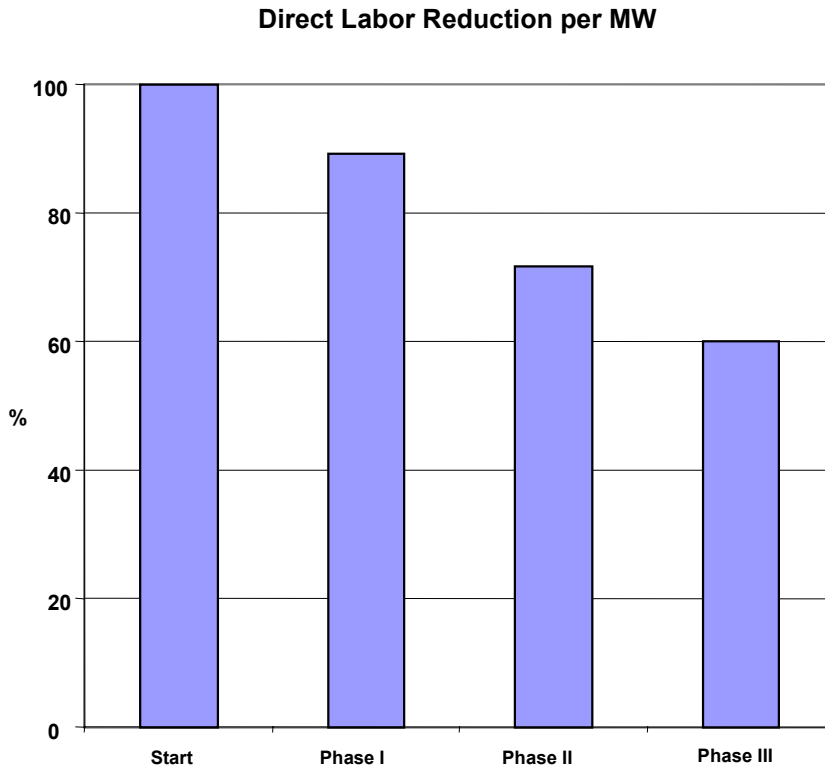


Figure 4. Productivity Gains

Thin/High Efficiency Cells

Thin Wafer Production

The making of thinner cells in the manufacturing process has a large cost advantage. This assumes no loss to yield problems. Figure 5 is a summary chart of previous testing done during our PVMat 4 contract¹ which shows wafering yield loss by part size and thickness. These data were gathered on a pilot run series of three ingots per part size and thickness and followed a systematic trend. In general the bigger the wafer, the lower the yield, and the thinner the wafer, the lower the yield.

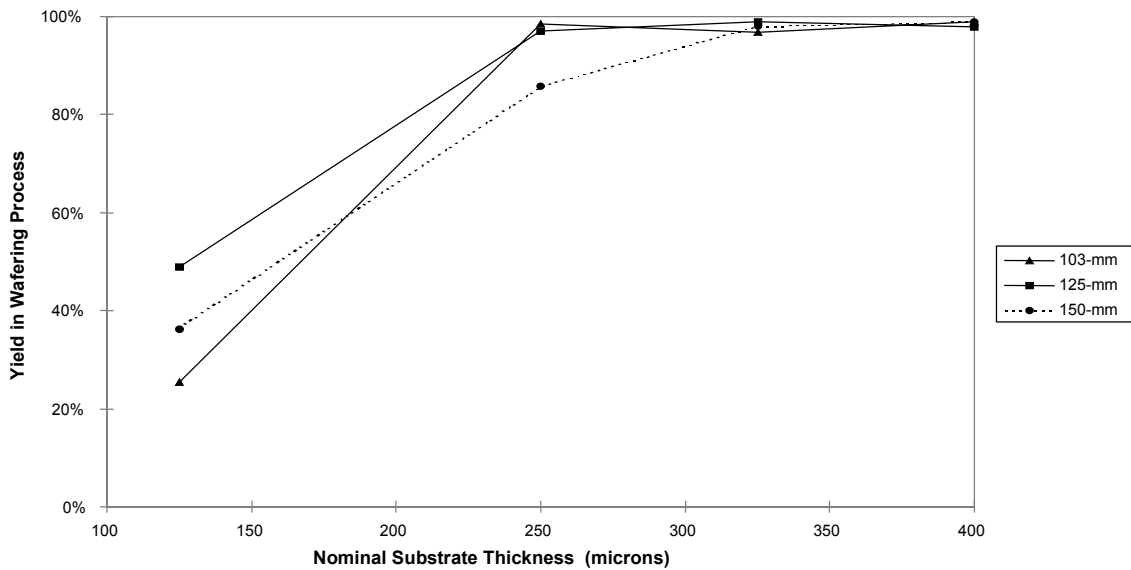


Figure 5. Thin Wafer Yield

250 micron Wafers:

Two runs with one mono and one tri-crystalline ingot each were cut on the same wire saw. The first run showed machine problems resulting in a high frequency of double cuts for the bottom ingot. The second run went without problems. The results of both runs are shown in Table 2.

Table 2. 250 micron Wafering Test Results

Material	Ingot name	Table position	Length	Number of wafers	Yield (%)
Mono	310314A	Top	393	855	99
Tri-Si	620805F	Bottom	391	754	88
Mono	630313B	Bottom	405	828	93
Tri-Si	620701C	Top	406	864	97

150 micron Wafers:

Two attempts were made to cut one mono and one tri-crystal ingot with 150 μm thickness. Both attempts failed as both top and bottom ingots were almost completely cut in chips and doubles. During the first cut a failure in the slurry pump system was detected and repaired. The second run however showed double cuts after cutting in the first 10 mm. A possible cause for the higher risk of doubles could be the decreased groove depth for the 150 micron. Pictures of the roller grooves (Figures 6 and 7) showed that standard and thin wafer rollers are machined with the same or similar wedge shaped tool with the same wedge angle. In order to achieve a smaller groove distance the depth of the grooves decreases proportionally: the groove depth of the standard roller is about 50% larger than the depth of the 150 micron rollers. In addition to the roller pictures the decreased groove depth was confirmed by a dial depth gauge. Further investigation is necessary to confirm whether the groove depth is a relevant issue for thin wafer cutting.

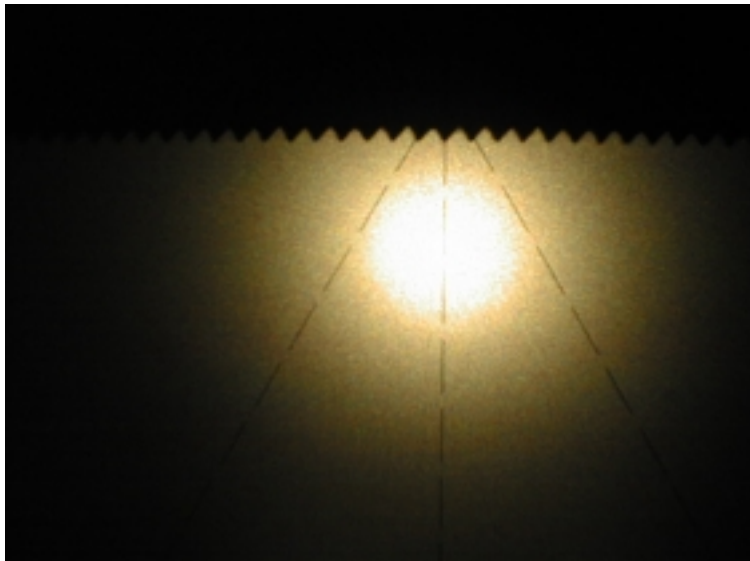


Figure 6. Standard Roller Grooves

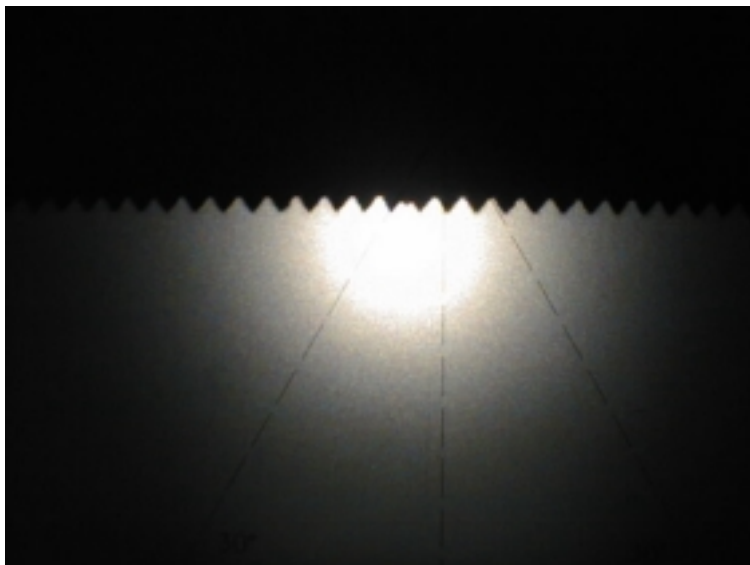


Figure 7. 150 micron Roller Grooves

Over 40 trial runs have been done on thin wafer cutting. The mechanical yield results are summarized in Figure 8. Based on the information gathered during all trial runs, SSI will focus efforts on cutting 200 thick wafers. It can be assumed from the data that the process would result in similar and overall more wafers produced. Assuming we can duplicate our current electrical yields at 200 microns, SSI will produce 180 to 200 more wafers per wafering run (Figure 9), a productivity gain of over 15% in watts and labor.

Wafering Yields @ Various Thicknesses and Effective Change to Efficiency (No BSF)

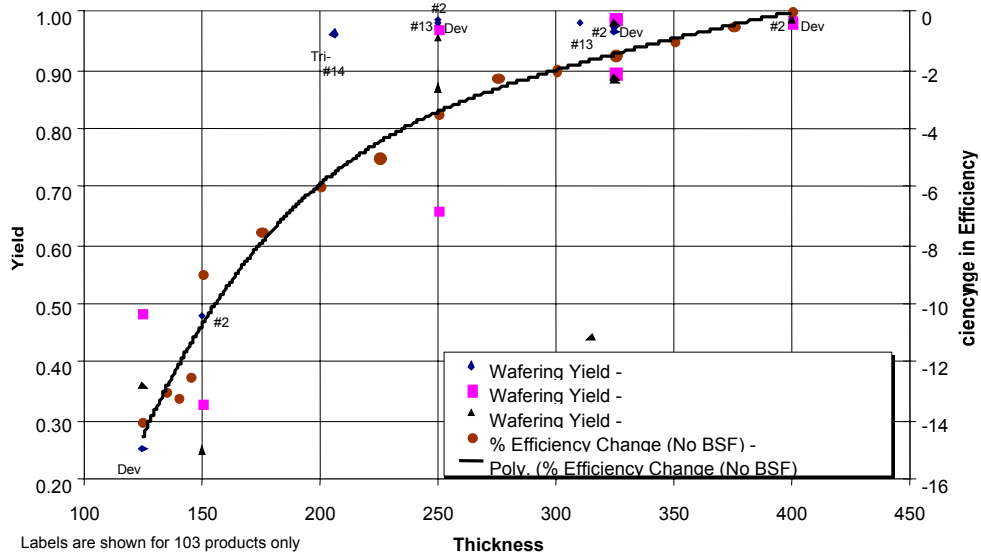


Figure 8. Wafer Pilot Runs vs. Thickness

**Calculated and Actual # of 103 - Wafers @ Varying Thicknesses
Wiresaw Process Only**

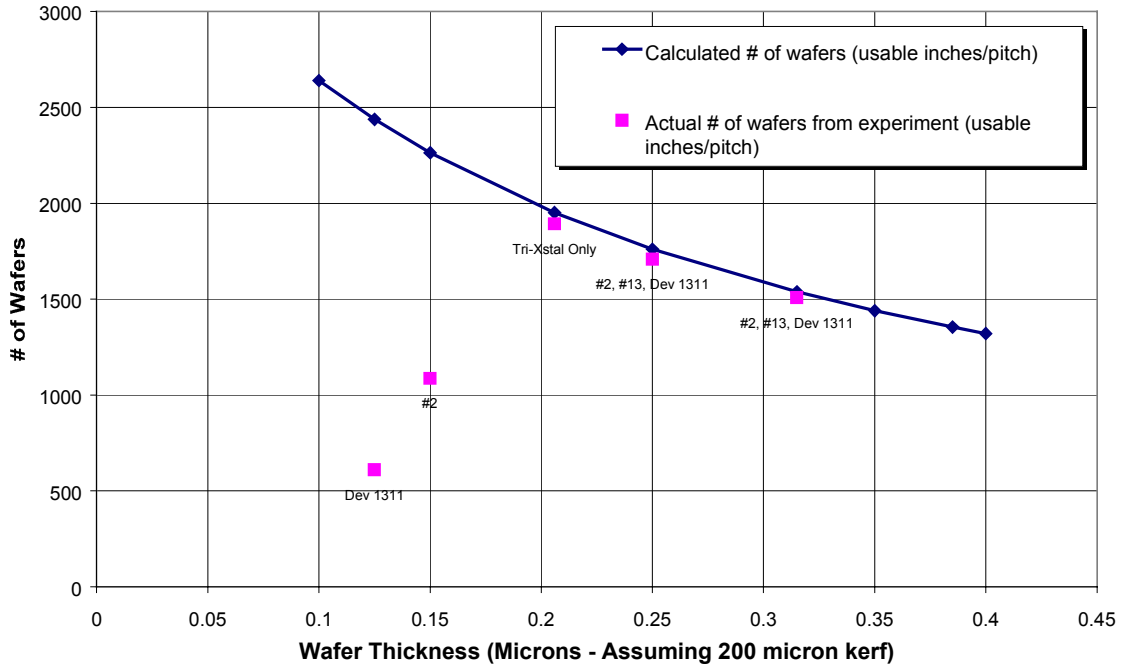


Figure 9. Wafering Productivity vs. Thickness

Thin Cell Processing

A pilot run of 125 micron thick cells were made during the last month of Phase II. Figure 10 shows the yield losses by operation incurred during the test run. The wafers were processed manually and included a Boron back surface field (BSF). All the wafers were evaluated electrical properties. The front and back screens were not optimized to take advantage of the BSF. A comparison of cell performance is shown in Figure 11, showing the optimized and non-optimized screen effects. Robots were not used and all load and unload functions were completed manually.

The mechanical yield losses of the thin cells exceeded 30% in total, offsetting the gain in productivity possible from wafering these thin wafers. Again, the cell thickness limit appears to be in the 200 micron range for high yield and better overall productivity and cost.

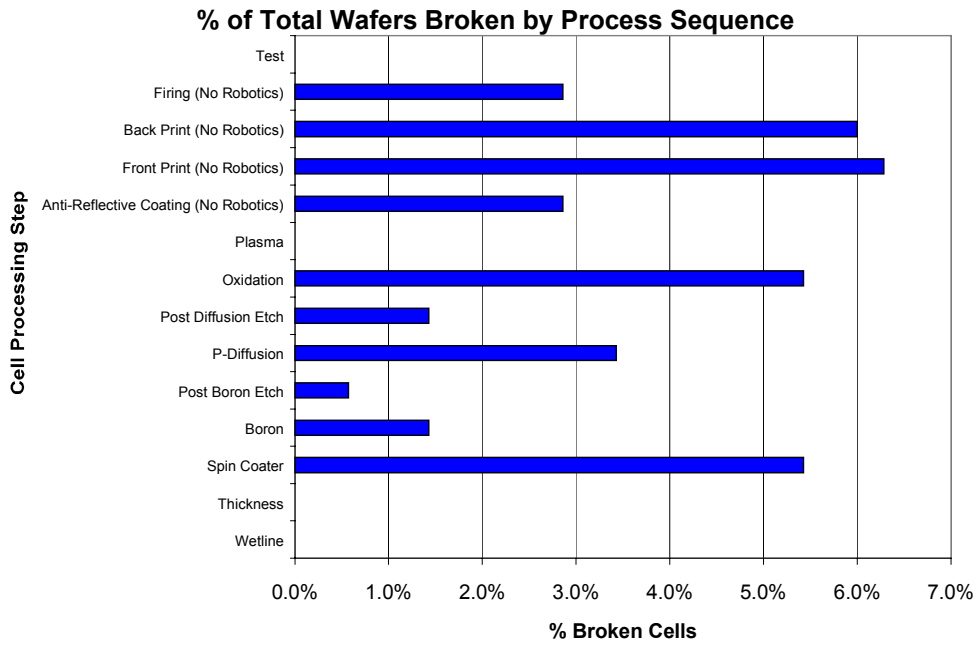


Figure 10. Yield Losses of 125 Micron Cells

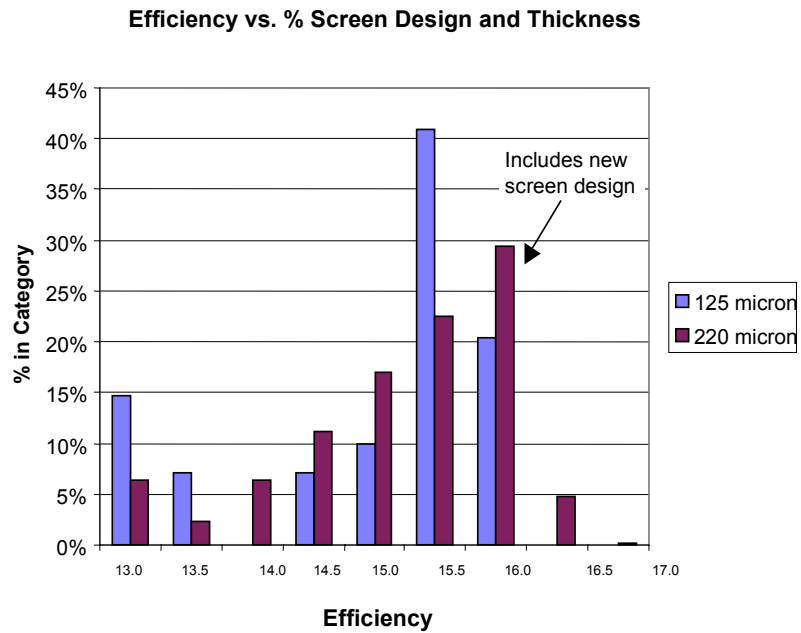


Figure 11. Thin Cell Efficiency

Boat to Boat System :

The Boat to Boat Transfer system (BTS) performs automated mass transfer of wafers from plastic to quartz boats and back again. The system was designed to accommodate all product lines manufactured at SSI. Its main purpose is to reduce wafer breakage by over 0.5% in four transfer steps. The BTS has been installed and released to production.



Figure 12. BTS System in use at SSI

The image above (Figure 12) shows the BTS system in operation at the clean room at Siemens Solar Industries' cell processing facility. Wafers from a quartz boat, following a diffusion process, are being transferred to a plastic boat. The wafers are slowly picked up and positioned above the plastic boats. Once in place, the wafers are gently lowered into the plastic wafer slots. The baskets are cleared and the process is repeated.

The productivity of the BTS is roughly 1/3 the productivity of a manual operator. The amount of operator involvement to setup and unload the BTS is close to the current labor load, 30 seconds versus 35 seconds. The productivity statistics are shown in Table 3. Initial tests on yield show no yield gain in use of the BTS (Tables 4 and 5). Further optimization also showed no strong benefit to using the system so an alternative called gentle dump transfer was developed.

Table 3. BTS Cycle Times vs. Manual Transfer of Cells

	Setup Time (Seconds)	Process Time (Seconds)	Removal Time (Seconds)	Total Cycle Time (Seconds)	# of Wafers Processed	# Wafers Processed per minute
BTS Targeted - Times for R-line (6"-wafer)	15	58	0	73	100	82
BTS Measured - Times for R-line (6"-wafer)	15	60	15	90	100	67
Manual Measured - Times for R-line (6"-wafer)	0	35	0	35	100	171

Table 4. Manual Transfer Yield Statistics

Rep ort Date	Time	B-Diffusion		PBE		P-Diffusion		PDE		Oxidation	
		Total	Scrap	Total	Scrap	Total	Scrap	Total	Scrap	Total	Scrap
6-Jul	Day	872	3	2086	14	1192	10	2673	27	2600	20
6-Jul	Nite	1989	11	600	0	1185	15	892	8	800	0
7-Jul	Day	1863	12	2100	0	1925	25	900	0	793	10
8-Jul	Day	1484	16	1800	0	1785	15	2095	5	2577	23
8-Jul	Nite	1113	12	1108	13	1050	35	1782	18	1385	15
9-Jul	Nite	2610	15	0	0	0	0	0	0	0	0
10-Jul	Day	2478	22	2987	13	2065	10	2073	27	1988	12
10-Jul	Nite	2841	34	2700	0	2591	19	1500	0	600	0
11-Jul	Day	1993	7	2379	21	2368	38	2376	24	1800	0
11-Jul	Nite	2858	17	2694	0	1775	25	2082	18	1985	15
12-Jul	Day	2300	0	3000	0	2538	12	2545	0	1594	14
12-Jul	Nite	1491	9	900	0	2250	32	1500	0	3535	25
13-Jul	Day	1740	10	2100	0	1938	12	2100	0	2590	17
13-Jul	Nite	372	3	1498	2	1350	57	2089	11	2110	10
14-Jul	Nite	2493	7	1792	8	1020	30	300	0	400	0
15-Jul	Day	2369	6	1784	16	1637	13	2073	27	1795	20
15-Jul	Nite	2979	21	1197	3	1629	21	898	2	1000	0
16-Jul	Day	2117	8	2386	14	2081	19	2682	18	1975	25
16-Jul	Nite	2988	12	1792	8	2077	23	300	0	800	0
Totals		38950	225	34903	112	32456	411	30860	185	30327	206
% Yield Loss			0.578%		0.321%		1.266%		0.599%		0.679%

Total Yield Loss for Manual processing is 3.44%

Table 5. BTS Transfer Yield Statistics

Rep ort Date	Time	B-Diffusion		PBE		P-Diffusion		PDE		Oxidation	
		Total	Scrap	Total	Scrap	Total	Scrap	Total	Scrap	Total	Scrap
17-Jul	Day	1250	10	2710	0	2106	31	2700	0	2390	20
17-Jul	Nite	25	25	1800	19	1841	41	2100	18	1837	52
18-Jul	Day	1750	15	2200	0	2100	8	3000	0	2200	10
18-Jul	Nite	500	5	610	0	1069	19	1624	0	2200	20
19-Jul	Day	2385	12	2100	29	1500	12	900	23	1600	0
19-Jul	Nite	2000	10	900	12	1050	10	1200	12	1000	0
20-Jul	Day	3490	14	3590	27	2950	29	2668	32	2390	10
20-Jul	Nite	3375	5	1734	0	2550	32	1490	13	1600	25
21-Jul	Day	1850	25	2100	0	1444	6	2100	0	0	0
21-Jul	Nite	2996	25	0	0	1184	16	630	6	1190	10
22-Jul	Day	3000	0	3000	0	1488	20	2700	0	2525	85
22-Jul	Nite	3858	17	1470	30	3300	82	1787	13	2980	20
23-Jul	Day	3950	20	3600	0	2977	35	3300	0	1985	19
23-Jul	Nite	2620	5	0	0	0	0	1659	15	3175	25
24-Jul	Day	1622	3	5398	15	4218	7	3579	21	1520	8
24-Jul	Nite	5236	14	3589	11	3422	28	2991	9	2766	34
Totals		39907	205	34801	143	33199	376	34428	162	31358	338
% Yield Loss			0.514%		0.411%		1.133%		0.471%		1.078%

Total Yield Loss for BTS processing is 3.606%

The gentle dump transfer tools were easily developed using designs from the supplier of quartz diffusion boats and the supplier of the plastic cassettes used in the chemical etching and cleaning processes. The process is shown in Figure 13 and has been implemented in production with a yield gain of over 1%.

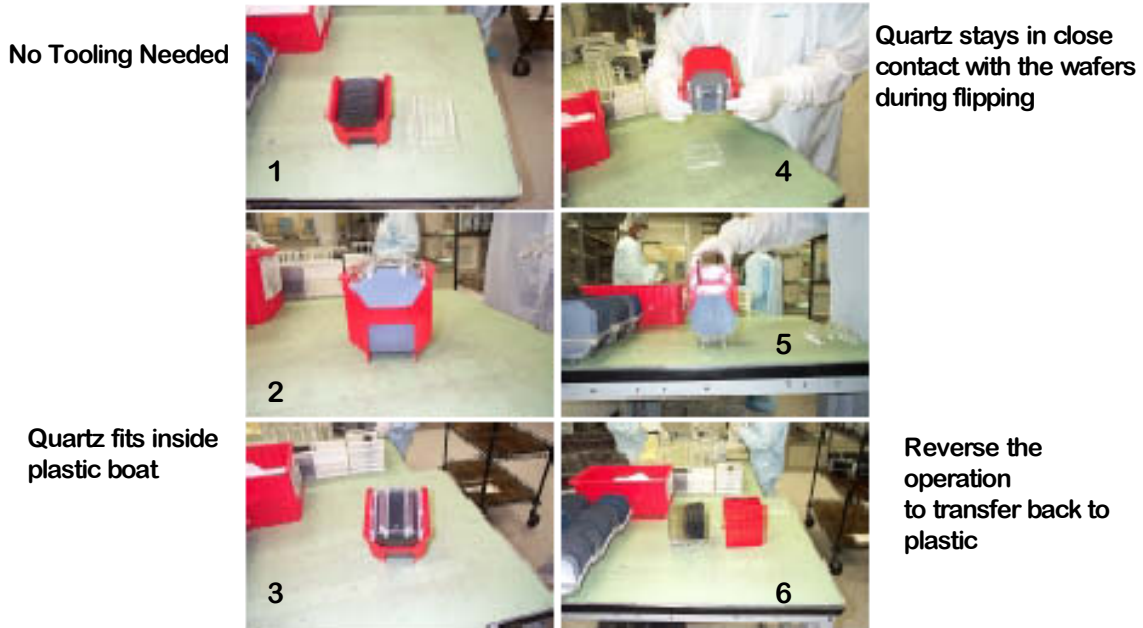


Figure 13. Gentle Dump Transfer

Back Surface Fields in Production:

The need for a Back Surface Field (BSF) to offset the electrical efficiency drop as wafers are made thinner has been reported in Phase I of this program^{2,3}. Figure 14 shows the performance of Aluminum and Boron BSF processes vs. thickness of the cell. The Boron BSF has been implemented in production. The electrical performance distribution using this process is shown in Figure 15 with averages above 16% efficiency. Optimization of the process was done with tuning the sheet rho in the phosphorous diffusion process. It was found that lowering the sheet rho slightly from approximately 54 ohms/cm² to approximately 50 ohms/cm² improved the I_{vr} or test current significantly. Figures 16, 17 and 18 show the contrast between the test group 1 and control group 2 with respect to sheet rho, I_{vr} and fill factor results.

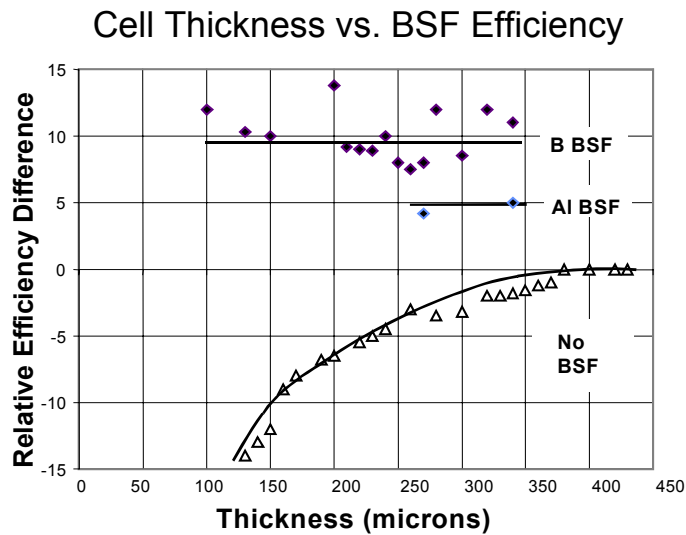


Figure 14. Back Surface Fields Performance vs. Thickness

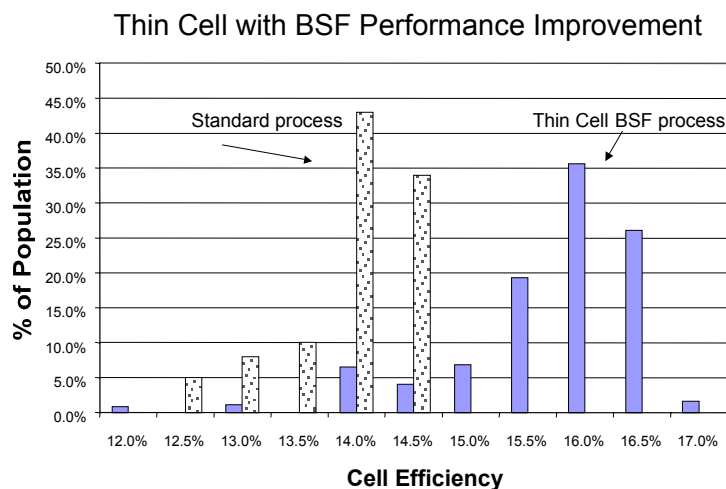
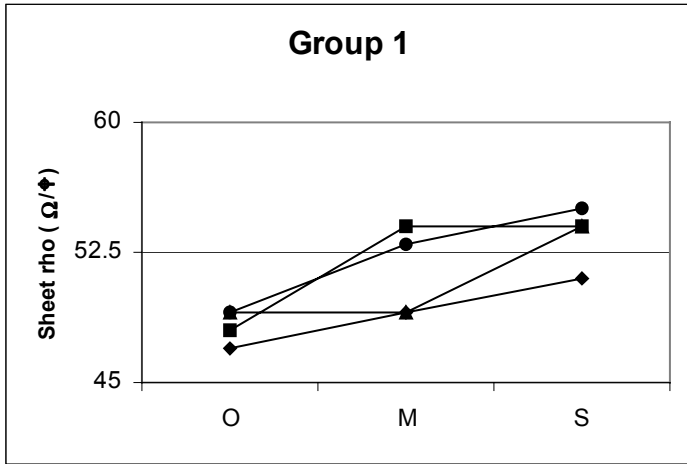
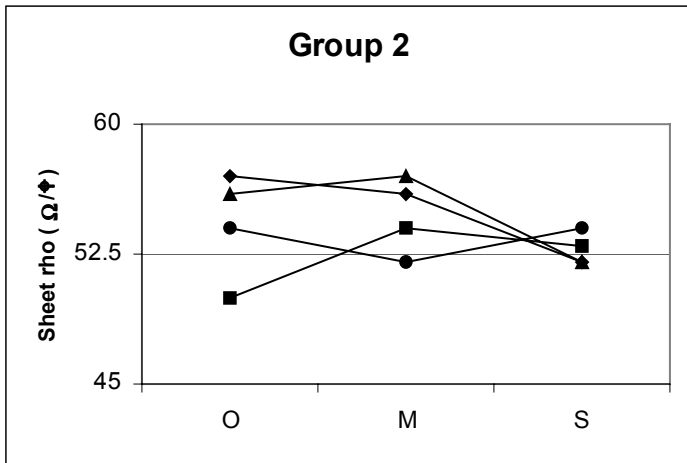


Figure 15. Boron BSF Cell Performance



Sheet rho for experimental group v. tube position



Sheet rho for control group v. tube position

Figure 16. Sheet rho for Control vs. Test Group

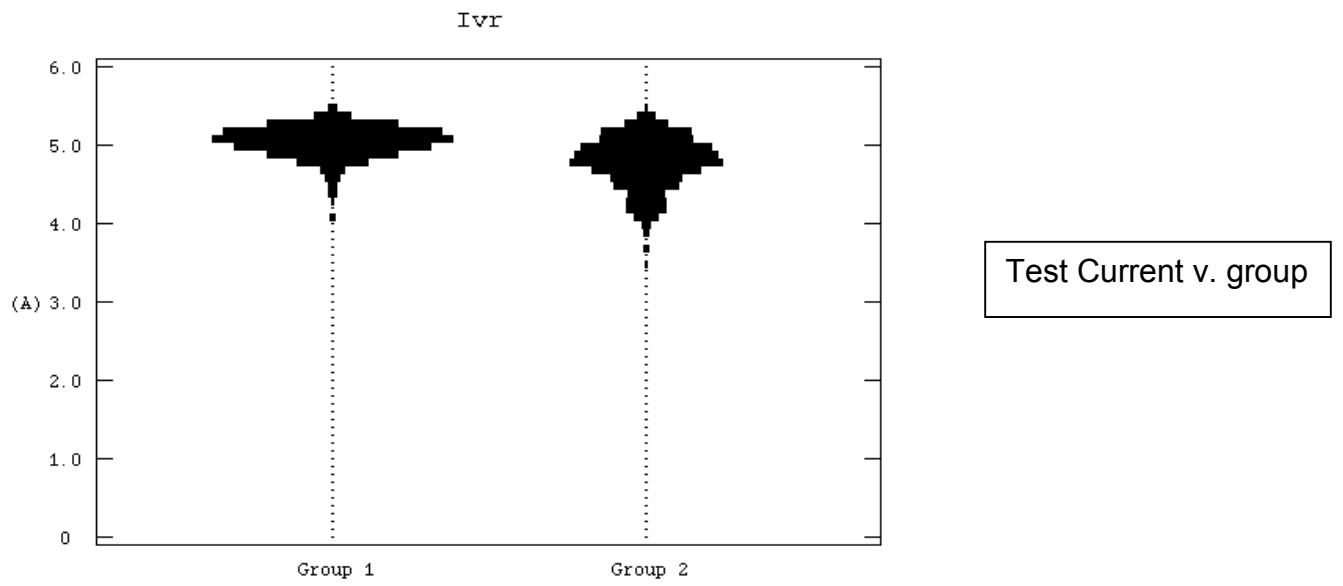


Figure 17. Ivr for Test Group vs. Control Group

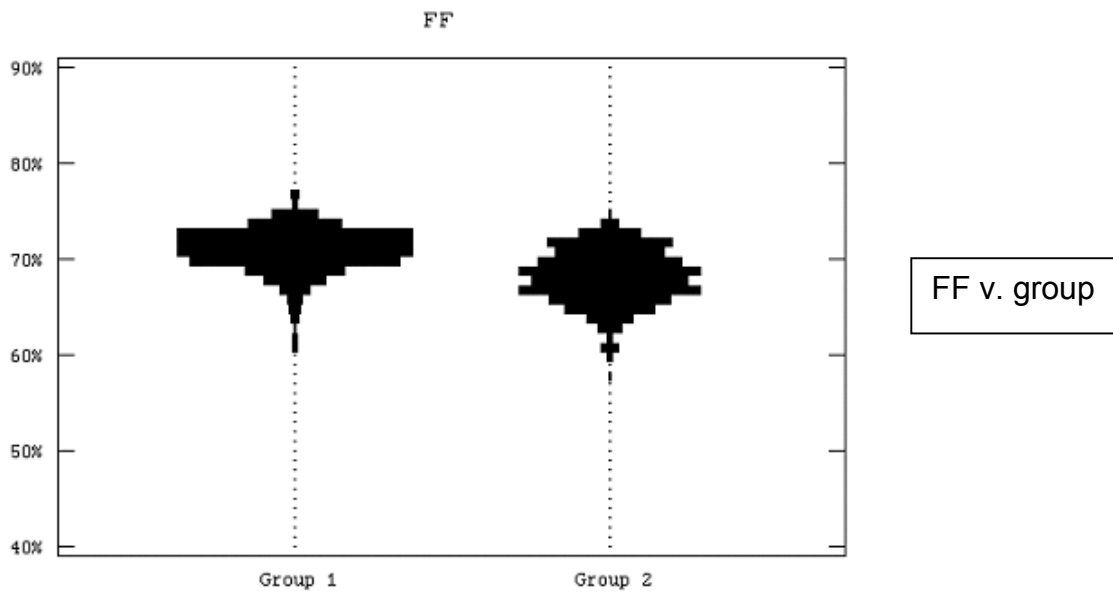


Figure 18. Fill Factor for Test Group vs. Control Group

Ingot Quality:

Reproducibility of the high efficiency runs was also low due to problems with the electronic quality of the ingots produced using recharge processing. Recharging is a cost reduction program implemented in the crystal growth process where the crucible is filled again and re-used without the machine being cooled off or the vacuum level changed. This process change had resulted in significant improvement in growth yields and productivity in our plant in Vancouver, Washington.

A model was developed looking at the starting polysilicon purity and the resultant "lifetime" of the ingot. The ingot lifetime was measured using a new tool developed by Ted Czekik's group at NREL. A correlation study was done linking the measurement of pucks or tail sections from ingots, measurements of the wafers produced prior to diffusion and measurements of the wafers after phosphorous diffusion and thermal oxidation processing. The lifetime measurements made on the wafers both pre and post diffusion were made using the tool developed by Ron Sinton and further measurements were done in making cells out of the wafers measured. The results are shown in Figures 19, 20, 21 and 22.

Figure 19 shows the correlation of the model to the recharge process. The ingot lifetime measured throughout the ingot and from recharge run to recharge run shows a predictable decay in electronic quality through each successive run.

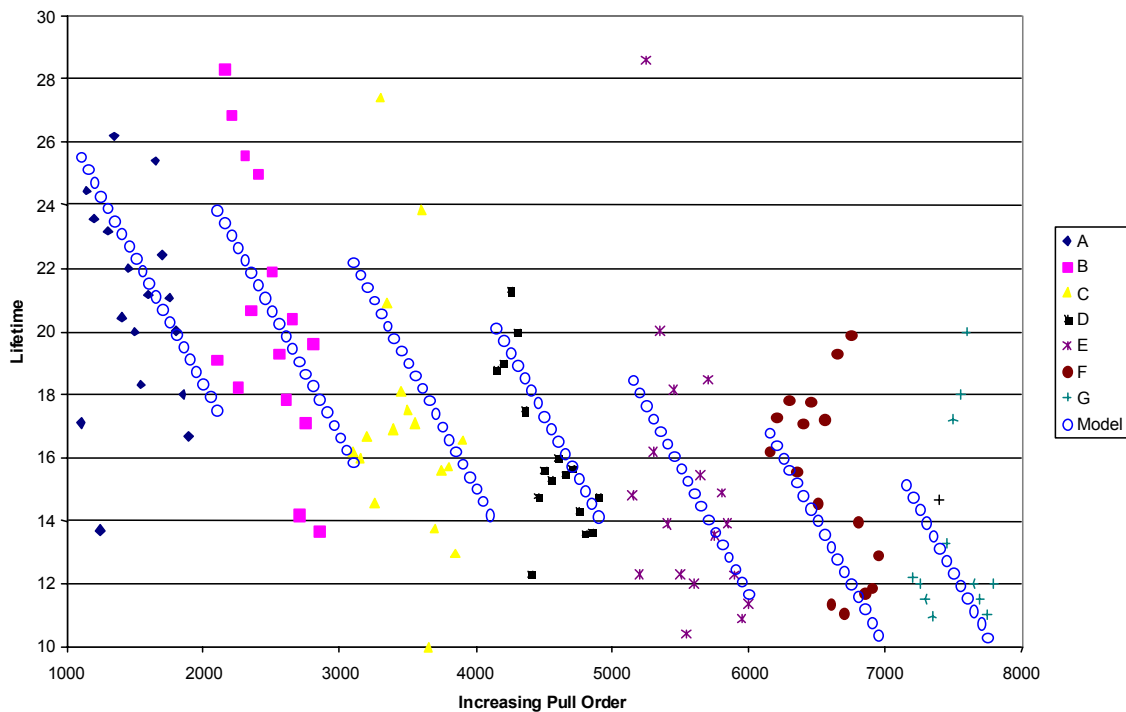


Figure 19. Ingot Lifetime vs. Recharge Run

Figure 20 shows the correlation of ingot puck lifetime to pre-diffusion lifetime and from pre-diffusion lifetime to post diffusion lifetime.

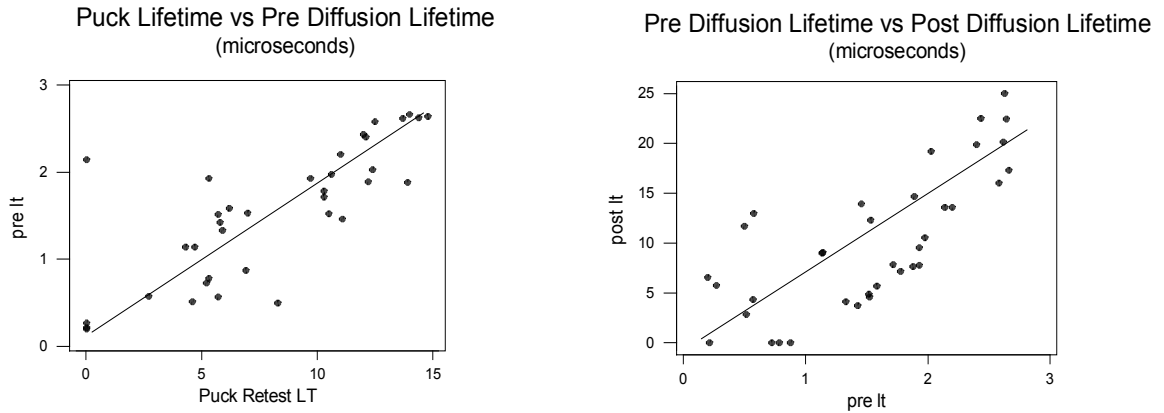


Figure 20. Lifetime vs. Process Condition

This strong correlation showed the usefulness of the ingot measurement tool to predicting the quality of the solar cell produced.

Figure 21 shows the average Voc * Isc vs. lifetime measured post oxidation, which again shows a strong correlation of lifetime to ingot quality.

Post Diffusion Lifetime vs Ingot average Voc*Isc

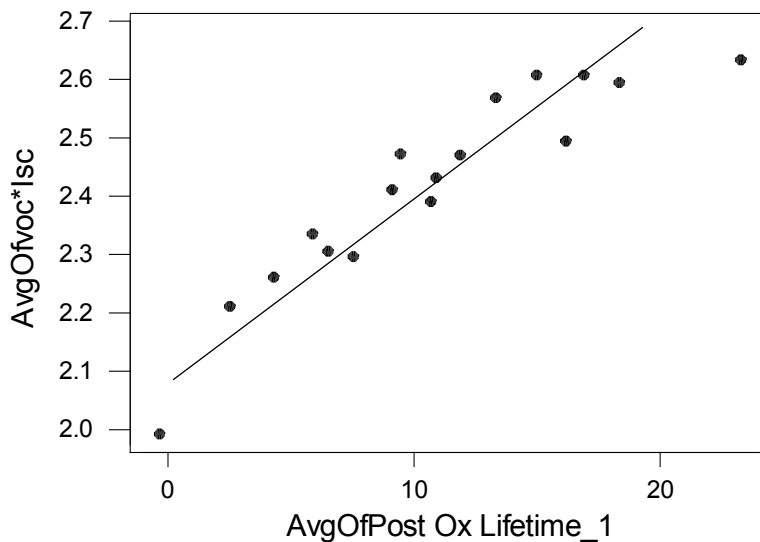


Figure 21. Ingot average Voc* Isc vs. Post Diffusion Lifetime

And finally Figure 22 shows the efficiency vs. post oxidation lifetime measurement.

Cell Efficiency vs Wafer Lifetime After Oxidation

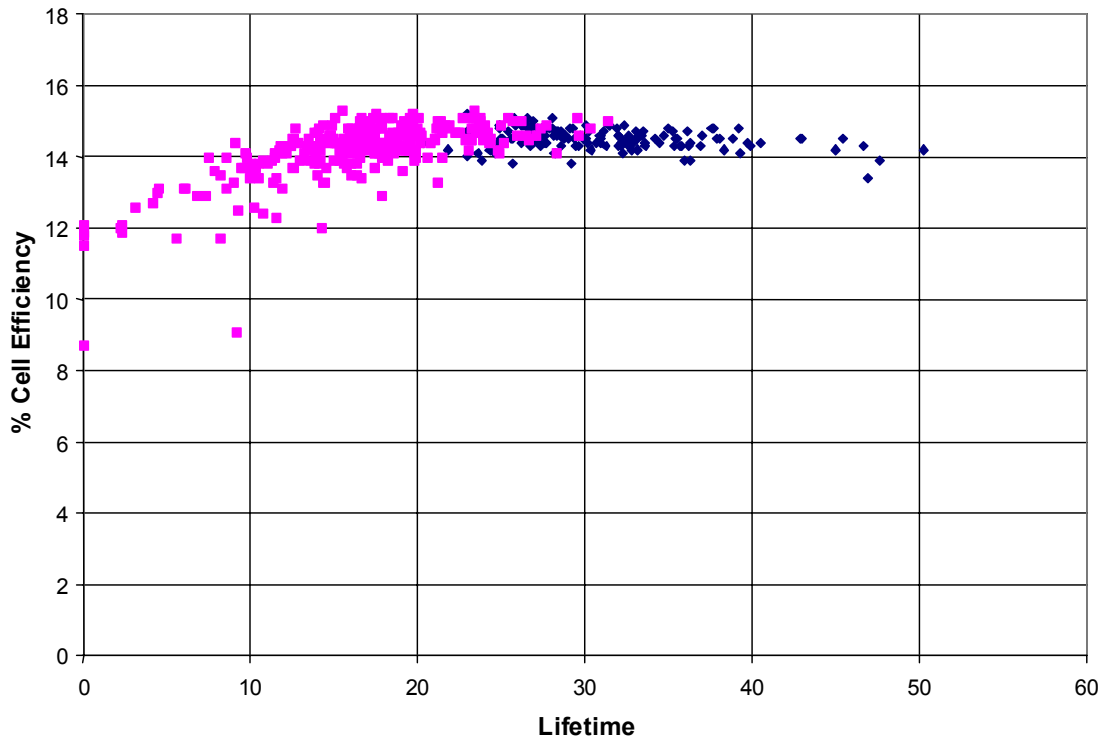


Figure 22. Cell Efficiency vs. Lifetime after Oxidation

The results of this work has been to implement 100% screening with the ingot lifetime tool to qualify ingot prior to the production of wafers and cells and to implement the post oxidation tool in a sampling mode.

Post Diffusion Etch effects:

A final source of instability in the making of high efficiency >16% cells was the control of the post diffusion etch process for removal of the diffusion glass. Figure 23 shows the effect of etch time on the test current of groups of cells. The optimum time is set at 5 minutes now for this process and measured each run.

Post Diffusion Etch Time vs. Test Current

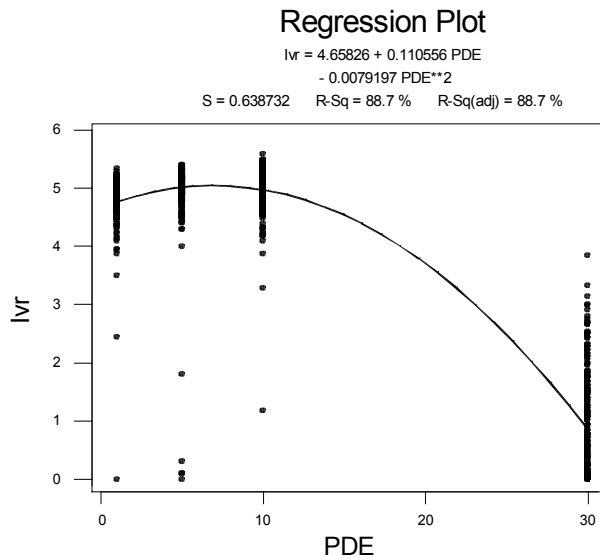


Figure 23. Post Diffusion Etch time vs. Test Current

Large Area Cells/Large Area Modules

200 mm Cells and Modules

Figure 2 shows the cost breakdown for SSI silicon solar modules. As can be seen, the ingot and wafer cost represents a total of 50% of the dollar per watt consumed in making a module. The wafering costs consist of the crystal growth component, and the wafering component. The crystal growth component of 30% can be highly leveraged by increasing the ingot size. (Currently SSI ingots are 150 mm diameter in the largest size produced.) By producing 200 mm diameter ingots, the watts produced are increased by over 30% in one crystal growth run. A given crystal growth run costs approximately the same amount for a given amount of polysilicon solidified, so that a 40 kg charge producing 103 mm ingots vs. 200 mm ingots is approximately the same. The 103 mm ingot produces 2600 watts per run, while the 200 mm ingot produces 3350 watts per run. This increase of watts produced represents a greater than 10% reduction in the \$/watt contribution at the ingot level.

The wafering costs of materials increase with increasing area, however the increased cost per unit is offset by the larger area and wattage produced by the wafer. Table 6 shows the contrast of 103 mm vs. 200 mm wafering costs and the cost contributions in total \$/watt. A given wafering run will produce 2200 watts of 103 mm product vs. 5400 watts of 200 mm product.

As can be seen by the chart the wafering cost contribution can be reduced by over \$0.08 per watt, and when combined with the crystal growth cost per watt the potential cost reduction using 200 mm ingot is in excess of 12%. This is one of the tasks outlined in Phases II and III of the above mentioned contract.

Table 6. Wafering Costs for Larger Diameter Wafers

Cost Category	103 mm Wafer (\$/W)	200 mm Wafer (\$/W)	\$/Watt Saved
Wire/Slurry/Solvents	.20	.20	0
Labor	.13	.09	.04
Depreciation	.07	.03	.04

Assumes 14.3% efficient cells in both cases, 103 mm wafers are 315 microns thick as cut with 180 micron kerf, 200 mm wafers are 385 microns thick as cut with 180 micron kerf. (1.5 Watts per 103 mm cell, and 4.5 Watts per 200 mm cell.)

200 mm Ingot Growth:

The growth of 200 mm diameter ingots is a relatively simple conversion of processing. A majority of the crystal growers in SSI's Vancouver facility are computer controlled and can be set up for 200 mm diameter tracking. Several ingots have been grown using the computer controlled tools (Figure 24).



Figure 24. 200 mm ingot as grown

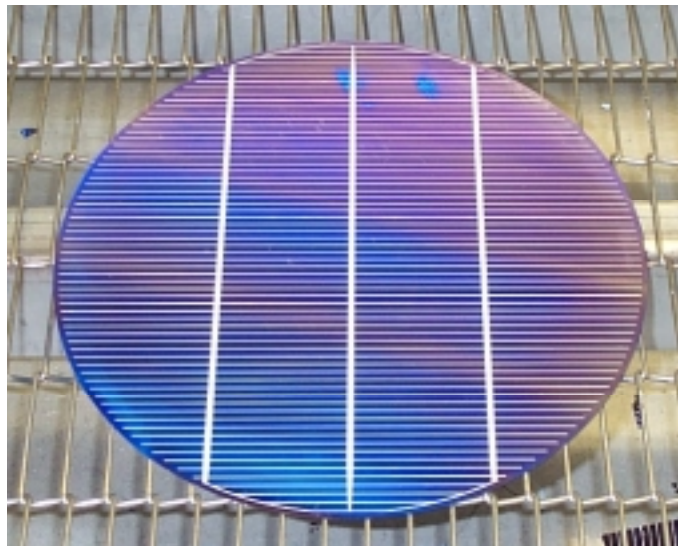


Figure 25. 200 mm cell in process

200 mm Cell Processing:

Approximately 1500 200 mm diameter cells have been processed (Figure 25) in pilot test runs in the Camarillo facility. Several tools in the fabrication sequence were upgraded to handle these larger cells. The diffusion furnaces required larger tubes, which were installed in new furnaces. The printing plates and vacuum chucks were modified to handle these cells in low volumes, any new equipment purchased will have 200 mm capability. Testing tools were modified as the high current produced by the cells exceeded our capability to measure the cells.

200 mm Module Processing:

Frameless modules have been produced using 200 mm diameter cells. The first module shown in Figure 26 uses 200 mm diameter cells as grown in the round shape. This module is approximately 160 Watts in performance and is approximately 6.5 feet long by 3 feet wide.

A second module using the cells shaped into a square is 130 Watts in power and is approximately 5.5 feet long by 2 feet wide. This module is shown in Figure 27.

The benefits of the larger cells again showed the processing of more watts per labor hour invested and more watts per machine hour used. The gains are significant and a ramp up is planned in manufacturing of these cells for production and sale.

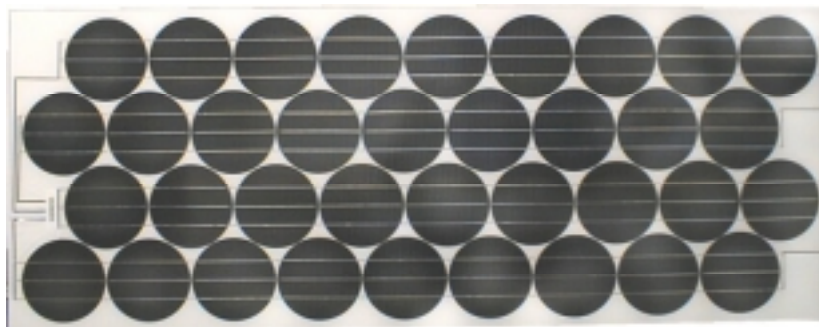


Figure 26. 160 Watt Module made with 200 mm cells

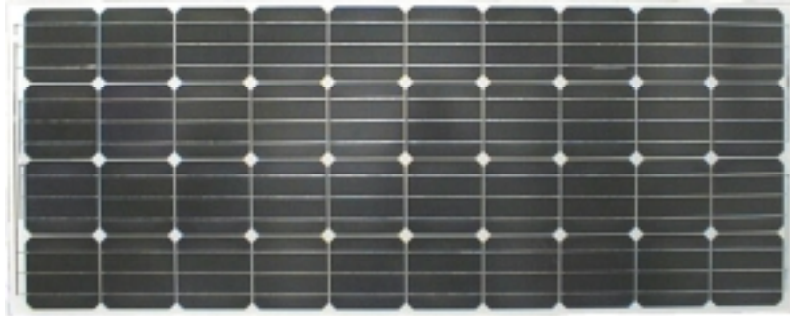


Figure 27. 130 Watt Module made with 200 mm cut cells

Hazardous Waste Reduction

Silicon Carbide Recovery

The work on recycling Silicon Carbide (SiC) under the contract has proceeded well. As background for the work, Silicon Carbide is the second highest cost driver in the manufacturing process SSI has deployed (Silicon feedstock is number one). A recycling unit has been deployed at SSI for two years and the results have been very positive.

There is variation in the amount recycled over time in our plant due to problems with the equipment. Figure 28 shows the SiC use by month, and how it varies due to the uptime of the SiC recovery machine. The machine was not used during Month 13, showing typical use rates without recovery. The best uptime obtained on the equipment has been during Months 17 and 18, which occurred with improved uptime of the equipment at >95%.

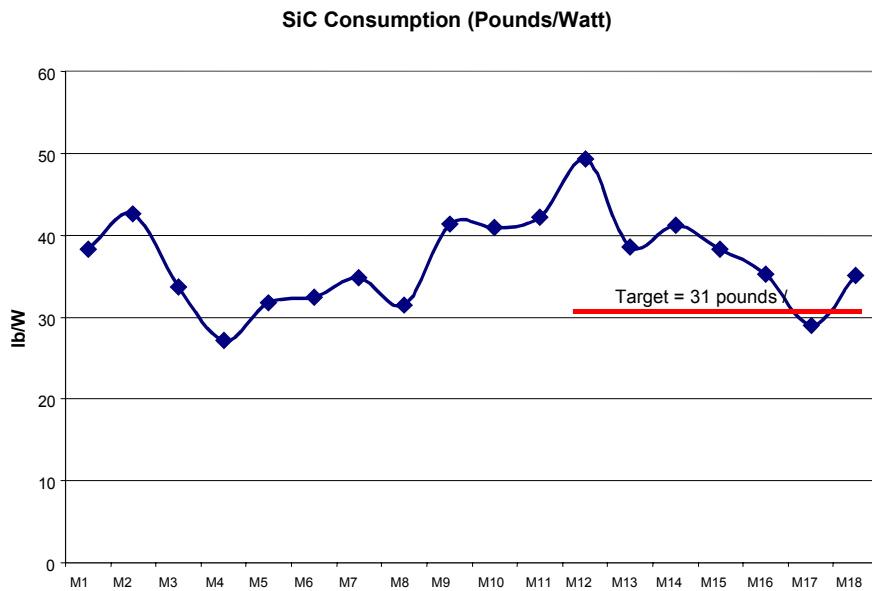


Figure 28. Silicon Carbide use per month

Several tests have been done to evaluate the effects of recycled SiC on yields in wafering. Figure 29 shows the dependence of wafer surface condition or “waviness” on fresh vs. recycled SiC. The recycled material tends to have more “wavy” wafers which are rejected under our current criteria. The root cause for this is under investigation.

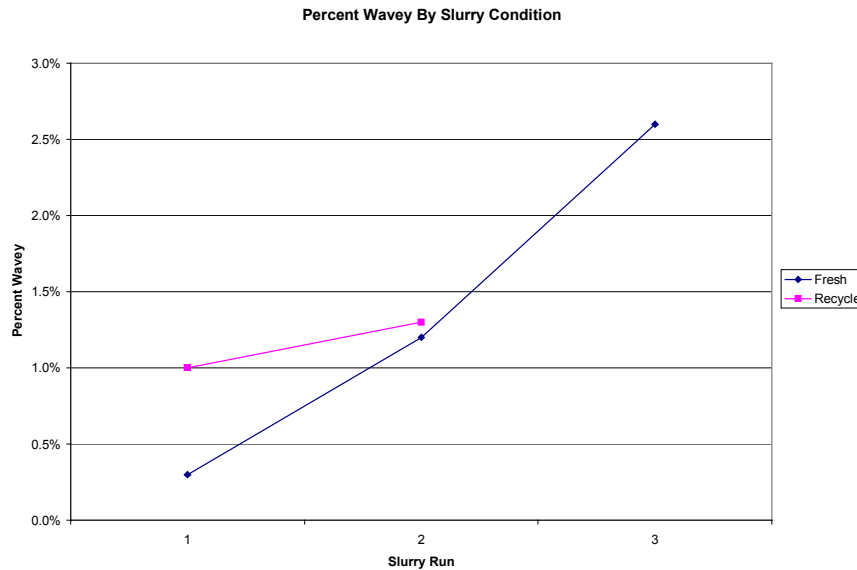


Figure 29. Wafer Surface vs Slurry condition

Figure 30 shows the process recipe flowchart being used with the recycled SiC. SSI has found that a “blended” SiC process using recycled and “new” SiC produces the best results both financially and from a process capability metric. Figure 31 shows the reduction in SiC (waste and use) affected by the program. This represents a 5% savings on a \$/Watt level. The first two years reduction was done with the system purchased and as our volume grew the system was not able to keep up with the demand. A new system is being installed this calendar year which is capable of meeting our needs for the next five year’s growth.

An added benefit to this work has been a significant process improvement in wafer thickness control as shown in Figure 32 where the solid line represents a higher yielding or more capable process.

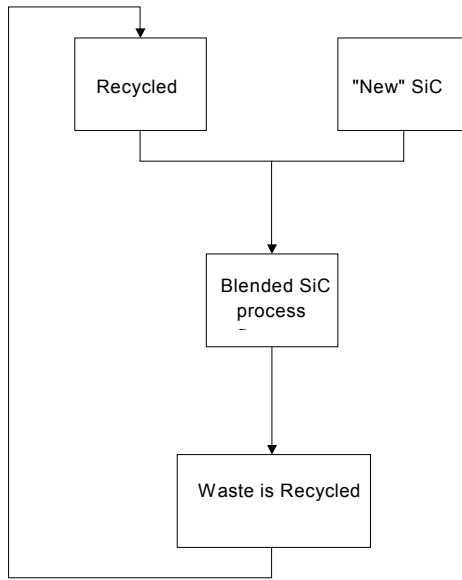


Figure 30. SiC Process Flowchart

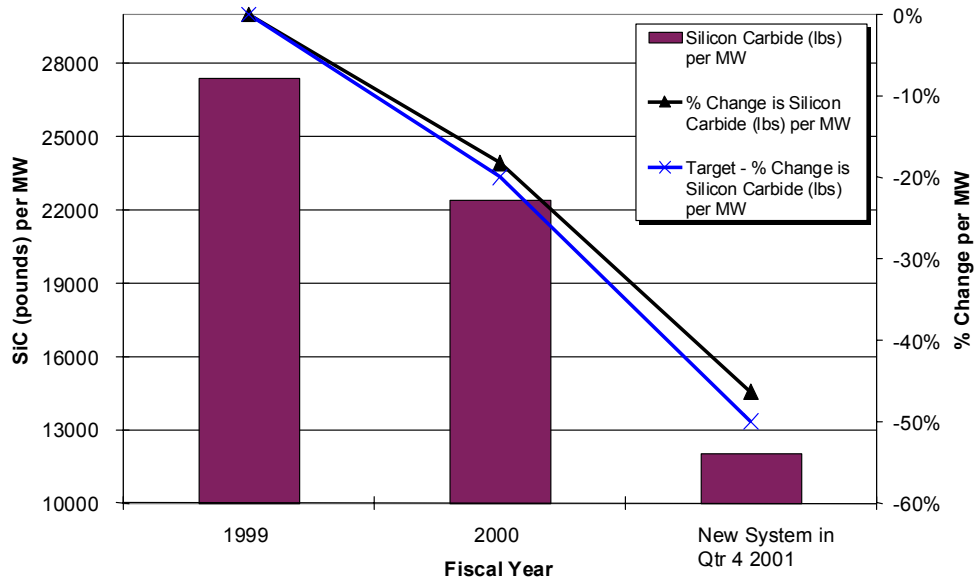


Figure 31. Silicon Carbide Waste Reduction

Thickness Distribution Curves Standard vs. Blended Slurry

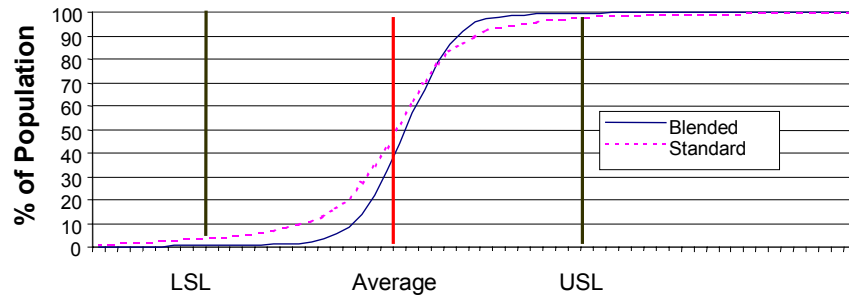


Figure 32. Blended vs Fresh SiC Performance

Caustic Waste Reduction

The work on reducing waste under the above referenced contract has proceeded well. As background for the work, caustic waste is a large cost driver in the manufacturing process SSI has deployed. Figure 33 shows the flowchart of how the caustic is used in fabricating solar cells at SSI. Figure 34 shows the reduction in waste by year under the contract period. As can be seen from the chart, the process waste the amount of waste generated has been reduced by well over 50%. The most significant thing that has been done is the extension of bath life in the caustic damage removal steps and the caustic texture etch steps in the wet etching processes. The net benefit since the beginning of the program is over 3000 gallons saved per megawatt produced, this equates to almost 90,000 gallons of waste reduced this year or a savings over \$100,000.

The final part of the caustic waste reduction work has been the implementation of a simple filtration recycling system to recover the caustic detergent for re-use. This was done in the last half of Phase III of the program.

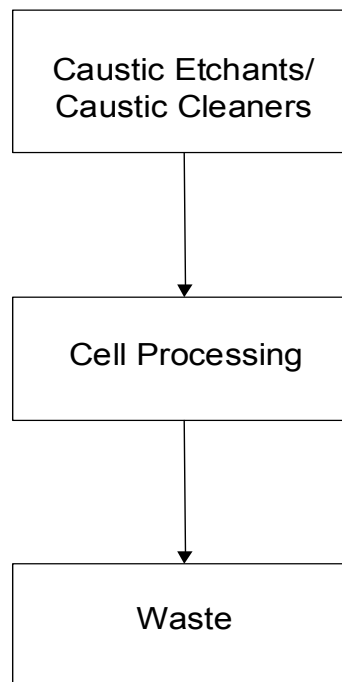


Figure 33. Caustic Use at SSI

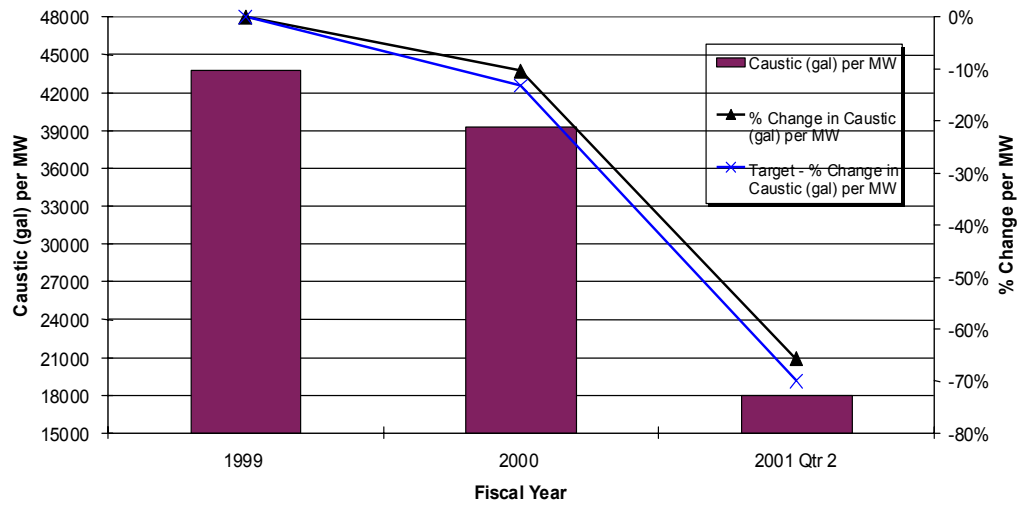


Figure 34. Caustic Waste Reduction under PVMat Program

Conclusions

The first step toward reducing cost in this PVMat 5A2 was to reduce wafer thickness. The original plan to start piloting wafers at 150 microns showed excessive yield losses. For this reason, the approach was modified to a two step reduction in thickness, from 385 microns to 250 micron cells, and then from 250 micron to 195 micron cells during Phases II and III. During Phase I the handling tools, the Back Surface Field (BSF) process, and the confirmation of the environmental integrity of thinner wafers was all accomplished. Phase II accomplished the pilot phase of 125 micron wafers, with very mixed yield results. The optimum thickness for productivity (best use of Silicon) was to slice wafers at approximately 220 microns making cells approximately 195 microns thick. Efficiency gains through the use of a Boron Back Surface Field Process has been highly successful as well as ingot and cell processing quality improvements. Thin, high efficiency cells were successfully piloted in Phase III.

The larger cells are made, the lower the potential dollar per watt. SSI developed and grew 200 mm ingot, wafers and cells. This larger ingot has proven to be a product which can be grown in the larger crystal growers which SSI has in it's Vancouver facility. Large area cells and modules have been designed and built in Phase II and Phase III. These larger cells continue to show the best cost structure as it optimizes the watts per kilogram consumed in producing the cells. It also optimizes the labor and machine utilization in the factory because more watts are produced for each invested hour.

Hazardous waste reduction has been attacked in two ways. The largest consumable item aside from polysilicon is Silicon Carbide (SiC) used in the wafer slicing process. This SiC use has been reduced significantly through recycling and re-use. The Silicon Carbide use has been reduced by over 50% during the life of this contract. The caustic waste has been reduced by over 70% by a combination of bath life and recycling efforts.

These three areas of focus, thinner cells, larger cells and modules and hazardous waste reduction have shown the potential of reducing cost by 30% per watt.

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1. Jester, T. L. (February 1999). "*Photovoltaic Cz Silicon Module Improvements, Final Subcontract Report*", 9 November 1996- 8 November 1998. Work performed by Siemens Solar Industries, Camarillo, CA. Golden, CO. National Renewable Energy Laboratory.
2. Jester, T.L. (December 1999). "*Specific PVMat R&D on Siemens Cz Silicon Product Manufacturing, Annual Subcontract Report*", June 1998-June 1999. Work performed by Siemens Solar Industries, Camarillo, CA. Golden, CO. National Renewable Energy Laboratory.
3. Jester, T.L. (September 2000). "*Specific PVMat R&D on Siemens Cz Silicon Product Manufacturing*", 28th IEEE Photovoltaic Specialists Conference, September 17-22, 2000, Anchorage, Alaska

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13. ABSTRACT (<i>Maximum 200 words</i>) This report describes work to improve the cost per watt of Cz modules and to improve PV module manufacturing technology. The focus of the three-year program was to implement a 17%-efficient, 195-micron-thick cell with a 30% reduction in manufacturing cost. In addition, the program developed a prototype, 200-mm-diameter cell with low-cost module packaging. A final result is also a 50% reduction in slurry use through recycling of silicon carbide, and a 70% reduction in caustic waste. Work focused on reducing the cost per watt of Cz silicon photovoltaic modules under Siemens Solar Industries' DOE/NREL PVMaT 5A2 subcontract is described in this report. Work on cell thickness reduction, the required electrical and mechanical changes to accommodate these thinner cells, larger cells, and waste reduction are all described in this final summary.				
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