

Silicon-Film™ Solar Cells by a Flexible Manufacturing System

**PVMaT Phase II Annual Report
February 1, 1999—January 31, 2000**

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AstroPower, Inc.
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NREL

National Renewable Energy Laboratory

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Table of Contents

Executive Summary	3
Introduction	3
Approach	4
Results	4
In-Line Wet Processing	4
Continuous In-line Wet Processing	4
Continuous Phosglass Etch System	5
Continuous Sodium Hydroxide Etch	7
Sodium Hydroxide Etch Bath Monitoring	8
Surface Cleanliness Analysis	10
Solar Cell Efficiency	12
Microdefect Characterization	12
Macroscopic Uniformity Analysis	15
Blue Response	16
Large Area Cell Testing	21
Metallization	22
Low Contact Resistance Ink	22
Large-Area Screen Printer	24
Large Area Modules	25
Customer Requirements	26
Size and Shape:	26
Frame and Mounting	26
Electrical	26
Laminate Design	27
Frame and Mounting Design	29
Module Cost Reduction	30
Junction Box	30
Summary	31
Acknowledgements	31

Figures

Figure 1.	Continuous HF etch system – load view.....	6
Figure 2.	AP-225 wafers between modules.....	7
Figure 3.	Bath monitoring experiment with reduced sodium hydroxide usage.....	9
Figure 4.	Etch bath monitoring experiment.....	9
Figure 5.	OSEE readings for wafers at various stages of surface preparation before diffusion.	11
Figure 6.	Mapping of dirty wafers with respect to orientation in the cassette.....	11
Figure 7.	EBIC image of a Silicon-Film™ mesa diode. Dark regions indicate low current collection.	12
Figure 8.	EBIC image of a mesa diode of Silicon-Film™ material.	14
Figure 9.	EBIC images of mesa diodes made from Silicon Film™ feedstocks A and B.	14
Figure 10.	Fill factor map of two AP-225 Silicon Film™ solar cells produced under different thermal profiles.	16
Figure 11.	Potential power gain from improved blue response versus IQE at 500 nm.	17
Figure 12.	Comparison of internal quantum efficiencies of an AP-225 cell before and after etch back.....	18
Figure 13.	Internal quantum efficiency of limited source diffusion and standard diffusion solar cells.....	19
Figure 14.	Net 5% increase in performance of lower quality wafers with the new diffusion process as compared to the old diffusion process.	20
Figure 15.	IQE data for new diffusion sequence on Silicon Film™ AP-225. The improved blue response has lead to a 6-10% increase in power.	20
Figure 16.	Spectral irradiance comparison for five light sources.....	21
Figure 17.	12x6 solar cell large area module.....	27
Figure 18.	Backside of large area module laminate	28
Figure 19.	Prototype large area Silicon Film™ module – front view	28
Figure 20.	(Partial) modules mounted on roof.....	29

Table

Table 1.	Fill factor data for front contact sample inks at various firing conditions.....	24
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Executive Summary

AstroPower is developing a manufacturing process for Silicon-Film™ solar cell production under an NREL-administered PVMaT cost-share program. This document reports on results from the second phase of a three phase effort. Progress is reported on the development of new procedures and equipment for in-line wet chemical processes, sheet fabrication, solar cell processing, and module assembly. Future concepts and goals for the Silicon-Film™ process are also discussed.

A major technical goal of this effort is the elimination of batch production processes in AstroPower's solar cell process. New processes are being developed that can accommodate large area Silicon-Film™ planks in an in-line, continuous manner. During Phase II of this program, an in-line chemical etching system for removing diffusion oxides was specified, procured, and installed. Operation of this system during Phase III of this program is expected to validate the in-line approach and will provide valuable information for use in the design of a second, and more challenging, in-line etch system.

Significant progress was made during this reporting period in the development of new screenprinting ink formulations for both the front and back metallization of Silicon-Film™ solar cells. Cost reductions and efficiency improvements were achieved as a result of these efforts.

Progress was made in the design of a new Silicon-Film™ plank machine as well as in improved processes to fabricate this material into cost-effective and efficient solar cells. Additionally, a new large-area module concept was developed and prototyped during this phase of the PVMaT program.

Introduction

The approach and accomplishments in this report focus on the concept of “flexible” solar cell manufacturing. This involves continuation of engineering efforts to generate large areas of high-quality Silicon-Film™ sheet material at high speeds and to implement new cassette-less, in-line processing equipment for solar cell manufacture. The Silicon-Film™ process is presently in production at AstroPower fabricating 240 cm² solar cells (AP-225). Efficiencies exceeding 12% have been measured for the AP-225 solar cell. Small, laboratory-scale devices have demonstrated efficiencies as high as 16.6%.

The areal dimensions of Silicon-Film™ wafers and solar cells increased from 10 x 10 cm to 15 x 15 cm during the AstroPower PVMaT-4 program. Solar cell fabrication processes are now being designed and developed within the AstroPower PVMaT-5 program to process large-area (30 x 30 cm) Silicon-Film™ solar cells.

During Phase II of this PVMaT program, significant progress has been made in developing large-area, process machines for AR coating, belt gettering, belt diffusion, hot caustic surface etching, and diffusion oxide etching.

Approach

There are three basic development areas that are involved in transferring Silicon-Film™ technology from the laboratory to the factory:

- Optimization of the sheet generation process -- high-speed, high quality and large areas are desired.
- Optimization of the solar cell fabrication sequence to achieve high-efficiencies with large areas. These processes must be compatible with manufacturing and preferably should be in-line and continuous rather than batch-mode.
- Integration of these developments in an industrial setting by generating (and selling) significant quantities of solar cells.

Results

In-Line Wet Processing

The goal of this task is to develop a set of production tools that are capable of processing large sheets of Silicon-Film™ material through a wet chemical process sequence using a cassette-less in-line approach. With this in-line technology we hope to increase throughput, reduce material cost, reduce operator exposure to process chemicals, and allow size independent processing of Silicon-Film™ wafers.

Continuous In-line Wet Processing

The solar cell production process at AstroPower currently includes several cassette-based chemical process steps. Two of these steps are surface preparation prior to diffusion and phosglass removal following diffusion. These labor intensive chemical processes require the wafers to be loaded into cassettes, moved between chemical tanks by hand, dried in cassettes, and then unloaded. The maximum wafer size is limited by cassette size, and the total throughput is limited by the tank size. A batch process such as this is difficult to control since the composition of the etchant and reaction by-products is constantly changing. Process chemicals must be continually added to the tanks between batches to replenish the baths. Operators are exposed to hazardous chemicals, including concentrated sodium hydroxide near its boiling point, dilute hydrochloric acid, and dilute hydrofluoric acid. Also, the use of cassettes in processing reduces the liquid flow to the wafers and at times results in uneven etching or cleaning at the edges.

The implementation of an in-line wet chemical processing system would eliminate many of the limitations discussed above. Such a system would be capable of handling wafers of various sizes, and even uncut Silicon Film™ planks. Operator exposure to chemicals could be minimized by a completely enclosed system where dry wafers are loaded for processing, and completely rinsed and dried wafers are unloaded from the system. The composition of the solutions could be maintained within operating limits by in-line monitoring and control. Such control would reduce raw material usage and waste stream volume. Throughput of the in-line system would no longer be limited by tank size and the time consuming cassette loading and

unloading operations. Total processing time could be further reduced by the more efficient cassette-less rinsing and drying steps.

There are also significant potential savings in labor and materials with an in-line wet chemical process. In comparison with our current batch process, continuous in-line processing will increase the throughput by more than a factor of two without requiring custom equipment. This is due to the method of wafer transport through the wet process systems. For the NaOH surface etching process, where material costs are dominant, in-line continuous processing yields a potential cost reduction of 54%. This is due to more efficient use of the etching solution. For the HF diffusion oxide etch process, in-line continuous processing yields a potential cost reduction of 58% due to savings in labor. This is due to the need to load wafers into and out of cassettes in order to process them.

Continuous Phosglass Etch System

The first process chosen for batch to continuous conversion was the diffusion oxide strip process. During the diffusion process a thin layer of phosphorus-doped silicon dioxide grows on the surface of the wafer. This oxide must be removed prior to the contact metallization steps. The diffusion oxide is removed by briefly etching the wafers in a dilute hydrofluoric (HF) acid solution. This is followed by several deionized (DI) water rinses and a drying step. At present the diffusion oxide etch is performed in wet process tanks in a chemical fume hood. The diffused wafers must be individually loaded into plastic cassettes for this type of batch processing. Once the diffusion oxide is etched, the wafers can be unloaded from the cassettes so that they can proceed to the next process step.

The main objectives for improving the diffusion oxide etching process are:

- process large-area Silicon Film™ planks
- eliminate cassette loading and handling
- increase the areal throughput rate by more than a factor of five
- eliminate operator exposure to the process chemistries
- reduce material and labor cost

Based on the above criteria and discussions with several manufacturers of in-line wet processing equipment a continuous HF strip system was specified. The system requirements were as follows:

- ability to handle Silicon Film™ wafers and planks without fixturing
- initial spray water rinse to remove particulates from the wafer
- immersion etch process (not a spray process, to minimize aerosols)
- utilize a cleaning process compatible with the textured surface of Silicon Film™ wafers
- cascading DI water rinse for water conservation
- wafer or plank must be dried completely before exiting the system
- etch solution must be fully contained
- pump system should include particulate filtering to extend etch solution life
- no operator exposure to HF, whether liquid or vapor

During Phase II this diffusion oxide HF etch system, shown in Figure 1, was completely specified and ordered. The wafer transport of this prototype system is 27" wide, which will accommodate three Silicon Film™ wafers across. The system is comprised of the following modules: load; rinse; HF etch; triple cascade rinse; brush clean; dry; and unload. Several additional items were added to the system, including an HF scrubber for the system exhaust and a neutralization system for disposal of spent HF etch solution. During the final design stage of the project several additional safety issues with regard to handling HF arose. These concerns were successfully handled by design modifications prior to assembly of the system.



Figure 1. Continuous HF etch system – load view.

The in-line diffusion oxide etch system was completed toward the end of Phase II. Several AstroPower engineers visited the manufacturer to evaluate the system prior to shipment to AstroPower. No HF was added to the immersion module during the evaluation process. Samples of all current AstroPower products were tested. The wafer transport system was capable of handling all of the wafer sizes with minimal wandering of parts (Figure 2). During the acceptance tests all of the safety features of the equipment were also reviewed.



Figure 2. AP-225 wafers between modules.

The system was then completed and shipped to AstroPower. Installation of the system will include design and construction of a waste treatment station for the waste rinse water, installation of the HF scrubber, and construction of walls to isolate the system and is presently underway. Enough space and resources have been allocated to accommodate two diffusion oxide etch units. Once installation is complete, testing with HF will begin. The process will be in production in the first quarter of 2000.

[Continuous Sodium Hydroxide Etch](#)

The next step in developing continuous wet chemical processing and eliminating cassettes from our solar cell process line is the conversion of our surface preparation step from batch to in-line. The surface etch process is based on a heated sodium hydroxide solution. The critical parameters are solution temperature, which strongly influences the silicon etch rate, and solution composition, which affects surface quality. It is also critical that the etching action be quickly terminated by flooding the surface with hot water to prevent surface “burning” by exposure to air. Allowing the wafers to be exposed to air while covered with a thin layer of sodium hydroxide solution produces uneven etching and staining. This hot water flood rinse is followed by a neutralization step, to remove residual NaOH, and then several cascading water rinses. At present this process is performed by operators who manually transfer cassettes filled with wafers from tank to tank.

The continuous in-line surface etch system will be based on our current tank-based process sequence. However, in the continuous etch system individual wafers will travel through the process sequence without need for loading and unloading from cassettes. The advantage of this, in addition to eliminating the individual load and transfer steps, is that larger wafers, different sized wafers, and even Silicon-Film™ planks can be processed by the same equipment with virtually no need for fixturing.

The equipment used for continuous in-line wet processing is based on individual process modules that perform a particular step in the process sequence and are combined into a complete system. For the continuous surface etch process, the individual modules consist of: (1) pre-etch rinse; (2) sodium hydroxide etch; (3) etch stop rinse; (4) acid neutralization; (5) cascading water rinse; and (6) dry. As an option, an HF etch and water rinse may be added after the cascading water rinse and before the drying step.

Many of the modules comprising the previously mentioned diffusion oxide etch system can also be used as components for designing an in-line surface etch system. Evaluation of materials for construction and a preliminary design have been completed. Equipment suppliers have been identified and qualified as a result of the work done in Phase II. In addition, mechanical design guidelines have been developed. A mechanical specification will now be developed which will lead to equipment purchase.

[Sodium Hydroxide Etch Bath Monitoring](#)

In order to gain a better understanding of the sodium hydroxide etch process and solution chemistry we developed several analytical techniques for monitoring the sodium hydroxide etch baths. Using these techniques, we performed etch bath monitoring experiments. The refresh rate of sodium hydroxide in our production scale batch process was cut in half as a result of the initial bath monitoring experiments. Following these changes two additional etch monitoring experiments were performed.

Figure 3 shows the results of the first of these experiments. Both sodium hydroxide and silica concentration appear to increase sharply during the etching of the first thousand wafers and then drops to an equilibrium value. The leveling of the silica curve is unusual because, according to mass balance calculations, over 1000 g of SiO_2 are added to the tank per 100 wafers etched. Either a steady state is reached where excess silica is washed out into the waste treatment system, sodium silicates are precipitating out of solution, or silicates are forming a complex which can not be measured by the silicomolybdate test.

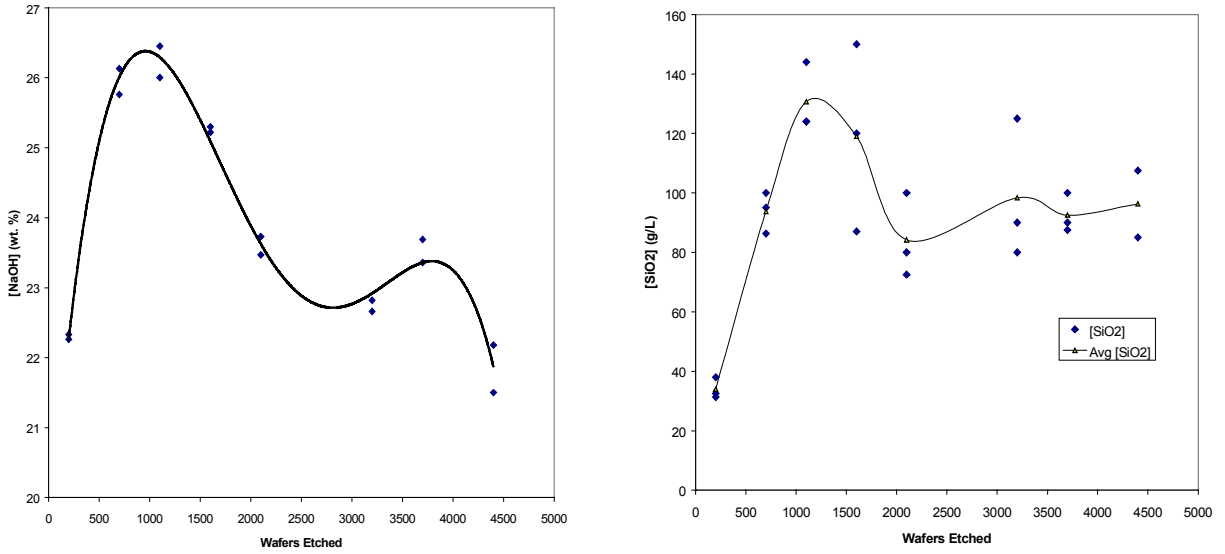


Figure 3. Bath monitoring experiment with reduced sodium hydroxide usage.

In another etch bath monitoring experiment, samples of the sodium hydroxide etch solution were taken during one shift of operation. The results are shown in Figure 4. Sodium hydroxide concentration in this experiment has stabilized. The silica concentration once again increased sharply and then stabilized around 130g/L.

These chemical bath monitoring techniques will be used to specify the process conditions needed in the in-line equipment under development.

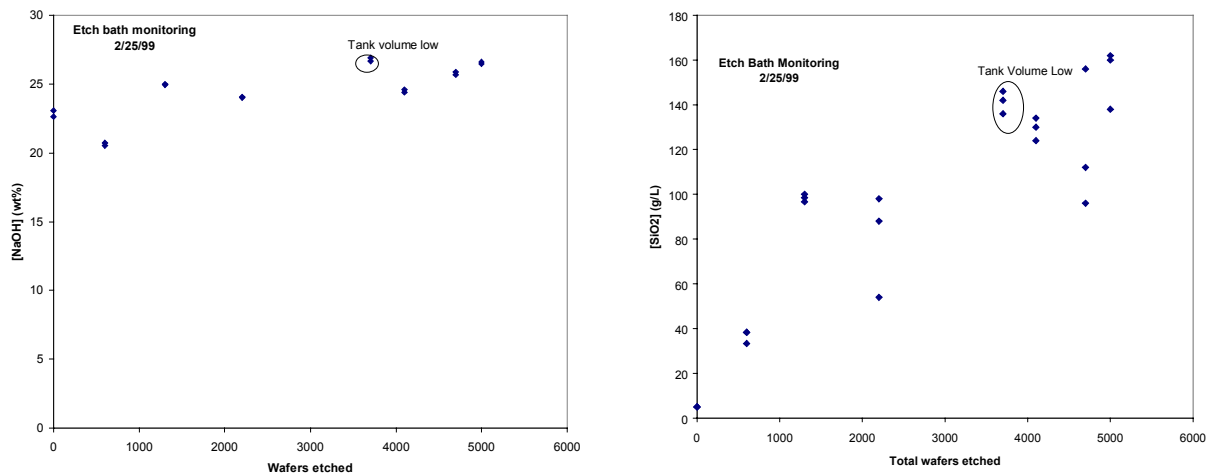


Figure 4. Etch bath monitoring experiment

Surface Cleanliness Analysis

Wafer surface quality may play a role in several processing steps such as diffusion, metallization and AR coating. Surface contamination may occur in the form of residue from the chemical process steps and wafer handling in the production. An SEM has been used to view the contaminants, and EDS has been used for elemental analysis of the residue. This form of analysis is capable of providing valuable information on the surface quality of the wafer; however, the process is time consuming, destructive, and limited to small sections of the wafer. A more production-oriented system for quantifying surface cleanliness is needed.

After some investigation, Optically Stimulated Electron Emission (OSEE) was identified for surface characterization. The surface is illuminated with an ultraviolet light source and electrons are photoemitted from the surface and collected by a sensor. In order for this technique to be used the surface must be photoemitting (the material work function must be less than 7 eV). Contamination on the surface, in most cases, reduces the number of electrons emitted from the surface, and therefore reduces the OSEE reading.

This measurement technique is non-destructive, and no sample preparation is required. The only requirement is that a constant sensor-to-surface distance must be maintained between samples for measurement consistency. This type of system can quantify the level of contamination but can not identify the type of contaminant. For manual systems the area of analysis is limited to the area of the sensor. Equipment is available that has scanning capability to map an entire wafer surface.

Several experiments focused on characterizing wafers directly after the surface preparation step. The surface preparation sequence is as follows: sodium hydroxide etch, three hot cascading DI water rinses, HCl bath to neutralize the excess NaOH, rinse, HF bath, rinse, and dry. Cassettes of wafers were pulled just before HCl, just before HF, and right after drying. Wafers that did not go through the HCl bath should contain residual sodium hydroxide and sodium silicates. The results of these measurements are shown in Figure 5. Higher OSEE readings indicate a cleaner silicon surface. The average reading for standard process wafers was 536. The dirty wafers, no HCl, averaged at 507. Wafers that did not receive the final HF strip step appeared cleaner than wafers that had gone through the entire surface preparation sequence. Nine measurements were taken per wafer. A “mapping” of the wafer surface for the dirty set of wafers is shown below (Figure 6). The center of the wafer appears to be dirtier than the edges. This may be an indication of poor water circulation in the hot rinses following the sodium hydroxide etch.

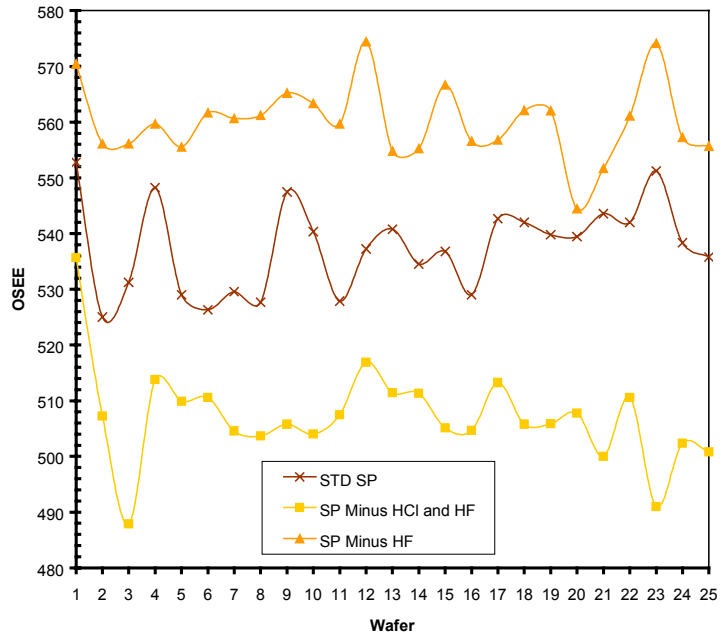


Figure 5. OSEE readings for wafers at various stages of surface preparation before diffusion.

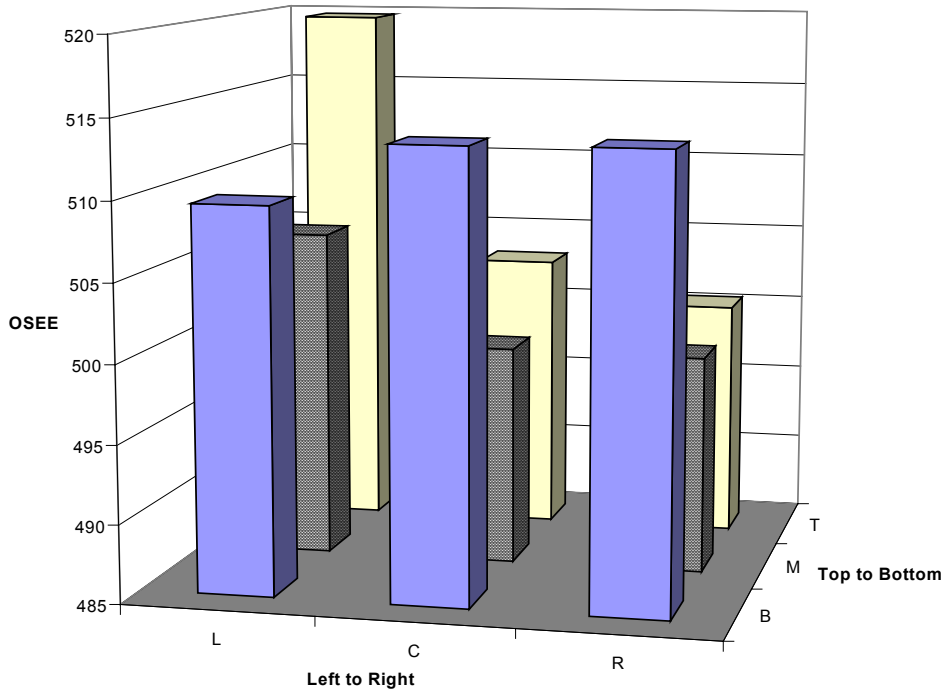


Figure 6. Mapping of dirty wafers with respect to orientation in the cassette.

The OSEE surface characterization technique will be used to develop and optimize the new in-line chemical processes. This technique has the potential to be used as a process monitoring tool, giving early indications of final solar cell performance and yield.

Solar Cell Efficiency

Microdefect Characterization

Scanning electron microscopy (SEM) and electron beam induced current (EBIC) studies were performed on Silicon-Film™ material. The overall goal of this work is to detect microdefects and understand how they degrade solar cell performance. Ultimately this knowledge will influence specifications for both feedstock purity and the thermal profile used for producing Silicon-Film™ wafers. Preliminary results are presented in this section.

Figure 7 displays an EBIC image of a 4.5mm square diode made from Silicon-Film™ material. Darker areas indicate lower electrical performance due to high electron-hole recombination. Grain boundaries are clearly evident and appear darker than intra-grain regions. In addition, metallic impurities prefer to reside along the grain boundaries and further increase recombination rates. The fine texture-like detail within grain boundaries is believed to be an artifact due to scattering of the electron beam off the rough sample surface.

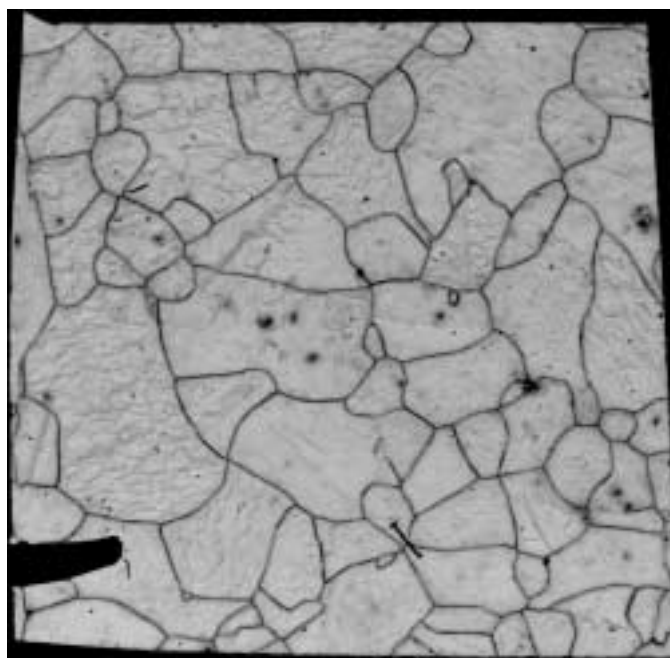


Figure 7. EBIC image of a Silicon-Film™ mesa diode. Dark regions indicate low current collection. Diode size 4.5x4.5mm. Dark shadow in the lower left is due to the probe.

Also present in the image are dark, hazy areas within the grains. These regions are defect clusters and have high local recombination. Both structural defects (e.g. dislocations) and metallic precipitates can cause these defect clusters to occur. The short circuit current density is adversely affected by these defects.

EBIC has been used to compare Silicon-Film™ solar cells produced under different growth conditions and with different feedstock material. Each sample is analyzed by grain size distribution, defect cluster size and density, and grain boundary recombination. Currently the analysis is limited to being qualitative. However, it is possible to obtain quantitative measurements using image processing software. This will be considered for future work. Another limitation is that EBIC can not be used as an in-line process monitoring tool for the sheet growth process. Only after Silicon-Film™ planks have been grown and cells been diffused can EBIC be used.

EBIC has been successful in correlating grain morphology to electrical performance for Silicon-Film™ material produced with different thermal profiles during the Silicon-Film™ sheet growth process. The material shown in Figure 7 contains many odd-shaped grains and curved grain boundaries. These features are likely to have a relatively high Gibbs free energy. The grain size distribution is large, ranging from approximately 150-1,000 microns. Virtually all grain boundaries appear dark, which indicates high recombination. Furthermore, several point defect clusters are seen as small dark spots within the grains.

A mesa diode produced by a different thermal profile was also analyzed, and the EBIC image is shown in Figure 8. A difference in grain structure is clearly evident. The median grain size increased and the distribution narrowed. The number of curved grain boundaries decreased dramatically and many were replaced by straight segments. Straight grain boundaries have lower Gibbs free energy. Mesa devices produced using this material have efficiencies 19.5% higher than devices made with the material shown in Figure 7.

In addition to these morphology changes, recombination along grain boundaries and from point defects decreased. A large number of grain boundary segments appear bright in the EBIC image, indicating low recombination activity. Furthermore, the number of point defect clusters is significantly reduced. Changes in the thermal profile may not only influence grain morphology and defects but also affect the location of impurities.

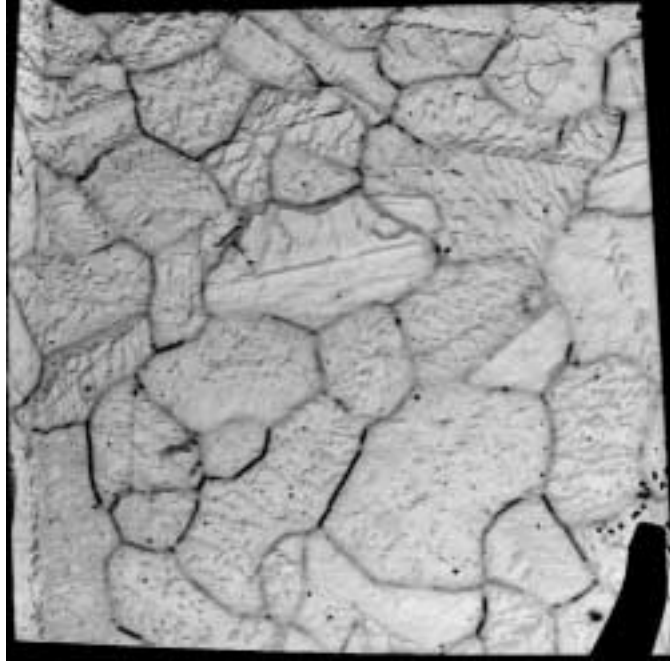
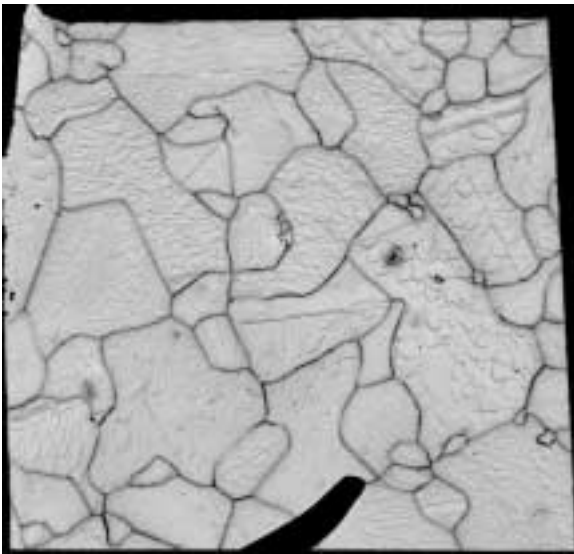
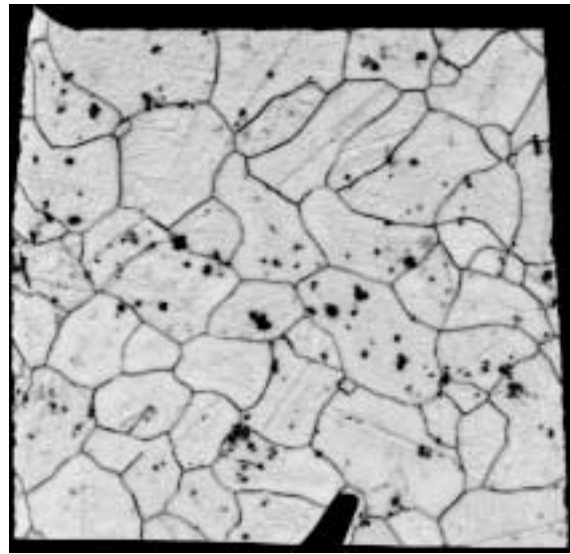


Figure 8. EBIC image of a mesa diode of Silicon-Film™ material. Diode size 4.5x4.5mm.

EBIC images of two mesa diodes made from feedstocks A and B are shown in Figure 9. Feedstock A is standard production material, and feedstock B is an experimental material with unknown purity levels. Diode A contained virtually no point defect clusters. In addition, more than half of the grain boundary segments were light, indicating low recombination.



Diode A – Feedstock A



Diode B – Feedstock B

Figure 9. EBIC images of mesa diodes made from Silicon Film™ feedstocks A and B. Diode sizes are 4.5x4.5mm.

In contrast, the most striking features of EBIC images of samples made from feedstock B were the numerous point defect clusters. The short-circuit current density is adversely affected by these defects. The measured J_{sc} of diode B was 16% lower than diode A. Since both samples were produced under the same thermal profile, it is unlikely that the point defect clusters are due solely to structural defects. This would suggest that feedstock B contains impurities at levels high enough to degrade solar cell performance.

Macroscopic Uniformity Analysis

In addition to microscopic techniques, such as EBIC discussed above, Silicon Film™ wafers are also characterized for larger scale non-uniformities. These non-uniformities generally result in lower fill factors in the finished solar cells. The results of a large area fill factor uniformity analysis is shown in Figure 10 for two wafers that were produced using two different thermal profiles during sheet growth. I-V data and fill factor maps were used to compare electrical performance of the two solar cells. The results indicate that the differences in thermal profiles during the growth of Silicon Film™ planks can affect the electrical performance of finished solar cells.

Electrical performance data was collected for two solar cells (A and B) processed with two different thermal profiles during plank growth. Improvements in all measured quantities were obtained with the modified profile (solar cell B). In an attempt to understand the low fill factors, both cells were diced into equally sized pieces to measure I-V data for the individual sections.

Figure 10 shows fill factor maps for the two solar cells. Solar cell A had regions of very low fill factors (<30%) scattered across the wafer surface which reduced overall cell efficiency. It is possible that structural or impurity-related defects are responsible for this phenomenon. In contrast, solar cell B did not have any of these “dead spots”-- localized areas with low fill factor. In addition, solar cell B has a much narrower range of fill factor values than solar cell A.

It is apparent that the modified thermal profile not only homogenized material quality across the wafer, but also eliminated dead spots. This resulted in a substantial performance difference (33% in P_{max}).

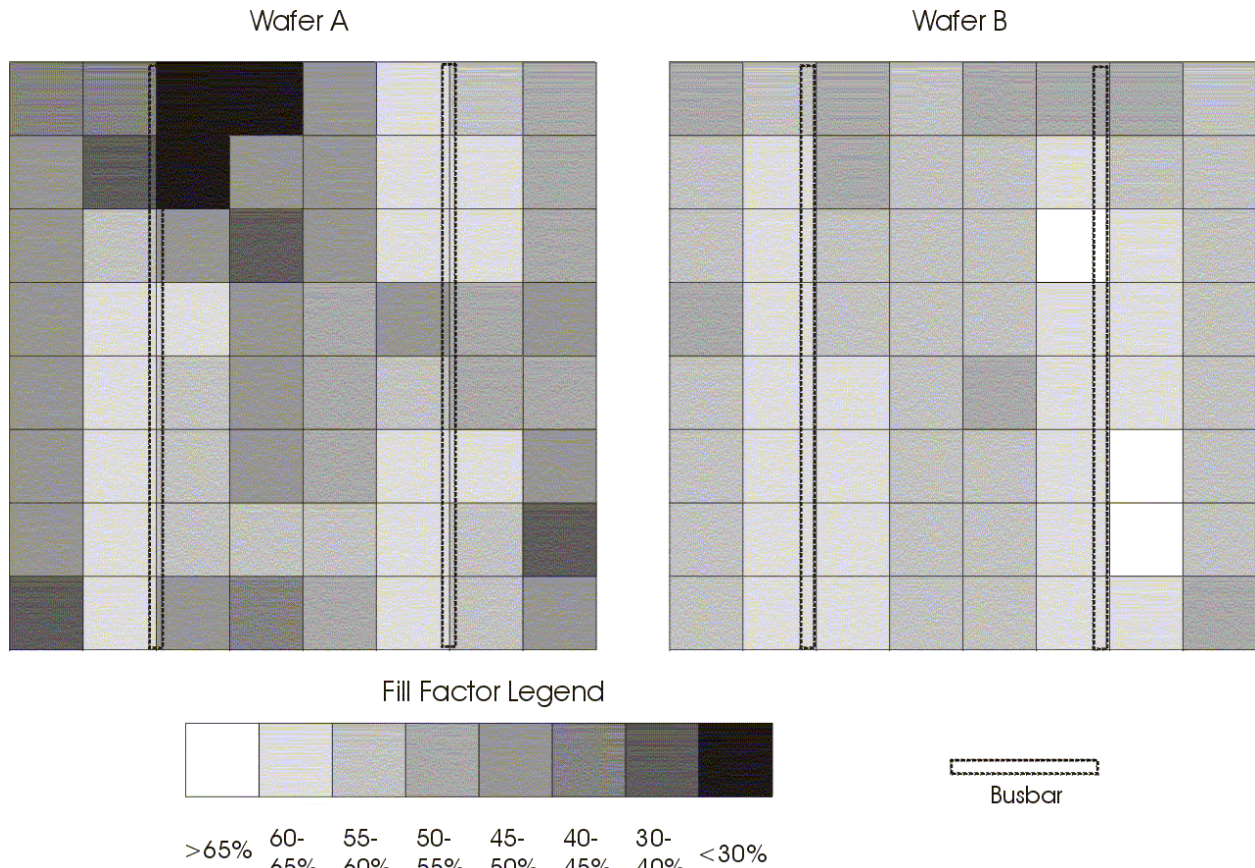


Figure 10. Fill factor map of two AP-225 Silicon Film™ solar cells produced under different thermal profiles. Due to the solar cell dicing process fill factors of segments shown above are lower than the fill factor of the whole solar cell.

[Blue Response](#)

Silicon-Film™ solar cells have typically had lower blue response than the polycrystalline silicon industry standard. Historically, the solar cell processing sequence has stressed the issues of cost and throughput. This approach has been successful in that the processes used for Silicon-Film™ solar cell diffusion are all high throughput and low cost. The low blue response however, represents an area of potential performance improvement and corresponding reduction in cost per watt.

Figure 11 shows the performance gain that can be realized by increasing emitter blue response. Blue response is shown on the x-axis as the Internal Quantum Efficiency (IQE) achieved at $\lambda=500$ nm. The previous diffusion process generated an IQE of 82% at 500 nm. The short-term goal for AstroPower is to achieve an IQE of 94% at 500 nm.

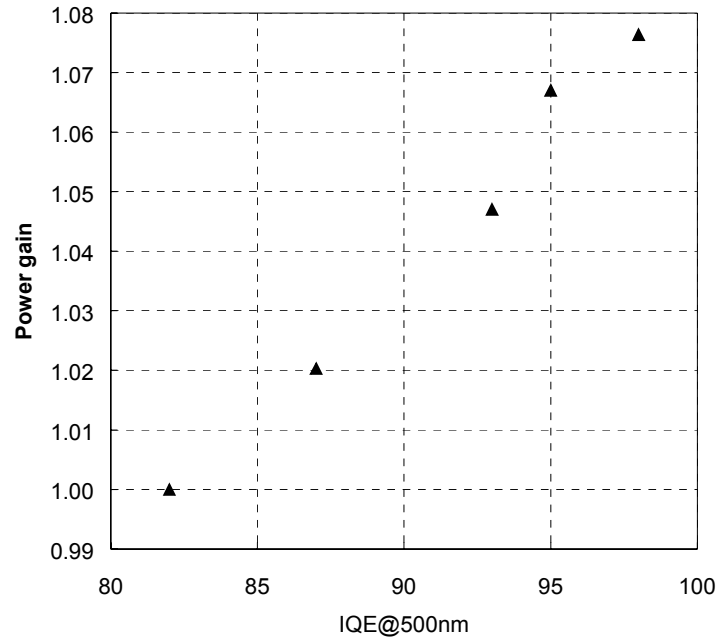


Figure 11. Potential power gain from improved blue response versus IQE at 500 nm.

In an effort to increase blue response we performed preliminary experiments using a laboratory-scale, emitter etch-back process to fabricate a high sheet resistance selective emitter. The selective emitter was achieved by performing the etch-back with front contact grids in place. This technique causes slow degradation of the contact adherence making it unsuitable for large-scale production. The exercise was designed to show the potential for improvement in solar cell performance using this technique. It appears that a “dead layer” causes internal quantum efficiency for wavelengths shorter than 900 nm to be lower than expected. This reduction in internal quantum efficiency can be accounted for by high emitter recombination. Figure 12 shows the IQE for an AP-225 solar cell that was measured before and after etch back. The blue response ($\lambda < 600\text{nm}$) is lower than expected, which is probably due to a poor front surface passivation due to the etch back.

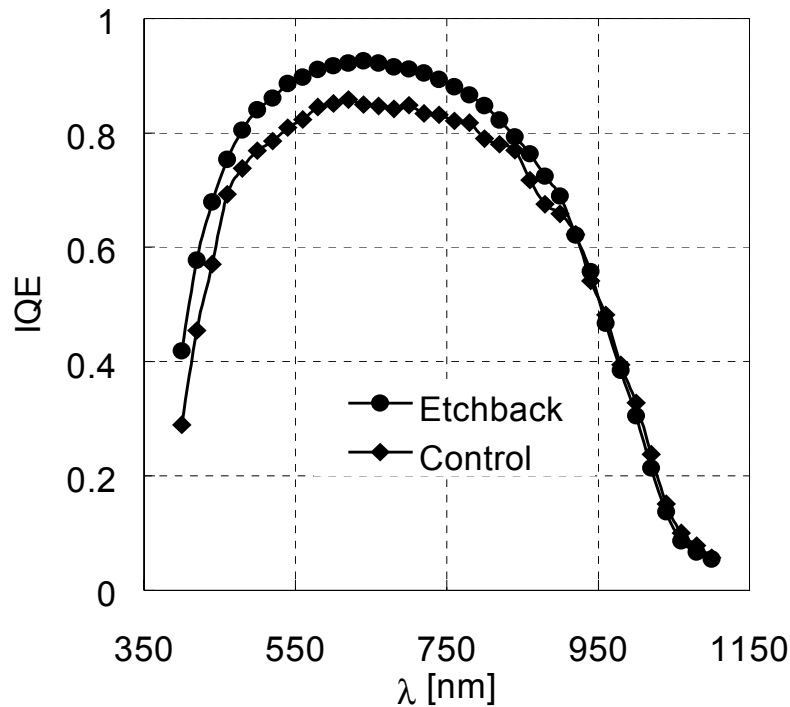


Figure 12. Comparison of internal quantum efficiencies of an AP-225 cell before and after etch back.

Although the laboratory etch back process could not be implemented in manufacturing the increase in blue response highlighted the potential improvement. PC-1D modeling was used to show that a selective emitter is not required to achieve the I_{sc} gains observed due to emitter etch-back. Upon further investigation of the emitter, large quantities of inactive phosphorus were suspected of forming a “dead layer” reducing the blue response significantly.

To determine the amount of current lost due to the dead layer, an experiment was performed by running a matrix of limited source diffusions in a tube furnace and comparing the blue response of those solar cells to our standard belt diffused cells. Figure 13 shows the IQE for both types of emitter. To establish that minimal amounts of electrically inactive phosphorus was present on the limited source diffusion wafers, several wafers were annealed and the sheet resistance was measured before and after the anneal. For the standard diffusion wafers the sheet resistance decreased by more than 50%. Wafers that were considered to be free of inactive phosphorus exhibited sheet resistance declines of about 5% which may be attributed to increased mobility due to a further drive-in of the already active dopant.

The results show that the blue response after limited source diffusion is better than the blue response (Figure 13) observed after emitter etch back (Figure 12). The IQE improvement at long wavelengths, however, was better with the etch back process.

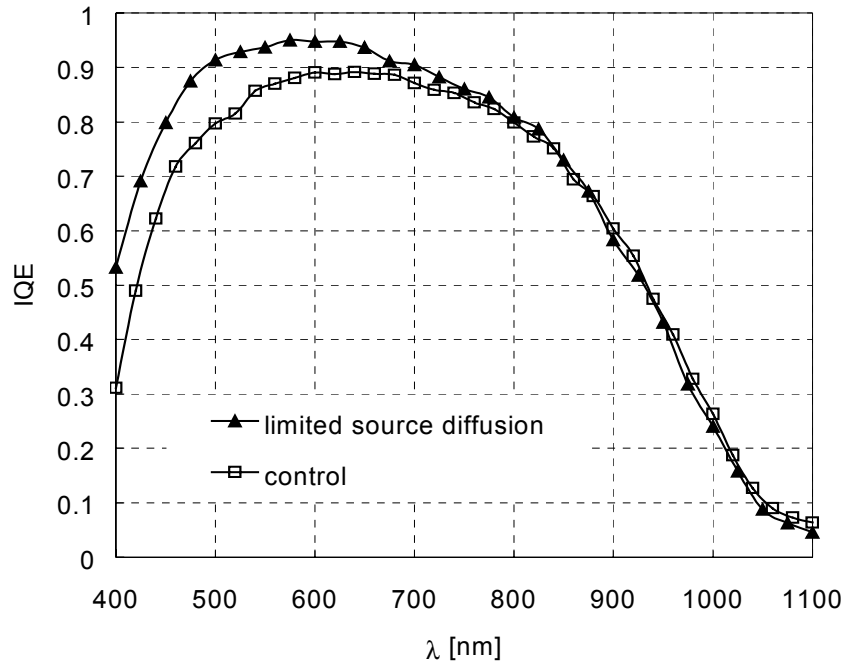


Figure 13. Internal quantum efficiency of limited source diffusion and standard diffusion solar cells.

Based on the results from the limited source diffusion experiments, a new diffusion process was implemented in production. The emitter sheet resistance of the new diffusion was 40% higher than the previous standard. In a large scale experiment two thousand Silicon FilmTM AP-225 solar cells were fabricated and tested with the new diffusion sequence. Power increased by 6-10% compared to the control cells. I_{sc} , V_{oc} and fill factor also increased. Figure 14 compares the current of wafers processed using the new and old diffusion processes. The fill factor increase was surprising, considering the higher emitter sheet resistance. The slight increase in fill factor was caused by reduced J_{02} that compensated for the increased series resistance. The new diffusion process caused the J_{02} to decrease by almost one order of magnitude. The new emitter also allowed us to reduce the front contact firing peak temperature by 80°C. This lower temperature results in less shunting and higher efficiency. The cause for the reduced firing temperature is probably due to the relatively abrupt junction profile ($x_j = 0.25$ - $0.3 \mu\text{m}$) and a high surface dopant concentration of this diffusion process.

This new diffusion process requires lower diffusion temperatures, which results in a lower thermal budget. This leads to increased efficiency. The lower temperature is also leading to higher diffusion lengths. Figure 15 shows the IQE of one of the 2000 cells processed.

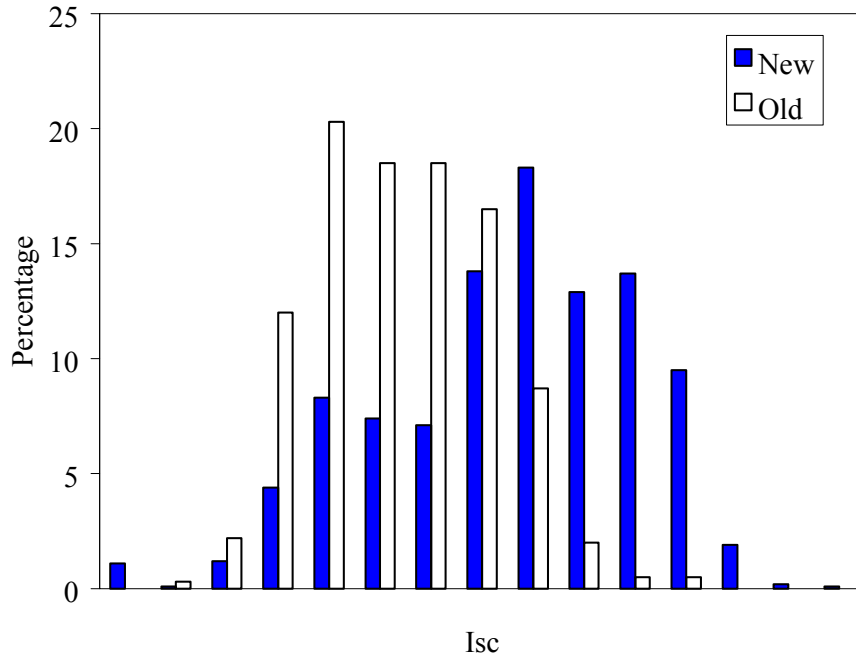


Figure 14. Net 5% increase in performance of lower quality wafers with the new diffusion process as compared to the old diffusion process.

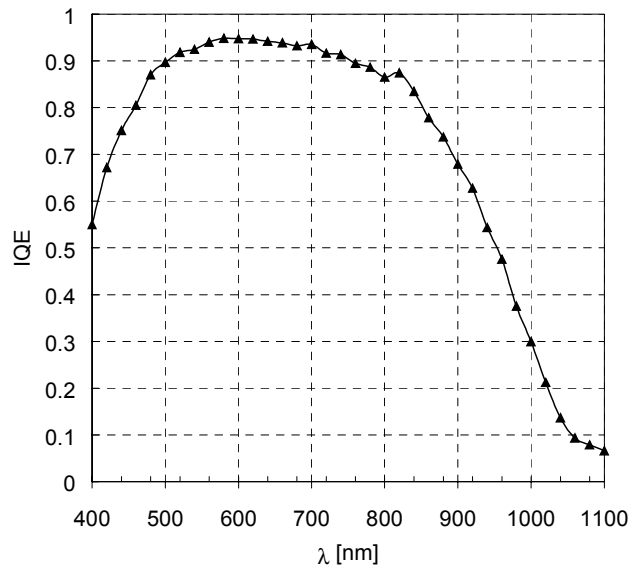


Figure 15. IQE data for new diffusion sequence on Silicon Film™ AP-225. The improved blue response has lead to a 6-10% increase in power.

Large Area Cell Testing

A new solar cell tester was constructed that can test Silicon-Film™ solar cells that are up to 200 x 200 mm. The new cell tester uses a bank of tungsten-halogen lamps for illumination rather than more conventional Xenon arc lamp or flash lamps. A study was conducted to determine potential errors due to differences in lamp spectral content during the solar cell test process.

Figure 16 compares the spectral irradiances for five different light sources of interest: AM1.5G, a filtered Xenon arc lamp, a tungsten-halogen lamp with a gold-plated reflector, and a standard tungsten-halogen lamp running at 80 and 110 Vrms [1,2]. These data were normalized by numerically integrating power from 300 to 1000 nm. The graph shows that the tungsten-halogen bulbs have significantly less blue light than Xenon arc and AM1.5G. In addition, without a gold-coated reflector, the tungsten-halogen bulbs running at either 110V or 80V have limited spectral content for wavelengths longer than 700 nm.

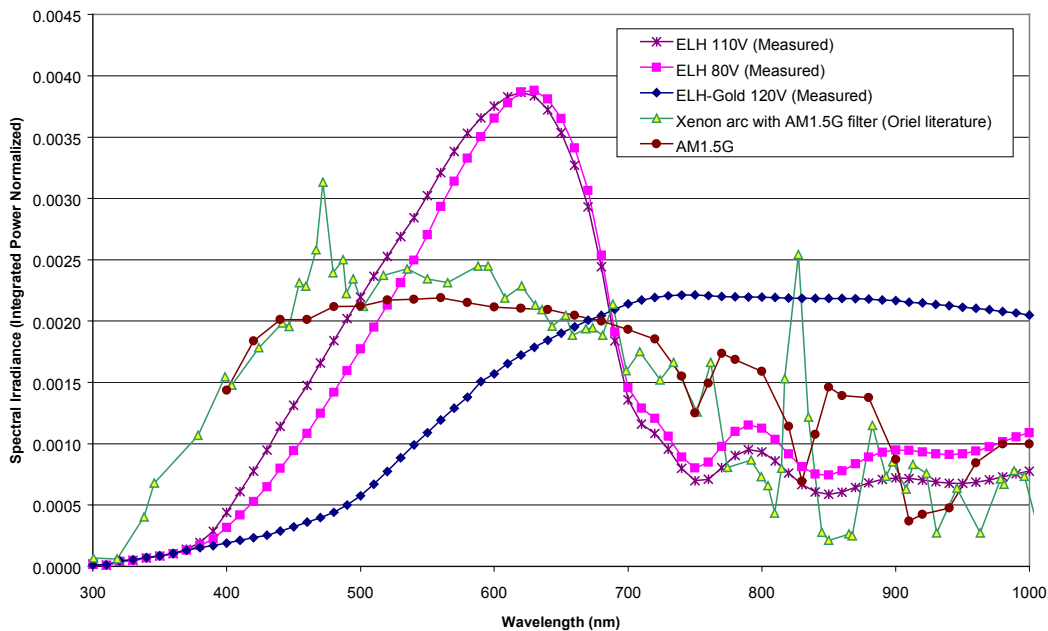


Figure 16. Spectral irradiance comparison for five light sources.

A detailed, model-based comparison of the four artificial light sources was undertaken. The model was tested with Silicon-Film™ solar cells that span the range of spectral responses seen in production. The spectral response of the tester calibration cell was also accounted for. The model indicates the 80V tungsten-halogen bulb resulted in less error than the 110V bulb. The maximum error for the 80V tungsten-halogen ELH bulb was $-2.6\%/+2.7\%$ and increased to $-3.0\%/+3.1\%$ for 110V bulb. The Xenon arc lamp was predicted to have the smallest errors of all four light sources, with a worst-case error of $-2.2\%/+2.3\%$. Although slightly inferior to the arc lamp in emulating an AM1.5G spectrum, the predicted error range for the ELH bulbs is still small. Based on these results tungsten-halogen bulbs will be used in production solar cell testers.

Metallization

Solar cell contact metallization systems were evaluated with the goal of developing a continuous, high-throughput process for large-area Silicon Film™ solar cells. The objectives of this task are to reduce cost, increase throughput, and reduce metallization contact resistance. The evaluation process includes the investigation of new ink formulations and new screen printing equipment.

During this contract phase, we achieved the following results:

- Evaluated front contact inks with varying glass frit compositions.
- Evaluated silver ink samples from three thick film ink manufacturers and as a result identified a replacement for the ink currently used in manufacturing.
- Improved line definition of front contact inks.
- Investigated reducing the thickness of aluminum back ink.
- Surveyed manufacturers and suppliers of screen printing equipment.

Low Contact Resistance Ink

Very little commercial innovation has occurred in the materials used to produce the thick film metallizations for silicon solar cells. Typically a supplier will provide thick film materials based on a guess of the requirements of a cell manufacturer. Our manufacturing philosophy has been to use available materials rather than custom-formulated inks, and to qualify second source suppliers whenever possible. While this approach is viable, as evidenced by the sheer volume of solar cells produced with thick film metallizations, we have found that Silicon Film™ wafers act differently than conventional single crystal silicon wafers when standard formulation front contact inks are used. As with all silicon wafers, if the contact firing energy (temperature x time) is too high, the junction will be shunted. If the wafers are fired "cold" excess series resistance occurs and fill-factor and power are lost. While there is a vast quantity of empirical data, the chemistry and physics of the silicon solar cell thick film metallization is not well understood.

Our goal for this work is to develop a better understanding of how the front contact inks interact with the Silicon Film™ wafer and its emitter diffusion, and to develop a new front contact ink that is optimized for this material. In particular, we would like to minimize front contact resistance and bulk metallization resistance while increasing the tolerance to firing conditions.

Front contact inks typically consist of silver particles blended together with a glass frit in an organic vehicle. The glass is believed to remove the oxide on the wafer surface ("flux") and to "stick" the silver particles to the wafer surface. Some manufacturers also add an N-type "dopant" that is supposed to "diffuse" ahead of the glass, minimizing junction shunting by the metallization. As a result of our discussions with an ink manufacturer, we defined a technical path to focus on the glass and dopant composition of the inks. In particular, we were interested in trying inks with new glass frits and phosphorus carrying compounds that were developed for use in other applications. The ink manufacturer provided candidate silver front contact inks that

AstroPower tested by fabricating cells with different time-temperature sintering schedules. These tests are discussed below.

A commercial ink manufacturer supplied samples of inks with low, medium, and high glass frit contents. The low frit sample was evaluated over a 100°C (750-880°C) temperature range did not appear to make good “as-fired” electrical contact to solar cells. Measured fill factors ranged from 30 to 38%. V_{oc} and I_{sc} were typical for the type of wafer used. The poor fill factors were found to be due to high contact resistance. The medium frit sample was tested in the same temperature range and had more promising results. The as-fired fill factors were in the high 60 and low 70% range. However, there were difficulties in duplicating these results. The process window appears to be narrow. Again, fill factor losses were attributed to contact resistance issues. The high frit contact glass acted similarly to the medium frit content glass.

In addition to the work with inks containing varying concentrations of glass frit, we evaluated front contact inks from several different manufacturers. Our objective was to improve the performance and reduce the cost of contact metallizations. For the initial work, single crystal wafers from the same source were used.

One particular front contact ink (Sample B) was supplied to us to reduce the front firing temperature and improve the fill factor. This ink was tested using a belt speed - temperature matrix (the usual first level screening experiment). We found that this ink performed better at faster belt speeds as compared to the established belt speed used for the control ink. The ink gave improved current, fill factor and power at the higher belt speeds. Because of the relatively small sample size, the statistical significance of these results is uncertain. The increase in throughput due to a belt speed increase is of interest for large-scale manufacturing.

Another front contact ink (Sample A) from a second manufacturer was submitted as a direct replacement for one of the front contact inks that we are presently using in production. We tested this ink first using our research printer and furnace, and then using production wafers processed by manufacturing. Cells were evaluated using split-lot electrical performance and pull strength measurements comparing the new ink to the existing ink. No changes were required to the furnace firing setpoints. Based on our results, we have recommended this ink for larger scale production tests.

Electrical results for the three front contact ink samples plus a control ink are shown in Table 1. All three inks were found to be acceptable and solar cell performance was essentially identical for all of the samples evaluated. The differences in the three inks are related to belt-processing issues.

Table 1. Fill factor data for front contact sample inks at various firing conditions. The temperatures noted are furnace setpoints, not actual wafer temperatures.

Ink	Temp. (°C)	Belt Speed (Normalized)				
		1	1.2	1.3	1.5	1.6
Control	840	74.8				
Sample B	840	72.9	74.1	75.5	75.6	74.7
	860	66.2	73.0	73.6	74.2	75.1
	880	38.4 (shunt)	63.6 (shunt)	71.2	73.6	74.7
Sample A	830	74.6	75.1	74.6	75.4	
	840	72.9	74.3	73.7	75.3	
	850	72.2	73.5	74.9	74.1	
Sample C	780	74.7	74.9	72.3	62.7 (Series)	
	800	74.7	74.7	73.8	70.5 (Series)	
	820	73.8	74.9	74.7	74.9	

Along with improved ink formulations we found that improvements in the processing of the thick film inks used for contact metallizations offer several potential avenues for efficiency improvement. In Phase II we focused on improvements in line definition of front contact inks. The target of this work was to improve line definition from approximately 250 microns to below 200 microns. The calculated gain in current, due to a reduction in shadowing, could exceed 1.5%.

Line definition improvements of front contact inks on single crystal wafers were achieved by altering the drying sequence, changing the finger line geometry in the screen, and varying the screen printer setup parameters. The solar cell production line is now routinely achieving <200 micron line definition on a production scale. These dimensions are improved from a baseline of 250 microns. The expected gain in current from these finer lines is being observed in solar cell performance and yield. These process changes will be directly applied to Silicon-Film™ wafers to achieve similar current gains.

[Large-Area Screen Printer](#)

There is an increasing need for highly automated, high speed screen printers that can handle large-area wafers and produce fine line metallizations. In the past photovoltaic manufacturers depended on screen printing equipment that was produced for the hybrid circuit business, that is, manufacturing electronic circuits on ceramic substrates for military and some

high temperature "under hood" automotive applications. In a survey of screen printer equipment manufacturers we found that any new technical screen printing equipment today is designed for and sold into the SMT business, that is, multi-layer PC boards. In that business the need for printing accuracy far outweighs the need for throughput because of the higher value added. An SMT screen printer is automated to handle different sizes of PC boards, has a vision alignment system, and cycle times that are 15 to 30 seconds long. This equipment is typically priced at over \$150,000, and is sold as one component of a highly integrated, multi-million dollar process line that consists of board handlers, printers, "chip shooters", and reflow furnaces.

During Phase II of the PVMaT contract we initiated a fairly wide survey of screen printing equipment manufacturers (or suppliers of screen printing equipment) who provide equipment for either hybrid circuit, PC board, or SMT manufacturing businesses. Many were identified in trade publications; some were identified by material suppliers, and others are known as present or former suppliers of equipment to PV manufacturers. Each of these equipment suppliers were provided a set of machine specifications which included the following: minimum print speed was to be 1,000 wafers per hour and the printed wafers were to be delivered to a 36" belt furnace. Our needs and plans were discussed, and their level of interest in providing equipment for our process was gauged.

While some screen printer equipment suppliers appeared to be somewhat responsive to us, many others were not at all interested in the photovoltaic business. The reason given is that photovoltaics does not provide enough of a business opportunity to justify the time and engineering cost of designing and producing new equipment, or even modifying their existing equipment design, and then supporting the equipment. Formerly independent equipment suppliers are being purchased by larger organizations, and some suppliers have disappeared altogether. Many suppliers do not provide equipment for hybrid circuit printing, instead concentrating on the more lucrative SMT business.

Although the results of our survey and subsequent discussions were not very encouraging, there are two screen printing equipment suppliers that look promising as eventual suppliers. It is clear that alternative approaches may be necessary to obtain the equipment that is necessary to increase the area and the throughput of the contact metallization processes. Accordingly, "non-traditional" suppliers of screen printing equipment, that is, equipment used for printing objects other than circuit boards are being investigated.

Large Area Modules

Residential PV systems have design requirements that differ from traditional PV systems. Aesthetics, installation cost, and installation convenience are important considerations in residential applications. Furthermore, installation issues are usually ignored when a module is designed. In order to address these special issues and simplify installation, the design of a large area Silicon-Film™ rooftop module system began by surveying selected PV system installers. The installers were asked to enumerate features that they felt should constitute an "ideal" residential system. Through several iterative loops of design and feedback, a design package was constructed.

Customer Requirements

As a result of our interviews with PV system installers, we developed a list of design elements. In general terms, large modules are desirable because they improve installation efficiency by filling the roof faster. Large modules also reduce the number of electrical and mechanical connections. A specialized framing system is another desirable feature as few PV modules on the market were designed to meet the unique needs of residential roof-top installations. Based on our research, the “ideal” residential system is summarized by the following list:

Size and Shape:

- Module should be larger than existing designs to minimize the number of roof penetrations, but no larger than 48” x 92” which will be too unwieldy.
- Module should be rectangular in shape; 2:1 ratio is ideal.
- An individual module should weigh no more than 100 lbs.
- Two installers should be able to handle the module without special lifting equipment or scaffolding. Standard roofing equipment should be used.

Frame and Mounting

- Bare edges of tempered glass laminates should be protected, either by a frame member or by a plastic protection strip.
- The mounting system should be flexible enough to allow the module to be mounted in either portrait or landscape orientation.
- Penetrations into the roof should be made in-line with rafters to minimize the potential for roof leaks and to improve uplift resistance. Rafters cannot be assumed to be regularly spaced, e.g. 24” – 36” on center.
- The modules should mount no more than 2” – 3” from the roof surface to minimize the profile.
- The finished array should appear monolithic with minimal holes and gaps between individual modules.
- Aesthetic considerations often outweigh performance issues in residential installations.

Electrical

- Module arrays should be flexible enough to be configurable on site from 36 to 48 Volts to interface with common inverters.
- Modules should be equipped with quick UL recognized connectors and adequate cable length to speed on-site “field” wiring.
- Sides of module frame should form a “conduit” for the array wiring to hide and protect the wires.
- The system must conform to all UL 1703 requirements.

Laminate Design

Laminate design began with two 72 cell footprints, 12x6 and 9x8. The designs met the criteria of doubling module size while retaining the ability to be manufactured in AstroPower's laminators. Customer feedback indicated that the 9x8 design was too square, thus limiting installation options. As a result, the 12x6 design is currently the preferred format (Figure 17). The 12x6 design can easily be scaled to 12x7 and 12x8 circuits if additional power is required. All of the large laminate designs are collectively known as Big Area Modules, BAM's.



Figure 17. 12x6 solar cell large area module

The 12x6 BAM laminate measures 76.5" x 38.1" and is manufactured using standard 1/8" thick tempered glass. This thickness was chosen to minimize weight and to remain consistent with current AstroPower designs. However, it was determined early in the design process that unsupported 1/8" glass of the required size would deflect approximately 1" at mid-span (in a simply supported frame). This issue dictated that the framing system must incorporate a support member on the backside of the laminate (Figure 18).

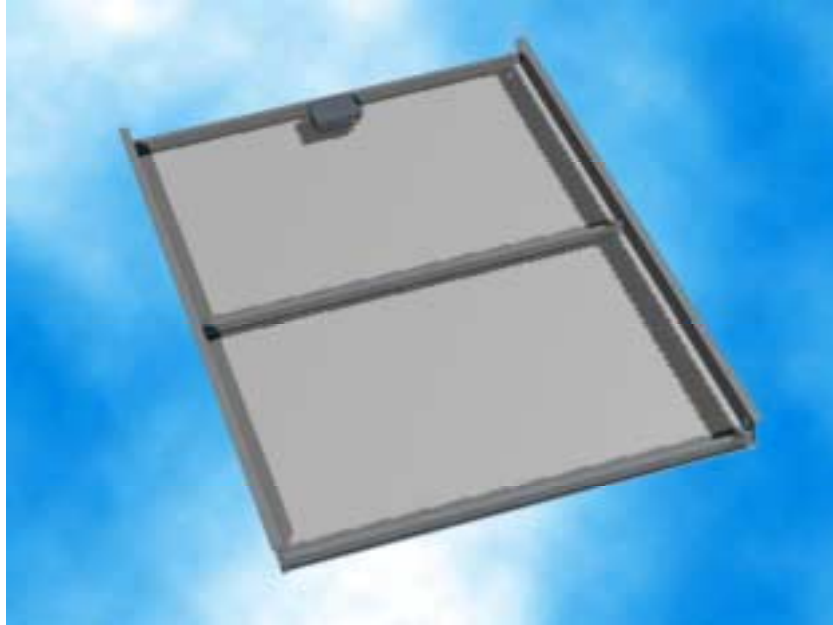


Figure 18. Backside of large area module laminate

An alternate design has been developed that utilizes two separate laminates mounted in one roof mount frame. The assembled module uses two APX-90SF laminates, each measuring 38.1" x 45.5". This design was primarily developed to take advantage of existing laminate designs and to simplify construction of a prototype (Figure 19).

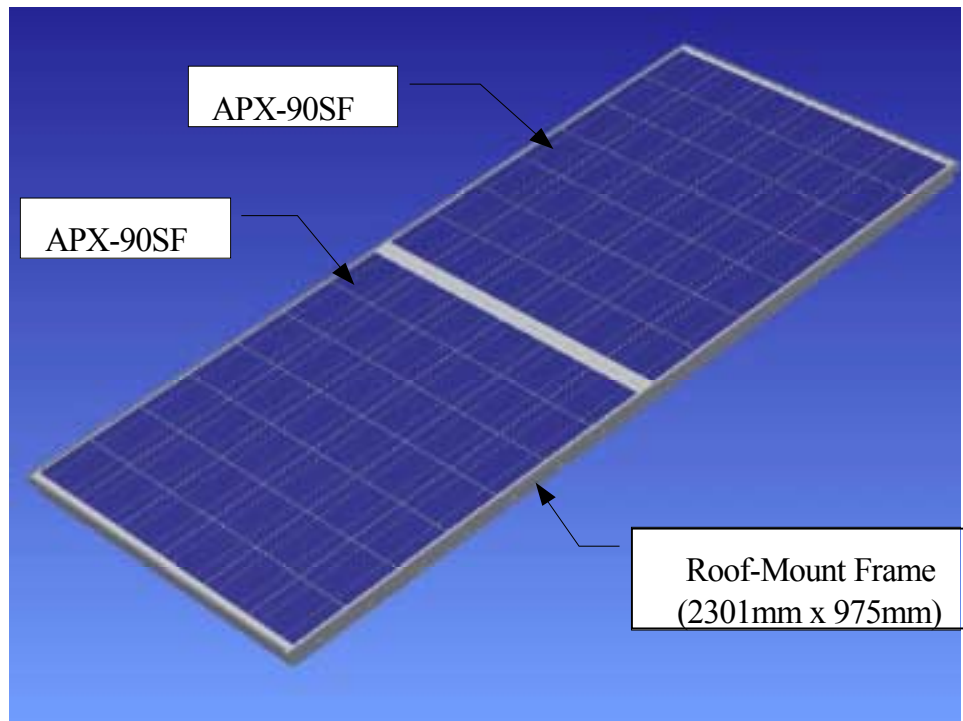


Figure 19. Prototype large area Silicon Film™ module – front view

Frame and Mounting Design

Feedback from installers stressed the need for a flexible framing/mounting system as the most important design criteria. Flexibility is paramount because residential installations can vary tremendously in terms of roof design, size and condition. Although some installers will mount the modules to the roof decking, a system that could not be easily attached to the rafters would have a very limited installer base (many municipal codes require rafter attachment). Roof penetrations into rafters are desirable in order to reduce the chance of leaks. Our early designs were intended to fasten into rafters but relied on the premise that roof rafters are on 16 or 24" centers. However, we learned from the installers that rafters are rarely at predictable or repeatable spacing. We determined that a design based on regular rafter spacing would have limited usefulness. In our current approach, we adopted the use of L-shaped mounting brackets. The rafters are first located and marked on the roof surface. Then, the L-brackets are installed into roof rafters. After the first module is positioned in the desired location, it is then bolted to the brackets by screwing a self-tapping screw into the module frame. After the lower edge is secured, the opposite side of the module is fastened to the roof in the same manner.

After both sides of the first module are bolted in place, the second module is pinned to the first module using predrilled holes in the frame. The pin joining method is beneficial because it reduces the total number of roof penetrations required for a given array. Pin joining also speeds and simplifies the installation process. After making the pin connection, L-brackets are installed to support the back edge of the module. The pinning/bracket process is repeated up the roof until the required module rows are installed (usually two or three). Figure 20 shows the many features of the new module design.

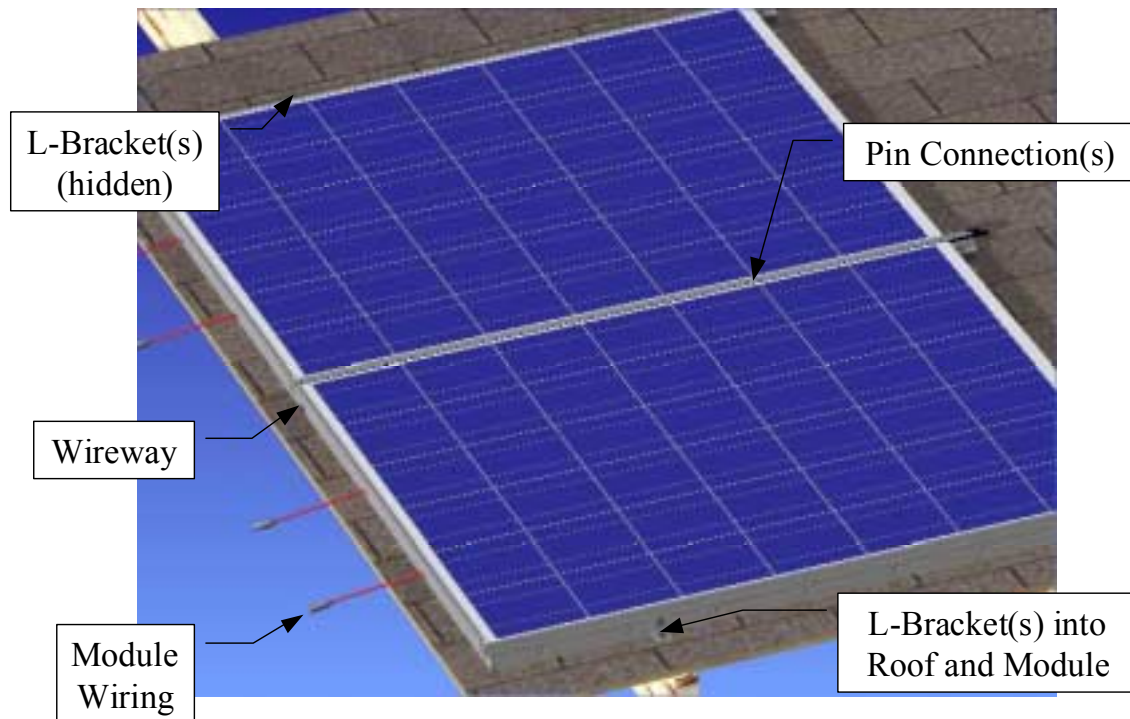


Figure 20. (Partial) modules mounted on roof

The pictured design allows the module to be mounted in either landscape or portrait orientation, which provides the installer with greater installation flexibility. The module incorporates a wire channel on each side, an improvement over previous designs, which limited the wire channel to two sides.

The current design package for a large area Silicon-Film™ rooftop module system addresses many of the special needs highlighted by customers and PV installers. As designed, the system will also help reduce costs at the customer job site. Additional refinements of the design now allow the modules to be mounted in either landscape or portrait orientation. Construction of a prototype for load testing is the next step.

Module Cost Reduction

Junction Box

During this phase, AstroPower developed and put into production a new module J-box that reduces module material and assembly costs. The new UL-approved junction box has conduit fitting knock-outs. This change reduces the number of parts required to assemble a module as knock-out hole plugs are not needed. Another benefit of the new box is the use of a water tight box lid that does not use a gasket, further reducing the materials cost and making installation easier.

Several new approaches to making electrical connections inside the module J-box were investigated with the goal of eliminating both welded diode connections and soldered ribbon tabbing connections. A low-cost, stainless steel screw-type connection was developed for direct connection of the module ribbon to the terminal block. This design is based on an available, UL-recognized terminal block with a custom jumper to connect the bypass diodes on the terminal block. Using these jumpers, the total parts count for the terminal block assembly was reduced from 23 to 18 components. The cost of these custom stampings is significantly less than off-the-shelf parts from the terminal block manufacturer. A quotation for a terminal block assembly using these jumpers was obtained from an assembler, and the projected cost of the terminal block assembly was approximately 30% less than the welded diode design that had been previously investigated.

A further reduction in module cost is possible by eliminating the terminal block altogether. A growing quantity of modules is provided with leads and quick-connectors, such as those manufactured by Multi-Contact. The large-area roof-mount system will incorporate such connectors. As a result, the terminal block is only providing a means of interfacing the leads to the module. Because of this we have designed a new PC card for the J-box that eliminates the terminal block.

Summary

AstroPower solar cell manufacturing technology is steadily progressing toward cassetteless, high volume, belt-driven processes. During Phase II of AstroPower's PVMaT-5A effort, significant progress in the areas of in-line processing, solar cell efficiency, and module cost reduction have been made. In-line chemical processing equipment for the removal of the diffusion phosglass has been specified and built. Equipment for in-line sodium hydroxide etching of silicon wafers is currently under development. During Phase III work will continue in these areas and also include developments in sheet generation and contact metallization.

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13. ABSTRACT (Maximum 200 words) AstroPower is developing a manufacturing process for Silicon-Film™ solar cell production under an NREL-administered Photovoltaic Manufacturing Technology (PVMaT) cost-share program. This document reports on results from the second phase of a three-phase effort. Progress is reported on the development of new procedures and equipment for in-line wet chemical processes, sheet fabrication, solar cell processing, and module assembly. Future concepts and goals for the Silicon-Film™ process are also discussed. A major technical goal of this effort is the elimination of batch production processes in AstroPower's solar cell process. New processes are being developed that can accommodate large-area Silicon-Film™ planks in an in-line, continuous manner. During Phase II of this program, an in-line chemical etching system for removing diffusion oxides was specified, procured, and installed. Operation of this system during Phase III of this program is expected to validate the in-line approach and will provide valuable information for use in the design of a second, and more challenging, in-line etch system. Significant progress was made during this reporting period in the development of new screenprinting ink formulations for both the front and back metallization of Silicon-Film™ solar cells. Cost reductions and efficiency improvements were achieved as a result of these efforts. Progress was made in the design of a new Silicon-Film™ plank machine, as well as in improved processes to fabricate this material into cost-effective and efficient solar cells. Additionally, a new large-area module concept was developed and prototyped during this phase of the PVMaT program.				
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