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A Novel Manufacturing Process For Fabricating Cds/CdTe Polycrystalline Thin-Film Solar Cells

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A NOVEL MANUFACTURING PROCESS FOR FABRICATING CdS/CdTe POLYCRYSTALLINE THIN-FILM SOLAR CELLS

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ABSTRACT: There are several production disadvantages inherent in conventional SnO_2/CdS/CdTe manufacturing processes. In this paper, we report a novel manufacturing process for fabricating polycrystalline Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe thin-film solar cells that yielded a CdS/CdTe device with an NREL-confirmed efficiency of 14.0%. This process addresses undesirable manufacturing issues such as time-consuming and expensive heat-up and cool-down processes and generation of large amounts of liquid waste. CdTe cells prepared by this process have good performance, good uniformity, acceptable device stability, and excellent reproducibility.
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1. INTRODUCTION

Cadmium telluride has been recognized as a promising photovoltaic material for thin-film solar cells because of its near-optimum bandgap of ~1.45 eV and its high direct-absorption coefficient. Commercial-scale modules with efficiencies of 6%-10% have been produced by several CdTe deposition techniques [1-5]. However, performance and reproducibility of CdTe modules have been limited by the conventional SnO_2/CdS/CdTe device structure used for many years. For example, higher short-circuit current densities (J_{sc}) can be achieved by reducing the CdS thickness in CdTe cells. However, reducing the CdS thickness can adversely impact device open-circuit voltage (V_{oc}) and fill factor (FF). Hence, a thicker CdS layer has to be used in most CdTe module manufacturing processes, which results in low J_{sc} (18-20 mA/cm^2). In addition, there are several undesirable production disadvantages in the conventional CdTe module manufacturing processes (see Figure 1). For example, the transparent conductive oxide (TCO) films are typically deposited at high temperatures using chemical-vapor deposition (CVD) or spray techniques. The CdS window layer is deposited at lower temperatures in liquid solution using chemical-bath deposition (CBD) or at high temperature using close-spaced sublimation (CSS) or CVD techniques.

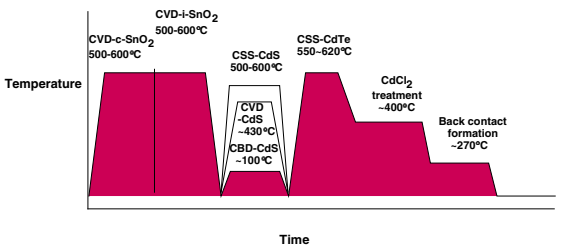

Figure 1. Conventional SnO_2/CdS/CdTe device manufacturing processes.

The high-temperature deposition process requires time-consuming and expensive heat-up and cool-down process segments. In addition, the treatment of a large amount of liquid waste solution generated in wet processes can increase manufacturing costs. Therefore, it is necessary to develop a more manufacturing-friendly process for fabricating CdTe modules. In this paper, we report a novel manufacturing process for fabricating Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe solar cells with potential for low cost and high throughput [6].

2. NEW MANUFACTURING PROCESS

Figure 2 shows a new CdTe device manufacturing process developed at NREL. Compared to conventional manufacturing processes, there are several new aspects in this CdTe device process. First, a novel device structure Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe developed at NREL has been used in the new process (see figure 3). In the modified device structure, the Cd_2SnO_4 (CTO) film replaces the conventional SnO_2 TCO film as a front-contact layer, and a Zn_2SnO_4 (ZTO) film is integrated into the device as a buffer layer. We have demonstrated that the device performance and reproducibility can be significantly improved by using this modified device structure [7-11]. For example, CTO TCO films have higher conductivity, higher transmission, and a smoother surface compared to the conventional SnO_2 films. CTO-based CdTe cells also have a higher average short-circuit current density (greater by 1 mA/cm^2) than SnO_2-based CdTe cells. Integrating a ZTO buffer layer helps maintain high V_{oc} and fill factor for CdTe cells when the CdS thickness is reduced to improve J_{sc}. Second, the first three layers (including CTO TCO layer, ZTO buffer layer, and CdS window layer) are prepared by the same deposition technique – RF magnetron sputtering at room temperature. RF sputtering is a mature technology with demonstrated production scaleability. Third, the new process has only one heat-up segment in the entire device fabrication process. The recrystallization of the first three layers and the interdiffusion at the three interfaces (including the CTO/ZTO, ZTO/CdS, and CdS/CdTe

interfaces) are completed during CdTe deposition by the CSS technique.

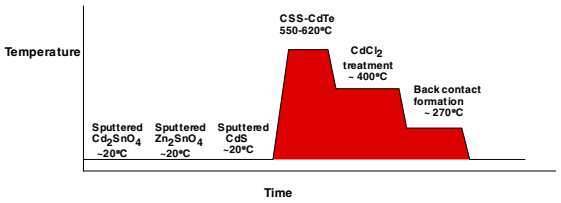

Figure 2. Novel CdTe device manufacturing process.

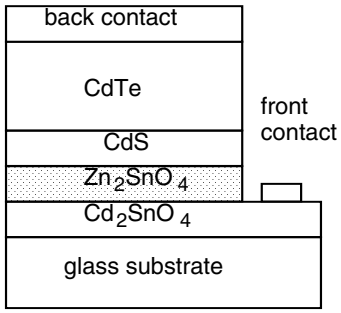

Figure 3. A modified CdS/CdTe device structure used in this process.

3. EXPERIMENTAL

The first three layers of the device (CTO, ZTO, and CdS) were deposited at room temperature by RF magnetron sputtering. The CTO and ZTO layers were prepared in pure oxygen using commercial hot-pressed oxide targets, and the CdS film was deposited in pure Ar. The CdTe layer was deposited by the CSS technique at a substrate temperature of 570°-625°C for 3 minutes. Samples then received a vapor $CdCl_2$ treatment at 400°-420°C for 15 minutes. The thickness of the CTO, ZTO, and CdS layers was varied from 1000Å to 3000Å. Several techniques were used for material and interface characterization, including Hall effect measurement, visible/near-ultraviolet spectrophotometry, X-ray diffraction (XRD), X-ray photoemission spectroscopy (XPS), secondary ion mass spectroscopy (SIMS), and transmission electron microscopy (TEM). The standard current-voltage (I-V) curves, absolute external and internal quantum efficiencies, time-resolved photoluminescence, saturation dark-current density, and device diode factor have been measured for device performance analysis.

4. RESULTS

In this new process, the first three layers (CTO, ZTO, and CdS) were deposited at room temperature. As-deposited CTO and ZTO films have an amorphous structure and very poor electrical and optical properties. After CdTe deposition at 570°-625°C for 3 minutes, the properties of the two films changed significantly in terms of material structure, and electrical and optical properties. We have worked to understand the changes for the two layers associated with processing. Table 1 shows that the resistivity of a CTO film decreases with CSS-CdTe deposition. Figures 4 and 5 show that transmission and structure of a CTO film change with CSS-CdTe deposition, respectively. It can be seen that the as-deposited CTO film has an amorphous structure, very high resistivity (>25 Ω cm), and a low bandgap (~2.6 eV). After CdTe deposition at 620°C for 3 minutes, the CTO film structure changed to a spinel polycrystalline structure, and the material properties improved significantly. The post-heat-treated CTO film has a bulk resistivity (~2.5×10^{-4} Ω cm) more than 5 orders of magnitude lower than the as-deposited CTO film, and it has a higher bandgap (~3.1 eV) and good transmission. The ZTO film shows similar changes after CSS-CdTe deposition. As-deposited ZTO films have an amorphous structure and very high resistivities (>1000 Ω cm). After CSS-CdTe deposition at 620°C, the ZTO film changed to a spinel polycrystalline structure, and its resistivities improved to 1-10 Ω cm, roughly matching the CdS resistivity. The bandgap of the ZTO film does not change (~3.6 eV) after CSS-CdTe deposition, but the transmission improved significantly.

Table 1. Resistivity changes of a CTO film after CSS-CdTe deposition at 620°C.

	Rs (Ω/Sq)	ρ (Ω cm)
As-deposited	$>10^6$	>25
After CdTe deposition at 620°C	~ 9	$\sim2.5\times10^{-4}$

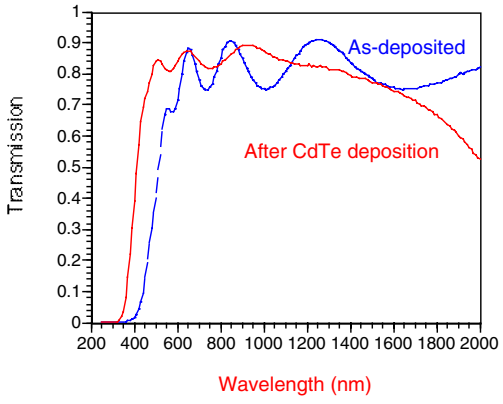

Figure 4. Transmission of a CTO film changes with CSS-CdTe deposition at 620°C.

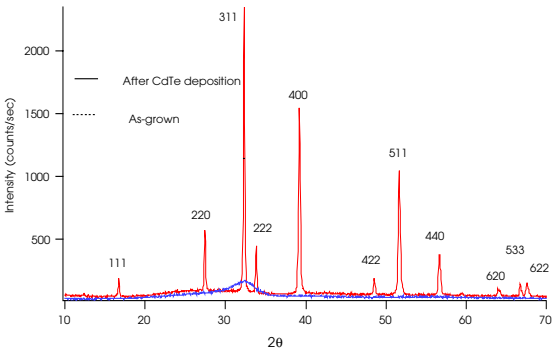

Figure 5. Structure of a CTO film changes with CSS-CdTe deposition at 620°C.

As-deposited sputtered-CdS films have small grain sizes (500Å~1000Å), smooth surfaces (average surface roughness R_a ~ 15Å), and high resistivity. After annealing at high temperature (400°~500°C), the grain size increased to the range of 1000Å~2000Å and the surface roughened (R_a~200Å). The post-heat-treated CdS films exhibited (002) preferred orientation.

We also investigated the interdiffusion among the four layers: CTO, ZTO, CdS, and CdTe. For example, the interdiffusion at both the CTO/ZTO interface and the ZTO/CdS interface has been studied. This was accomplished by depositing a CTO film on a 7059 Corning glass substrate at room temperature by RF sputtering. A ZTO/CdS layered structure was then deposited on a second piece of 7059 glass. After deposition, the two samples were annealed face-to-face at 620°C in Ar. SIMS and XPS techniques were used to determine the composition changes for these two samples. XPS and SIMS results show that interdiffusion occurs at both the CTO/ZTO interface and the ZTO/CdS interface. Figure 6 shows the SIMS depth profiles. It can be seen that Zn from the ZTO film diffused into both the CTO film and the CdS film, and Cd from both the CTO film and the CdS film diffused into the ZTO film. This interdiffusion can be used to improve device performance and reproducibility [12]. For example, the interdiffusion at both the CTO/ZTO interface and the ZTO/CdS interface can relieve the stress resulting from the $CdCl_2$ treatment, yielding improved device adhesion. The improvement of device adhesion provides much greater latitude in optimizing the $CdCl_2$ treatment process, and thus, to improve device junction properties and CdTe film quality.

We have fabricated a $Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe$ solar cell with an NREL-confirmed efficiency of 14.0% (V_{oc} = 841.1 mV, J_{sc} = 22.28 mA/cm^2, fill factor = 74.95%) by this new process (see Figure 7). We believe that this is the highest NREL-confirmed efficiency ever reported for any thin-film solar cell with both the TCO and the CdS layer deposited at room temperature.

The device results also demonstrate that CdTe cells prepared by this process have good uniformity and reproducibility, which is desirable for scaling up the process. Table 2 shows the I-V data of four cells prepared from one substrate. The good device uniformity can help reduce the efficiency gap between small-area cells and modules.

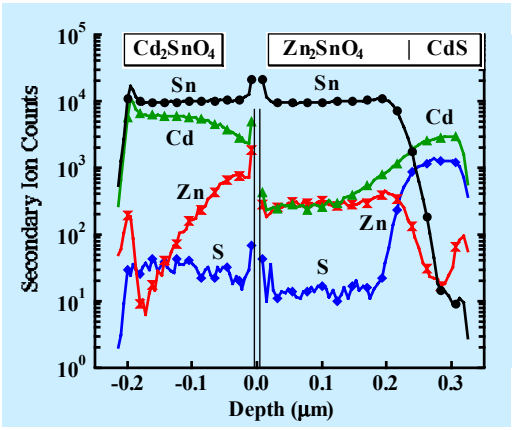

Figure 6. SIMS depth profile shows interdiffusion at the CTO/ZTO and the ZTO/CdS interfaces after annealing at 620°C.

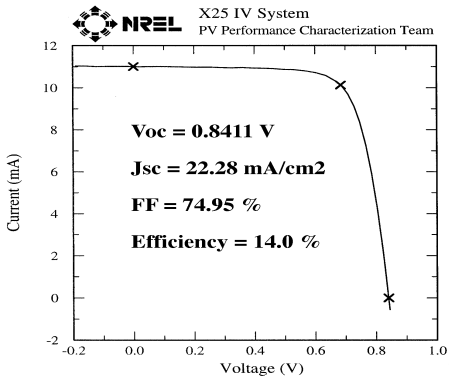

Figure 7. I-V curve of a $Cd_2SnO_4/Zn_2SnO_4/CdS/CdTe$ cell prepared by the new process.

Table 2. Uniformity of CdTe cells prepared by the new process.

Device #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
W331-A	840	22.9	73.3	14.1
W331-B	838	22.5	73.2	13.8
W331-C	835	23.3	72.9	14.2
W331-D	835	23.3	71.5	13.9

Preliminary device reliability results obtained using accelerated testing procedures indicate that the CdTe cells prepared by the new process behave similarly to NREL baseline CdTe cells. Figure 8 shows the CdTe device stability as a function of stress time. The device was stressed at 100°C, at maximum power point, and at 2-suns illumination. For these stress conditions, the acceleration factor is believed to be 500-1000X.

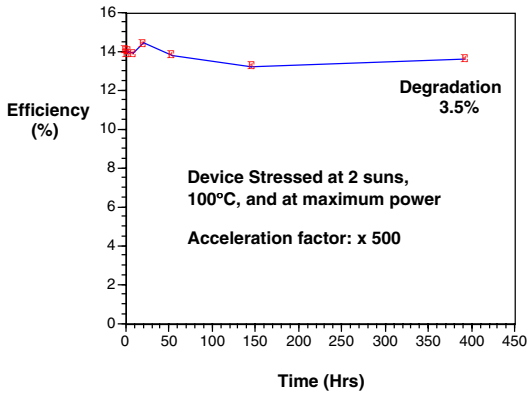

Figure 8. Stability of a CdTe cell prepared by the new process.

5. POTENTIAL BENEFITS

We expect to obtain several benefits from this new process:
(1) This process can significantly reduce the thermal budget, because the first three layers are deposited at room temperature and the entire process has only one heat-up segment.
(2) This process can significantly reduce the process time, thus increasing the throughput. Because the first three layers are deposited at room temperature, no time is required for substrate heat-up and cool-down. In addition, because the first three layers are prepared by the same deposition technique, no additional time is required for substrate loading and unloading.
(3) This is a completely dry process using two compatible deposition techniques: CSS and RF sputtering. Hence, no liquid waste will be generated, and a "continuous" process is possible.
(4) This process does not rely on commercial SnO_2-coated glass, and therefore, we can tailor the TCO properties to optimize device performance.
(5) This process can provide high yields, because all layers are prepared by two compatible deposition techniques: CSS and RF sputtering. Substrates can stay in vacuum through the entire process, and thus, devices have "clean" interfaces. In addition, devices prepared by the new process have no adhesion problems, due to the benefits of the ZTO buffer layer.
(6) This process can produce high-performance CdTe cells with good uniformity, good reproducibility, and acceptable device stability.

6. CONCLUSIONS

We have developed a low-cost manufacturing-friendly process with the potential of high throughput for fabricating CdTe solar cells. CdTe cells prepared by this process have good performance, good uniformity, acceptable device stability, and excellent reproducibility. We have demonstrated the highest NREL-confirmed efficiency (14.0%) ever reported for any thin-film solar cell with both the TCO and the CdS layer deposited at room temperature. These results, coupled with the improved process manufacturability, provide an attractive alternative for fabricating CdTe modules.

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REFERENCES

[1] R.C. Powell, U. Jayamaha, G. Dorer, and H. McMaster, Proceeding of 15th NREL/SNL PV Program Review Meeting, pp. 31-37, (1998).
[2] D. Bonnet and M. Harr, Proceeding of 2nd World Conference on PVSEC, pp. 397-402, (1998).
[3] S.P. Albright, B. Ackerman, and J. Jordan, IEEE Transactions on Electron Devices, **37**, No. 2, pp. 434-437, (1990).
[4] H. Ohyama, A seminar titled "Characterization of CdS Thin-Film in High-Efficiency CdS/CdTe Solar Cells" at NREL, (2000).
[5] D.W. Cunningham, K. Davies, L. Grammond, J. Healy, E. Mopas, N. O'Connor, M. Rubcich, M. Sadeghi, D. Skinner, and T. Trumbly, 16th European PVSEC, (2000).
[6] X. Wu and P. Sheldon, U.S. Patent: "Novel process for fabricating CdS/CdTe thin-film solar cells, and cells produced thereby."
[7] X. Wu, T.J. Coutts, P. Sheldon, and D.H. Rose, U.S. Patent 5922142, (1999).
[8] X. Wu, P. Sheldon, T.J. Coutts, D.H. Rose, W.P. Mulligan, and H.R. Moutinho, Proc. 14th NREL/SNL PV Program Review Meeting, pp. 693-702 (1996).
[9] X. Wu, P. Sheldon, T.J. Coutts, D.H. Rose, and H.R. Moutinho, Proc. 26th IEEE PVSC, pp. 347-350 (1997).
[10] X. Wu, P. Sheldon, Y. Mahathongdy, R. Ribelin, A. Mason, H.R. Moutinho, and T.J. Coutts, Proc. 15th NREL/SNL PV Program Review Meeting, pp. 37-41, (1998).
[11] X. Wu, R. Ribelin, R.G. Dhere, D.S. Albin, T.A. Gessert, S. Asher, D.H. Levi, A. Mason, H.R. Moutinho, and P. Sheldon, "High-Efficiency $Cd_2SnO_4/Zn_2SnO_4/Zn_xCd_{1-x}S$/CdS/CdTe Polycrystalline Thin-Film Solar Cells," to be published.
[12] X. Wu, S. Asher, D.H. Levi, D.E. King, Y. Yan, T.A. Gessert, and P. Sheldon, "Interdiffusion of CdS and Zn_2SnO_4 Layers and its Application in CdS/CdTe Polycrystalline Thin-Film Solar Cells," to be published.

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