PROGRAM AND PROCEEDINGS

NCPV Program Review Meeting 2000

April 16–19, 2000

Adam's Mark Hotel

Denver, Colorado

NREL

Sandia National Laboratories

NOTICE

Available electronically at http://www.doe.gov/bridge

Available for a processing fee to U.S. Department of Energy and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: reports@adonis.osti.gov

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Research Needs of c-Si Technology Required to Meet Roadmap Milestones

D. S. Ruby
Sandia National Laboratories
MS 0752, Albuquerque NM

T. F. Ciszek and B. L. Sopori
National Renewable Energy Laboratory
1617 Cole Blvd, Golden CO 80401

ABSTRACT

In this paper, we examine the areas in c-Si growth, materials, and processing that require improvement through research to overcome barriers to the implementation of the PV Roadmap's Si goals.

1. C-Si Materials Growth

The key issues in c-Si materials growth for reaching the Roadmap's module production goals are throughput of the growth processes, control of impurities and defects, and effective utilization of silicon-feedstock material. Trade-offs are required in order to achieve an optimum balance between these key issues. Let's look at them in more detail and examine the associated R&D needs.

Throughput of the Growth Processes

To improve PV module throughput to the Roadmap target of 200 MW/factory/year, the typical Si-PV factory must produce >4,000 m^2/day of silicon. This assumes 15% modules capable of generating 150 W_p/m^2, and round-the-clock operation with 10% down time and/or yield losses. For the growth methods currently in use, the throughput per machine and total number of growth machines (growers) required is approximately:

Growth Method	Throughput (m^2/day)	No. of Growers
Dendritic Web	1	4,000
ESP/String Ribbon	1.7	2,350
Capillary Die Growth	20	200
Czochralski (CZ) Growth	30	133
Directional Solidification	70	57
Float-Zone (FZ) Growth	80	50
Electromagnetic Casting	600	7
Substrate Melt Shaping	>1000	<4
Thin-Layer Si Growth	?	?

For ingots, the throughput numbers assume concomitant wire-sawing yielding 20 wafers/cm of ingot. Most thin-layer growth approaches are not at a mature enough stage to estimate throughputs. Research is required to improve the throughput of existing growth methods, to evolve higher-throughput methods, and to demonstrate comparable throughputs with thin-layer growth approaches.

Control of Impurities and Defects during Growth

The growth methods that can sustain a factory with fewer than ten growth machines will generate ingot material with smaller grains than other approaches. Or they generate sheet material with still smaller grains as well as impurities from melt/substrate and melt/ambient interactions. Research is required to improve grain size and perfection, to reduce impurity contents during growth by these fast methods, and to understand defect and impurity behavior in the growth processes, with the goal of in-situ amelioration of adverse effects.

Effective Utilization of Silicon Feedstock Material

In the growth of the PV and integrated-circuit (IC) semiconductor silicon industries, we have, on average, reached the point where the PV demand for low-cost Si feedstock exceeds the IC supply of off-specification and reject Si. One approach that can be taken is to develop alternatives to the silane and chlorosilane processes for creating IC-purity silicon from metallurgical-grade (MG) Si, with the goal of obtaining sufficient, but not excessive, impurity levels for solar-grade silicon at a lower cost. Another approach is to focus on thin-layer Si growth methods that utilize less silicon. Both are daunting research tasks in light of the throughput and module performance requirements of the Roadmap.

2. Material Quality Enhancement in Si Solar Cells

Low-cost silicon wafers used in commercial production of solar cells contain high concentrations of impurities and defects in the as-grown form. The PV industry uses economical processes that have been optimized to upgrade the material quality by incorporating impurity gettering and passivation during cell fabrication. Current solar cells have efficiencies in the 14%-15% range, which is a remarkable achievement. However, higher cell-efficiencies must be reached to meet the future goals of the PV Industry Roadmap. It is imperative that advanced processing methods be developed that can overcome current limitations in the material quality of solar cells. Key issues in the device processing are: developing techniques that can further improve the device performance through quality enhancement of the substrate; implementing these advanced approaches as high-throughput production processes; ameliorating the impurity and defect issues through use of thinner devices; and improving process reliability through efficient monitoring.

Impurity gettering

In solar cell fabrication, impurity gettering is accomplished through phosphorous diffusion and Al alloying employed for junction and contact formation, respectively. These processes are able to remove a majority of dissolved transition-metal impurities from the wafer. Recent research has shown that although the majority of the cell area exhibits strong gettering, large regions (~20%) show low performance. These regions, which have been identified as "defect clusters," are decorated with precipitated impurities. Because precipitated impurities are immobile, it is difficult to getter them by standard solar- cell

fabrication processes. Modeling results have shown that these regions act as shunts to degrade voltage-related cell parameters. Their removal from the wafer necessitates their dissolution with concomitantly long, high-temperature anneals. Thus, the challenge is to invent processes to reduce the time and/or temperature for gettering such precipitates. One approach is to inject point defects during the process.

Modeling results show that successful gettering of precipitated impurities will result in 18%-20% efficient cells on the low-cost material. Alternately, it may be necessary to perform crystal growth with the objective of eliminating impurity precipitation. These new considerations may redefine the as-grown material quality and crystal growth conditions for low-cost Si.

Hydrogen passivation

H-passivation is used as a standard process by many companies in solar-cell manufacturing. Typically, hydrogen is incorporated during plasma-enhanced chemical vapor deposition (PECVD) nitridation followed by a higher temperature drive-in process. The detailed mechanisms of H-diffusion and passivation are still not well understood. Because PECVD can be tailored to include surface passivation, such a process can be very valuable. It is interesting to note that effective passivation also requires that impurities be in a dissolved state. The challenges are to develop simpler, more effective passivation processes based on a comprehensive understanding of passivation mechanisms. An important issue is whether hydrogen can passivate defect clusters.

Processes for increased throughput

It is clear that the processes for upgrading material quality must constitute standard procedures of cell fabrication that are compatible with high throughput, without incurring additional process costs. Forming gas annealing, rapid thermal processing (RTP), continuous optical furnaces, and low-temperature oxidation are potential future processes. New designs are needed to ensure throughputs that are compatible with the needs of the PV industry.

Thinner wafer processing

For the same material quality, thinner wafers can yield higher cell performance. Another important advantage of thin cells is that their passivation and gettering processes can be less time consuming. Thus, much emphasis will be placed on thin cells. However, thinner wafers raise a variety of issues related to the need for:

- Significantly lower interface recombination through surface passivation.
- Reduced stresses due to metallization and asymmetric depositions.
- Automated handling for minimum breakage.

3. Crystalline-Si Cell Processing

The PV Roadmap efficiency goals for c-Si cells call for production-line average efficiencies of 16% in 3 years, 18% in 10 years, and 20% in 20 years. Industrially-produced cells will need to incorporate many of the high-performance features demonstrated by laboratory cells, but use low-cost, high-throughput fabrication techniques.

Low-recombination emitters

High performance requires the use of passivated emitters that have a selectively-doped emitter profile. This allows the Si to remain highly doped beneath the gridlines for low contact recombination and resistance, but more lightly doped between gridlines for reduced emitter recombination. The lightly doped portion of the emitter needs to have excellent surface passivation to avoid losses due to surface recombination. These selective emitter structures have been demonstrated by several research groups, some using single-diffusion techniques amenable to mass production.

Surface passivation

Plasma-deposited silicon-nitride films have been shown to provide excellent emitter and rear-surface passivation. They also double as an effective antireflection coating. In addition, they can provide good bulk-defect passivation by providing a source of atomic hydrogen, which can diffuse into the bulk to passivate defects and impurities. This can allow use of lower-quality feedstock or growth methods. The critical need is to design a high-throughput plasma deposition system with low operational cost.

Thinner wafers

Besides affording lower cost through better material utilization, thin cells are more tolerant of lower-quality bulk Si. However in order to maintain performance, thin cells require excellent light absorbing properties and low back-surface recombination.

Texturing

Lower-cost multicrystalline, sheet, and ribbon Si need affordable texturing to reduce front-surface reflectance and redirect absorbed light obliquely within the cell. This increases optical path length, generates carriers closer to the junction for increased collection, and can trap weakly-absorbed light through total internal reflection.

Self-doping metallizations

Metals which contain appropriate dopants have the potential to form self-aligned selective-emitters and back-surface fields at low cost by avoiding the need for additional diffusion steps. Some new metal deposition techniques also have the potential to reduce contact and series resistance by avoiding the use of oxide frit and organic binders.

Back-contacts

Cells with rear gridlines can benefit from the avoidance of gridline shadowing and may allow significant cost-savings due to simplified cell-interconnection methods.

4. Summary

The challenges for c-Si cells to meet the Roadmap goals are substantial. At the projected production levels, it will be necessary to have sources of low-cost solar-grade silicon or to evolve growth processes that utilize much less material. High-throughput growth processes with low defect and impurity concentrations will also be a necessity. Novel high-throughput cell processing for higher device efficiency and low-cost material upgrading will also be needed.