Capabilities of the High Voltage Stress Test System at the Outdoor Test Facility

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1. Abstract

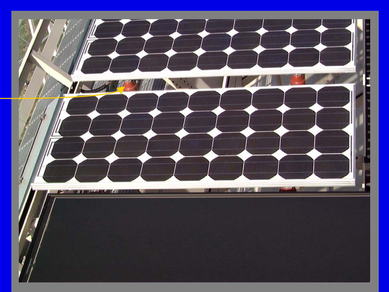
We illustrate the capabilities of the High Voltage Stress Test (HVST) which operates continuously in the array field east of the Outdoor Test Facility at the National Renewable Energy Laboratory. Because we know that photovoltaic (PV) modules generating electrical power in both residential and utility-scale array installations will develop high-voltage biases approaching 600 VDC and 1,000 VDC, respectively, we expect such high voltages will result in current leakage between cells and ground, typically through the frames or mounts. We know that inevitably such leakage currents are capable of producing electrochemical corrosion that adversely impacts long-term module performance. With the HVST, we stress or operate PV modules under high-voltage bias, to characterize their leakage currents under all prevailing ambient conditions and assess performance changes emanating from high-voltage stress. We perform this test both on single modules and an active array.

2. Objectives & Motivation

- A Long-term (2020) goal of Solar Program Multi-Year Plan:
  - Help commercialize PV modules with 30-year lifetimes or more, while sustaining less than 0.5% annual performance degradation rate, at costs consistent with market-rates of electricity.
- In the 1980's, the Jet Propulsion Laboratory investigated connection between leakage currents and contact corrosion in PV modules and established key thresholds of accumulated charge (integral over time of leakage current) that would result in 50% failure for crystalline-silicon (c-Si) & amorphous-silicon (a-Si) modules [1]
  - For c-Si: 1–10 coulombs per linear centimeter (C/cm) of module perimeter length, and
  - For a-Si: 0.1–1 C/cm.
- Investigate effects of long-term exposure to high voltage to assess capability of PV products to meet Solar Program goals and to help identify shortcomings or improvements.

3. Technical Approach

- External High-Voltage Bias (Phase I: started in 1998, Phase II: 2001):
  - Modules deployed with frames/anchors floating with respect to ground;
  - Module terminal leads shorted together and biased at ±600 VDC at all times (except ± 2200 VDC for 1 min daily at noon);
  - Leakage currents between frames & ground monitored continuously (measured across a drop resistor) along with environmental conditions.
- Self-Bias High Voltage Array (Phase III, started in 2005):
  - Modules deployed with frames/anchors floating with respect to ground;
  - Array of 24 copper-indium-diselenide (CIS) modules deployed in two bipolar strings of 12 each, capable of nominally ±300 VDC open-circuit;
  - Programmable multi-channel electronic load connected to strings and executes full current-voltage (I-V) traces, peak-power tracking or other types of bias-profile (voltage, current) tracking continuously;
  - Monitor the leakage currents between frames and ground, plus environmental conditions with data acquisition system.

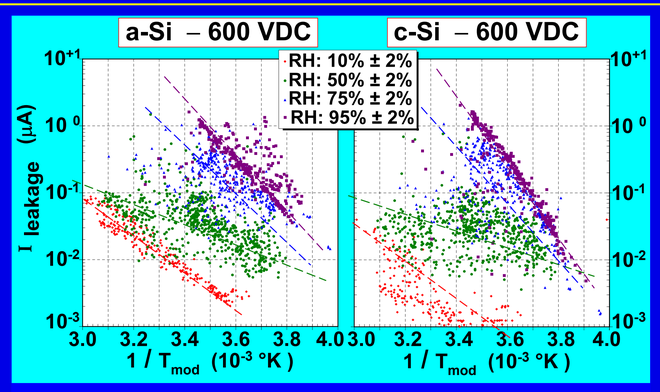


Results from Phase I:

- Leakage currents (i) were found to be thermally activated, strong functions of the ambient humidity, and could be formulated by Equation 1 below:

$$i(RH,V_b,T) = i_0(RH,V_b)e^{-E_A(RH)/k_B T} \quad (1)$$

- Where *RH, Vb*, and *T*, respectively, represent the relative humidity, bias voltage and module temperature.
- On the right-hand side of Eq. 1, the pre-factor (i_0) was found to be a function of temperature and bias, the activation energy E_A in the exponent was found to be a function of *RH*, and k_B is Boltzman's constant.
- Data illustrated in figure at right for a-Si and c-Si, within four RH windows.

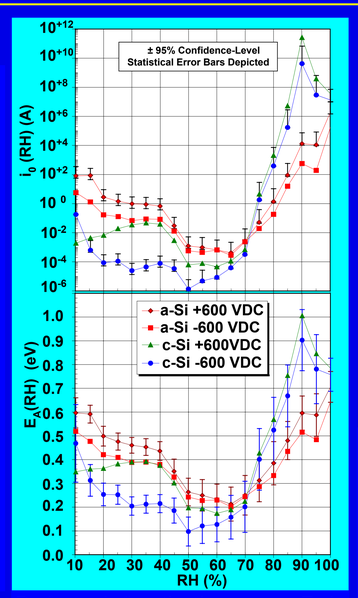


Thermally Activated Behavior: Leakage Current Data for a-Si & c-Si modules (microAmps) biased at -600 VDC plotted vs. $1/T_{mod}$ (°K *10^{-3}) within four RH windows centered at 10%, 50%, 75% and 95%.

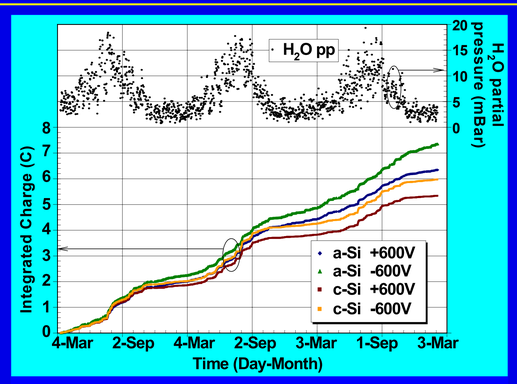
- Leakage current data for a-Si and c-Si modules exhibit temperature and RH dependence as given by Eq. 1 (dashed lines are approximate straight-line fits);
- Dotted lines at left depict straight-line fits to data, indicating changes in activation energy (E_A) and prefactor (i_0) in Eqn. 1 with changing RH;
  - at high RH, E_A ~ 0.8-0.9 eV ; at low RH, E_A ~ 0.2-0.4 eV .

Leakage Pathways

- Summary of E_A and i_0 dependence vs. RH depicted at right for four modules (2 a-Si + 2 c-Si), gives clues as to the type of conduction pathway responsible for leakage [2] :
- At high RH, it appears that conductance through the glass is the dominant leakage path:
  - Because E_A of ~0.8-0.9 eV is consistent with conduction through soda-lime glass
- At low RH, the conductance along interface surfaces between the cells, EVA and glass appears dominant.



Prefactor i_0 & activation energy E_A in Eq. 1 vs. RH for a-Si & c-Si modules



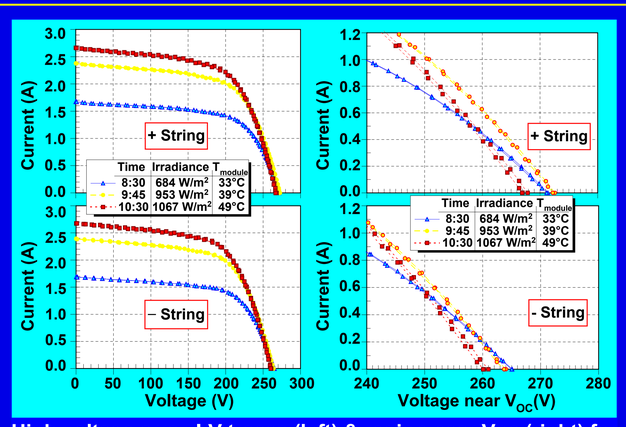
Charge accumulated over 3 years & H_2O partial pressure vs. Time for c-Si & a-Si modules at ±600 V

Accumulated Charge

- 5.2-7.2 C, over 3 years stress, equivalent to 6 years normal, due to round-the-clock operations, acceleration factor of ~ 2 estimated.
- With modules perimeters ~ 200 cm, these data indicate modules could incur minimum critical damage-thresholds doses within:
  - 18-20 years for a-Si, maybe a problem for these modules
  - More than 30 years for c-Si , not a problem for these modules.

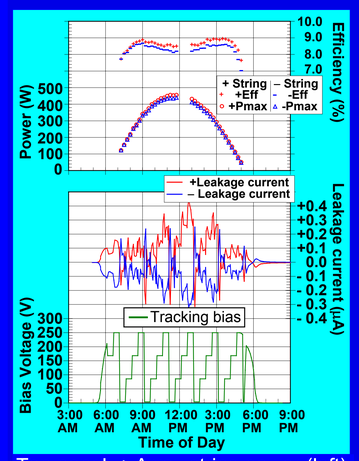
New Capabilities in 2005:

- High voltage array commenced operation in February 2005
- Data acquisition system (DAS) interfaced to multi-channel programmable electronic load (PEL) controls and monitors CIGS array:
  - Measures full I-V traces on continuous schedule during daylight hours:
    - ✓ Affords the capability to analyze sources of performance degradation as opposed to just peak-power tracking which only looks for maximum-power point current and voltage
  - Performs peak-power tracking and/or any other type of stepped bias control:
    - ✓ Allows testing of bias condition effects on performance
    - ✓ Allows correlation of bias effects on leakage currents



High voltage array I-V traces (left) & region near Voc (right) for + / – strings, measured 4/13/05 at various times & irradiance.

- Full I-V traces measured allow analysis of degradation sources:
  - Fill factor losses caused by increase in series resistance may be identified via slope near V_{OC}, may point to contact losses;
  - I_{SC} or V_{OC} degradation may point to absorber degradation;
  - Increase in shunt conductance via slope near I_{SC}
- Data in figure at right for new high-voltage array taken on Sept. 20, 2005
  - Continuous power & efficiency monitoring via the I-V traces (top panel)
  - Array bias stepped in units of 86 V, every 30 minutes (bottom panel):
    - ✓ Shows effects of bias steps on leakage currents clearly;
    - ✓ Leakage currents also exhibit transient behavior immediately after bias steps;
    - ✓ Can uncover bias effects on leakage and performance.



Top panel: ± Array string power (left) & efficiency (right) vs. Time of day
Bottom panel: Array tracking bias (left) and ± string leakage current (right) vs. Time of day

Conclusions

- High voltage leakage currents quantified and conductance pathways analyzed & identified.
- Aids early detection of potential corrosion problems in high-voltage PV power generation.
- For the HVST array, we analyze long-term changes in performance concurrently with the leakage.
- Identifies capability of PV products to meet DoE long-term goals.

References

[1] G.R. Mon, R.G. Ross. 'Electrochemical Degradation of Amorphous-Silicon Photovoltaic Modules.' Proc. 18th IEEE PVSC, Las Vegas, NV, 1142 (1985).

[2] J.A. del Cueto, T.J. McMahon, Progress in PV Res. & App. 10, 15–28 (2002).