February 2003 • NREL/CP-520-33435

12th Workshop on Crystalline Silicon Solar Cell Materials and Processes

Summary Discussion Sessions

Editor:
Bhushan Sopori

Prepared by:
Bhushan Sopori, Dick Swanson, Ron Sinton, and Teh Tan

Workshop held at Beaver Run Resort
Breckenridge, Colorado
August 11-14, 2002

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

NREL is a U.S. Department of Energy Laboratory
Operated by Midwest Research Institute • Battelle • Bechtel

Contract No. DE-AC36-99-GO10337

February 2003 • NREL/CP-520-33435

12th Workshop on Crystalline Silicon Solar Cell Materials and Processes

Summary Discussion Sessions

Editor:
Bhushan Sopori

Prepared by:
Bhushan Sopori, Dick Swanson, Ron Sinton, and Teh Tan

Workshop held at Beaver Run Resort
Breckenridge, Colorado
August 11-14, 2002

Prepared under Task No. PVP33101

National Renewable Energy Laboratory

1617 Cole Boulevard
Golden, Colorado 80401-3393

NREL is a U.S. Department of Energy Laboratory
Operated by Midwest Research Institute • Battelle • Bechtel

Contract No. DE-AC36-99-GO10337

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at http://www.osti.gov/bridge

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: reports@adonis.osti.gov

Available for sale to the public, in paper, from:
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: http://www.ntis.gov/ordering.htm

Printed on paper containing at least 50% wastepaper, including 20% postconsumer waste

Executive Summary

The 12th Workshop on Crystalline Silicon Solar Cell Materials and Processes was held in Breckenridge, Colorado, on Aug. 11-14, 2002. The workshop was attended by 106 scientists and engineers from 25 international photovoltaic (PV) and semiconductor companies, 28 research institutions, and 3 government agencies from different countries. In addition to the review and the poster presentations, there were discussion sessions to address recent progress, critical issues in implementing new technologies, and the role of fundamental R&D in the growing PV Industry. A proceedings of the papers presented at the workshop was published and provided to the attendees at the workshop registration.

The theme of the workshop was "Fundamental R&D in c-Si: Enabling Progress in Solar-Electric Technology." This theme was chosen to reflect a concern that the current expansion in the PV energy production may redirect basic research efforts to production-oriented issues. The PV industry is installing added production capacity and new production lines that include latest technologies. Once the technologies are selected, it is difficult to make changes. Consequently, a large expansion can stagnate the technologies and diminish interest in fundamental research. To prevent the fundamental R&D program being overwhelmed by the desire to help immediate engineering issues, there is a need to establish topics of fundamental nature that can be pursued by the universities and the research institutions. Hence, one of the objectives of the workshop was to identify such areas for fundamental research.

The workshop offered two special sessions: (i) Wire Sawing and Future Wafering Techniques— covering recent advances in wafer sawing, fundamental physics of sawing, and practical aspects of sawing. This session also discussed future needs and approaches for sawing wafers thinner than is possible by the current technologies; and (ii) Shunting in Si Solar Cells: Mechanisms and Diagnostics— it addressed shunting in solar cells arising from improper processing such as metal indiffusion during contact formation, incomplete edge passivation of mesa etch, and from the materials issues such as defects and precipitates in the wafer. This session also discussed methods for characterizing shunts in solar cells. A detailed summary of the discussion sessions is in preparation and will be published in the near future.

Graduate Student Awards were given to 9 students representing Georgia Institute of Technology, North Carolina State University, University of California, Berkeley, Texas Tech University, University of South Florida, and University of Arkansas, for their research work in photovoltaics. Each student received a $300 check from funds contributed by the PV industry.

Session Discussions

Session 2: Advances in Crystal Growth

Discussion Leaders: Greg Mihalik, Shell Solar; and Andrew Gabor, Evergreen Solar, Inc.

The first part of the discussion expounded on an earlier provocative proposition by Jim Rand in his oral presentation — that the one who uses the dirtiest (and hence the cheapest) Si substrates (such as AstroPower ThinFilm material) will win. Clearly, the success of using "dirtiest Si" would lean heavily on the incorporation of very effective impurity-gettering and H passivation processes in solar cell fabrication. The discussion leaders explored other strategies of crystal growth /substrate formation that could be the winning candidates for low-cost Si. This led to a lively discussion of other potential "winners" who would:

— Use the minimum amount of Si per watt of PV power
— Use the best quality Si that would yield the highest solar cell efficiency
— Be the largest producer of PV energy
— Own the deepest pockets
— Receive the most government support.

Although each category by itself could be a winner for a multitude of reasons, the winning strategy might involve a combination of the above features. Also, because success of each category is contingent upon meeting a number of other processing conditions, predictions of success are not easy.

The rest of the discussion emphasized issues related to the quality of the material produced by existing crystal-growth techniques, and quality enhancement by cell-fabrication processing. Some of the issues are the following:

- Cell/module efficiency is a dominant criterion that determines the PV energy cost. For example, a growing market for cast mc-Si may be attributed to the fact that the efficiency of mc-Si is only a couple of percentage points below that of Czochralski (CZ) silicon, whereas the cost of mc-Si substrates is considerably lower.

- CZ solar cells have lifetimes in the range of 30-50 μs, and the mc-Si substrates have lifetimes of about 20 μs after gettering or cell fabrication. However, the efficiency of mc-Si cells is lower. A major reason for lower efficiency is an excessive shunting in mc-Si solar cells. It may be possible to further narrow the gap between the performance of CZ and mc-Si solar cells by developing processing to overcome shunting mechanisms.

- High-quality, boron-doped, CZ cells can have a starting minority-carrier lifetime at ~100 μs, but degrade to ~20-30 μs by light-induced degradation (LID). After LID, the lifetime in CZ and the best mc-Si is about the same. Perhaps CZ substrates should be high resistivity B-doped or doped with Ga.

- CZ cells are in the 18% efficiency range, but the wafer cost is ~50% of the module cost. Multicrystalline Si cells have efficiencies in the 15% range, with the wafer cost ~25%-30% of the module cost. Whereas mc-Si cell efficiencies need to be increased to ~18%, the cost of CZ wafers should be decreased to ~ 25% of module cost.

- Much progress has been made during the last decade in understanding point defects, and C, O, and metal impurities in Si. However, it appears the efficiency improvements are gradual (and not keeping up with the depth of understanding and knowledge). Perhaps not all Si solar cell manufacturers are using this knowledge to the fullest extent, because there is still some disparity in the efficiencies reached by various vendors of mc-Si. Some researchers feel that the current level of understanding of impurity gettering and passivation should allow formulation of a more or less universal process, which can yield a high-efficiency device on any commercial solar cell substrate. However, many feel that such a process is probably not feasible.

Session 3: Wafer Sawing and Future Wafer Techniques

Discussion Leaders: Steve Shea, BP Solar; and Keith Matthei, GT Solar Technolocies, Inc.

Wire sawing has been a major cost-reduction factor in Si solar cell technology. The current status of wire sawing allows wafer thickness of about 300 μm with a kerf loss of about 50 μm. However, further cost reduction requires improvements in a variety of areas of wire sawing. These include wire quality, abrasive quality, reuse of slurry, and system reliability.

- Abrasive recovery: For wire sawing to be an economical process, it is important to recover expensive items such as abrasive (SiC) and glycol.

- Minimizing wire breakage: Wire is also an expensive item, but appears to be quite durable, with only about one breakage in every 20 runs. Unfortunately, once the wire brakes, it cannot be recovered. Wire breakage typically occurs because of problems associated other parts of the saw, e.g., the pulley. Fortunately, upon occurrence of such an incident, most wafers are recoverable.

- Uniform particle size: It is desirable to have a uniform particle size of the abrasive in the slurry. But, SiC manufacturers produce them in a variety of sizes. It may be too expensive to have slurry with predominantly 10-μm SiC particle size.

Wire sawing is also becoming the primary method of wafering CZ Si for the integrated circuit (IC) industry. The total area used in solar cell fabrication has become equal to that used in IC fabrications during last year and is expected to surpass that of the IC usage in the near future. While the wafering cost may not be a concern for the IC industry, it is for the solar cell industry.

Session 5. Solar Cell Fabrication

Discussion Leaders: Ajeet Rohatgi, Georgia Institute of Technology; and Frank Schuurmans, Shell Solar Energy

The discussion opened by pointing out that a large number of cell design features and processing steps exist that can increase cell efficiency, but they are not currently incorporated in cell manufacturing for cost reasons. Most notably, very high-efficiency cells using high-quality wafers and advanced design/processing schemes incur a tremendous cost. The PV industry has the option of making solar cells that are either high efficiency/high cost or low efficiency/low cost. The majority of the manufacturers have adopted the latter option. The real research challenge is to increase the efficiency of low-cost cells without cost increases. That is, to use the ~20-μs lifetime wafers of mc-Si and boost the cell efficiency from 14%-15% to ~18% without using the presently available costly processing steps.

It may seem reasonable to optimize the existing manufacturing processes. However, this is quite difficult because the low-cost substrates used for solar cell manufacturing (even just for a single kind, e.g., EFG) have large variations in material properties, such as wafer thickness, resistivity, etc. Thus, intuitively, it might be desirable to narrow down the window of specification. But the industry has recently experienced the opposite trend — they were able to drive their net cost down by enlarging their spec-window (which resulted in decreasing the efficiency of some cells) to gain an overall increased productivity. Thus, no clear trend on this issue has emerged. It appears that a systematic study is needed to establish an acceptable window for various material properties. Opinions vary on whether university research should address more applied, manufacturing issues. Existing manufacturing lines may benefit from incremental improvements, and perhaps new production lines can take advantage of the high cell efficiency approach at a reasonable cost.

Other issues discussed were:

- A promising aspect is that a low-cost contact technology based on screen-printing with improved paste, etc., is seemingly making good progress (Europe) and could soon be implemented for cell efficiency improvement.

- Another current manufacturing issue is reduced yield due to wafer breakage, for which an understanding of some basic mechanisms is needed.

- A significant issue is that, in contrast to the IC industry, the PV industry does not have a well-accepted national or international roadmap[1] and there is no working group to pursue this effort. It appears that Europe is on the way to this goal, but with the tasks yet to be defined. The opinions are varied. On the one hand, there is the feeling that the time is right for such an attempt, but on the other hand it seems hard to accomplish, in view of the diversified materials

[1] In 2000, a working group comprising members of industry, universities, and the national laboratories published the U.S. Photovoltaic Industry Roadmap. This document is mentioned on page 13.

and applications involved. Nonetheless, it is probably valid to map a limited version in terms of the cell efficiency, cost, etc.

Session 6. Characterization/Shunting

Discussion Leaders: J. Werner, University of Stuttgart; and J. Szlufcik, IMEC

Recently there have been impressive developments in the areas of diagnosis and testing used in the PV industry. Automatic wafer handling has allowed standard measurements such as IV characterization of finished cells to be done at high speeds. At the same time, new tools and techniques allow measurement of a large number of material and cell parameters such as minority-carrier lifetime, shunts, and process-monitoring parameters such as antireflection (AR) coating thickness, and metallization. Many of these tools have the capability for fast, nondestructive testing suitable for on-line characterization. The question is, should these tools be used for on-line monitoring and for process control? If so, which parameters are important?

Typically, on-line monitoring is used for process development and yield enhancement. One important advantage of on-line monitoring is that it offers a capability for adaptive processing. The discussion broke into two camps on this issue. Some people believe that in-line measurement and adaptive processing of some sort (perhaps by batch) is important for future production lines, especially if you believe that solar cells need to be made on low-cost materials with the resulting large variations in material quality and parameters. Others believe that solar cell processing must be cheap and simple, and therefore a single robust process must exist in the line, and the material must be made to conform to parameters suitable for this process.

Currently, there is little or no wafer-tracking through processes, so adaptive processing based on measured parameters for each wafer is not feasible. Could wafers be sorted and batched, then processed in batches with optimized parameters? Several cases where this could be advantageous were discussed.

In general, there is no consensus on which parameters are the most important, or where and when to measure them. Although industry is using minority-carrier lifetime measurement as a qualifying test prior to sawing, some think the data do not correlate directly to cell efficiency. In the mid-1990s, lifetime round robins often showed poor correlation in lifetime measurements between labs, and also had poor predictive qualities for solar cell results. However, more recent laboratory studies have shown that lifetime measurements after phosphorus diffusion are very well correlated to final cell efficiencies. It was generally agreed that the parameters to be monitored should include lifetime, its variation and distribution, wafer position and ingot history, and wafer resistivity and its distribution. In addition to sorting by lifetime, it was pointed out that the actual temperature of a wafer in a belt furnace is a strong function of the wafer thickness. So the optimum set temperatures during paste-firing is different for different thicknesses of wafers. Is it worth measuring the wafer thickness for each wafer if this information is not subsequently used to optimize the firing? Similarly, is it worthwhile to monitor the results of firing in detail for each wafer if this is, in effect, just an indirect measurement of the wide distribution in the wafer thickness?

It appears that the hard shunt problems, caused by improper kerf isolation and by contact formation processes, have already been solved by process modifications. What is still unsolved are the bulk material shunts, which are strong recombination centers due to crystalline defects and metal impurity contaminations or can lead to an inversion layer. There is a need to continue to study materials defects, process-induced defects, and their interactions.

The topic then moved on to a discussion of whether the new tools are best used for episodic problem-solving or for in-line continuous process control and optimization. Are these best addressed by detailed studies to occasionally assess and "fix" process equipment and process parameters, or should there be continuous in-line monitoring of these parameters? This issue went unresolved.

There is the interesting suggestion a diagnosing/monitoring facility that could be "rented," which would serve to identify a problem and redesign a process. It will be interesting to see which of the new characterization techniques industry develops or picks up, and how they are applied in the near future. The criteria may be as simple as whether or not a tool is proven to be certain to pay for itself in improved efficiency or yield in such a short time as to become an obvious good purchase. Because many new silicon lines are now in the planning stage or the early stage of production, this seems like a good opportunity to introduce a new generation of measurement tools.

Session 8: Hydrogen Passivation and Processing

Discussion Leaders: Jack Hanoka, Evergreen Solar, Inc.; and Bob McConnell, National Renewable Energy Laboratory

The discussion was directed into three areas:

1. What we know and how is it done.
2. What we do not know.
3. What we would like to know.

What we know and how is it done

There is an increasing trend in the PV industry to perform impurity and defect passivation through a process that combines AR coating, metallization firing, and hydrogenation. The passivation process is a two-step process. First, about ~800 Å of SiN is deposited on the cell by a PECVD process using SiH_4 and NH_3. Then a metallic contact is screen-printed and fired through the nitride. This process results in indiffusion of H. Because a PECVD process involves energetic ionized species, a certain degree of damage is introduced at the surface of the cell. The damaged surface layer is believed to retain the majority of H. This layer acts as a source of H that is driven into the cell in a subsequent metallization firing step. There is some evidence that remote plasma hydrogenation is not as effective as the PECVD process, lending support to the need for a damaged layer.

- The hydrogenation process steps are empirically optimized by each vendor. RTP processing with rapid cooling has yielded cell efficiencies of 15.9% for EFG and 15.6% for string ribbon.

- The process works on ribbon, cast poly, RGS (high [O] slows it down) and Silicon Film (AstroPower).

- Earlier experience: poorer material – larger improvement in cell efficiency; better material – smaller improvement in the cell efficiency.

- Decorated dislocations are passivated.

- The process optimization appears to ensure that sufficient H diffuses into the cell while preventing out diffusion of H. It is believed that the Al back contact serves as a capping layer. Likewise SiN layer may prevent out-diffusion of H.

- Commercial PECVD systems are based on both tube machines (boats) and horizontal (~ in-line) machines (trays). There are some issues with commercial systems:

  - SiN deposition where you don't want it – on boats, trays, and/or inside of machine
  - Cost and throughput.

- Newer approaches for deposition of SiN suitable for passivation are being investigated. These include:

  - Expanding thermal plasma suitable for very high throughput
  - Reactive sputtering, potentially high throughput, lower capital cost
  - Hot-wire plasma.

What we don't know and would like to know

What defects are passivated?
Which decorated metals actually do passivate - silicides, oxides, carbides, silicates?
How much H actually gets in the Si?
How to get H to the "bad" defects and keep it there? (Debonding starts at 350°C)
What is the ultimate capability of hydrogen passivation? How much of a magic bullet is it?

Session: Wrap-Up
Discussion Leader: Dick Swanson, SunPower Corporation

This year, the wrap-up session that traditionally summarized highlights and identified research issued was changed to develop a roadmap for wafered Si using the input from the workshop attendees.

The Wafered Silicon Roadmap

It is often said that the biggest problem facing wafered silicon PV is the wafer. The implied conclusion is: If it were not for the wafer, wafered silicon modules would be quite cost effective given their high performance and reliability. The problem with the wafer is that it uses large amounts of expensive starting material, requires an expensive casting or ingot growth process, and must be sawn into wafers despite the fact it is a very hard and brittle material. Tough issues indeed. Rather than dismissing out of hand wafered silicon as a viable long-term candidate, however, this begs the question: "How expensive is the wafer, what sort of price reduction can be expected over time, and what is the impact of the wafer cost on overall system cost?" We took advantage of the unique assembly of silicon PV experts from around the world who gathered for this workshop to shed some light on these issues. The results of this activity are presented below.

Methodology

Most cost studies done in the past involved assembling a group of experts who conferred, did calculations, canvassed other experts, came to consensus, and wrote their results. On the contrary, this analysis is based on the notion that independent averaging of the opinions of a large number of experts is a powerful way of accurately extracting information that is buried in noise and uncertainty. The averaging technique diminishes the impact of overly conservative and overly optimistic participants. The secret ballot form of gathering information minimizes the impact of persuasive individuals, allows participants to express their views anonymously without regard to employers or funding agencies, and prevents collusion. Forms were distributed that asked participants to state their opinion on each of eight factors that will impact wafer cost for the years from 2002 to 2012. The factors are: poly silicon cost, ingot growth cost, poly to ingot material yield, wafer thickness, kerf loss, sawing cost, saw yield, and cell efficiency. Participants were asked to make their assessment for either cast multi-crystalline silicon (mc-Si) or Czochralksi-grown, single-crystalline silicon (CZ-Si). The results are tabulated in Attachment A. Data to the left of the double line are averaged input data, and data to the right are calculated from these results. Fifteen participants supplied data for mc-Si and eight for CZ-Si.

In forming their responses, participants were asked to assume that the PV market grows at a rate of 23% per year over the next decade. This results in an eightfold increase in production volume by 2012. It is also assumed that each of the factors listed is subject to continual R&D to drive down costs. In other words, this is a roadmap that could be realized, given that the industry continues on its present robust course.

The costs are intended to be manufacturing cost (cost of goods sold in U.S. finance terms). These include all factory overhead, but specifically do not include R&D, marketing and sales, general and administrative costs, or profit.

Input Results

The following sections discuss the input data obtained from the study.

(A) Polycrystalline Silicon Cost

Poly silicon is expected to experience a modest decline of around 25% in price over the next 10 years. This reflects the impact of poly production facilities dedicated to the production of "solar grade" silicon. Alternatively, the mainstream suppliers to the microelectronics industry may engender such reductions through the normal course of business. After all, poly costs have decreased tenfold over the period 1975 to the present, from $300/kg (in current dollars) to the $30/kg. Figure 1 shows the projection. It is seen that CZ-Si growers are expecting to use slightly more expensive silicon.

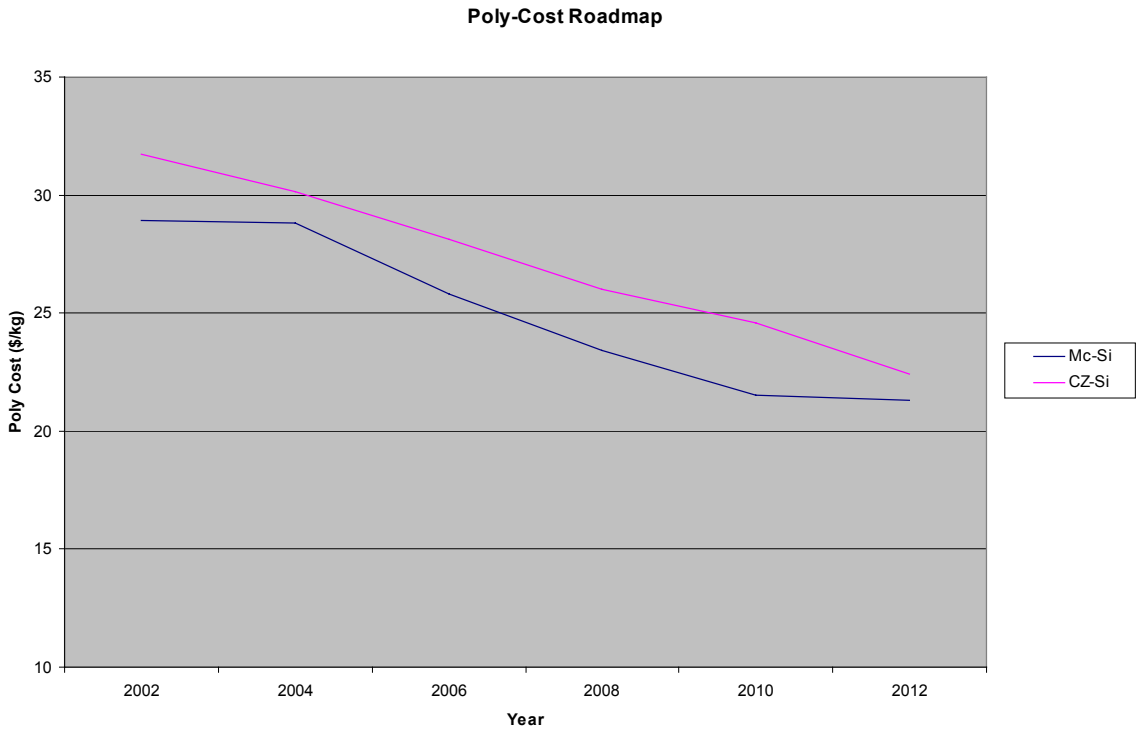

Figure 1. Poly-Cost Roadmap

(B) Ingot Growth

Ingot growth is expected to decrease in cost by about 35% over the period, about a 4% per year decrease. CZ growth is about $10/kg more expensive than casting at present, although the difference decreases to $6/kg by 2012.

(C) Poly-to-Ingot Material Yield

This is a critical factor because current yields are rather low. In casting, the top, bottom, and side regions must be removed from the grown ingot. In CZ, the tops and tails of the ingot are removed and there is pot scrap left in the ingot following growth. Continuous recharge can reduce these losses. Yields are expected to improve from the present 70% to around 80% during the next 10 years.

(D) Wafer Thickness

Wafer thicknesses are decreasing, and will continue to do so. Figure 2 shows the consensus projection. Interestingly, the wafer thicknesses projected for CZ-Si are considerably less than mc-Si. This could reflect the more fragile nature of cast material, or perhaps CZ workers are more aggressive in their projections. Because cast material is less expensive than CZ, the impact of reduced wafer thickness for cast material is less than for CZ.

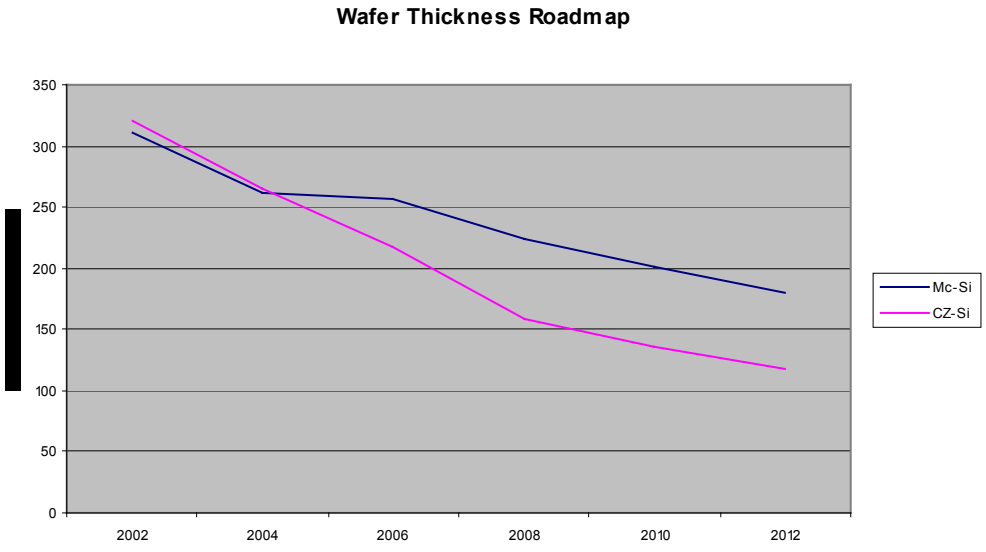

Figure 2. Wafer thickness roadmap

(E) Kerf Loss

Kerf loss is expected to continue to decline, from the current 190 micrometers to 130 micrometers for mc-Si and to 70 micrometers for CZ-Si. Once again, the CZ community is much more bullish on the prospects for reduction. Clearly, they are counting on some replacement for wire saws, such as laser-assisted cutting.

(F) Saw Cost and Yield

Saw cost has been dropping rapidly over the recent period due to developments such as slurry recycling and the introduction of new generations of more productive machines. Costs are expected to drop from the current $0.55 per wafer to around $0.35 per wafer over the next decade. This is a 4% per year drop. Saw yields will benefit from typical learning effects and improve from the current 89% to around 93%.

(G) Cell Efficiency

Cell efficiencies will continue to improve with the introduction of new processes and designs, plus improvements in screen-printing, hydrogenation, and similar processes. Figure 3 shows the consensus projection. CZ cells have an advantage of about two percentage points; however, half this advantage is lost due to the larger coverage fraction of the square cast wafers as opposed to the semi-square CZ wafers. Efficiencies will increase to 18% for mc-Si and 20% for CZ-Si. This seems very reasonable, given recent laboratory results.

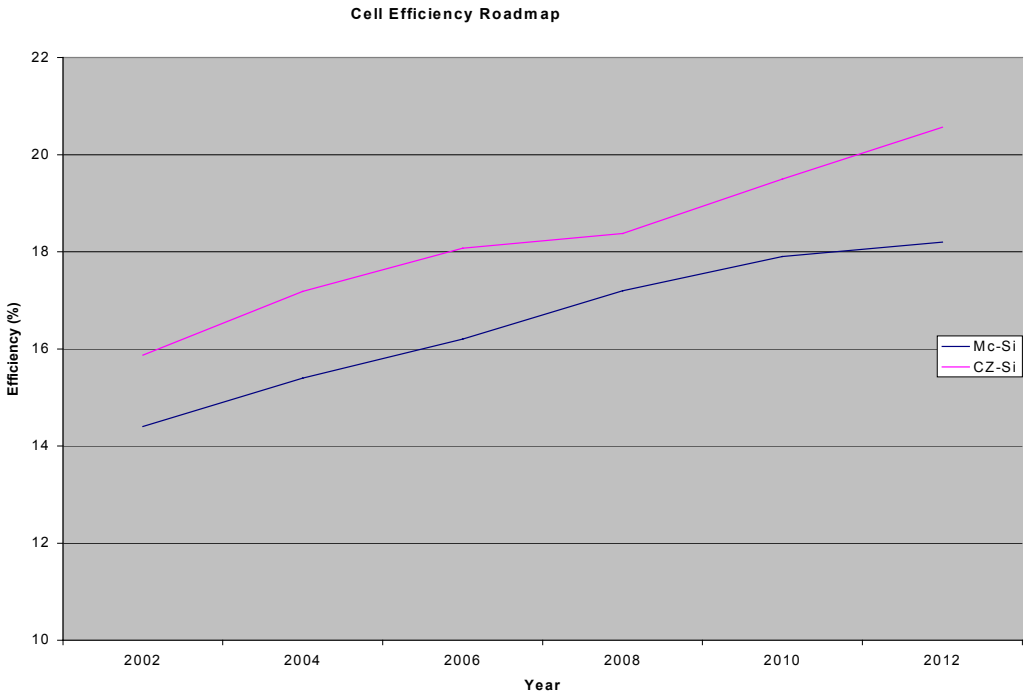

Figure 3. Cell efficiency roadmap

Output Results

In this section, the input results are analyzed to see what overall costs they project.

(A) Wafer Cost

The wafer cost computed is shown in Figure 4. Note that the wafer is 12.5 cm by 12.5 cm square for mc-Si, whereas it is 12.5 cm semi-square for CZ. Interestingly, the cost of CZ wafers is projected to become less than mc-Si in around 8 years. This is clearly a result of the aggressive kerf loss projections. In Appendix B, the CZ-Si results are recomputed using the kerf loss projections for mc-Si. It can be seen that this erases any significant difference between mc-Si and CZ-Si in terms of system and module costs. In fact, it should not be supposed that the accuracy of this study is sufficient to resolve any residual cost difference between mc-Si and CZ-Si, but rather to indicate the approximated long-range potential of wafered silicon PV in general.

(B) Module and System Costs

To compute module and system costs, it is necessary to assume some cost for cell processing, module lamination, and balance of system (BOS) costs. To get some idea of these factors, it was assumed that cell processing currently costs $\$80/m^2$ (referenced to module area), lamination costs $\$120/m^2$, and the BOS costs $\$200/m^2$. Although not exact, these numbers probably represent the approximate state of the art. For projecting into the future, these numbers were arbitrarily assumed to decrease 4% per year. This results in a decrease in 33% for the non-wafer costs during the next decade. Interestingly, the wafer cost decreases 60% during this period due to the various process improvements projected. Such might be expected, as the wafer is the new, high-tech portion of the product, whereas the remainder of the components use rather normal construction materials. As we shall see, this difference has significant impact on the competitiveness of alternatives to wafered silicon, such as thin-film and concentrator approaches.

Figure 5 shows the projected module costs and Figure 6 the projected system costs. Once again, no significance should be attributed to the difference in mc-Si and CZ-Si costs. Figure 6 shows the DC system costs. Here the BOS assumption is that appropriate for larger, stand-alone installations. Module manufacturing costs decrease from about $2.70/W at present to $1.00/W in 10 years. This significant decrease is driven largely by decreases in wafer thickness and increases in cell efficiency. The remaining factors all have rather low cost reductions of around 4% per year, corresponding to a 10% learning curve (10% cost reduction for each doubling of cumulative production) under the assumed 25% per year growth. Such a low number is below most industrial product learning curves rates, and is likely conservative. Interestingly, the module cost projection has about a 20% learning curve, which is actually the historical average.[2]

[2] We have used the fact here that for exponential growth, the cost as a function of production rate decreases at the same rate as the cost as a function of cumulative volume (the integral of an exponential is an exponential with the same time constant).

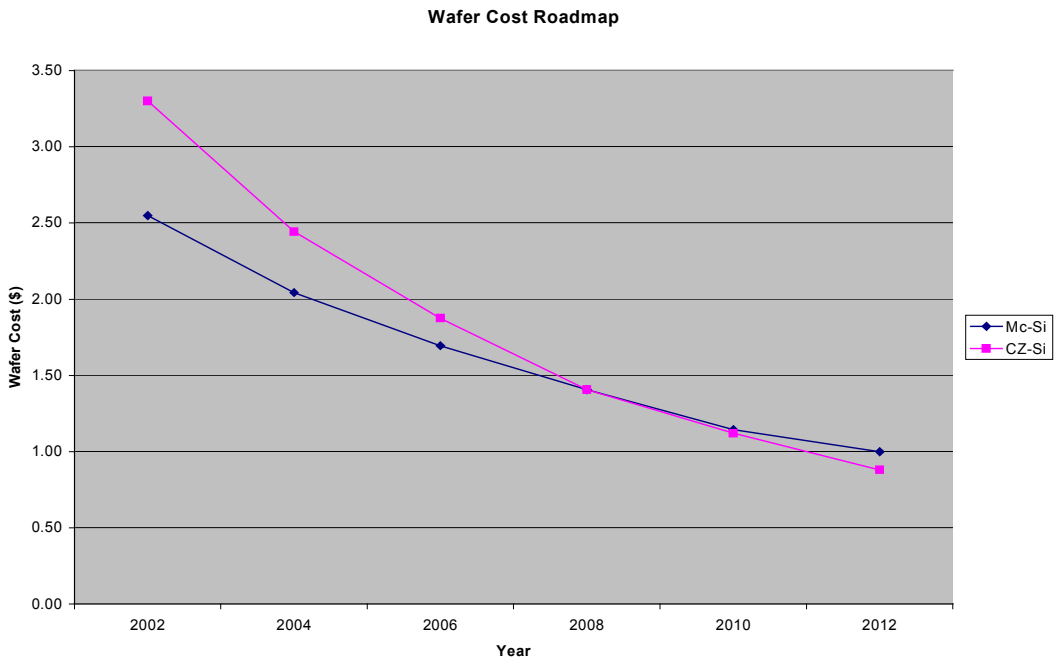

Figure 4. Wafer cost roadmap

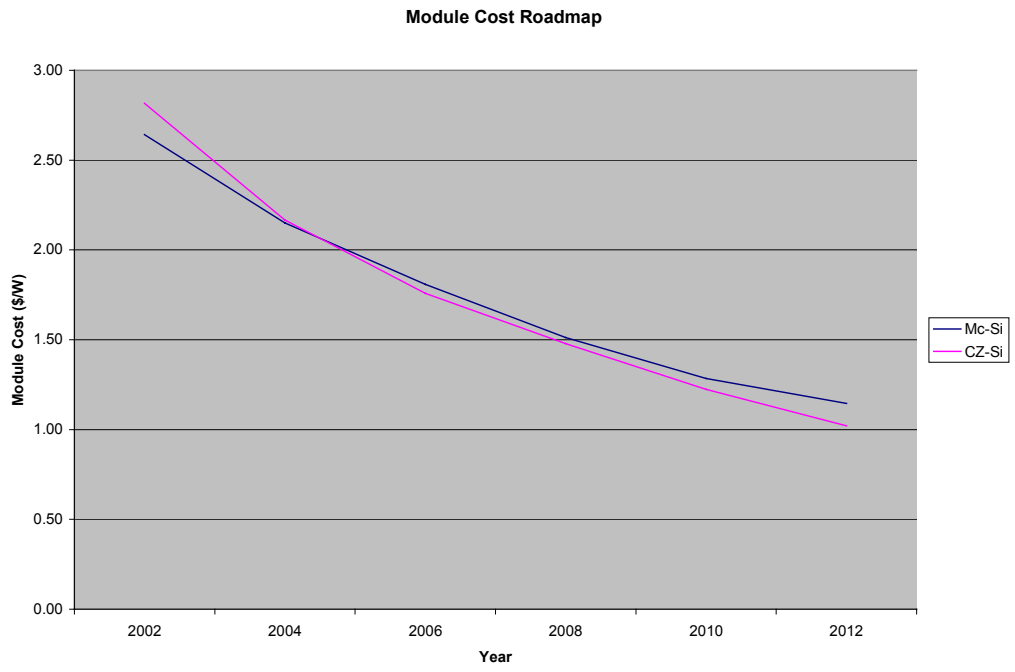

Figure 5. Module cost roadmap

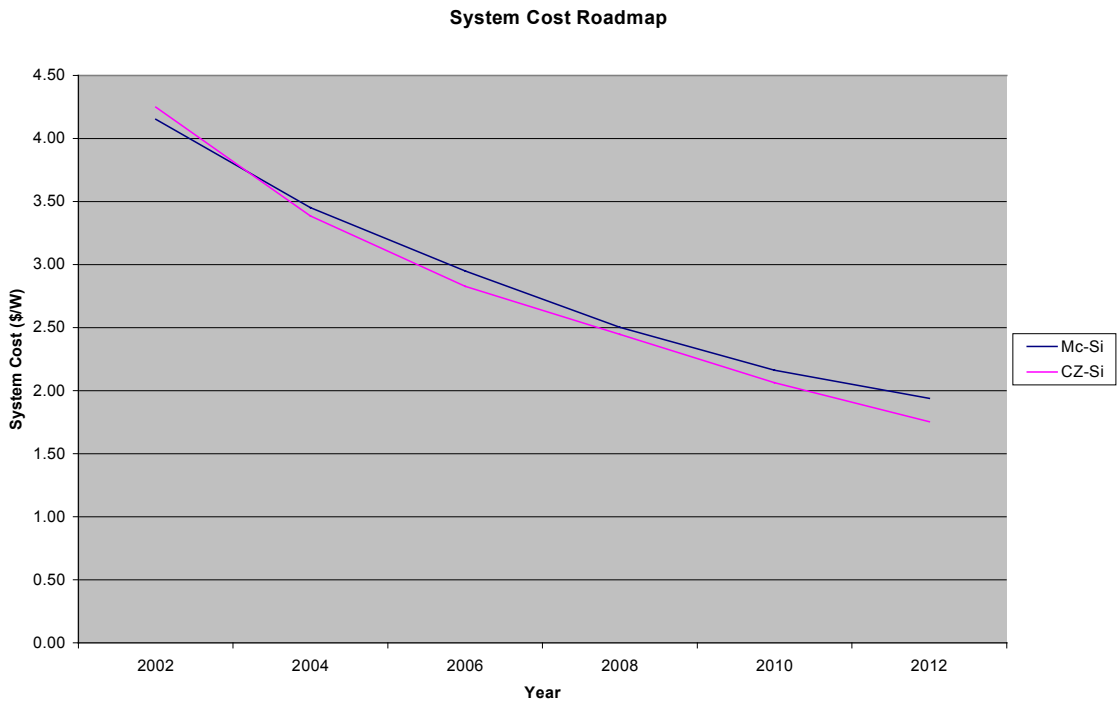

Figure 6. System cost roadmap

(C) System Sales Price

In order to compare the above with other projections of sales prices, Figure 7 shows the projected system price. A gross margin of 35% is assumed for the sale. Such a margin is reasonable in for a high-volume manufacturing enterprise; for example, 5% R&D, 5% sales and marketing, 10% G&A, and 15% pretax profit. This rather low margin does not provide much in the way of excess capital for capacity investment. It is also the overall value chain margin (exclusive of poly cost, which is an assumed input material). Different components of the value chain will probably command different margins. Interestingly, the result is only slightly greater than the U. S. PV Industry Roadmap, which predicts system sales prices of $3/W in 2010. System prices of $3.00/W are expected to open large, unsubsidized markets for point-of-use power generation. This will be necessary, of course, to support the two plus gigawatt per year market that the above assumptions imply.

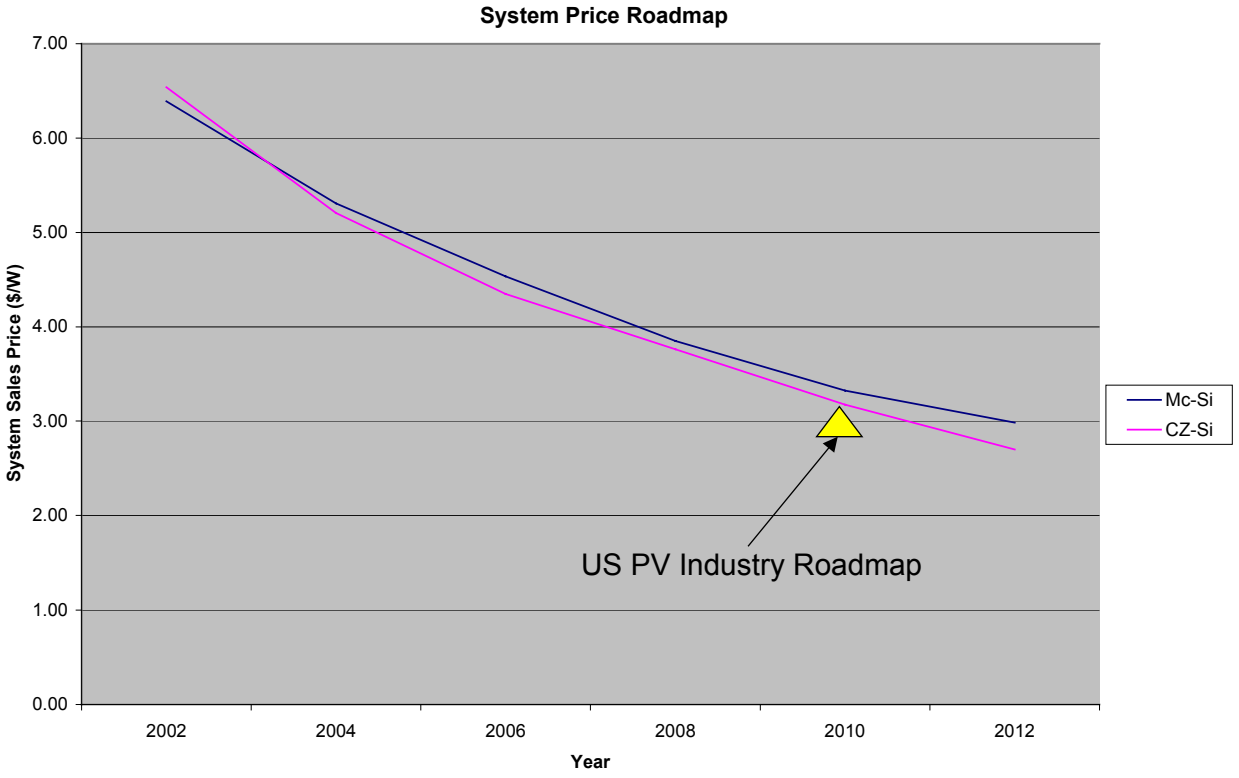

Figure 7. System price roadmap

Implications for Thin-Film PV

Independent projections are often made for competing technologies that are hard to compare because different assumptions are made for each technology. These results offer an interesting opportunity to compare thin-film and wafered silicon. If one assumes that the cost of making a thin film cell is equal to, or more expensive than, processing a silicon wafer into a cell, then a lower bound on thin-film cost is obtained from the above by simply setting the wafer cost to zero. Is this a reasonable assumption? It seems likely in that the processes for wafered silicon are all quite inexpensive—diffusion, screen-printing, and the like. As far as lamination is concerned, thin-film modules use about the same amount of materials as wafered silicon. The only difference is in the stringing operation, but this has become quite automated and is done a very low cost. In fact, it might be considered that wafered silicon has an advantage in that cells can be rejected prior to stringing, whereas in thin-film modules, the whole module must be rejected if it has a bad cell. In any case, the above assumption can be used to compute the minimum module efficiency that a thin-film module must have to compete with the wafered silicon projection to achieve the same system prince. This is shown in Figure 8. It is seen that the required efficiency today is around 10%, and this must increase to 15% over the next decade. Although these efficiencies are in line with various projections, they are substantially higher than what is commercially available today. It must be remembered, also, that these are the minimum

required efficiencies for cost parity. Normally, a considerable advantage must accrue to a new technology before it can displace the incumbent (wafered silicon in this case).

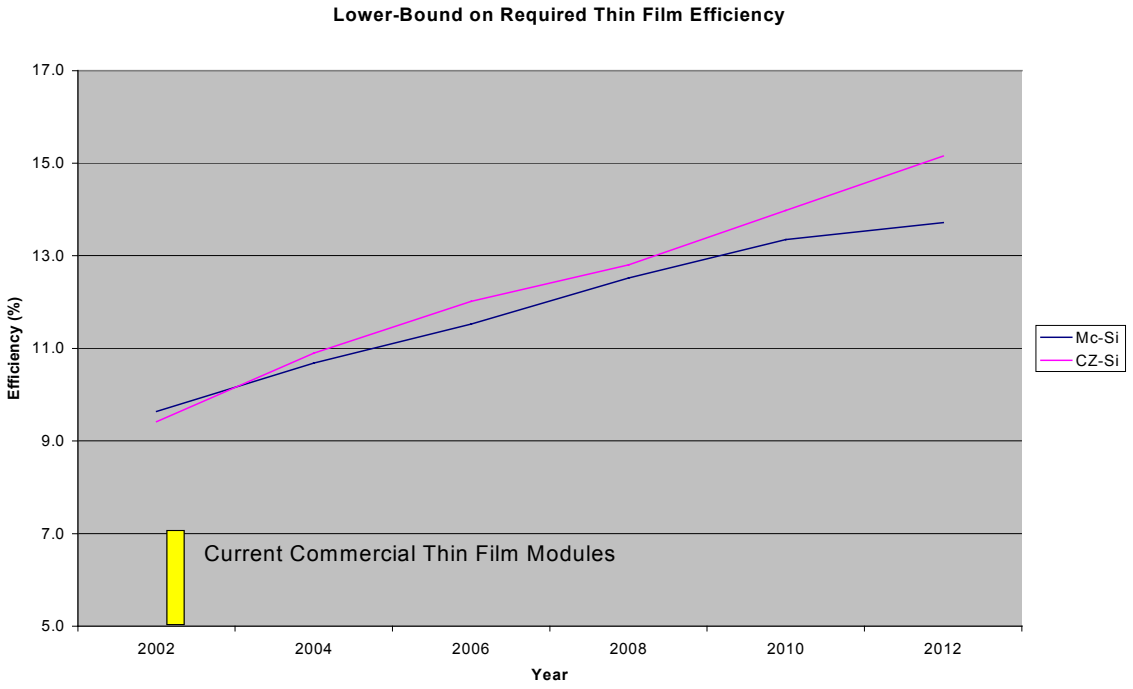

Figure 8. Required thin-film efficiency to compete with wafered silicon modules.

Conclusions

The cost projections of this study are consistent with wafered silicon PV achieving the cost goals of $3.00/W by 2010, which should establish PV as a very cost-competitive distributed energy source for many applications. If the same rate-of-learning is assumed, cost reduction can be continued for another 10 years, the system price will be below $1.50/W, and PV will be able to compete directly with fossil fuel sources of electric power in 2022. This would require that PV be manufactured at a rate of about 35 GW per year at that time. So we see that not only will the costs be competitive as a primary source of energy, but industry will be poised with significant volume capacity so that it will begin to play a truly significant energy role. The timing is auspicious, because fossil fuels are projected be undergoing significant price increases due to supply and demand issues at about this time.

The PV industry should set goals for all the factors relating to wafer cost, and track these over time to insure that we are staying on track to meet roadmap goals. In addition, sponsored R&D in all critical areas common to all participants should be encouraged. These include poly cost, sawing, etc. In reviewing the numbers, it becomes apparent that the lamination and BOS costs

are already the largest cost elements, and that this will become more so in the future. Clearly, a concerted effort at new lamination and BOS technologies and concepts is highly warranted. Unfortunately, most R&D effort has gone into wafer and cell manufacturing. Improvements in lamination and BOS at a rate faster than the assumed 10% learning curve reduction would make thin films relatively more attractive than the current cost analysis projects, and reduce the projected prices for all technologies dramatically. Therefore, the entire industry should mobilize to promote R&D in these areas.

As the incumbent technology, wafered silicon PV will continue to dominate the market based on its ever-decreasing costs. This will likely make it difficult for either thin-film or concentrator approaches to garner significant market share in the next decade. Things are less certain in the following decade: 20% thin-film modules, 40% concentrator cells, and other disruptive developments may provide an opportunity for competing approaches, but even this may be difficult if the cost reductions in wafered PV can continue. Note that the projected wafer cost of \$50 to \$60/m^2, or \$0.30 to \$0.35 per watt, in 2012 is already sufficient to meet the 2022 system price goal of \$1.50 per watt, providing that lamination and BOS costs are sufficiently reduced. Wafered silicon PV has enjoyed recent dramatic growth, emerging as a viable industry. It appears that this momentum will continue for the foreseeable future.

Program Committee

Juris Kalejs, Jim Rand, Tadashi Saitoh, Ron Sinton, Michael Stavola, Dick Swanson, Teh Tan, Eicke Weber, Juergen Werner, Bhushan Sopori, Mowafak Al-Jassim (Invited Member)

NREL Administrative and Workshop Support

Sandy Padilla, Monica Forest, and Irene Passage

NREL Conference Services Support

Sara Huntley

Acknowledgements

A special note of appreciation goes to the following companies for their contribution to the Graduate Student Awards:

AstroPower, Inc., BP Solar, Crystal Systems, EBARA Solar, Inc., Evergreen Solar, Shell Solar, GT Equipment, NPC America Corporation, and Sinton Consulting

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE February 2003	3. REPORT TYPE AND DATES COVERED Workshop--Conferences Proceedings 11-14 August 2002, Breckenridge, Colorado
4. TITLE AND SUBTITLE 12th Workshop on Crystalline Silicon Solar Cell Materials and Processes: Summary Discussion Sessions; 11-14 August 2002, Breckenridge, Colorado		5. FUNDING NUMBERS PVP33101
6. AUTHOR(S) B. Sopori, D. Swanson, R. Sinton, and T. Tan		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)		8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393		10. SPONSORING/MONITORING AGENCY REPORT NUMBER NREL/CP-520-33435
11. SUPPLEMENTARY NOTES		
12a. DISTRIBUTION/AVAILABILITY STATEMENT National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161		12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words):* This report is a summary of the discussion sessions of the 12th Workshop on Crystalline Silicon Solar Cells and Processes. The theme of the workshop was "Fundamental R&D in c-Si: Enabling Progress in Solar-Electric Technology." This theme was chosen to reflect a concern that the current expansion in the PV energy production may redirect basic research efforts to production-oriented issues. The PV industry is installing added production capacity and new production lines that include the latest technologies. Once the technologies are selected, it is difficult to make changes. Consequently, a large expansion can stagnate the technologies and diminish interest in fundamental research. To prevent the fundamental R&D program from being overwhelmed by the desire to address immediate engineering issues, there is a need to establish topics of fundamental nature that can be pursued by the universities and the research institutions. Hence, one of the objectives of the workshop was to identify such areas for fundamental research.

14. SUBJECT TERMS: PV; crystalline silicon, solar cells; materials and processes; feedstocks; impurities and defects; passivation			15. NUMBER OF PAGES 16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102