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Office of Energy Efficiency & Renewable Energy

NREL National Renewable Energy Laboratory

Innovation for Our Energy Future

Proceedings of The 19th National CdTe R&D Team Meeting

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Thin Film Photovoltaics Partnership Program

National Center for Photovoltaics

NREL Visitors Center • Golden, Colorado • March 9-10, 2006

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National CdTe R&D Team Meeting Notes
Golden, Colorado
March 9-10, 2006
Prepared by Peter V. Meyers

1.0 INTRODUCTION

1.1 Harin Ullal, NREL, opened the meeting by greeting participants and presenting an overview of recent events related to PV, thin film, and CdTe PV. (The meeting **agenda** and **list of Team members** are attached) DOE's PV budget for 2006 is $71 M; $10.8 M was "earmarked" for special projects. Worldwide production of PV in 2005 was 1727 MW. Thin film PV manufacturing in the US continues to grow, exceeding 40 MW in 2005; predicted 2008 production exceeds 170 MW/yr. If one considers only US owned companies, thin film PV module production exceeded X-Si module production in 2005! Harin also pointed participants toward information on the Solar America Initiative (SAI) and Notice of Program Intent (NOPI). A meeting is scheduled in Chicago, IL; April 18-19, 2006 for inputs from the various stakeholders.

2.0 INDUSTRY OVERVIEWS

2.1 Peter Meyers, First Solar, provided a brief overview of recent First Solar activities. Production and sale of thin film CdTe PV modules exceeded 20 MW in 2005; most product went to Germany. The 50 MW manufacturing expansion begun in May 2005 continues and first modules from the new lines are expected to be produced in the first half of 2006. First Solar now employs 350 people in Ohio, Arizona and Germany. As of last month manufacturing is 24/7; 11,000 modules were produced in a single week. Peter also reviewed First Solar's comprehensive environmental, health and safety program which includes a prepaid module return program at the end of module useful life.

2.2 Kurt Barth, AVA and CSU, presented **"Brief update of progress at AVA Technologies LLC"**. Kurt stated that a CSU VP described the AVA-CSU relationship as a model for effective university-industry partnerships. Production equipment is being built to produce modules on 16.5" X 16.5" substrates with plans to scale to 60 cm X 120 cm. Emphasis is on process control of a) temperature, b) ambient and c) flux. Deposition equipment is in place and a successful 78 hour thermal trial run has been completed. Back contact electrodes are produced by screen printing or spraying Ni on carbon pastes supplied by Acheson. Line widths of 0.1 mm have been achieved. Cell interconnection is achieved through a) laser scribe of TCO, mechanical scribing for the via, and screen printing of Ni/C back electrode. Cost estimates based on 20 MW/yr production indicate direct costs <$1/W; equipment capital costs are $10 M (does not include building). AVA is looking for a partner to take it to the "third stage" of it's plan – initial production.

2.3 Nick Dalacu, CANROM, was not able to attend but he sent word that development is going well and he has plans to further expand his business.

3.0 DEVICE PHYSICS

3.1 Victor Karpov, UT, opened the Device Physics portion of the program.

3.2 Brian McCandless, IEC, presented **"Characterization of CdTe devices with a transparent ZnTe:Cu contact"**. Devices were fabricated with the structure: TEC15/CdS/CdTe/Interfacial layer (IFL)/ZnTe(Cu)/ITO/grid where ZnTe(Cu) was deposited galvanically and triethanolamine (TEA) was used to regulate Cu concentration. Illumination through the rear electrode eliminated the blocking barrier effect of BrMe-etched back contacts. Log Jsc vs Voc plots including illumination from both front and rear fall on a single line indicating that a single junction determines Voc. The fact that front surface illumination produces higher QE at λ=830 nm than does back surface illumination is attributed to the reduced absorption coefficient of the CdTe-S alloy (compared to that of CdTe) that occurs only at the CdS/CdTe interface. C-V analysis agrees with the IEC interpretation of front/rear QE curves. Stressed devices show rollover with front, but not back, surface illumination indicating that stress is affecting the back contact region.

3.3 Tim Gessert, NREL, presented **"Analysis of identical ZnTe:Cu/Ti contacts fabricated onto various CdS/CdTe device materials"**. Light and dark IV, CV, and SIMS depth profiles of CdTe/CdS films from various sources were analyzed and results compared to SCAPS simulations. Under optimum conditions (contact deposition at 320 C) devices had peak Voc ~820 mV and N_A ~2 x 10^{13} cm^{-3}. Back contact barriers were eliminated and current transport was by tunneling between ZnTe:Cu and Ti. Cu concentration in CdTe and CdS and reaction of Ti with ZnTe all increased with process temperature. SCAPS simulations matching experimental data confirm the CdTe acceptor concentration and indicate N_D~1 x 10^{17} cm^{-3} in CdS.

3.4 Diana Shvydka, UT, presented **"Piezo-effect in CdS-based solar cells"**. Diana described studies in which CdTe/CdS and CIGS/CdS thin films were subjected to normal pressure and lateral compressive strain. Independent of direction of stress, Voc decreased and Jsc increased in CdTe devices, while for CIGS devices both Voc and Jsc decreased. Effects of pressure were largely reversible; permanent changes were attributed to physical damage. Piezo-electric effects in the CdS were identified as the most probable explanation. In additional studies CdTe/CdS devices were processed with electrical bias during a chloride heat treatment (CHT). Best results were obtained at forward bias but other effects are suspected to have also played roles.

3.5 Ramesh Dhere, NREL, presented **"Study of CdS/CdTe junction by modulated reflectance"**. Photo- and electro-reflectance data from CdTe/CdS solar cells were fitted to a model indicating an electric field of 32-35 kV/cm in Te-rich CdSTe alloys of high efficiency devices. Ramesh used ebic data to support a model in which Voc of high efficiency devices (840-850 mV Voc) is attributed to an n^+ Cl-doped Te-rich cubic CdTeS alloy junction to p-type CdTe. The role of CdS it not primarily as a heterojunction partner; rather CdS serves primarily to produce the Te-rich, n^+ CdTeS alloy.

3.6 Alan Fahrenbruch, ALF/CSU, presented **"Photoconductive CdS and anomalous AQE effects: comparison of experiment and modeling"**. CdS is modeled as a fully depleted layer with a total acceptor concentration of 2 X 10^{16} cm^{-3} and a donor concentration of 7 X 10^{15} cm^{-3}, however due to the complete depletion, characterization as "n" or "p" does not apply. Illumination increases the net positive charge and enhances junction current; the "photoconductive"

effect of CdS is more aptly labeled "photo-gating". In experimental investigations using high intensity blue and red LED's, Alan showed how photo-induced transients in forward biased devices could produce negative apparent quantum efficiencies (AQE) with both blue and red light. The direct current (DC) method of measuring AQE provides more reliable and meaningful data than does the more conventional lock in amplifier (LIA) QE measurement.

3.7 Wyatt Metzger, NREL, presented **"Measuring recombination in CdTe solar cells"**. Wyatt described the measurement equipment and interpretation of time-resolved photoluminescence (TRPL) data. TRPL measures the lifetime of the photo-induced excess carrier concentration; not just the radiative lifetime. For CdTe radiative lifetime is on the order of 0.1% of the total lifetime; measured lifetime is Shockley-Reed-Hall (SRH) lifetime. As transit time across a typical CdTe depletion region is ~100 ps, TRPL lifetime is not a good indicator of photocurrent collection. As Voc is proportional to $\ln[Jsc/J_0]$, where J_0 is the reverse diode saturation current, and J_0 is proportional to τ_{PL}, where τ_{PL} is the photoluminescence lifetime, therefore Voc varies as $\ln[\tau_{PL}]$. Naturally many factors contribute to Voc, but in order to avoid lifetime limiting of Voc requires lifetimes greater than 2 ns.

3.8 Victor Karpov, UT, presented **"Indicative facts and device model"**. Victor listed several "indicative facts" along with their possible implications with respect to a model of device operation. Victor argues that these indicative facts can be explained with a "reverse field model" in which the electric field in the CdS is opposite to that in the CdTe. He presented an analytical solution that describes device performance using the reverse field model. Further Victor argues that the recombination lifetime is much longer than the drift time (that time required for a carrier to transit through the depletion region) and that therefore SRH recombination has negligible impact on device performance. Device performance is determined by non-uniform recombination characterized by weak diodes.

3.9 Jim Sites, CSU, presented **"Impact of lifetime and back-contact barrier on CdTe current-voltage curves: Simulation of commonly seen features"**. Jim described a conventional device model and explored effects of variation of carrier lifetime and back contact barrier height. Considering variations in carrier lifetime from 0.005 to 50 ns (0.5 ns corresponds to 16.5% cell) and back barrier height from 0.3 to 0.7 eV, Jim was able to simulate a) variation of FF, b) rollover, c) crossover and d) low Voc. Jim argues that there is no need for non-standard models and that non-uniformity is not a limiting factor in the best cells.

A short discussion of device modeling followed the formal presentations.

Victor Karpov asked whether we should give greater emphasis to discussion of qualitative models.

Alan Fahrenbruch commented that in his models ~2 mA/cm^2 of Jsc originates in the CdS. Alan also noted that above Vmp most current is lost due to recombination at the back contact.

Fred Seymour stated that in his simulations a surface recombination velocity $<10^4$ cm/s results in Voc ~ 1V.

Peter Meyers asked whether separating FF into Vmp/Voc and Jmp/Jsc provided useful information. Alan Fahrenbruch commented that while some useful information might be obtained, it is better to have the complete I-V curve.

4.0 STABILITY

4.1 Dave Albin, NREL, introduced the Stability subteam session by presenting **"Modes and Mechanisms – an Update"**. Dave briefly summarized device-related aspects of the Accelerated Aging Testing in Photovoltaics Meeting held Feb. 22-23 in Maryland. Industry and DOE are increasing interested in quantifying PV device stability and reliability and treat these as "fundamental" research areas. Modes of failure during IEC and IEEE qualification testing differ significantly between wafer Si and thin film PV modules. At the conference the Device Stability breakout group identified several key areas that will promote improving and quantifying device stability.

4.2 Alan Davies, CSU, presented **"Effects of Cu and $CdCl_2$ on stability and uniformity of CdTe solar cells"**. Alan monitored I-V and light beam induced current (LBIC) uniformity of CSU-produced devices with and without Cu and with "poor" and "good" CHT and stressed them at 65 C OC with a 5 hr on; 3 hr off illumination cycle. Pre-stress performance of Cu-treated devices had higher FF and efficiency and better LBIC uniformity than devices processed without Cu. Stressing reduced performance and uniformity of all tested devices, but Cu-containing devices were more robust. "Good" CHT also provided a significant improvement in stability that was attributed to minimization of lifetime reduction due to Cu diffusion.

After the talk Kurt Barth, CSU, stated that there is a small amount of Cu diffusion due to stress. In response to a question, Jim Sites, CSU, speculated that Cu enhances uniformity because variations in high back contact barriers are manifested by larger variations in device performance compared to variation in device performance due to similar variations in low back contact barriers.

4.3 Chris Ferekides, USF, presented **"Stability studies of CdTe devices: Cu in back contact vs. Cu in CdS"**. When devices are stressed at OC, the amount of dark series resistance increase and Voc decrease both increased with increasing Cu level at the back contact of the stressed devices. Stressing at short circuit (SC) produced different changes in performance, but in general these were less severe than those produced by OC stress. In other studies, CdS:Cu devices produced without intentional Cu at the back contact had Voc >800 mV but "noisy" FF – apparently due to poor back contacts. Performance of these devices improved with the first 100 hrs of stress followed by a degradation of Voc. Chris suggested that with improved processing, Cu-free back contacts could be further improved.

4.4 Michael Kempe, NREL, presented **"Effects of encapsulation on CdTe based device performance"**. Individual cells were contacted with a Ag ink "post" and then laminated using a variety of materials. Lamination resulted in changes in performance that were mostly, but not always, negative. Laminated devices were stressed at 1 sun illumination, 60 C, and at either 1.4% or 60% relative humidity (RH). Higher lamination temperatures and longer lamination times resulted in greater losses during lamination and also during post-lamination stress. Voc loss increased with RH. Voc loss was not due to shunting or to reduced carrier concentration. Infrared imaging and TRPL measurements suggested that degradation was associated with the region located below the Ag post. Moisture ingress may increase the concentration of metal ions or may promote their increased mobility due to swelling of the carbon dag.

4.5 Dave Albin, NREL, presented **"Temperature dependent degradation in CdTe devices – What T is appropriate for ALT?"**. Analysis of similar devices stressed at 60, 80, 100 and 120 C identified different mechanisms that are active at different temperatures. At 60 C back contact mechanisms dominate, at 80 C voltage-dependent collection is

affected, and above 100 C junction recombination affects Voc. Device performance was not observed to stabilize in these studies.

After the presentation, Tom McMahon commented that the activation energy of 0.63 eV – identified in Dave's analysis as characteristic of degradation below 80 C – was characteristic of Cu diffusion.

5.0 MATERIALS CHEMISTRY

5.1 Brian McCandless, IEC, introduced the Materials Chemistry subteam. The subteam purpose is to understand and quantify the relationships among processing, chemistry, and electronic properties in order to achieve improved performance, thinner CdTe and reduced processing time.

5.2 Brian McCandless, IEC, presented **"Decoupling control variables and quantifying chemistry in high throughput CdTe/CdS solar cell processing"**. Brian listed major effects of varying process variables on physical and electrical properties of films and devices and quantified CdTe growth rate and CdTe oxidation reactions. In addition Brian provided detailed information on Cd and Zn chloride heat treatment, alloy formation, alloy and oxide properties and on bulk and grain boundary diffusion. In addition Brian provided details of device performance achieved with a range of growth rates, CHT temperature and time, and etchants.

5.3 Fred Seymour, CSM, presented **"Performance and defects in CSS and VTD CdTe cells treated with and without Cu and $CdCl_2$"**. Devices produced with CdTe from four sources (NREL - CSS/Cd_2SnO_4, NREL - CSS, IEC - VTD and CSM – VTD/gas jet) were analyzed both by IV and admittance spectroscopy (AS). Correlations were observed between Voc and a) capacitance spread and b) "base" capacitance, both measured at 65 C. Details of AS, J-V-T - including freeze out of Jsc, capacitance transients, and DLTS - can be found in Appendix 19.

5.4 Chris Ferekides, USF, presented **"PL studies of CdTe films and junctions"**. PL spectra measured at 15 - 100 K were measured on various film stacks both as-deposited (AD), with CHT and with an additional CuCl treatment. PL spectra depend strongly on details of the process, e.g. CSS vs CBD CdS. Specific PL emission at 1.332 and 1.511 eV are associated with CdSTe alloys. A band at 1.232 eV is eliminated by CHT and created by Cu diffusion. Work continues.

5.5 Caroline Corwine, CSU, presented **"Linking defects seen in PL to device performance"**. Analysis of devices produced on CdTe from a variety of different sources indicates that the Cu_i-O_{Te} "D-center", located 125 meV below the conduction band, is a compensating donor that is associated with good devices. It is speculated that this D-center may replace the mid-gap V_{Te}, but that it also limits attainable Voc. Caroline suggests that an alternative way to replace V_{Te}, e.g. with Sb_{Te} or Cl_{Te}-V_{Cd}, might produce good devices with higher Voc.

5.6 Al Enzenroth, CSU, presented **"Observations of Cu diffusion in CdTe PV devices"**. Al used transient ion drift (TID) to measure diffusion of Cu_i^+ in CdTe and concluded that Cu_i^+ has no significant impact on device performance except to the degree that mobile Cu ions react with less mobile defects. Using transient admittance spectroscopy (TAS) to determine the concentration of Cu_i-V_{Cd} (X-V) pairs, Al showed that X-V pairs are associated with unstable performance and that stressing of devices produced with non-optimum processing converted X-V defects to Cu_{Cd}. X-V pairs are expected to originate at surfaces or interfaces and then to diffuse into the CdTe. Stable CdTe devices are expected to have the following characteristics: low trap density, no Cu reservoir, Cu_{Cd} dopants, and non-detectable levels of X-V pairs.

5.7 Glenn Teeter, NREL, presented **"The thermal decomposition kinetics of Cu_2Te: Relevance to CdTe devices"**. The presence of Cu_2Te at the metal-CdTe interface is believed to convert a Schottky barrier to an ohmic contact. In this study the presence of Cu_2Te on CdTe was confirmed using AES. Glenn analyzed the kinetics of Cu_2Te decomposition into Cu(s) and Te(v) using thermal decomposition mass spectroscopy (TDMS) of Cu_2Te formed on Cu foil in a vacuum. Cu_2Te is unstable above 400 C.

5.8 Clemens Heske, UNLV, presented **"X-ray and electron spectroscopy of surfaces and interfaces in CdTe thin film solar cells"**. Clemens described an arsenal of surface and near-surface analytical techniques available at UNLV and suggested that there may be many opportunities for collaboration with the thin film community. For example, X-ray emission spectroscopy of the CdTe from UT before and after CHT showed that CHT created both CdS and SO_4^{2-} plus some Cl-Cd bonds on the free CdTe surface. Typically in order to perform analyses of interfaces requires preparation and analysis of several substrates including "with" and "without" the over layer film as well as substrates with intermediate layers of 10 or 20 nm.

5.9 Rommel Noufi, NREL, presented **"Chemical fluctuation-induced nanodomains in $Cu(In,Ga)Se_2$ films (implication on charge separation in the device)"**. Rommel showed the experimental validation of a material model of Cu-poor CIGS as a two phase material with Ga segregating to an α-phase and V_{cu} segregating to a β-phase. Phases are crystallographically coherent but electronically different. Misalignment of the conduction band minima and valence band maxima of the two phases produces nano-domains that tend to separate charge carriers, reduce recombination, and thereby enhance device performance.

6.0 CDTE V_{OC} MINI-WORKSHOP

6.1 Fred Seymour, CSM, opened the Voc mini-workshop. In order for CdTe PV to improve its competitive position with respect to wafer Si PV it must increase efficiency. Comparing current champion device parameters to target and "near ideal" parameters indicates that Voc has the most room for improvement. The purpose of the workshop was therefore to raise team awareness of Voc limiting issues and to collectively develop a list of ideas for raising Voc.

6.2 Victor Karpov, UT, presented **"Voc workshop: Back contact and Nonuniformity"**. Victor focused on back contact effects on Voc and emphasized that average properties may not be as relevant as nonuniformities. Weak diodes and reach-through-diodes can create areas of high current at applied voltage much lower than the area-weighted average Voc and thereby greatly reduce device Voc. Surface doping may be the key to higher Voc.

6.3 Jim Sites, CSU, presented **"Can Voc for CdTe cells be increased significantly?"**. Jim believes that improved Voc requires a combination of increased doping levels – a reasonable goal would be 2×10^{16} cm^{-3} – combined with a large carrier lifetime - >1 ns – and low interface recombination velocity – say 0.0002 v_{th}. Conduction band offset is a problem in that it reduces the drift velocity of electrons in the interface-recombination region and thereby increases recombination velocity. A reduction in trap density would be expected both to increase hole density and to increase electron lifetime. Perhaps a ZnTe back surface electron reflector part of the solution.

6.4 Alan Fahrenbruch, CSU, presented a few slides to illustrate the implications of p-i-n compared to p-n device models. In p-i-n devices Voc tracks the back barrier whereas for p-n junctions Voc may increase with donor concentration but efficiency can still drop due to reduced depletion width and

increased recombination. If Alan had $50 M to invest he would spend it to improving the back barrier - $25 M to increase lifetime and $25 M to increase doping. At Voc 50% of the current is lost due to recombination at the back barrier. Why did ZnTe not work as a back barrier? It would be worth knowing. Trial and error may be the best approach. Also, we should avoid Cu.

6.5 Brian McCandless (IEC) & Chris Ferekides (USF), presented the results of a survey that had been sent earlier to all participants – **"Fabrication perspective on open circuit voltage in CdTe/CdS thin film solar cells"**. These responses were not discussed in detail, but selected comments from responders are listed below.

CSU

- a manufacturing-worthy process goal is 850 mV Voc
- favored approach - using cost-effective HRT
- Voc is limited by interface state pinning (see Darmstadt results and analysis)

IEC

- Process control can lead to 900 mV Voc
- Voc is limited by
  - Low absorber conductivity [carrier concentration]
  - Screening by back contact combined with low doping
  - Vbi (note Voc saturation at 200 K)
  - Recombination
  - Windows play secondary role – rather effect is on CdTe-TCO interaction [consider Golden Photon devices]
  - Also listed are suspected impact of various process steps
- Approaches
  - control equilibrium defect chemistry and thereby carrier lifetime
  - focus on deposition rather than post-deposition
    - Cd/Te ratio during growth
    - in situ doping
    - controlled growth
  - consider substrate configurations – enables direct control of junction properties
  - modify absorber bandgap
  - CdZnTe alloys (demonstrated 13.3% efficiency with Eg=1.50 eV: 840 mV Voc, 24.4 mA/cm^2 Jsc, 65% FF)
  - ZnS to replace CdS window
  - nitrogen doping
  - modify absorber conductivity

NREL

- Thick vs thin CdTe is key issue – best efficiencies with thick but there are real advantages with thin!
- Shows data on effects of buffer, Cu in graphite paste, CHT enhancement of Cu impact, Ag vs Ni, NP etch, vapor CHT oxygen ambient

USF

- Key issues
  - High work function back contact (data showing impact of Cu_xTe thickness on Voc)
  - CHT-Cu-O parameter space has been fully optimized
    - Data showing impact of CHT, In_2O_3 and CdS thicknesses on Voc
    - Process step interactions
    - Need to break out!
- Key options
  - Increased doping
  - Better contacts
  - Thinner CdTe combined with novel back contact that can be applied with a "decoupled" process step

CSM

- Complex process interactions limit control of Voc making it difficult to identify root cause
- Suspect Voc is sensitive to process parameters that are not well controlled
- Need to simplify and control process
- Possible ways to exceed 850 mV
    - Alternative window
    - Surface/interface treatment
    - Increase absorber doping
    - Passivate deep defects

6.6 Xuanzhi Wu, NREL, presented **"Voc Improvement"**. Xuanzhi reviewed performance of record devices to make the point that , while both Jsc and FF are relatively close to their practical limits, Voc has significant room for improvement. TRPL of 2200 ps has been demonstrated in CdTe films. The key issues are producing uniform, high quality films over large areas and reduction of Cu, Cl and O related defects. Higher Voc can be achieved through a combination of identification of defects that affect Voc and development of processing procedures to reduce their concentration.

6.7 Fred Seymour, CSM, led an active discussion of Voc limitations and possible remedies; Fred's summary lists 37 ideas separated into 6 categories.

7.0 PLANNING

7.1 Harin Ullal and Chris Ferekides led a discussion of planning future CdTe Team activities. Harin noted that announced thin film manufacturing capacity expansions indicate that thin film PV manufacturing capacity worldwide will be 874 MW by 2010. Five new CIS companies are expected to be announced in the US in the near future.

Participants discussed modifications to the present CdTe Team organization into three subteams; there was general agreement that the three subteam structure should continue. Workshops, such as the mini-workshop on Voc, could be included as appropriate.

Members made several suggestions - a few are listed below. None were selected for further action but may be adopted as appropriate.

- Ken Zweibel suggested that thin films, even though highly desirable, should not be a major Team focus.
- Dean Giolando suggested that we might bring in guest speakers from other related technologies.
- Jim Sites suggested that Measurements would be a good topic for a future workshop.
- Alan Fahrenbruch said we need more comprehensive measurements on selected cells including detailed descriptions of how the measurements are made.
- Victor Karpov suggested we should have a Team database.
- Bolko vonRoedern stated that we should be careful of "unfiltered data".
- Markus Gloeckler suggested that we should encourage material measurements such as of grain structure and electroluminescence.

7.2 Adjourn - Harin Ullal complimented members on their contributions and active participation and formally closed the meeting. The next National CdTe R&D Team Meeting will be held in Golden, CO in about 9-12 months.

National CdTe R&D Team Meeting

Harin S. Ullal & Peter V. Meyers

Thin Film Photovoltaics Partnership Program

National Center for Photovoltaics

NREL Visitors Center • Golden, Colorado • March 9-10, 2006

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National CdTe R&D Team Meetings

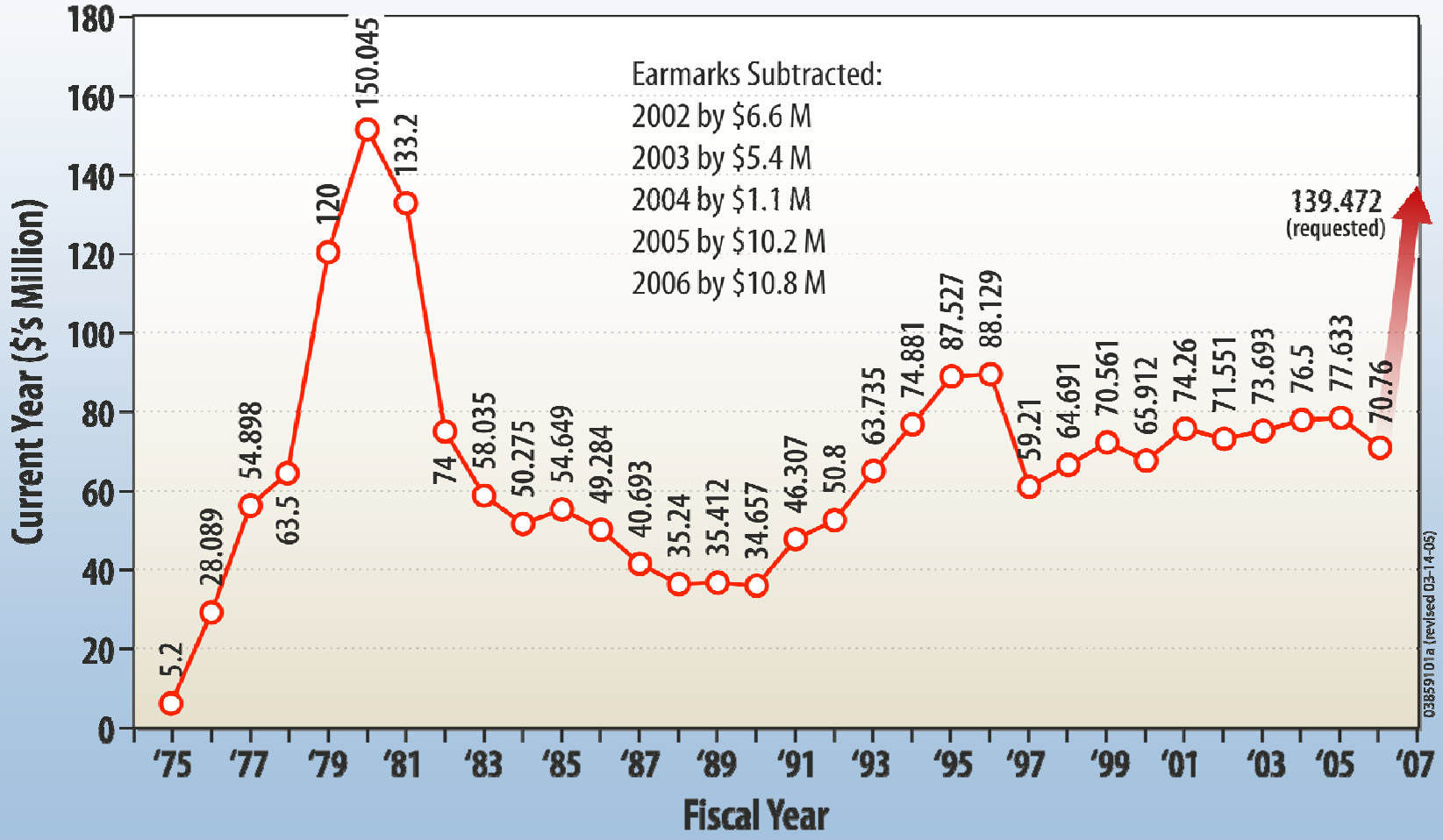
- December 5-9, 1994; Kona, HI
- May 16, 1995; Lakewood, CO
- January 22, 1996; Newark, DE
- May 15, 1996; Washington, DC
- November 18, 1996; Lakewood, CO
- April 30, 1997; Newark, DE
- October 1, 1997; Anaheim, CA
- January 15-16, 1998; Cocoa, FL
- September 8, 1998; Denver, CO
- May 6-7, 1999; Golden, CO
- January 27-28, 2000; Golden, CO
- January 25-26, 2001; Golden, CO
- October 14, 2001; Lakewood, CO
- March 14-15, 2002; Cocoa, FL
- Oct. 31-Nov. 1, 2002; Golden, CO
- July 10-11, 2003; Golden, CO
- February 26-27, 2004; Perrysburg, OH
- May 5-6, 2005; Golden, CO
- March 9-10, 2006; Golden, CO

DOE/NREL Budget

Group	DOE EERE	DOE PV	NREL PV	NREL
1995	$ 1.2 B	$ 85 M	$ 48 M	$ 237 M
1996	0.8 B	60 M	39 M	175 M
1997	0.8 B	56 M	39.7 M	149 M
1998	0.9 B	62 M	44 M	173 M
1999	1.0 B	72 M	51 M?	176 M
2000	1.06 B	66 M	48 M	187 M
2001	1.2 B	75 M	58 M	215 M
2002	1.3 B	66 M	52 M	215 M
2003	1.3 B	66 M	55 M	230 M
2004	1.3 B	75 M	57 M	211 M
2005	1.3 B	77 M	51 M	202 M
2006	1.2 B	71 M	49 M	189 M

03967201

DOE PV Program Budget History
(Fiscal Year)



SAI & NOPI Websites

Ullal, Harin

Subject: SAI & NOPI - Websites

NOPI_DE-PS36-06G
O96020.pdf

Solar America Initiative (SAI)

http://www1.eere.energy.gov/solar/solar_america/index.html

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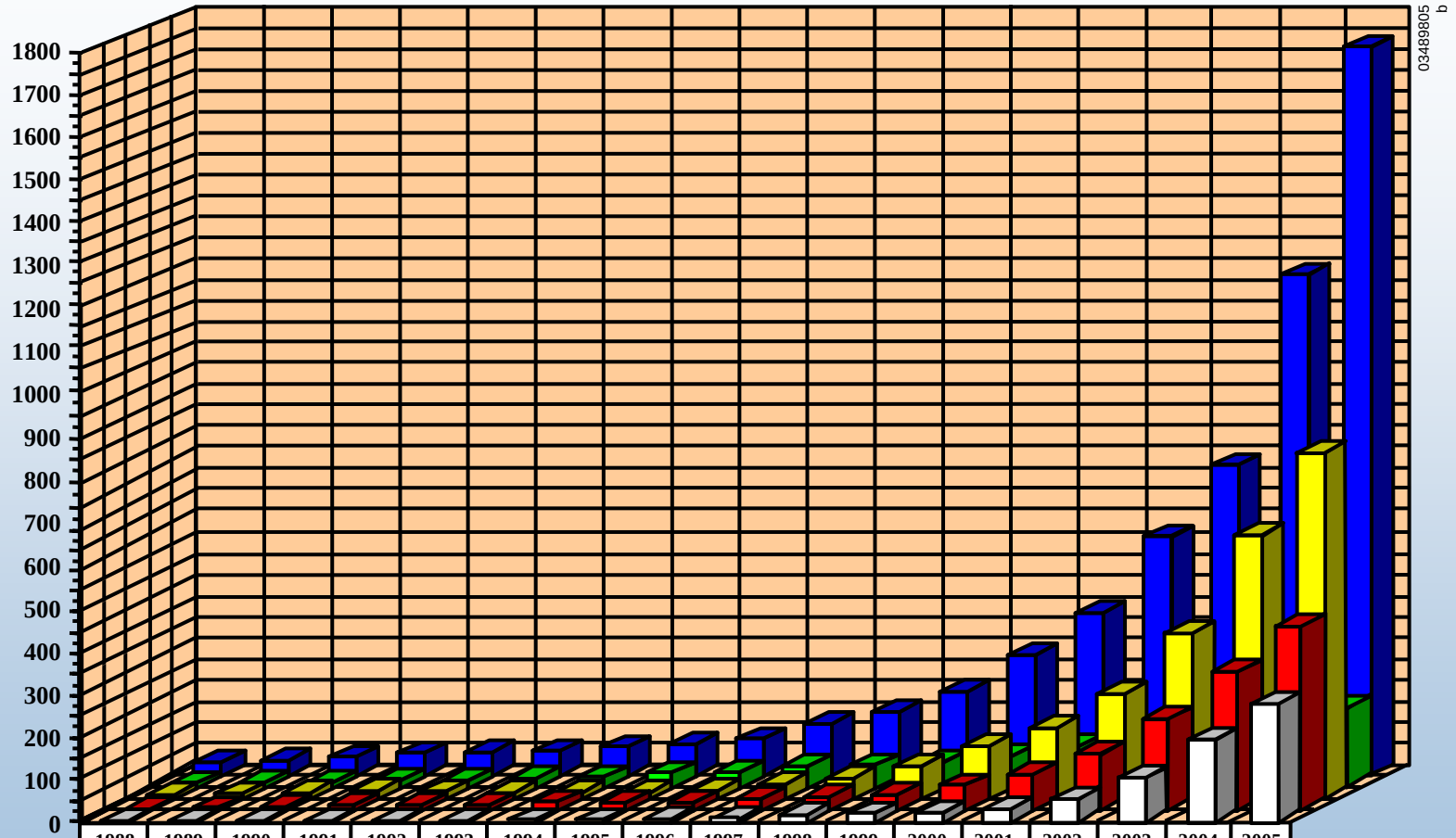
Notice of Program Interest (NOPI), Solar America Initiative Technology Pathway Partnerships

This Notice of Program Interest (NOPI) addresses one of the planned funding mechanisms for obtaining industry participation in the Solar America Initiative: The Technology Pathway Partnerships - Phase 1 Funding Opportunity Announcement. Per the NOPI, a Technical Exchange Meeting will be convened in Chicago, Illinois in mid-April 2006 to facilitate external contributions to planning for the Solar America Initiative. For access to the NOPI, visit the Department of Energy's e-Center at: <https://e-center.doe.gov/>, and Browse Financial Assistance Opportunities by date, select March 2006, and select the March 3 posting. The full announcement can be accessed by selecting "Full Announcement & Other Files" at.
<https://e-center.doe.gov/iips/faopor.nsf/8df825feb86675de852564650046fa ea/8cb1060444f7907a852571260063ecd1?OpenDocument>
Or, download the pdf at:
<https://e-center.doe.gov/iips/faopor.nsf/UNID/8CB1060444F7907A852571260 063ECD1/$file/NOPI_DE-PS36-06GO96020.pdf>
Solar America Initiative:
<http://www1.eere.energy.gov/solar/solar_america/index.html>
White House, Advanced Energy Initiative:
<http://www.whitehouse.gov/infocus/energy/>

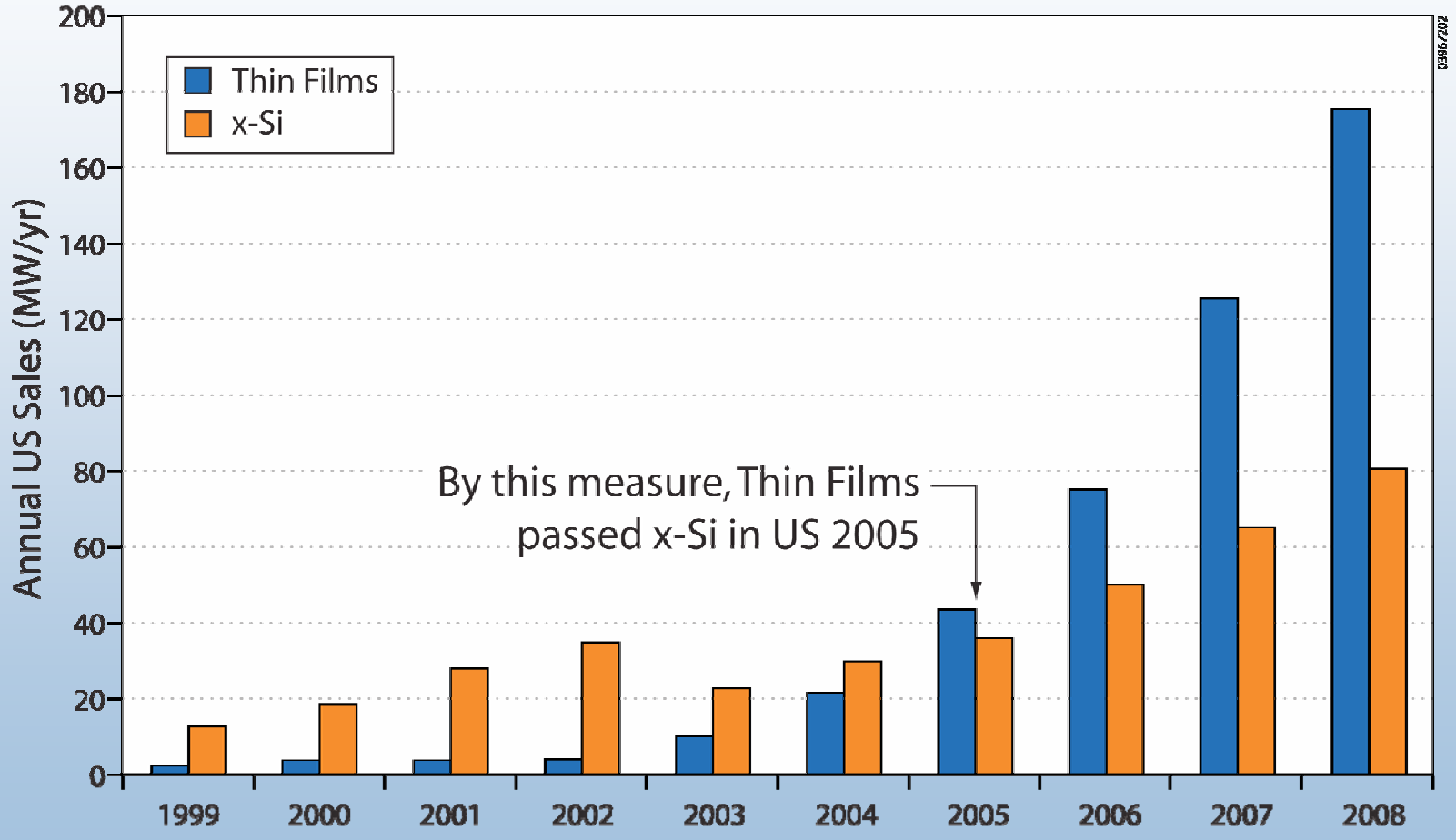
World PV Cell/Module Production (1988-2004) Megawatts



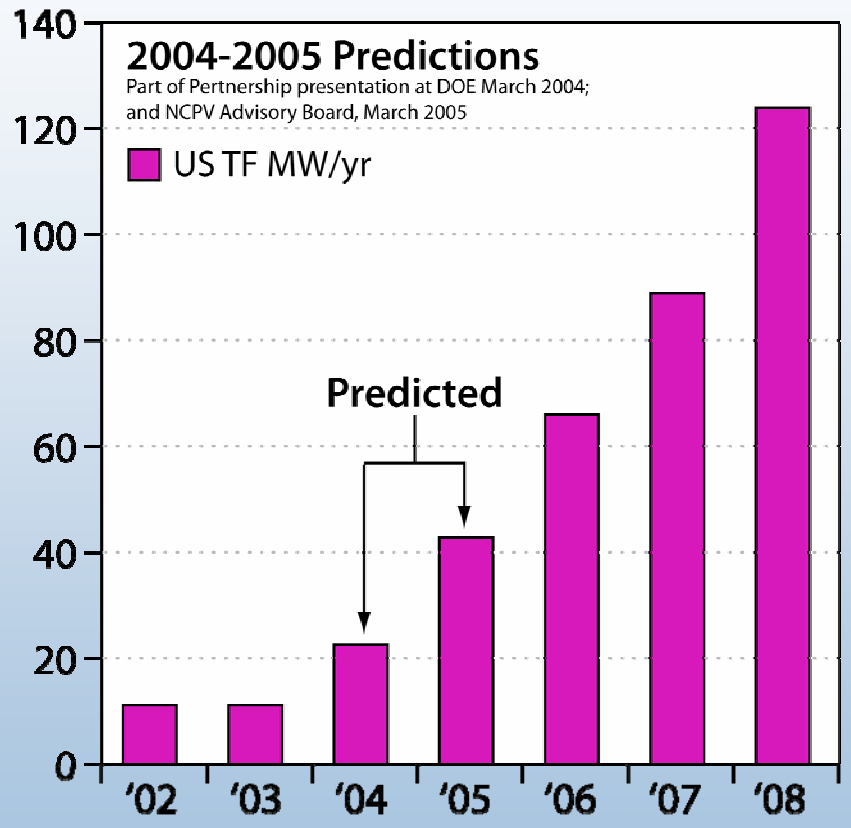
	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005
Rest of World	3	4	4.7	5	4.6	4.4	5.6	6.35	9.75	9.4	18.7	20.5	23.42	32.62	53.55	84	129	289
Europe	6.7	7.9	10.2	13.4	16.4	16.55	21.7	20.1	18.8	30.4	33.5	40	60.66	86.38	135.05	190	308	452
Japan	12.8	14.2	16.8	19.9	18.8	16.7	16.5	16.4	21.2	35	49	80	128.6	171.22	251.07	364	618	833
United States	11.1	14.1	14.8	17.1	18.1	22.44	25.64	34.75	38.85	51	53.7	60.8	74.97	100.32	120.60	104	139	153
Total	33.6	40.2	46.5	55.4	57.9	60.09	69.44	77.6	88.6	125.8	154.9	201.3	287.65	390.54	560.27	742	1194	1727

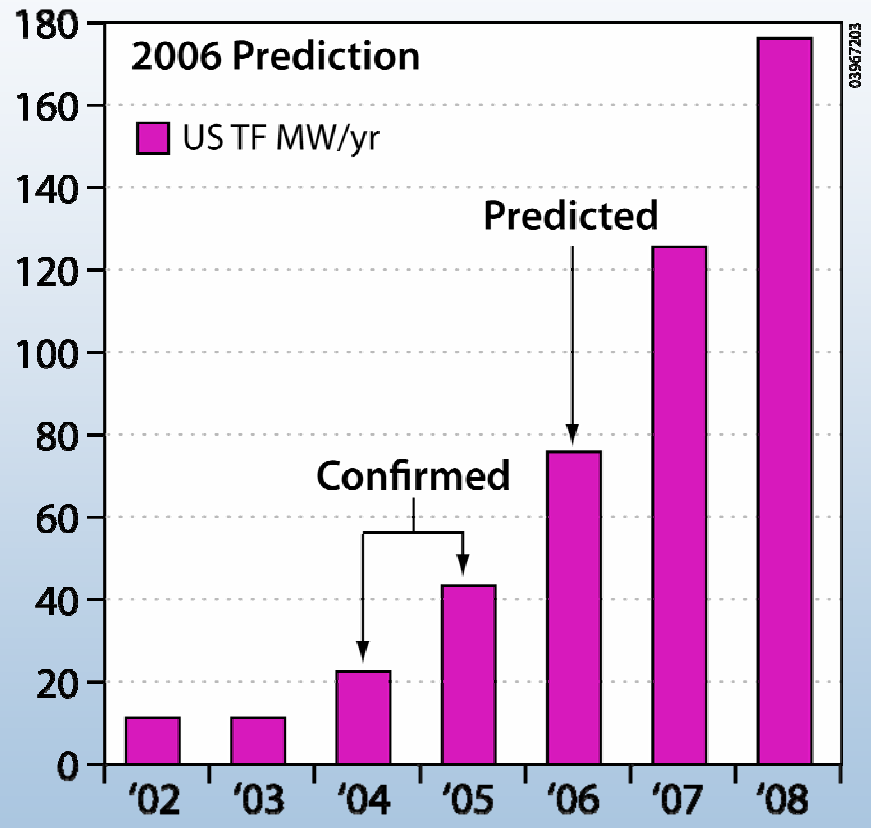
From PV News, Paul Maycock, Editor; yearly February editions.

Historical and Projected x-Si & Thin Film Modules Made in the US *(through 2004)* by US-Owned Companies



Accelerating US Thin Film Production





Thin Film PV Partnership
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Device Physics Subteam

B. McCandless (IEC)
Back surface illumination study

T. Gessert (NREL)
Analysis of identical ZnTe:Cu/Ti contacts fabricated on various device materials

D. Shvydka (UT)
Piezo-electric coupling in CIGS and CdTe standard and flexible devices

R. Dhere (NREL)
Electro-reflectance diagnostics of CdTe PV

Break

A. Fahrenbruch (ALF/CSU)
Photoconductive CdS and anomalous AQE effects: Comparison of modeling and experiment

W. Metzger (NREL)
Recombination lifetimes in CdTe PV

V. Karpov (UT)
Indicative facts and field reversal device model

J. Sites (CSU)
Impact of lifetime and contact barrier on CdTe J-V

General Discussion

Stability Subteam

Dave Albin (NREL)
Team Introduction, "Update on CdTe Degradation Modes"

Alan Davies (CSU)
"Smoothing and stability enhancing behavior of Cu in un-etched, $CdCl_2$ treated, CdTe solar cells"

Chris Ferekides (USF)
"Stress Studies of CdTe Devices: Intentionally Cu in CdS vs. Back Contacts"

Mike Kempe (NREL)
"Effects of Encapsulation on CdTe Based Device Performance"

Dave Albin (NREL)
"Stress Temperature Effects on Conventional Light-Soak, Open-Circuit CdTe ALT"

Materials Chemistry Subteam

B. McCandless / Dave Albin
Decoupling control variables and quantifying chemistry needed for high throughput CdTe/CdS device processing.

F. Seymour
Admittance spectroscopy analysis of CSS and VT devices with different $CdCl_2$ processing.

C. Ferekides
Photoluminescence analysis of CSS CdTe films and devices with different Cu, $CdCl_2$, O_2 processing.

Caroline Corwine / Tim Gessert
Photoluminescence analysis of CdTe/CdS films from different labs: NREL, CSU, USF, IEC, and FS.

A. Enzenroth
Transient ion drift method for determining diffusivity and concentration of Cu ions in CdTe cells.

Glenn Teeter
Kinetics of Cu_xTe decomposition.

Clemens Heske
X-ray emission spectroscopic analysis of CdTe films and devices.

Rommel Noufi
Chemical Fluctuations-Induced Nanodomains in CIGS Films.

Mini-Workshop — Improving V_{oc}

1) **Introduction (Seymour, ~ 5 minutes)**

2) **Device Physics (Karpov, ~ 15 minutes + ~5 minutes questions)**
   Lateral non-uniformites, back contact and other ideas for increasing V_{oc}

3) **Device Physics (Sites, ~ 15 minutes + ~ 5 minutes questions)**
   Doping, SRH recombination defects, window layer and heterojunction ideas for increasing V_{oc}

4) **Device Fabrication (Ferekides & McCandless, ~ 30-40 minutes)**
   Device fabricator perspectives and survey results. Each cell fabricator might comment/respond to their survey input ideas for increasing V_{oc}

5) **Team/Panel Discussion on Increasing V_{oc} (Seymour moderator, ~ 30-40 minutes)**
   Start with top 10-12 ideas based on survey and panelist input. List divided into "refine existing device design" and "novel approaches". The goal is to reach team consensus on the most promising ideas for increasing V_{oc} and ultimately setting a new record dell efficiency

6) **Conclusions and Closure (Seymour, ~ 5 minutes)**

National CdTe R&D Team Meeting
List of Attendees

March 9-10, 2006

No	Name	Organization
1.	Harin Ullal	NREL
2.	Jim Sites	CSU
3.	Xuanzhi Wu	NREL
4.	Bolko von Roedern	NREL
5.	Markus Gloeckler	FSLLC
6.	W.S. Sampath	CSU
7.	Al Enzenroth	CSU
8.	Caroline Corwine	CSU
9.	Rick Luess	CSU
10.	Alan Davies	CSU
11.	Tim Nagle	CSU
12.	Jun Pan	CSU
13.	Ana Kanevce	CSU
14.	Mowafak Al-Jassim	NREL
15.	Kannan Ramanathan	NREL
16.	Dave Albin	NREL
17.	Samuel Demtsu	CSU
18.	Ramesh Dhere	NREL
19.	Roger Green	FSLLC
20.	Alan Fahrenbruch	ALF
21.	Tom McMahon	NREL
22.	Joe Beach	CSM
23.	Peter Meyers	FSLLC
24.	Ken Zweibel	NREL
25.	Brian McCandless	IEC
26.	Sally Asher	NREL
27.	Rommel Noufi	NREL
28.	Larry Olsen	PNNL

National CdTe R&D Team Meeting
List of Attendees *(cont.)*

March 9-10, 2006

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32.	Chris Ferekides	USF
33.	Al Compaan	UT
34.	Anke Abken	FSLLC
35.	Craig Perkins	NREL
36.	Victor Karpov	UT
37.	Diana Shvydka	UT
38.	Jie Zhou	NREL
39.	Yanfa Yan	NREL
40.	Wyatt Metyer	NREL
41.	Jasum A	NREL
42.	Gary Jorgensen	NREL

No	Name	Organization
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45.	David Strickler	Pilkington
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50.	Carol Riordan	NREL
51.	Pat Dippo	NREL
52.	Joel Pankow	NREL
53.	Kurth Barth	CSU
54.	Robert Collins	UT
55.	Tim Ohno	CSM
56.	Joel del Cueto	NREL

PRESENTATIONS FROM

INDUSTRY

Brief Update of Progress at AVA Technologies LLC

National CdTe Team Meeting
March 7 and 8, 2006

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AVA Technologies LLC
Fort Collins, Colorado

AVA Technologies LLC

AVA Technologies LLC:
Advance CdTe thin film PV manufacturing

- **Formed 1997**
- **Principals: Barth, Enzenroth and Sampath (equal stake)**
- **Funded by DOE since 3/2001**

AVA Technologies

I. AVA Tech and CSU Partnership

- 3 principals are faculty at CSU
- Conflict of interest management plan with CSU
- AVA Tech and CSU partnership promoted as model by University

II. Current DOE Project (Barth PI):

Advance Manufacturing technology, Modules installed for beta testing

Participants

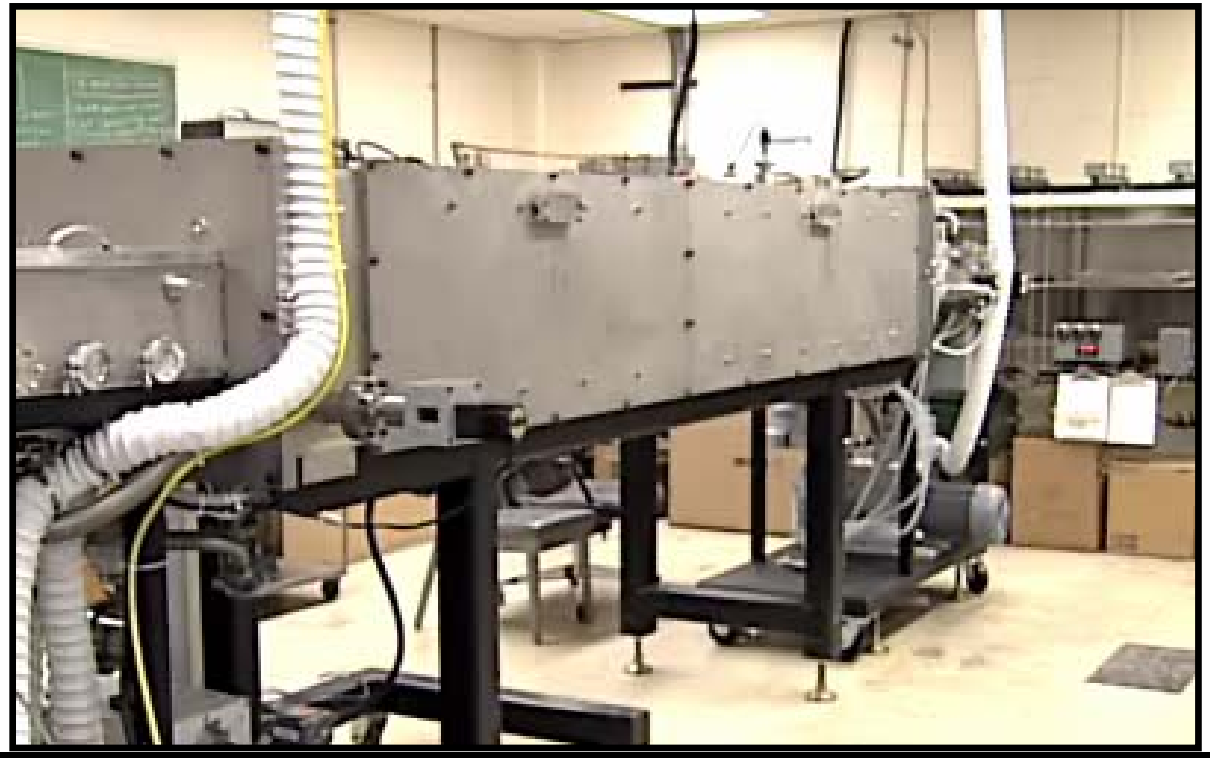
- Colorado State University Engineering is a subcontractor
- NSC/Acheson is partner
- CSU Facilities: PV system engineering, beta testing

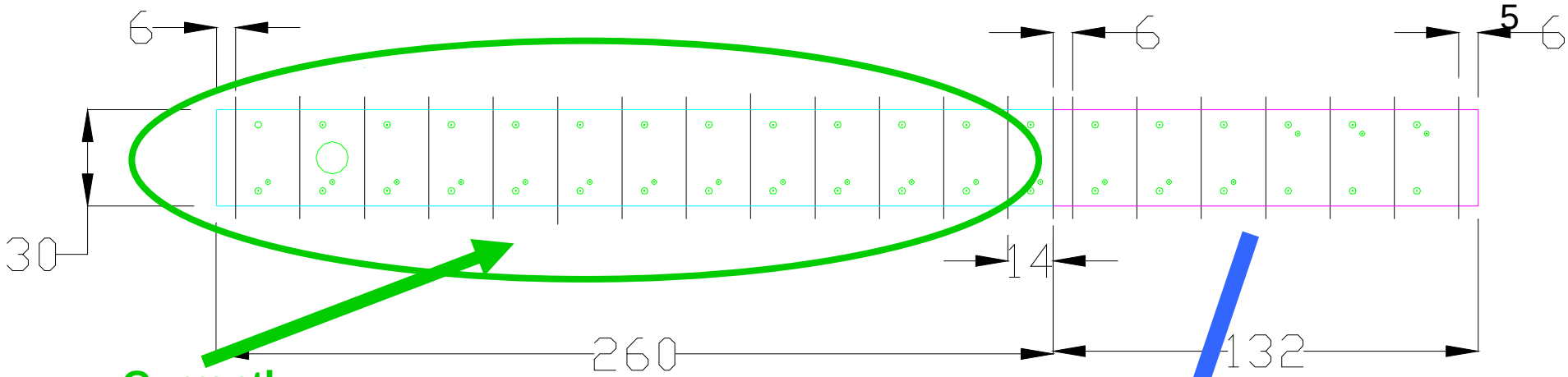
Brief Overview of Technical Progress

I. Completion of nominal 2 MW/yr. semiconductor system

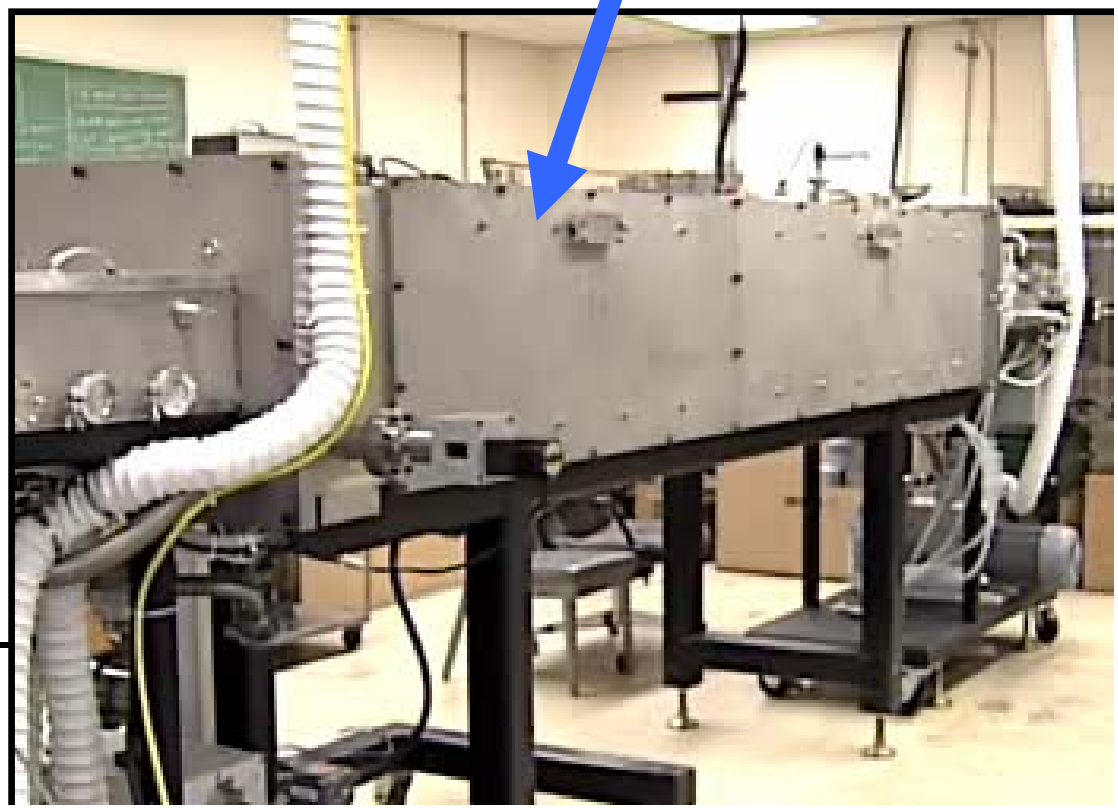
A. Attributes

- Unique automated, continuous semiconductor manufacturing
- Glass in one side, panel out every 2 minutes





Currently under construction



Progress

- Chamber extension
- Design being finalized
- Plans presented to vendor
- Design is being developed to easily scale to 120x60 cm substrates

System delivery expected in 2-3 months

Brief Overview of Technical Progress

II. Process head development for 2 MW/yr. system

A. Process Heads: thermal sublimation

- Same for <u>all</u> processes: CdS, CdTe, $CdCl_2$ and back contact

- Conditions are defined for each processing stage at the film growth surface
  - Substrate temperature
  - Vapor flux
  - Ambient gas conditions

- Process/hardware developed to maintain same process conditions, independent of substrate size

Brief Overview of Technical Progress

II. Process head performance

Process heads constructed and tested

- 78 hr continuous thermal test
- Substrate motion with process heads at full temperature
- No glass cracking observed when numerous 16.5 x 16.5 inch substrates heated from 25C to ~500C in two minutes

At CdTe deposition temperature 500+ C process head thermal performance: + 0%/ -1.3%

Brief Overview of Technical Progress

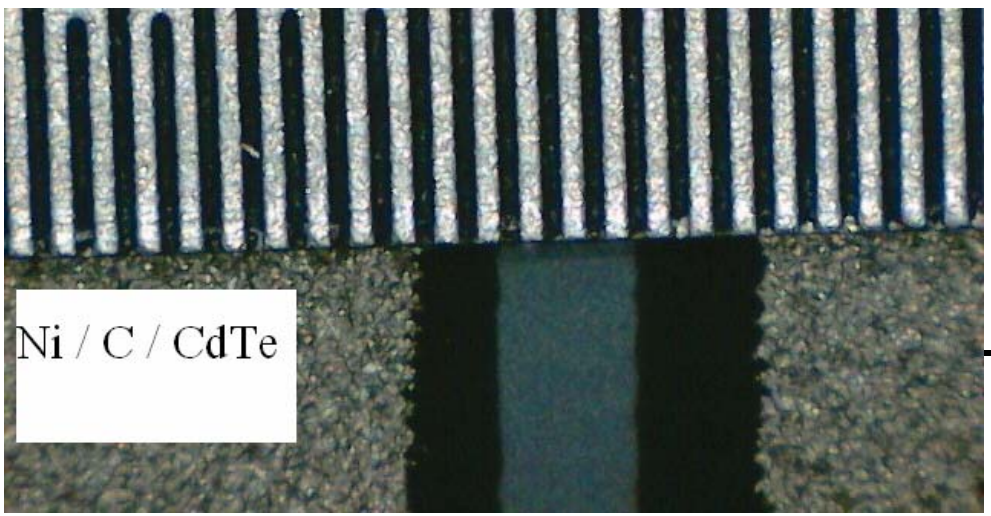
III. Optimization of Back Electrode for Manufacturing

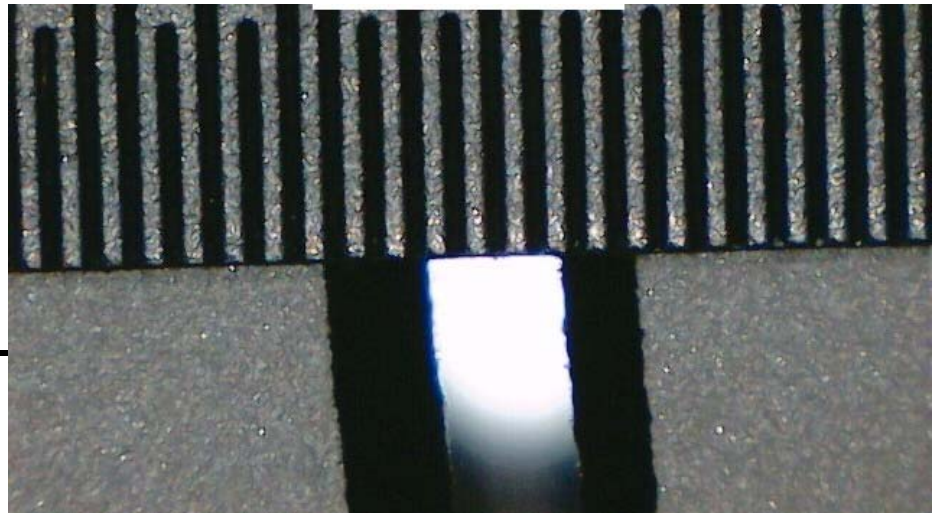
Back electrode: 2 layers: Carbon (in polymer binder) against CdTe then more conductive layer

- Acheson Industries leading effort
- Investigated spray and screen print

  Screen printing avoids "third scribe"

  Methods developed to remove spray coatings
- Excellent adhesion demonstrated with both methods





Cost Methodology

I. The equipment, materials costs and labor requirements were obtained from direct quote or consultation with reputed vendors

II. There are 25 processes to produce modules with this advanced technology. Most utilize commercially available standard industrial equipment

- **Thin film modules are monolithically integrated and have no "cell" stage of processing**
- **There are many significant differences in both the semiconductor and packaging processing between c-Si and thin film modules**

Cost Estimates Background

I. The cost analysis is based on information from the CdTe thin film pilot line and production prototype development at CSU.

II. The analysis is for the following plant and module specifications:

- **Nominally 20 MW/yr. facility**
- **Operating 2 shifts/day, 7 days/week, 49 weeks/yr. (to start)**
- **120x60 cm thin film modules**
- **Module rating of 63 watts**
- **Glass/glass laminate package without frame (typical for CdTe PV)**

Cost Estimate Results

I. The total manufacturing costs with a 95% yield (direct and indirect materials and labor multiplied by 1.05) + estimated overhead, indirect, other costs are approximately

< $1.00/Watt.

II. The total one time equipment costs are approx. $10,000,000

Pathways to Commercialization

AVA Tech has a production manufacturing technology for thin film PV to address current and future market needs

A large company can provide commercialization, business and manufacturing resources

Strategic partnership between AVA Tech and "large company"

A. AVA Tech is the Technology Partner

B. Large Company is the Commercialization Partner

Possible Structure for Business Relationship

Three Step Approach

Staged involvement: The partnership progress as jointly agreed upon milestones for both parties are achieved

1. Initial Involvement:
   - Immediate start after signing contract
   - Accelerate development

2. Production plant development:
   Bring full AVA Tech knowledge/experience resources

3. Full production:
   Plant commission, rapid volume expansion

Pathway to Commercialization

Partnerships with a very large manufacturer
Currently being developed

Target: 20 million watts per yr. plant operational in Fort Collins by end of 2008

Rapid manufacturing capacity expansion

PRESENTATIONS FROM

DEVICE PHYSICS SUBTEAM

Characterization of CdTe Devices with a Transparent ZnTe:Cu Contact

Darshini Desai, Steven Hegedus, Brian McCandless,

Kevin Dobson, Robert Birkmire, Kevin Hart

Institute of Energy Conversion

University of Delaware

Newark DE, USA

Development of CdTe cells with a transparent back contact driven by need to quantify and understand CdS/CdTe device operation

CdTe Device with ZnTe:Cu Contact

Motivation

CdTe device with transparent back contacts using Cu doped ZnTe:

- **Diagnostic tool to characterize device operation**
- **Cu doping source**
- **Transparent interconnect for tandem cell applications**

Goal

Expand the fundamental understanding of CdTe solar cell operation using bifacial device configuration and evaluate ZnTe:Cu as an alternative source of Cu doping

Semi-Transparent ZnTe:Cu Film

Deposition Process

Galvanic deposition with Zn anode and substrate cathode*

Aqueous Electrolyte:

$ZnSO_4$, TeO_2, $CuSO_4$

pH = 3

Temperature: T = 68°C

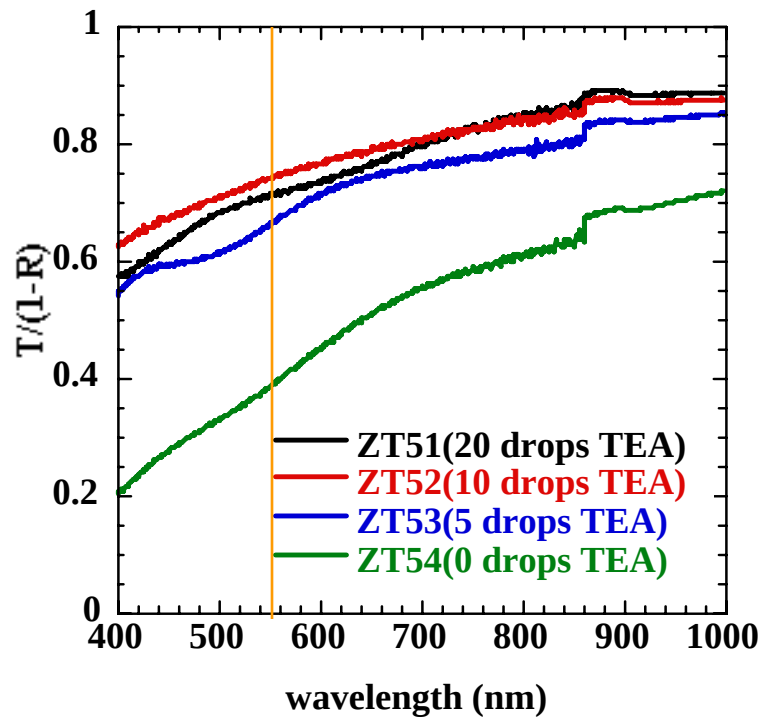
Deposition time 1.5 min ⇒ 50 nm ZnTe

Triethanolamine(TEA):

Regulates Cu activity: higherconcentration = less Cu in ZnTe and higher optical transmission

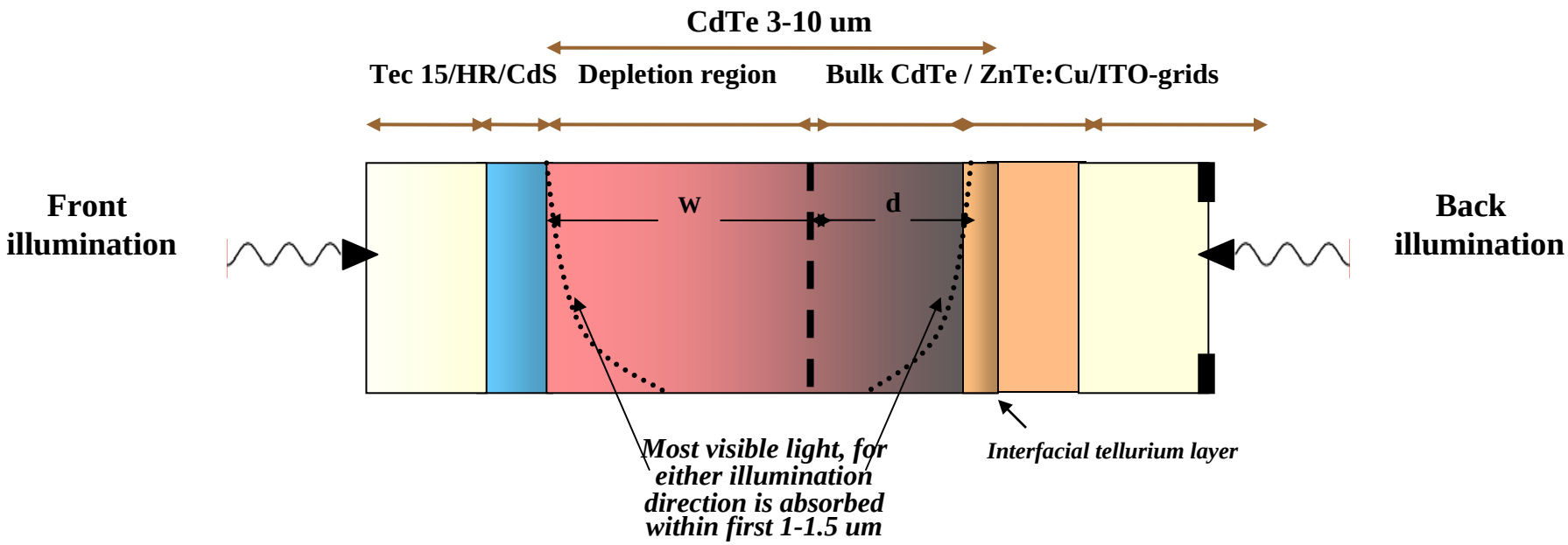
20 drops, [Cu] ~ 10^{-8} M used for devices

Optical Properties ZnTe:Cu on Tec 15



**A. Mondal and B. McCandless, Sol. Energy Sol. Cells 26 (1992) 181*

Bifacial Device Structure using ZnTe:Cu



- **Back contact always in dark for front illumination**
- **90% of visible light absorbed within first micron**
- **ONLY Long λ(RED) can reach collecting junction for back illumination**
- **Wider depletion width (W), greater diffusion length (L), ⇒ narrower field-free region d = (t-W) ⇒ higher collection for back illumination**

Results: CdTe Device with ZnTe:Cu/ITO Contact

Contact	Light direction	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
ZnTe:Cu/ ITO	front back	0.82 0.66	20.3 0.6	68.0 66.3	11.3 0.2
Cu/Ni	front	0.82	20.8	68.7	11.8

Similar front wall performance to baseline metal contact

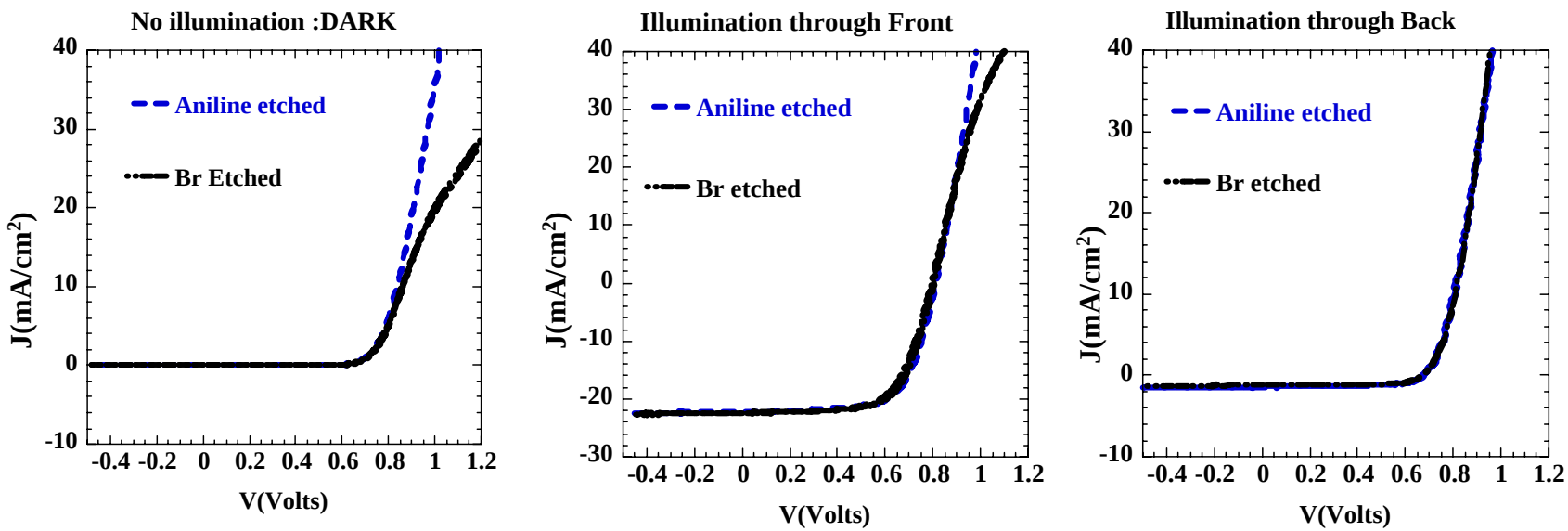
Evaluate effects of:

Etchant : Aniline, BrMe

CdTe thickness : 5 μm (baseline) , 10 μm , 8 μm and 3 μm

Cu : Free Cu regulated by TEA

Bifacial JV Results: Effect of Etchant



CdTe surface etchant: 1) BrMe (<10 nm Te) 2) Aniline (~50 nm Te)

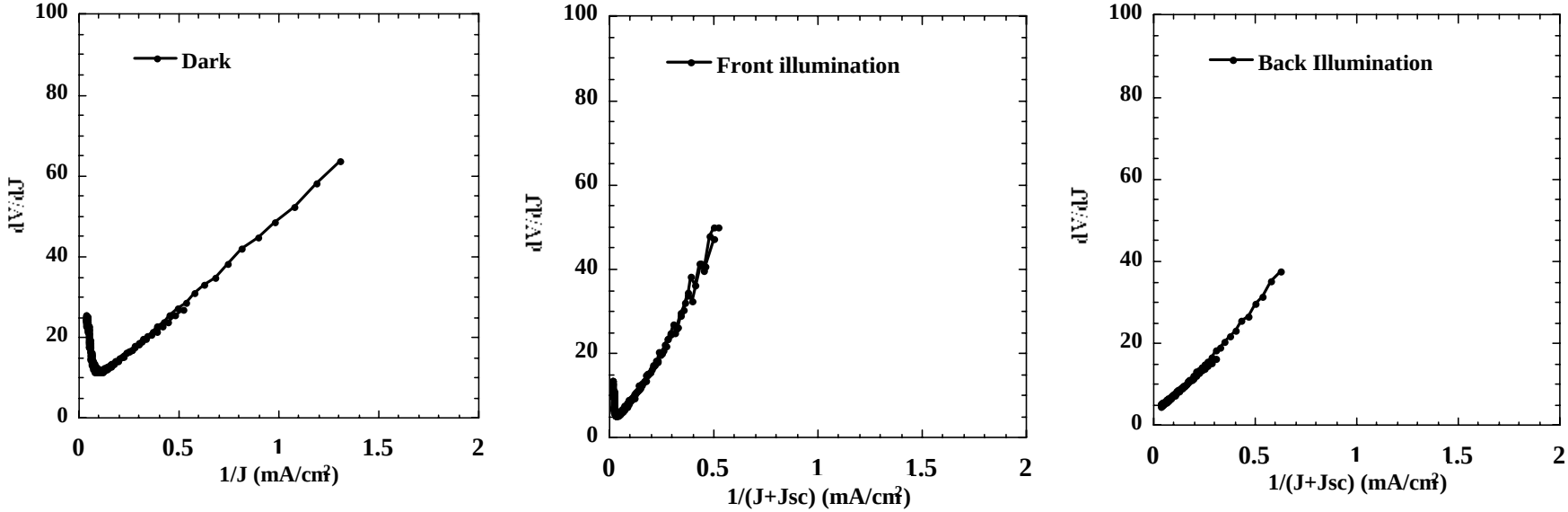
Both have similar FW behavior: Voc>800mV, Jsc~23 mA/cm2, FF > 65%, η > 12.3%

Photoconductive blocking barrier: with BrMe but not with Aniline

- **Blocking contact for front illumination and dark JV**
- **Light through back contact "turns off" the barrier**

Photoconductive Back Contact: dV/dJ Analysis

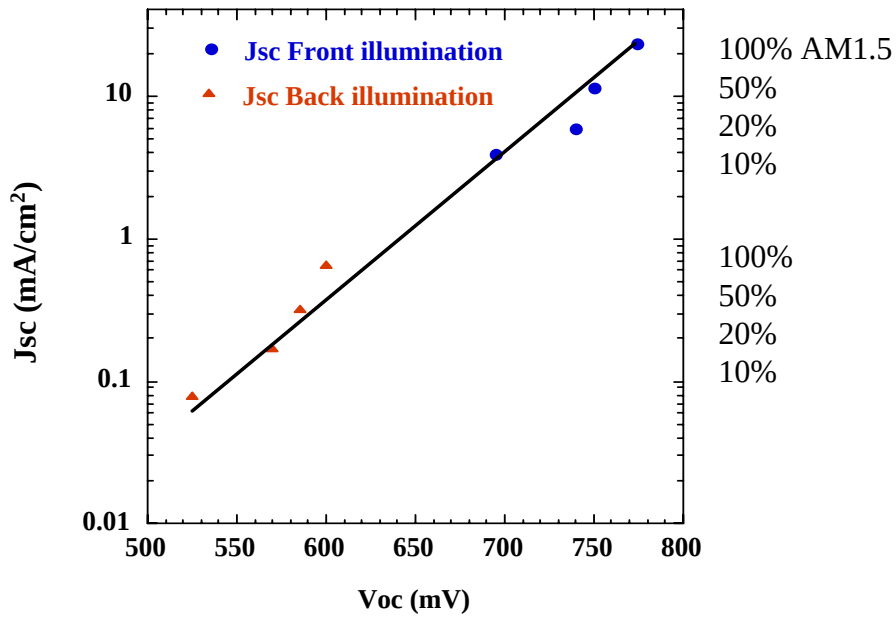
Device with 5 μm CdTe, etched with BrMe



Inflection, corresponding to blocking barrier observed at high J values for front illumination and dark

No barrier seen when device illuminated through the back contact

Bifacial Voc-Jsc for Different Illumination



Voc and Jsc measured at 100%, 50%, 20% and 10% of AM1.5 for front and back illumination

Voc for back illumination same as would have been obtained at lower light intensities from front illumination,

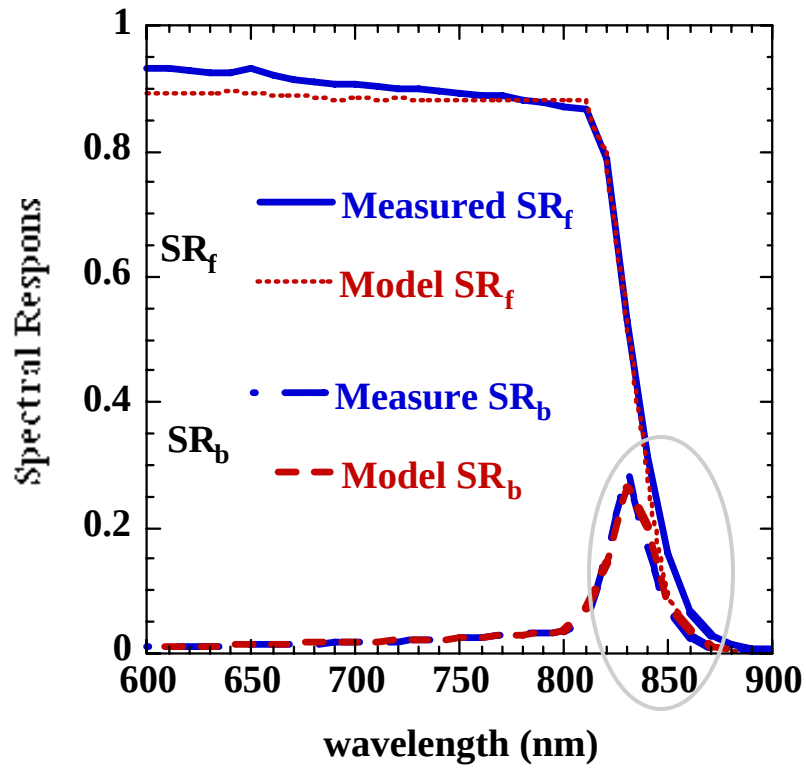
Indicates a single junction determines Voc (no secondary back junction)

Similar results obtained for cells with CdTe from 3 – 10 μm.

Spectral Response: Analysis and Modeling

Fit front and back SR using approach developed by Phillips, 1st WCPVEC 1994

- **Determine internal SR ⇒ collection**
- **Evaluate collection based on diffusion length (material property) and depletion width (dependent on bias) relationships**
- **Input : absorption coefficient and thickness**
- **Fitting parameters: L & W**
- **Fit at different bias: W(V)**

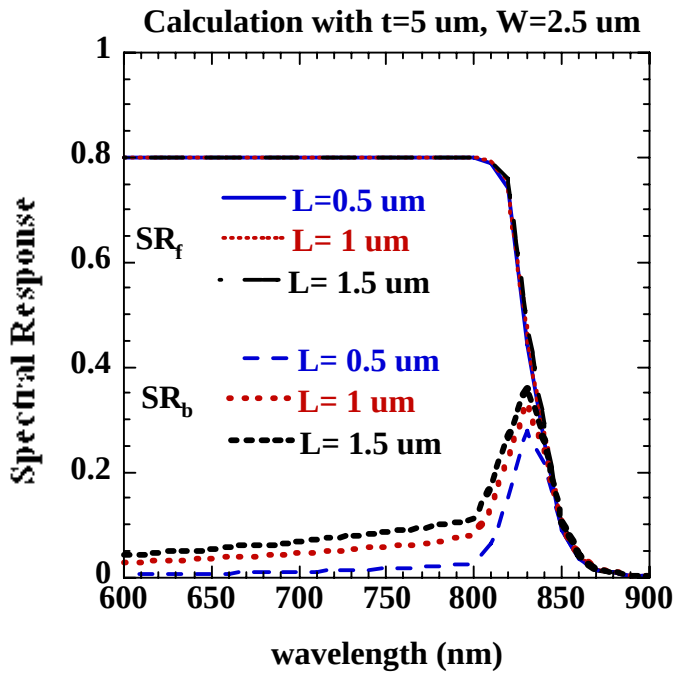


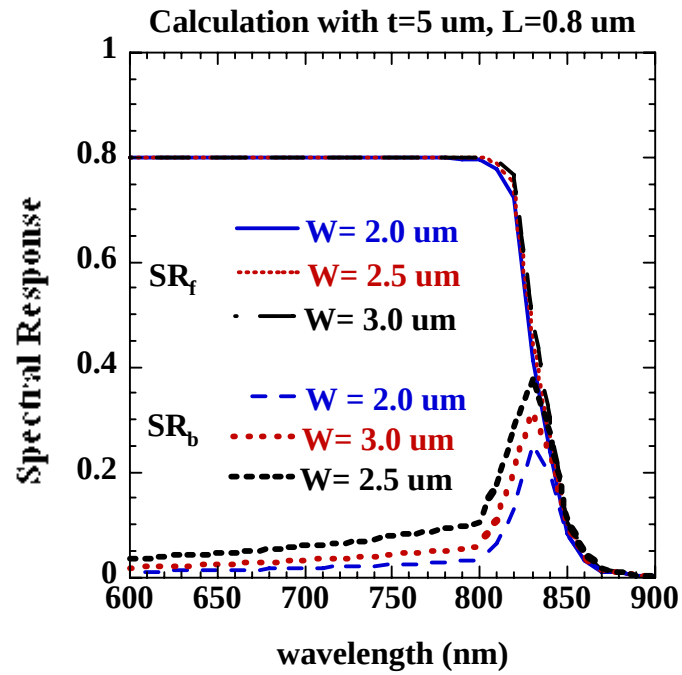
Example: Measured and modeled data at 0V for t = 5 μm CdTe device:

L= 0.72 μm, and W = 2.2 μm

Front SR @830nm > Back SR @830 nm qualitatively consistent with lower bandgap due to S incorporation via interdiffusion of CdS-CdTe

Spectral Response: Modeling Dependence on L and W



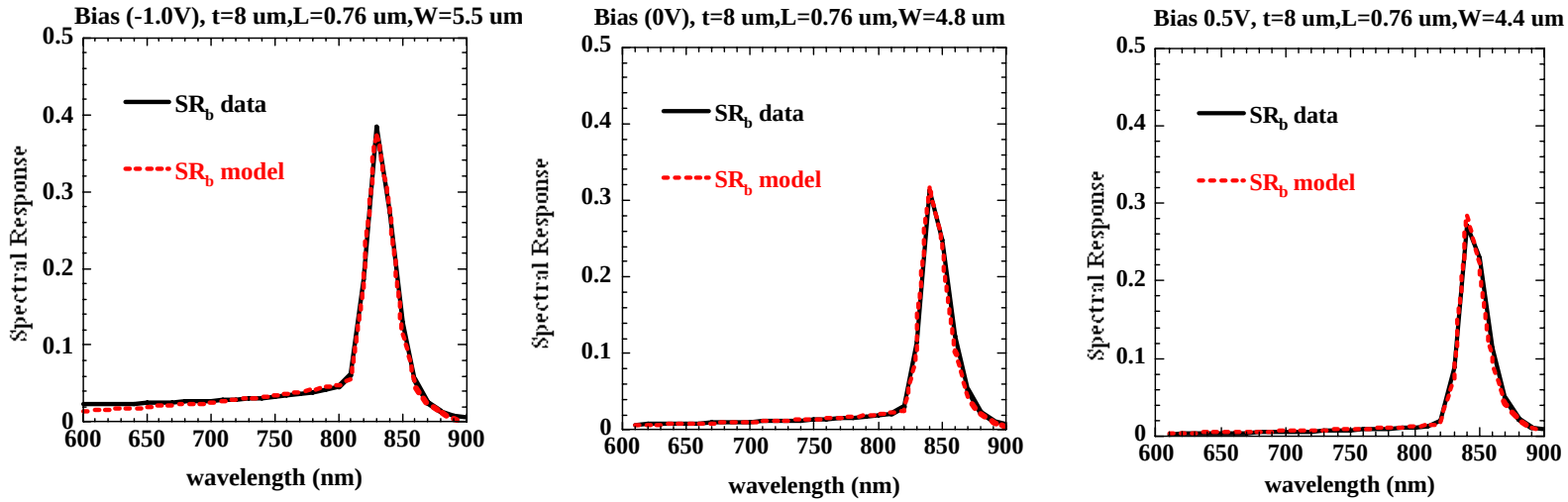


Front SR ⇒ insensitive to changes in both L and W ⇒ near 100% internal QE

Back SR ⇒ very sensitive to changes in L and W since distance carriers must diffuse is (t-W), >> L for t = 5 µm device

Only the carriers generated within the distance L+W from back contact can be effectively collected.

Bifacial SR: Effect of Applied Bias (-1, 0, +0.5V)



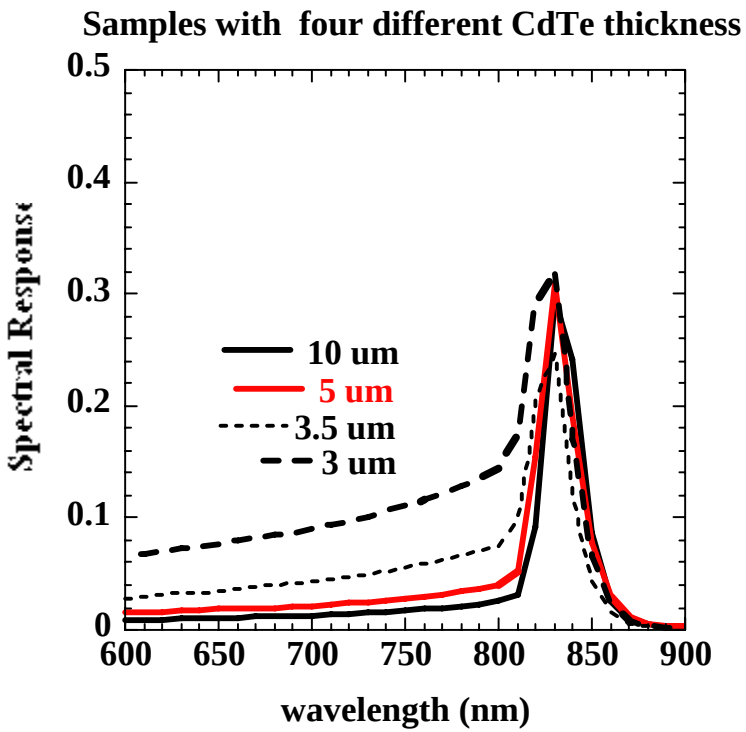
Back SR is very sensitive to W(V): For L= 0.76 μm:

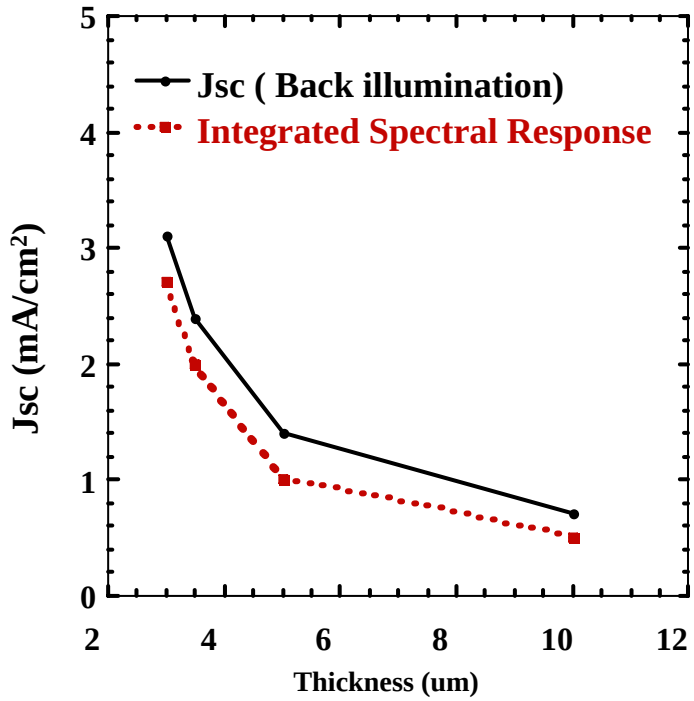
W(-1.0V) = 5.5 μm W(0V) = 4.8 μm W(0.5V) = 4.4 μm

Larger W ⇒ better collection since L+W larger ⇒ more carriers collected at the edge of depletion region

Front SR insensitive to applied bias for V < 0V due to large W: slight decrease in SR for V > 0V

Measured BW SR: Effect of Absorber Thickness





Back SR higher for thinner devices due to smaller field free region (t-W) for carriers to diffuse across before being collected

Consistent with higher Jsc and higher ∫SR higher for thinner devices

Comparison of W(V) from SR Fit and CV

Sample	Thickness (um)	W(-1.0V) SR	W(-1.0V) CV	W(0.0V) SR	W(0.0V) CV	Diffusion Length (L) um
VT 181	8	5. 5	5. 4	4. 8	4. 8	0.76
VT 178	5	2. 6	2. 4	2. 4	2. 0	0.72
VT 180	3	1. 8	1. 7	1. 3	1. 4	0.6

Depletion width from back SR consistent with CV (10 kHz, FW light)

Results validate the bifacial analysis procedure to obtain L and W

Need to separate possible reasons for decreasing W with film thickness

Conclusions

Bifacial device characterization is a extremely useful diagnostic non-destructive tool to determine transport in CdTe devices and can separate effects of front junction and back contact

Depletion width values obtained from SR analysis are consistent with C-V measurements

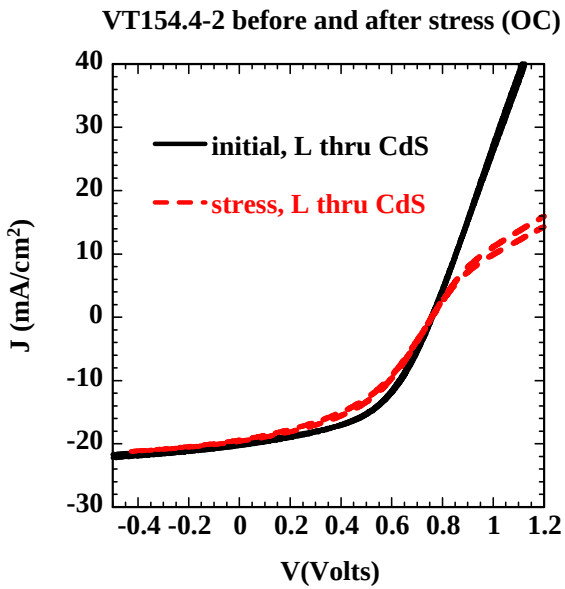
Bifacial SR results indicate the absorber band gap is lower near junction than in 'bulk'

Solar cell performance is determine by voltage dependent collection and not the diffusion length

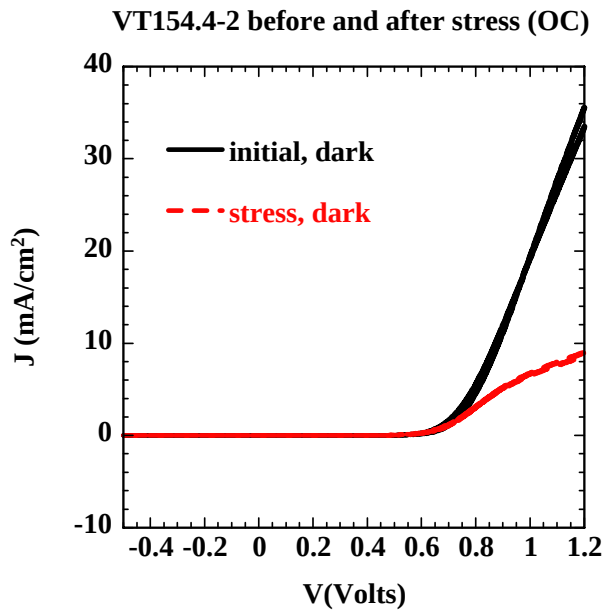
The blocking back contact due to surface etching is photoconductive

Effect of "Stressing ": Back Contact

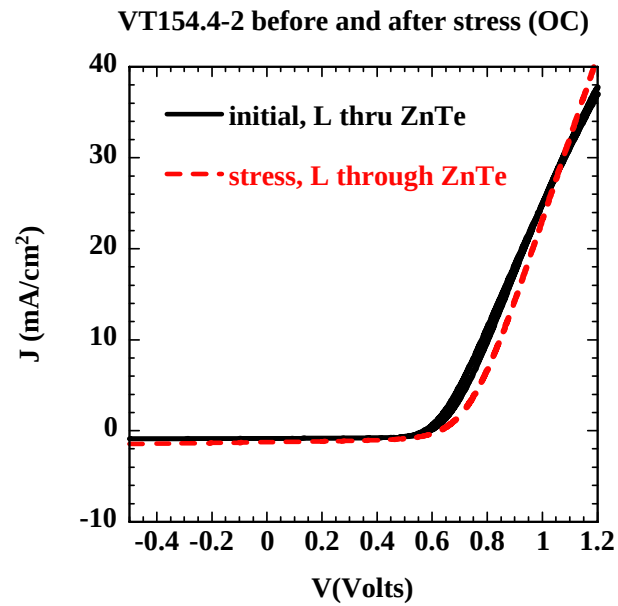
Front illumination



DARK -No illumination



Back illumination



Voltage dependent current collection noticeable for front wall

Barrier observed through front wall and dark but none through back wall

Back contact : Photoconductive, does not degrade with stress

Voc for back wall illumination increases after stress

Analysis of Identical ZnTe:Cu/Ti Contacts Fabricated onto Various CdS/CdTe Device Materials

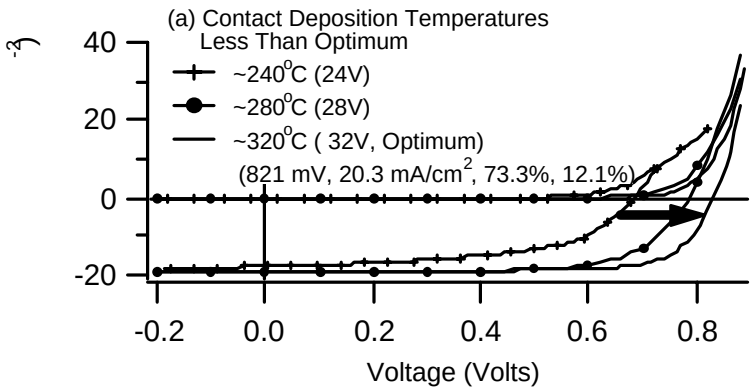
(*LIV/DIV/C-V Analysis*)

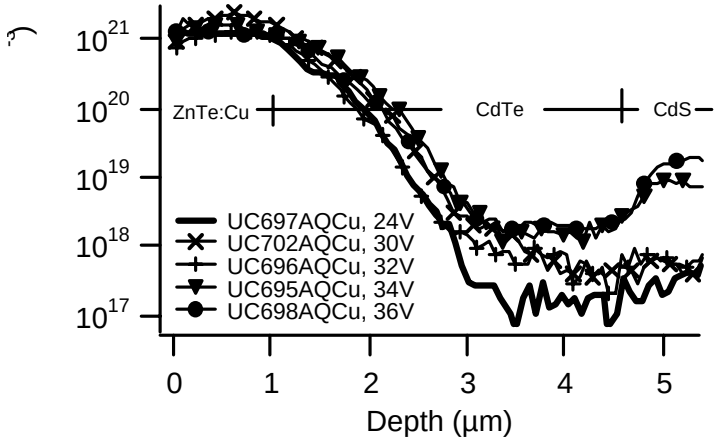
Tim Gessert, Caroline Corwine (CSU), Steve Johnston, Sally Asher, Tom Moriarty, Kurt Barth (CSU), Xuanzhi Wu, Pat Dippo, Matt Young, and Anna Duda

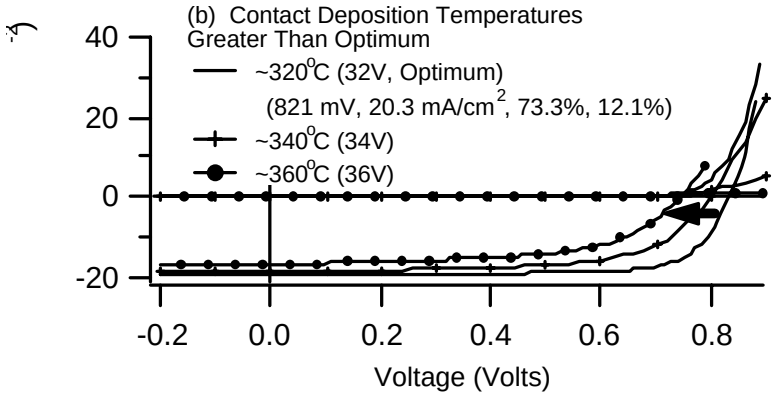
Some Effects of Cu Diffusion into CdS/CdTe/ZnTe:Cu/Ti Devices

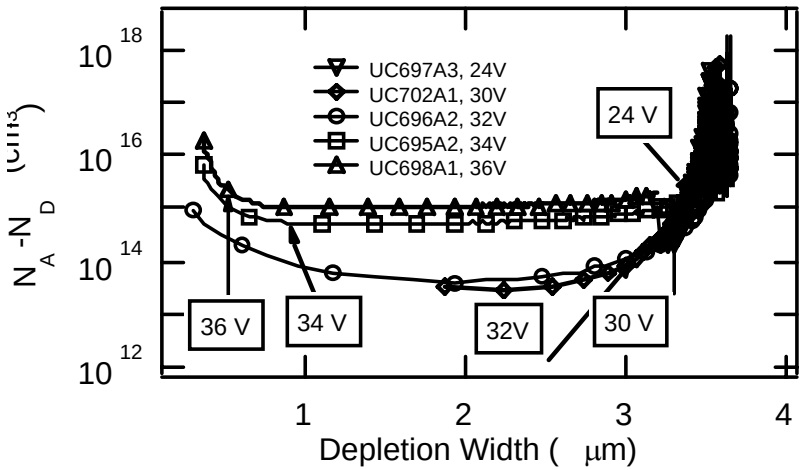
Data Presented in 31st IEEE PVSC

(Commercial VTD Material, 4.6 µm Thick)



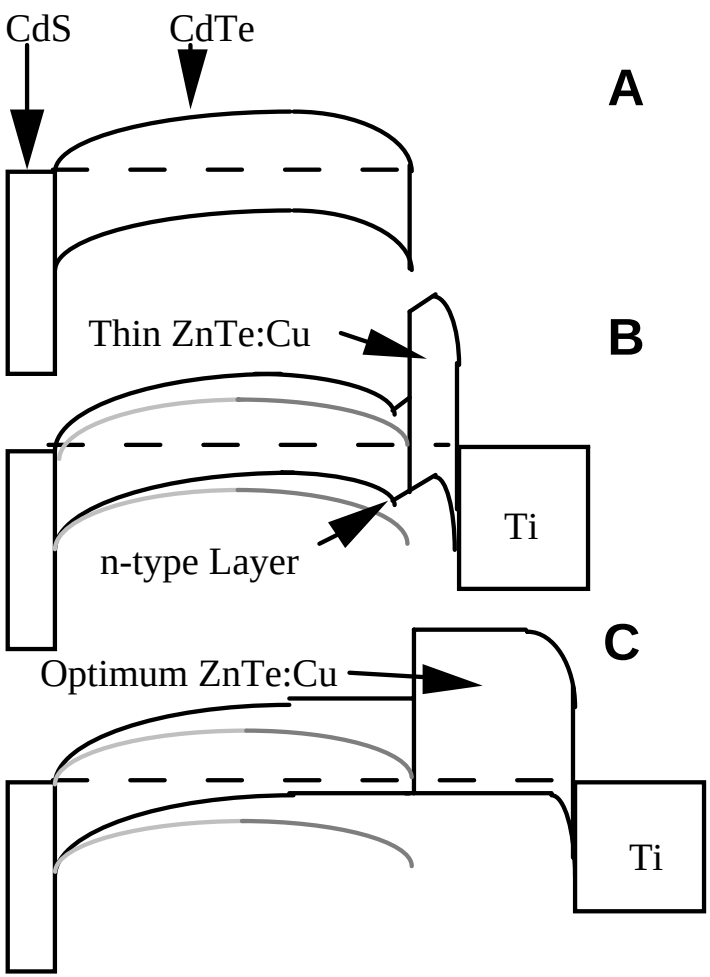


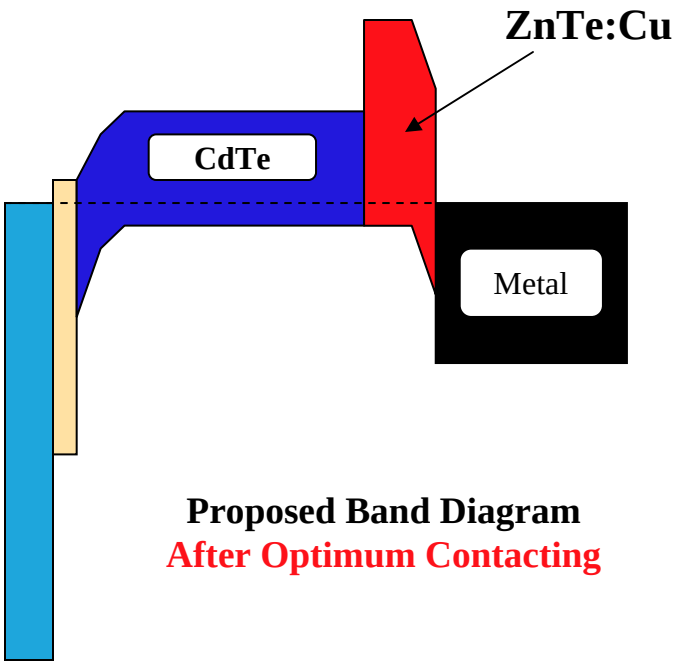




Tim Gessert

Evolution of CdTe During Contacting
(31st IEEE PVSC, pp. 291-294)





Proposed Band Diagram
After Optimum Contacting

Notes:

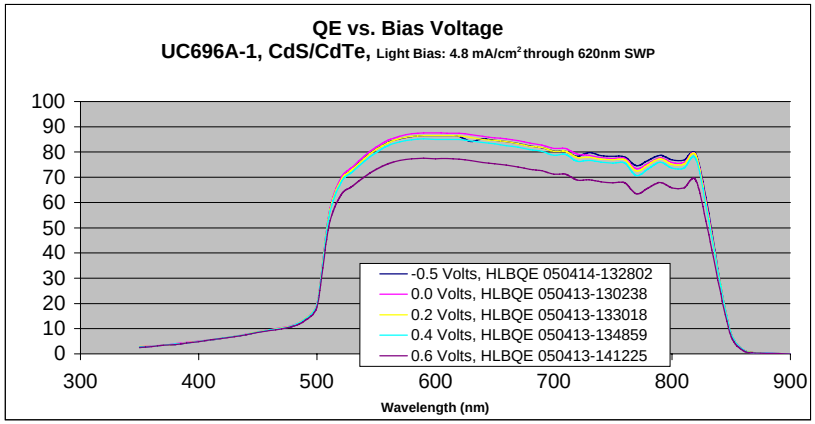
1. **Flat bands at back of CdTe.**
2. **Barrier at ZnTe:Cu/Ti interface tunneling (not thermionic emission)**

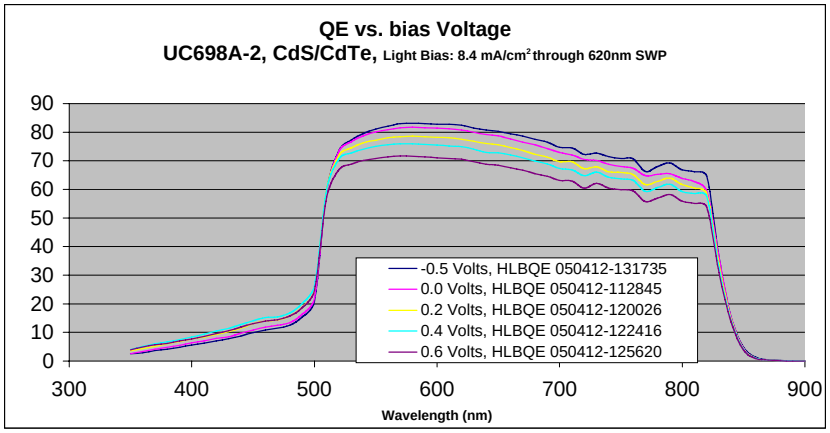
Some Recent Related Analysis

Devices with Optimum Cu (UC696)

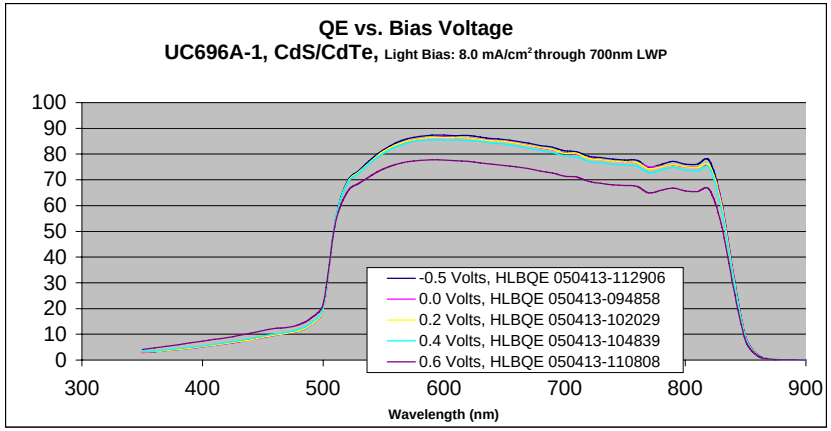
Devices with Excessive Cu (UC698)

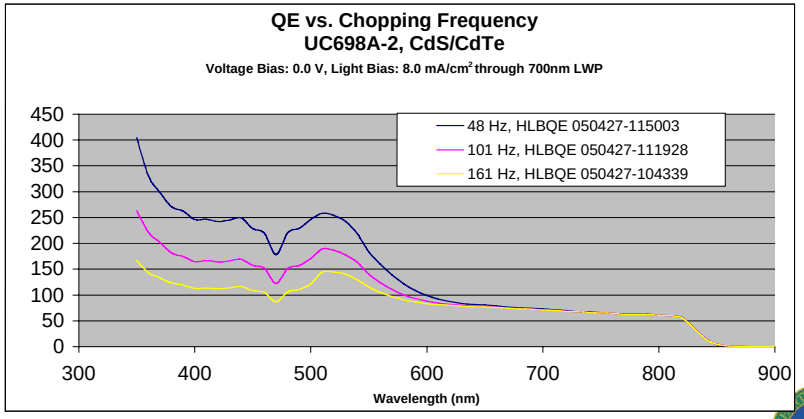
V-QE, Blue Light Bias





V-QE, Red Light Bias





Main Observations So Far:

1. **LIV/DIV/SIMS- Cu diffusion into CdTe during contacting correlates with significant voltage and FF increase - at least up to an "optimum" concentration of Cu**
2. **CV - Cu diffusion correlates with increase in acceptor level in CdTe.**
3. **VQE - Excessive Cu diffusion into CdS leads to photoconductivity effects, and possible donor compensation in CdS.**

Next Questions:

1. **Can the data so far form basis of a consistent model?**
2. **How accurate is this picture for device material other than Commercial VTD material?**

SCAPS Parameters Used *(Basic Bergelmann)*

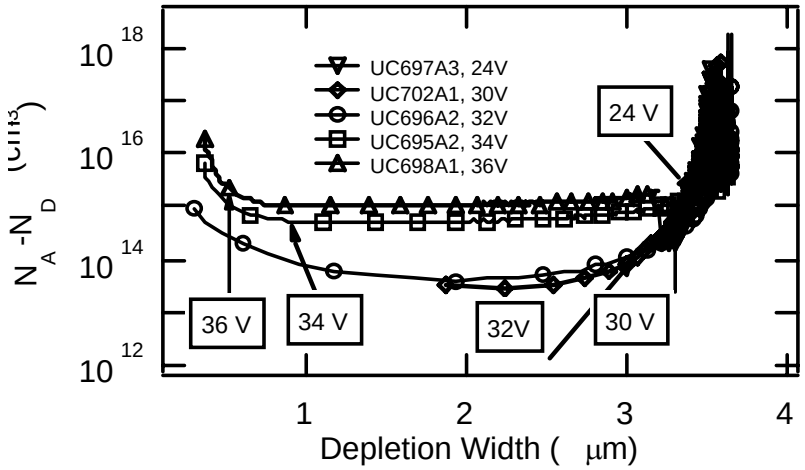
(Simple 2-layer Simulation, No Interface or Deep Defect States, Flat Bands at Contact)

CdS	
Thickness	0.3 µm
E_g	2.45 eV
X_e	4.5 eV
ε_o	10.0
N_{CB}	1.5e18 cm^{-3}
N_{VB}	1.8e18 cm^{-3}
V_{th} (electron)	1e7 cm/sec
V_{th} (hole)	1e7 cm/sec
µ(electron)	50 cm^2/V-sec
µ(hole)	20 cm^2/V-sec
Shallow n	1e17 cm^{-3} (Vary)
Shallow p	0
Absorption	9e5 cm^{-1}

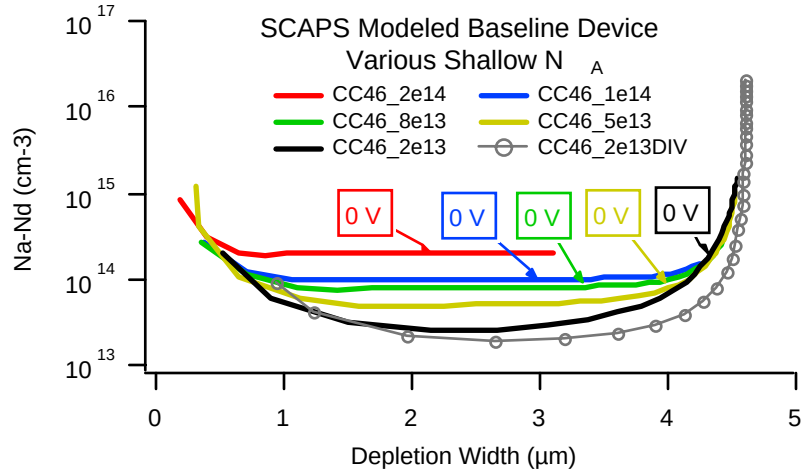
CdTe	
Thickness	4.5 µm or 1.8 µm
E_g	1.45 eV
X_e	4.3 eV
ε_o	10.0
N_{CB}	1.3e18 cm^{-3}
N_{VB}	7.6e18 cm^{-3}
V_{th} (electron)	1e7 cm/sec
V_{th} (hole)	1e7 cm/sec
µ(electron)	50 cm^2/V-sec
µ(hole)	30 cm^2/V-sec
Shallow n	0
Shallow p	2e14 cm^{-3} (Vary)
Absorption	File-CdTe.abs

SCAPS Modeling of Initial C-V Analysis

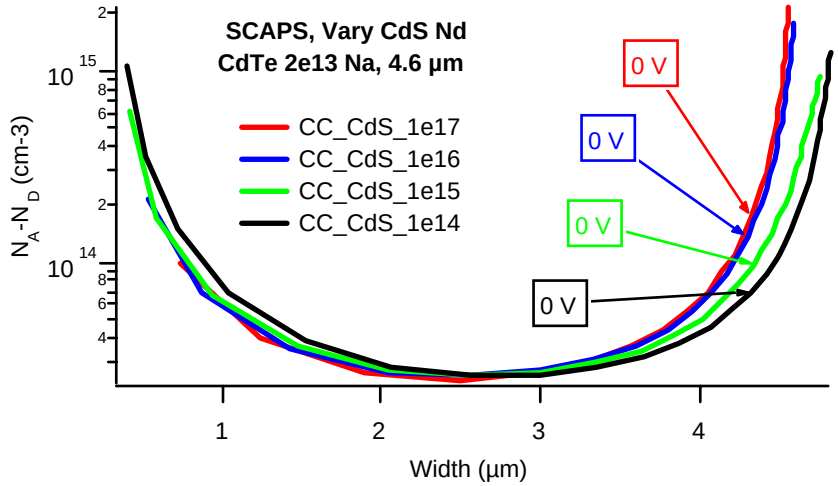
31st IEEE PVSC, pp. 291-294



SCAPS C-V Simulation
Various CdTe Shallow CdTe N_A



SCAPS C-V Simulation
Various Shallow CdS N_D

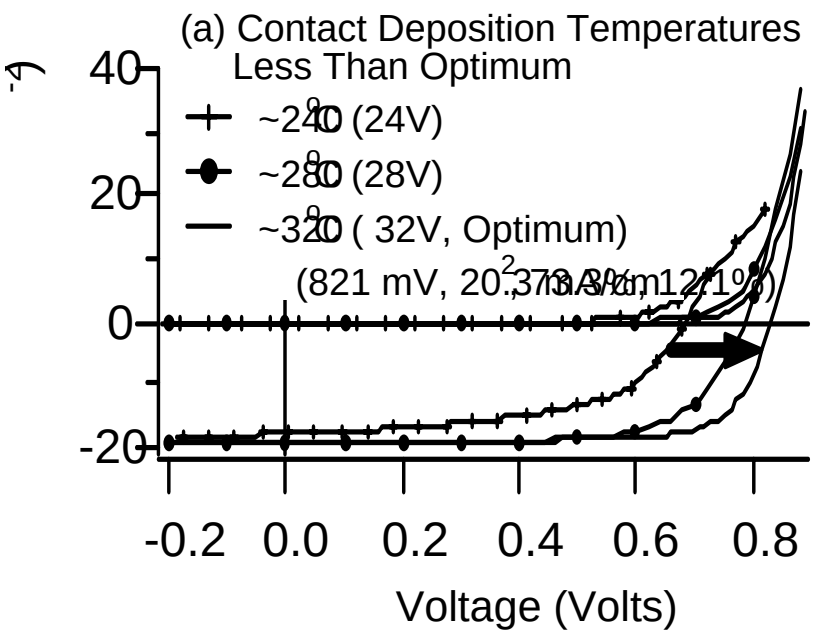


<u>Some Modeling Implications</u>

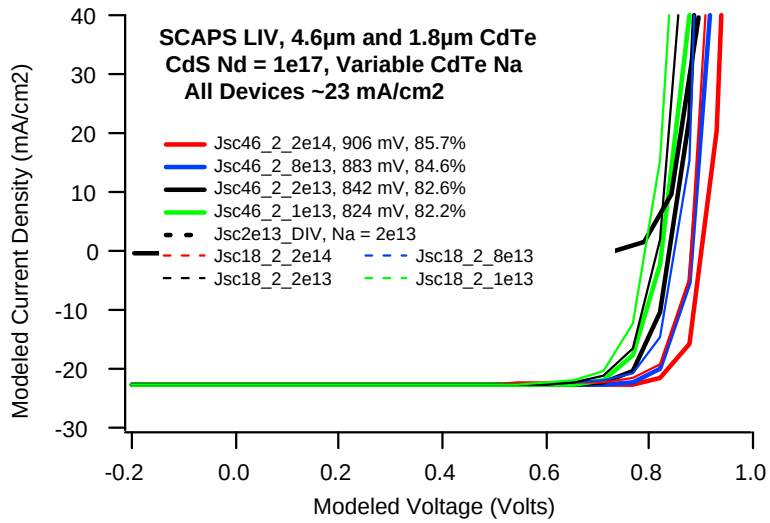
- **General C-V trends observed can be reproduced by simulating changes in CdTe N_A.**
- **For 4.6 µm CdTe, N_A values < ~1e13 cm^{-3} cannot be observed.**
- **CdTe N_A of ~2e13 cm^{-3} seems consistent for many cells.**
- **CdTe N_A of 1e15 cm^{-3} indicated for some cells.**
- **CdS N_D as low as 1e14 cm^{-3} shows little effect on depletion width for CdTe N_A of 2e13 cm^{-3}.**

SCAPS Modeling of Initial LIV/DIV

31st IEEE PVSC, pp. 291-294



SCAPS LIV Simulation
Various Shallow CdTe N_A
(4.6 µm and 1.8 µm CdTe)

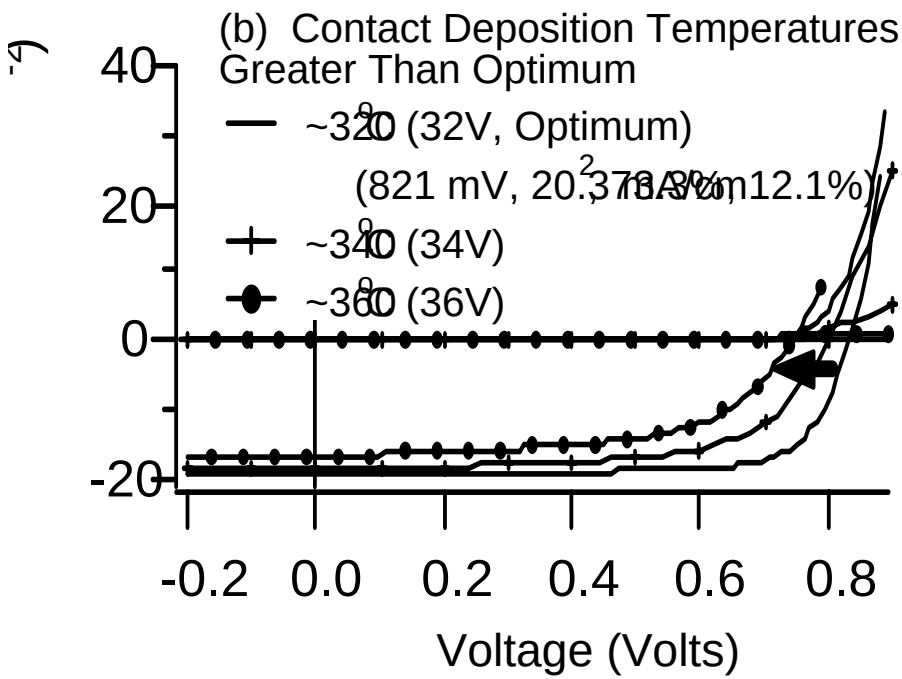


<u>Implications</u>

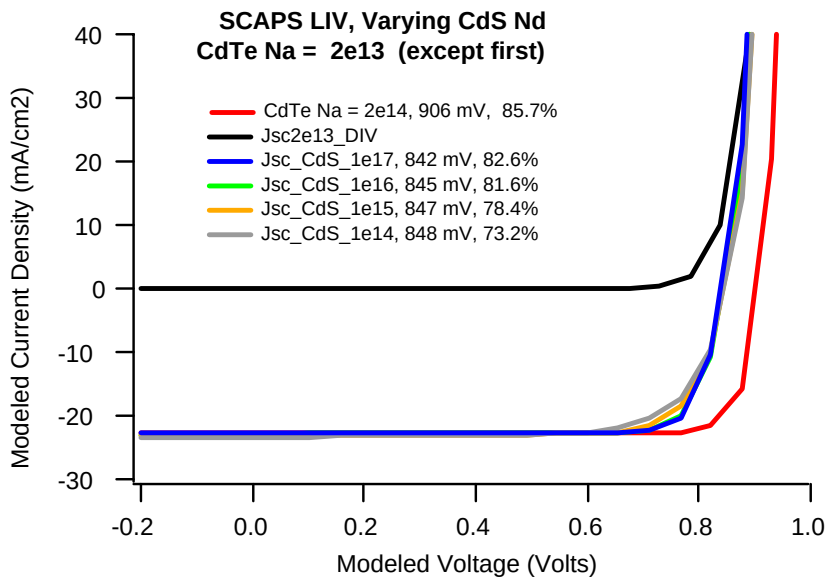
- **Simple 2-layer model with CdTe N_A of ~2e13 cm^{-3} yields approx. observed max V_{oc}**
- **1.8 µm devices may demonstrate ~40 mV less V_{oc} than 4.6 µm devices**

SCAPS Modeling of Initial LIV/DIV

31st IEEE PVSC, pp. 291-294



SCAPS LIV Simulation
Various Shallow CdS ND
(4.6 µm CdTe)



<u>Implications</u>

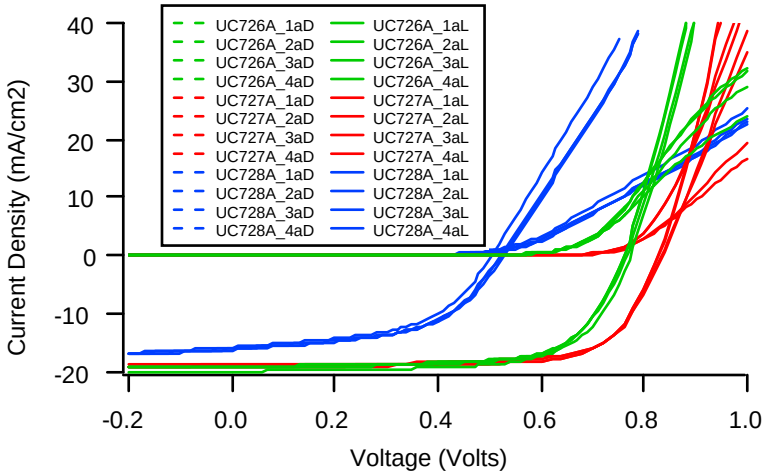
- **Reduction of CdS N_D from 1e17 to 1e14 cm^{-3} does not readily simulate LIV of devices with excessive Cu in CdS.**
- **Reduction of CdS N_D (by Cu) may manifest in FF more than V_{oc}**

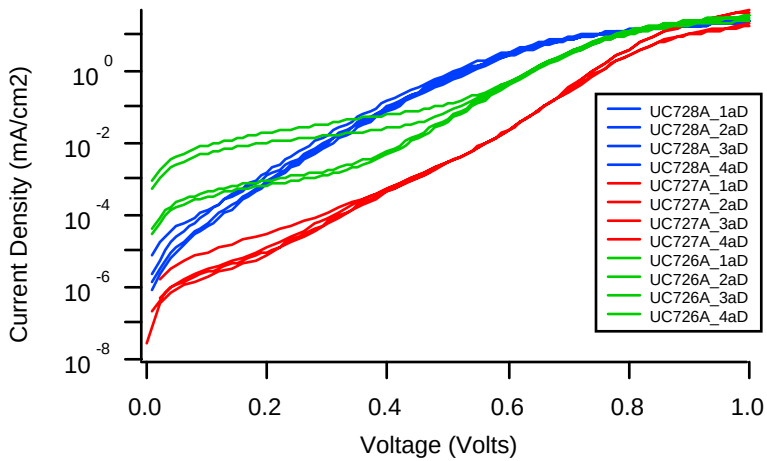
Initial Indications of LIV/DIV Difference Between Materials

Contact Temperature

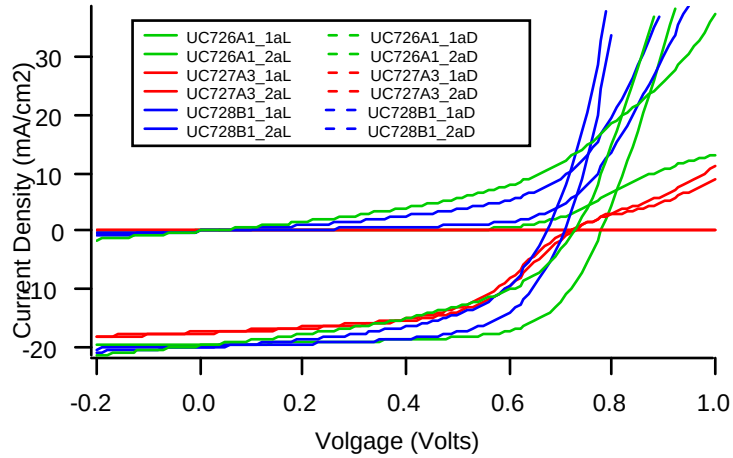
280°C
320°C
360°C

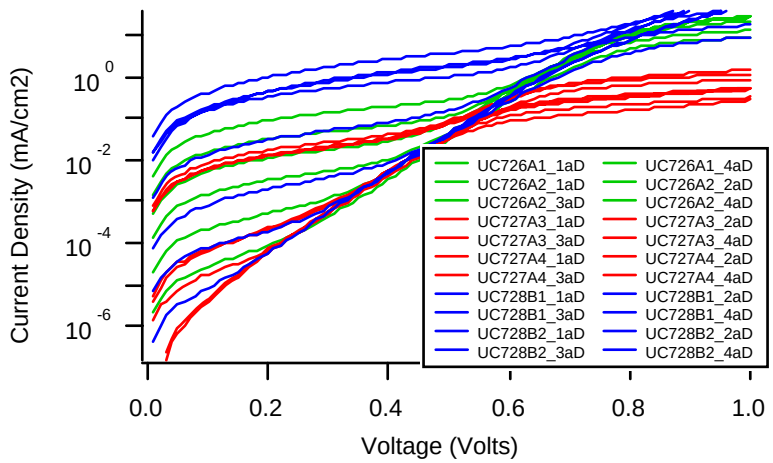
Commercial VTD Material





CSU Material



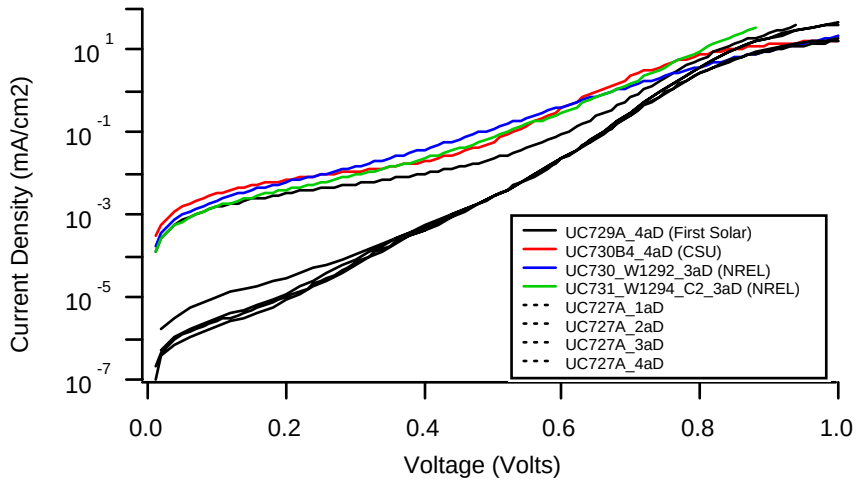


Tim Gessert
CdTe National Team Meeting - 3/9/06

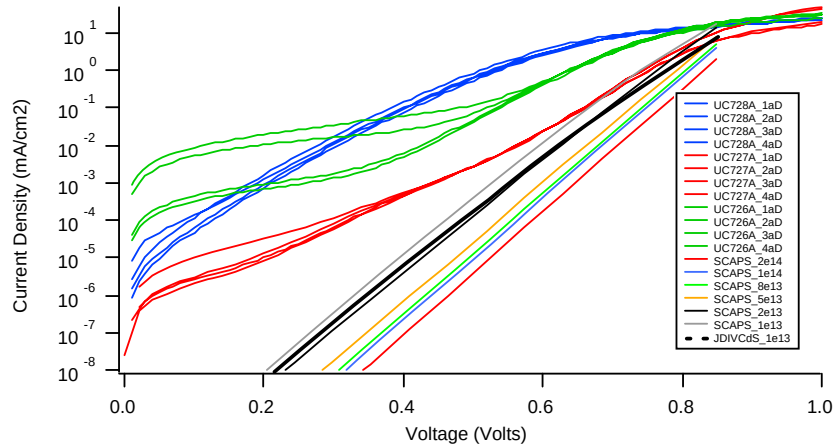
SCAPS Modeling of Initial LIV/DIV

SCAPS Simulation of DIV of Commercial VTD Material
Various Shallow CdTe N_A And Effect of Reducing CdS N_D to 1e15 cm-3

VTD, CSU, and NREL Best DIV Devices



VTD Device with SCAPS Simulation



<u>Implications</u>

- **Suggests general trends of both LIV (V_{oc}) and DIV parameters for 360°C reproduced with CdTe N_A = ~2e13 cm^{-3}.**
- **If devices with lower contact temps has much lower N_A, CV cannot observe.**

Recent Comparisons of VTD, CSU, and NREL CSS Materials

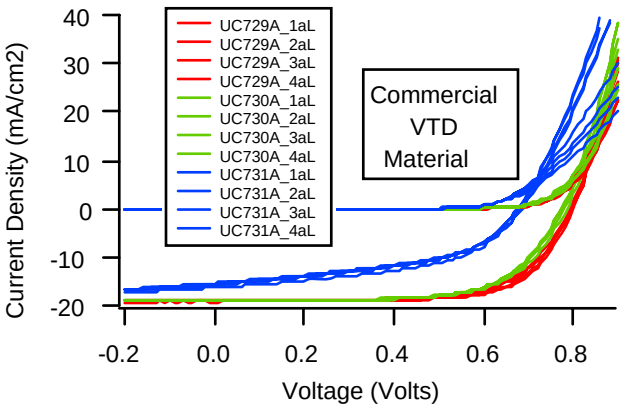
Contact Temperature

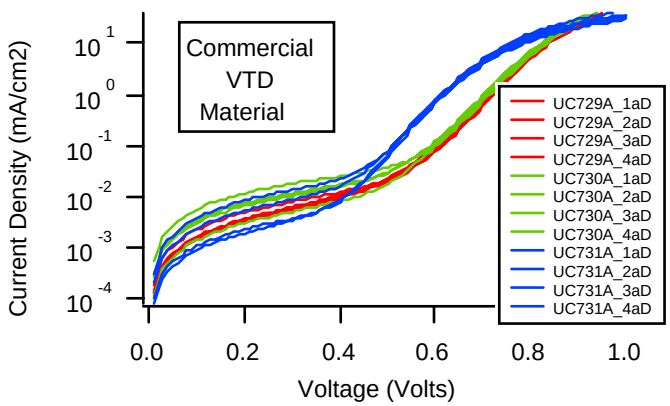
280°C

320°C

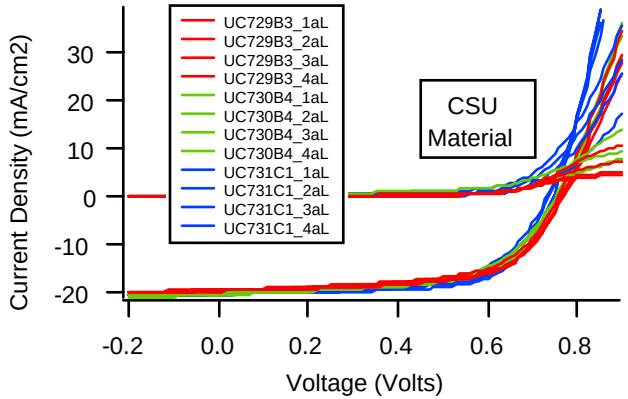
360°C

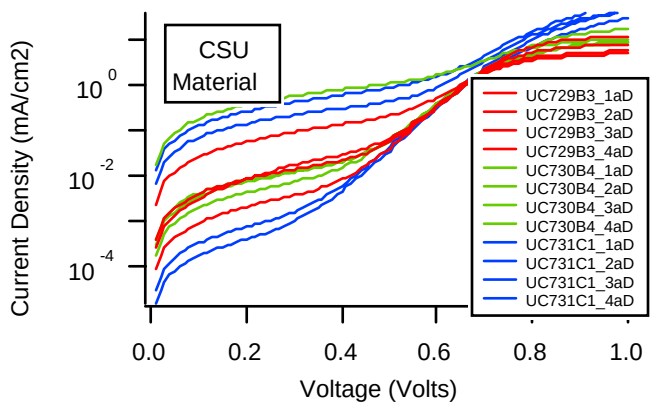
Commercial VTD Material





CSU Material





Tim Gessert

Recent Comparison of VTD, CSU, and NREL CSS Materials

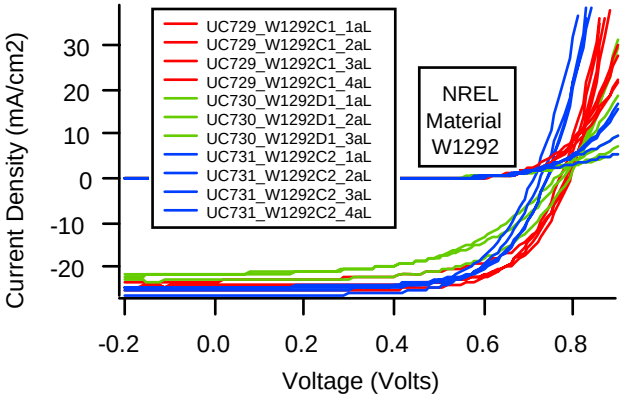
Contact Temperature

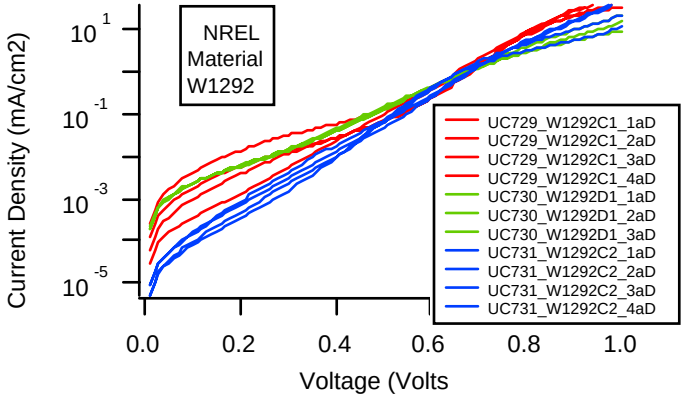
280°C

320°C

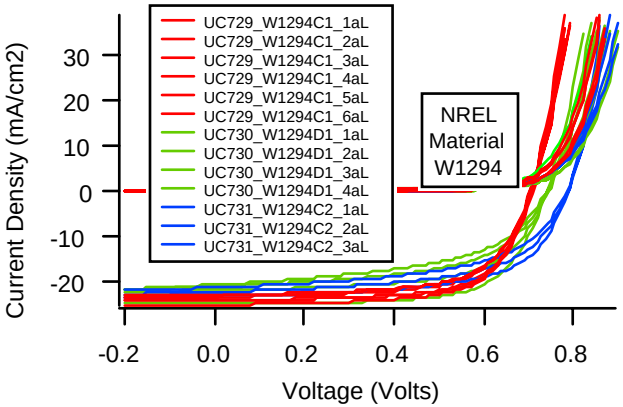
360°C

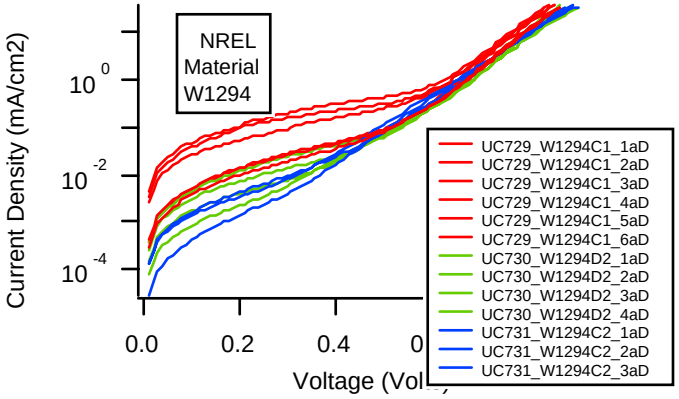
NREL CSS Material (Wu W1292)





NREL CSS Material (Wu W1294)

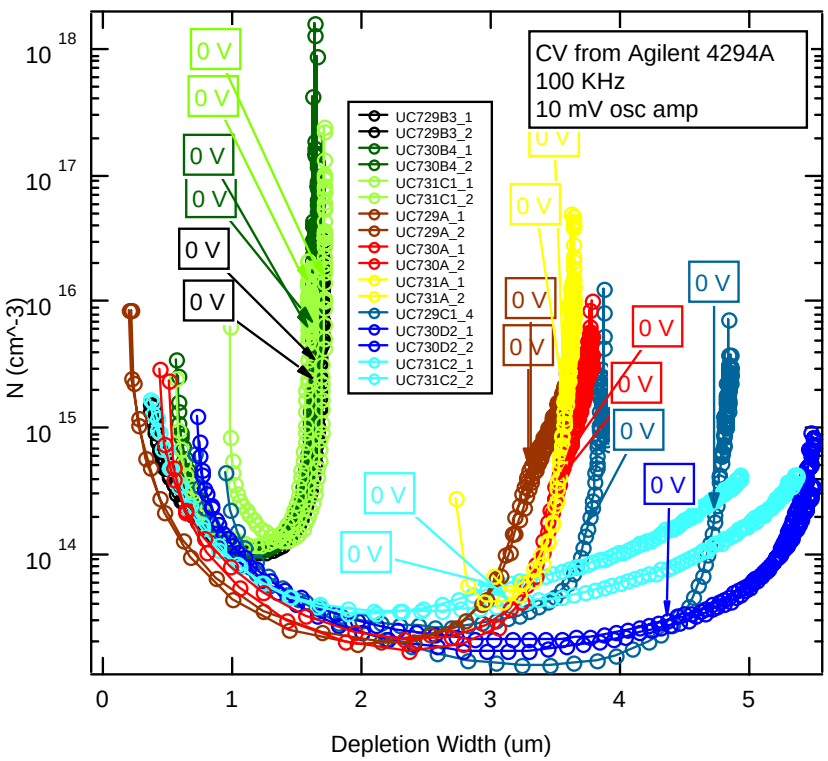




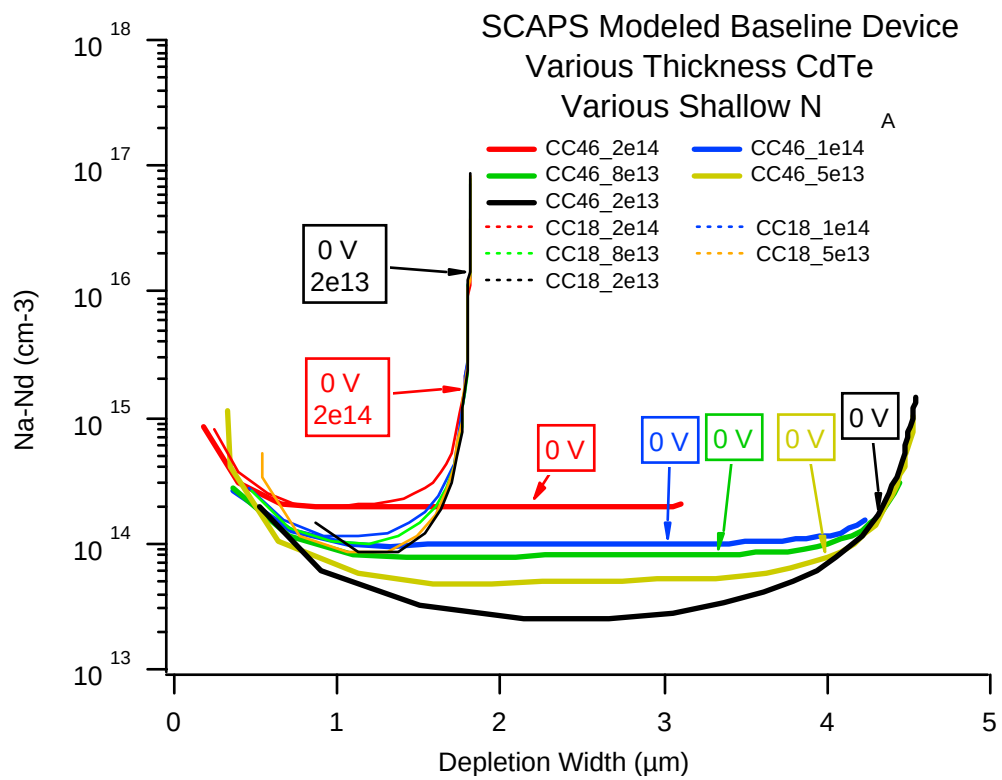
Tim Gessert

C-V Analysis of Commercial VTD, CSU, and NREL CSS

Data from Commercial VTD, CSU and NREL CSS Devices



SCAPS Simulated C-V Profiles



Observations/Implications

- **Lowest "C-V measurable" carrier concentration in CSU material by CV analysis may be only ~1e14 cm-3**
- **NREL material seems to loose free carrier with increasing contact temp.**

Some SIMS Observations / Comparisons

All Films
- *As-expected systematic increase of Cu concentration in CdTe with increasing contact temperature.
- *Systematically (and significantly) more Ti remaining on ZnTe:Cu surface as temperature increases. Surface reactions occurring.

VTD/NREL
- *As-expected increases of Cu concentration in CdS with increasing contact temperature.

CSU
- *Highest Cu concentration observed for both CdTe and CdS
- *No change in Cu concentration in CdS with temperature
- *Almost no oxygen in CdTe
- *Highest concentration of Cl near junction

Com. VTD
- *Significantly less Cu in CdS than for pervious studies at 360°C
- *Diffusion tail from ZnTe:Cu larger than for other samples?!

NREL
- *Lowest Cu concentration observed in both CdTe and CdS
- *Significant Cl at CdTe/ZnTe:Cu interface, except at 360°C

Conclusions

SCAPS Simulations

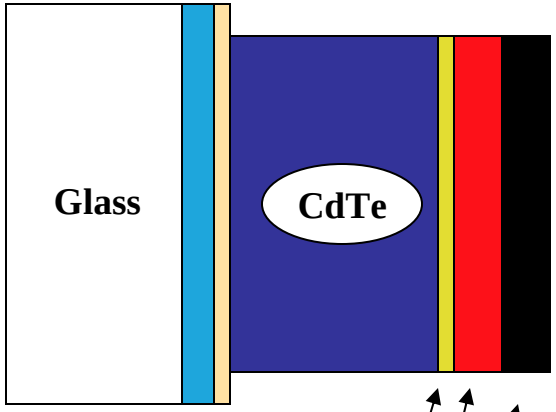
- **Simple 2-layer SCAPS model reproduces observed C-V trends well.**
- **Suggests CdTe N_A for most good 4.6 µm devices ~2e13 cm^{-3}.**
- **N_A for 1.8 µm devices < 1e14 cm^{-3} not observable.**
- **CdS N_D reduction to 1e13 cm-3 does not simulate observed CdS:Cu effects.**
- **Flat-band approximation at contacts seems appropriate for ZnTe:Cu/Ti contact, but need tunneling for simulation to approximate observed FF.**

Comparisons of NREL/VTD/CSU Devices

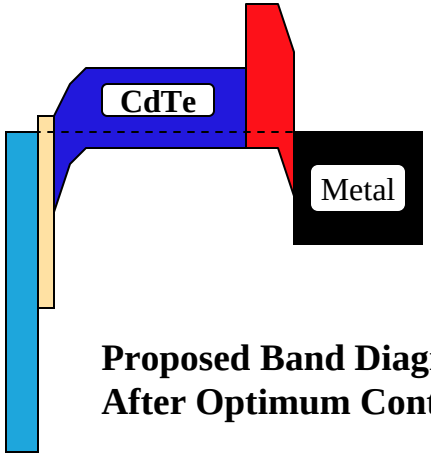
LIV/DIV *CSU - J_o does not evolve much during contacting
*VTD - J_o evolves during contacting
*NREL - J_o evolves slightly during contacting

C-V *CSU - N_A changes unclear. More simulation may help.
*VTD - N_A changes observed but small. ~2-4e13 cm^{-3} with temp.
*NREL - N_A decreases with increasing temperature. This is unexpected, but consistent with LIV for this particular device set.

Review ZnTe:Cu Contact Process



Photolithography
0.25 cm² Devices

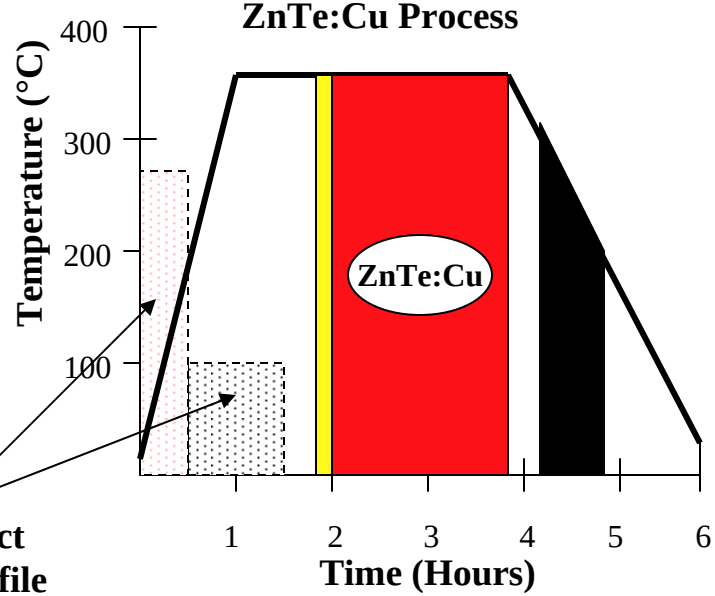


Proposed Band Diagram After Optimum Contacting

Contact Process Steps

- **Ion-Beam Mill (~0.1 µm)**
- **rf Sputter ZnTe:Cu (~1 µm)**
- **dc Sputter Ti (~0.5 µm)**
- **Photolithographic Process**

Temperature Profile of ZnTe:Cu Process



Paste Contact Thermal Profile

Piezo-effect in CdS-based solar cells

Presented by Diana Shvydka

Contributions by
Jennifer Drayton and Mukut Mitra

University of Toledo

Outline

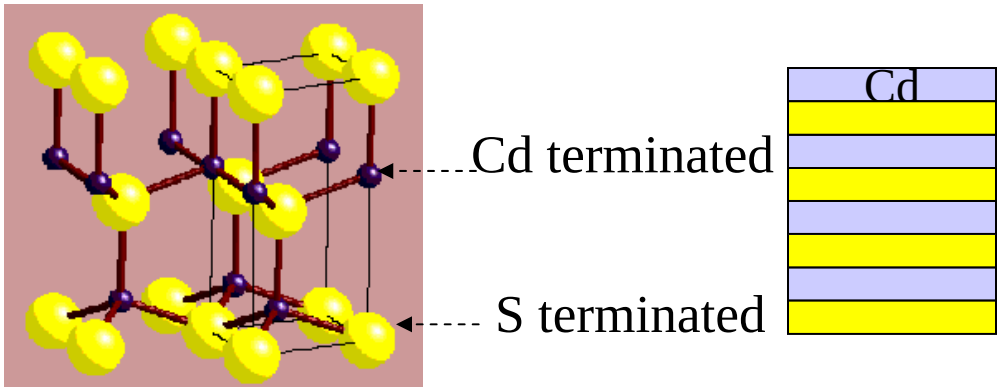
- Motivation
- Pressure (stress) dependence of PV parameters
  - glass and flexible substrate
  - normal pressure and lateral compression (bending)
  - CdTe and CIGS - based cells
- $CdCl_2$ treatment in external field
- Summary and future work

Motivation

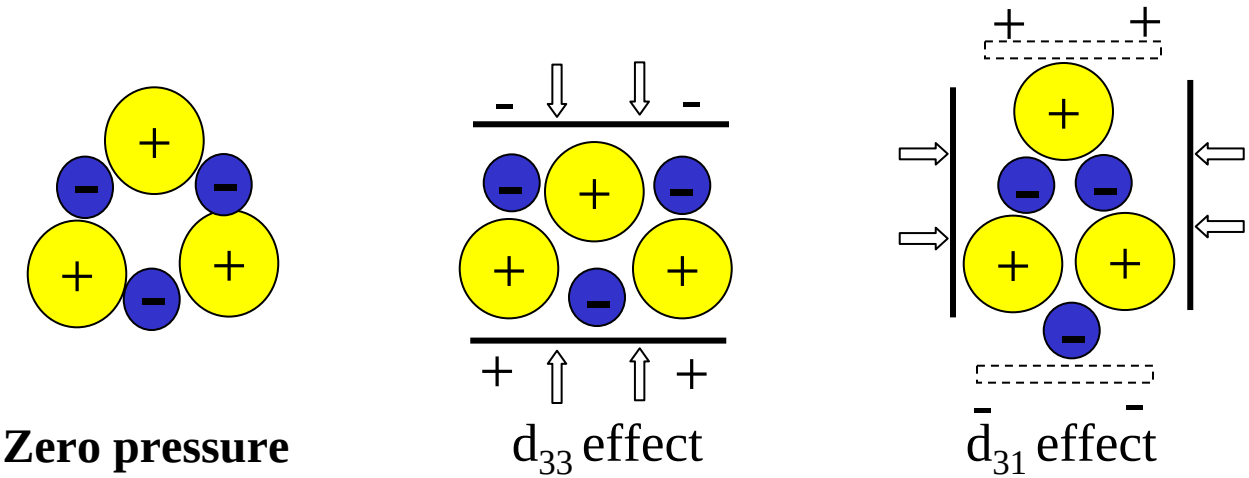
- Strong piezo-effect in CdS known since 1950's; both in crystals and thin films
- Observed pressure dependent PV in CdS-based cells
- Significant consequences for PV:
  - Insulating CdS
  - Strong electric field and potential drop across CdS
  - CdS grains being electric dipoles
  - Role of internal stress in device manufacturing

Nature of piezo-effect in CdS

- Hexagonal CdS
- No inversion symmetry
- Significant ionicity



Piezoelectric constants, in 10^{-12} C/N: d_{31}=-5.18, d_{33}=10.32, d_{15}=-13.98

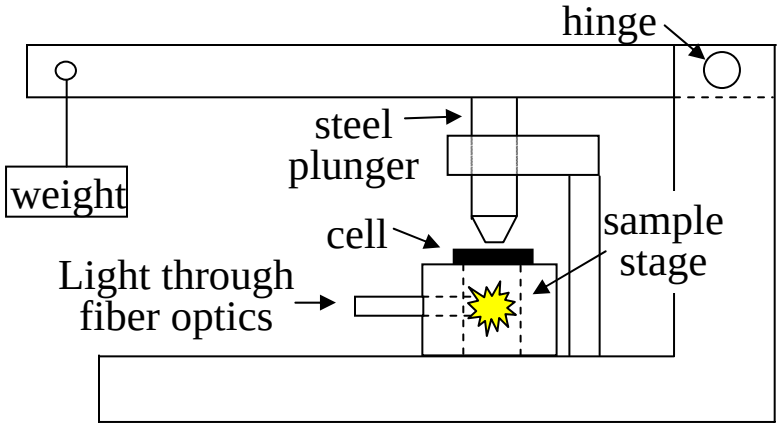


Pressure (stress) application experiments

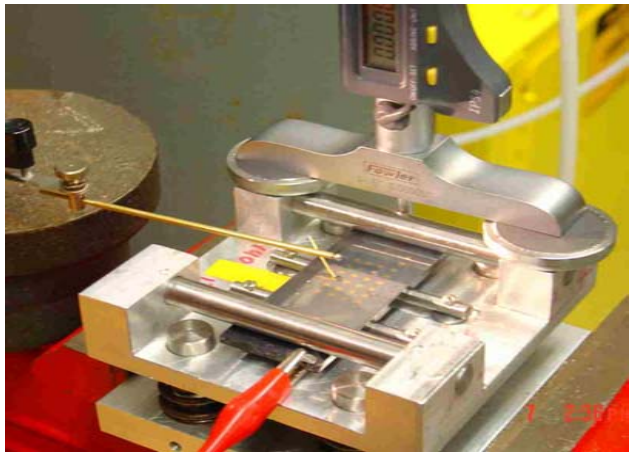
- Glass substrates: perpendicular and lateral to the film plane
- Flexible substrates: in the lateral direction
- Samples: mostly CdTe-based solar cells, some CIGS
- Main observation: reversible changes of PV parameters under pressure

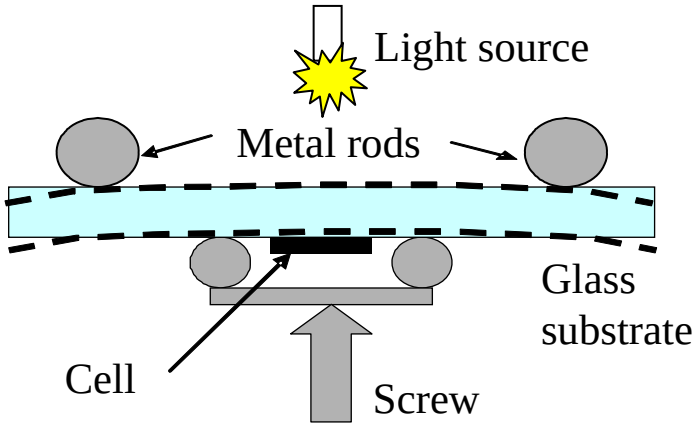
CdTe solar cells on glass substrate

Normal Pressure Application



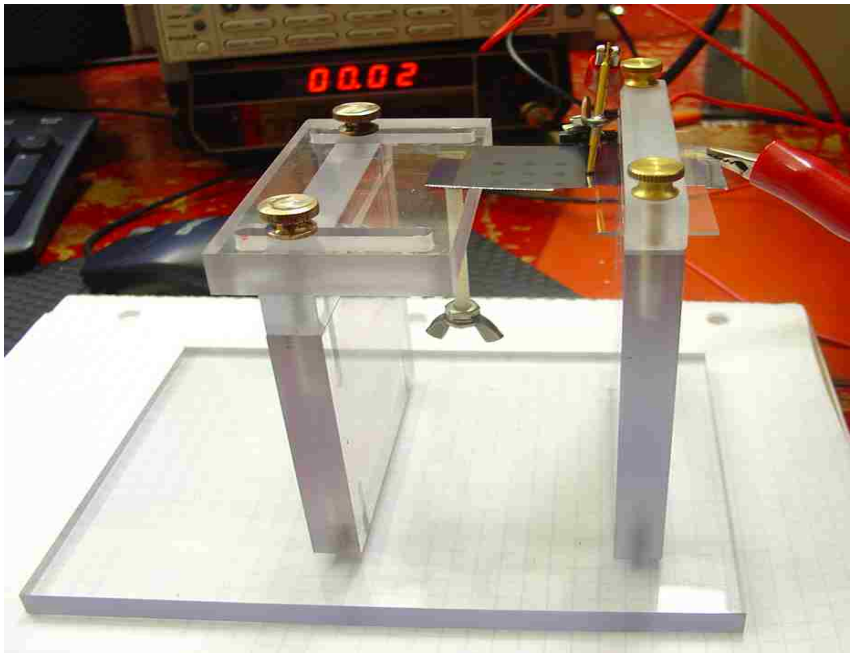
Lateral compression (bending, MOR-type)

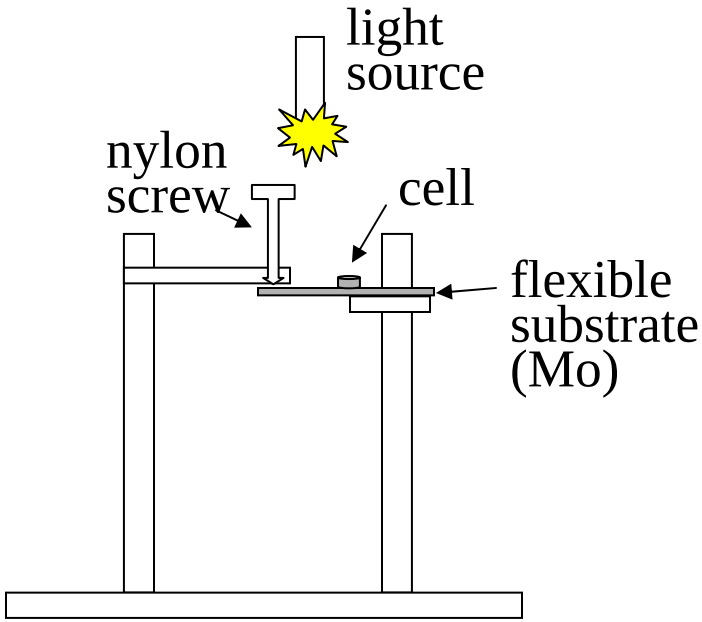




CdTe solar cells on flexible substrate

Lateral compression (bending)



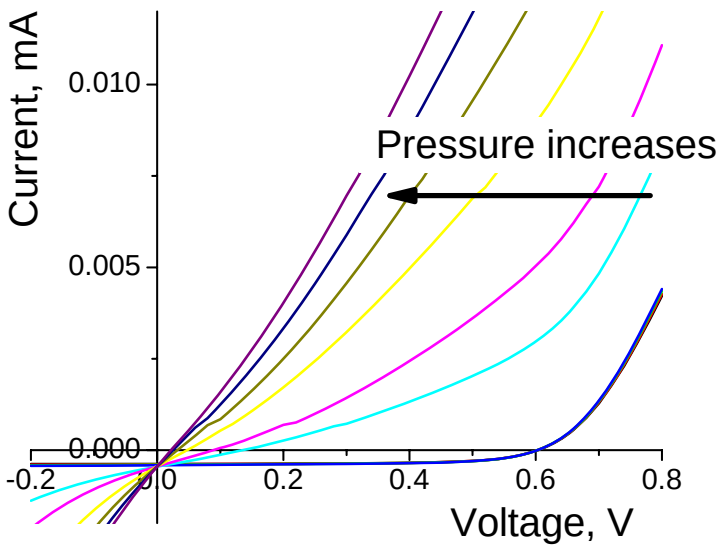


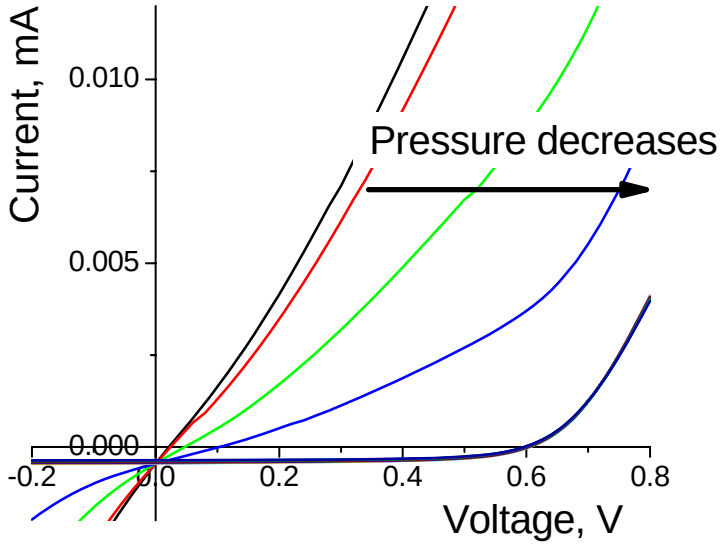
Seemingly the most natural setup, however:

-- lower initial cell efficiencies

-- inelastic effects after several bending cycles

Pressure dependent JVs in CdTe cells
(normal pressure application)

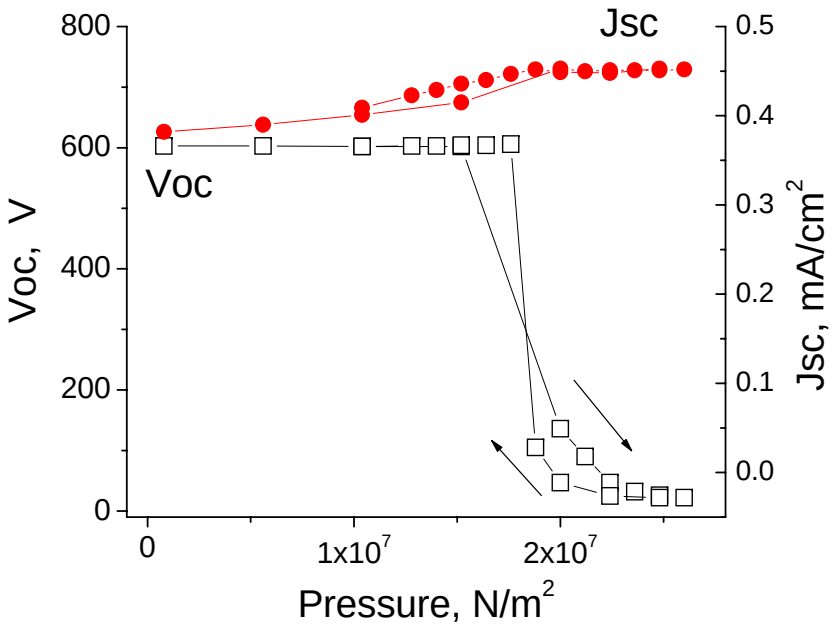




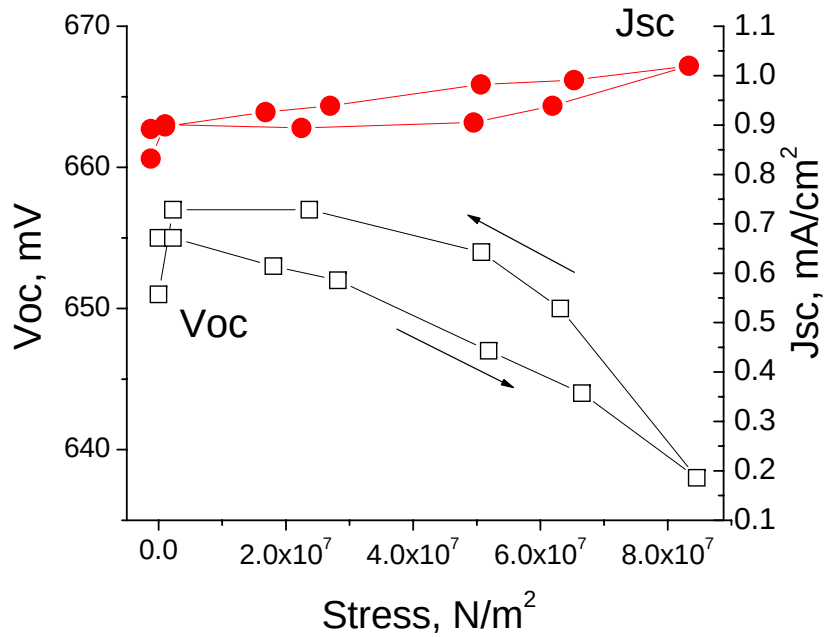
- Reversible changes in J-V through multiple cycles
- Effect is stronger for lower light intensity
- Different recipes show similar behavior

Pressure dependent PV : CdTe cells on glass substrates

One full cycle; light intensity ~ 0.01 Sun



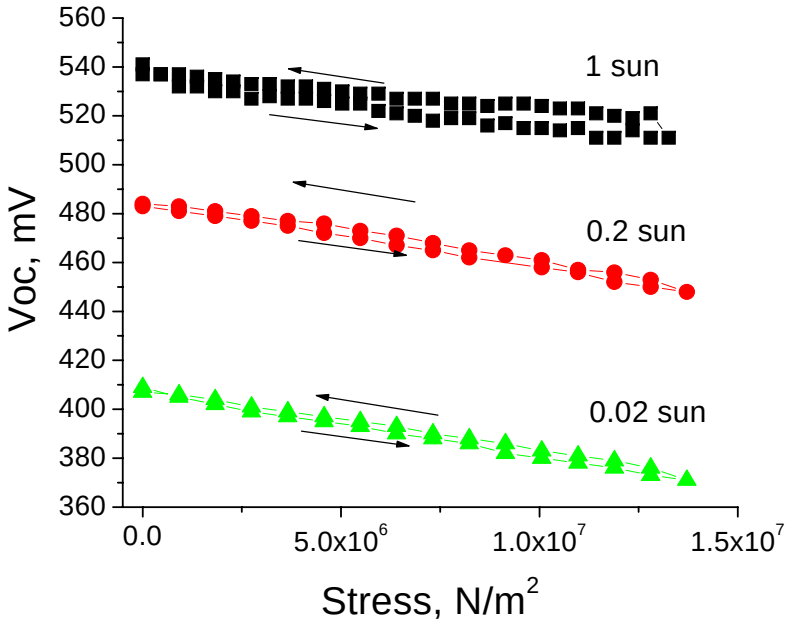
Normal pressure application

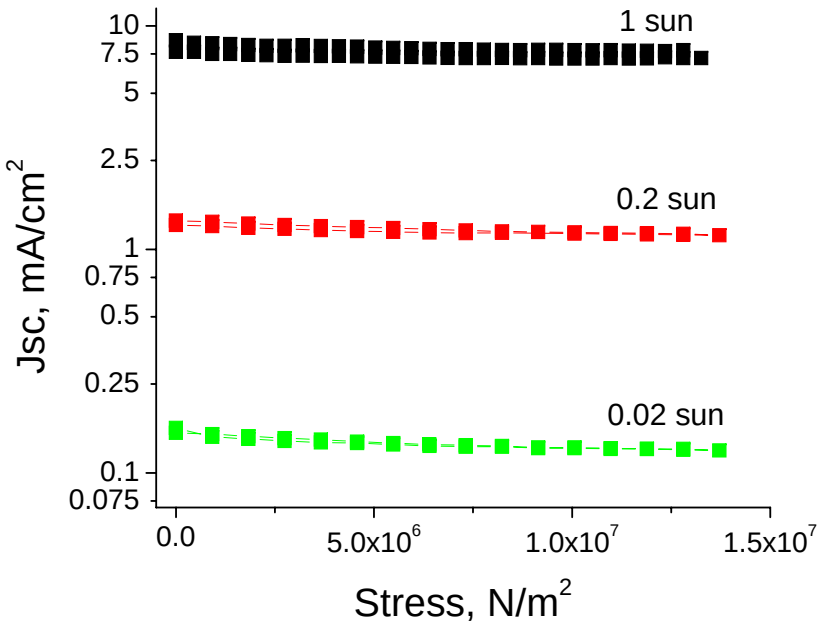


Lateral compression (bending, MOR-type)

Pressure dependent PV : CdTe cells on flexible substrates

Cells supplied by A. Vasko

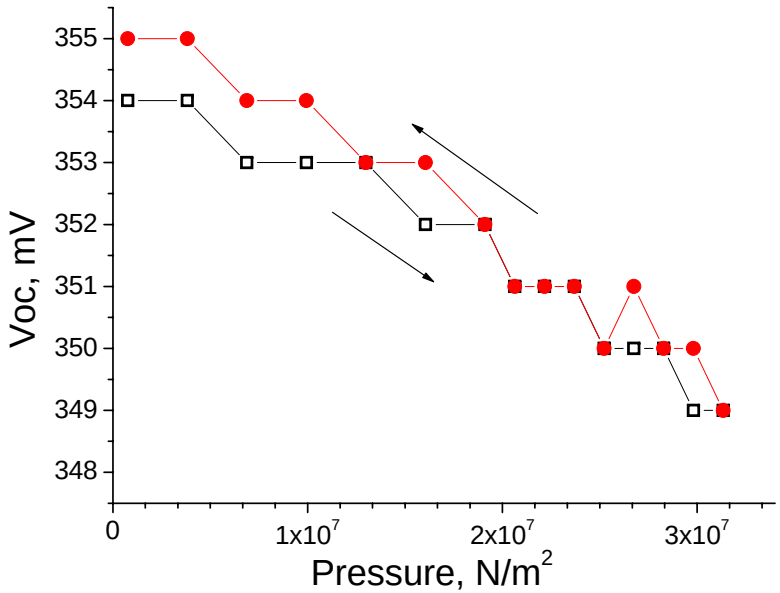


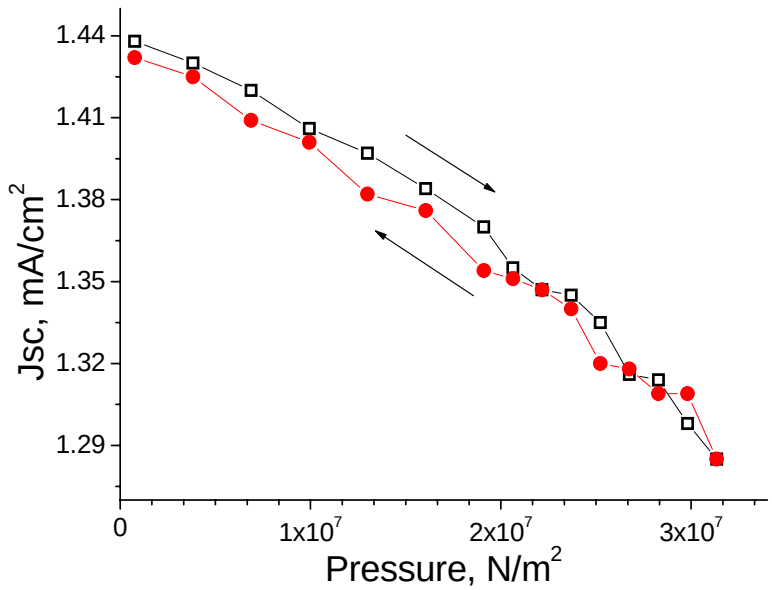


- Full cycle for each light intensity
- Effect is more pronounced at lower light intensity
- Film cracking problem: irreversible changes after several cycles

Pressure dependent PV : $CIGS_2$ cell on thin glass substrate

Cells supplied by S.X Marsillac





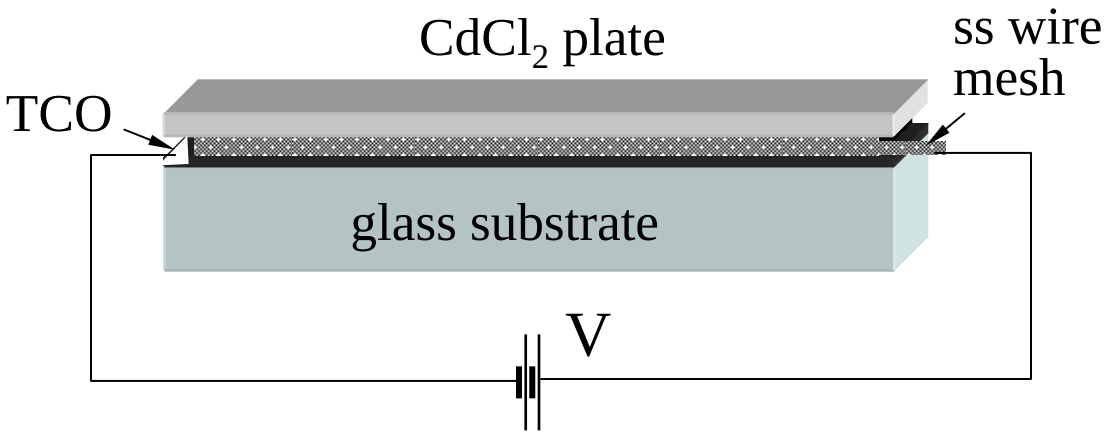
One full cycle; light intensity ~ 0.01 Sun

Effects weaker than in CdTe-based cells:

-- CdS is 3 times thinner

-- substrate configuration, shadowing and weak diode effect

$CdCl_2$ treatment under external bias (aligning CdS dipoles)



- Vapor $CdCl_2$ treatment at 387°C for 30-35 min
- Wire mesh used as the top contact to provide O_2 access
- Voltage range ±3V, ±6V, OC, SC
- Bromine-methanol etch to make surface look the same
- Au contacts, no Cu, no post-metal diffusion

$CdCl_2$ treatment under external bias (aligning CdS dipoles)

- Results are mixed
- Forward bias rather beneficial
- Technical problems with field application (leakage, shunting, device structure evolving in time, necessity to supply O_2 , etc.)
- Other effects superimposed (back surface changes, electro-diffusion, etc.)

Example: ~ 40 cells for each condition

Parameter	No Bias	Bias + 6V	Bias - 6V	Short Circuit
Voc, V	0.799 ± 0.047	0.768 ± 0.015	0.734 ± 0.04	0.727 ± 0.021
Jsc, mA/cm^2	20.49 ± 0.41	21.2 ± 0.55	19.94 ± 0.58	20.04 ± 0.47
FF, %	59.76 ± 3.80	63.15 ± 1.38	62.59 ± 2.72	62.93 ± 1.84
Eff, %	9.83 ± 1.03	10.28 ± 0.38	9.18 ± 0.76	9.79 ± 2.10

Summary

- Strong reversible pressure dependence confirmed in all types of CdS based cells
- Attributable to CdS piezo-effect
- Implies certain features of CdS in device model
- Suggests new venues in device manufacturing
- Future work
  - treatments under electric field and light bias
  - intentional CdS compression
  - quantitative understanding

Study of CdS/CdTe junction by modulated reflectance

Unpublished results

R. Dhere, Y. Zhang, M. Romero, S. Asher

Acknowledgement – X. Wu, K. Ramanathan, T. Gessert, T. Coutts, D. Albin, H. Moutinho, A. Mascarenhas

NREL

Junction Studies

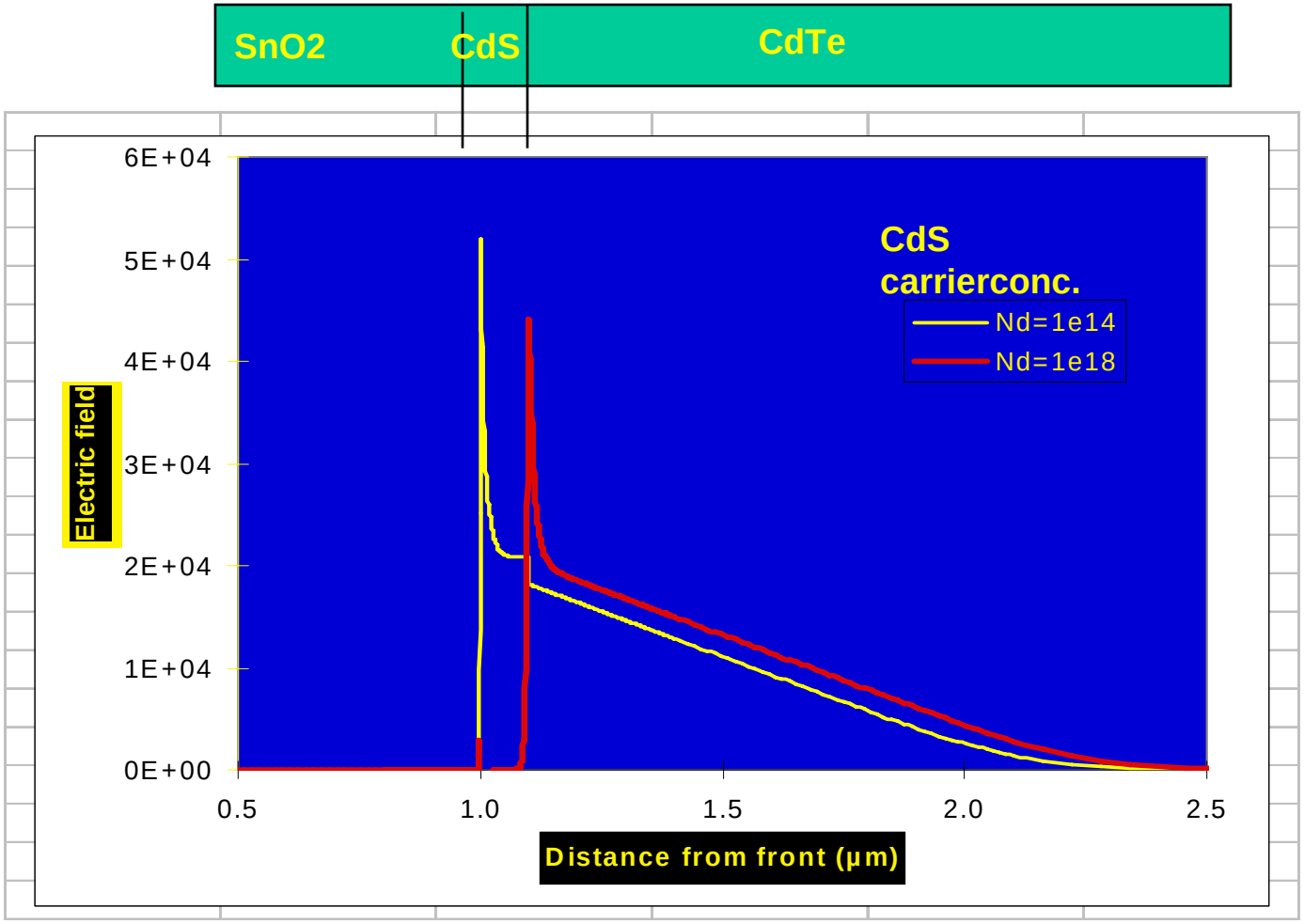
•Understand the nature of the junction in the CdTe/CdS device

Background:

n^+-p device model for CdS/CdTe device (6/95)- based on blue QE loss:

- One sided junction with depletion width entirely in CdTe.
- Only field assisted collection.

(Published in IEEE 97)


SnO2
CdS
CdTe
CdS
carrierconc.
Nd=1e14
Nd=1e18
Electric field
6E+04
5E+04
4E+04
3E+04
2E+04
1E+04
0E+00
0.5
1.0
1.5
2.0
2.5
Distance from front (µm)

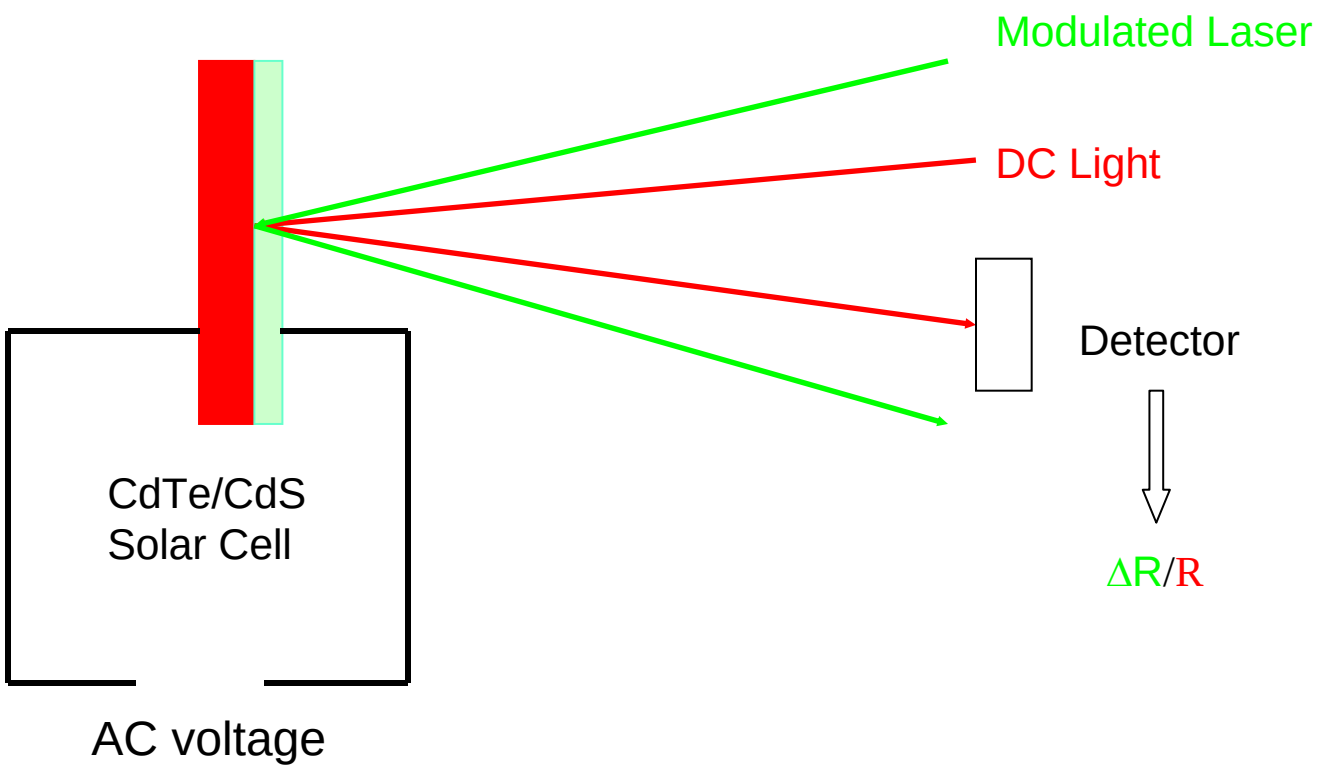
Problems with the n^+-p model

•Phenomenological Model – can explain the device performance but without physical basis.

•CBD CdS has carrier concentration around $10^{13}/cm^3$ which is even less than CdTe.

Modulated electro-reflectance and photo-reflectance technique allows the measurement of high electric fields (in 10's of kV). Can be useful for the validation of n^+-p model.

Photo- or Electro-Modulated Reflectance (PR or ER)



Reflectance modulation

$$R = \left| \frac{n - n_a}{n + n_a} \right|$$

$n^2 = \varepsilon_1 + i\,\varepsilon_2$, $\quad n_a^2 = \varepsilon_a$ (real)

$$\frac{\Delta R}{R} = \mathrm{Re}\left(\frac{2n_a}{n(\varepsilon - \varepsilon_a)} \Delta\varepsilon \right) = \alpha \Delta\varepsilon_1 + \beta \Delta\varepsilon_2$$

α and β are Seraphin coefficients.

Near band-gap, $\alpha >> \beta \Rightarrow$ major contribution is from $\Delta\varepsilon_1$:

$$\frac{\Delta R}{R} \approx \alpha \Delta\varepsilon_1$$

Fitting Modulation Reflectance Spectrum

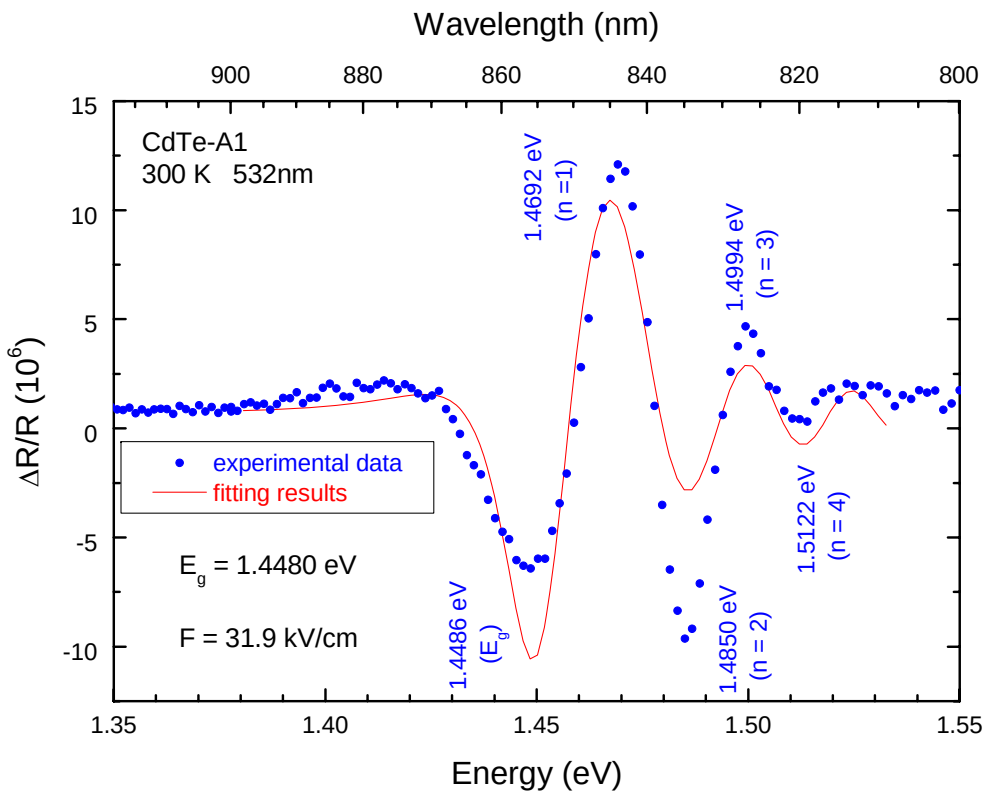
$$\Delta\varepsilon_1 = \frac{2e^2\eta^2 \,|\, \vec{e}\cdot\vec{P}_{cv} \,|^2}{m^2(\eta\omega)^2}\left(\frac{2\mu_0}{\eta^2}\right)^{3/2}\sqrt{\eta\Omega_0}\left(G\left(\frac{E_g-\eta\omega}{\eta\Omega_0}\right)-\sqrt{\frac{E_g-\eta\omega}{\eta\Omega_0}}F\left(\frac{E_g-\eta\omega}{\eta\Omega_0}\right)\right)$$

$$F(\eta) = \pi[A_i'^2(\eta) - \eta A_i^2(\eta)]$$

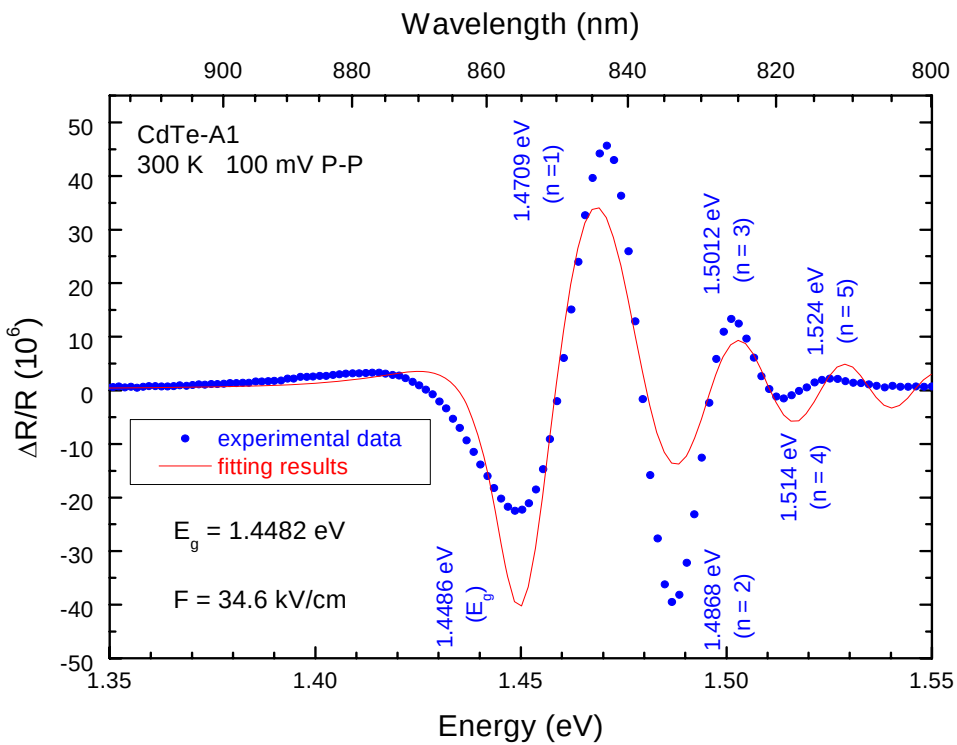
$$G(\eta) = \pi[A_i'(\eta)B_i'(\eta) - \eta A_i(\eta)B_i(\eta)]$$

Shen & Pollak, Phys. Rev. B 42, 7097 (1990)

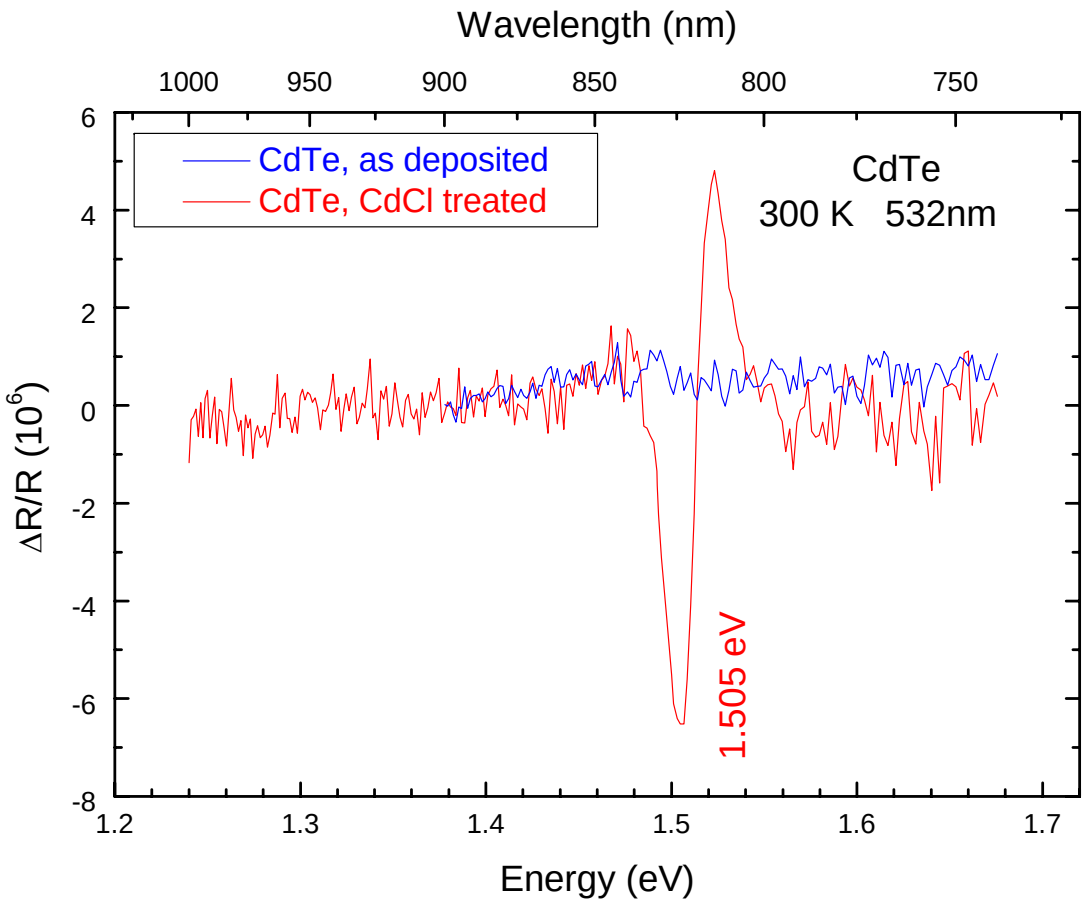
Photo-reflectance



Electro-reflectance



Effect of CdCl treatment (by PR)



Modulated Reflectance

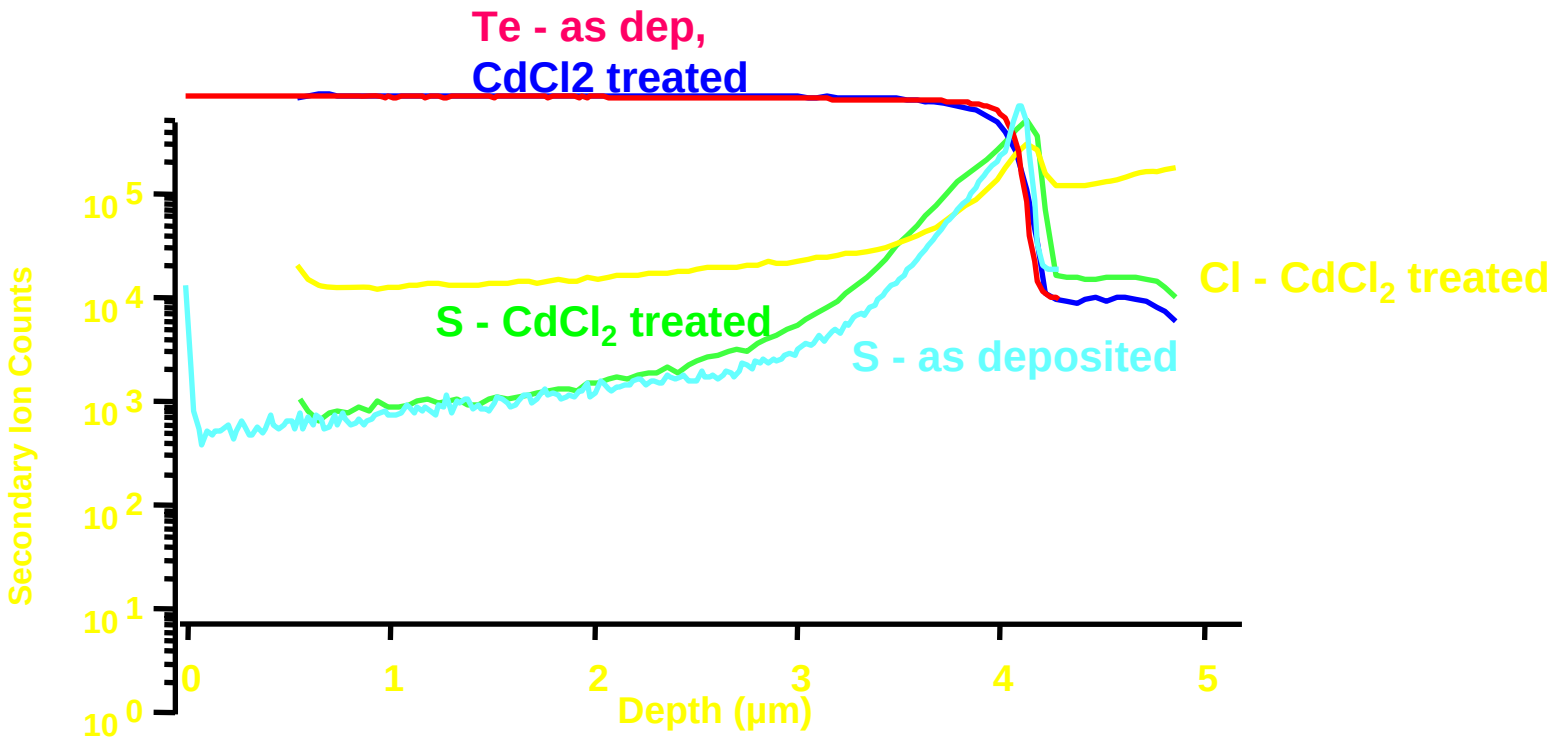
- Modulated electroreflectance and photoreflectance studies identify a region of high electric field (~32-35 kV/cm) for high efficiency CdS/CdTe devices. The field is present in the region of 1.45 eV material.
- SnO_2/CdTe devices do not show high field region

The high field region corresponds to Te-rich CdSTe alloy.

From E_{max} = 32 kV and
depletion width on p-side = 3 μm

Using $E_{max} = qN_AX_p/\varepsilon_s$
Gives $N_A = 5.5\text{x}10^{14}$ cm^{-3}

Evaluation of N_D based on SIMS and EBIC results

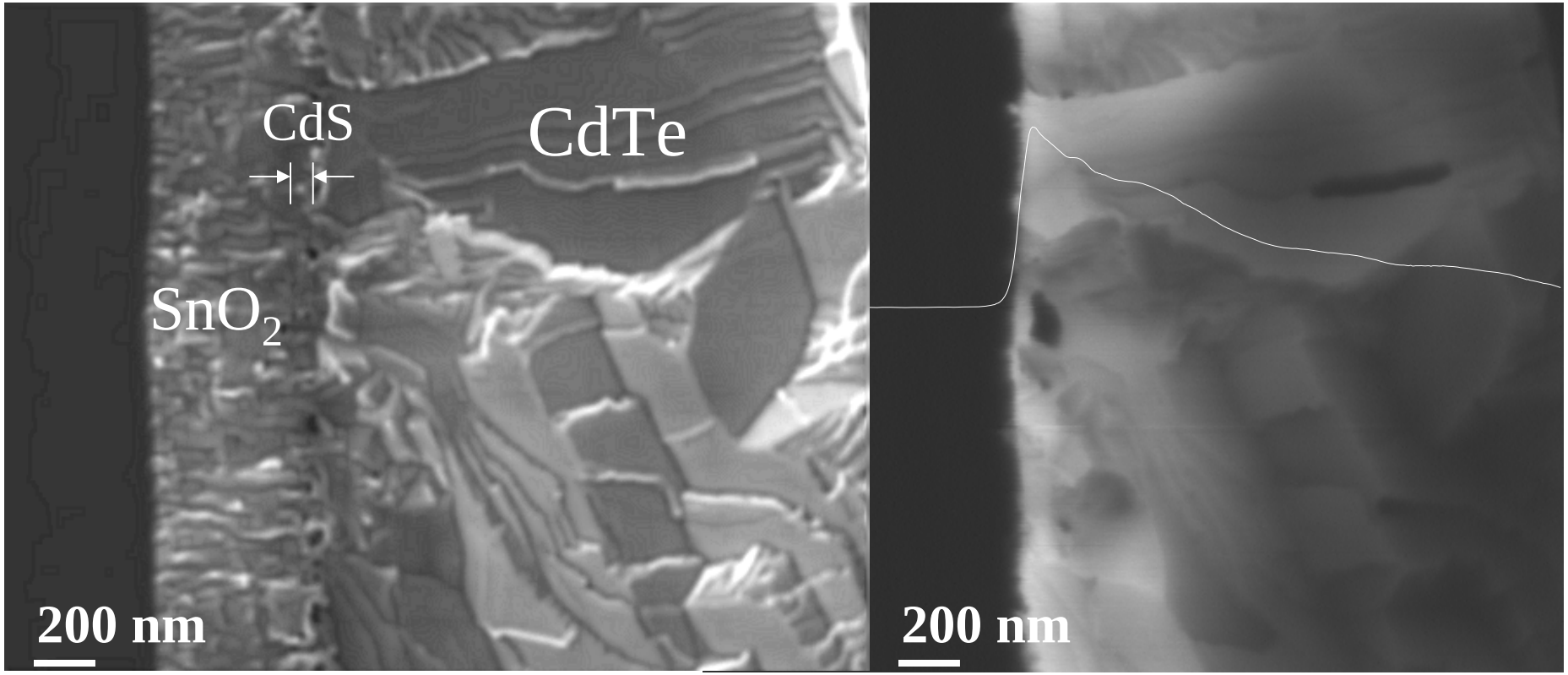


SIMS depth profile of sample deposited at 600 C

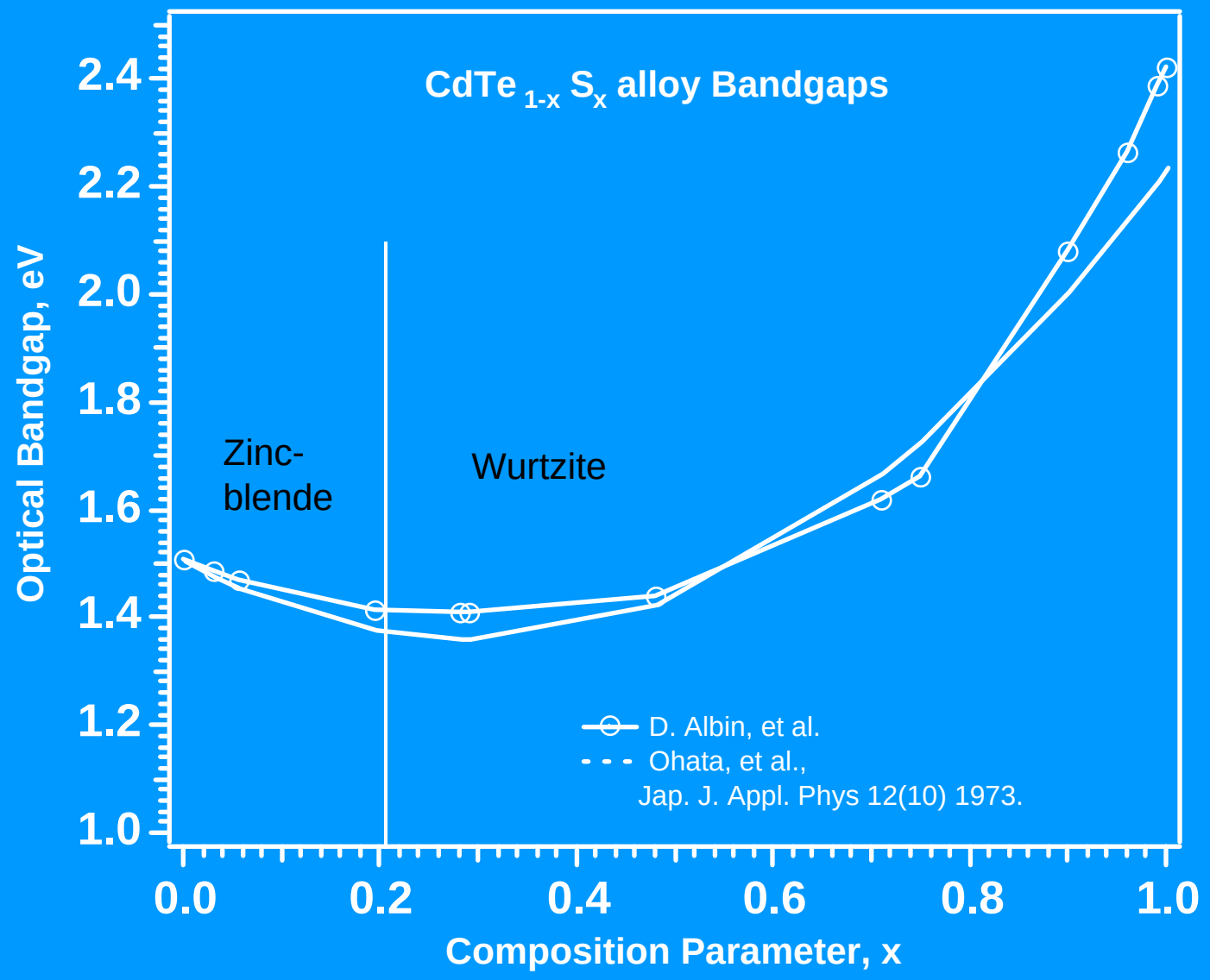
Observations

- Interdiffusion at CdS/CdTe interface increases with T_{sub} and $CdCl_2$ HT
- Accumulation of Cl at CdS/CdTe interface after $CdCl_2$ HT. Level of Cl increases with level of HT
- Cl is a n-type dopant in both CdS and CdTe; also in the intermixed alloy

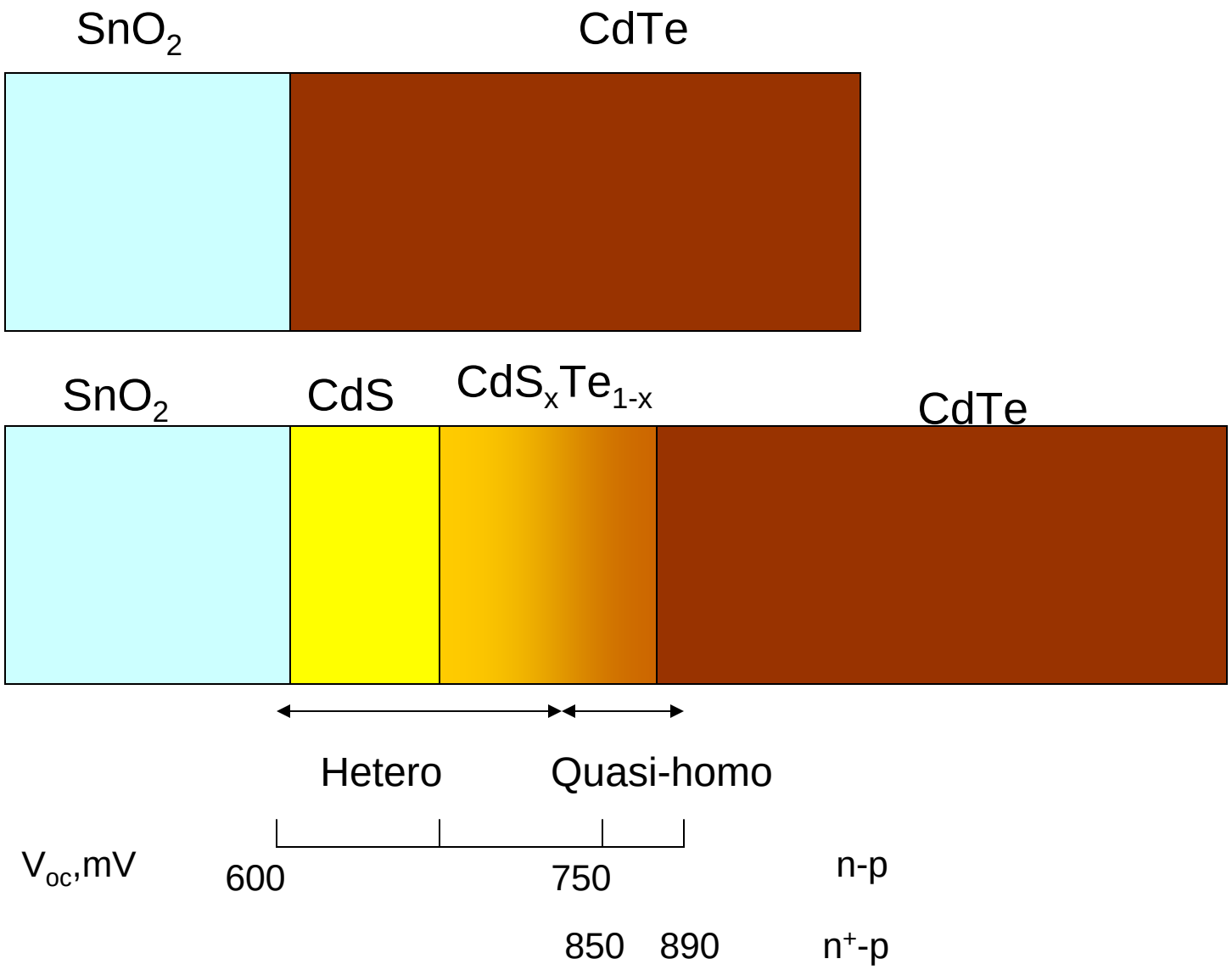
Electron-beam-induced-current



HREBIC


CdTe 1-x Sx alloy Bandgaps
Optical Bandgap, eV
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
Zinc-
blende
Wurtzite
D. Albin, et al.
Ohata, et al.,
Jap. J. Appl. Phys 12(10) 1973.
0.0
0.2
0.4
0.6
0.8
1.0
Composition Parameter, x

Device model



Device structure	V_{oc}, mV
SnO_2/CdTe	600-650
CdS/CdTe as dep	720-750
CdS/CdTe w/ $CdCl_2$	840-850

• Lower V_{oc} devices are true hetero-junctions, whereas the devices with $CdCl_2$ treatment have a junction between n+ Te-rich CdSTe alloy (doping with Cl) and p-type CdTe with compatible cubic structure i.e. quasi-homojunction.

• A true hetero-junction CdS/CdTe device performance will be dominated by interface defects at the interface which will be within the depletion region. This may be the case for as deposited devices fabricated at lower temperatures and SnO_2/CdTe devices giving low Voc.

• Role of CdS is mainly to produce Te rich alloy layer that gets doped to n-type during $CdCl_2$ process and passivation of the surface.

PHOTOCONDUCTIVE CdS AND ANOMALOUS AQE EFFECTS: COMPARISON OF EXPERIMENT AND MODELING

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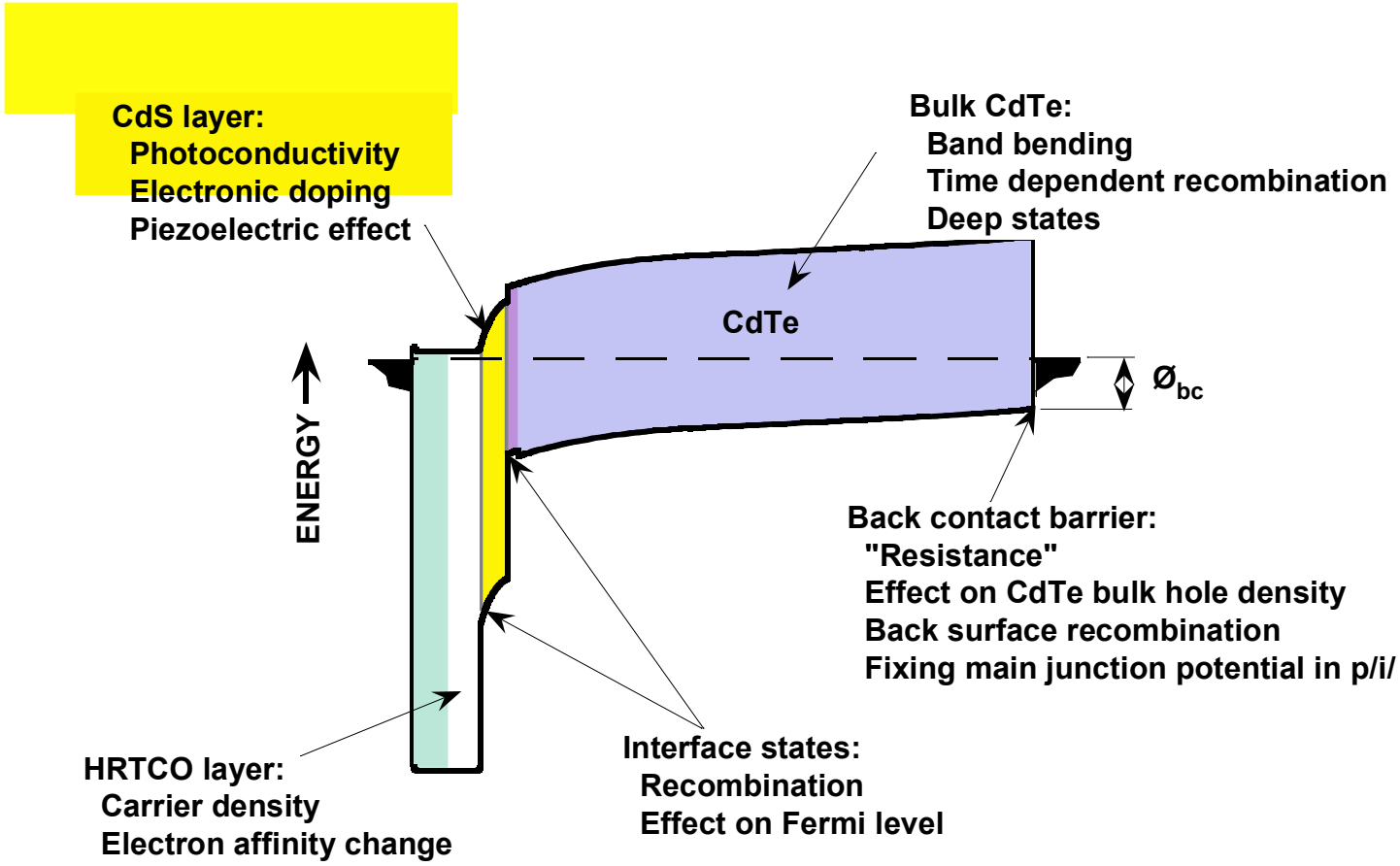
My appreciation to those that contributed cells: W. Sampath, A. Enzenroth, B. McCandless, S. Hegedus, T. Gessert.

The author acknowledges the support by NREL through Colorado State University, and the encouragement of Jim Sites, Tim Ohno, Fred Seymour and the CdTe Team members. Modeling results obtained using AMPS-1D (Version 1,0,0,1), written by S. Fonash, Pennsylvania State Univ., with EPRI support.

OUTLINE

- **FOCUS ON CdS PHOTOCONDUCTIVE EFFECTS**
- **PROPERTIES OF CdS**
- **MODEL ILLUSTRATION OF MECHANISM**
- **AQE vs. BIAS VOLTAGE…EXPERIMENT AND MODELING**
- **dc AQE MEASUREMENTS**
- **MODELING OF dc MEASUREMENTS**
- **CONCLUSIONS**


CdS layer:
Photoconductivity
Electronic doping
Piezoelectric effect
Bulk CdTe:
Band bending
Time dependent recombination
Deep states
CdTe
ENERGY
Ø$_{bc}$
Back contact barrier:
"Resistance"
Effect on CdTe bulk hole density
Back surface recombination
Fixing main junction potential in p/i/
HRTCO layer:
Carrier density
Electron affinity change
Interface states:
Recombination
Effect on Fermi level

Properties of CdS

Little info on carrier density or even resistivity in CdS layers in CdS/CdTe cells

Recipes for solar cells appear to not include any doping.

Cu states in CdS E_{Cu} ~ 0.7 - 0.9 eV (Bube et al. Phys. Rev. 128. 532 ('62)

Existence of p-type CdS debated

High densities of Cl (0.03 eV donor) and Cu (0.7- 0.9 eV acceptor) by SIMS suggest highly compensated material

Similar thin films of CdS:Cu on glass are highly photoconductive.

Number of researchers have suggested influence of pc on CdS/CdTe cells over many years.

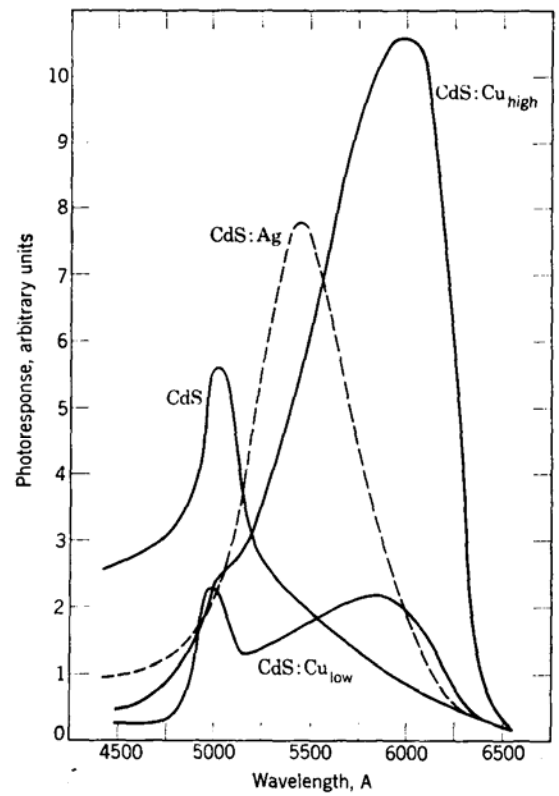


Fig. 6.4–9 Photoconductivity excitation spectra of CdS evaporated layers with various impurities. (After Veith [118])

To illustrate effect of a photoconductive CdS layer, use simple AMPS model

"Reasonable" model

In CdTe:

$N_a - N_d = 1.5e14$

$Ø_{bc} = 0.46$ eV

At CdS/CdTe interface:

$\Delta E_{cb} = 0.1$ eV (cliff)

In CdS:

$N_d = 7e15$ at 0.1 eV

$N_{a1} = 1e16$ at 0.9 eV

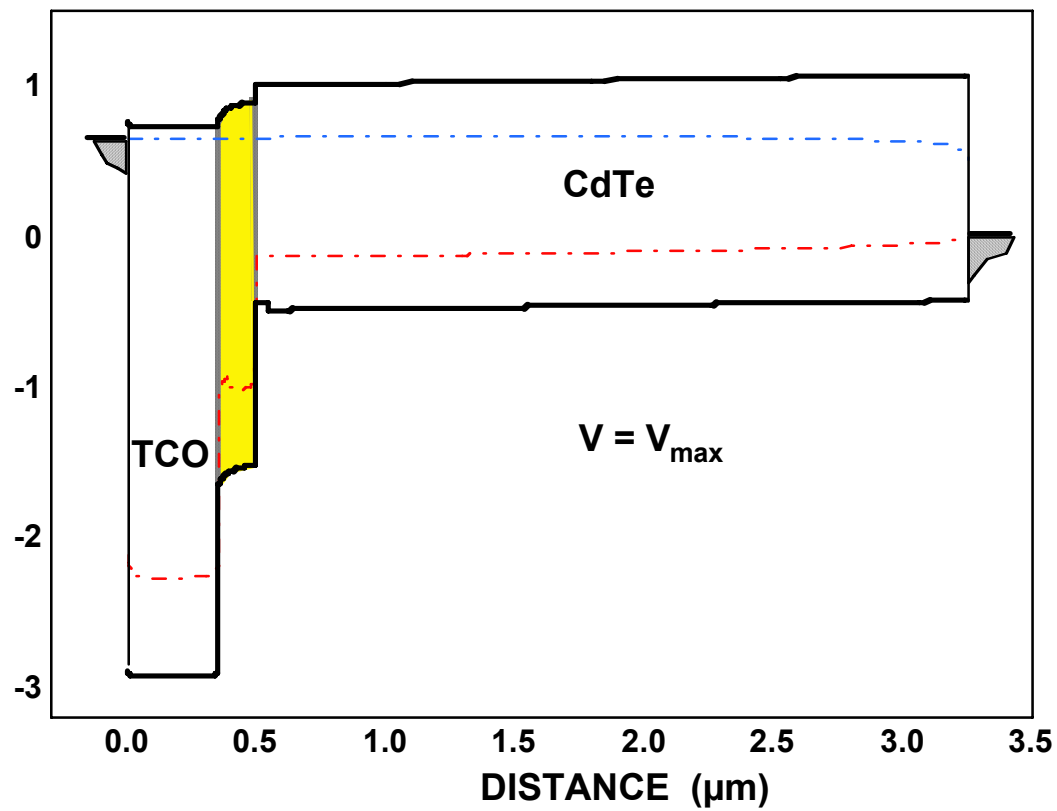
$N_{a2} = 1e16$ at 0.35 eV

==========

$V_{oc} = 0.783$

ff = 0.743

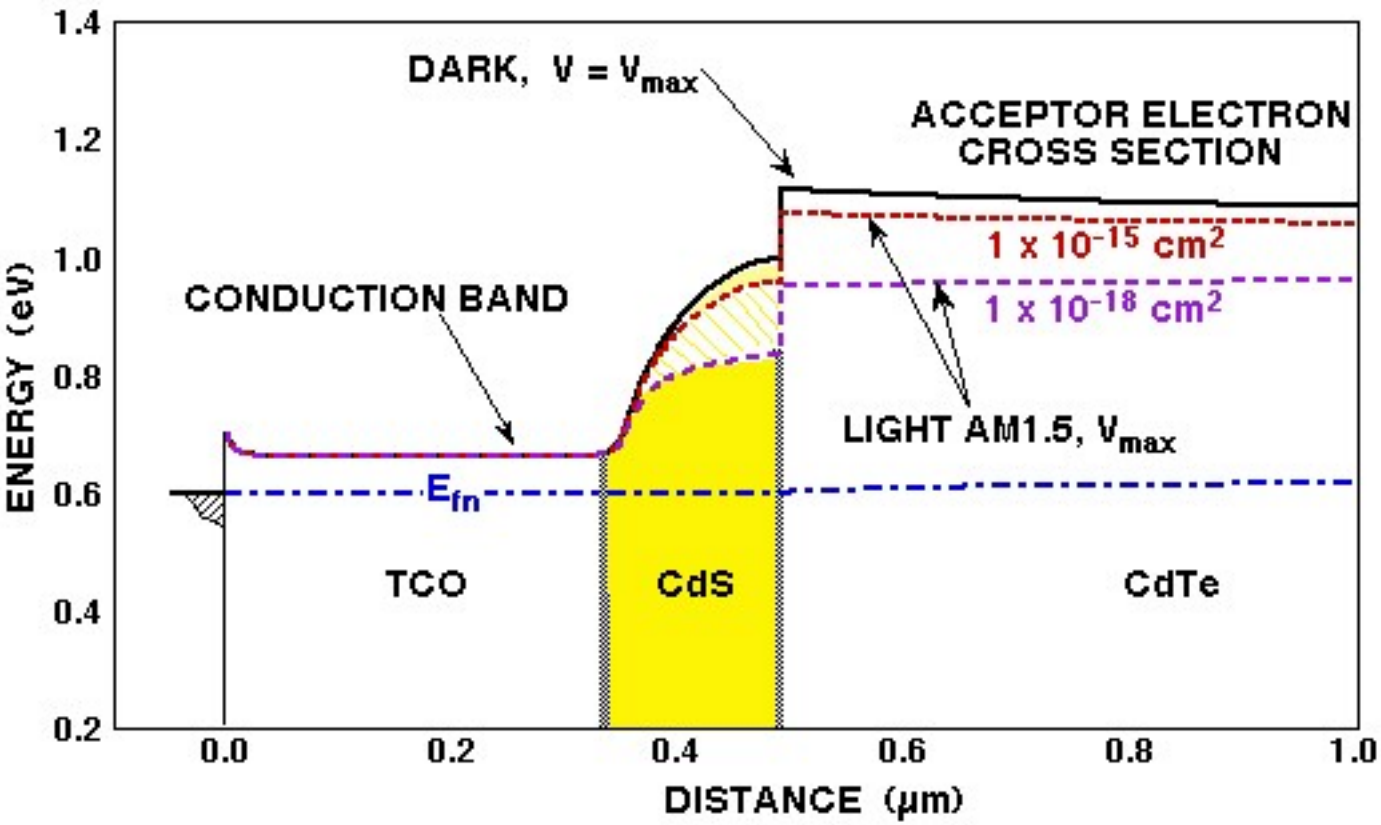
Eff = 12.1% at AM1.5



CdS would be p-type in bulk

In thin film, "borrows" charge from TCO, acts like an n-type layer

Compare two cases whose is only difference is electron cross section of Cu acceptor levels in CdS:

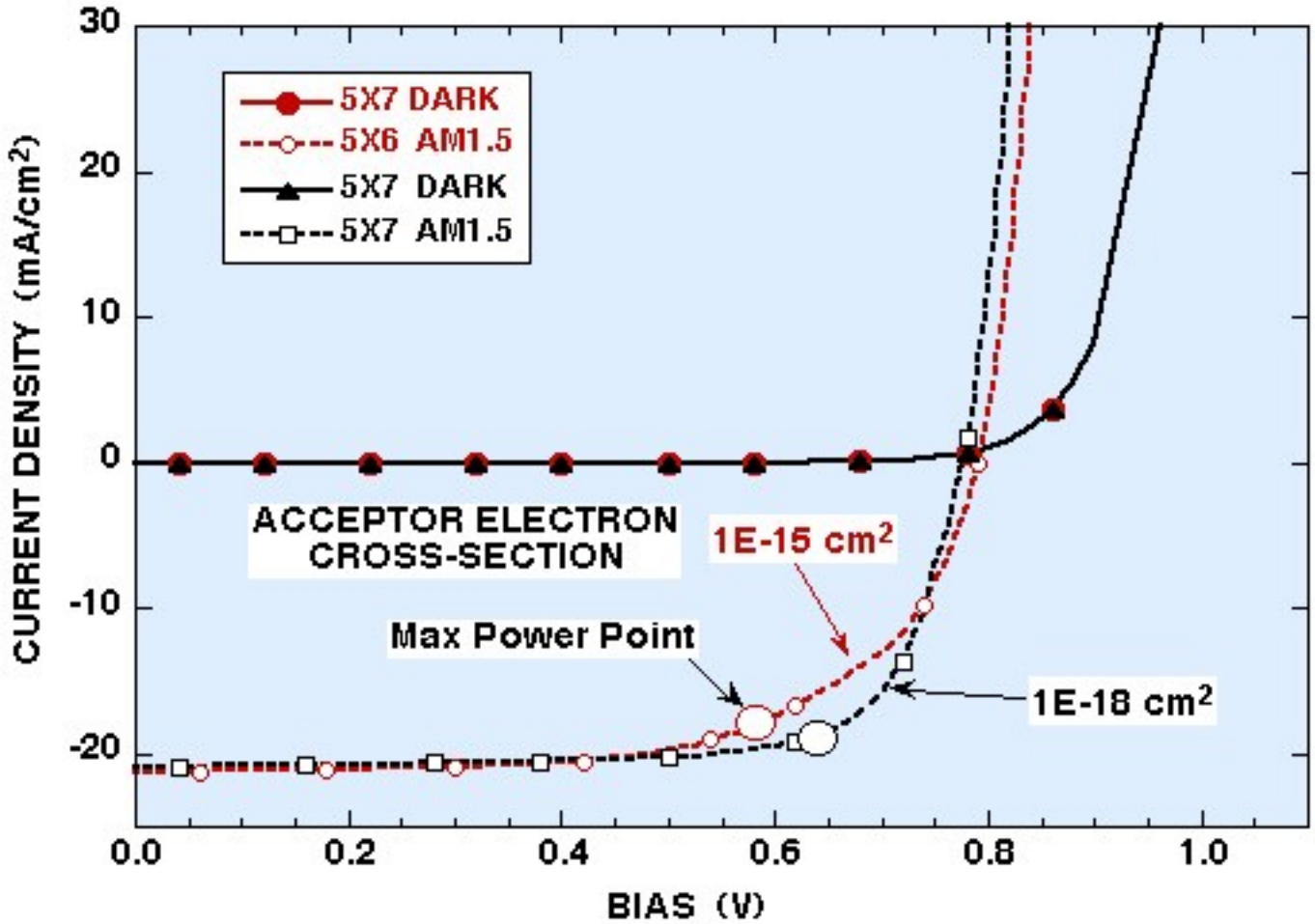


CdS is slightly p-type and pushes up barrier, reducing collection, reducing ff. Dark current is reduced, causing crossing.

Light absorbed in CdS neutralizes acceptors, making CdS more n-type.

Specific case of more general effect termed "Electronic Doping" by A. Rose.

Resulting J-V curves:



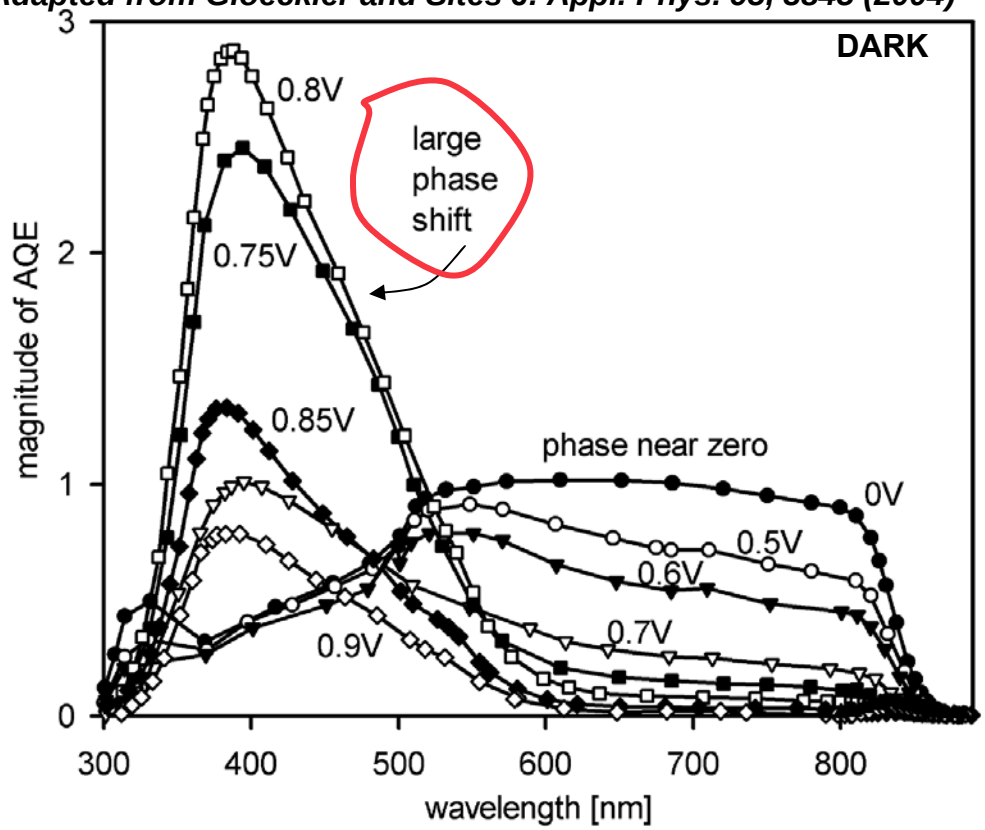
Cross-over is equivalent to negative Apparent Quantum Efficiency, and can give |AQE| > 1.

AQE vs. VOLTAGE MEASUREMENTS

Promising tool to explore junction, valuable adjunct to modeling

Many studies aimed at explaining light/dark cross-over of J-V curves

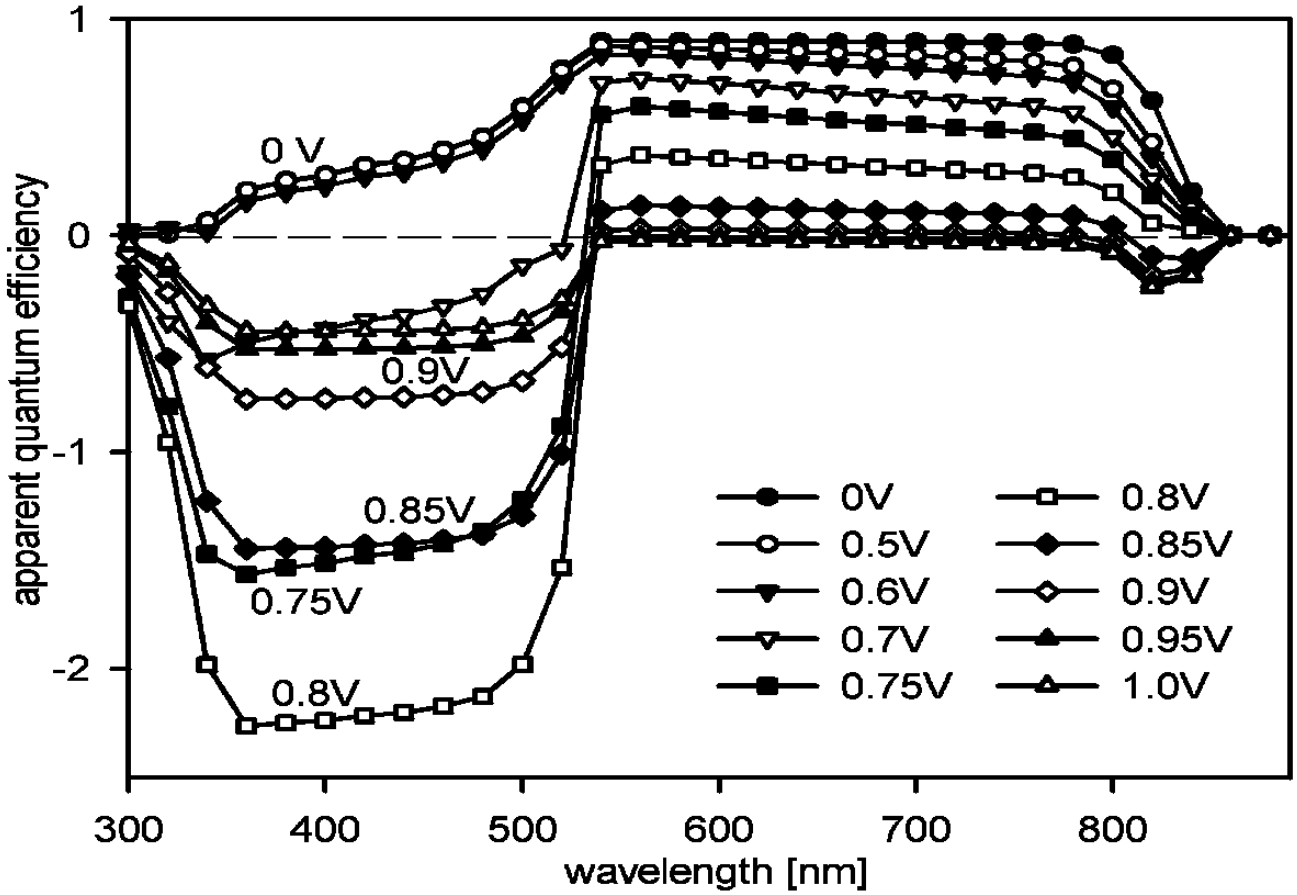
Original data from Batzner et al., Mat. Res. Soc. Symp. Proc. Vol. 668 (2001)
Adapted from Gloeckler and Sites J. Appl. Phys. 95, 3845 (2004)



Lock-in amplifier data (typically 200-300 Hz). Small-signal ac measurement.

Phase shift (~ 110°) interpreted as negative AQE

Gloeckler and Sites did extensive modeling of AQE effects



Gloeckler and Sites J. Appl. Phys. 95, 3845 (2004)

AMPS modeling is dc, based on two stable states.

PRESENT AQE MEASUREMENTS

ac AQE, Davies LIA at CSU shows apparent negative AQE for short wavelengths

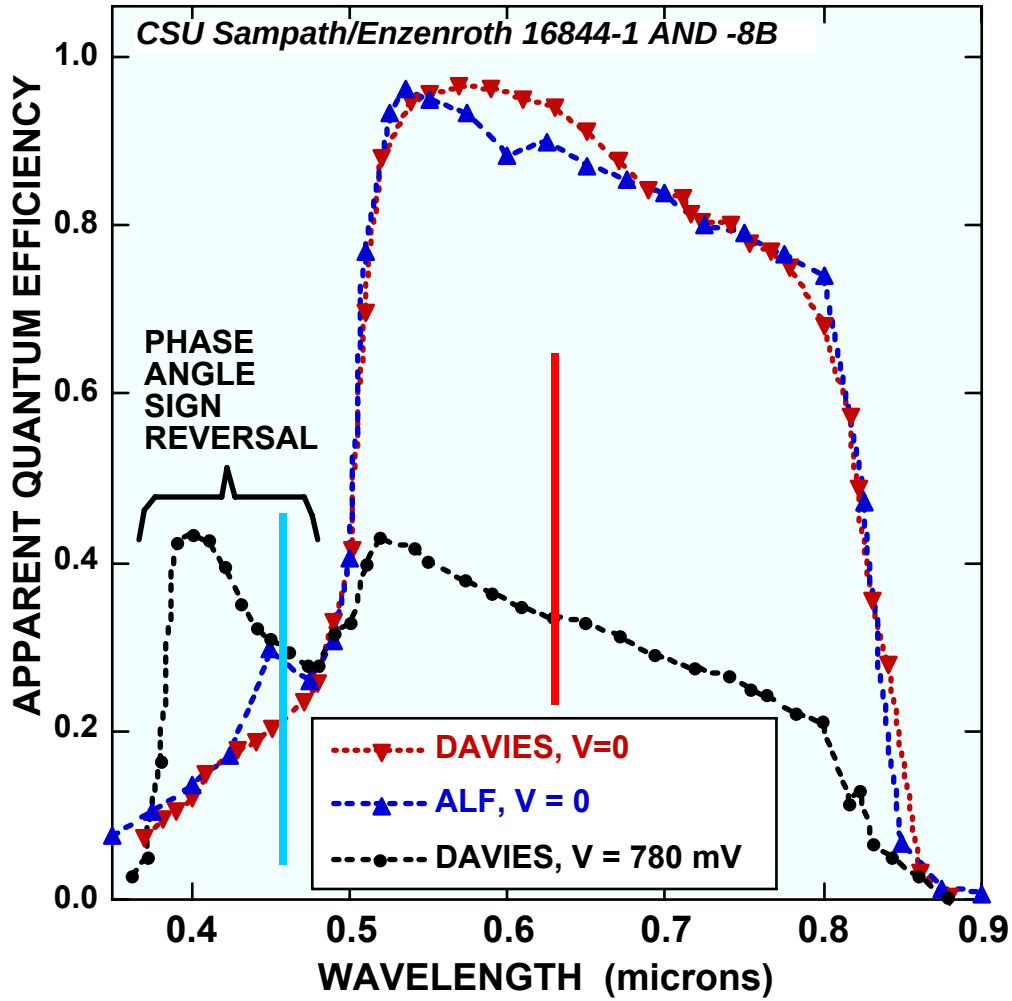
dc AQE (measuring step when light is turned on), ALF at CSU-West

Good agreement, but limited to V = 0

Mononchromator light current ≈ 3 - 7 μA/cm^2, signal- to-noise too large for higher bias

LED light current ≈ 1 - 5 mA/cm^2 also instant turn-on, linear flux-current relationship

470 and 630 nm



At low bias:

Positive AQE, well shaped steps.

At high bias:

Negative AQE, slow transients for both red and blue

Red:

J_{sc} = 4.9 mA/cm²

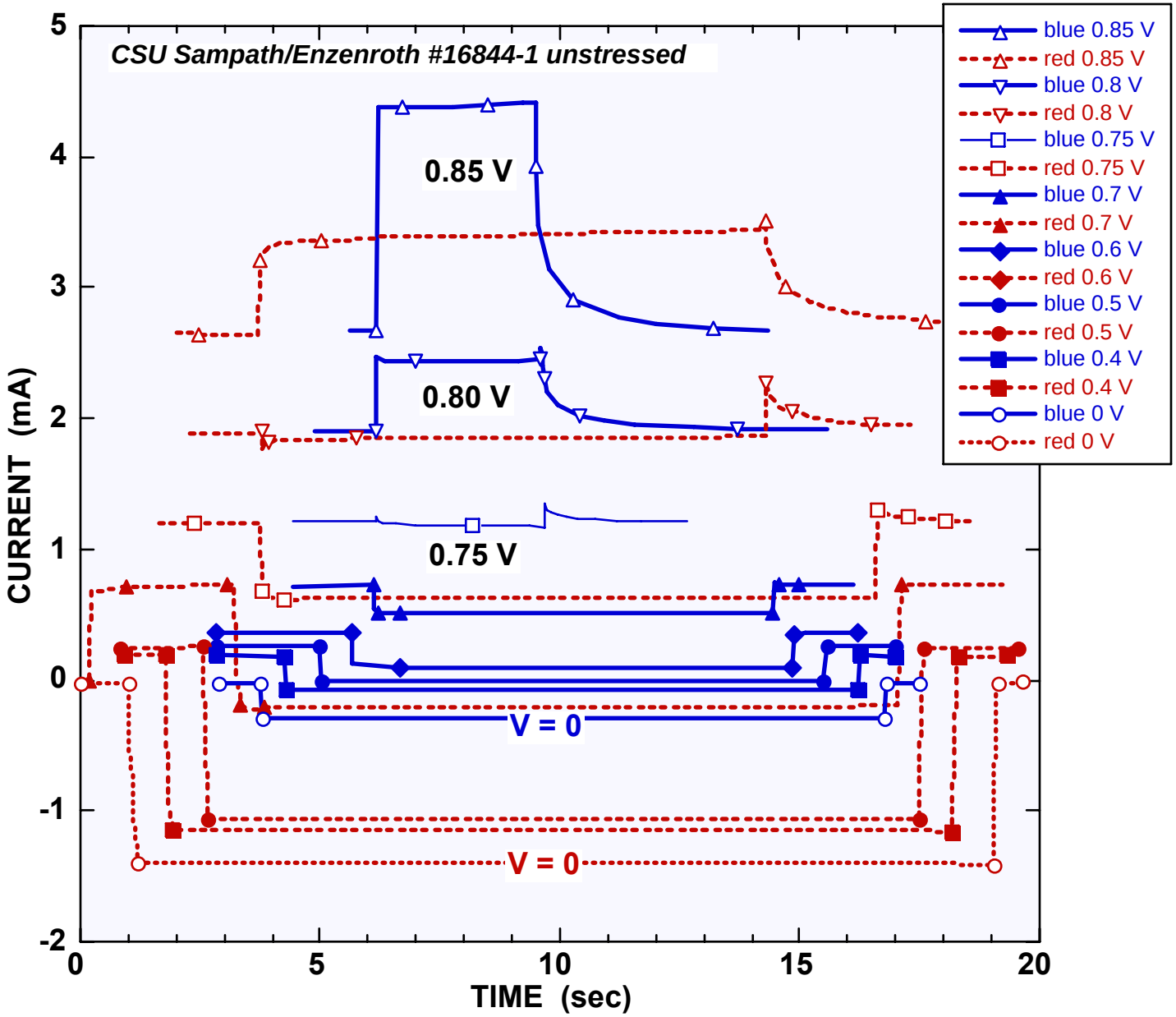
Blue:

J_{sc} = 1.0 mA/cm²

Other cells:

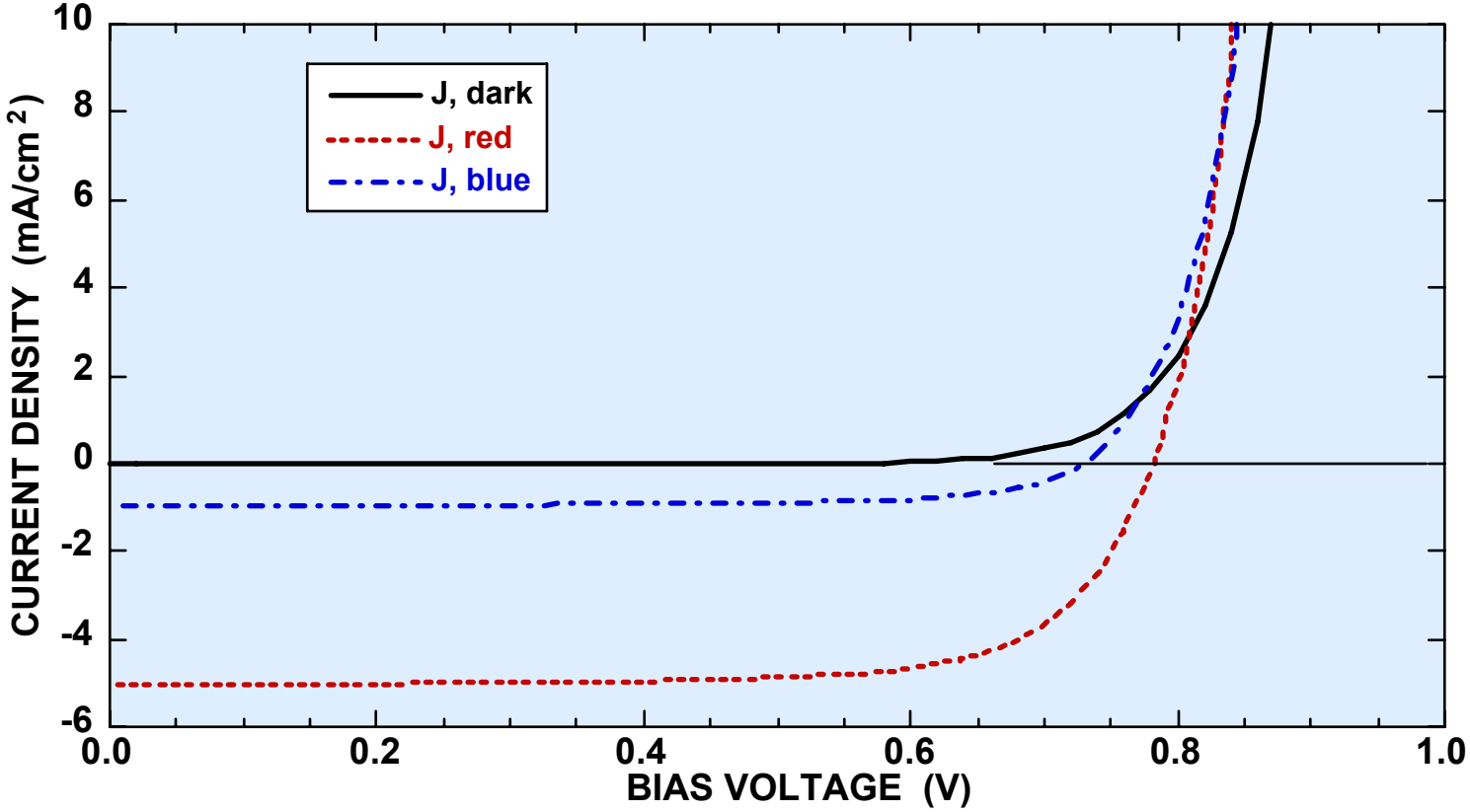
Well shaped steps to > 1 V bias.

Negative QE for red and blue still present

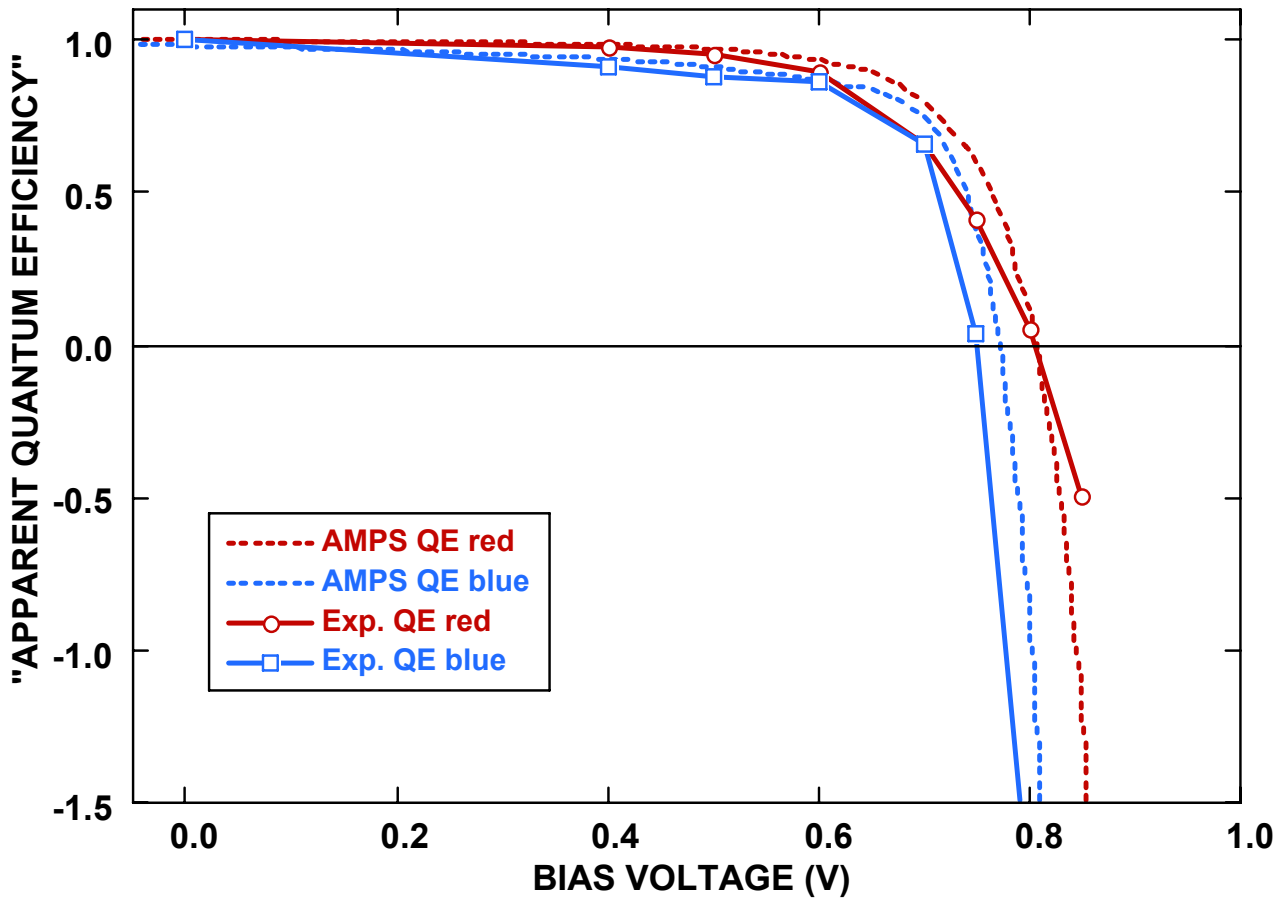


AMPS modeling of LED experiments (same parameters as before)

Same Jsc as experimental data just presented



Cross-over appears at lower voltage for blue than red



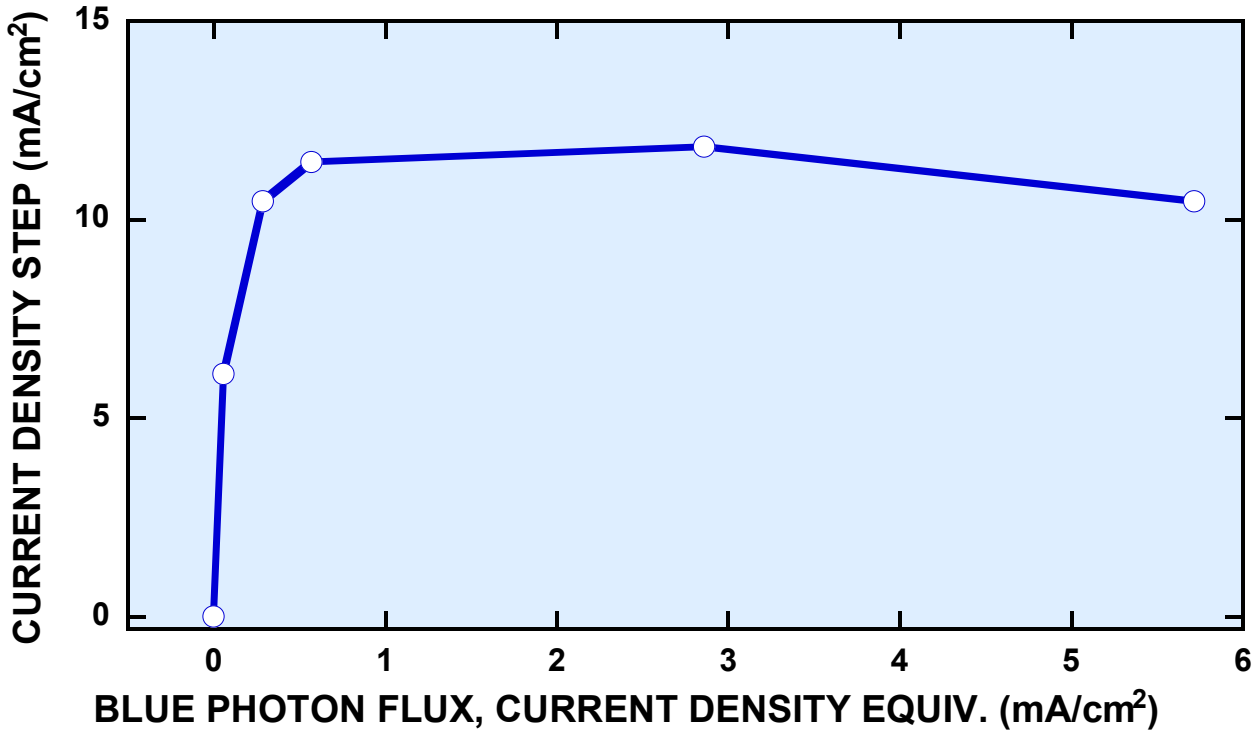
Opinion:
Apparent negative AQE is change in forward-bias transport mechanism. Light generated current cannot be separated from "dark" current

Transition to negative AQE can be associated with onset of negative electric field in CdTe near junction. Field aided diffusion length gets longer, forward bias current gets larger.

Observation:

Contrary to LIA results, dc measurements show negative QE for red light as well as blue…observed in a number of cells from different fabricators.

Forward-bias step is a function of illumination intensity



"Blue" step at V = 0.85 saturates near 0.5 mA/cm^2 equivalent photon flux

CONCLUSIONS

- Dark, forward-bias QE for 300 – 500 nm extremely sensitive to density and cross-sections of Cu acceptors in CdS
- LIA QE measurements sometimes questionable
- dc AQE measurements enable:
  - Direct observation of transients
  - Observation of "probe" beam intensity dependence
  - Large signal-to-noise ratio
  - Instant turn-on and proportional intensity control
- Experiment and model show negative AQE in 630 nm region
- Simplified AMPS model without spikes, n-CdTe, or high ΔEc for TCO/CdS interface
- CdS pc and electronic doping important for V > Vmax region and thus for increasing Voc

Measuring recombination in CdTe solar cells

Questions

How is the recombination lifetime measured?

What is the recombination lifetime in CdTe?

What causes the recombination?

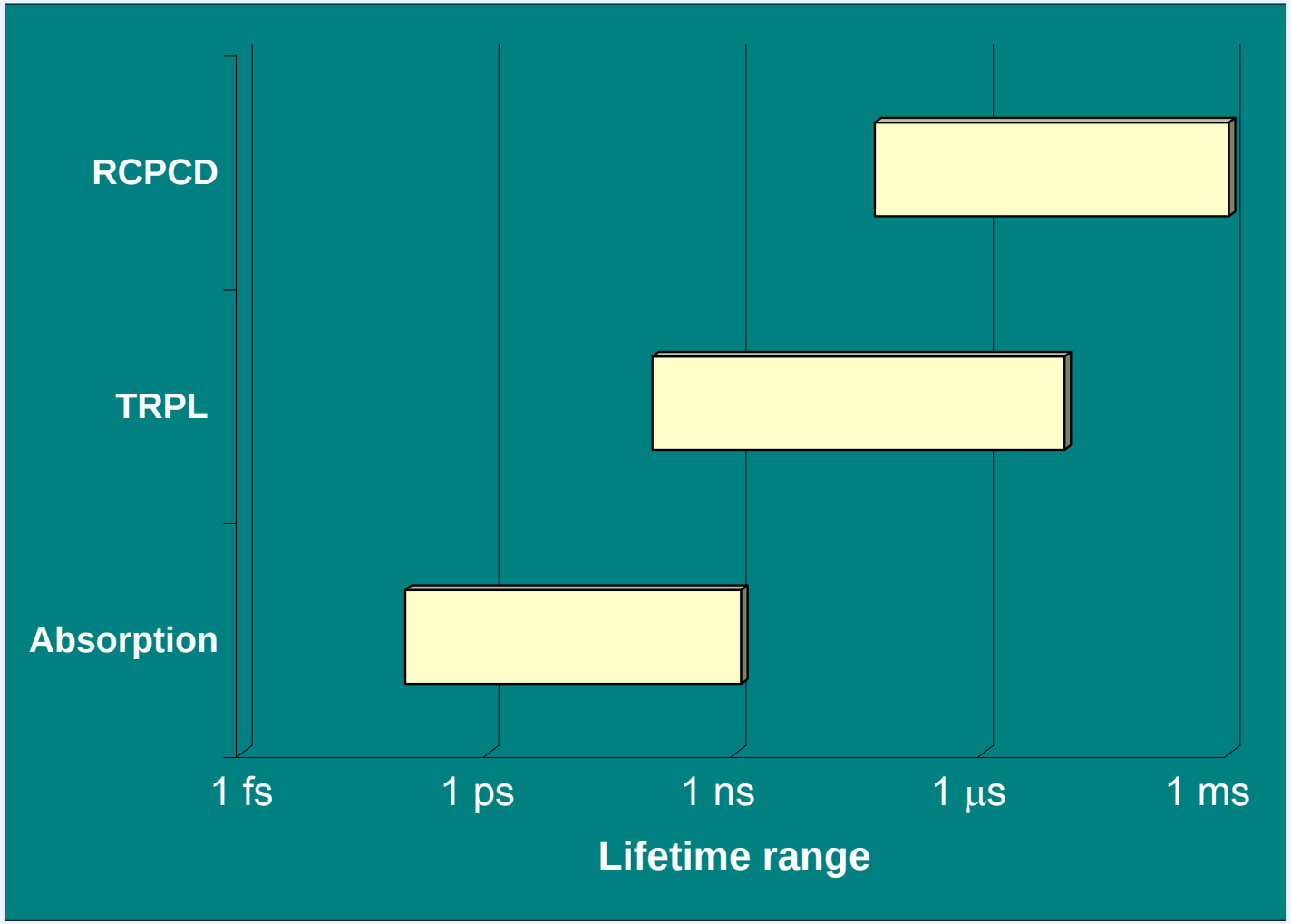
Does lifetime have anything to do with device performance?

Do the experimental values agree with device models?

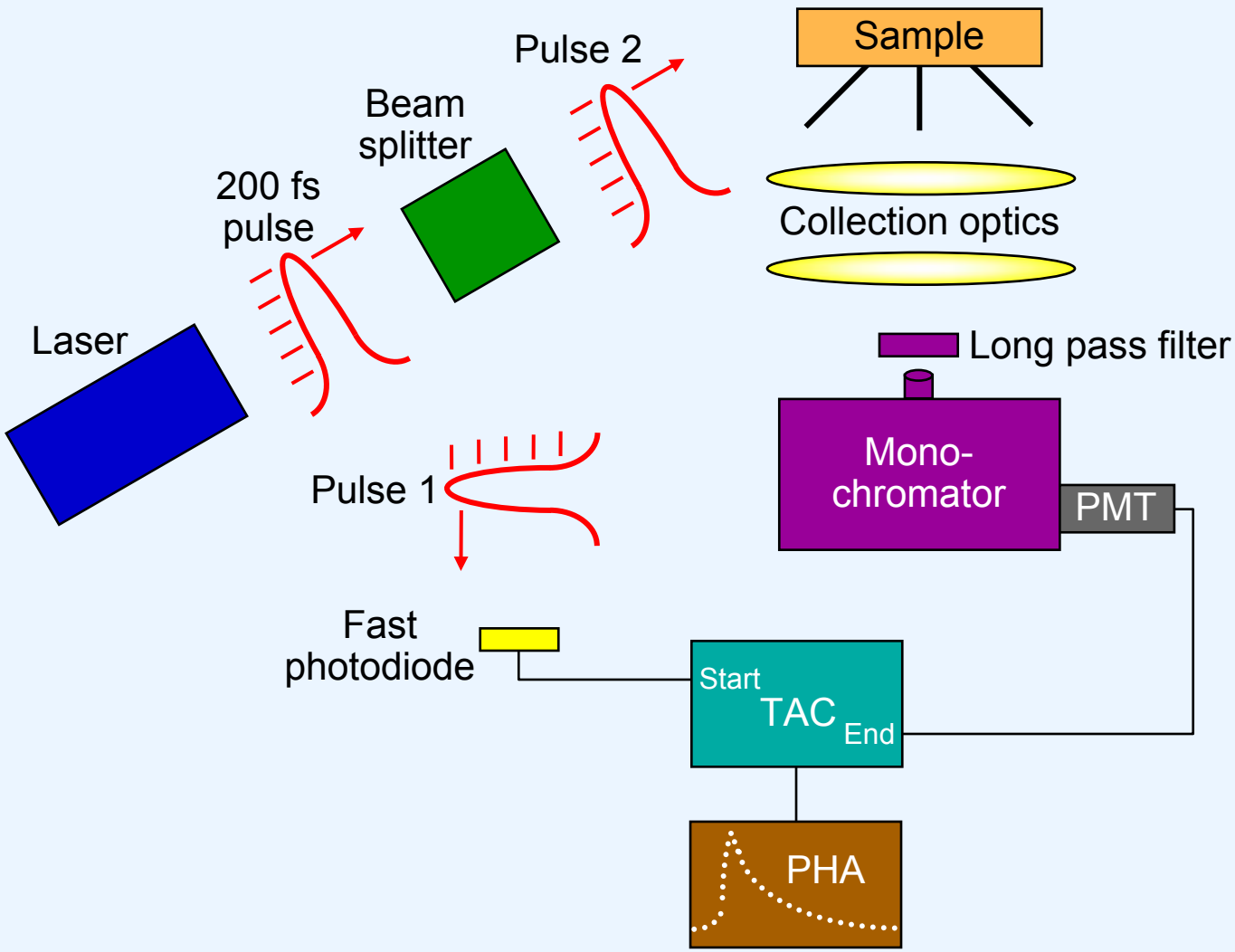
Lifetime measurements

- Inject excess carriers into a sample with a laser pulse
- Watch a property related to the excess carrier concentration decay
- Photoconductivity, luminescence, absorption, …

NREL experiments



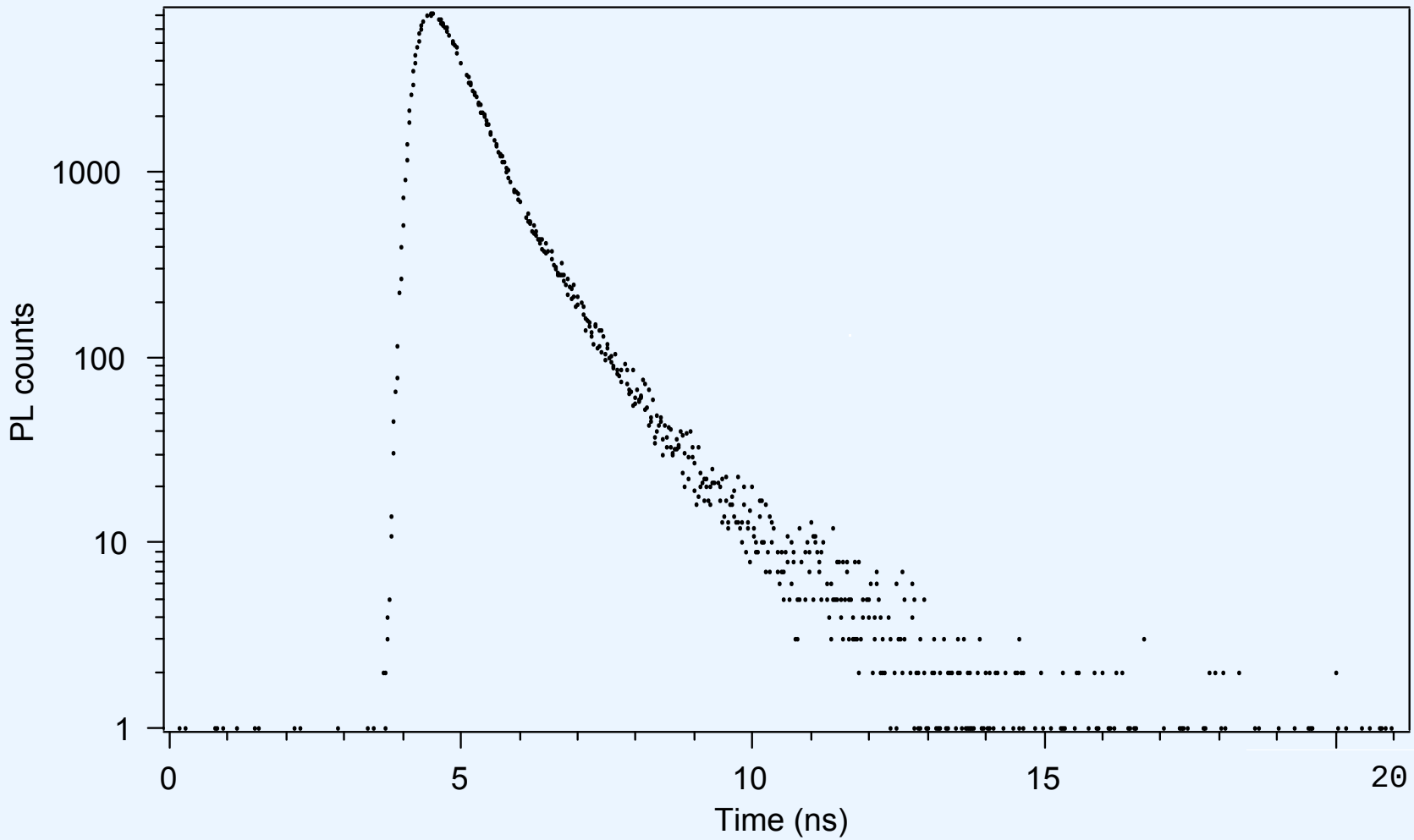
Single photon counting schematic



1. We count a photon about once in every 200 attempts.
2. We make about 250,000 attempts per second.
3. We finish with a histogram of photon counts vs. time.

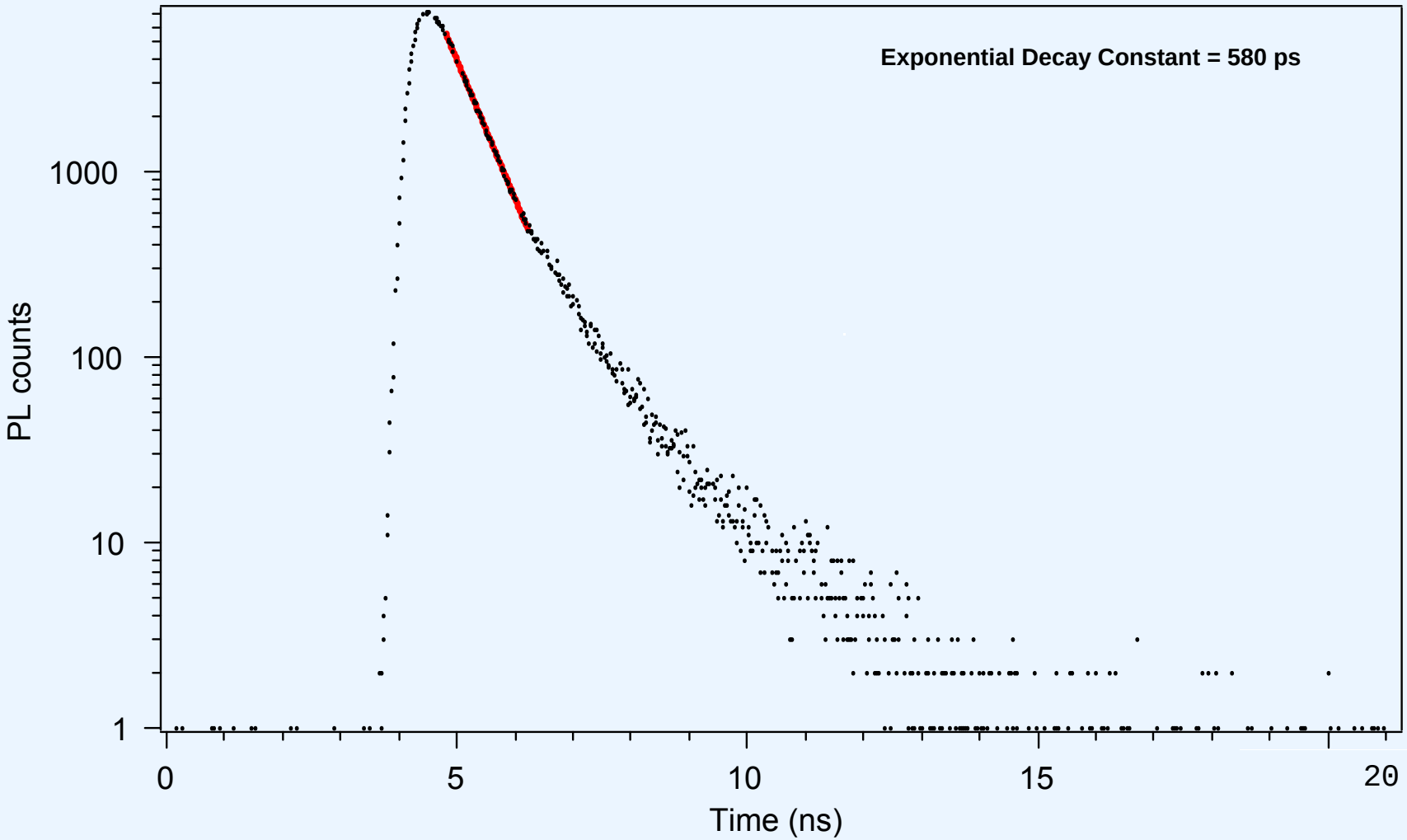
Results

Measurement taken on a completed CdTe solar cell



Results

Measurement taken on a completed CdTe solar cell



Doesn't TRPL only measure the radiative lifetime?

$r_{total} = r_{srh} + r_{surf} + r_{rad} + r_{auger} + \ldots = r_{nrad} + r_{rad}$

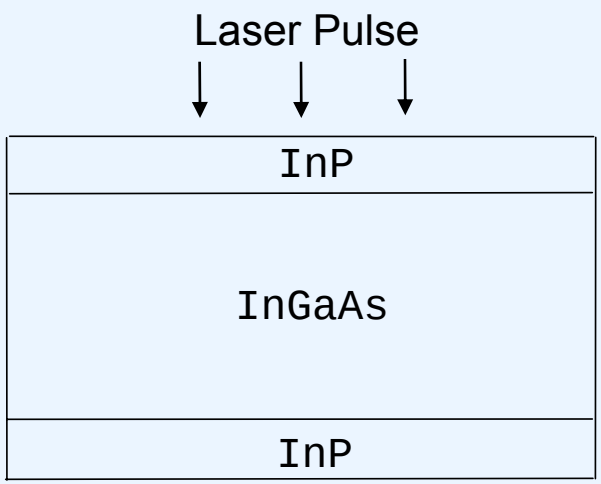
$$PL_{\text{int}}(t) \propto B(pn - p_o n_o)$$

<u>For p-type material,</u> $p_0 >> n_0$

$$PL_{\text{int}}(t) \propto B p_o [\Delta n(t)]$$ in low injection, $\Delta n << p_0$

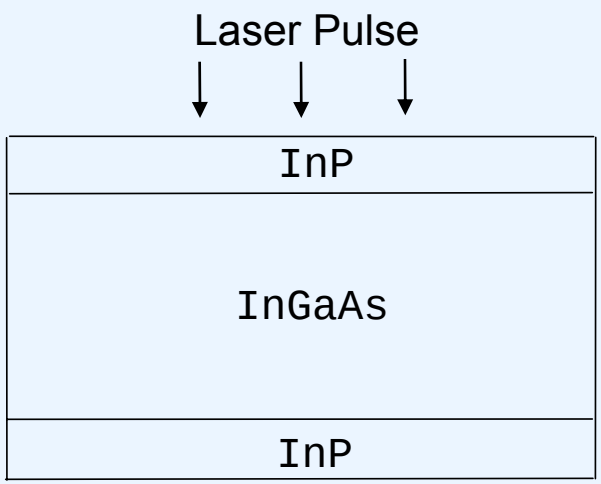
$$PL_{\text{int}}(t) \propto B[\Delta n(t)]^2$$ in high injection, $\Delta n >> p_0$

An ideal sample



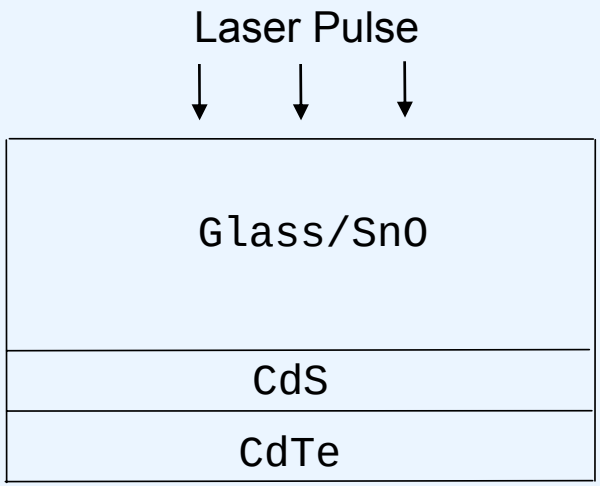
- Double heterostructure confines carriers and provides surface passivation
- Cap layers are thin and transparent to PL and incident laser light
- Interpretation is simplified

An ideal sample



- Double heterostructure confines carriers and provides surface passivation
- Cap layers are thin and transparent to PL and incident laser light
- Interpretation is simplified

A CdTe sample



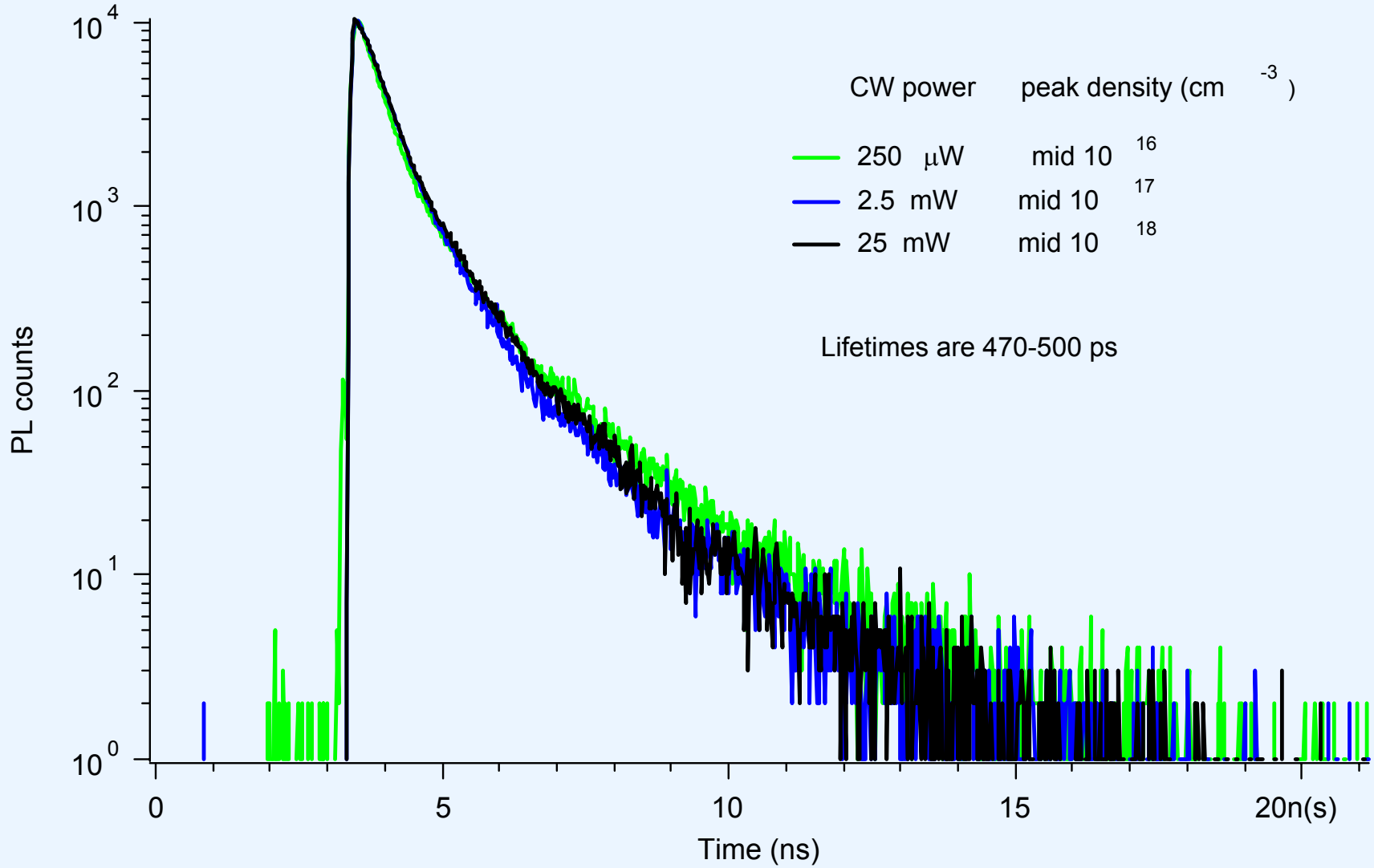
What does the junction do?

- In low injection, the field separates charge and the PL decay curve is dominated by charge separation

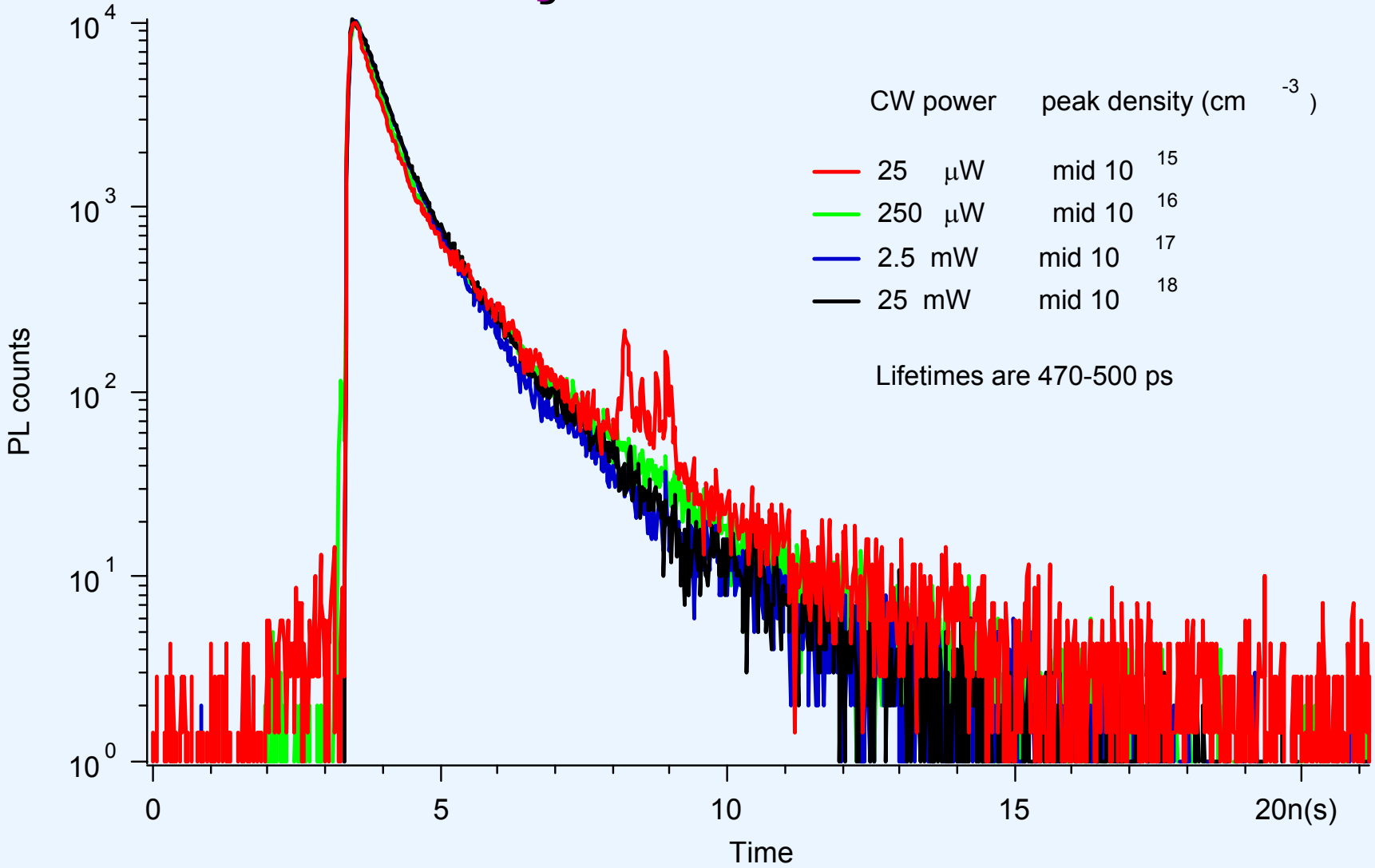
- In high injection, the equilibrium field is washed out and the decay curve is dominated by recombination (Metzger *et al*., Phys. Rev. B **71**, 035301)

- How do injection levels affect the lifetimes?

Injection level



Injection level



What is the recombination mechanism?

- $\tau_{rad} \approx 1/Bp$ $\tau_{auger} \approx 1/Cp^2$
- The injection dependence is not right for Auger or radiative recombination
- The short lifetimes are not consistent with radiative recombination
- The CdTe radiative efficiency, $r_{rad} / r_{tot,}$ is on the order of 0.1 %.
- We are looking at SRH or surface recombination

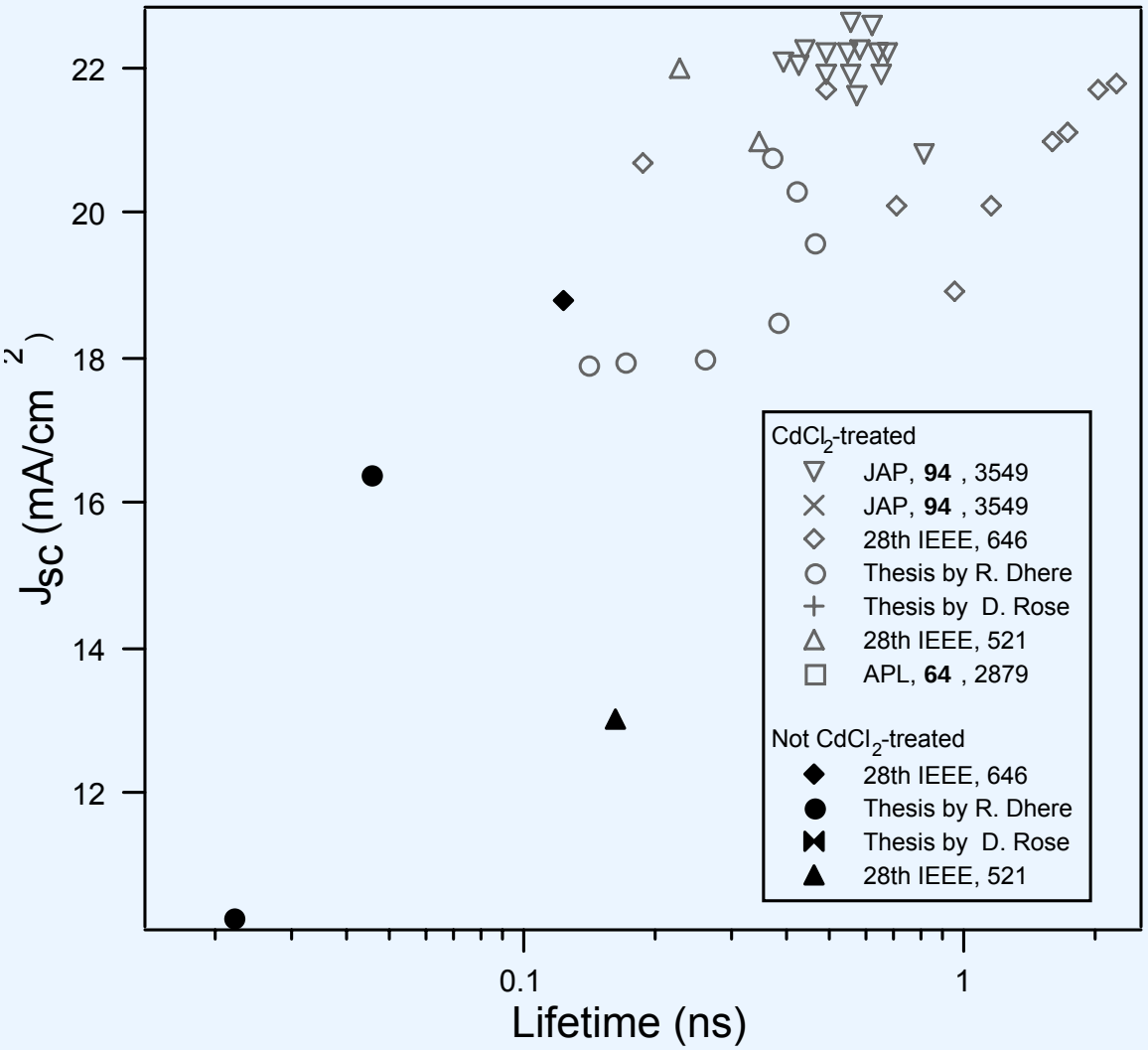
What is the source?

•Not enough extrinsic control and information to separate out GB recombination, interface recombination, and bulk recombination.

•Modeling does not favor a scenario where recombination away from the interface is significantly larger than the lifetime values reported here (i.e. 10ns)

•Technique is generally not great for determining defect density, capture cross sections, and trap energy levels

Jsc vs. lifetime

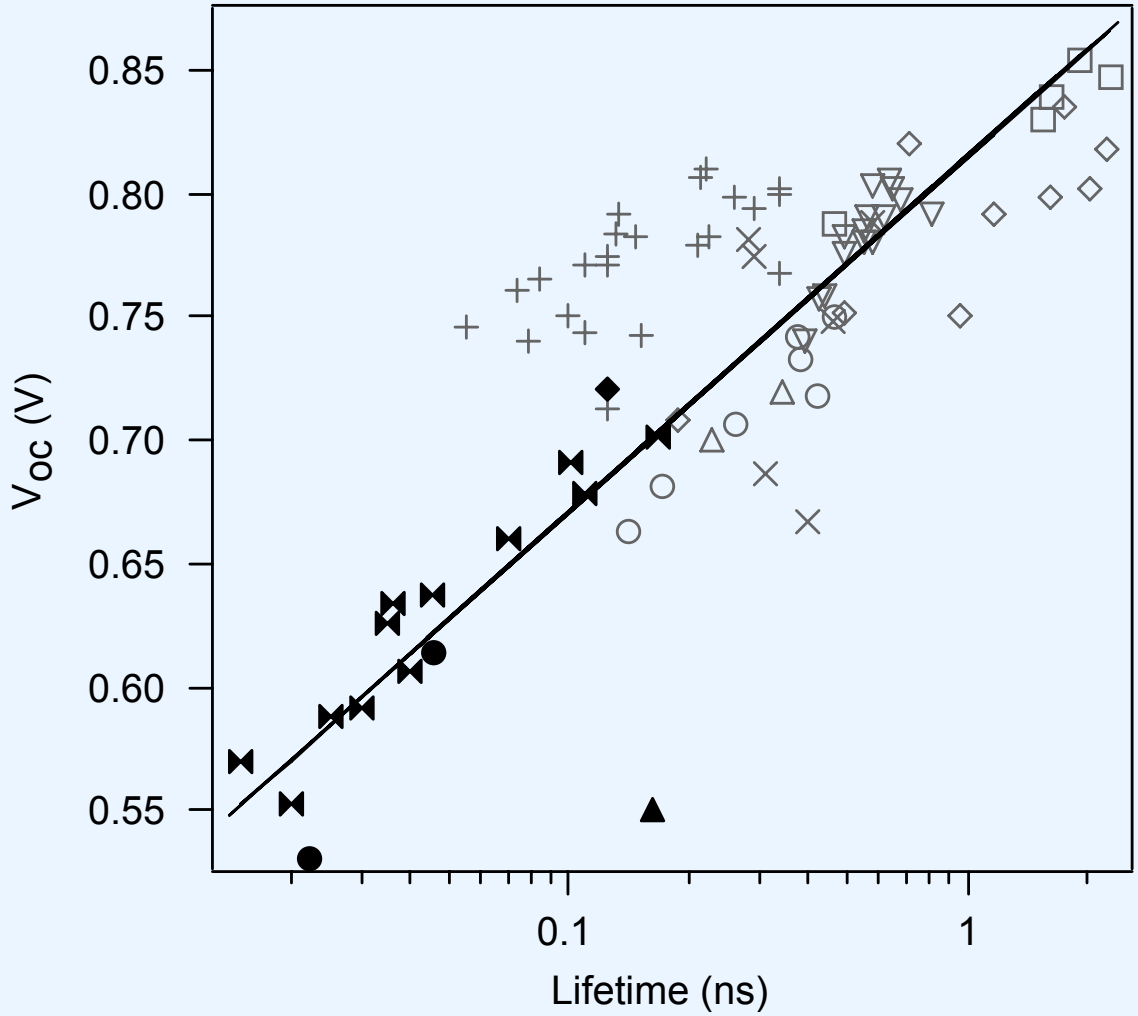


Why good current is easy in CdTe solar cells

- About 85% of the AM 1.5 spectrum is absorbed within 0.5 μm of the CdTe/ CdS interface. About 95% is absorbed within 1.0 μm.
- The depletion region is about 1-4 μm.
- Transit times across the junction are around 100 ps

So long diffusion lengths and lifetimes are not necessary for reasonably good photocurrent collection.

V_{oc} and lifetime



Voc and lifetime

Device physics for various heterojunction and homojunction models gives ,

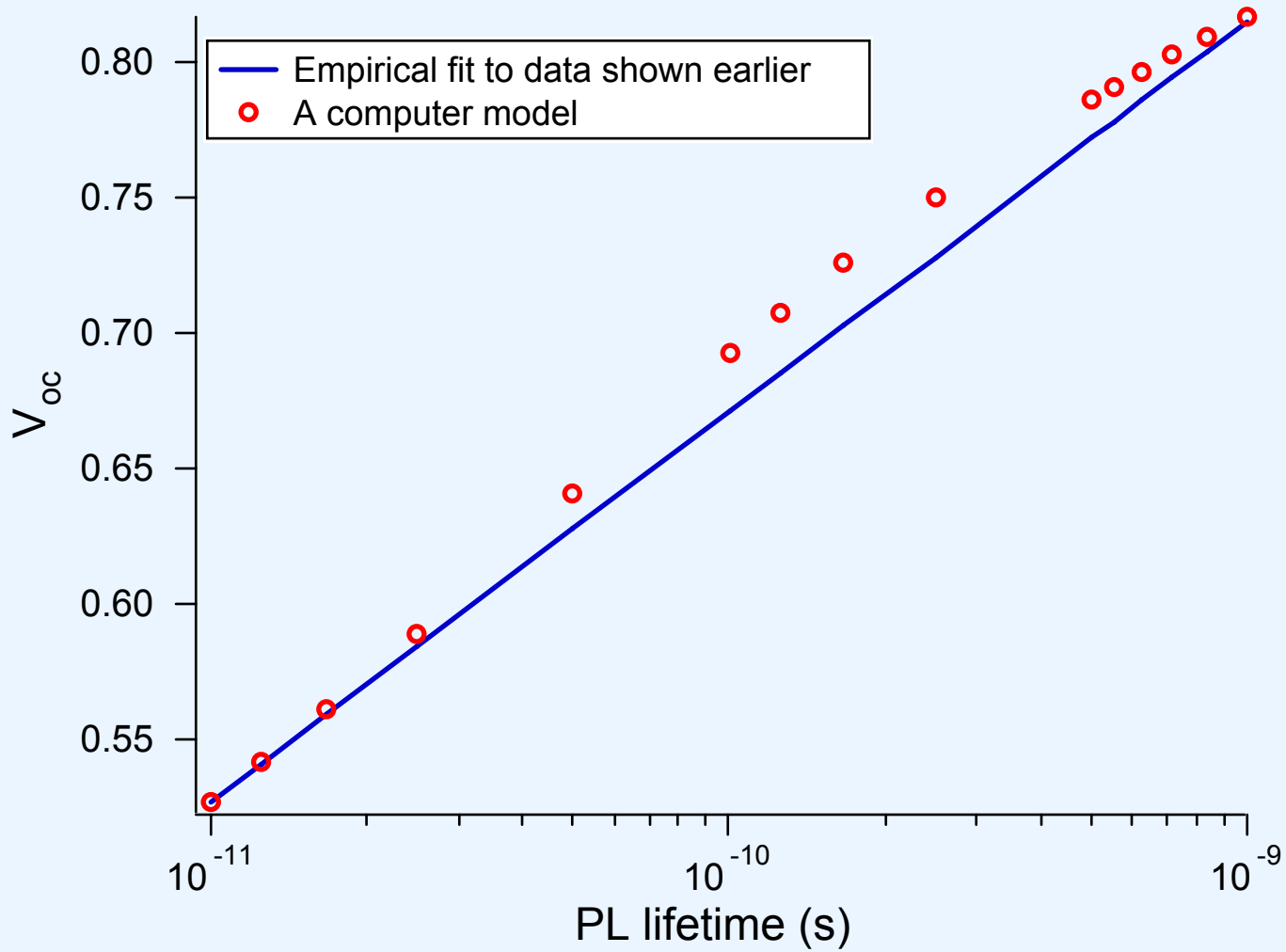
$$V_{oc} \approx \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0}\right)$$

The fit is,

$$V_{oc} \approx \frac{1}{16} \ln[4.6 \cdot 10^{14} \tau_{PL}(s)]$$

This gives an ideality factor of 2.5,
and means J_o is inversely proportional to τ,
which is consistent with strong recombination in the depletion region

The lifetime values are reasonable



The proper perspective

Many things contribute to V_{oc}

Amongst fluctuations in many other variables, there is a strong correlation between the measured lifetime and V_{oc}

A strong correlation between the measured lifetime and V_{oc} does not, and should not, hold for every sample set

Concluding remarks

- TRPL can assess recombination in CdTe solar cells.
- This recombination affects device performance
- These lifetime values are consistent with models.
- There is no need for the statement “if CdTe is so bad, why does it work so well”
- CdTe lifetimes are consistent.
- If you want to improve V_{oc}, achieve lifetimes greater than 2 ns.

References

Metzger *et al*., JAP **94,** 3549

Metzger *et al*., Phys. Rev. B **71**, 035301

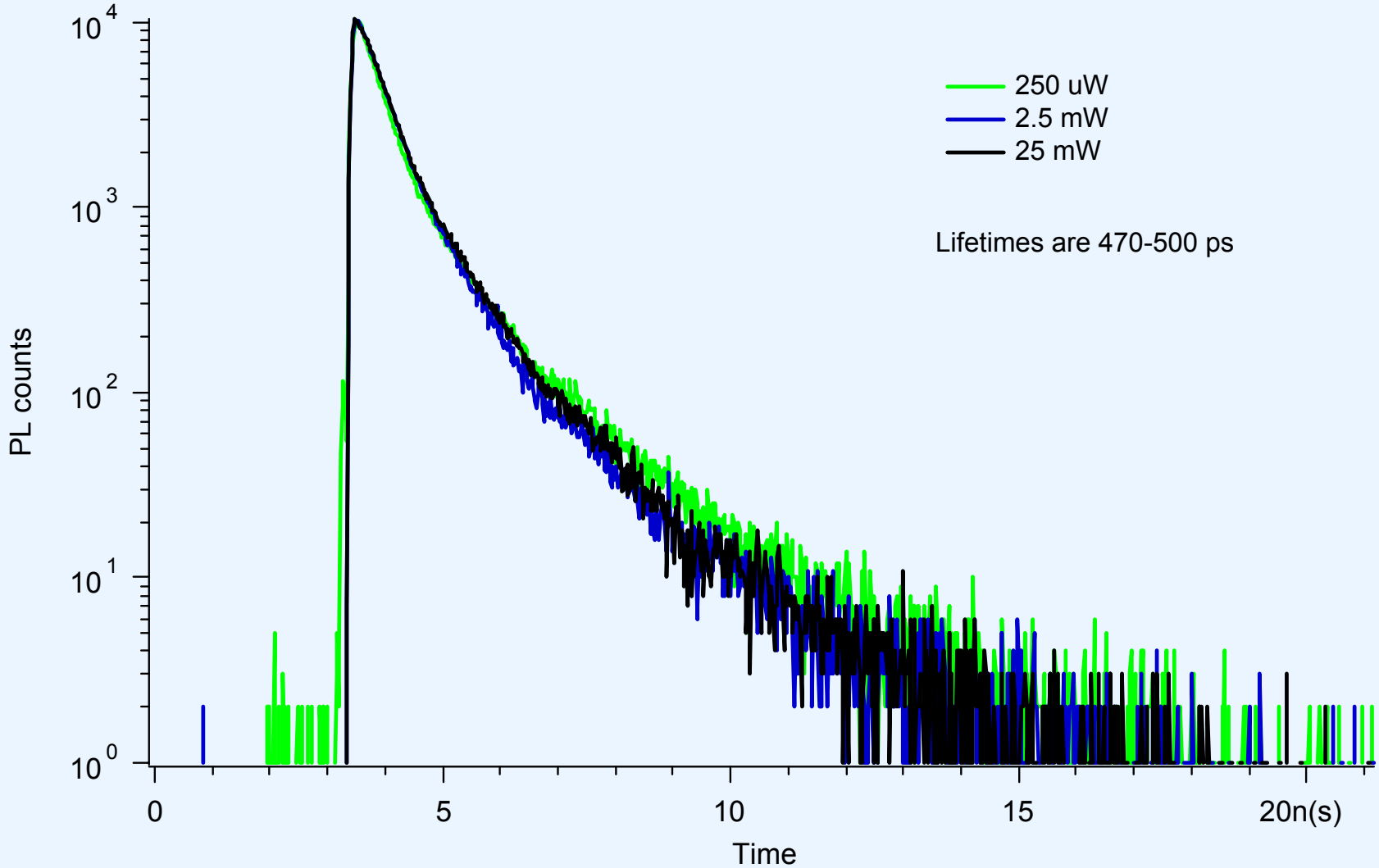
Metzger *et al*., JAP, in press

Metzger *et al*., upcoming IEEE

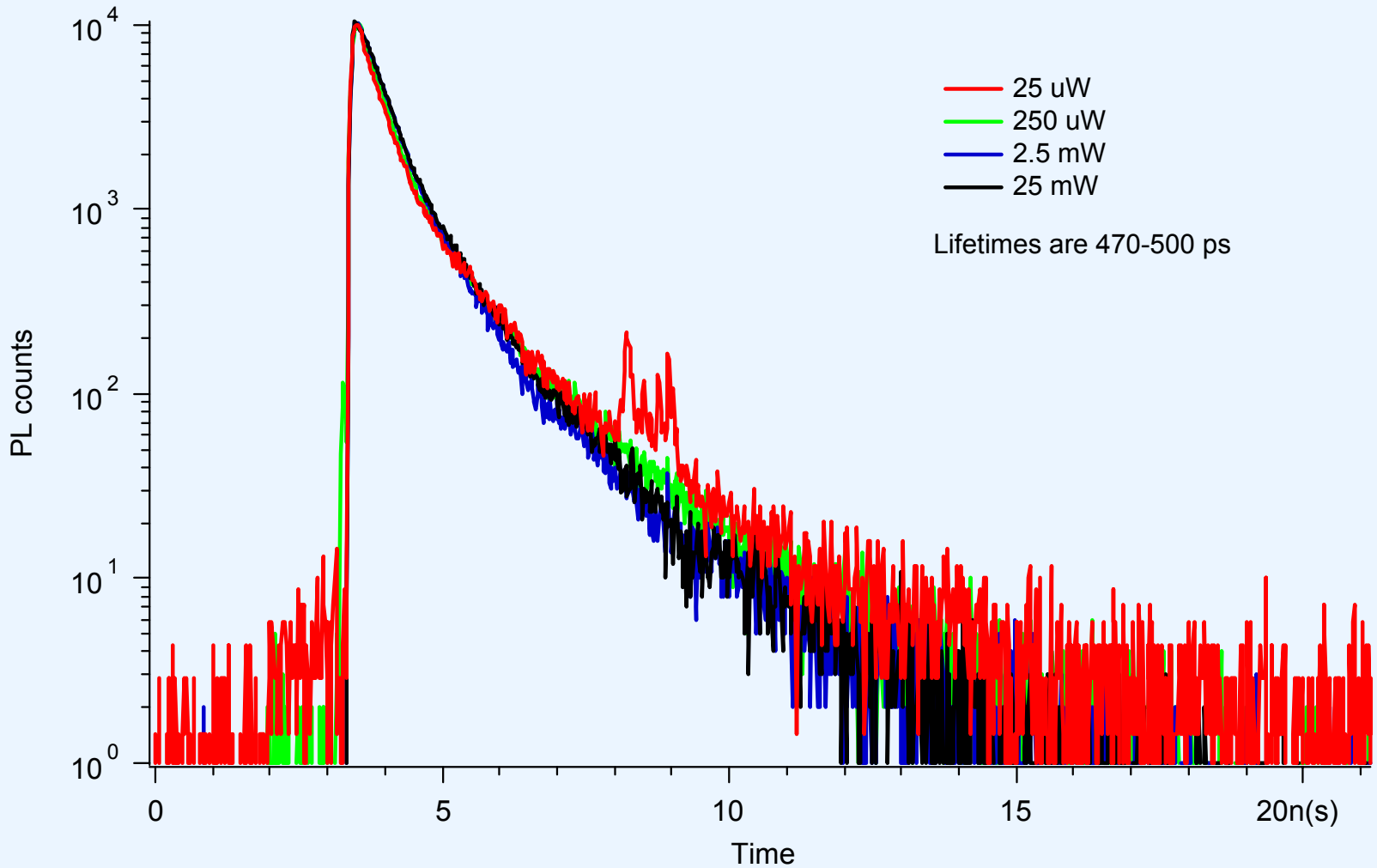
Demtsu *et al.*, in progress

EXTRAS

Injection level



Injection level



Voc and lifetime

Device physics for various heterojunction and homojunction models gives ,

$$V_{oc} \approx \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0}\right)$$

The fit is,

$$V_{oc} \approx \frac{1}{16} \ln[4.6 \cdot 10^{14} \tau_{PL}(s)]$$

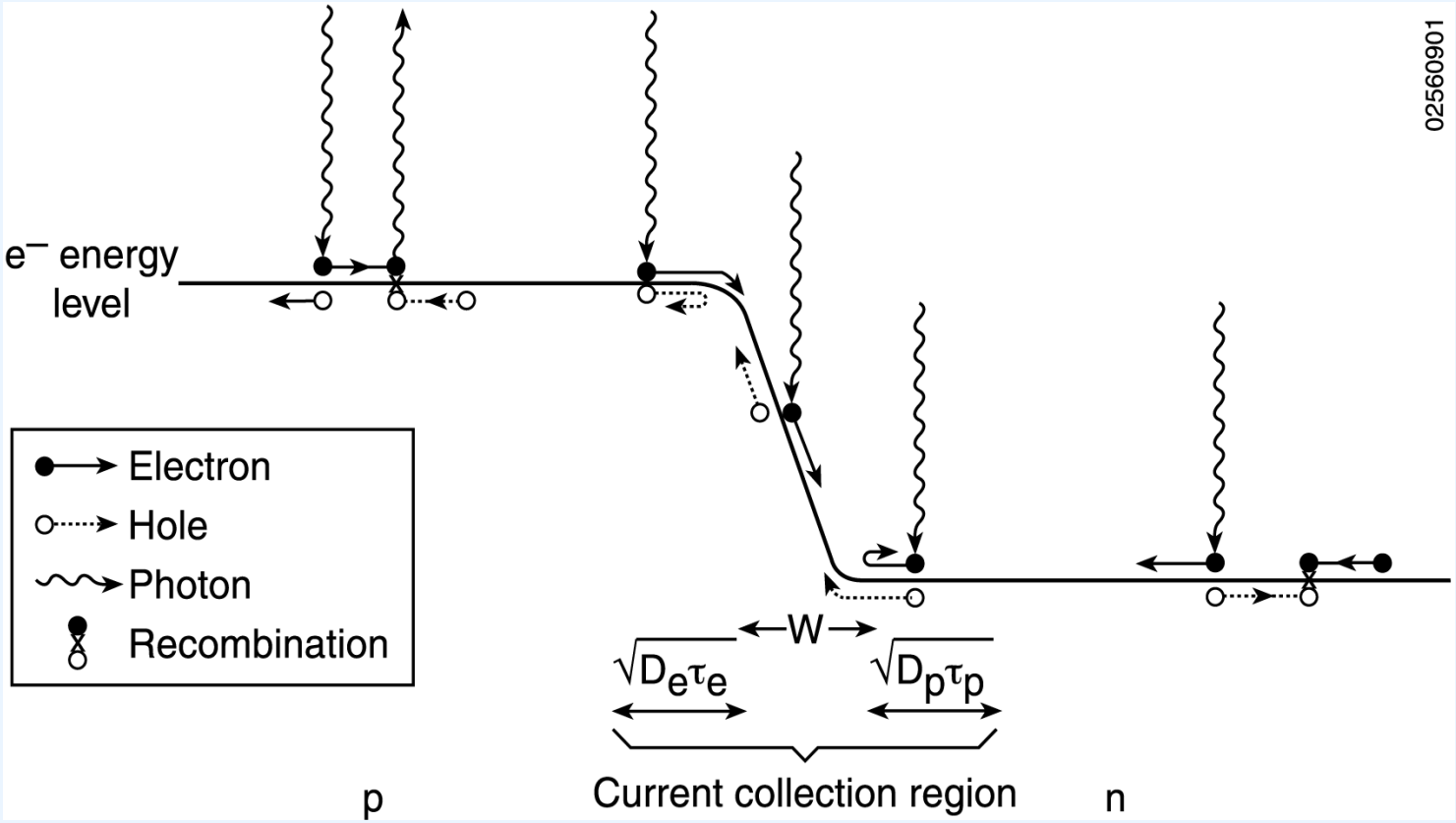
V_{oc} and lifetime

For various homojunction and heterojunction models,

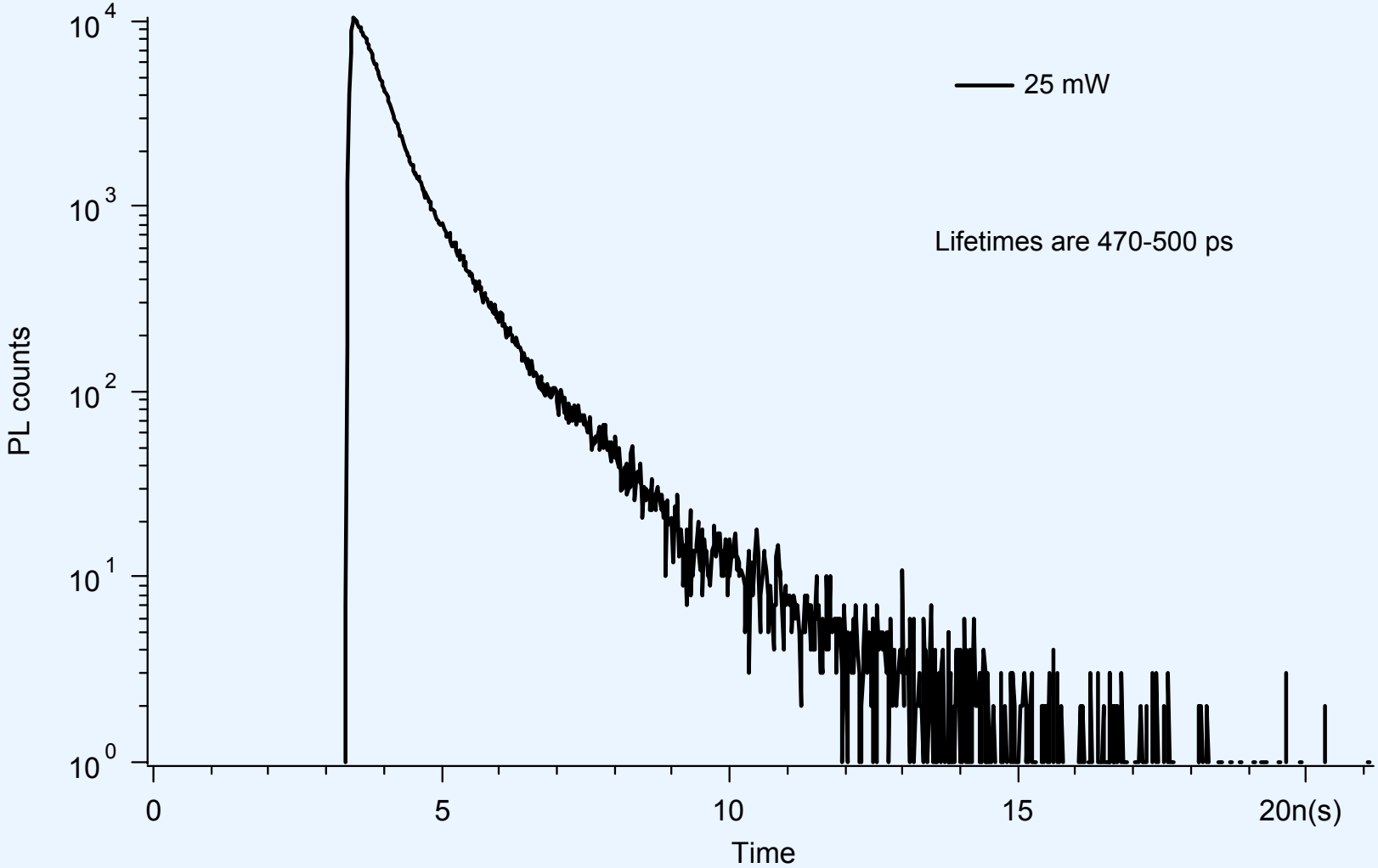
$$J(V) = J_o(e^{qV/nkT} - 1) - J_{sc}$$

Time-resolved Photoluminescence

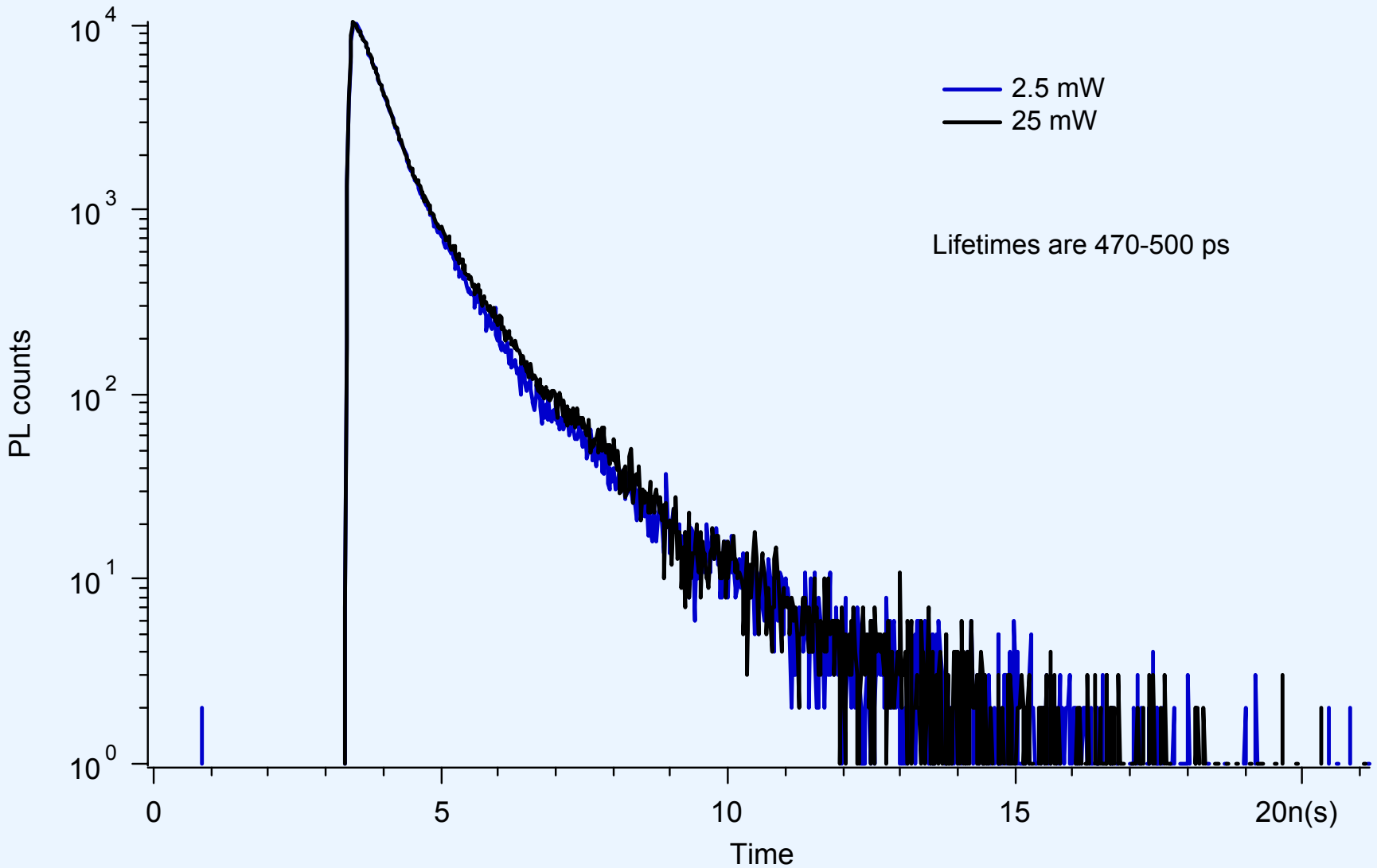
- Inject excess carriers into a sample with a laser pulse to excite photoluminescence
- Watch the photoluminescence intensity decay
- Use a semiconductor diode, single photon counting, up-conversion TRPL


02560901
e⁻ energy level
Electron
Hole
Photon
Recombination
W
$\sqrt{D_e\tau_e}$
$\sqrt{D_p\tau_p}$
Current collection region
p
n

Injection level



Injection level



Indicative facts and device model

University of Toledo

Presented by V. G. Karpov

Contributions by

D. Shvydka, L. Cooray, J. Drayton, and A. D. Compaan

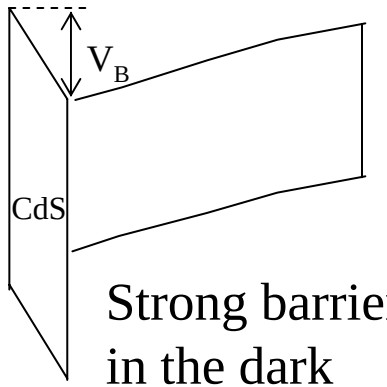
Summary

- Indicative facts help to shape the model
- It is not a p-n junction, rather MIS
- Field reversal in CdS
- No significant SRH recombination
- Losses due to the barrier and nonuniformity
- Practical importance of CdS & interfaces

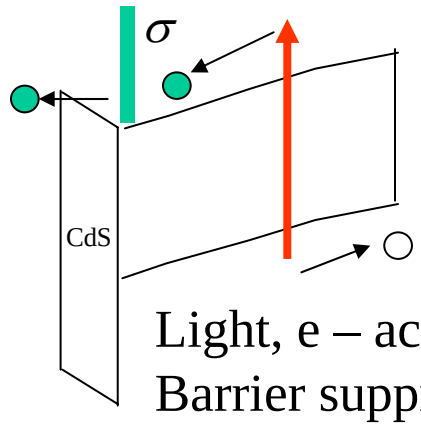
Indicative facts

Observation	Implication
Interactive processing (*e.g.* everything has to be reoptimized with a new HRT) (*Bolko's generalization).*	Strong interactions between layers; thickness smaller than depletion widths; shunting-like phenomena
Lack of carrier collection from CdS *(General: Handbook of PV, etc.)*	Small diffusion length in CdS? Invalid observation? Field reversal?
Reach-through, morphology dependent effects of buffer layers *(Roussillon et. al. 2004; Ferekides et. al. 2005)*	Insulating CdS
Negative QE for thick CdS with filtered blue light *(S. Hegedus et. al. 2000)*	Field reversal in CdS?
Pressure dependent PV performance attributable to the piezo parameters of CdS *(Shvydka et. al.*)	Insulating CdS. CdS grains as electric dipoles. Energetically favorable grain orientation predicts CdS field reversal.

Reverse field Model



Strong barrier
in the dark



Light, e – accumulation,
Barrier suppression

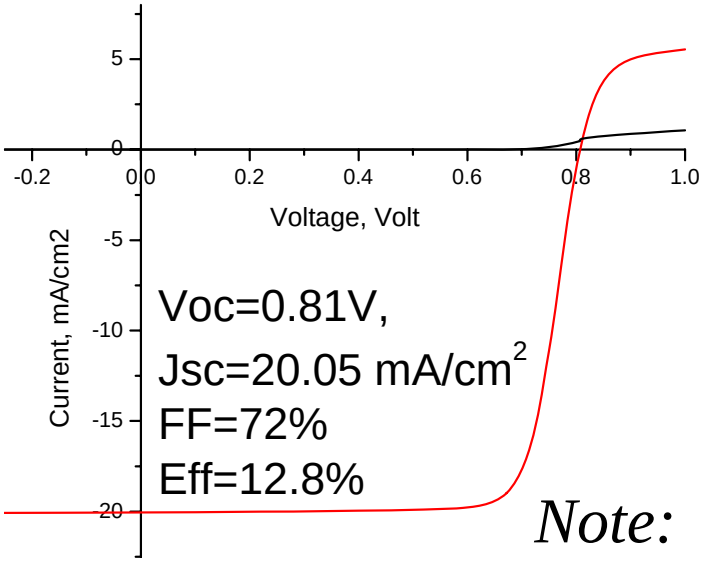
- No collection from CdS (field reversal)
- QE<0 in blue light and thick CdS
- Barrier suppression under the light similar to CdS photoconductivity
- Light to dark JV crossing
- Consistent with Piezo effect

See: M. L. C. Cooray and V. G. Karpov, Appl. Phys. Lett. **88**, 093508, (2006)

New device equation
(Analytical solution numerically verified)

$$J = J_{S1} + J_{L1} - \frac{J_{L2} + J_{S2} + J_{L1} + J_{S1}}{1 + \left(J_{S2} / J_{S1}\right)\exp(qV / kT)} - J_R$$

Example



- Explicit expressions for:

  Jsc, R_{sh} and $R_{s,}$ JV crossing etc.
- Losses due to the barrier

Note:

no recombination

– Yet, realistic parameters

Recombination: SRH irrelevant (1)

- Two lifetimes: τ_d (drift) and τ_r (recombination)
- Either $\tau_d >> \tau_r$ or $\tau_d << \tau_r$,

  but not $\tau_d \sim \tau_r$ (different physics involved)
- If $\tau_d >> \tau_r$,

  then most carriers disappear, QE<<1 – never observed
- If $\tau_d << \tau_r$,

  then recombination can be neglected
- Only $\tau_d << \tau_r$ acceptable:

  SRH recombination negligibly small

Recombination: SRH irrelevant (2)

- In the existing AMPS and SCAPS modeling,

  $\tau_d \sim \tau_r$

  in order to explain losses and yet not to kill QE, Jsc.

- This miracle is assumed for all technologies and processes (CdTe, CIGS)

- Cannot be a valid assumption: defects and τ_r differ a lot

Recombination: SRH irrelevant (3)

- Based on dc photoconductivity ($\Delta\sigma/\sigma \sim 10 - 1000$),

  $\tau_r \sim 10^{-4} – 10^{-6}$ s

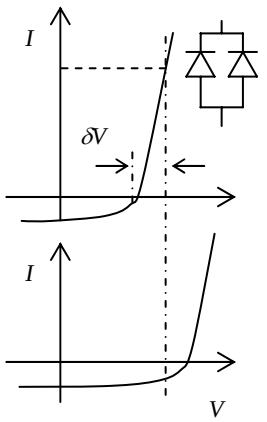
  (much shorter TRPL τ likely due to e-h separation, not recombination)

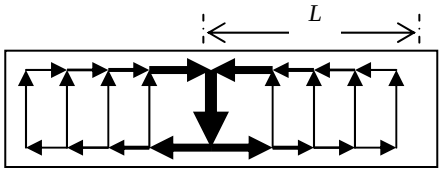
- Based on carrier mobility, $\tau_d < 10^{-9}$ s

- Once again $\tau_d << \tau_r$:

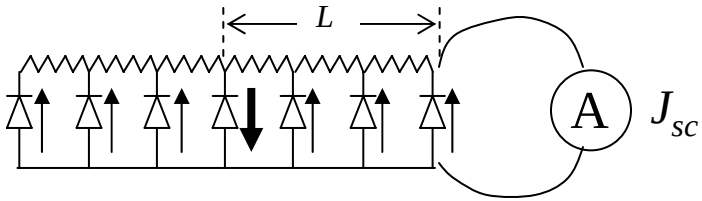
  SRH recombination negligibly small

Nonuniform recombination rather than SRH (weak diodes)

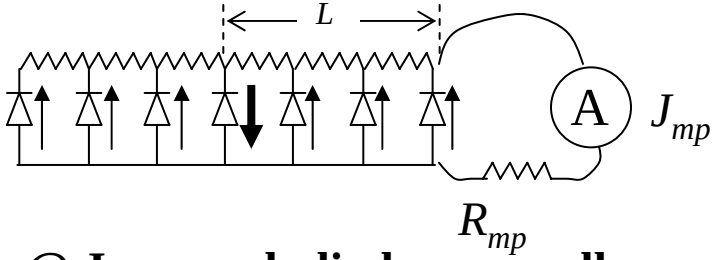




Current robbing by weak diodes



@ Jsc weak diodes are blocked by TCO resistance: No Jsc loss



@ Jmp weak diodes are well connected compared to Rmp: Jmp, Voc and FF loss

Weak diodes hurt V_{oc} and FF, but not J_{sc}

Practical implications

- Interfacial properties/morphology of CdS important
- Hence, buffer layer morphology
- Depleted, yet conductive CdS to minimize barrier loss
- Hopping conduction, defective (amorphous) CdS
- Avoid weak diodes to keep Voc and FF up
- Avoid pinholes in CdS and CdTe
- Bad spots on the back surface especially detrimental

Conclusions

- Indicative facts help to shape the model
- It is not a p-n junction, rather MIS
- With field reversal in CdS
- No significant SRH recombination
- Losses due to the barrier and nonuniformity
- Practical importance of CdS & interfaces

Impact of Lifetime and Back-Contact Barrier on CdTe Current-Voltage Curves: Simulation of Commonly Seen Features

Jim Sites, Jun Pan,and Markus Gloeckler*
Colorado State University

*now at First Solar, LLC

Assumptions

(1) Hole density is in the 10^{14} range (based on evaluation of capacitance measurements from a large number of cells).

(2) Lifetime (average time until a photoexcited or forward-current electron recombines) is in the 1 ns range (need to compare with time for electron to cross junction).

(3) Back barrier is between 0.3 and 0.7 eV.

0.3 eV does not affect J-V

0.4 eV has very minor effect on J-V at RT

0.5-0.7 eV progressively distorts J-V

(4) CdS is sufficiently photoconductive that its dark Fermi level is not an issue.

(5) Uniformity is not limiting voltage for best cells.

(6) Absorbers are thicker than two microns.

Discussion of Lifetime

Inverse Lifetime =

Density of the primary trap x Cross section x Thermal velocity

It can be varied in a simulation either by changing the trap density or the cross section. The former is favored from a physical point of view.

The magnitude of electron lifetime must be larger than the exit time of a photogenerated electron, or collection will suffer. Back-of-the-envelope calculation of exit time:

Drift velocity = Mobility x Field ~ 100 cm^2/Vs x 5000 V/cm = 500,000 cm/s

Exit time = Absorption depth/Drift velocity ~ 0.00002 cm/500,000 cm/s

~ 0.04 ns

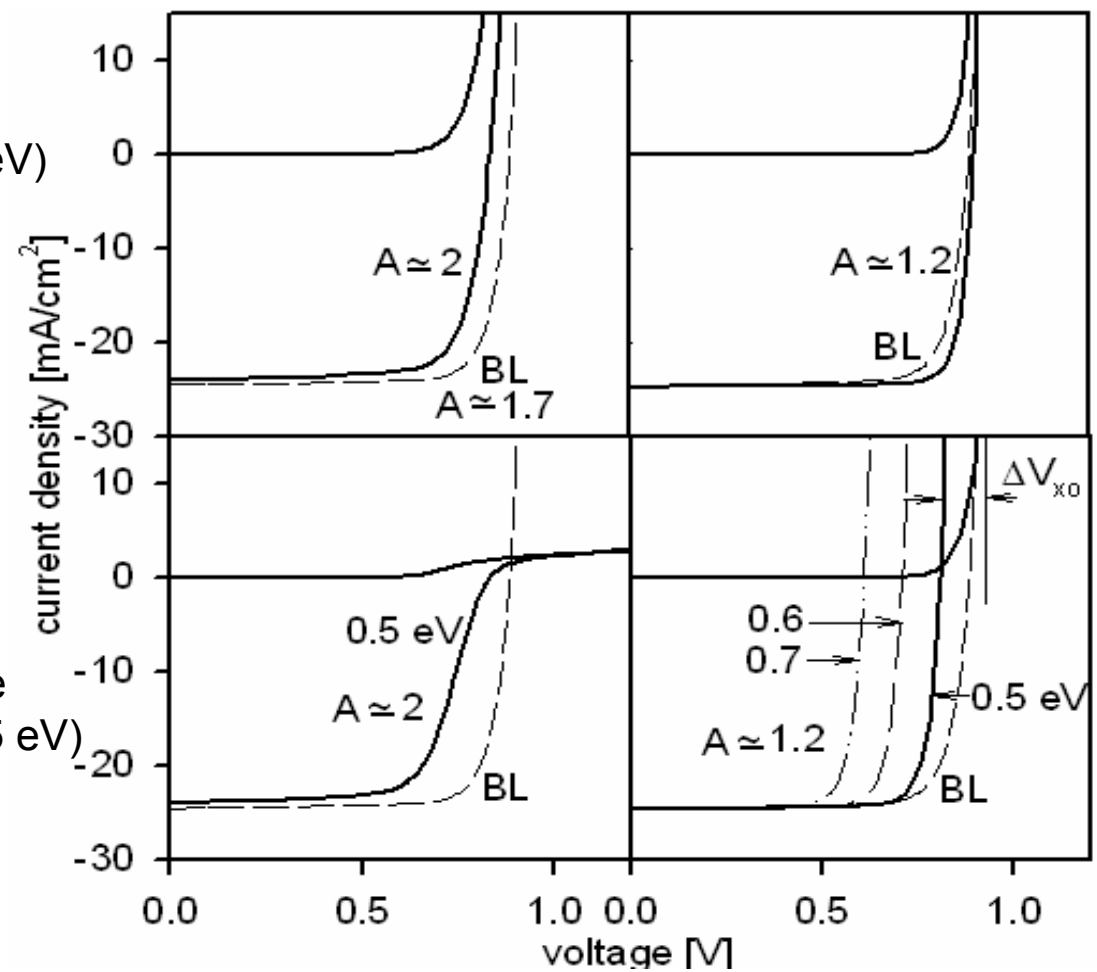
Hence, lifetimes below 1 ns will start to impact J-V

Four Cases (Dashed Baseline for Reference)

p = $2x10^{14}$; d = 4μm BL lifetime 0.5 ns; low and high mean factor of 10

Low Lifetime
Low Barrier (0.3 eV)

High Lifetime
Low Barrier



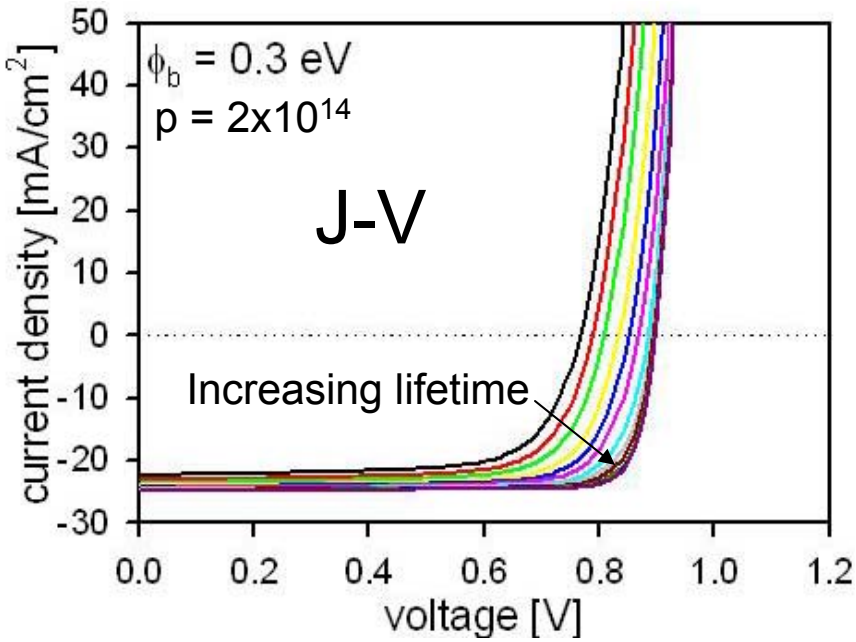
Low Lifetime
High Barrier (0.5 eV)
"rollover"

High Lifetime
High Barrier

Simulations
using AMPS

Variations in Lifetime (low barrier)

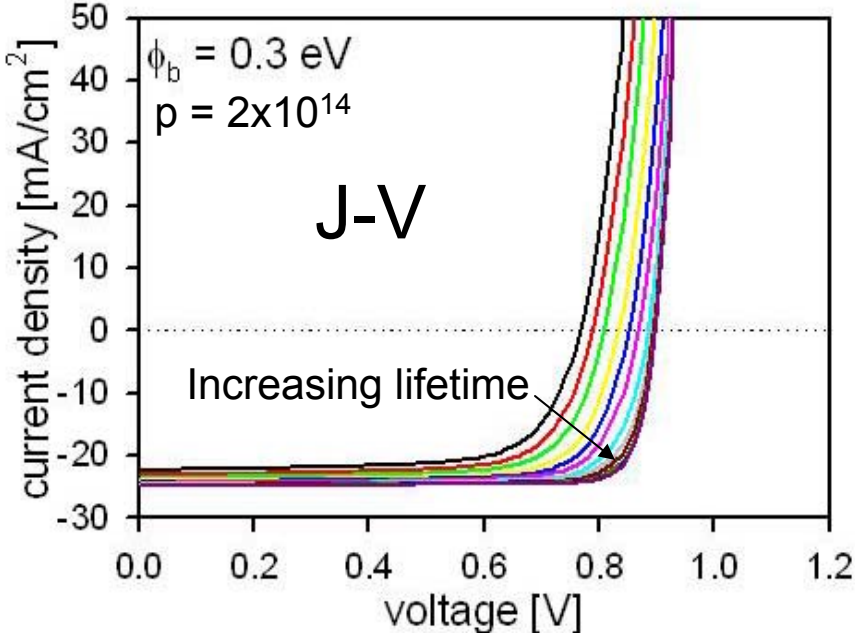
CdTe lifetime variation from
0.005 to 50 ns (simulation)

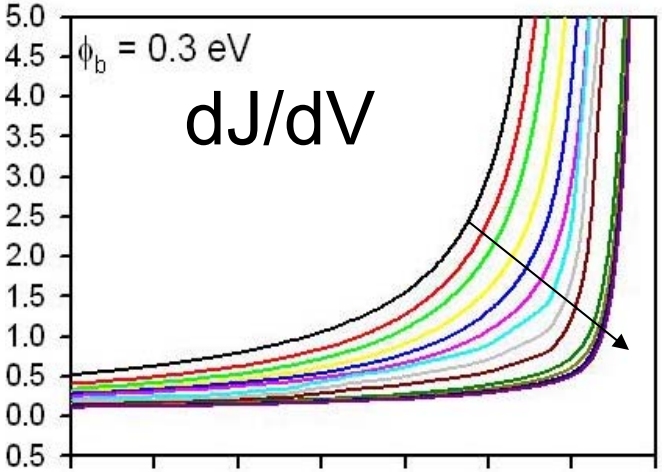


Note: 0.5 ns (middle curve)
corresponds to 16.5% record cell

Variations in Lifetime (low barrier)

CdTe lifetime variation from 0.005 to 50 ns (simulation)

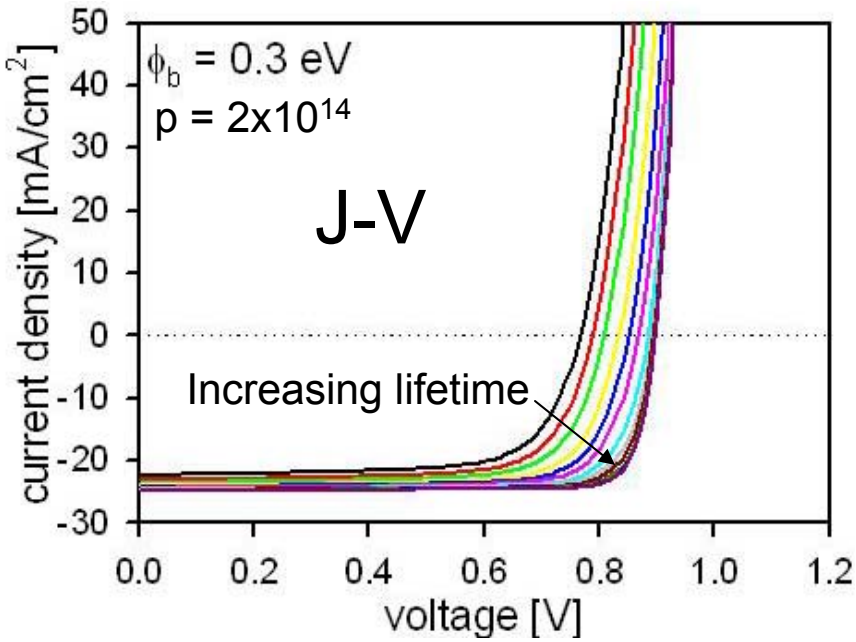


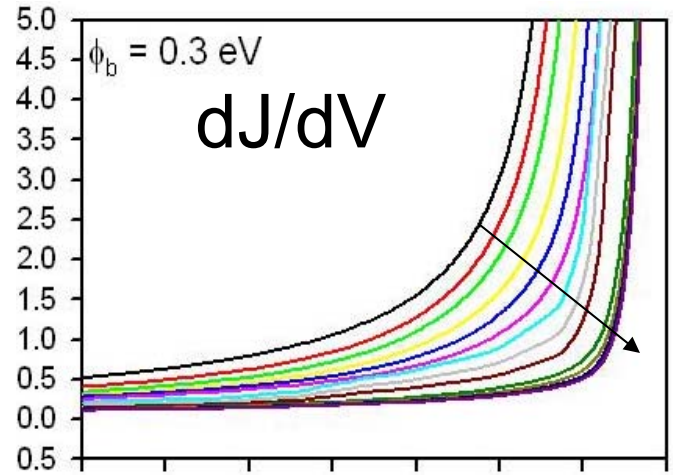


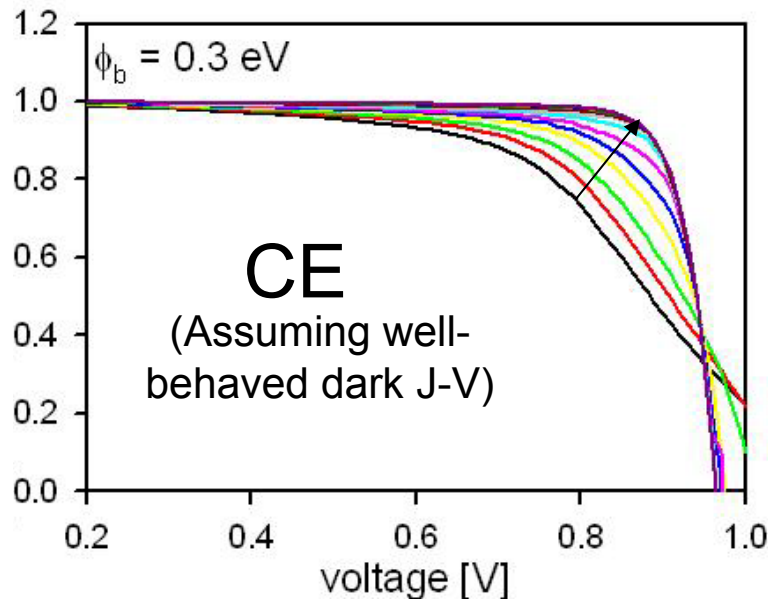
Note: 0.5 ns (middle curve) corresponds to 16.5% record cell

Variations in Lifetime (low barrier)

CdTe lifetime variation from 0.005 to 50 ns (simulation)



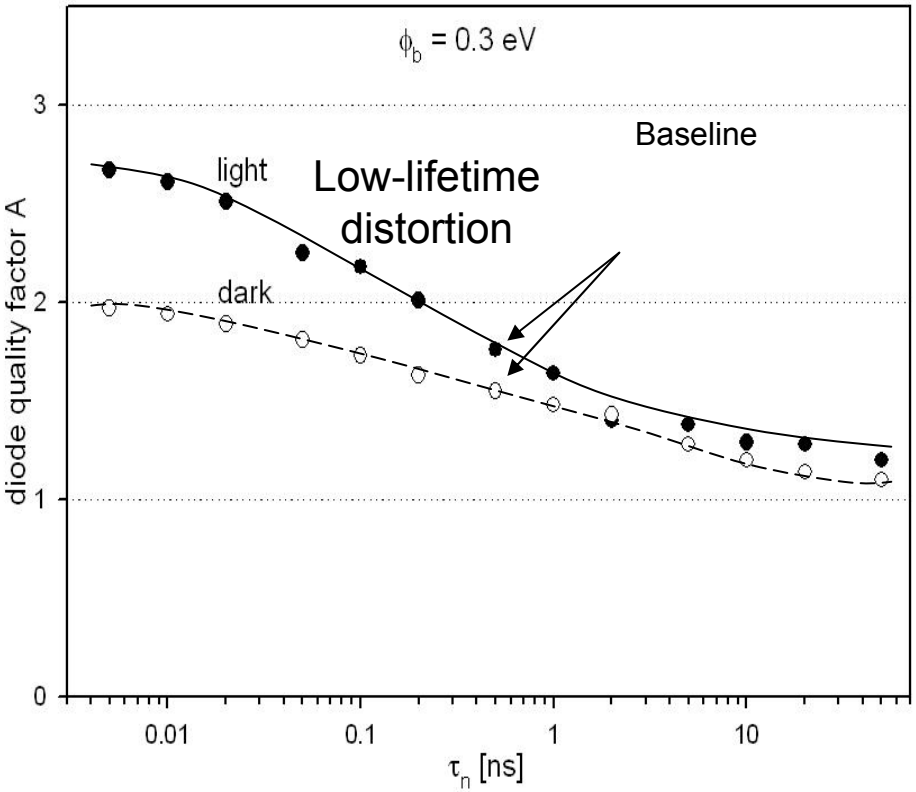




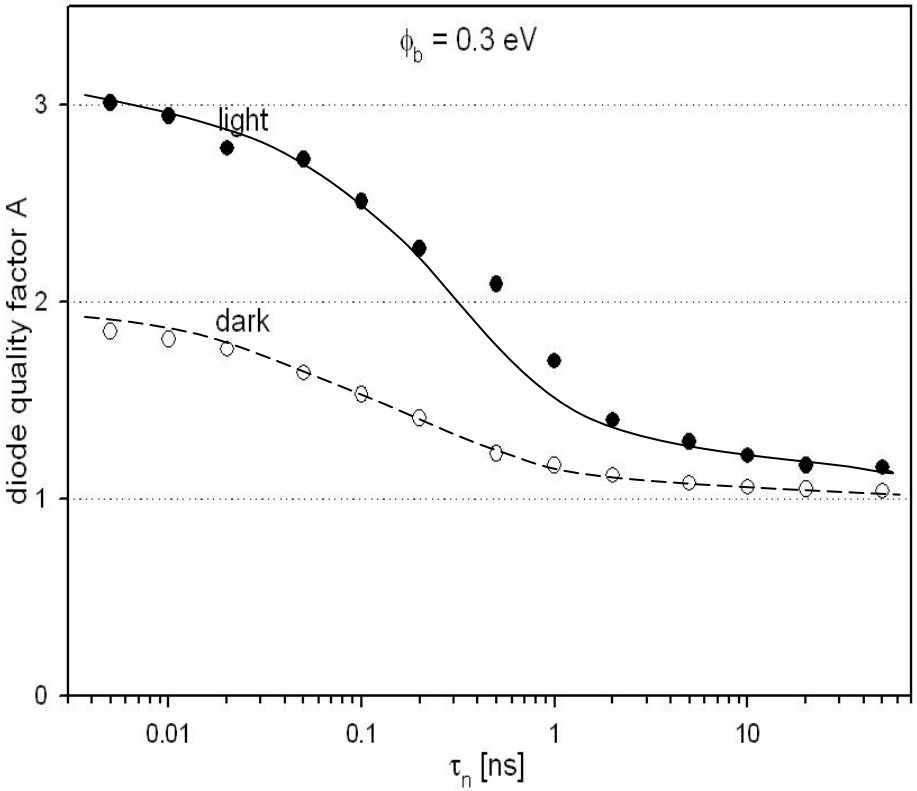
Note: 0.5 ns (middle curve) corresponds to 16.5% record cell

One Consequence: Unphysical A-factors

$p = 2x10^{14}$



$p = 2x10^{16}$

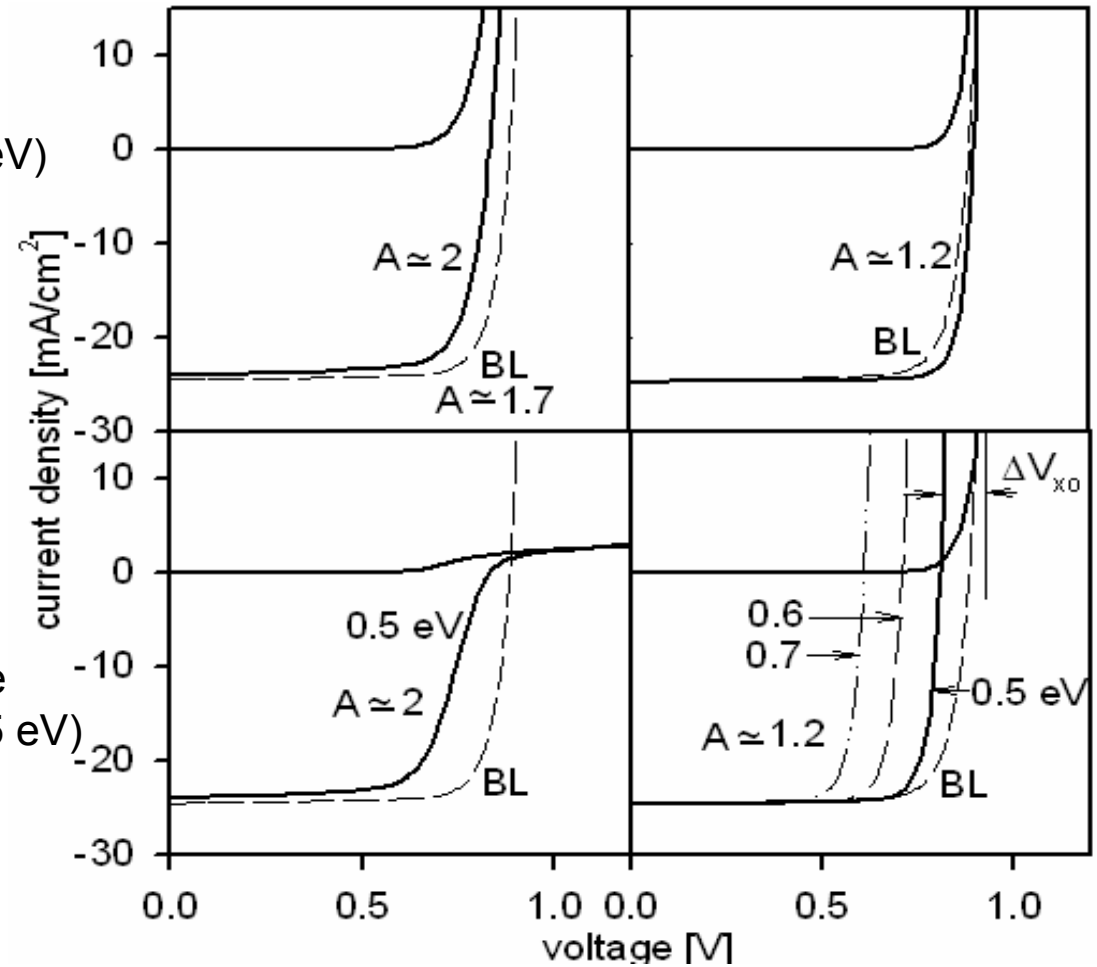


Now Focus on Bottom Two (high barrier)

p = 2×10^{14}; BL lifetime 0.5 ns; low and high mean factor of 10

Low Lifetime
Low Barrier (0.3 eV)

High Lifetime
Low Barrier



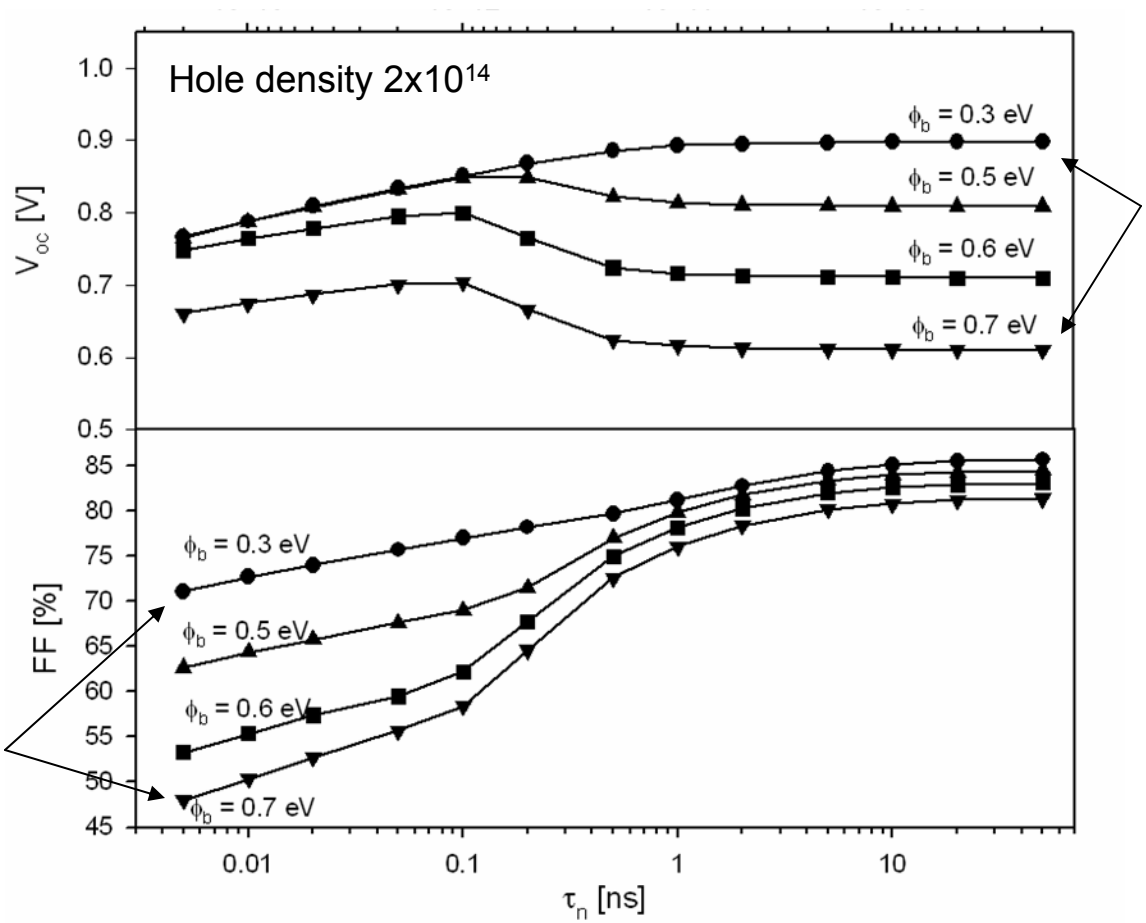
Low Lifetime
High Barrier (0.5 eV)
"rollover"

High Lifetime
High Barrier

Colorado State University

Combined lifetime and barrier effects

Curves flatten at large lifetimes

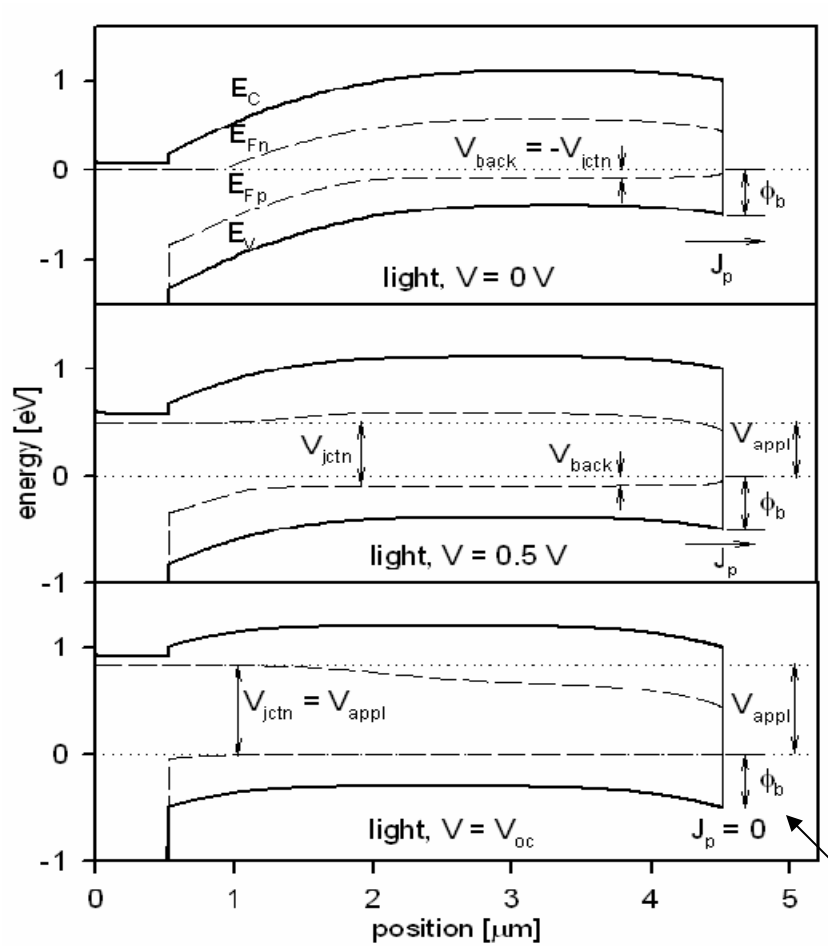


Voltage Reduction Effect

Rollover Effect

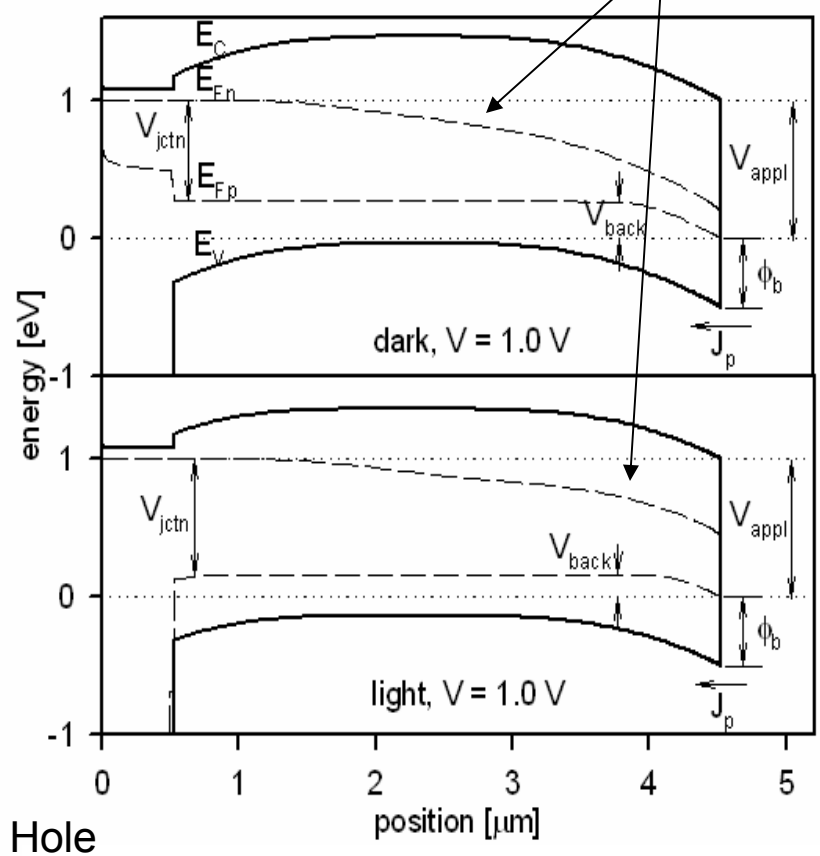
Rollover Region (low lifetime, high barrier)

Increasing Voltage (light on)



First quadrant dark/light

Electron density very low



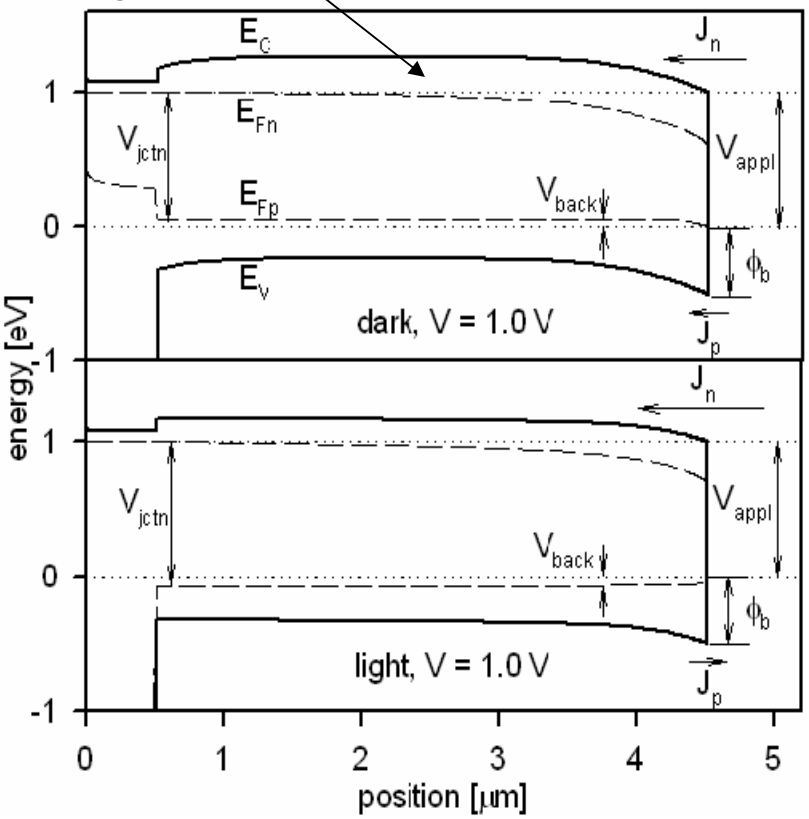
Hole Impedance Increases

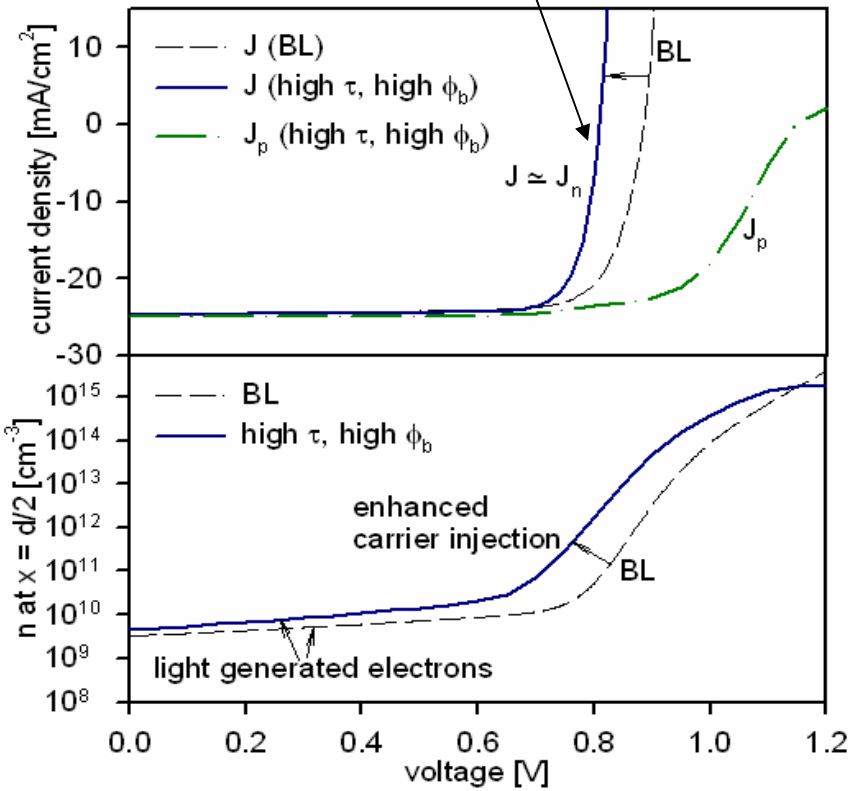
Reduced Voltage Region: Electron Enhancement

Electron Density High

Larger forward current means reduced voltage

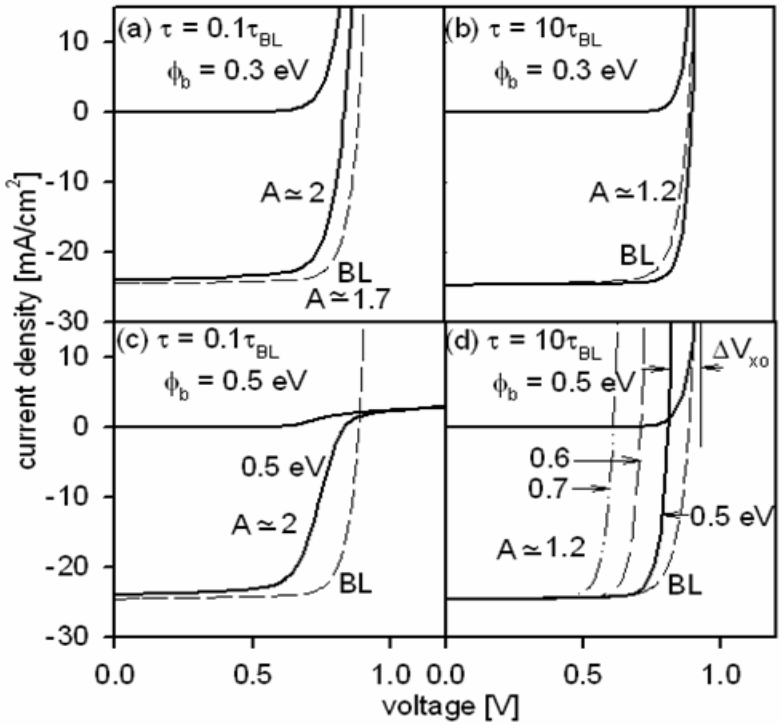
Large Forward Current (Electrons)

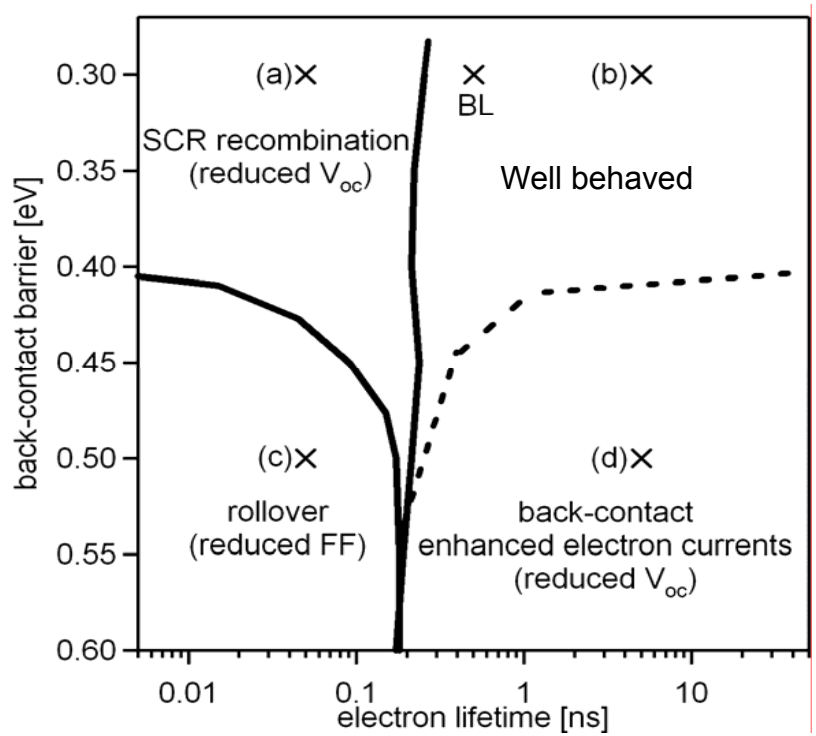




Overlap of primary and back depletion not required

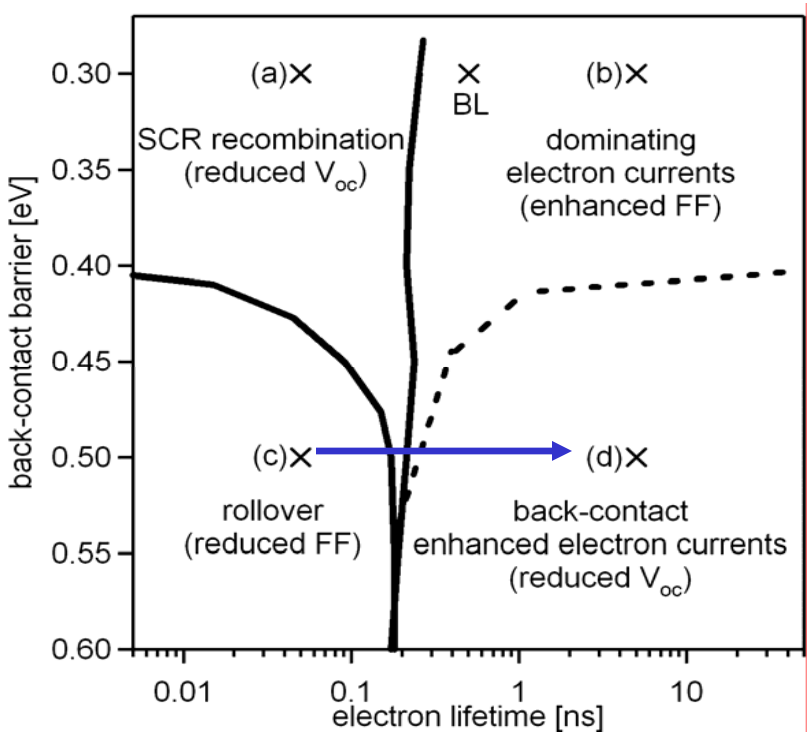
Division of Lifetime/Barrier Space

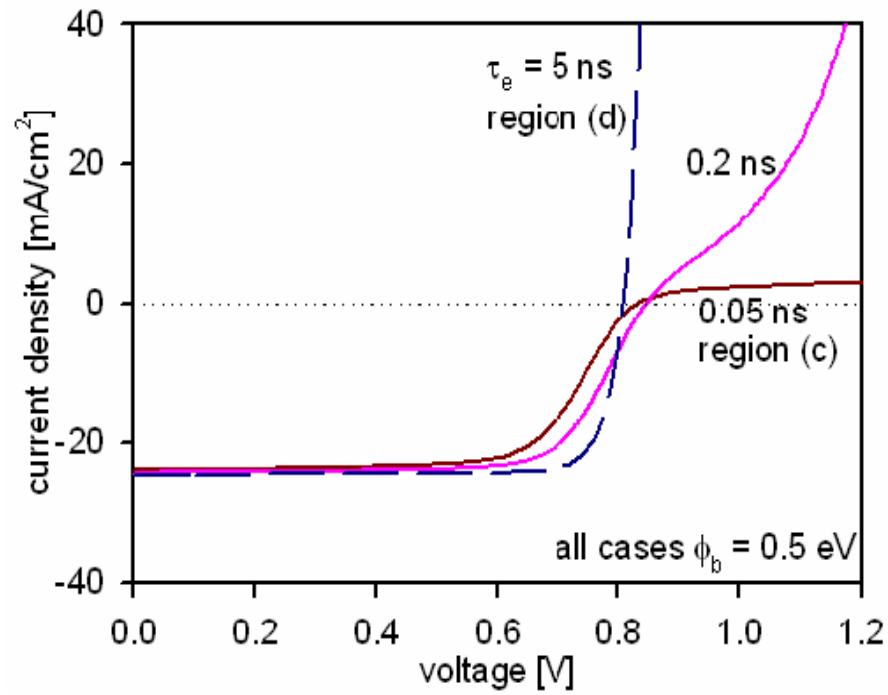




Is there an orderly transition between the two bottom regions?

Transition from Rollover to Voltage Reduction





Conclusions

(1) Reduction of CdTe lifetime, with a small barrier, reduces voltage and fill factor.

(2) Increase in CdTe lifetime, again with small barrier, increases fill factor, but does not significantly increase voltage.

(3) The combination of low lifetime and larger barrier yields the rollover effect.

(4) The combination of high lifetime and barrier yields large electron densities and hence large forward current and reduced voltage.

(5) There is no obvious need for a non-standard device model.

PRESENTATIONS FROM

STABILITY SUBTEAM

Modes and Mechanisms – An Update

National CdTe Team Meeting

Denver, CO March 9-10, 2006

Stability Subteam Presentations

NREL

CSU

USF

General observations or “Modes” of the Accelerated Aging Testing in Photovoltaics Meeting

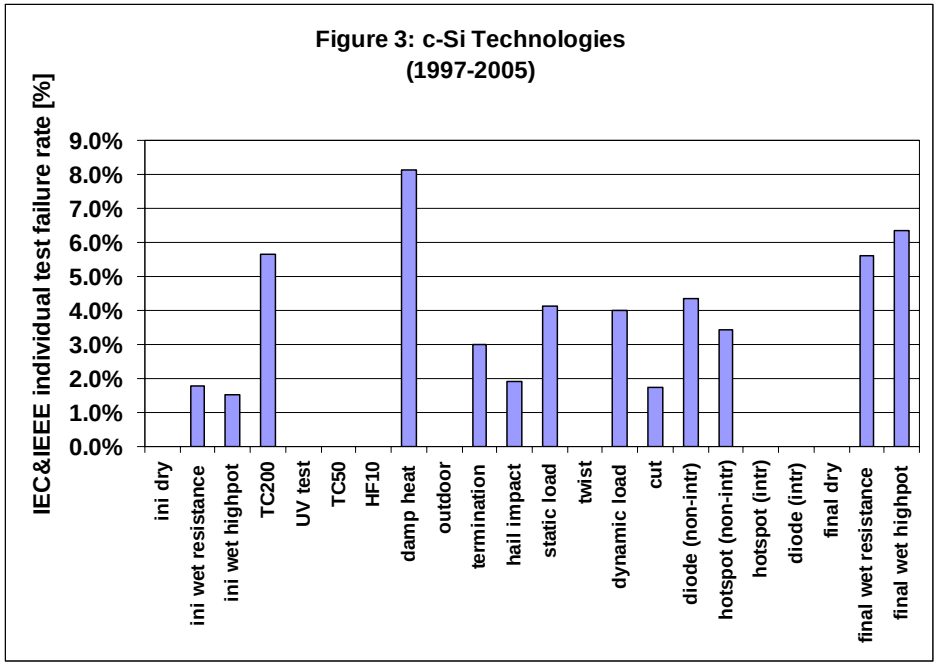
(Maritime Institute, Maryland, Feb 22-23, 2006)

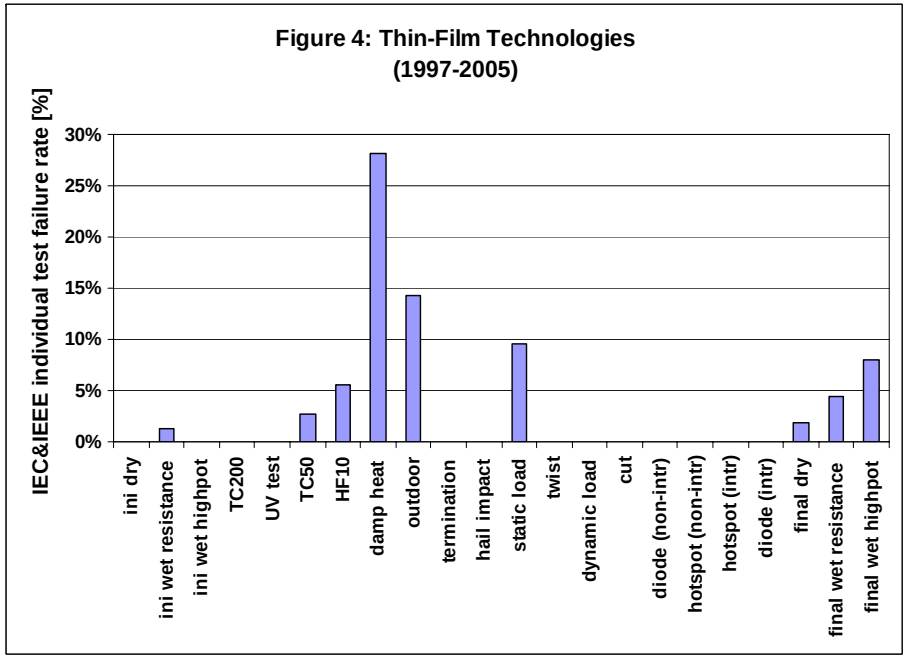
- PV reliability is gaining increased importance to manufacturers.
- DOE is actively pursuing input from manufacturers.
- First Budget proposal reflects both of the above (reliability as a “fundamental” research area) as do the Solar America Initiative and Technology Pathway Partnership approaches)
- Stability and Reliability are being considered within various product development models (e.g. stage-gate process) for approving research dollar support for PV.
- Of course, all of the above applies to what we currently do best, e.g., improve device performance and manufacturing (e.g. NOPI).
- We are early in the decision process; congressional approval still required, then there are the ear-marks.

The basic “mechanism” behind the “mode”

IEC and IEEE Qualification Test Programs – A Failure Rate Analysis
(1997-2005 @ ASU-PTL)

ref: Mani Tamizh-Man, Director





Notice different scales of failure rates between crystalline and thin-film technologies

Thin-Film technologies don’t have as many ways of failing.

Primary thin-film “problem areas”: damp heat, outdoor, and static load failures

(3) Break-out Sessions
Device Stability Breakout Summary

- **Understand mechanisms**. Reliability focuses on modes and mechanisms. Modes are what you see (decreased Voc, IR hot spots, TCO delamination). Mechanisms are the science behind it (recombination, shunting, Na-outdiffusion) Modeling of degradation.
- **Minimodules**. This will shorten the "relevancy" distance between device-level research and actual field testing. Less cumbersome approach; better statistics; better reproducibility
- **Databases**. "Central" depository of stability related data with universal access (safety important) suggested to organize work from different groups. To facilitate concensus.
- **Faster acceleration tests**. Industry wants this badly. Silicon functions because it has 30 years of field data. Thin films do not. See earlier work by UT and CSU.
- **Applicable screening tests or protocols** to qualify "reliability" in the eyes of the consumer. Existing qual tests derived from work on Silicon. Not applicable to thin films. "1" universal test improbable.
- **Layer-specific tests.** Don't have to do just devices. Need *fundamental* understanding regarding how films and device-level components react to light, temperature, fields, humidity, shear stresses, by-products of encapsulant decomposition, etc.
- **"Big Box" additions to program.** STF will produce large-area films (6" x 6") of good uniformity. Fabrication basis for mini-modules? Big boxes: 1) automated large-sample stability tool to test devices/mini-modules under different bias, illumination, ambient, temperature, 2) tools for doing interconnect development and study, 3) new diagnostic approaches

Stability Subteam Presentations

- Alan Davies – Effects of Cu and $CdCl_2$ on Stability and Uniformity of CdTe Solar Cells
- Chris Ferekides – Stress Studies of CdTe devices: Intentional Cu in CdS vs Backcontact
- Michael Kempe - Effects of Encapsulation on CdTe based Device Performance
- Dave Albin – Temperature-dependent degradation in CdTe devices – you betcha!

Colorado State University

Effects of Cu and $CdCl_2$ on Stability and Uniformity of CdTe Solar Cells

Alan Davies
Physics Dept.
Colorado St. University

Thanks to:
Jim Sites for project oversight
W.S. Sampath group for cells used in this study
NREL for project funding

Outline

Colorado State University

- Motivation and Background
- Experimental
- Discussion
  - Uniformity
  - Stability
- Conclusions

Motivation/Background

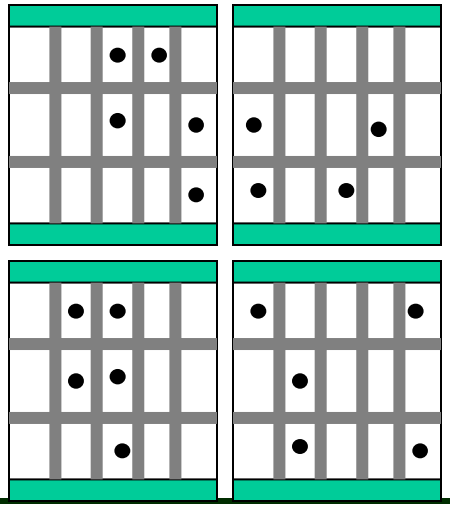
Colorado State University

- Should Cu be used or not?
- Can optimized $CdCl_2$ treatment ensure stability?
- S.E. Asher, et. al., "Determination of Cu in CdTe/CdS Before and After Accelerated Stress Testing," *28th IEEE PVSC*, (2000), pp. 479-482.
  - More Cu => more degradation with stress
- A.O. Pudov, et. al., "Effect of Back-Contact Copper Concentration on CdTe Cell Operation," *Proc. 29th IEEE PVSC, New Orleans, LA* (2002), pp. 760-763.
  - More Cu => better stability, better uniformity
- Cu, in conjunction with $CdCl_2$, affects carrier lifetime and back barrier height

Experimental

- Device Set
  - Two variables: Cu, $CdCl_2$ treatment
- Initial Characterization (all devices)
- Stressing
- Re-Characterization (subset)

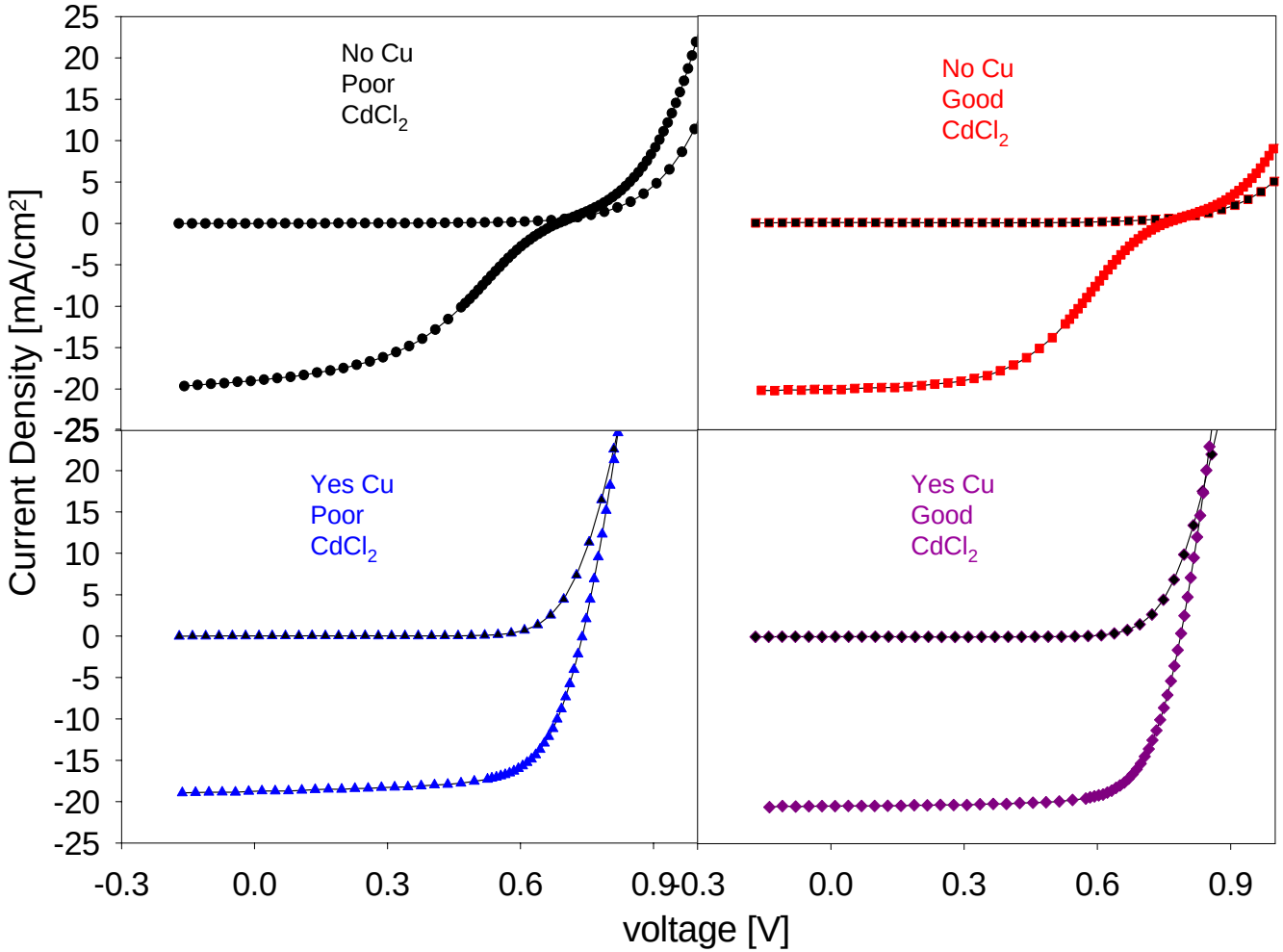
No Cu Poor $CdCl_2$	No Cu Good $CdCl_2$
Yes Cu Poor $CdCl_2$	Yes Cu Good $CdCl_2$



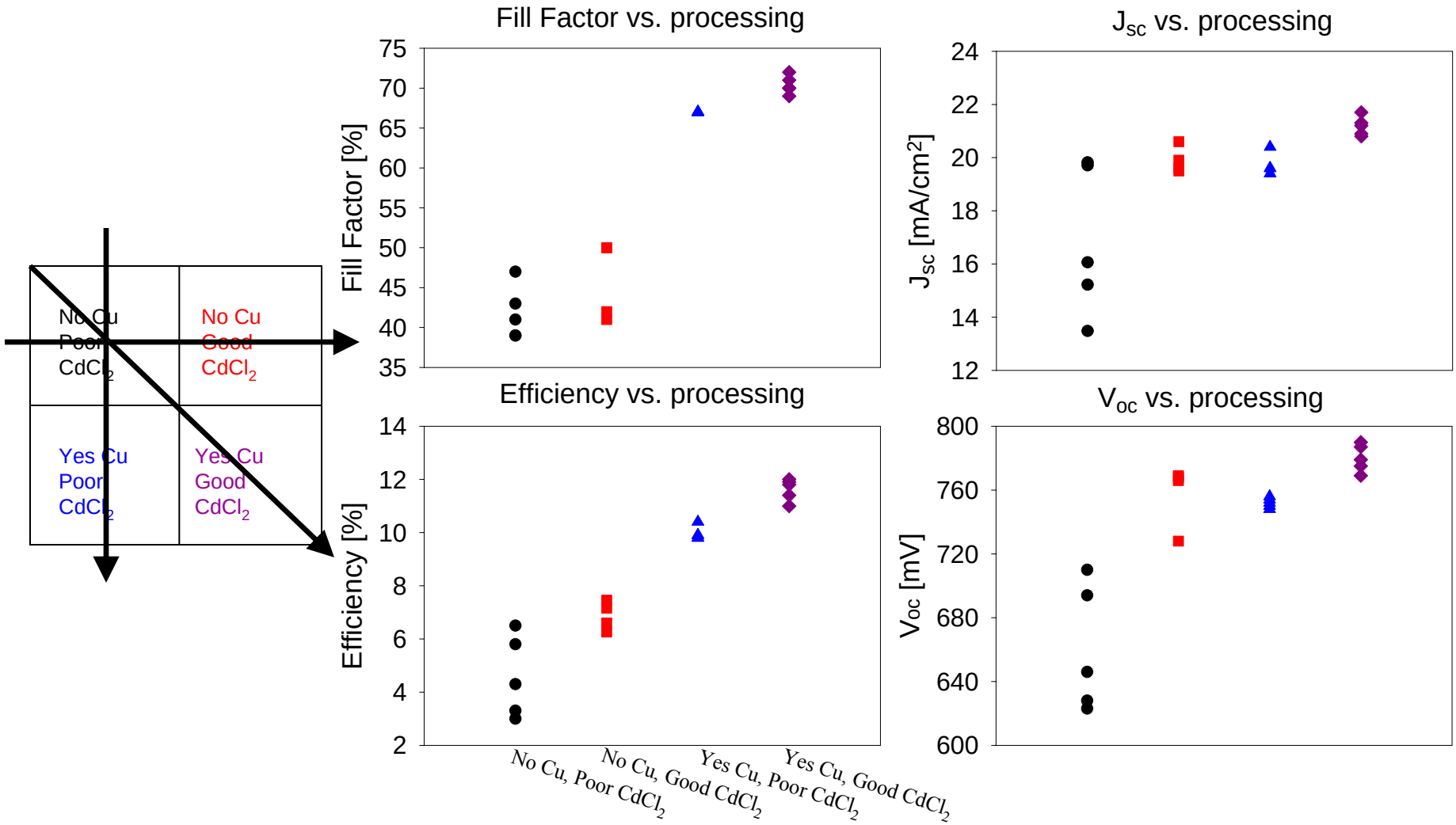
Random sample set

Initial J-V behavior

No Cu Poor $CdCl_2$	No Cu Good $CdCl_2$
Yes Cu Poor $CdCl_2$	Yes Cu Good $CdCl_2$

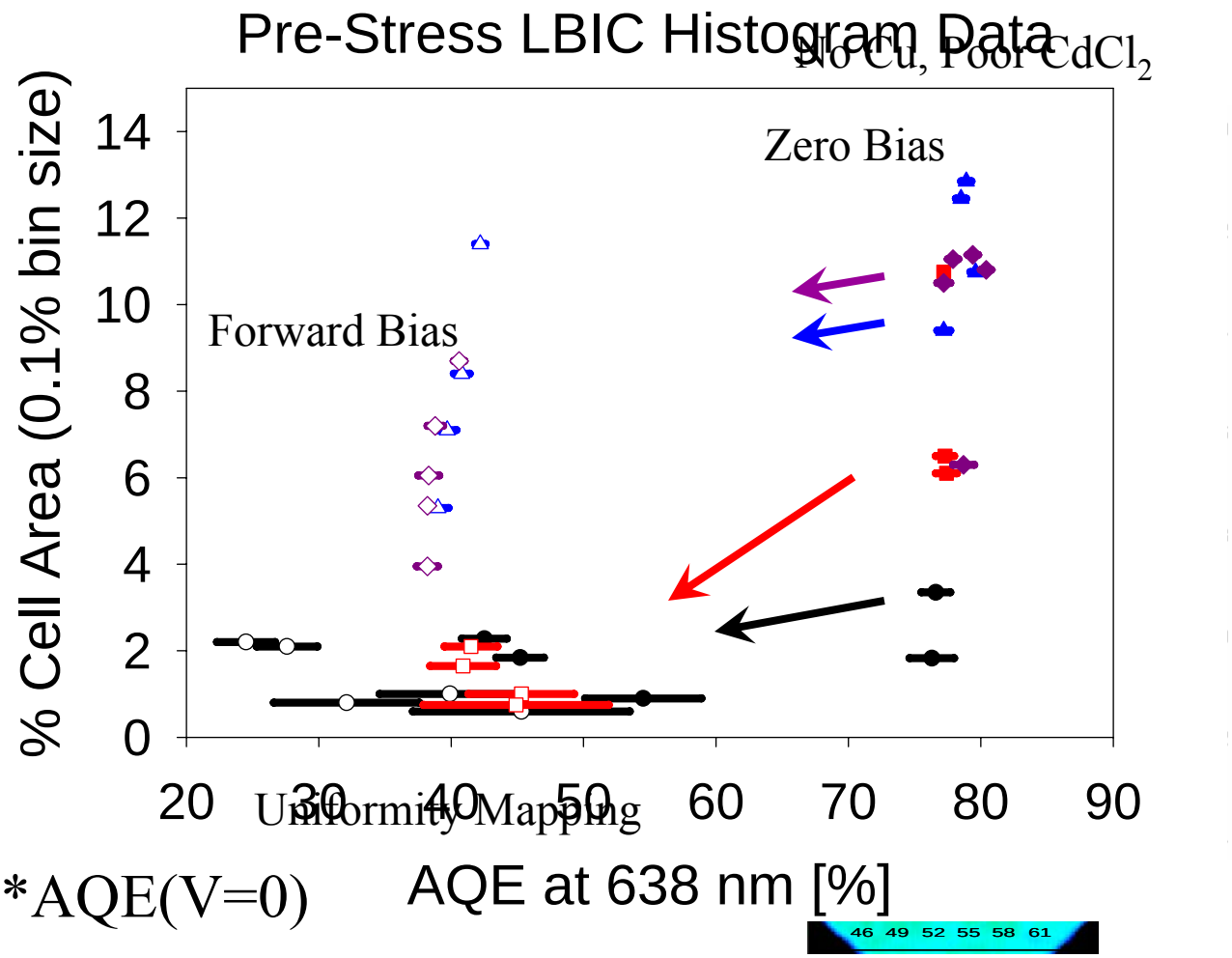


Initial Performance



Initial Uniformity

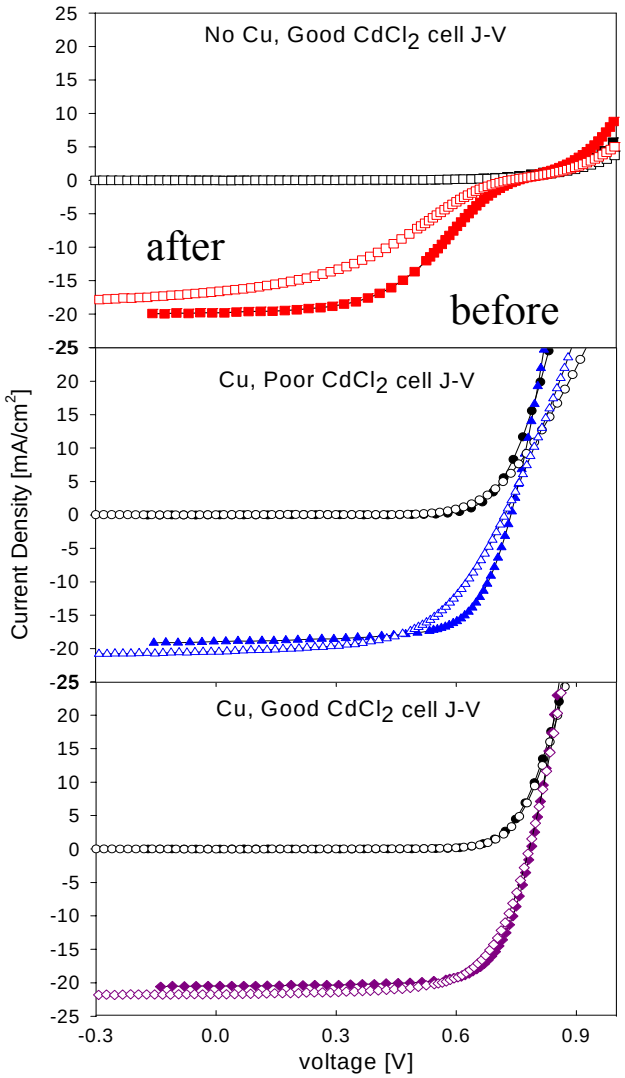
No Cu Poor $CdCl_2$	No Cu Good $CdCl_2$
Yes Cu Poor $CdCl_2$	Yes Cu Good $CdCl_2$



Bias Condition:

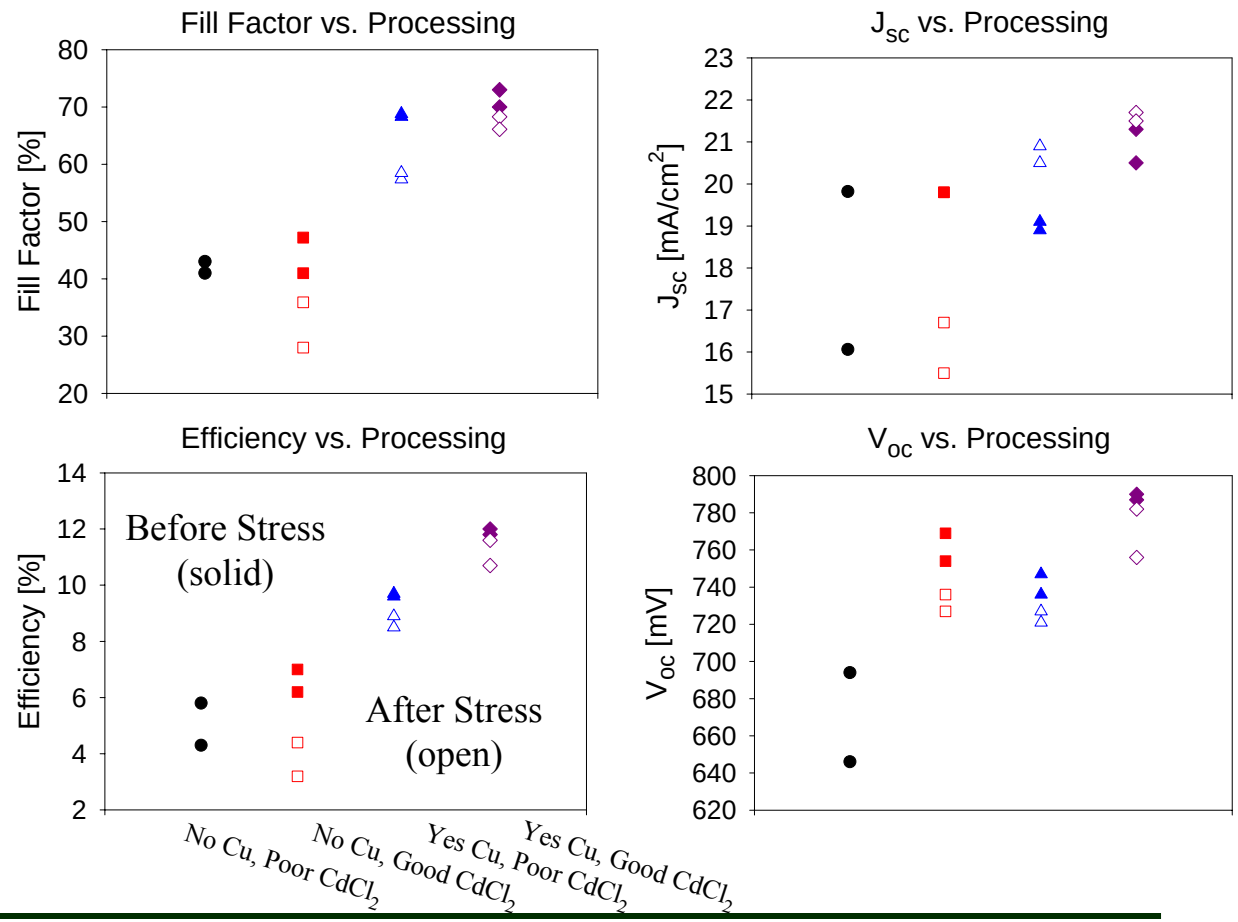
AQE(bias) ≈ 0.5*AQE(V=0)

J-V Response to Stress



Conditions: 65°C, OC, 5 hr./3 hr. on/off illumination

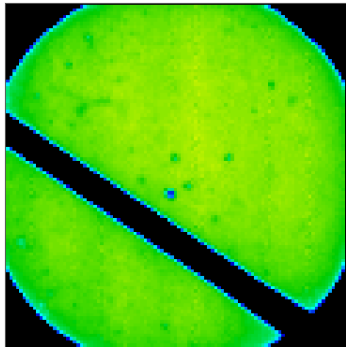
Filled Symbols: Pre-Stress, Open Symbols: Post-Stress



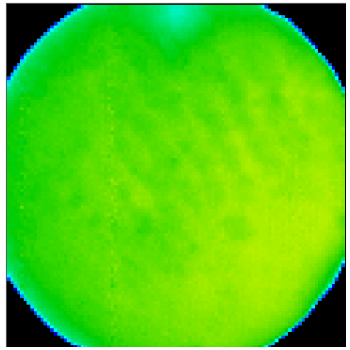
Uniformity comparison with stress

Before Stress

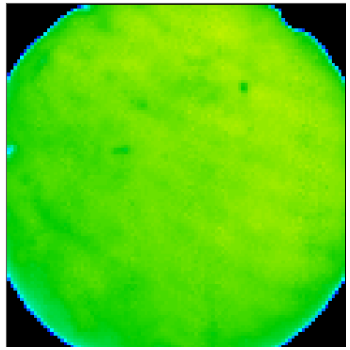
Color Scale: Δ = 1% AQE



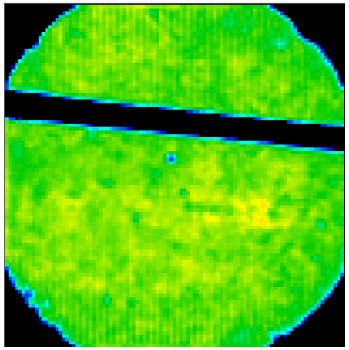
No Cu, Good $CdCl_2$

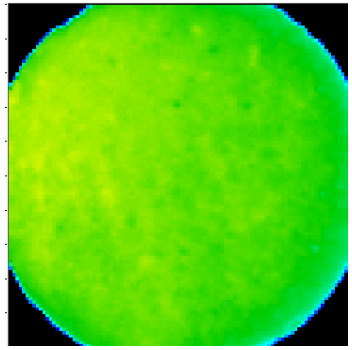


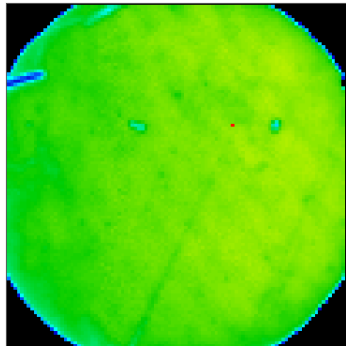
Yes Cu, Poor $CdCl_2$



Yes Cu, Good $CdCl_2$





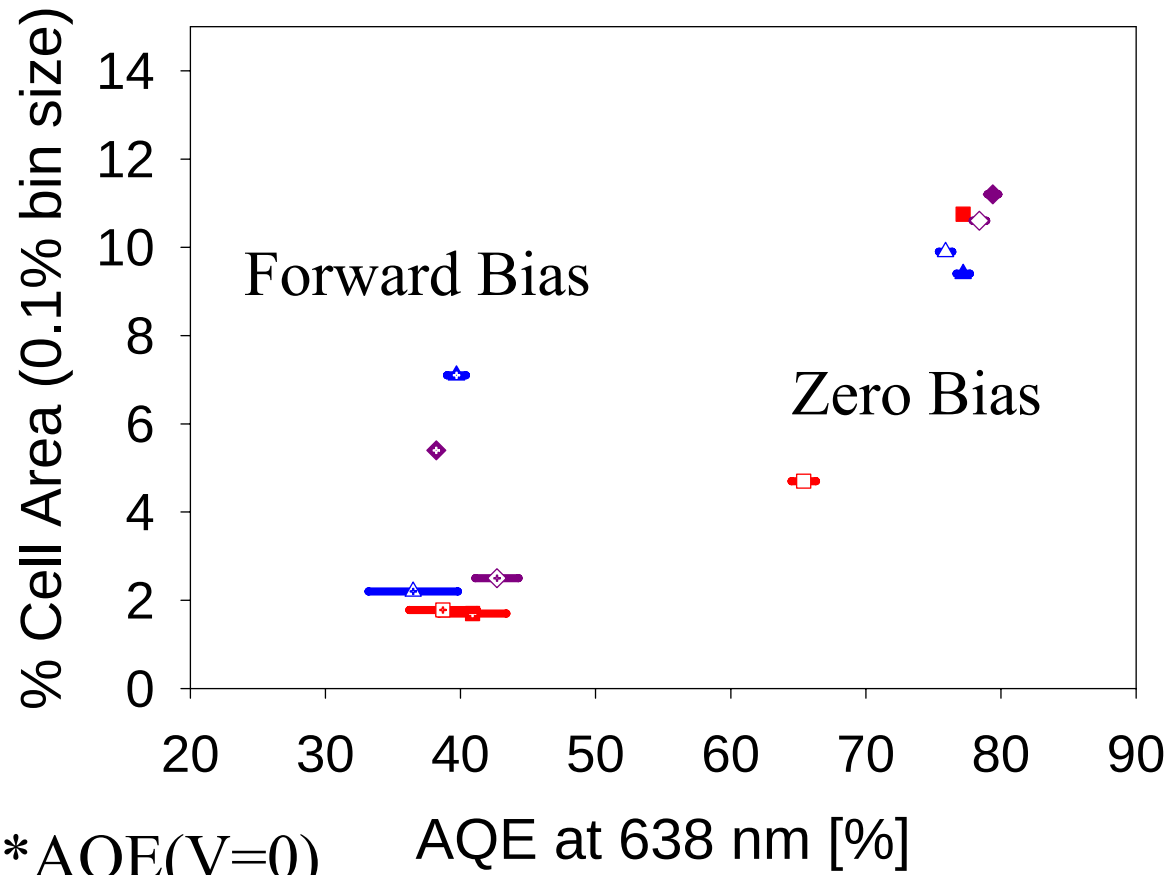


After Stress

All photomaps at zero bias

Uniformity Response to Stress

No Cu Poor $CdCl_2$	No Cu Good $CdCl_2$
Yes Cu Poor $CdCl_2$	Yes Cu Good $CdCl_2$



Bias Condition:

AQE(bias) ≈ 0.5*AQE(V=0)

Summary

Colorado State University

- Improvement of $CdCl_2$ modestly improves Jsc and Voc
- Cu alone more strongly improves Jsc, Voc, FF
- cm scale uniformity most improved by Cu
- Forward bias and post-stress micro-uniformity most improved by Cu
- Combination of Cu, optimized $CdCl_2$ achieves best performance and stability

Conclusions

Colorado State University

- Cu containing contact necessary for stable devices
  - Dominant behavior before and after stress is back barrier reduction (Conclusion may be specific to stress conditions)
- Should Cu be used? YES
  - Conclusion may be specific to CSU and similar processing (vac. Strength, etch, ambient, deposition method, temperature profile, etc.)
- Improved $CdCl_2$ process enhances beneficial effects of Cu
  - Minimizes lifetime reduction due to Cu diffusion

Stability Studies of CdTe Devices: Cu in Back Contact vs. Cu in CdS

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D. L. Morel and C. S. Ferekides

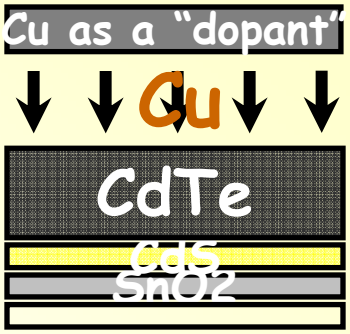
Clean Energy Research Center
Department of Electrical Engineering
University of South Florida, Tampa, FL 33620

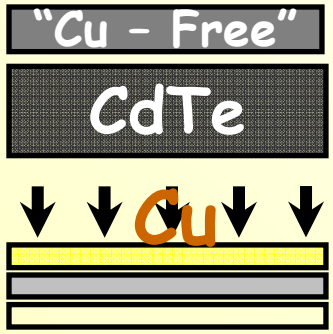
Work performed under NREL Sponsorship

OUTLINE

- ◊ **Main Objective - Study Cu effects on device stability**

- ◊ **Two types of devices depending on Cu incorporation method**
  - ◊ Cu in Back Contact - sputtered to several thicknesses
  - ◊ Cu in CdS w/o intentional Cu in back contact





Cu in Back Contact

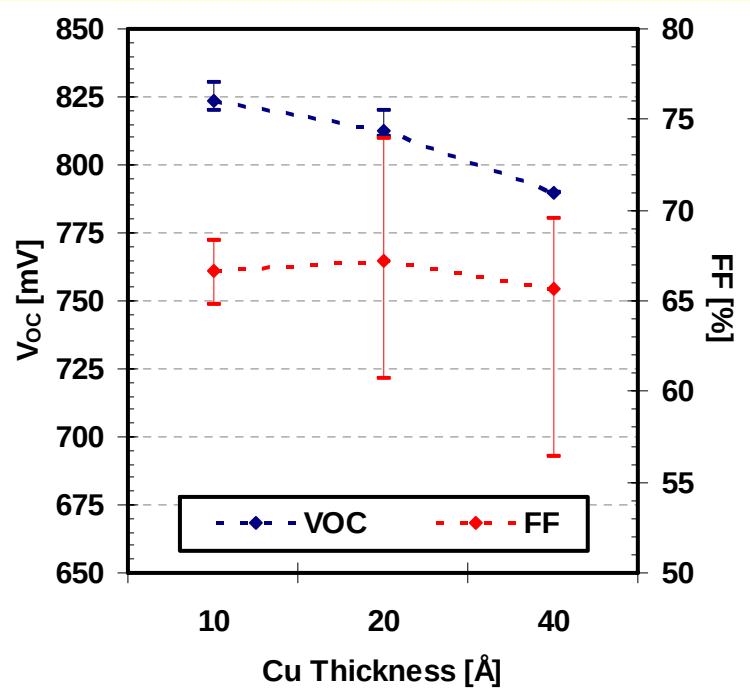
- Bi-layer TCO: SnO_2:F/SnO_2
- (CBD)CdS
- (CSS) CdTe
- $CdCl_2$ HT – Br_2 (0.1%) etch
- Cu deposition (10, 20, 40 Å)
- Back electrode: graphite (as-received); HT @ 240°C

Cu in CdS

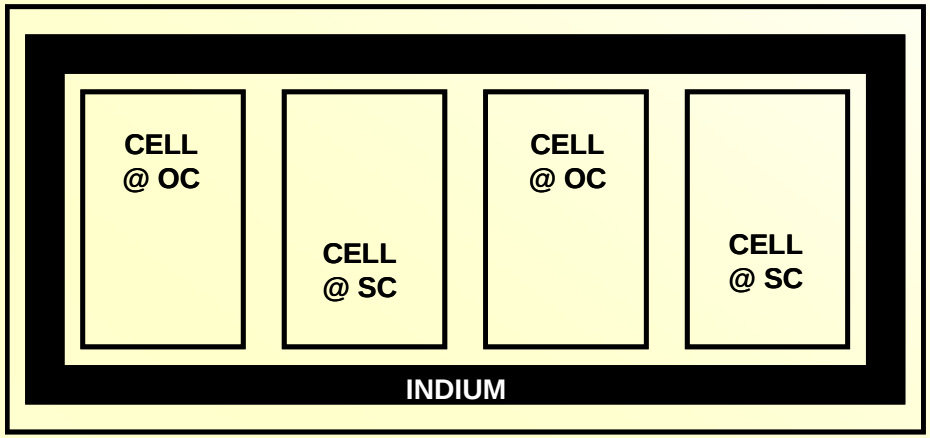
- Bi-layer TCO: SnO_2:F/SnO_2
- (CSS in O_2)CdS "CuCl – treated"
- (CSS) CdTe
- $CdCl_2$ HT – Br_2 (0.1%) etch
- Back electrode: sputtered Mo

"Cu-Based" Back Contact

- *Initial Performance*



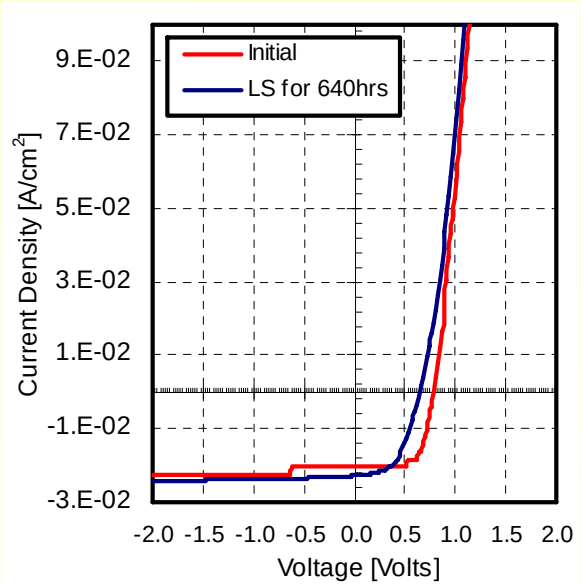
- *Substrate/cell arrangement*



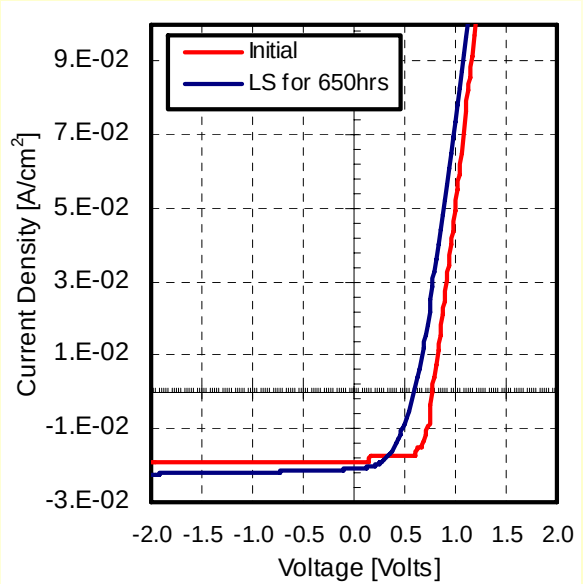
- V_{OC} decreases with amount of Cu
- Scattering in FF for 20 and 40 Å Cu thickness
- Two "identical" cells at each stress condition (OC & SC)

Light J-V @ OC

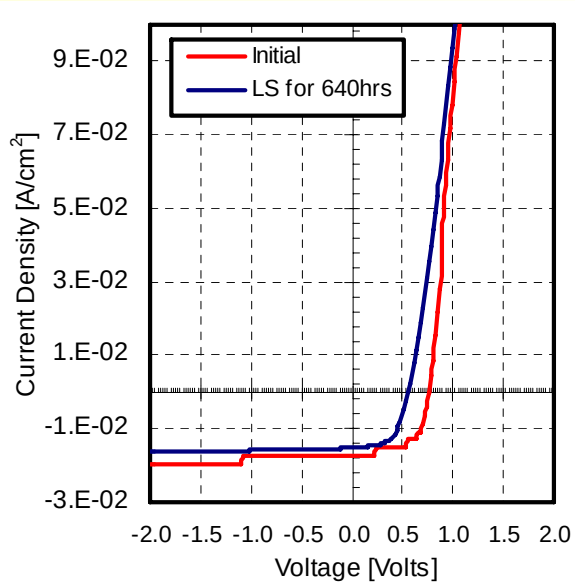
10 Å



20 Å



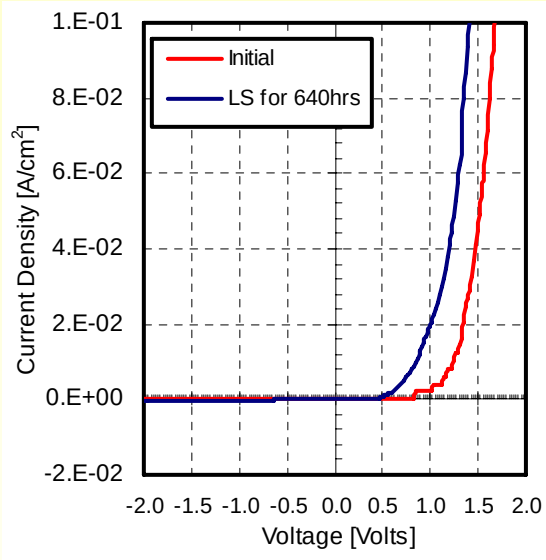
40 Å



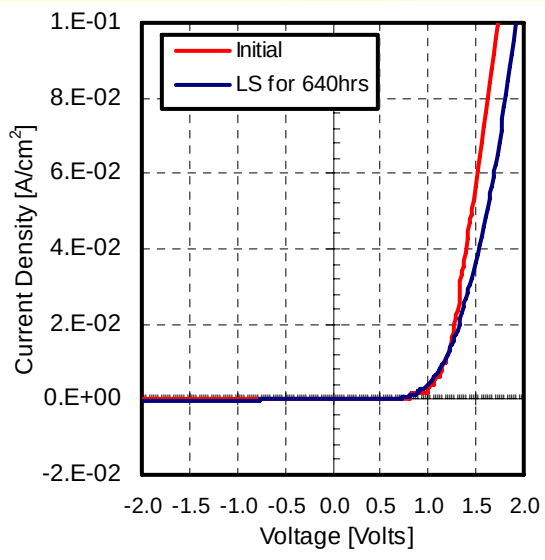
- Qualitatively L-J-V appear to show the same trend
- No shunting
- Potentially a small increase in the forward J-V slope (R_S)
- Drop in V_{OC}; increases with Cu thickness (see slide7)
- Increase in collection losses more likely (vs. increased J_O)

Dark J-V @ OC

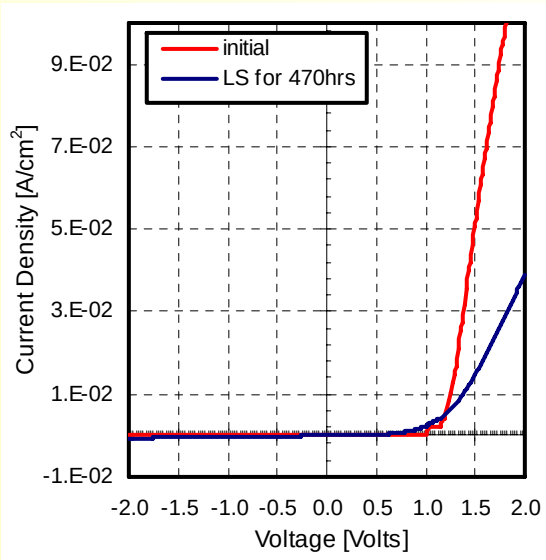
10 Å



20 Å



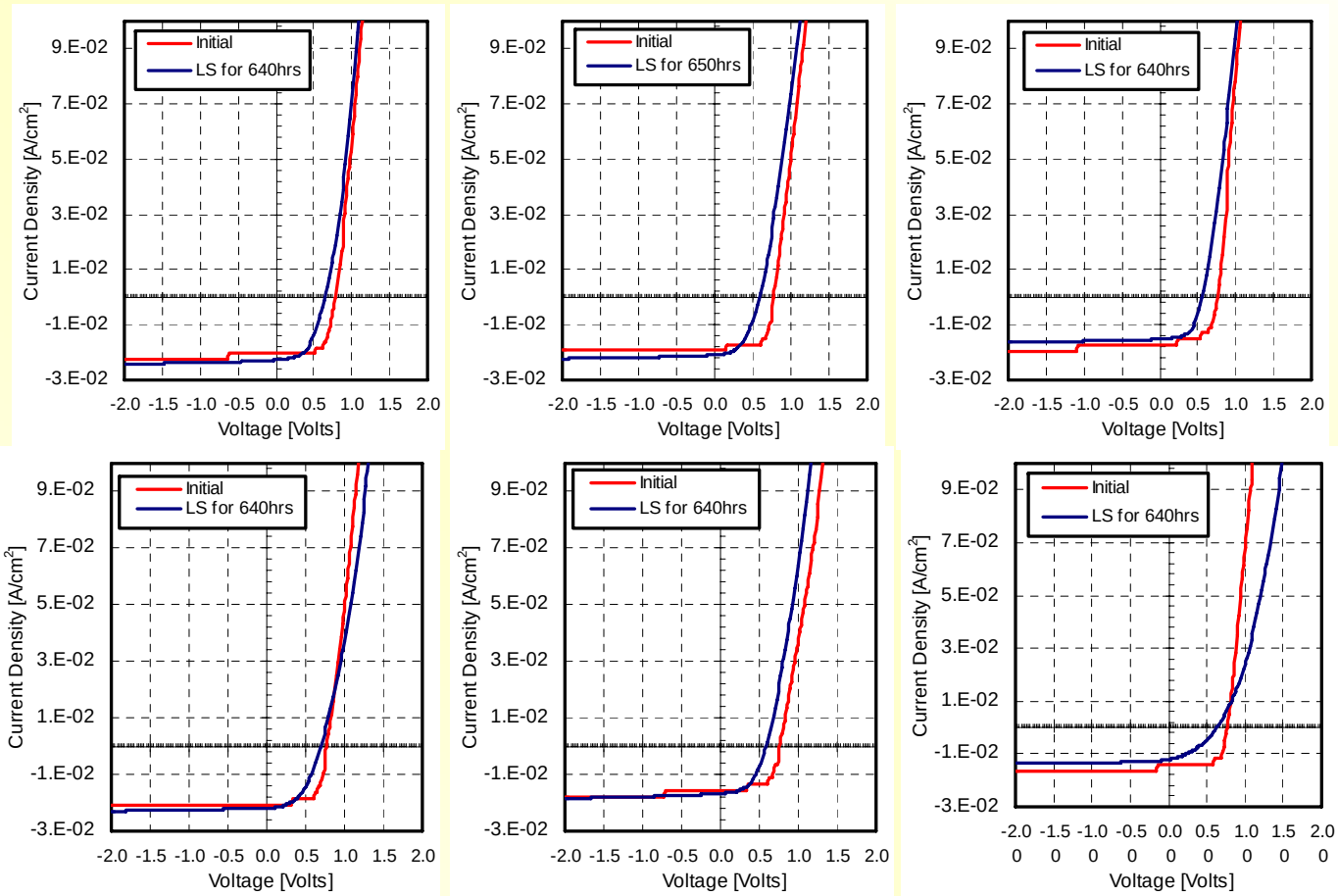
40 Å



- Dark R_S increases with Cu thickness
- Increase in R_S due to increased CdS resistivity (?) i.e. CdS:Cu
- In none of these cases do we observe the formation of a back barrier as a result of stressing

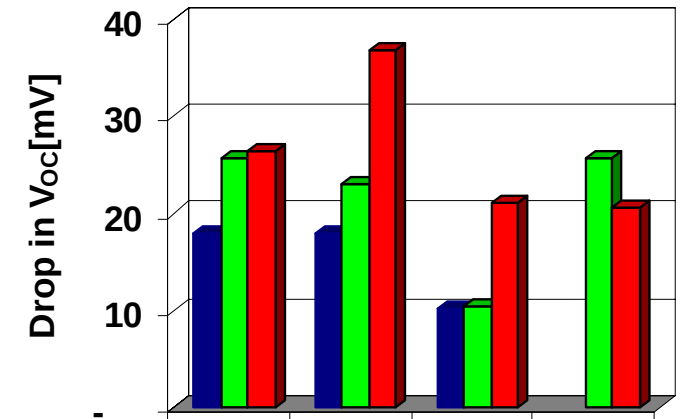
Light J-V OC vs. SC

10 Å **20 Å** **40 Å**

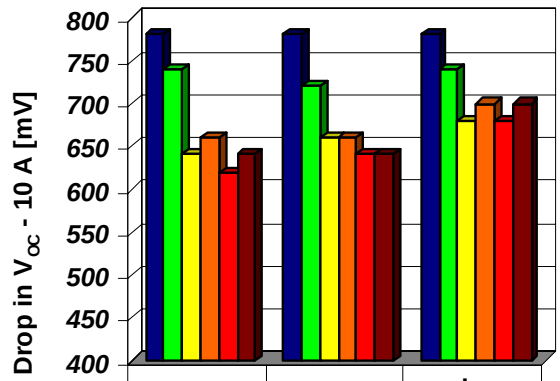


- Under SC conditions the increase in R_S also apparent in L-J-V
- Do SC conditions lead to more rapid accumulation of Cu in CdS (?)

SUMMARY (V_{OC})



	a	c	b	d
240-10	18	18	10	
240-20	26	23	11	26
240-40	26	37	21	21



	a	c	b
initial	779.953	779.953	779.964
0.08	739.971	719.986	739.965
150	640.031	660.061	680.049
350	660.066	660.06	700.048
450	620.021	640.047	680.067
640	640.033	640.035	700.041

- V_{OC} losses increase with Cu in all cases (REM: initial V_{OC} also decreased with Cu)
- Losses higher at @ OC vs SC
- "Bulk" of V_{OC} loss occurs within first 100 hours

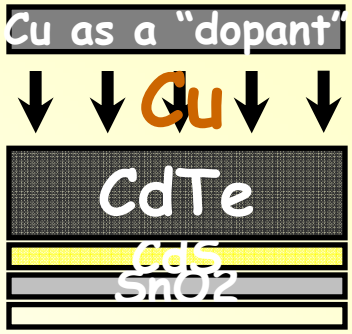
"Cu-Based" Back Contact Cells Summary

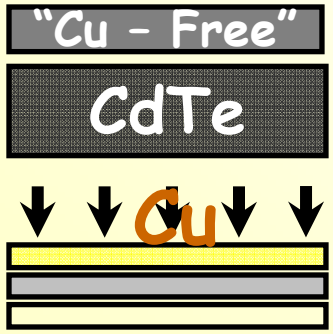
- LS leads to an increase in R_S; more pronounced at SC conditions and large Cu amounts
- V_{OC} losses increase with Cu in all cases
- OC conditions lead to higher losses (vs. SC) in V_{OC}
- "Bulk" of V_{OC} loss occurs within first 100 hours

- FF behavior more complex than V_{OC}:
  - @ the smallest Cu thickness little or no change (with initial increase @ OC)
  - @ the largest Cu thickness increased @ OC and decreased @ SC (R_S increase, collection losses)

OUTLINE

- ◊ Main Objective - Study Cu effects on device stability
- ◊ Two types of devices depending on Cu incorporation method
  - ◊ Cu in Back Contact - sputtered to several thicknesses
  - ◊ Cu in CdS w/o intentional Cu in back contact





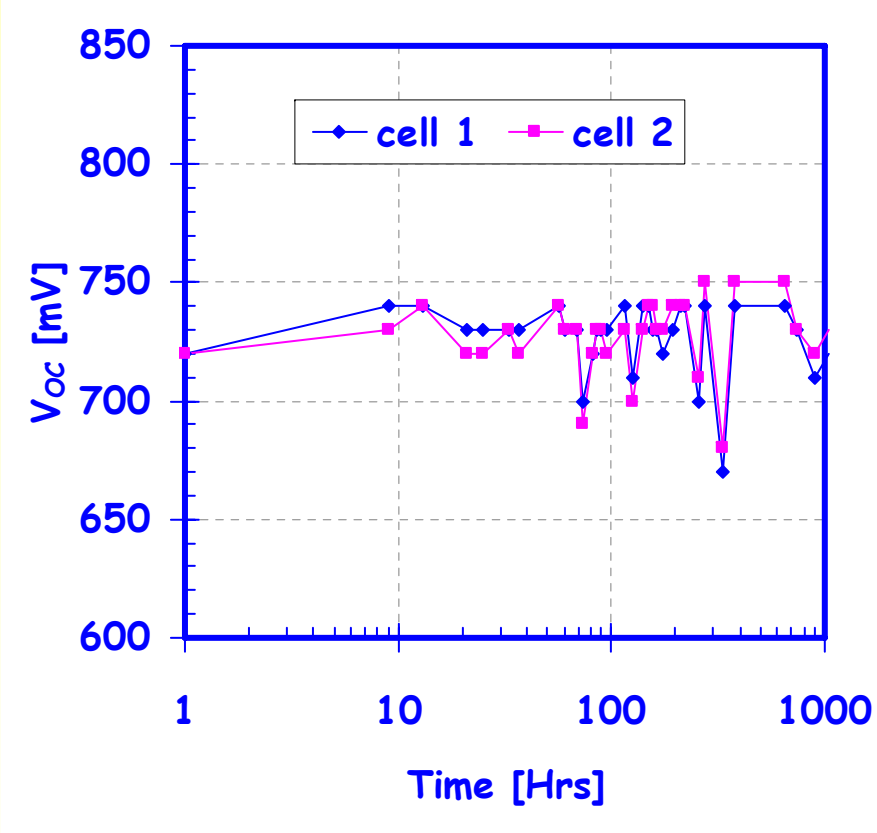
Cu in Back Contact

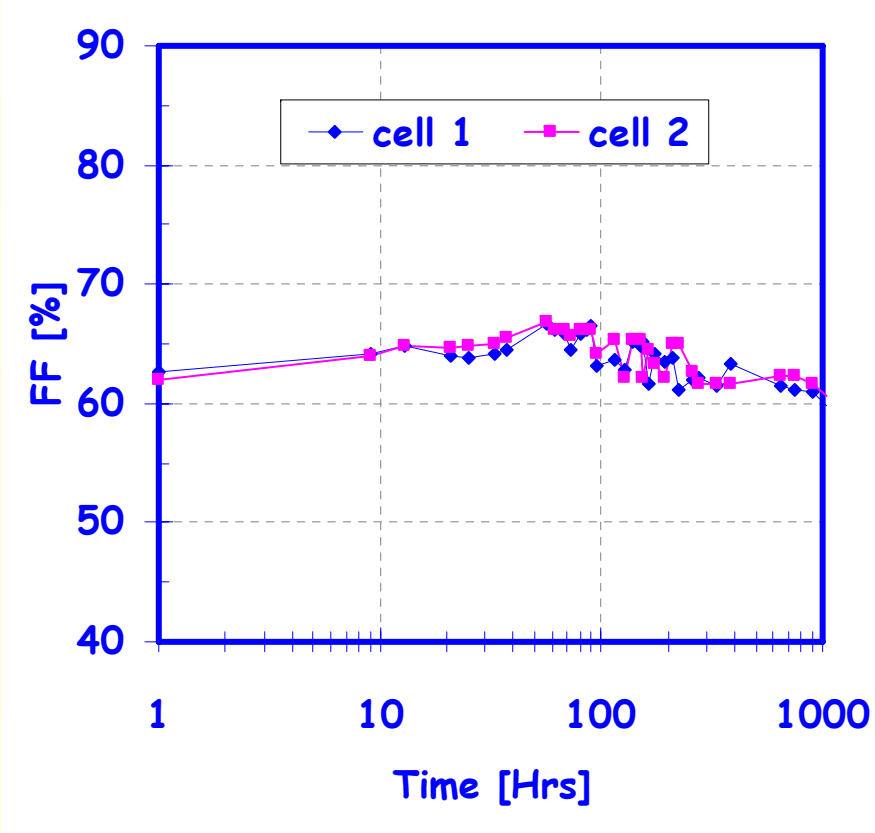
- Bi-layer TCO: SnO_2:F/SnO_2
- (CBD)CdS
- (CSS) CdTe
- $CdCl_2$ HT – Br_2 (0.1%) etch
- Cu deposition (10, 20, 40 Å)
- Back electrode: graphite (as-received); HT @ 240°C

Cu in CdS

- Bi-layer TCO: SnO_2:F/SnO_2
- (CSS in O_2)CdS "CuCl – treated"
- (CSS) CdTe
- $CdCl_2$ HT – Br_2 (0.1%) etch
- Back electrode: sputtered Mo

"Cu-doped" CdS Cells (no Cu in back contact)





***Data from last team meeting*

- These particular devices were contacted with "as-received" graphite paste and had CSS-CdS:Cu as a window
- Light soaked for 1000 hours at OC
- Measured @ operating T

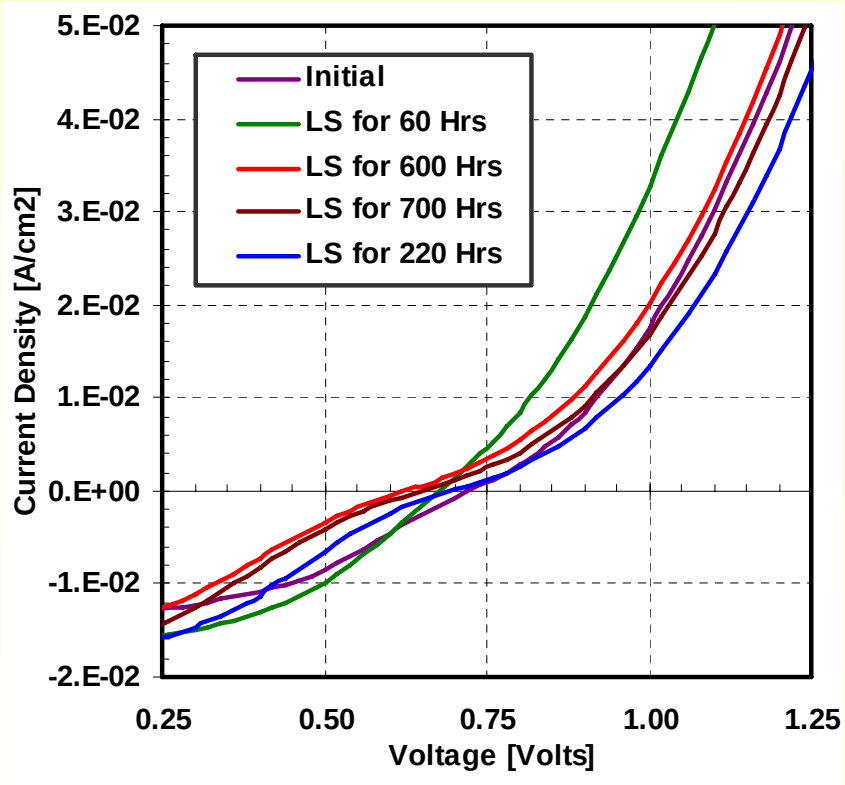
Performance Summary of CdS:Cu Cells

		V_{OC} [mV]		FF [%]	
Sample ID	cc/min	Initial	Final	Initial	Final
1-8-A17	10/10	807.5	755.0	55.0	34.0
3-23-A1	12/8	807.5	807.5	64.5	62.0
1-8-B11	10/10	812.5	785.0	62.9	38.2
4-2-B8	12/10	815.0	690.0	44.2	43.2
2-26-A7	10/10	816.7	793.3	63.6	50.0
2-26-A23	12/10	786.7	766.7	65.0	48.8

***ALL data are averages from 3-4 cells*

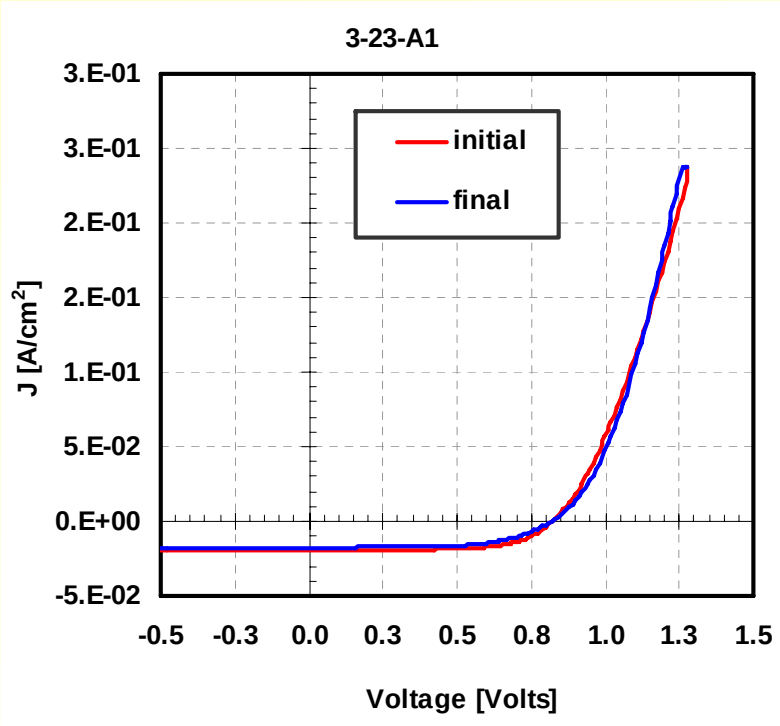
- *CuCl Solution in the 10^{-8} M range (optimum range for graphite contacted cells)*
- *Devices contacted with Mo (sputter-deposited)*
- *Initial V_{OC} was in most cases over 800 mV but the FF was "noisy" due to what appears to be poor back contact*
- *LS for approx. 700 hours lead to further degradation of most cells*

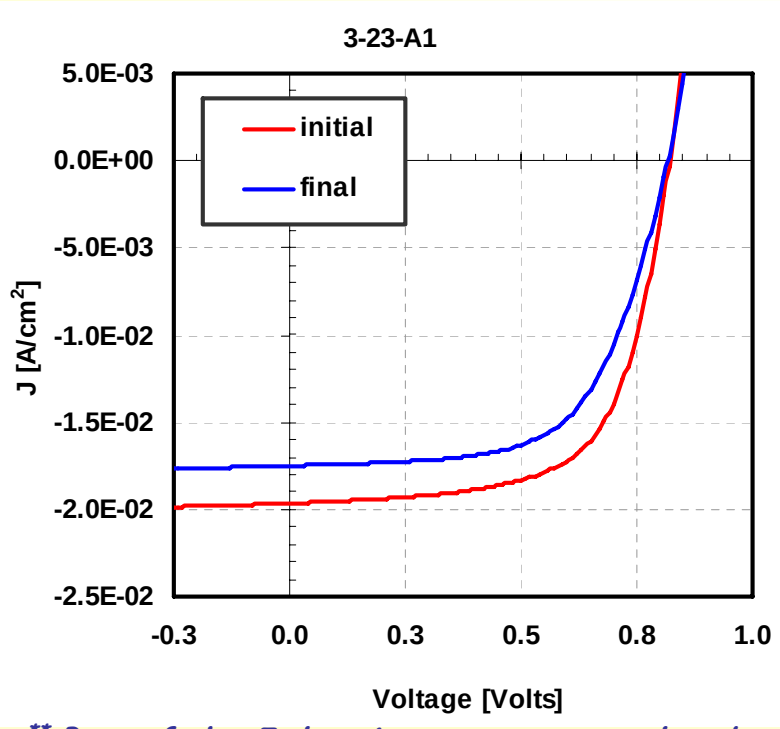
CdS:Cu Cells
Degradation Due to Back Contact



- *All devices exhibited the same trend*
- *There was an apparent improvement in the J-V characteristics (typical increase in performance observed during light soaking experiments)*
- *Eventually (after 100 hours) the J-V characteristics around V_{OC} degraded*
- *The extent of the degradation varied but the mexhanism appeared to be the same for all (i.e. back barrier)*

"Best" Overall Performance





*** Part of the J_L loss is measurement related; real loss is estimated @ 3-5% or less (QE)*

- *V_{OC} is very robust*
- *FF Losses are also due to a back barrier (but effect much smaller)*

Summary

- All Cu-based back contact-cells exhibited some degradation
- Increased amount of Cu and OC conditions lead to increased losses in V_{OC}
- Increase in R_S and collection losses could be related to Cu accumulation in CdS

- Results from CdS:Cu cells suggest that Cu incorporation in CdTe devices can be potentially manipulated/optimized for long term stability – V_{OC} and FF very robust; J_{SC} needs further evaluation
- Degradation was due to back contact barrier

- Further performance gains in devices with CdS:Cu can be realized if the "Cu-free" back contact is further improved
    - CdTe surface (?)
    - Mo deposition (?)

Effects of Encapsulation on CdTe Based Device Performance

Michael Kempe, David Albin, Tom McMahon, Wyatt Metzger, and Joel Pankow

National Renewable Energy Laboratory

Samuel Demtsu

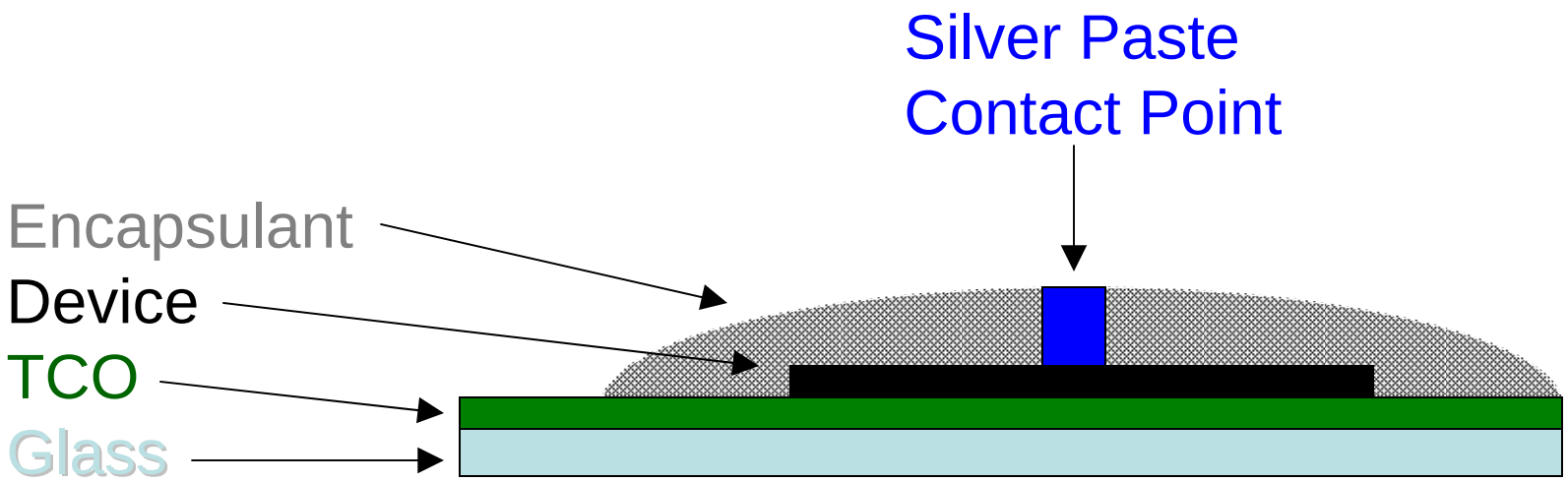
Colorado State University

CdTe Team Meeting 3/9/6

Motivation

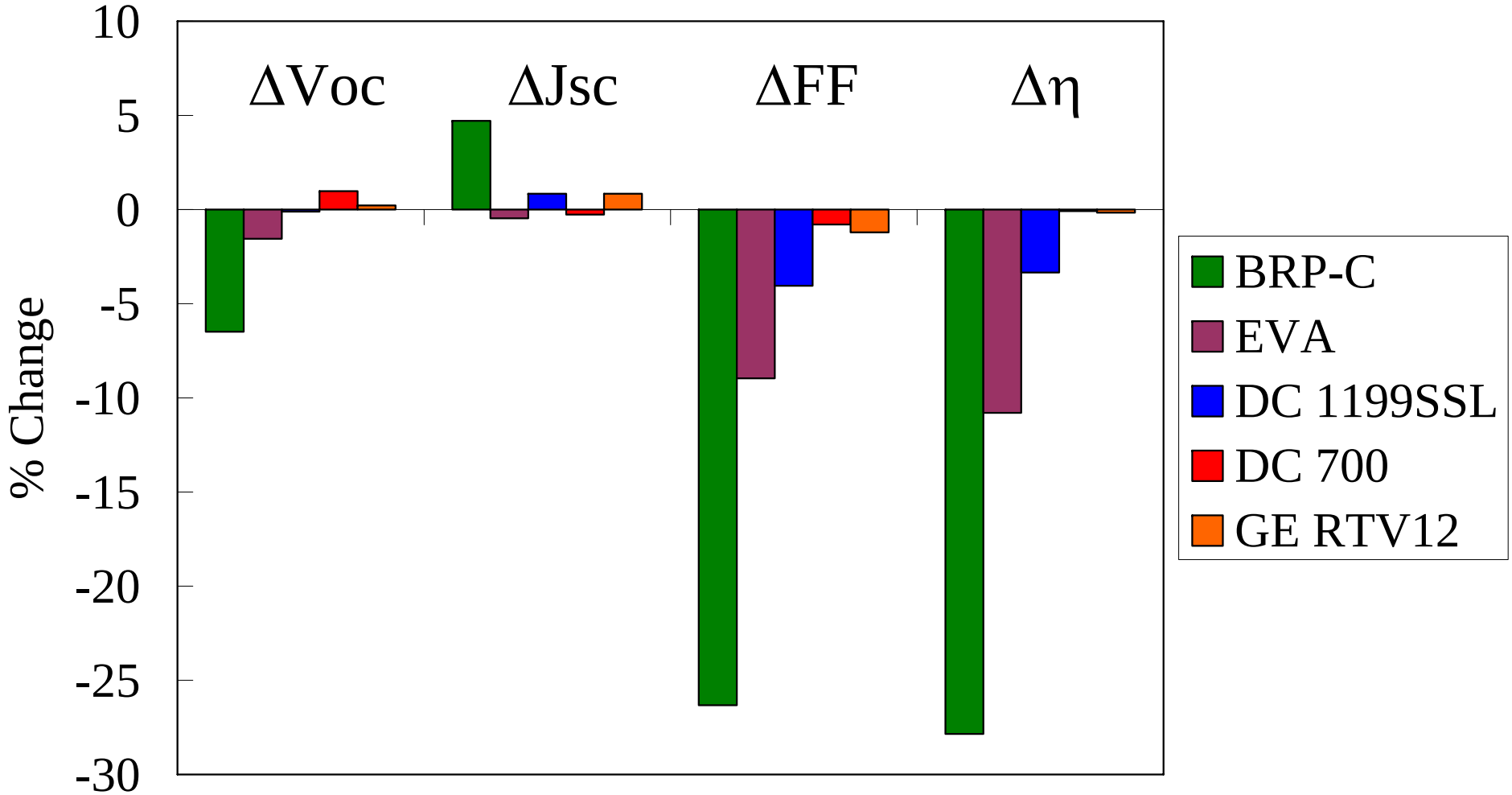
- It has been suggested that the lamination of CdTe devices permanently affects their performance and that moisture ingress is a significant factor affecting long term performance.
- This study has been undertaken to verify and help quantify the nature and scope of these performance issues.

Device Structure Enabled Lamination



- Cells were constructed using margins to eliminate shunting along the edges of cells.
- Cells were etched using nitric and phosphoric acid.
- Environmental stress was performed nominally at 60ºC.
  - 1 sun 1.4% RH testing in an Atlas Suntest CPS+
  - 1 sun 60% RH testing in an Atlas Ci65

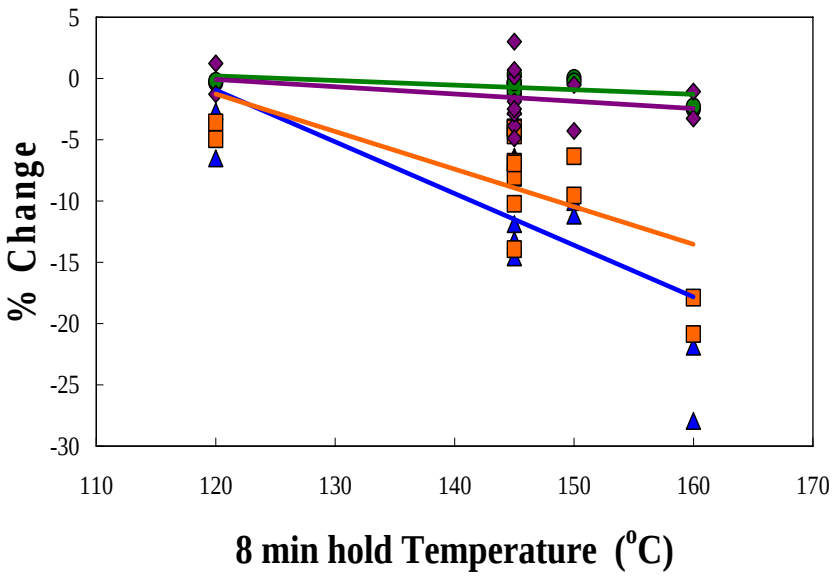
No Significant Initial Lamination Losses With RTV Silicones

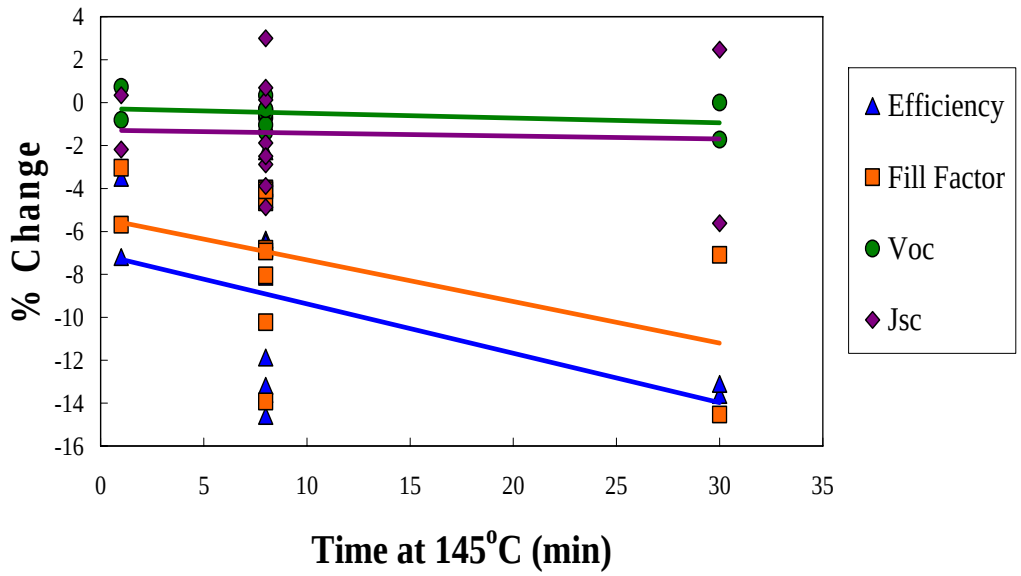


Note: In a data set not plotted, RTV12 showed improvement (~4%) after lamination.

Lamination Loss Increased by Heat

CdTe Laminated in EVA where the time and temperature of the cure cycle peak was varied.

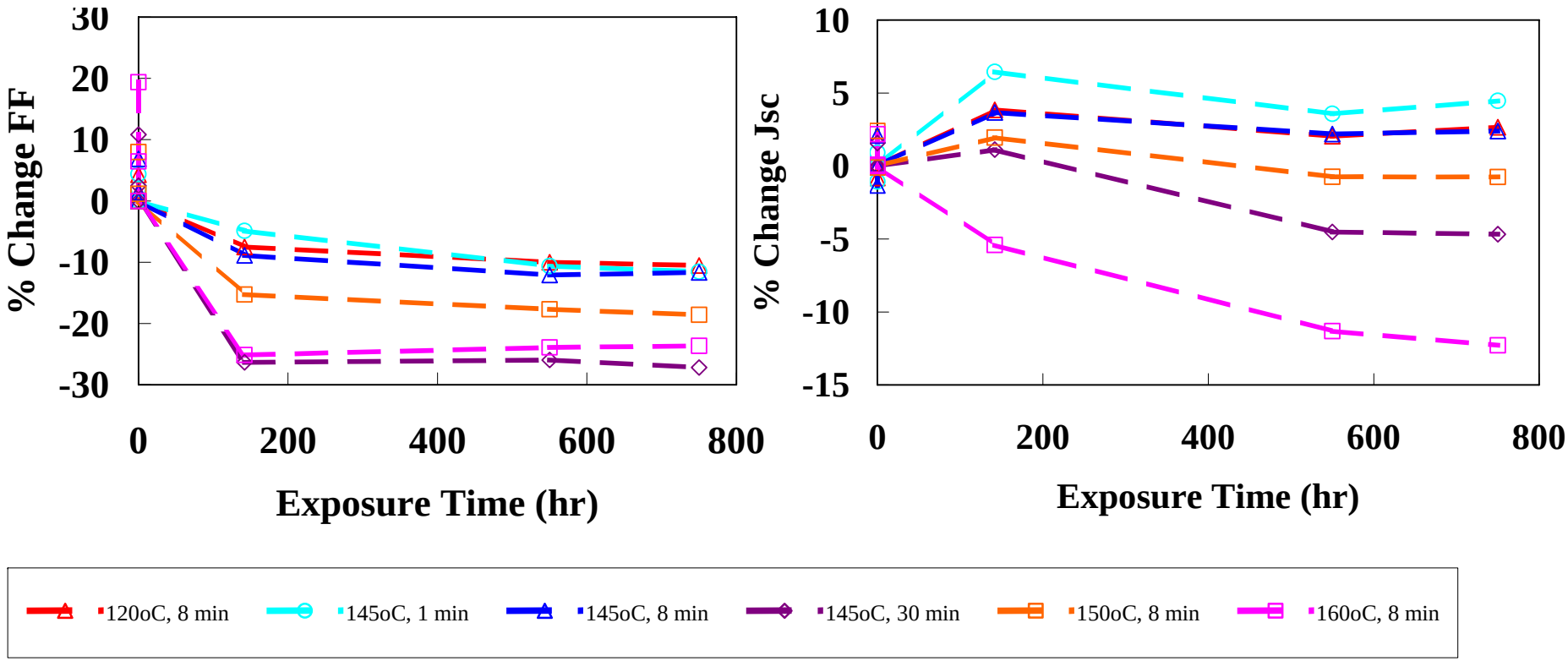




Higher lamination temperatures produce larger initial losses.

Longer Lamination Times produce larger initial losses.

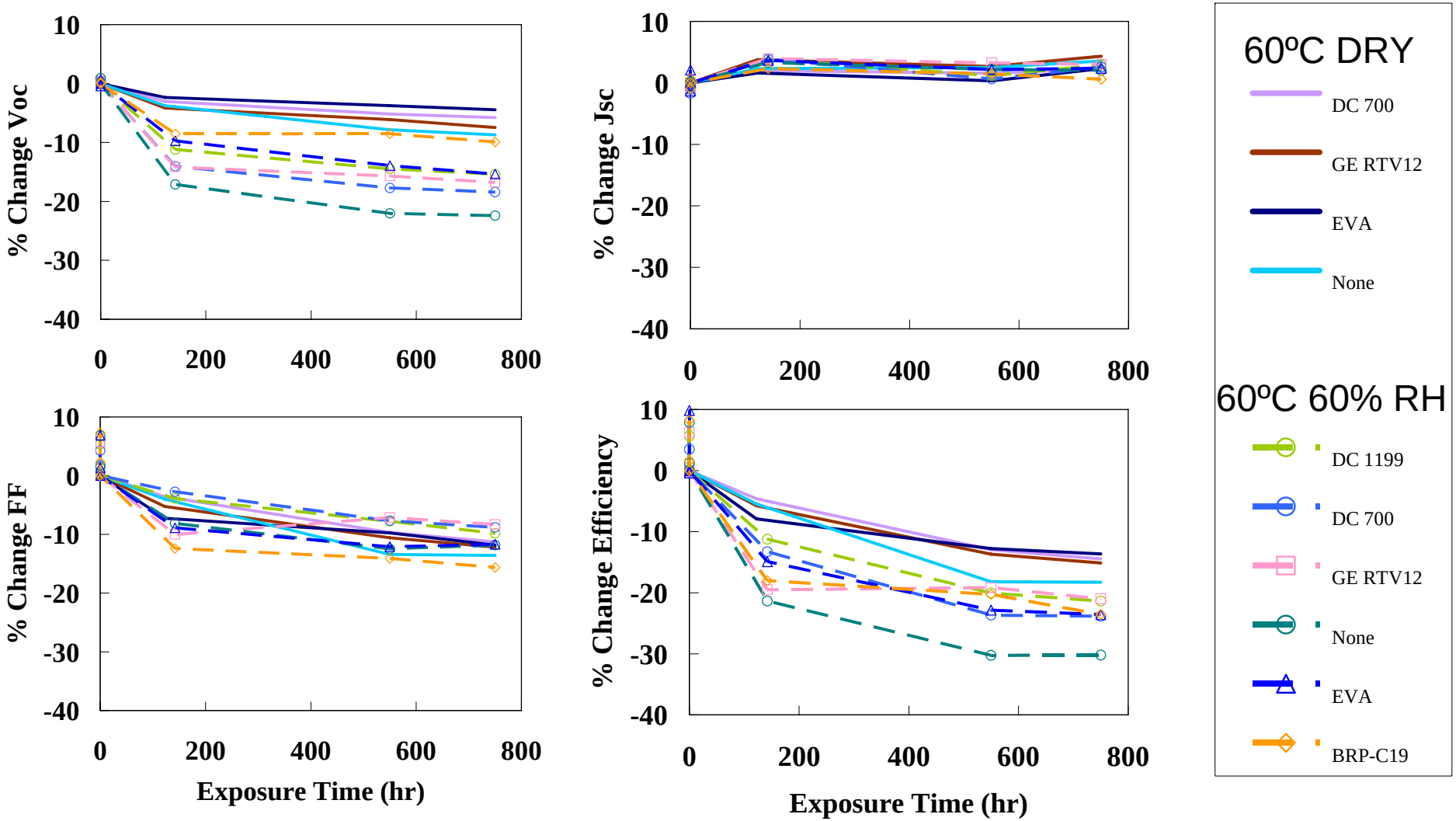
Lamination Heat Affects Stability Under Stress



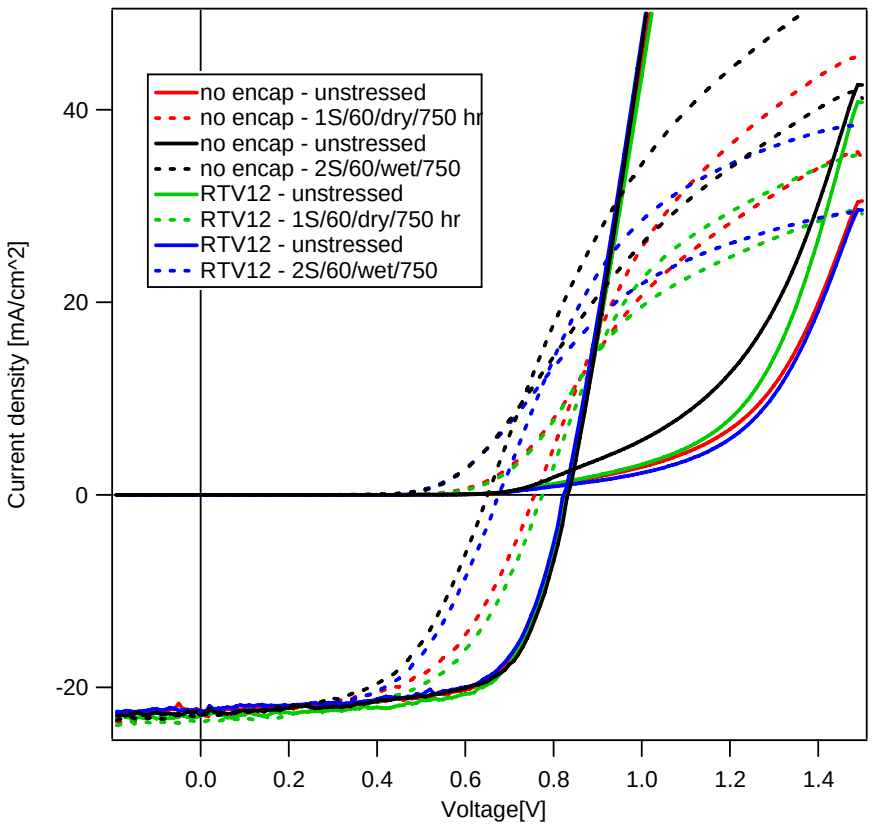
Increasing the time and/or temperature adversely affects the long term stability.

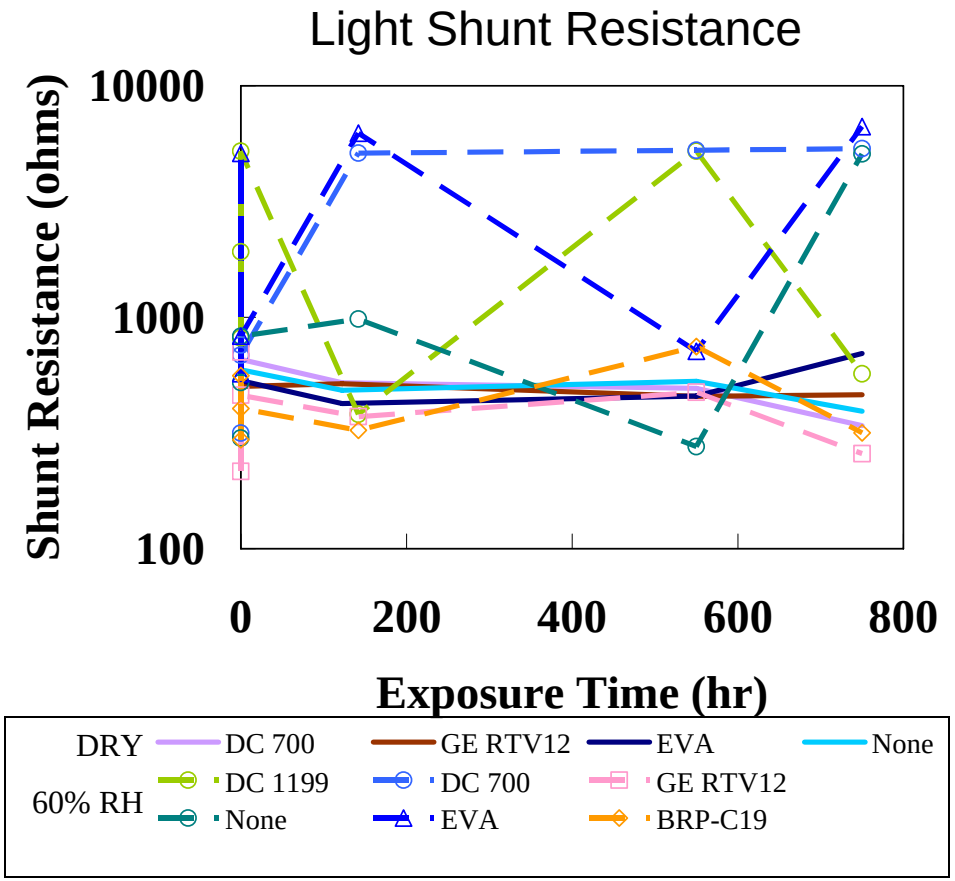
Cells were encapsulated with EVA with different temperatures and times at the maximum temperature.
Cells were exposed to 60C, 60% RH and 1 sun illumination.
The percent change is normalized to the performance after lamination.

Humidity Increases V_{oc} Losses



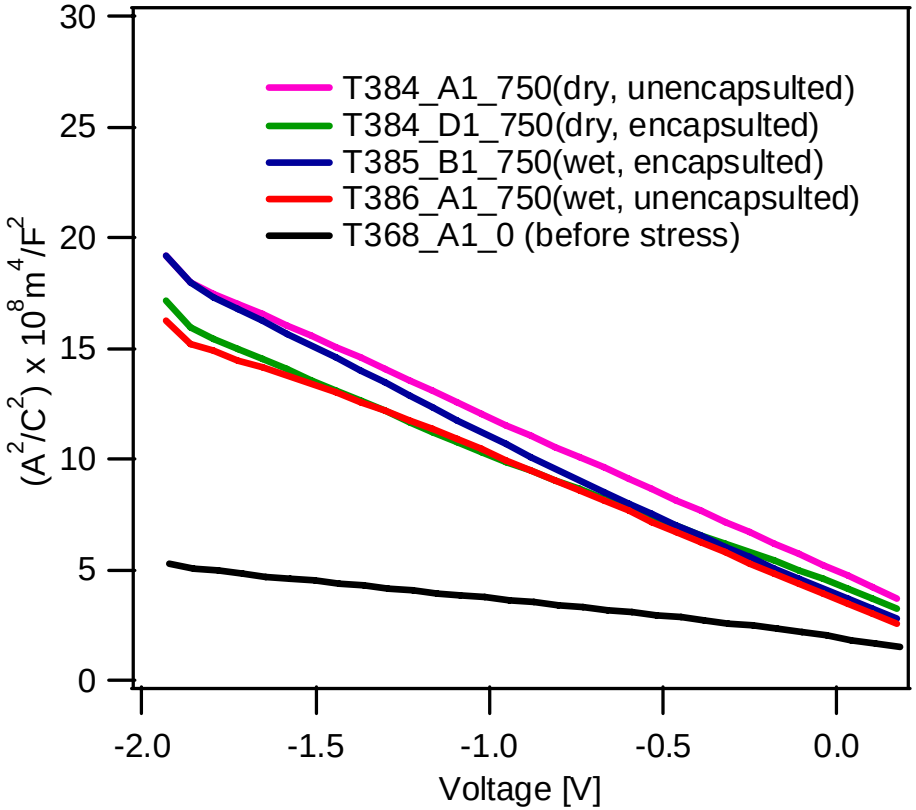
V_{oc} Loss Not Caused by Shunting

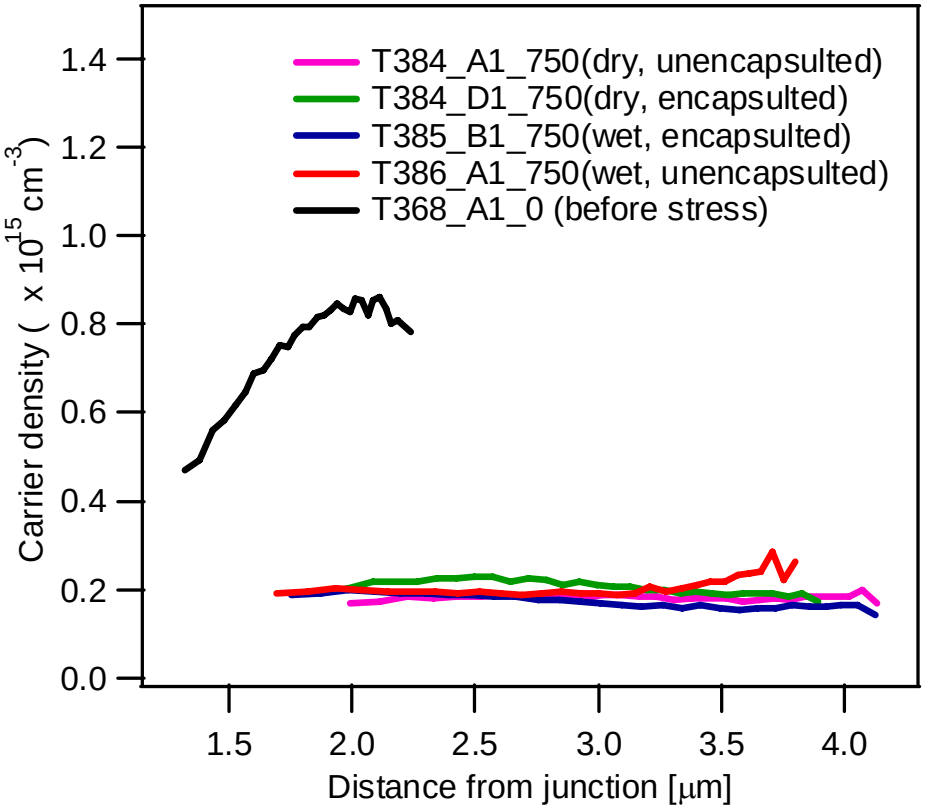




Dark Shunt Resistance > 10,000 Ω

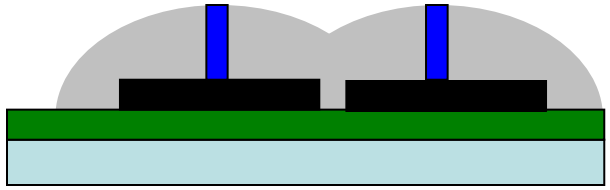
Wet vs Dry V_{oc} Drop Not Related to Carrier Density



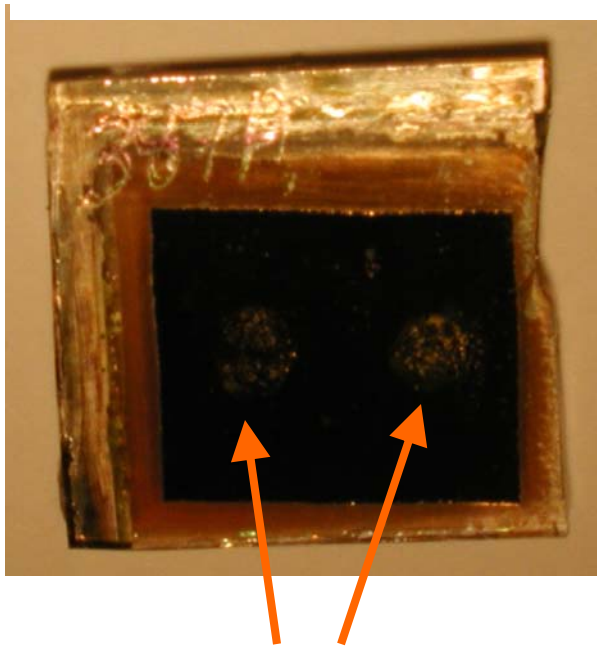


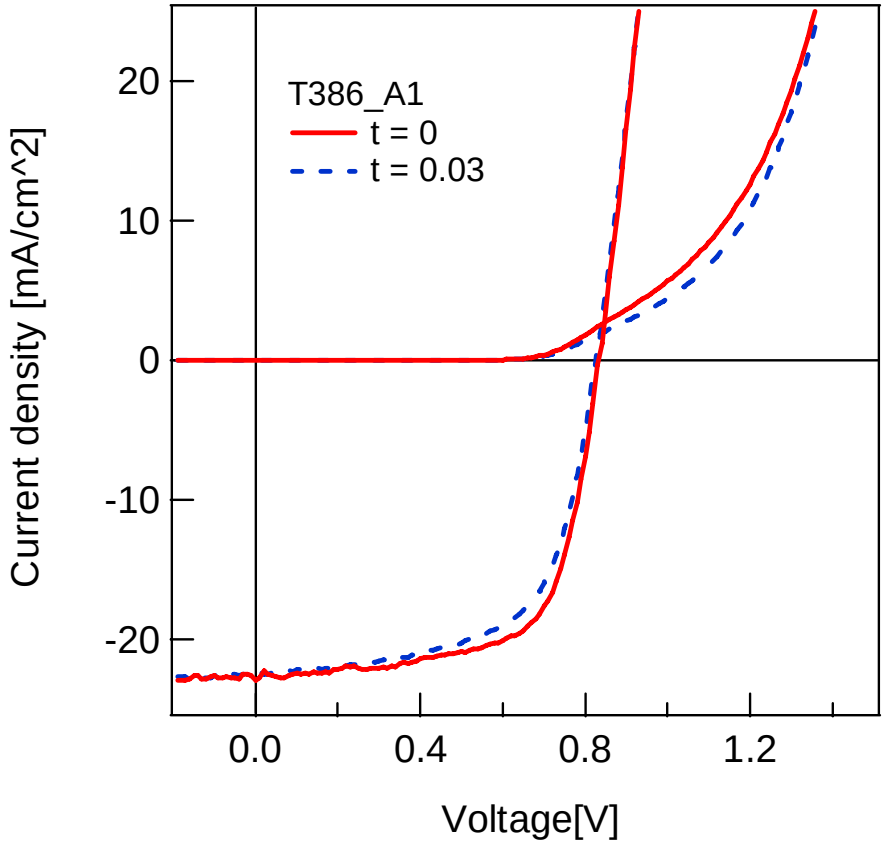
Samples stressed for 750 hours at 60C dry or at 60% RH.

Unlaminated Cells Demonstrated a Loss Associated With the Contact



Front Side





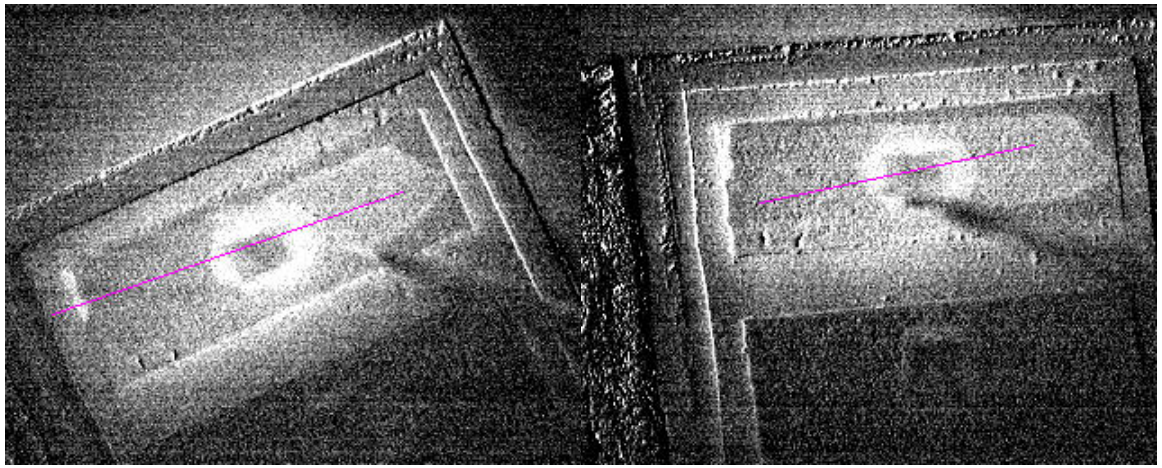
On a few cells, spots (one for each cell on the substrate) appeared under the contacting post after stress testing.

t=0 measured right after completing the cells.

t=0.03 measured after the other cells had been laminated.

Infrared Imaging and TRPL Suggest Weak Diode Under the Contact

Cells imaged under forward bias (4.8 mA and 0.845 V)
(no IR signal under reverse bias)



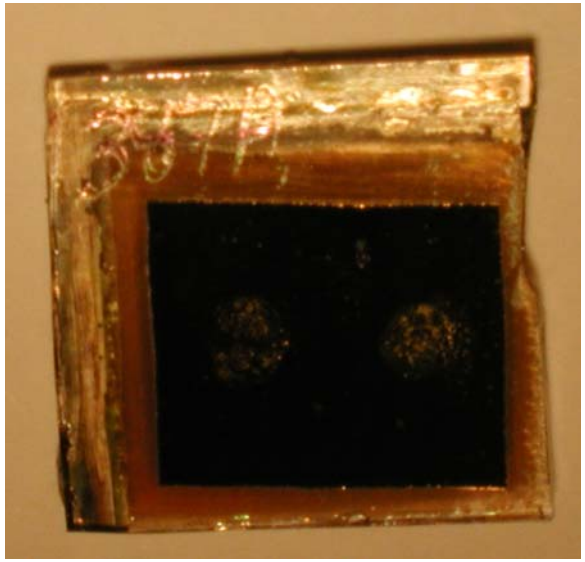
Unencapsulated cells after 750 hours at 60ºC and 60% RH under 1 sun illumination.

Bright areas are about 0.5ºC.

Time Resolved Photoluminescence (TRPL) measurements similarly did not show a significant difference between dry and wet stress when the whole cell was exposed.

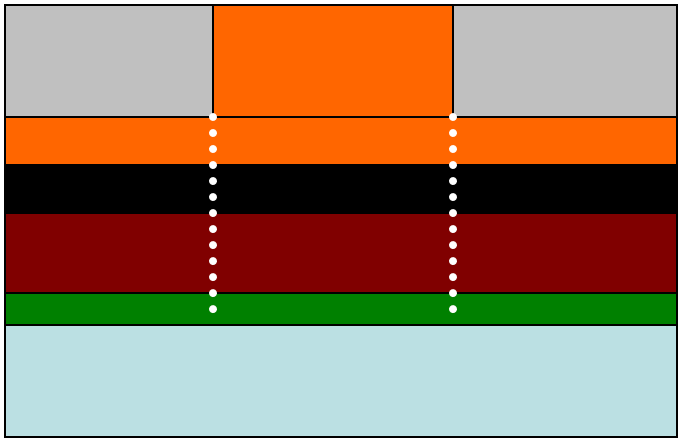
When the cells were masked to test only the area under the contact, the damp heat stressed samples had a shorter lifetime (800 ps vs 1000 ps).

All Cells Will See the Same Water Chemical Potential



CdTe Device Stack

Encapsulant
Silver Paste
Carbon Dag
CdTe/CdS
SnO2
Glass



The silver paste consists of silver particles in a PVC (~50%) polymer binder. This will allow moisture to permeate, will produce HCl, and convert some of the silver to AgCl making it more mobile.

The carbon dag consists of carbon particles, HgTe, and $Cu_{1.4}Te$ in a polyacrylic acid (~50%) polymer binder. This polymer is used in ionexchange columns and can be water soluble; therefore, it will swell with water increasing Ag permeation rates.

Conclusions

- Lamination heat creates an initial performance loss in addition to reduced long term performance manifested primarily as a fill factor loss.
- Exposure to damp heat produces a large V_{oc} loss.
- The Contact method used induced a greater susceptibility to the formation of a weak diode upon exposure to damp heat.
- V_{oc} loss is may be due to either the ingress of silver, or copper or from an oxidative reaction that increased the carrier recombination rate.

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Temperature dependent degradation in CdTe devices - What T is appropriate for ALT?

Dave Albin[1] and Samuel Demtsu[2]

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[2]Colorado State University, Fort Collins, CO

acknowledgements and thanks

T. McMahon, J. Sites, J. Pankow, W. Metzger, D. Young, M. Kempe, M. Dabney, R. Noufi

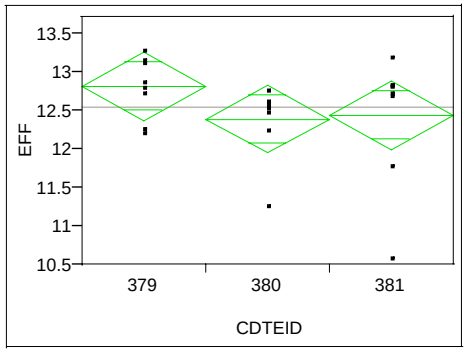
Background

- ALT temperatures should be chosen so that they accelerate the failure modes under consideration, but do not introduce failure modes that would *never* occur under use conditions.
- Historically, CdTe device stress-testing has involved temperatures ranging from about 60 °C to 200 °C.
- Systematic studies looking at degradation as a function of stress temperature are limited (USF, Tetali and Ferekides)

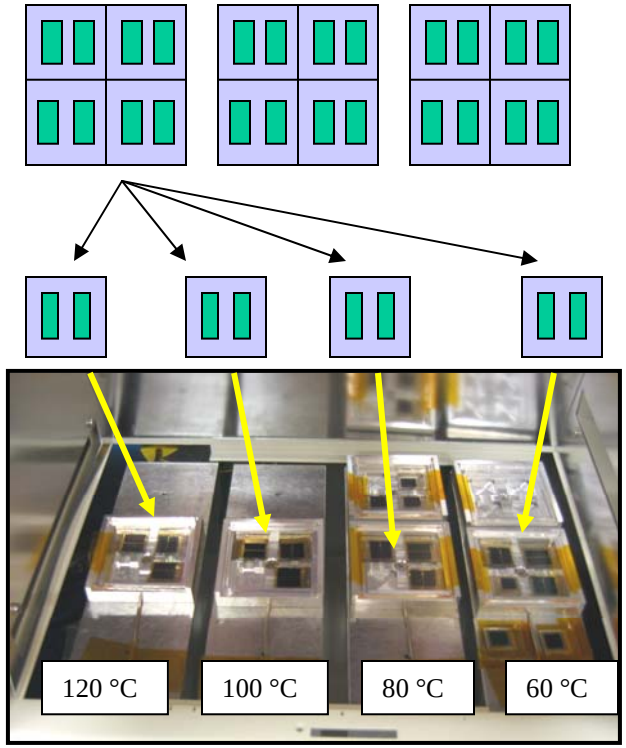
Experimental Design

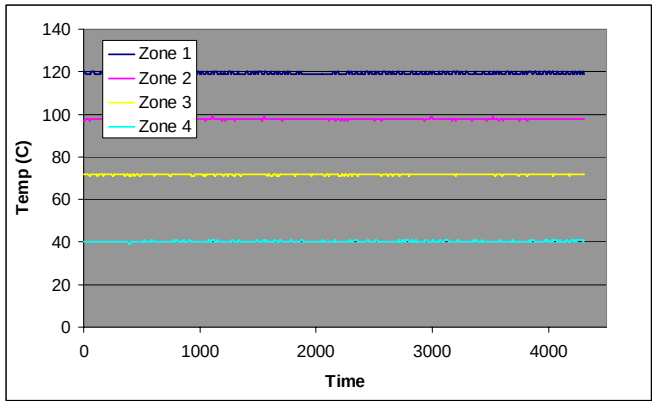
Device	Stress Method	Stress Temp, C	Voc	Jsc	FF	Eff
T379_A1	Combi_1	80	0.83	21.82	67.51	12.23
T379_A2	Combi_1	80	0.82	22.68	65.65	12.27
T379_B1	Combi_1	60	0.84	22.80	69.81	13.30
T379_B2	Combi_1	60	0.83	22.56	69.93	13.16
T379_C1	Combi_1	120	0.83	22.97	66.60	12.74
T379_C2	Combi_1	120	0.83	22.77	69.33	13.14
T379_D1	Combi_1	100	0.83	22.72	67.69	12.82
T379_D2	Combi_1	100	0.83	22.68	68.25	12.88
T380_A1	Combi_1	80	0.83	22.70	66.77	12.60
T380_A2	Combi_1	80	0.83	21.95	67.68	12.26
T380_B1	Combi_1	60	0.83	22.26	67.60	12.55
T380_B2	Combi_1	60	0.83	22.51	67.60	12.64
T380_C1	Combi_1	120	0.83	22.69	66.42	12.56
T380_C2	Combi_1	120	0.83	22.43	68.51	12.77
T380_D1	Combi_1	100	0.83	22.60	66.80	12.50
T380_D2	Combi_1	100	0.82	21.83	63.20	11.27
T381_A1	Combi_1	80	0.83	22.86	67.45	12.75
T381_A2	Combi_1	80	0.80	21.56	61.63	10.60
T381_B1	Combi_1	60	0.83	22.52	68.64	12.84
T381_B2	Combi_1	60	0.83	22.65	70.13	13.20
T381_C1	Combi_1	120	0.83	23.02	66.51	12.71
T381_C2	Combi_1	120	0.83	22.74	68.26	12.83
T381_D1	Combi_1	100	0.83	23.11	67.27	12.86
T381_D2	Combi_1	100	0.81	22.57	64.29	11.80

initial device performance



3 different CdTe substrates





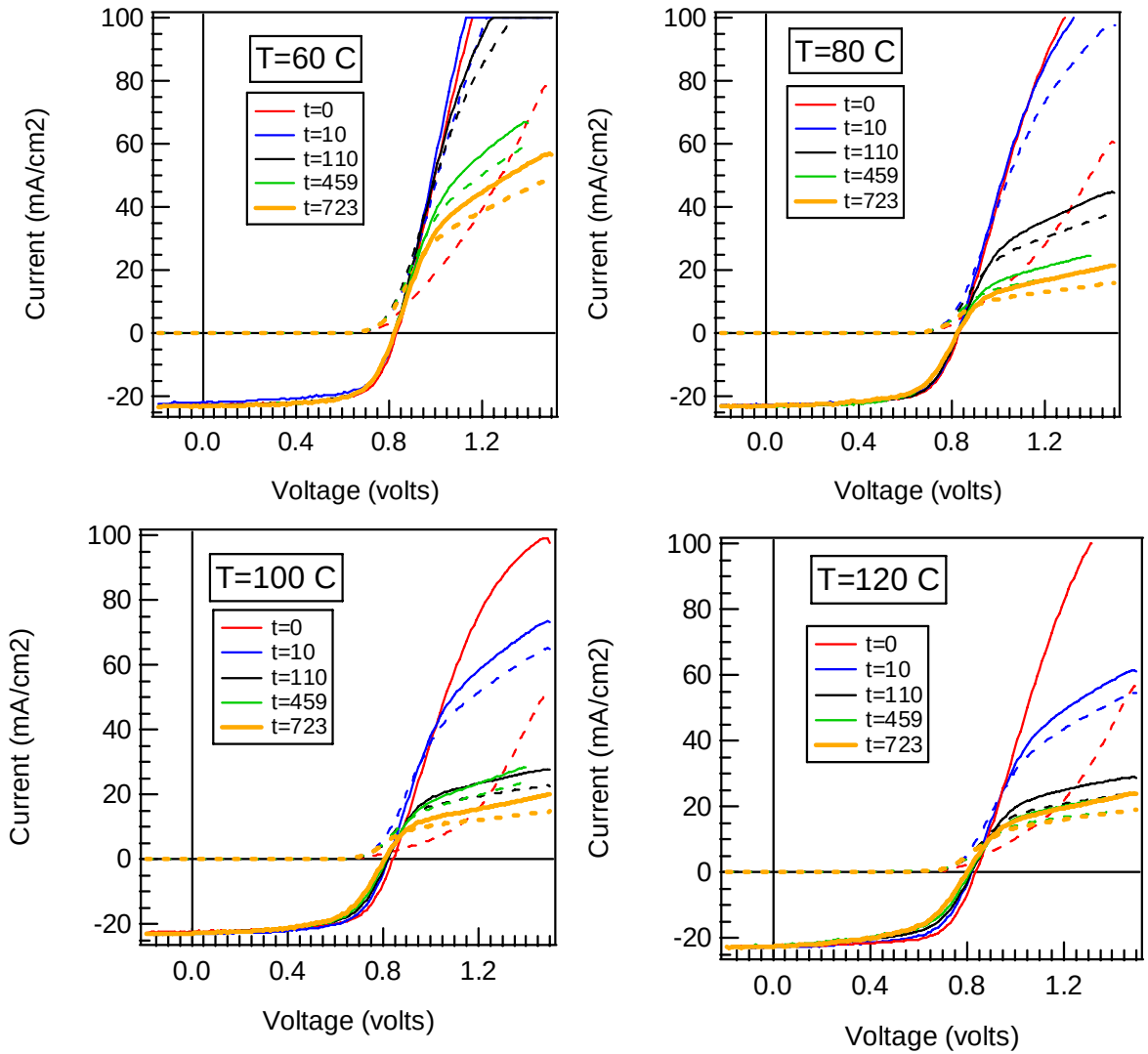
T_{dev}=120 C

T_{dev}=100 C

T_{dev}=80 C

T_{dev}=60 C

JV Changes with Stress



- Increase in Rollover (increased backcontact barrier/decreased conductance) apparent at all temperatures
- Decreasing FF (increased series resistance; voltage dependent collection) primarily at 80, 100, and 120 °C
- Decreasing V_{oc} only at 100, 120 °C

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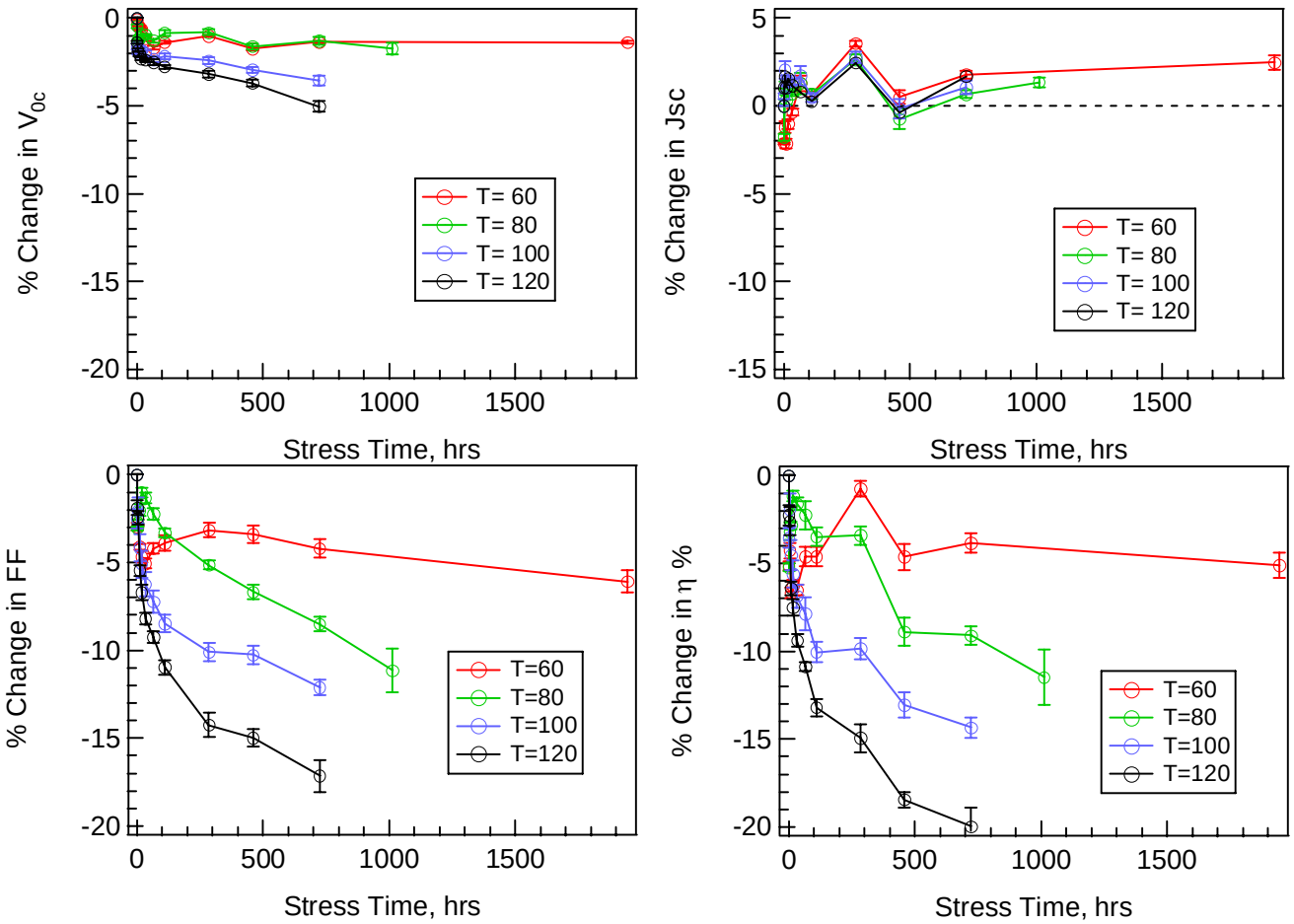
JV Changes with Stress

error bars show 95% C.I for mean



T = 60 °C

- η% drops slight
- due to slight decrease in FF

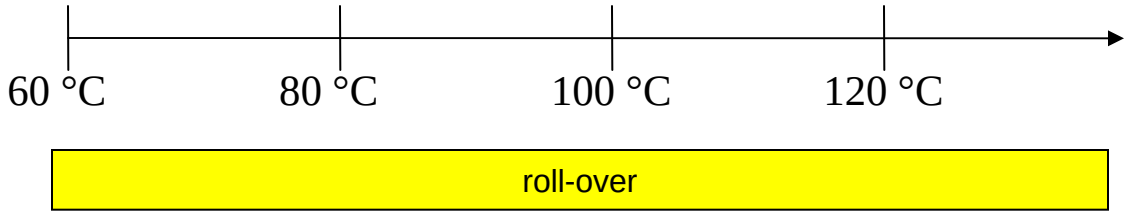
T = 80 °C

- η% drops more severe
- due to drop in FF (resistive loss; possibly voltage-dependent collection);
- **NO** V_{oc} drop

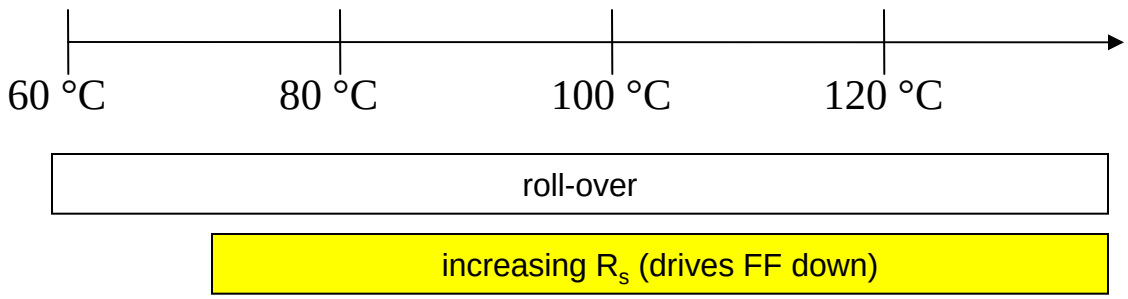
T = **100** and **120** °C

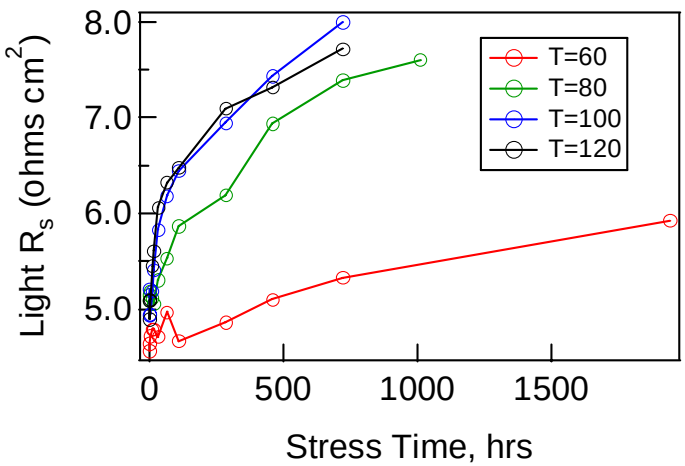
- η% drops severe
- due to drop in FF **AND** V_{oc} (resistive losses, voltage-dependent collection, **recombination**

Temperature-dependent Degradation Modes and Mechanisms



Temperature-dependent Degradation Modes and Mechanisms





Both modes representative of something occurring at the back contact

- increased barrier height
- reduced contact conductance
- Cu motion at the CdTe/contact interface

Temperature-dependent Degradation Modes and Mechanisms

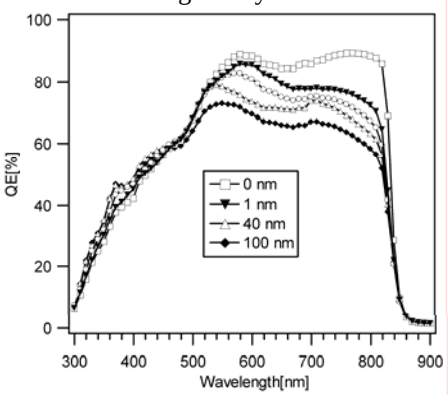
60 °C — 80 °C — 100 °C — 120 °C

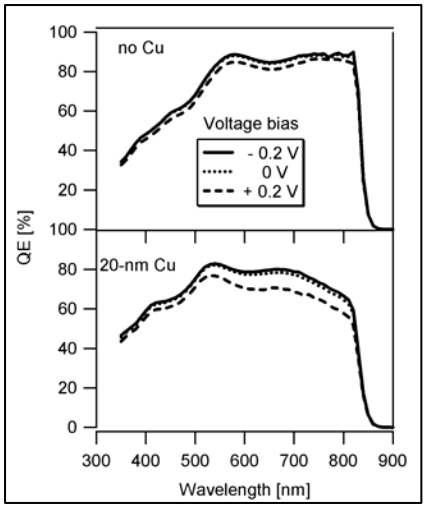
roll-over

increasing R_s (drives FF down)

Voltage-dependent collection (drives FF down further) see S. Demtsu et al., to be submitted to Appl. Phys. Lett.)

increasing Cu layer thickness





Cu introduces voltage-dependent QE

related to Cu motion from backcontact into CdTe

Temperature-dependent Degradation Modes and Mechanisms

60 °C — 80 °C — 100 °C — 120 °C

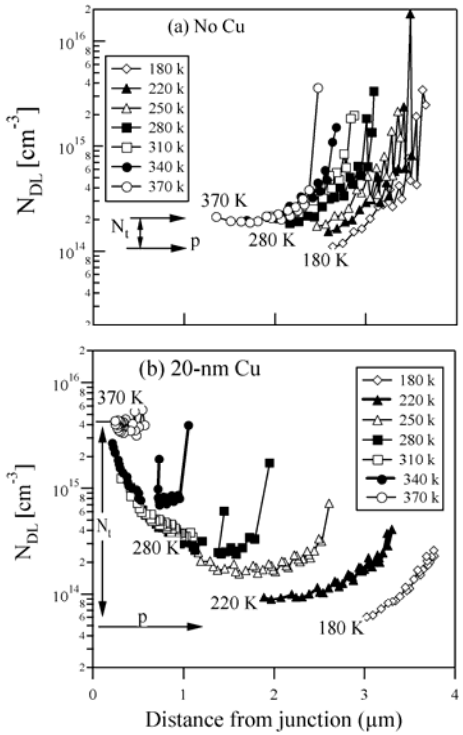
roll-over

increasing R_s (drives FF down)

Voltage-dependent collection (drives FF down further) see S. Demtsu et al., to be submitted to Appl. Phys. Lett.)

decreasing V_{oc} ; see S. Demtsu et al., WCPEC - Hawaii

increasing Cu penetration towards junction



increased recombination due to increased trap density at CdS/CdTe due to Cu

Quantitative identification of different degradation mechanisms

ref: www.weibull.com

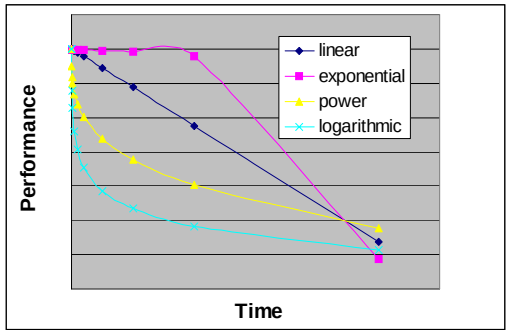
- Define a "level of failure" in order to calculate "life"
- Measure the degradation of samples under different stress temperatures over time
- Measure or model the "time to failure" for each stress temperature
- Common Degradation Models:

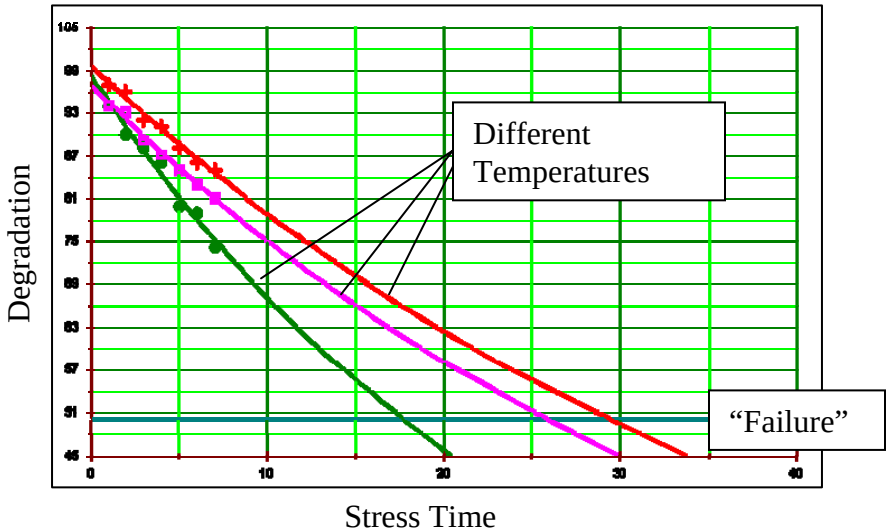
Linear: $y = a \cdot x + b$

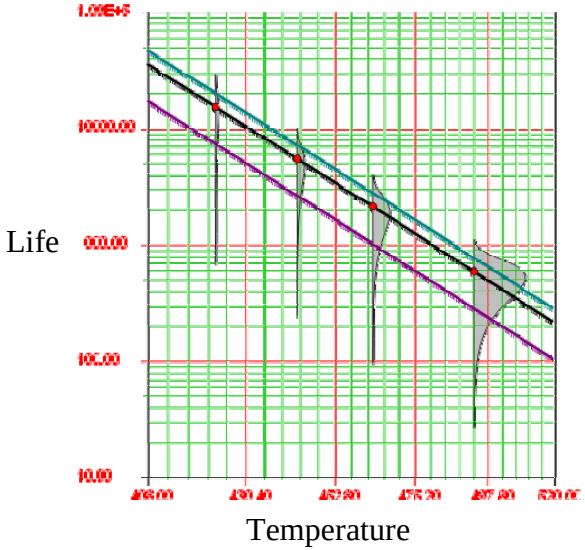
Exponential: $y = b \cdot e^{a \cdot x}$

Power: $y = b \cdot x^{a}$

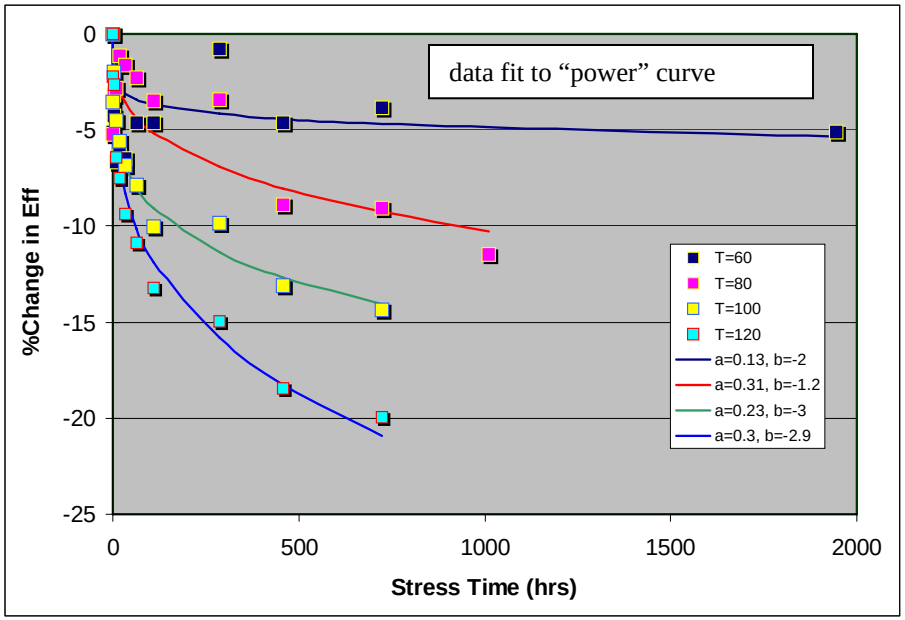
Logarithmic: $y = a \cdot \ln(x) + b$

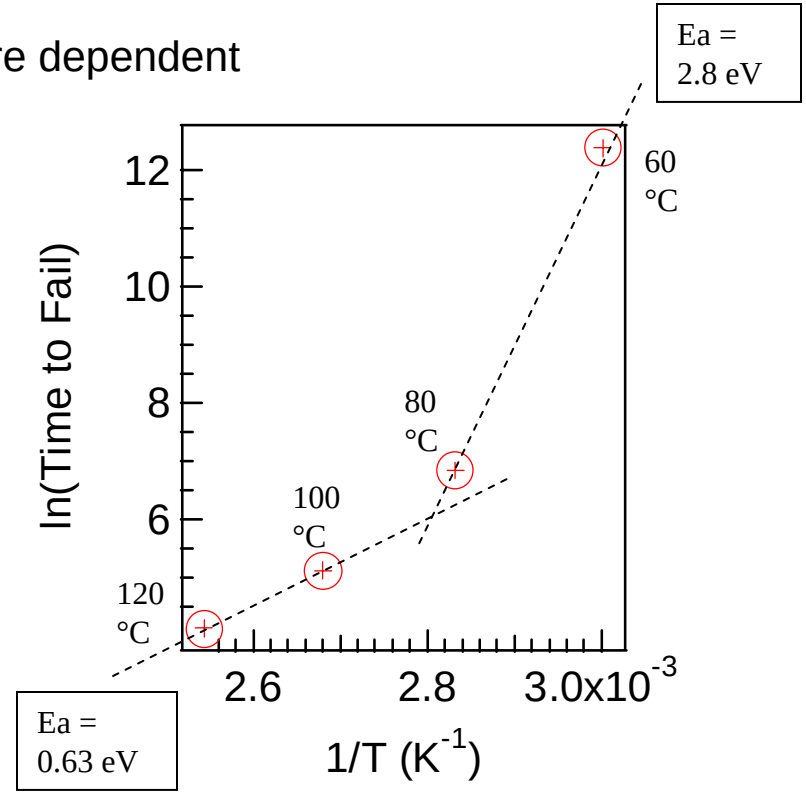






Dominant degradation mechanism is temperature dependent





arb. assign 10% as "time to fail"

Temp	Time to Failure
60	240000
80	940
100	168
120	62

slope = (E_A/k) = activation energy/Boltzman's constant

Summary

- We observed temperature-dependent degradation modes between 60 and 120 °C
- As temperature increased, degradation mechanisms can be explained by considering the motion of Cu.
  - at 60 °C, backcontact mechanisms dominate
  - at 80 °C voltage-dependent collection appears (bulk CdTe)
  - at 100, 120 °C junction recombination and loss in V_{oc} (CdS/CdTe junction)
- Time-to-failure analysis confirms the presence of temperature-dependent degradation (at low T, E_a = 2.8 eV; at higher T, E_a = 0.63 eV)
- Need to understand real “use” temperature in order to determine temperature used in temperature-activated ALTs

PRESENTATIONS FROM

MATERIALS CHEMISTRY SUBTEAM

Materials Chemistry Sub-Team

Brian McCandless and Tim Ohno

Institute of Energy Conversion

University of Delaware

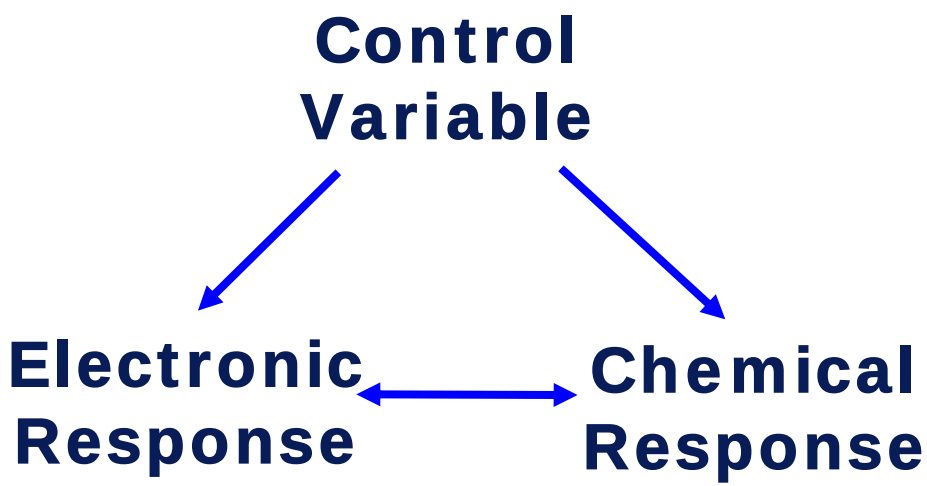
and

Colorado School of Mines

Sub-Team Purpose

Quantify and understand relationships between processing-chemistry-electronic properties for:

- **improved device performance**
- **reduced CdTe thickness**
- **reduced processing time**



Critical Questions

1. How does CdTe/CdS processing chemistry affect defect formation and distribution, how do these defects limit or enhance device operation and stability, what is the processing sensitivity, how do we measure and control them?

2. Can we separate fundamental device performance limits from processing-related limitations?

3. Do film structure and morphology exert a direct influence on device operation, or do they merely change the kinetics during film growth, treatment and contacting?

Presentations

Brian McCandless, IEC (15 min) Introduction/Presentation:
Decoupling control variables and quantifying chemistry in high throughput CdTe/CdS processing.

Fred Seymour, CSM (10 min)
Admittance spectroscopy analysis of CSS and VT devices with different CdCl2 processing.

Chris Ferekides, USF (10 min)
Photoluminescence analysis of CSS CdTe films and devices with different Cu, CdCl2, O2 processing.

Caroline Corwine, CSU (10 min)
Photoluminescence analysis of CdTe/CdS films from different labs: NREL, CSU. USF. IEC, FS.

Al Enzenroth, CSU (10 min)
Relating characterization and stress results to processing in the context of Cu diffusion. Including some discussion of Cu diffusion energy barriers.

Glenn Teeter, NREL (10 min)
Kinetics of CuxTe decomposition.

Clemens Heske, UNLV (15 min)
X-ray emission spectroscopic analysis of CdTe films and devices.

Rommel Noufi, NREL (10 min)
Micro-domains

Decoupling control variables and quantifying chemistry in high throughput CdTe/CdS solar cell processing

Brian McCandless

Institute of Energy Conversion

University of Delaware

Acknowledgement: contributions of Michael Angelo, Derek Birkmire, Wayne Buchanan, William Crandley, Darshini Desai, Kevin Dobson, Greg Hanket, Steve Hegedus, Sergey Rykov. Work supported by NREL under contract: ADJ-1-30630-12.

Goal

High device performance with short processing time, high materials utilization and minimal processing steps

Approach

Utilize chemical and kinetic relationships to control structural, compositional and electronic properties in CdTe/CdS solar cells with CdTe deposited by vapor transport (VT) onto commercially available substrates

Outline

1. Processing steps and control variables

2. Summary of qualitative effects

3. Quantitative relationships

4. Results
   a. Diffusion modeling
   b. Reduced deposition time
   c. Reduced $CdCl_2$ treatment time
   d. Process sensitivity
   e. Reduced etch

5. Summary

Processing Steps and Control Variables

1. CdTe Film Deposition: Vapor Transport (VT)
   - Source temperature
   - Deposition temperature and translation speed
   - Carrier/background gas composition, pressure

2. $CdCl_2$ Vapor Processing
   - Source temperature
   - Reaction temperature
   - Ambient composition

3. Surface Preparation
   - Etch composition
   - Temperature

Summary of Qualitative Effects: Physical

Step Variable	Effect at Max Value	Effect at Min Value
CdTe source temp	high GR, high rms	low GR, low rms
CdTe deposition temp	glass mp, low GR, CdS loss	high GR
Carrier gas flow rate	undersaturated vapor	saturated vapor, low GR
Deposition pressure	low effusion, low re-evap	high effusion, high re-evap
O_2 partial pressure	oxidation, low rms	high rms, pinholes
$CdCl_2$ source temp	enhanced reactivity, residues, diffusion	
Reaction temp	enhanced oxidation, diffusion	
O_2 partial pressure	enhanced oxidation, diffusion	
Etch composition		
OH^- type	removes oxides, no Te	
H^+ type	decomposes CdTe, forms Te, penetrative	
viscous NH_2 route	forms Te, topotaxial	
Etch temp	excessive reaction	

Summary of Qualitative Effects: Electrical

Step Variable	Effect at Max Value	Effect at Min Value
CdTe source temp	shunts, particulates	
CdTe deposition temp	low yield, pinholes	
Carrier gas flow rate		
Deposition pressure		
O_2 partial pressure	low FF	low Voc
$CdCl_2$ source temperature		low J_L
Reaction temperature	shunts, high J_L	low J_L
O_2 partial pressure	rollover	low Voc
Etch composition		
OH^- type	low FF	rollover
H^+ type	shunts	rollover
viscous NH_2 route		rollover
Temperature		

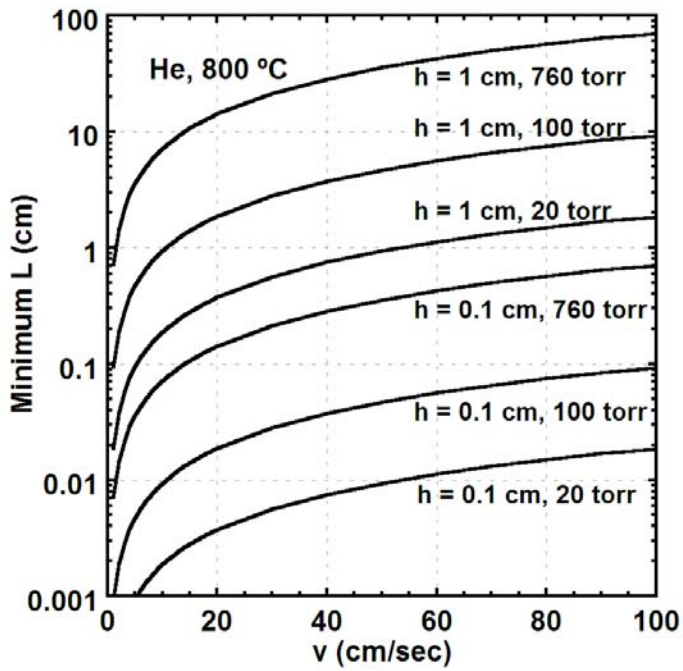
Quantitative Relationships: Film Growth

CdTe Sublimation

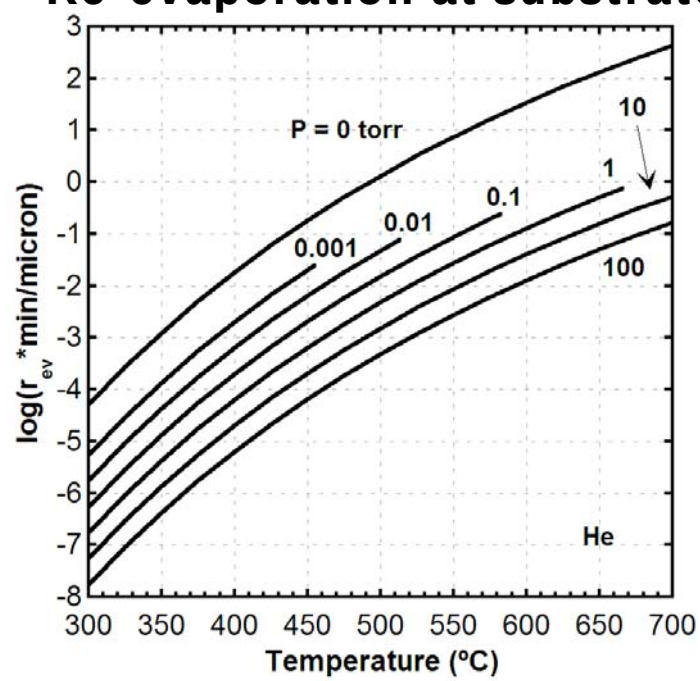
$$p_{sat}^{CdTe}(Torr) = e^{-\left(\frac{10650}{T(K)}\right)} - 2.56\ln(T) + 15.08$$

T (C)	p^{CdTe} (Torr)
500	0.006
800	1.89

Saturation



Re-evaporation at substrate



- *Source temperature and flow rate controls delivery*
- *Total pressure controls re-evaporation*

Quantitative Relationships: Oxidation

CdTe oxidation in dry air

$$CdTe(s) + 1.5O_2(g) \Leftrightarrow CdO(s) + TeO_2(s) \Leftrightarrow CdTeO_3$$

$$\Delta G_{rxn}(400°C) = -72.46 \text{ kcal/mol}$$

in situ GIXRD at 400ºC: $CdTeO_3$, linear oxide development for 0 < t < 100 min, *R* = 2 nm/min, Arhennius relation (350-500ºC): $R_{RH=0}(\mu m/min) = 330\, exp\left(-\frac{7638}{T(K)}\right)$

Binary oxide free energies:

CdO ΔG_f^o = -54.5 kcal/mol

TeO_2 ΔG_f^o = -15.3 kcal/mol

CdTe oxidation in humid air

$$2CdTe(s) + 3O_2(g) \Leftrightarrow 2CdO(s) + 2TeO_2(s) \Leftrightarrow CdO + CdTe_2O_5$$

$$\Delta G_{rxn}(400°C) = -72.46 \text{ kcal/mol}$$

in situ GIXRD at 400ºC: $CdTe_2O_5$, CdO, linear oxide development for 0 < t < 60 min, R = 15 nm/min, Arhennius relation (350-500ºC): $R_{RH=80\%}(\mu m/min) = 98.5\, exp\left(-\frac{5653}{T(K)}\right)$

- *Humid air enhances oxidation rate and oxidation products*
- *CdO free energy ~3.5x TeO_2 free energy*

Quantitative Relationships: Metal Halide Vapor Treatment

Metal Halide Sublimation*

$$p_{sat}^{CdCl2}(Torr) = e^{-\left(\frac{10650}{T(K)}\right)} - 2.56\ln(T) + 15.08$$

$$p_{sat}^{ZnCl2}(Torr) = e^{-\left(\frac{10650}{T(K)}\right)} - 2.56\ln(T) + 15.08$$

T (C)	p^{CdCl2} (mTorr)	p^{ZnCl2} (mTorr)
280	0.003	2.8
400	3.6	705

CdTe reaction with $CdCl_2$ and O_2 (dry ambient)

$CdTe(s) + CdCl_2(s/g) + O_2(g) \Leftrightarrow 2CdO(s) + TeCl_2(g)$

ΔG_{rxn} (400°C) = -49.33 kcal/mol

GIXRD: $CdTeO_3$ and CdO

XPS d.p.: oxide d ~ 7 nm/min.

CdTe reaction with $ZnCl_2$ and O_2 (dry ambient)

$CdTe(s) + ZnCl_2(s/g) + O_2(g) \Leftrightarrow 2ZnO(s) + TeCl_2(g)$

ΔG_{rxn} (400°C) = -68.28 kcal/mol

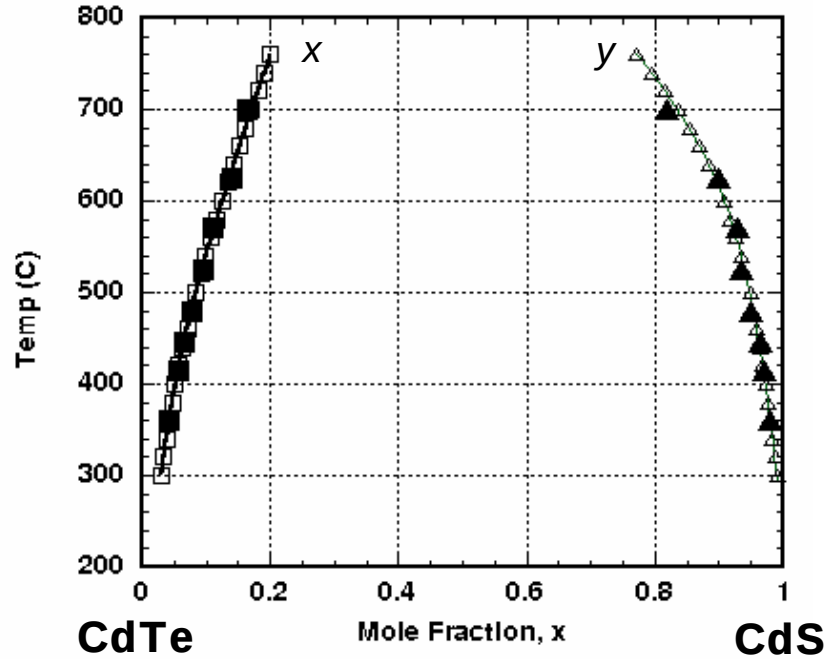
- *Lower working temperatures for $ZnCl_2$ compared to $CdCl_2$*
- *For vapor $CdCl_2$:O_2 HT in dry ambient, higher oxidation rate than in O_2 only*
- *nb: In humid ambient, halide sources poisoned by formation of CdO, ZnO*

**O. Knacke, O. Kubaschewski, K. Hesselmann, Thermochemical Properties Inorg. Sub. 1991*

Quantitative Relationships: Alloy Formation

Miscibility Gap*: Measured (solid) and Modeled (open)

Modeled solubility accounts for non-ideal mixing thermodynamics



Data shown for $CdCl_2$ at 3 mTorr: enhances rate, not end-point

$ZnCl_2$ different: reacts with CdS, converts to ZnS

$CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ solubility

$$x = (4.717e-2) + (-3.104e-4)T + (9.543e-8)T^2 + (-3.687e-10)T^3$$
$$y = (-1.684e-1) + (1.172e-3)T + (-2.639e-7)T^2 + (2.348e-10)T^3$$

*B. E. McCandless, G. M Hanket, D.G. Jensen, R. W. Birkmire, J. Vac. Sci. Tech. A 20(4) 2002 1462-1467

Quantitative Relationships: Alloy and Oxide Properties

$CdTe_{1-x}S_x$ Thin Film Optical Band Gap

$CdTe_{1-y}S_y$: Eg (eV) = 1.51 – 0.94y + 1.84y(1-y), (b~1.7, x-tal)

Thin Film Oxide Properties

Oxide	Structure	Eg (eV)	σ_d (S/cm)	E_A (eV)	σ_L (S/cm)
CdO	halite	2.35	$< 10^{-5}$	-	$< 1O^{-5}$
$CdTeO_3$	monoclinic	3.65	$4x10^{-4}$	0.1	$3.5x10^{-3}$
$CdTe_2O_5$	triclinic	?	?	?	?

- *CdS diffusion reduces CdTe band gap, E_g = 1.41 eV at 480ºC sol limit*
- *CdO insulating, $CdTeO_3$ photoconductive*

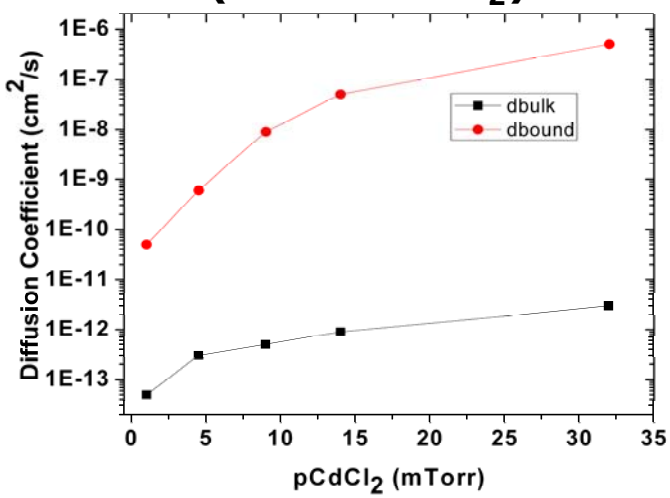
Quantitative Relationships: Bulk and Grain Boundary Diffusion

Measured diffusion coefficients for CdS in CdTe*
at 1 atm, p($CdCl_2$) = 9 mTorr and p(O_2) = 150 Torr:

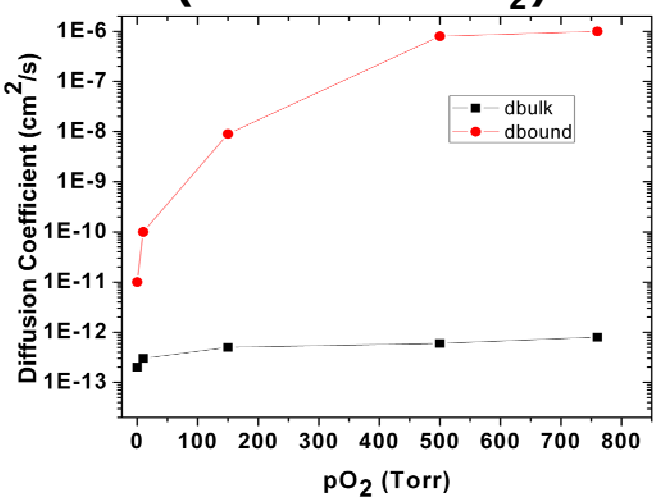
$$D_{grain_bulk} = 2.4x10^{7}\ exp(-2.8/kT)$$

$$D_{grain_boundary} = 3.4x10^{6}\ exp(-2.0/kT)$$

$CdCl_2$ Partial Pressure (150 Torr O_2)



O_2 Partial Pressure (9 mTorr $CdCl_2$)



- *Ambient chemistry: strong effect on grain boundary, weak on bulk diffusivity*
- *Vapor treatment allows separation of reaction temperature from $CdCl_2$ concentration*

**B. E. McCandless, M. G. Engelmann, R. W. Birkmire, J. Appl. Phys. 89(2) 2001 988-994*

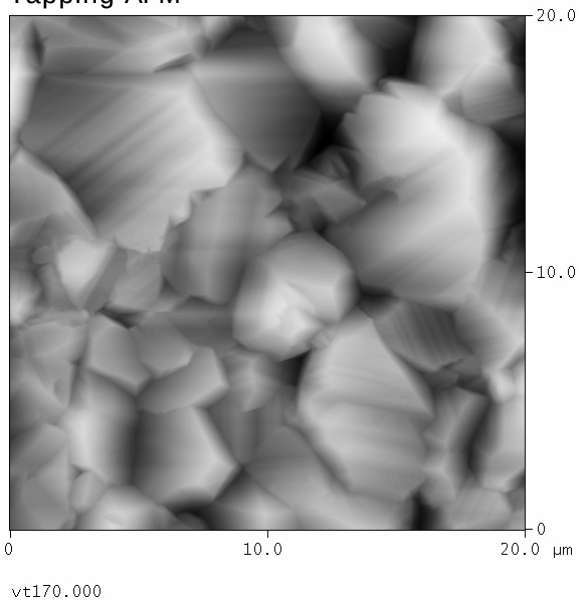
Results: Diffusion Modeling

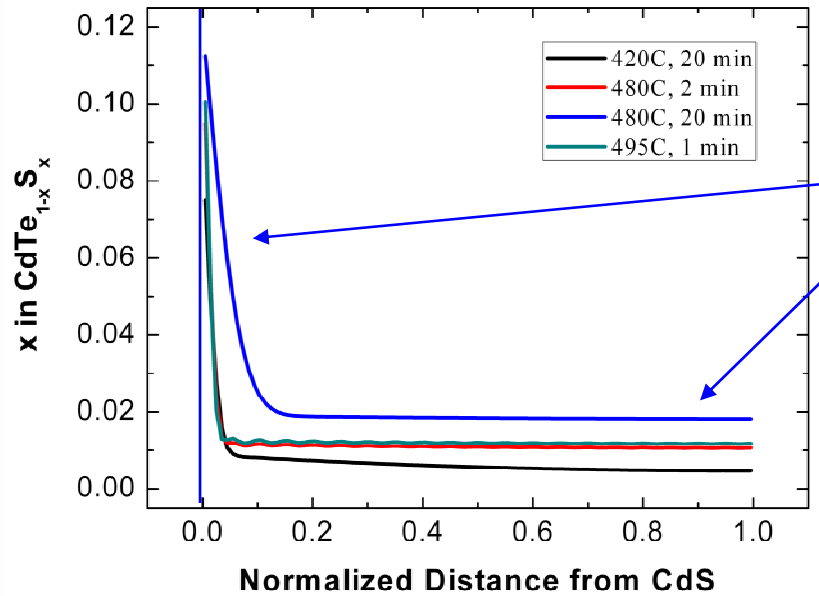
Modeled 2D diffusion* for:

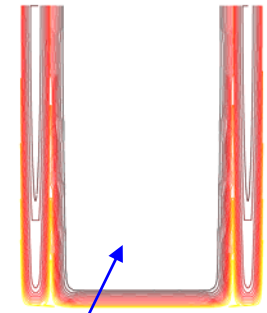
5 μm VT CdTe film deposited at 550ºC in He:O_2 with log-normal grain size distribution, peak = 5 μm

p(O_2) = 150 torr, p($CdCl_2$) = 9 mTorr

Tapping AFM







bulk

grain boundary

d_{eq}(CdS)

100 nm

40 nm

20 nm

- *Modeling allows estimation of CdS consumption under different processing conditions*
- *For treatment at 480ºC for 2 min, expect band gap reduction at CdS, 40 nm CdS loss and ~ 13 nm $CdTeO_3$*

**B. E. McCandless, M. G. Engelmann, R. W. Birkmire, J. Appl. Phys. 89(2) 2001 988-994*

Results: Devices w/ Different CdTe Growth Rate

10 x 10 cm SL/TEC15 plate, Ga_2O_3 HRT, 80 nm CdS
VT CdTe 6-7 μm thick, deposited at 550ºC in $He:O_2$
vapor $CdCl_2$ HT at 420ºC, 20 min , BDH etch, Cu/Ni contact, 0.36 cm2

Best cell of 8 cells per piece

CdTe GR (μm/min)	Time/ plate (min)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
6	8	806	23.5	67	12.7
9	8	842	24.1	64	13.0
12	8	804	23.8	66	12.7
81	1.2	736	24.8	53	11.0

High growth rate → lower junction quality

Results: Devices, Varied Vapor $CdCl_2$ T, t

Cells from 3 VT runs: 8-10 μm/min, Cu/Ni contact, 0.36 cm^2

T CdTe (ºC)	time (min)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
None	-	640	13.5	48.4	4.2
415	25	801	23.0	71.7	13.2
420	20	801	22.5	70.0	12.6
410	20	808	23.8	69.2	13.3
440	2	634	20.4	60.2	7.8
465	2	755	24.2	60.2	11.0
480	2	804	24.7	63.3	12.6
495	2	787	25.6	65.1	13.1
490	0.5	740	24.9	51.3	9.5

- *Reduced $CdCl_2$ treatment time by 10X → recover junction quality by raising temperature*
- *Higher temperature → higher Jsc due to increased CdS diffusion*
- *FF loss → voltage dependent collection (S. Hegedus)*

Results: Devices, Varied Vapor $CdCl_2$ time

Cells from 1 VT run: 7 μm/min, Cu/Ni contact, 0.36 cm^2

T CdTe (ºC)	time (min)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	QE @ 400 (nm)	Final dCdS (nm)
480	1	783	23.6	66.6	12.3	40	60
480	2	813	23.6	66.2	12.7	44	55
480	2.5	800	23.3	65.1	12.2	44	55
480	4	819	24.3	64.6	12.9	50	35

Vapor $CdCl_2$ HT at 480ºC:

- *Voc and FF ~constant for 2-4 min treatment time*
- *CdS diffusion controlled by treatment time*

Results: Devices, Modified Etch

Best cell of 8 per piece, Cu/Ni Contact, 0.36 cm^2

Etch	time (min)	GIXRD*	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
BDH	4	30 nm Te	750	24.0	60.0	11.0
Aniline	4	10 nm Te	783	23.6	66.6	12.3
None	-	CdTe	800	23.3	65.1	12.2

No crossover or rollover in these devices

Reduced $CdCl_2$ treatment time simplifies contact process:

- *Reduced oxide formation*
- *Elimination of process step*
- *Stability?*

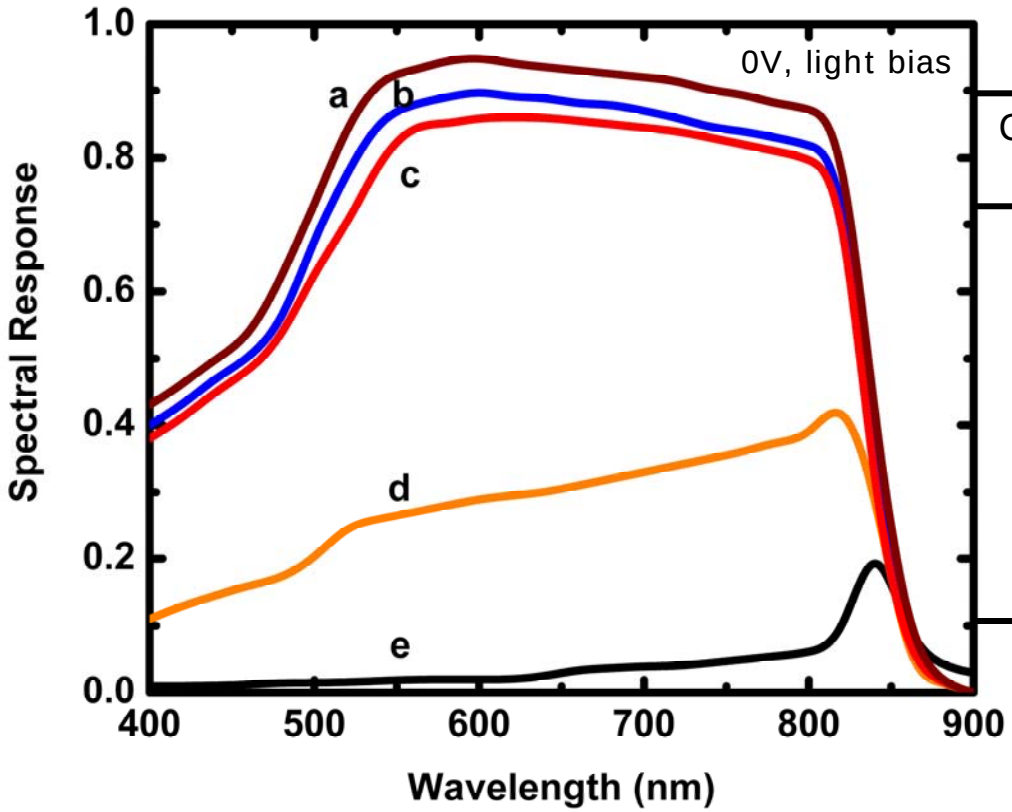
**B. E. McCandless, Conf. Rec. Spring M.R.S. Meeting, San Francisco (2005)*

Conclusions

1. Separation of process variables facilitates dramatic reduction of processing time and control of oxidation and CdS consumption
2. Analytic expressions determined for CdTe growth, oxidation, interdiffusion, etching
3. CdTe growth rate ~80 μm/min → reduced junction quality
4. For short vapor $CdCl_2$ treatments, 1-2 min, junction quality maintained by raising treatment temperature
5. Shorter $CdCl_2$ treatments promotes less oxidation, removing need for etch
6. Carrier gas influences electrical properties

Results: QE and Voc Process Sensitivity

Cells from 2 VT depositions (He and N_2), 9 mm/min, 2 min vapor $CdCl_2$ HT



Cell	Carrier Gas	$pCdCl_2$ (mTorr)	pO_2 (Torr)	Voc (mV)
a	N_2	3	150	800
b	N_2	0.1	150	794
c	N_2	3	$<10^{-6}$	650
d	N_2	0	0	650
e	He	0	0	550

Continuous flow

- *For no $CdCl_2$ HT, improved collection for CdTe deposited in N_2 carrier gas*
- *For vapor $CdCl_2$ HT, optimal collection for 3 mTorr $CdCl_2$ and 150 Torr O_2*
- *Not shown: O_2 only required during first few seconds of HT to achieve high Voc and QE*

Performance and defects in CSS and VTD CdTe cells treated with and without Cu and $CdCl_2$

Fred H. Seymour

Victor Kaydanov

Tim R. Ohno

OUTLINE

- Introduction
- J-V performance results
- Admittance Spectroscopy defect detection
- Defect correlations to V_{OC}
- Conclusions

INTRODUCTION

Cells sources and treatment

- Four sources
  - NREL – CSS/Cd_2SnO_4 (CdTe T_{SUB}=625^oC)
  - NREL – CSS (CdTe T_{SUB}=610-620^oC)
  - IEC – VTD (CdTe T_{SUB}=550-575^oC)
  - CSM – VTD/Gas Jet (CdTe T_{SUB}>375^oC)

- Four post-deposition treatments
  - Yes Cu and Yes $CdCl_2$
  - No Cu and Yes $CdCl_2$
  - Yes Cu and No $CdCl_2$
  - No Cu and No $CdCl_2$

Performance Results

Efficiency (%)

$Cu/CdCl_2$	Wnrel	Anrel	IEC	CSM
yes/yes	14.1	12.4	11.2	10.0
no/yes	7.2	11.1	8.7	5.6
yes/no	10.4	9.0	2.9	0.6
no/no	8.5	7.3	2.1	0.0

J_{SC} (mA cm^{-2})

$Cu/CdCl_2$	Wnrel	Anrel	IEC	CSM
yes/yes	23.7	23.9	23.6	24.4
no/yes	24.6	24.2	22.4	23.1
yes/no	20.9	22.0	10.1	4.7
no/no	18.9	21.2	10.0	0.1

V_{OC} (mV)

$Cu/CdCl_2$	Wnrel	Anrel	IEC	CSM
yes/yes	823	816	786	711
no/yes	658	784	709	612
yes/no	751	718	583	324
no/no	734	689	599	312

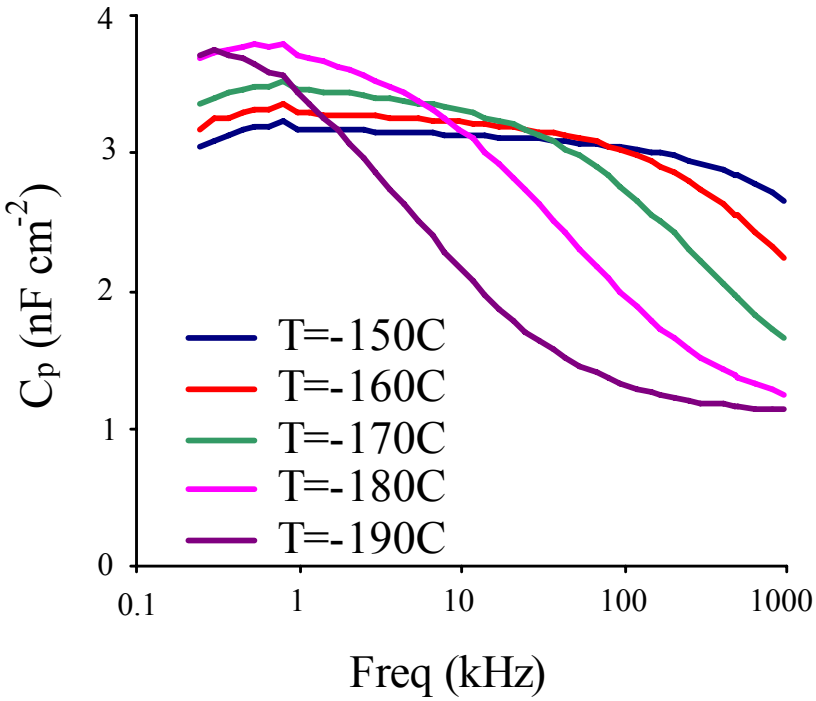
Fill Factor (%)

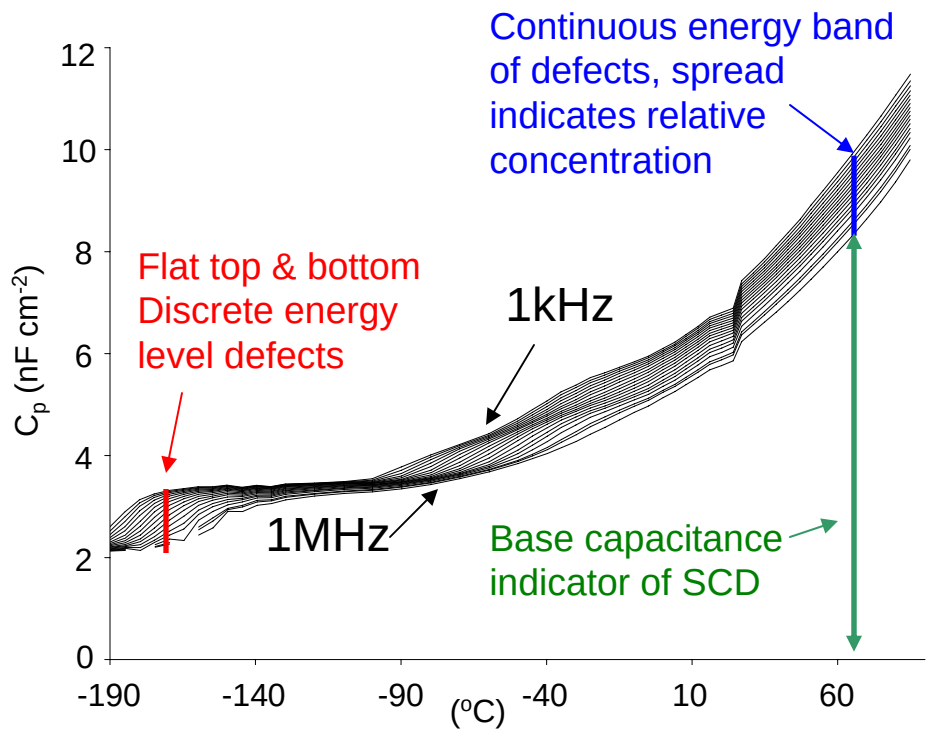
$Cu/CdCl_2$	Wnrel	Anrel	IEC	CSM
yes/yes	72	63	60	58
no/yes	44	59	55	41
yes/no	67	57	49	41
no/no	61	50	35	25

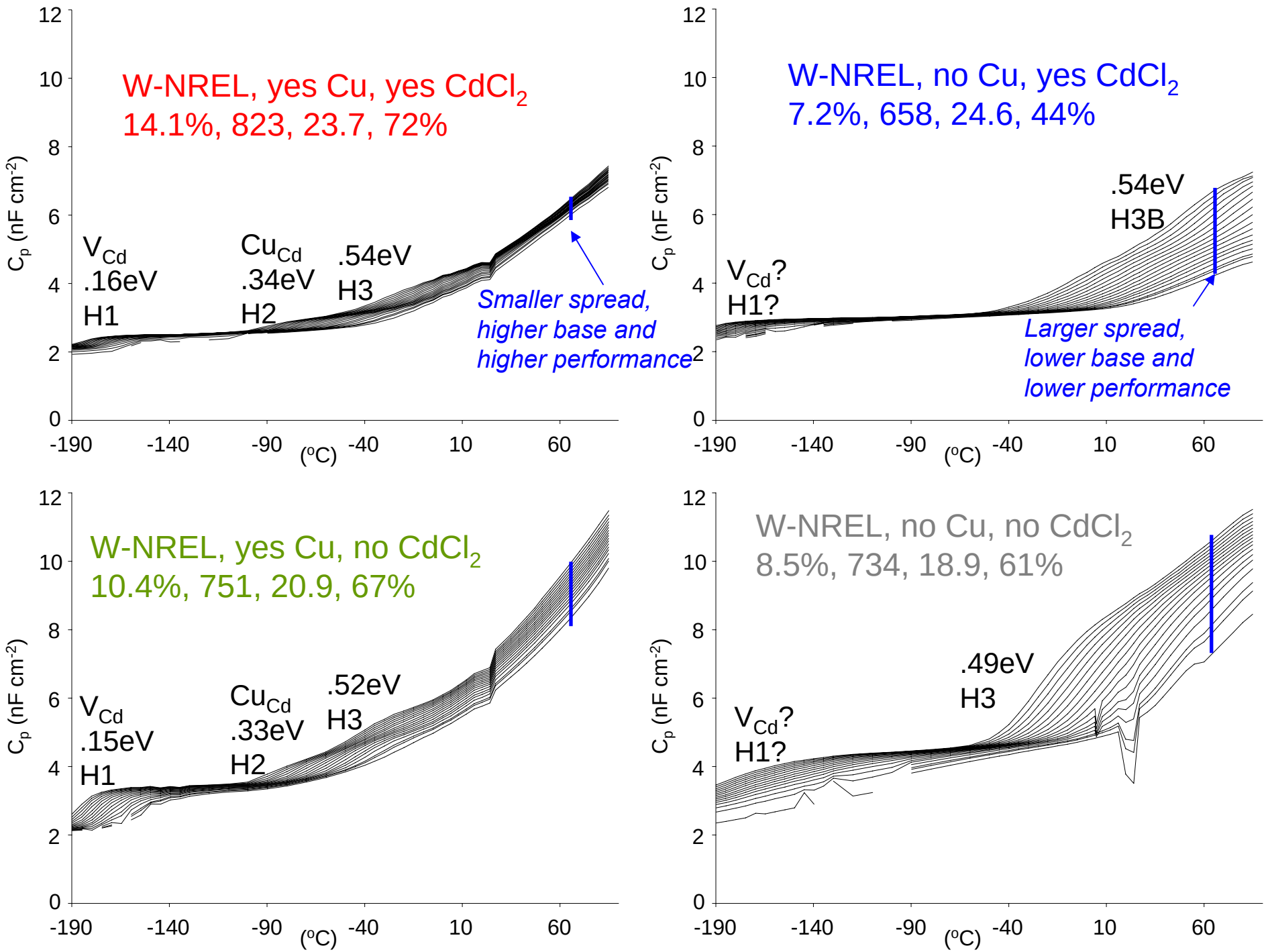
Admittance Spectroscopy

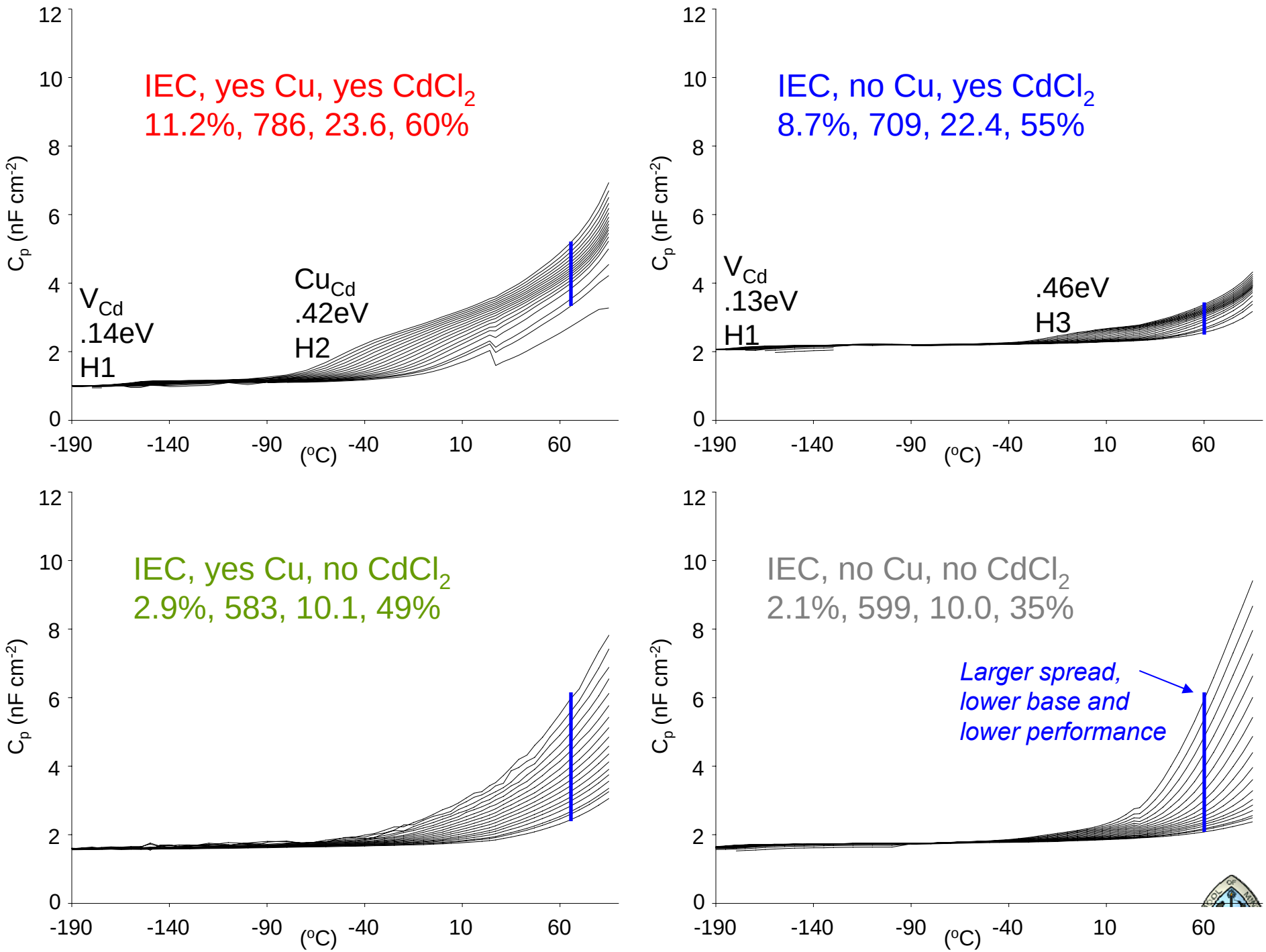
Tool for detecting deep electronic states that can impact cell performance

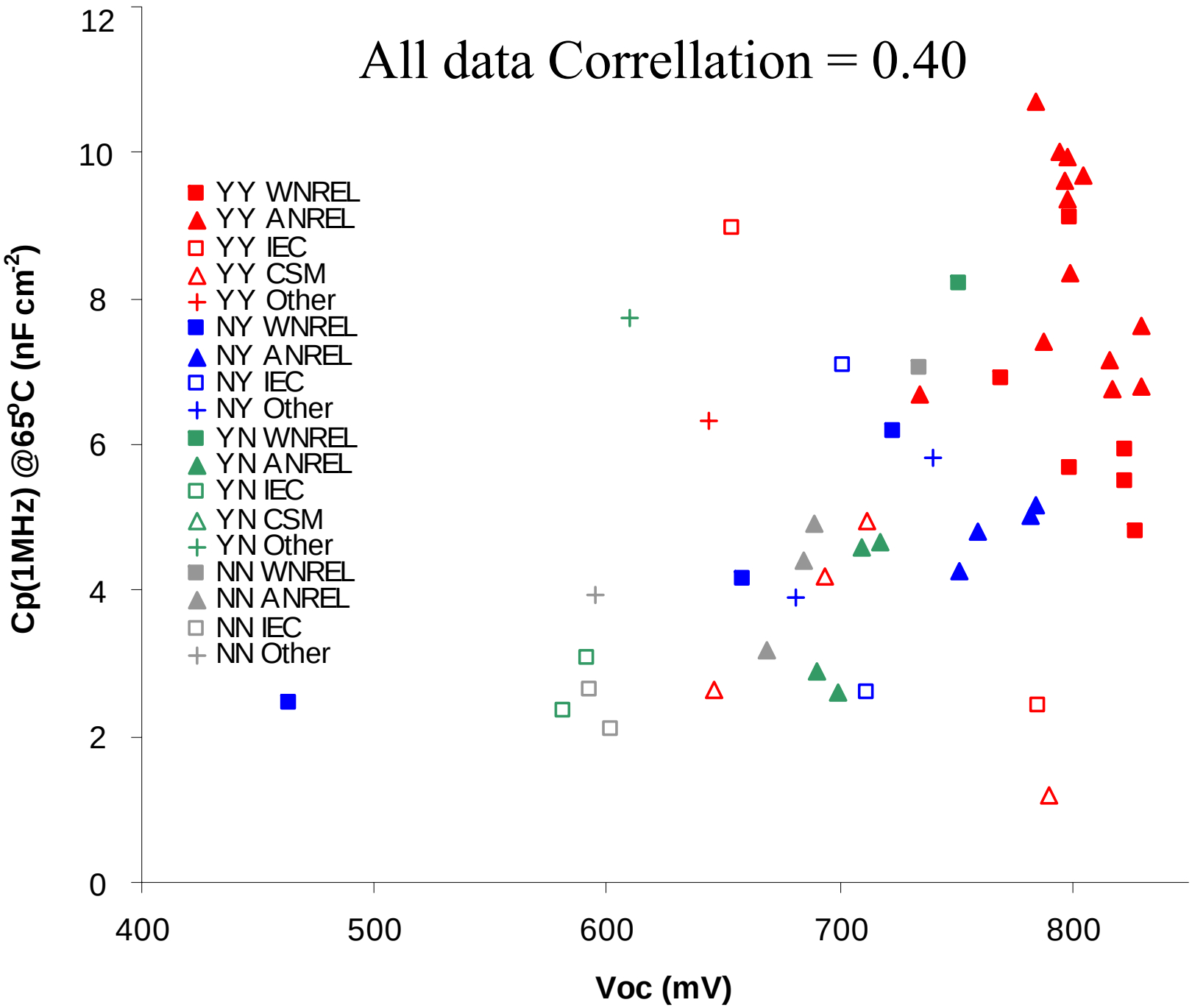
$$e_p = \sigma_p v_p N_v \exp\left(\frac{-(E_t - E_V)}{K_b T}\right) \quad c_p = \sigma_p v_p N_v \exp\left(\frac{-(E_f - E_V)}{K_b T}\right) \quad \omega_t = e_p + c_p + e_n + c_n$$

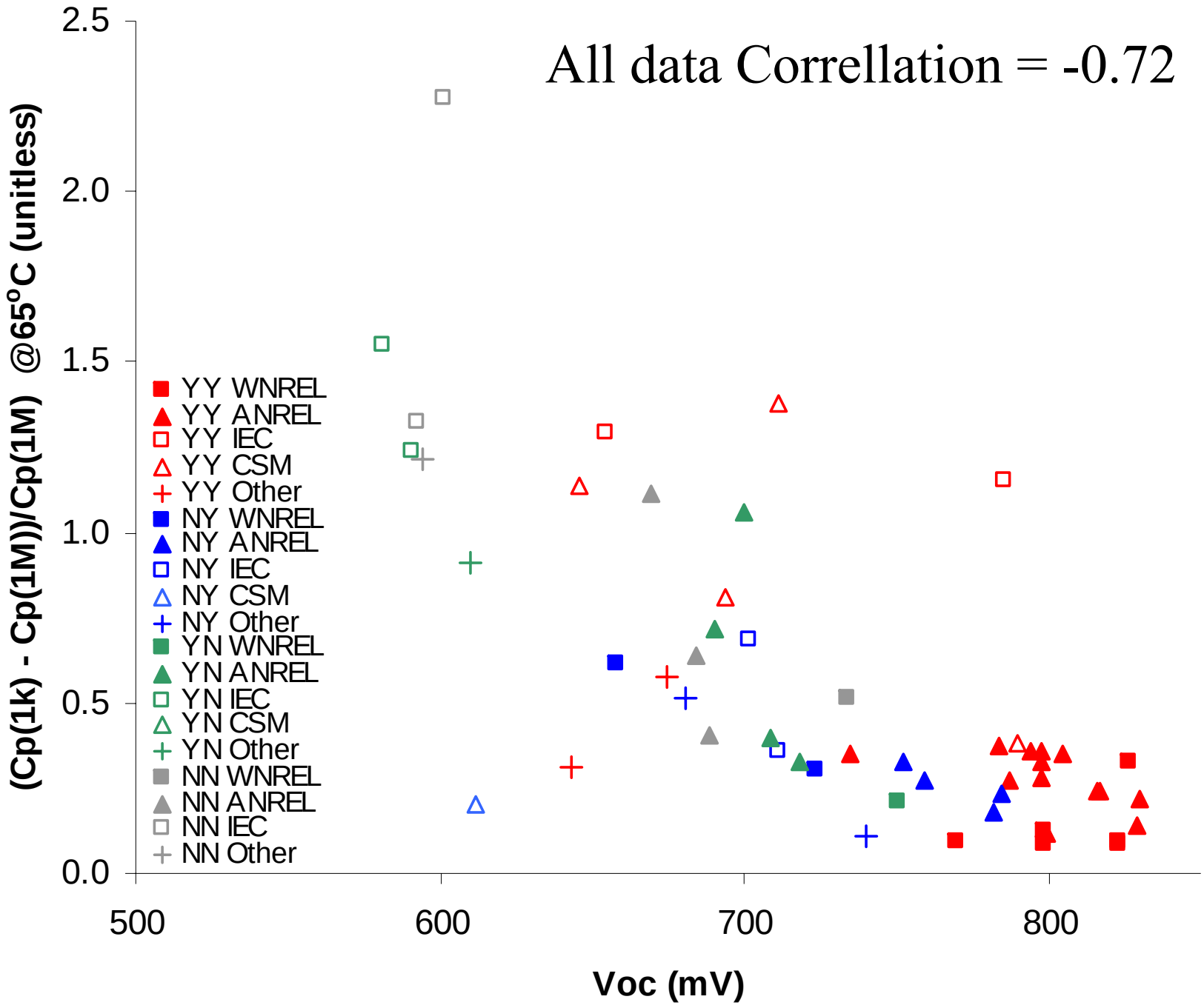





W-NREL, yes Cu, yes CdCl2
14.1%, 823, 23.7, 72%
VCd
.16eV
H1
CuCd
.34eV
H2
.54eV
H3
Smaller spread, higher base and higher performance
W-NREL, no Cu, yes CdCl2
7.2%, 658, 24.6, 44%
VCd?
H1?
.54eV
H3B
Larger spread, lower base and lower performance
W-NREL, yes Cu, no CdCl2
10.4%, 751, 20.9, 67%
VCd
.15eV
H1
CuCd
.33eV
H2
.52eV
H3
W-NREL, no Cu, no CdCl2
8.5%, 734, 18.9, 61%
VCd?
H1?
.49eV
H3
Cp (nF cm-2)
(oC)
-190
-140
-90
-40
10
60
0
2
4
6
8
10
12


IEC, yes Cu, yes CdCl2
11.2%, 786, 23.6, 60%
VCd
.14eV
H1
CuCd
.42eV
H2
IEC, no Cu, yes CdCl2
8.7%, 709, 22.4, 55%
VCd
.13eV
H1
.46eV
H3
IEC, yes Cu, no CdCl2
2.9%, 583, 10.1, 49%
IEC, no Cu, no CdCl2
2.1%, 599, 10.0, 35%
Larger spread,
lower base and
lower performance
Cp (nF cm-2)
(oC)
12
10
8
6
4
2
0
-190
-140
-90
-40
10
60

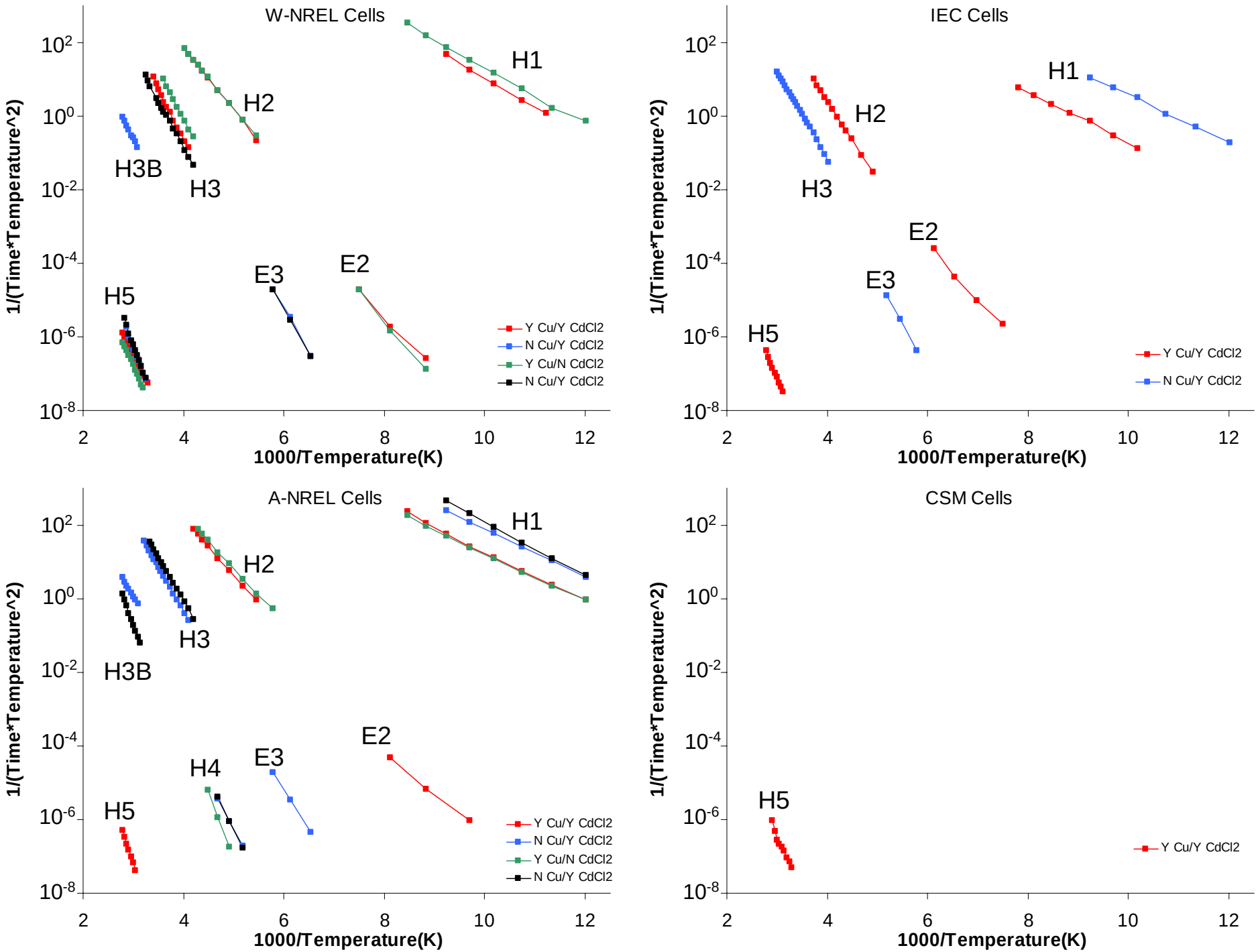

All data Correllation = 0.40
Cp(1MHz) @65°C (nF cm-2)
Voc (mV)
0
2
4
6
8
10
12
400
500
600
700
800
YY WNREL
YY ANREL
YY IEC
YY CSM
YY Other
NY WNREL
NY ANREL
NY IEC
NY Other
YN WNREL
YN ANREL
YN IEC
YN CSM
YN Other
NN WNREL
NN ANREL
NN IEC
NN Other


All data Correllation = -0.72
(Cp(1k) - Cp(1M))/Cp(1M) @65°C (unitless)
Voc (mV)
2.5
2.0
1.5
1.0
0.5
0.0
500
600
700
800
YY WNREL
YY ANREL
YY IEC
YY CSM
YY Other
NY WNREL
NY ANREL
NY IEC
NY CSM
NY Other
YN WNREL
YN ANREL
YN IEC
YN CSM
YN Other
NN WNREL
NN ANREL
NN IEC
NN Other

CONCLUSIONS

- Moderate negative correlation between capacitance spread at 65°C and V_{OC}
- Moderate positive correlation between 1MHz “base” capacitance at 65°C and V_{OC}
- VTD cell performance more sensitive than CSS to $CdCl_2$ treatment

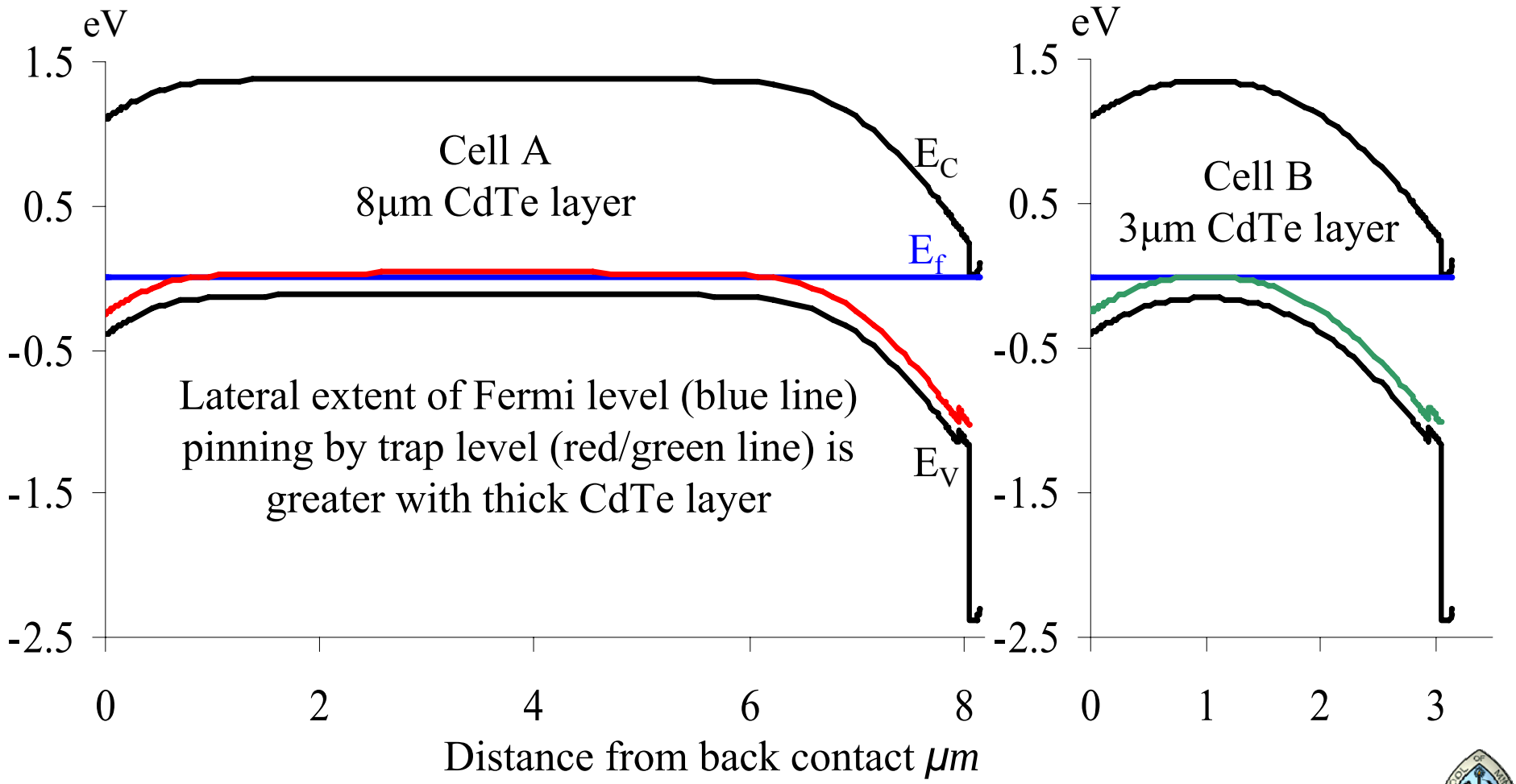
Supplemental Slides Follow

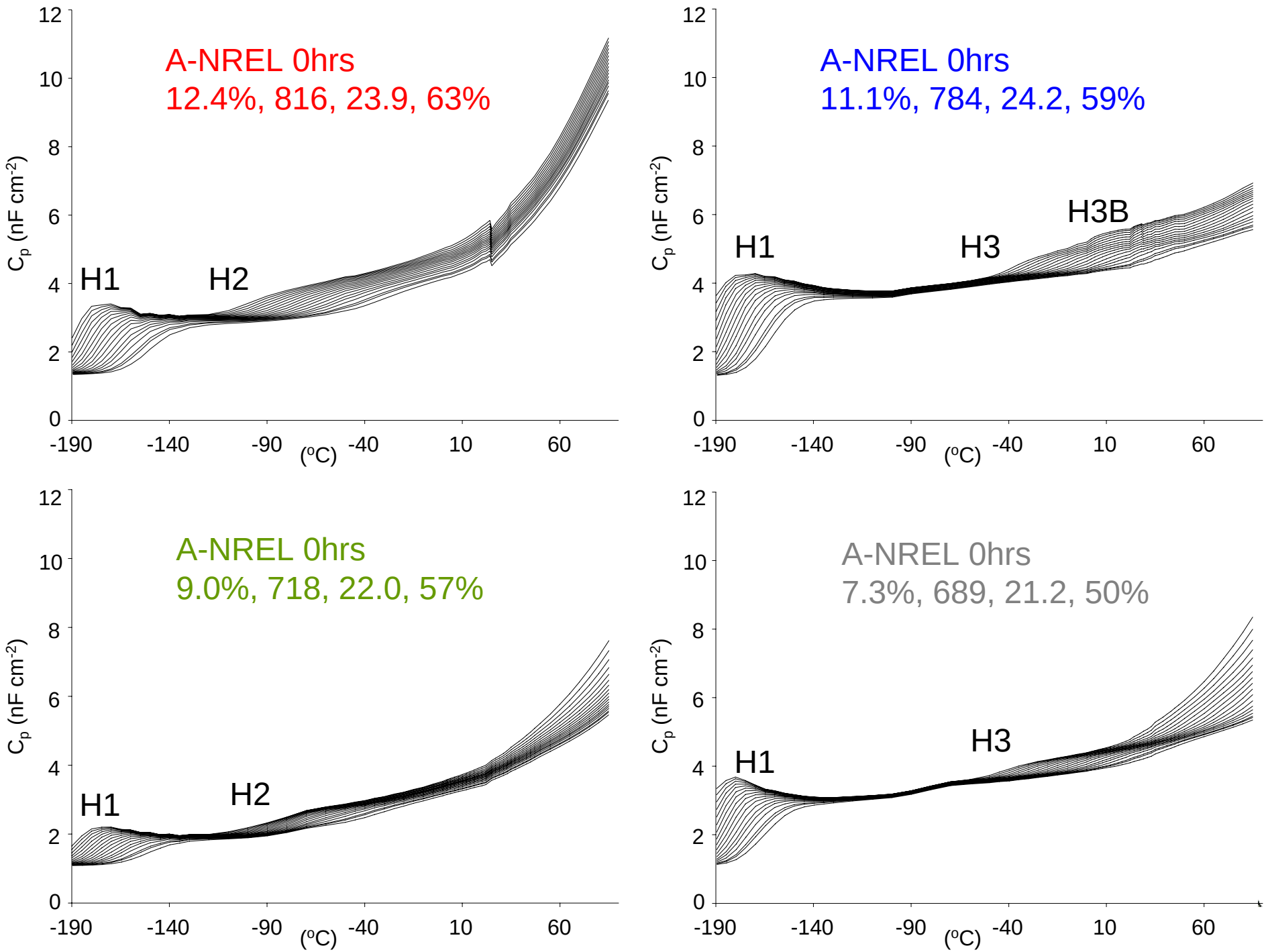

W-NREL Cells
IEC Cells
A-NREL Cells
CSM Cells
1/(Time*Temperature^2)
1000/Temperature(K)
H1
H2
H3
H3B
H4
H5
E2
E3
Y Cu/Y CdCl2
N Cu/Y CdCl2
Y Cu/N CdCl2
N Cu/Y CdCl2

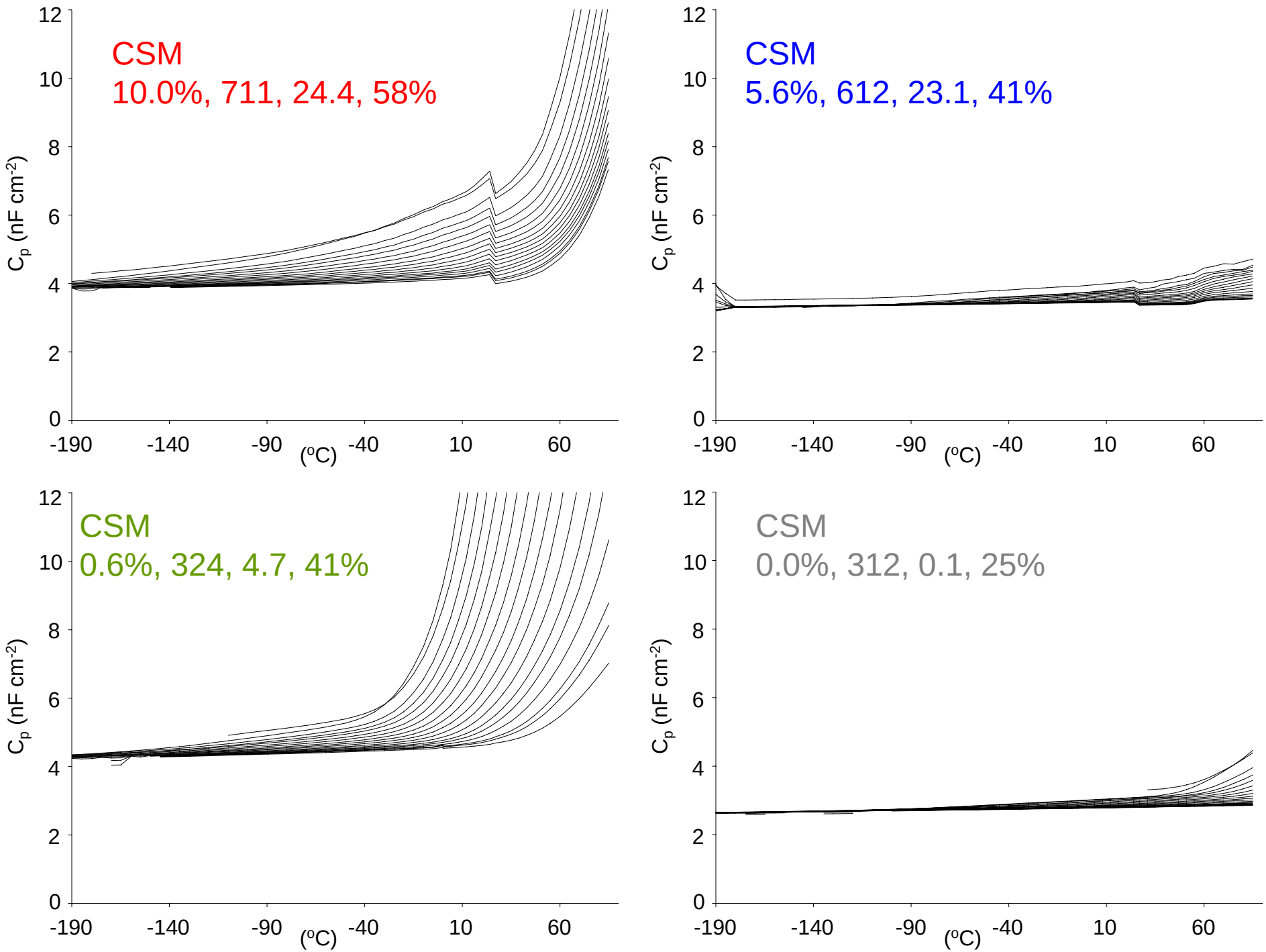
SCAPS Simulated CdTe Solar Cell, -170°C

Simulated DES, (E_a=0.15 eV, σ_a=2 X 10^{-14} cm^2 , N_t=3 X 10^{14} cm^{-3})

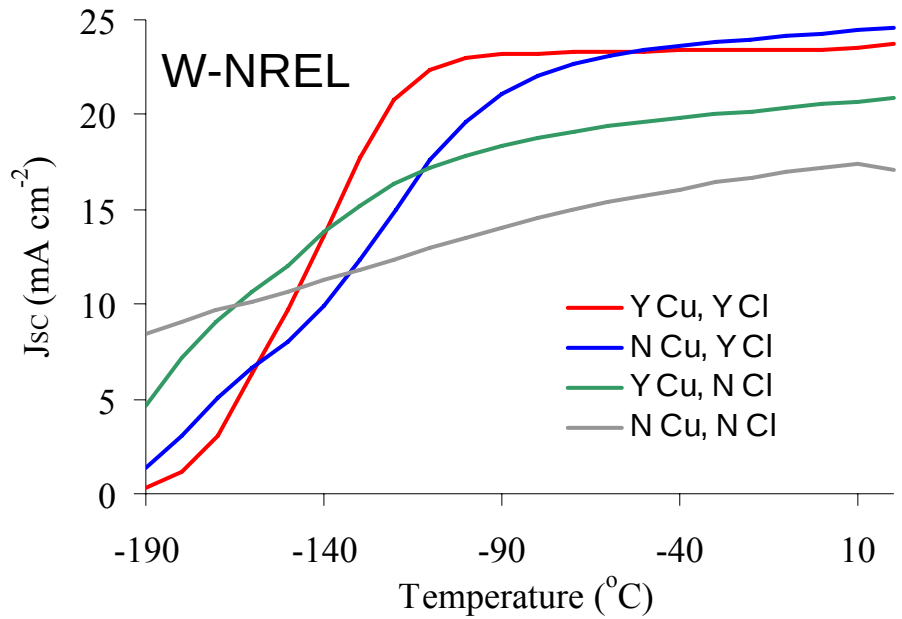
Negligible shallow level acceptor concentration N_a=10^{12} cm^{-3}

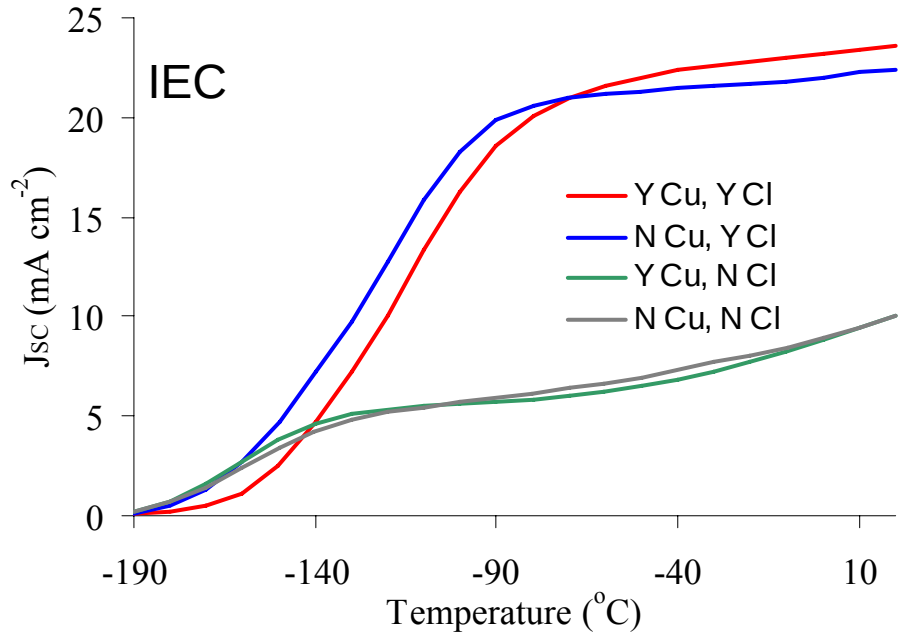


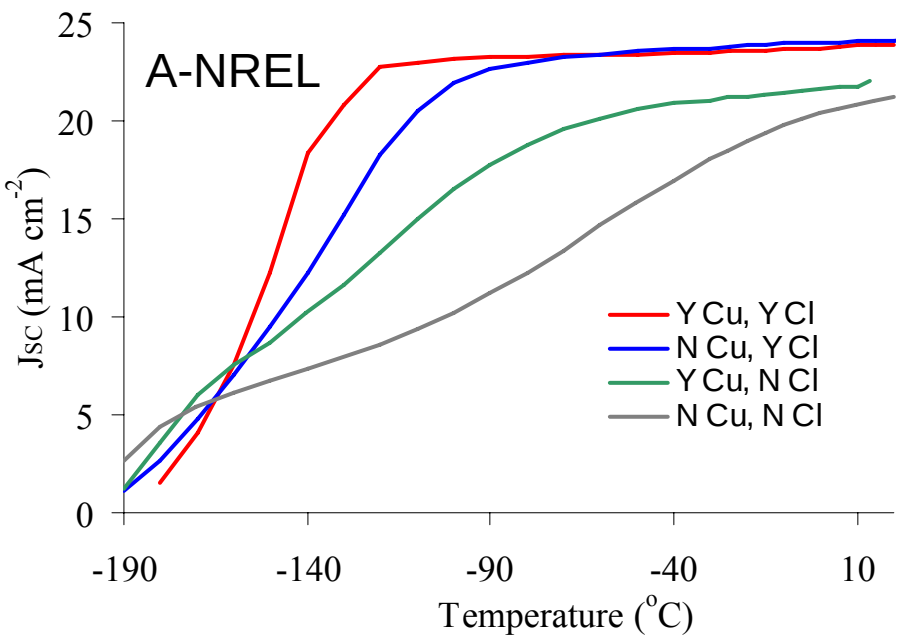

A-NREL 0hrs
12.4%, 816, 23.9, 63%
H1
H2
A-NREL 0hrs
11.1%, 784, 24.2, 59%
H1
H3
H3B
A-NREL 0hrs
9.0%, 718, 22.0, 57%
H1
H2
A-NREL 0hrs
7.3%, 689, 21.2, 50%
H1
H3
C_p (nF cm^{-2})
(°C)
0
2
4
6
8
10
12
-190
-140
-90
-40
10
60

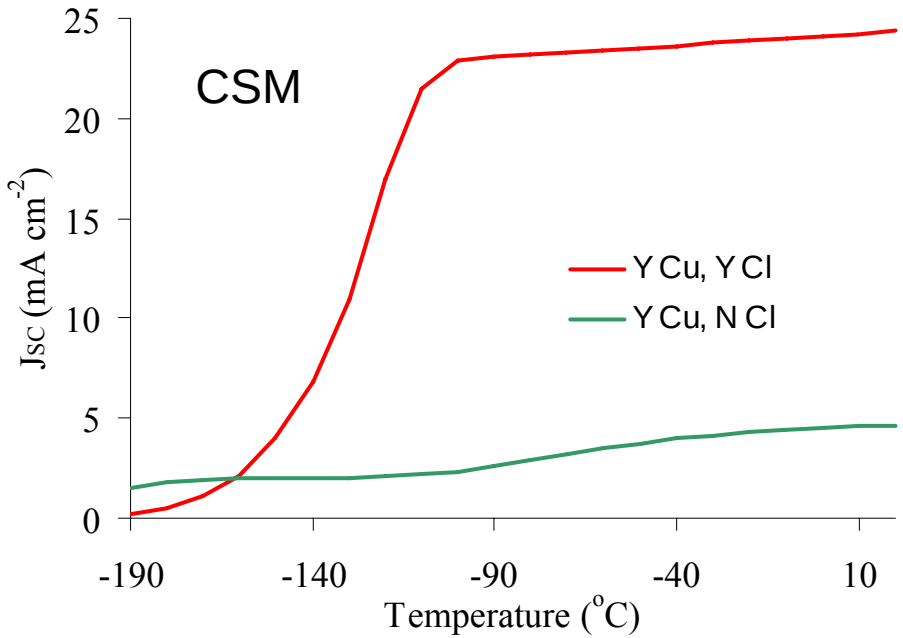

CSM
10.0%, 711, 24.4, 58%
CSM
5.6%, 612, 23.1, 41%
CSM
0.6%, 324, 4.7, 41%
CSM
0.0%, 312, 0.1, 25%
C_p (nF cm^{-2})
(°C)
0
2
4
6
8
10
12
-190
-140
-90
-40
10
60

J-V-T J_{SC} versus Temperature

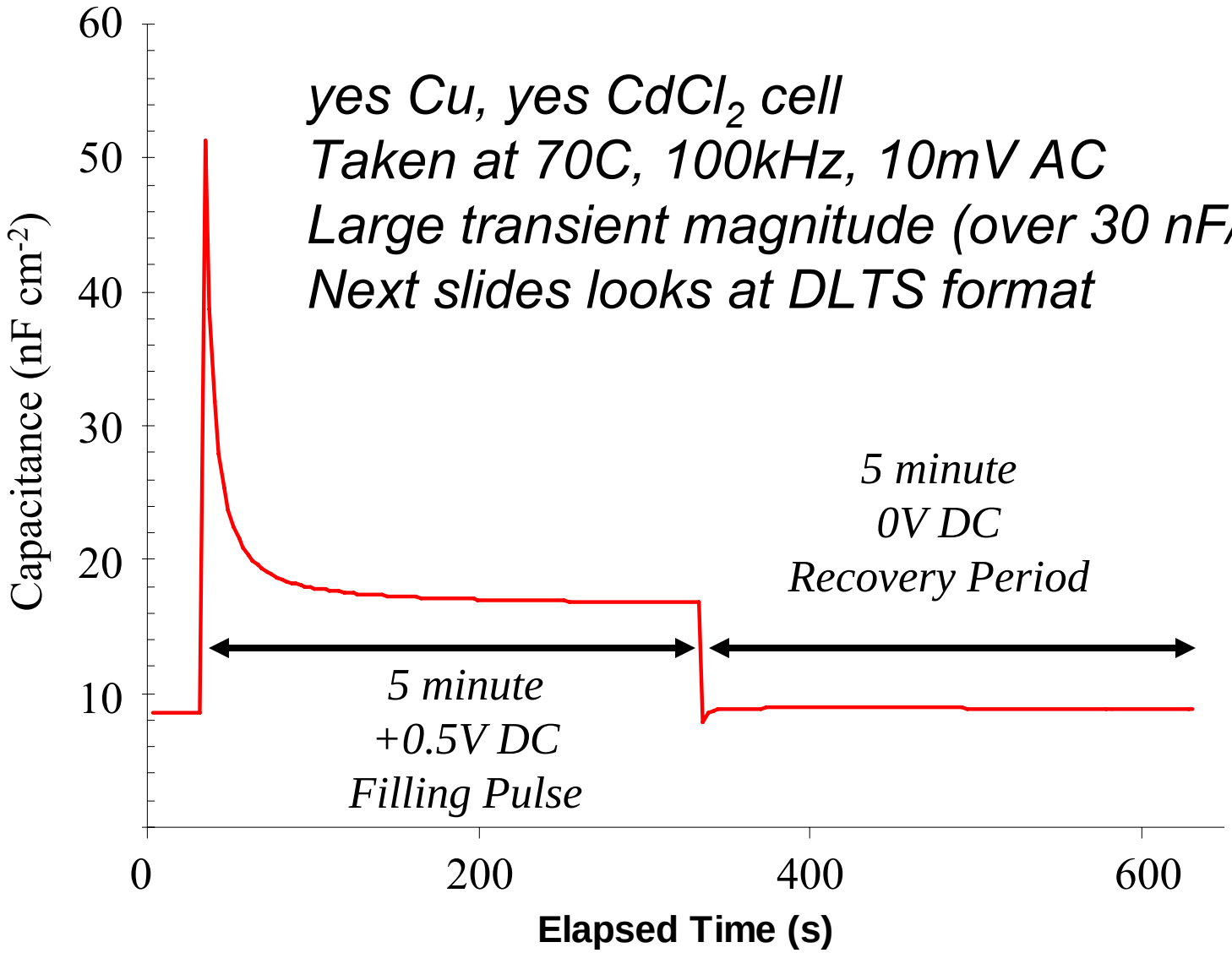




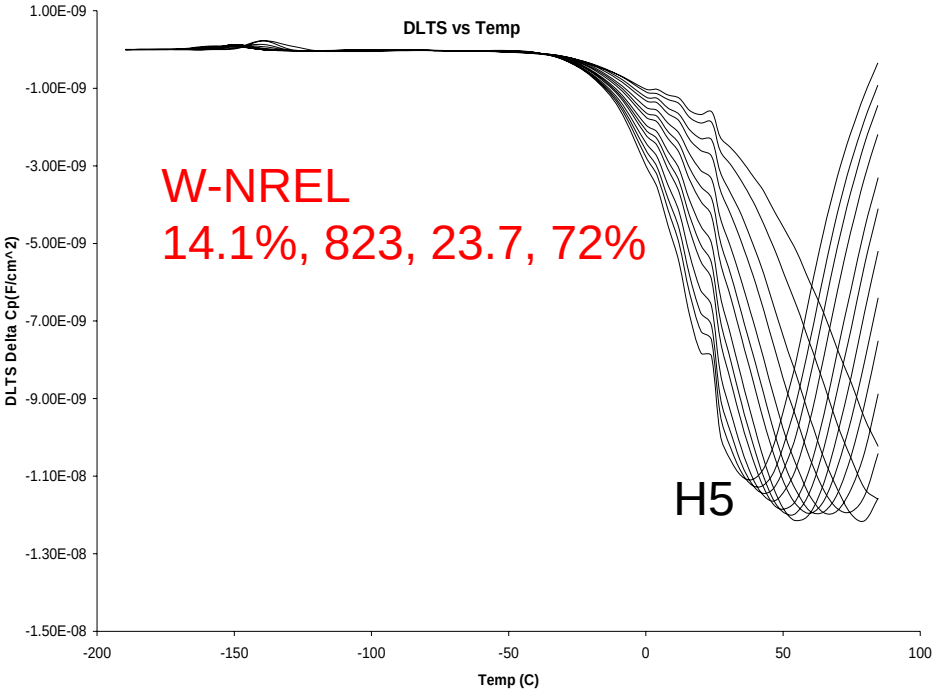


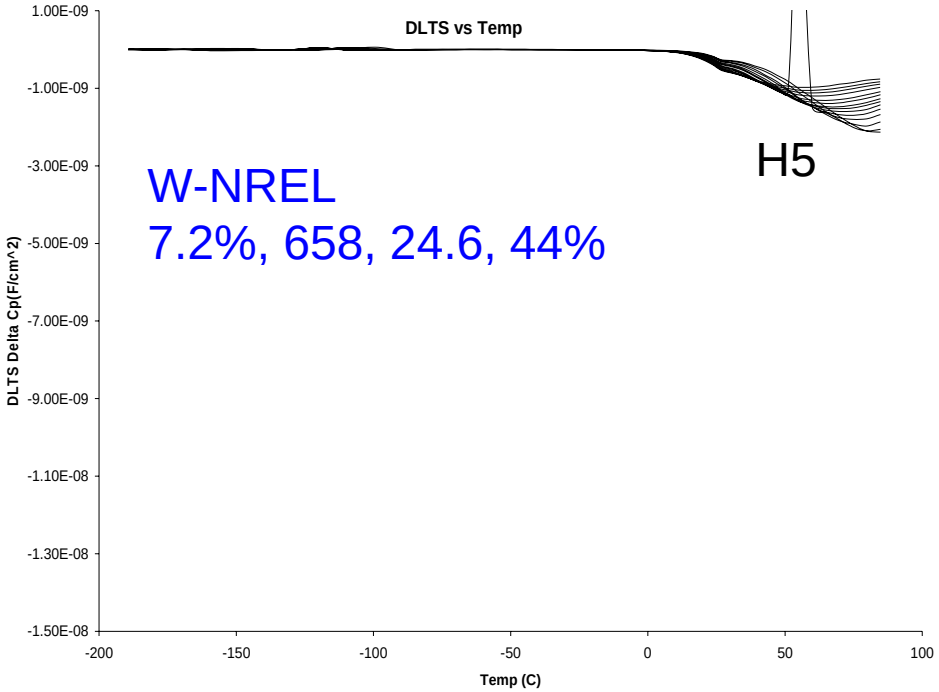


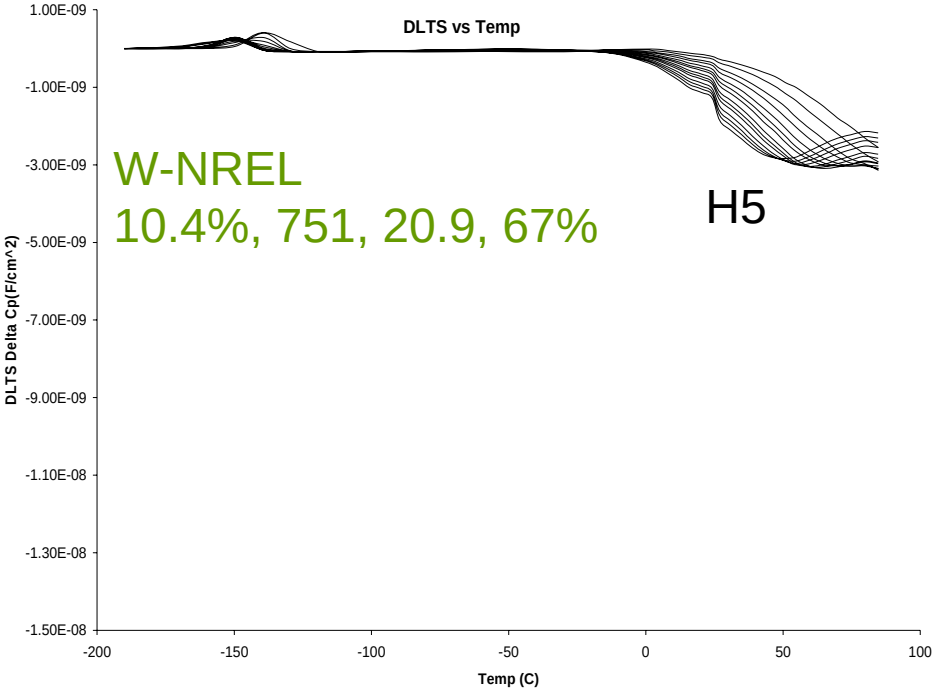
Capacitance Transient

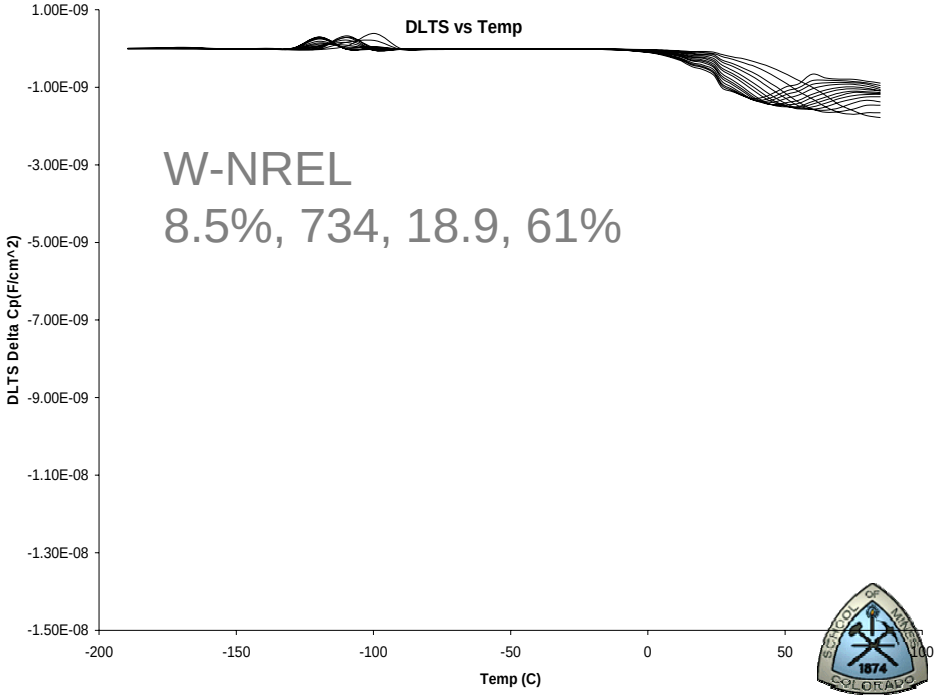


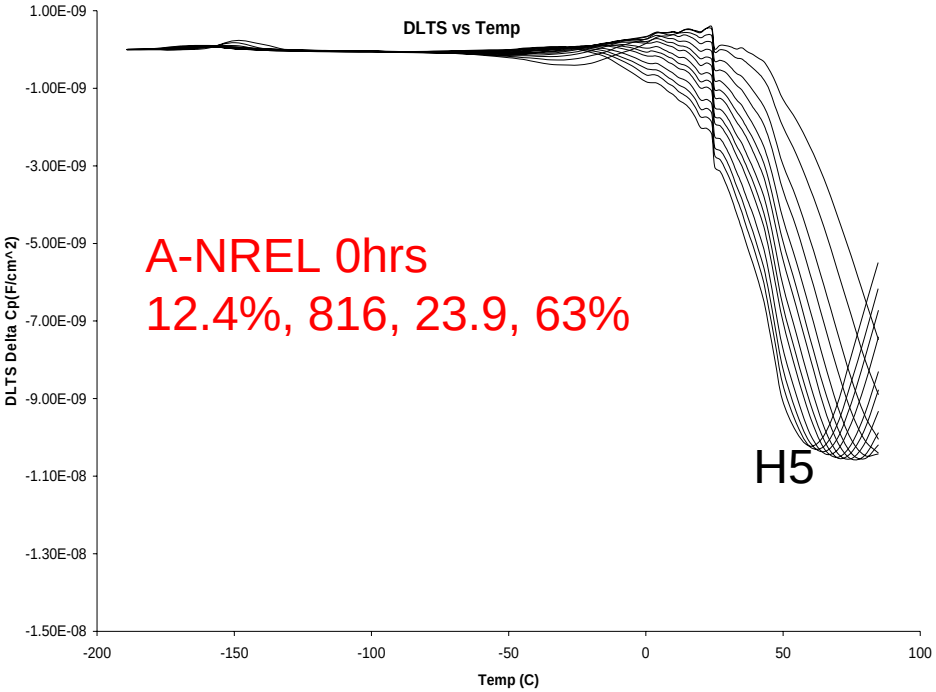
yes Cu, yes $CdCl_2$ cell
Taken at 70C, 100kHz, 10mV AC
Large transient magnitude (over 30 nF/cm^2)
Next slides looks at DLTS format

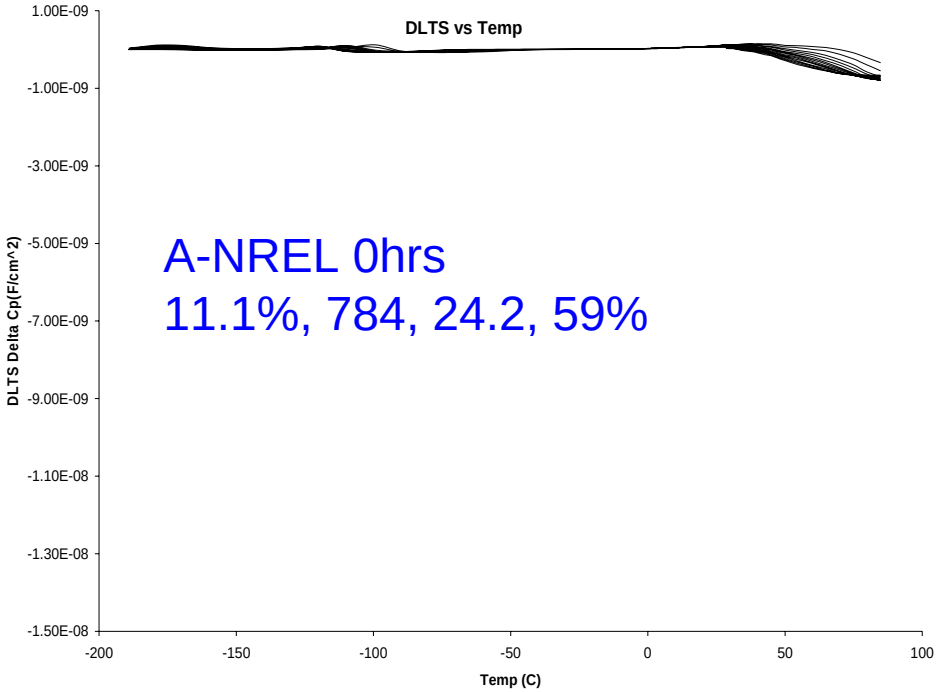

DLTS vs Temp
W-NREL
14.1%, 823, 23.7, 72%
H5
DLTS Delta Cp(F/cm^2)
Temp (C)

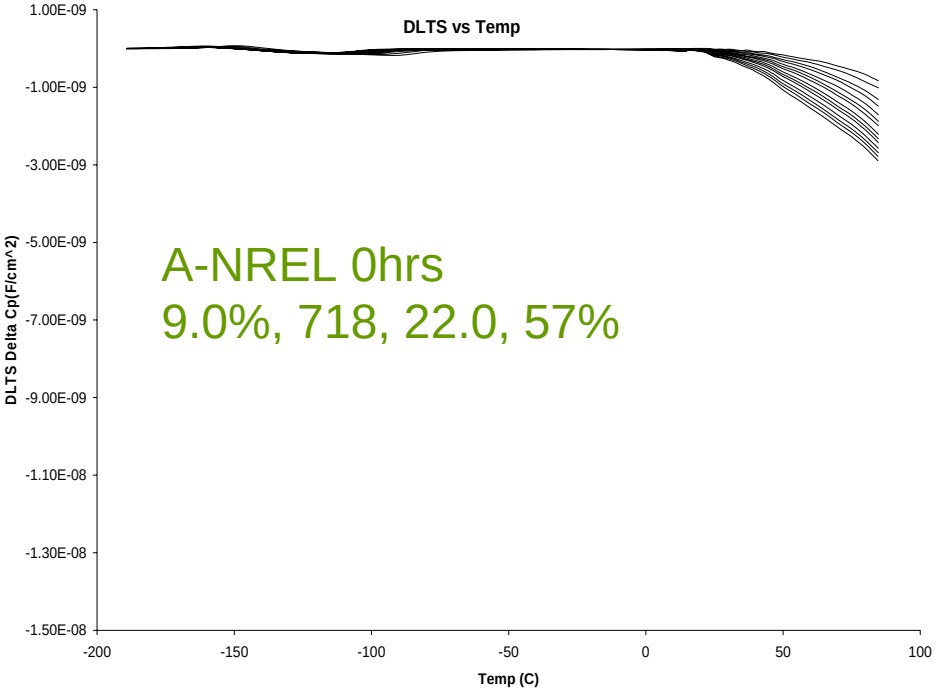

DLTS vs Temp
H5
W-NREL
7.2%, 658, 24.6, 44%
DLTS Delta Cp(F/cm^2)
Temp (C)

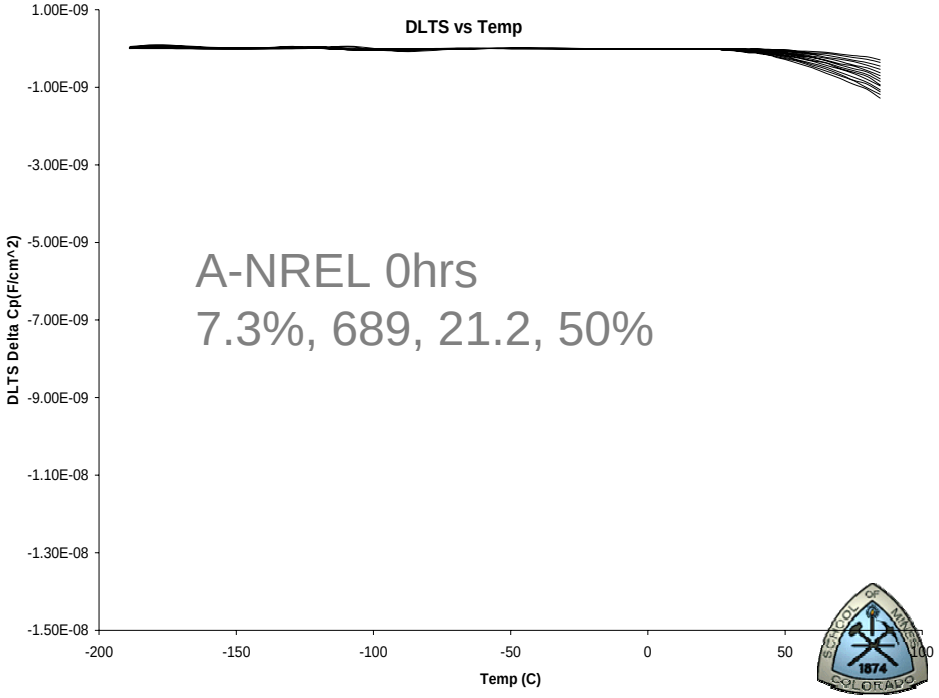

DLTS vs Temp
W-NREL
10.4%, 751, 20.9, 67%
H5
DLTS Delta Cp(F/cm^2)
Temp (C)

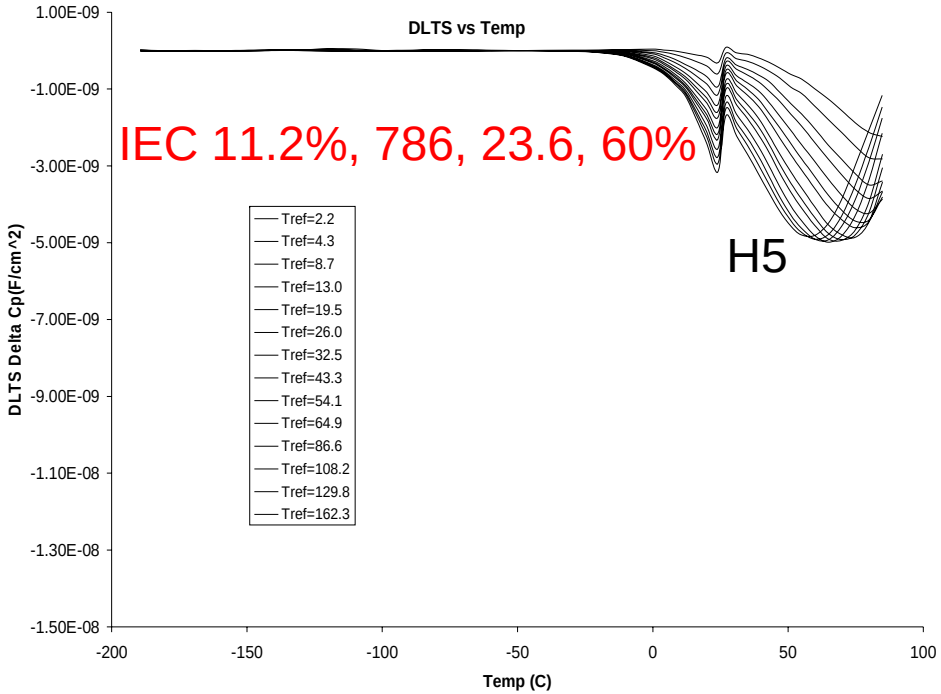

DLTS vs Temp
W-NREL
8.5%, 734, 18.9, 61%
DLTS Delta Cp(F/cm^2)
Temp (C)

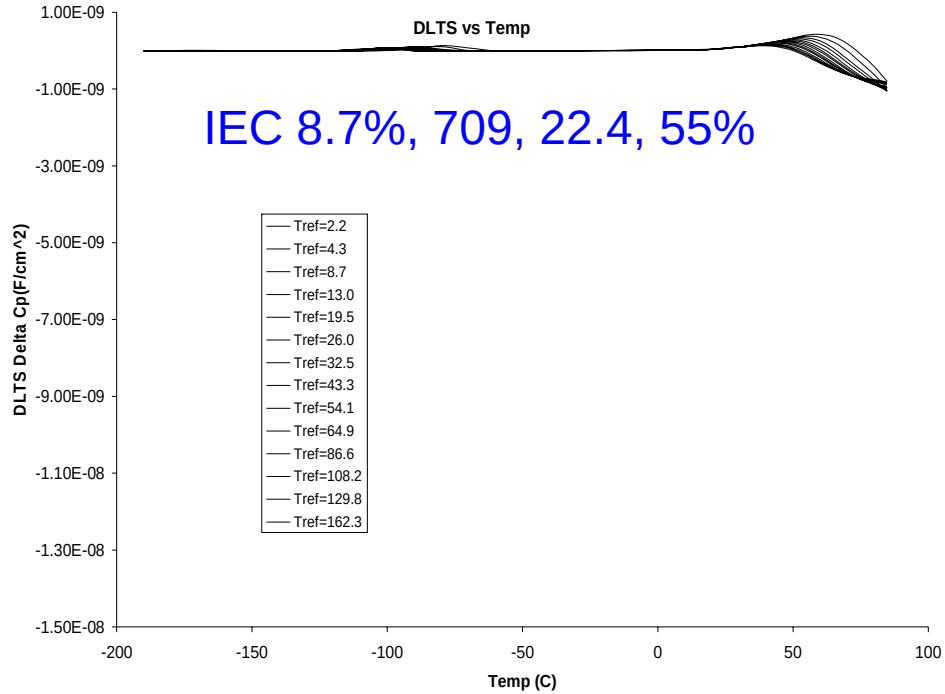

DLTS vs Temp
A-NREL 0hrs
12.4%, 816, 23.9, 63%
H5
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100

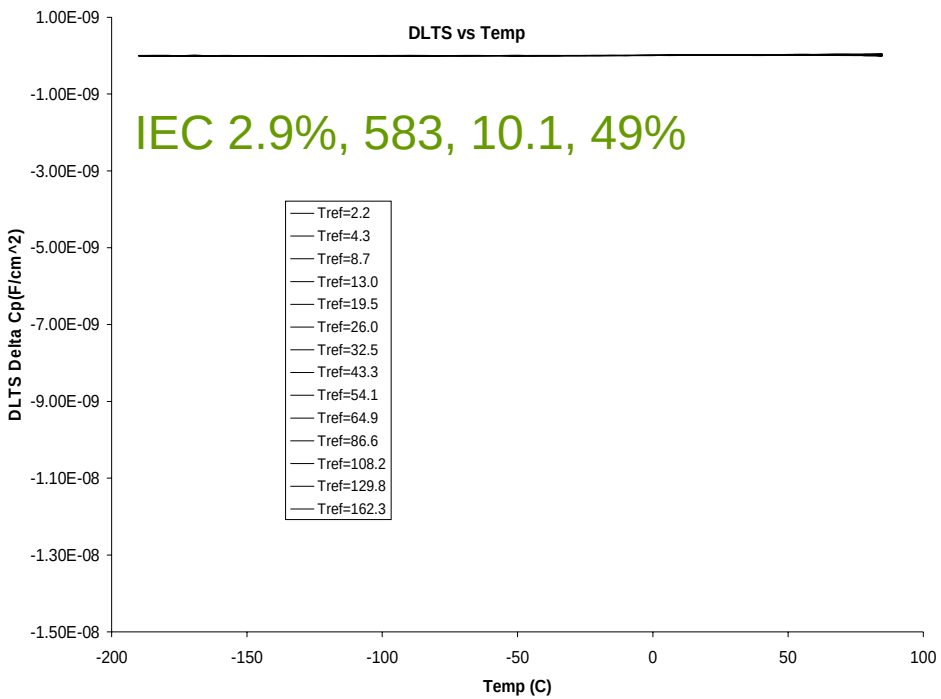

DLTS vs Temp
A-NREL 0hrs
11.1%, 784, 24.2, 59%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100

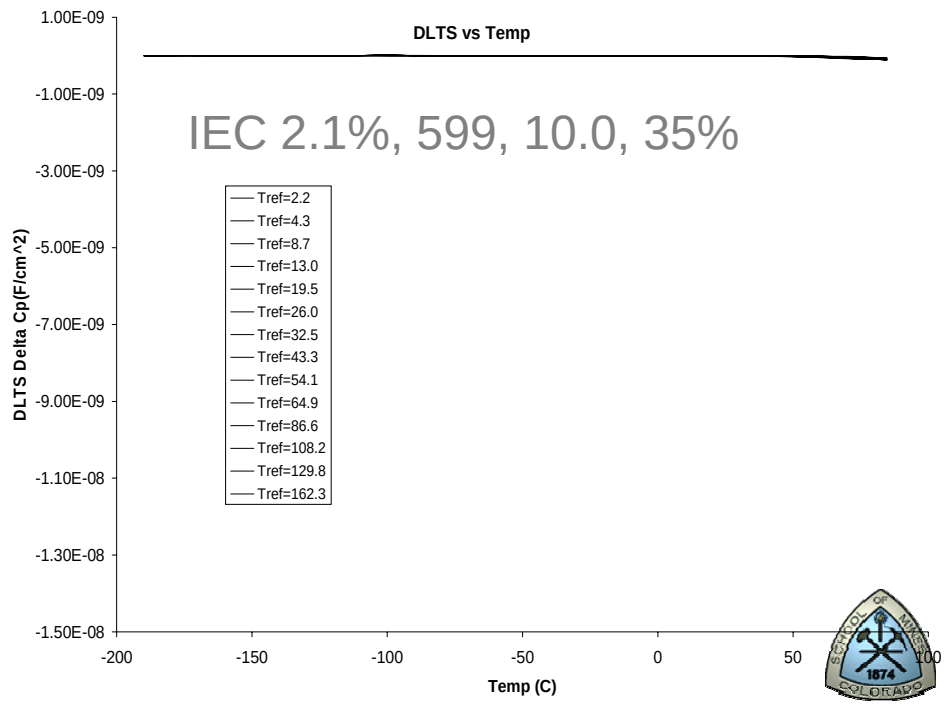

DLTS vs Temp
A-NREL 0hrs
9.0%, 718, 22.0, 57%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100

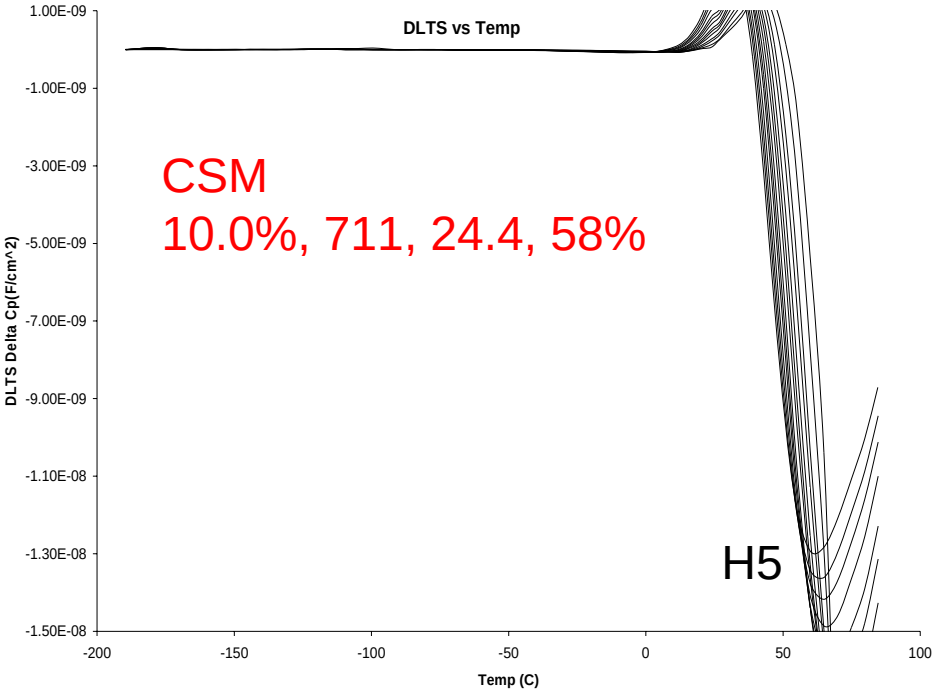

DLTS vs Temp
A-NREL 0hrs
7.3%, 689, 21.2, 50%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100

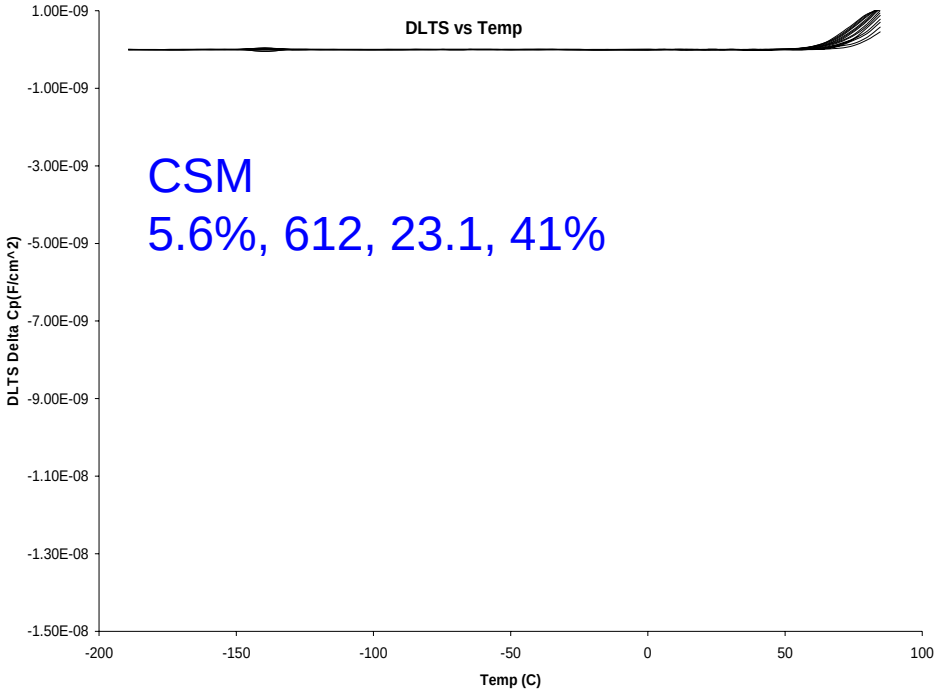

DLTS vs Temp
IEC 11.2%, 786, 23.6, 60%
H5
DLTS Delta Cp(F/cm^2)
Temp (C)
Tref=2.2
Tref=4.3
Tref=8.7
Tref=13.0
Tref=19.5
Tref=26.0
Tref=32.5
Tref=43.3
Tref=54.1
Tref=64.9
Tref=86.6
Tref=108.2
Tref=129.8
Tref=162.3

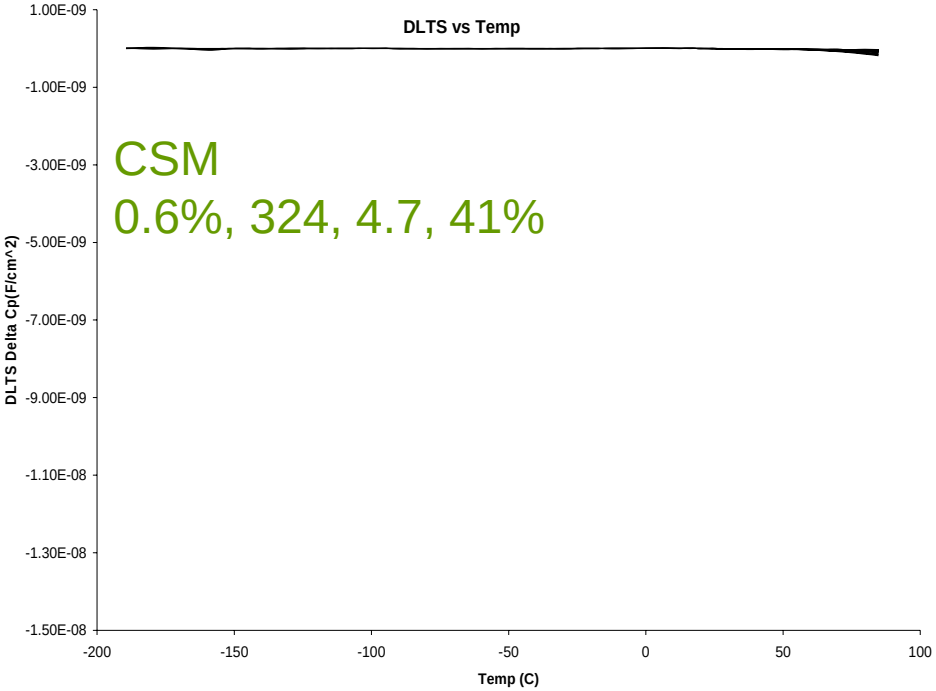

DLTS vs Temp
IEC 8.7%, 709, 22.4, 55%
DLTS Delta Cp(F/cm^2)
Temp (C)
Tref=2.2
Tref=4.3
Tref=8.7
Tref=13.0
Tref=19.5
Tref=26.0
Tref=32.5
Tref=43.3
Tref=54.1
Tref=64.9
Tref=86.6
Tref=108.2
Tref=129.8
Tref=162.3

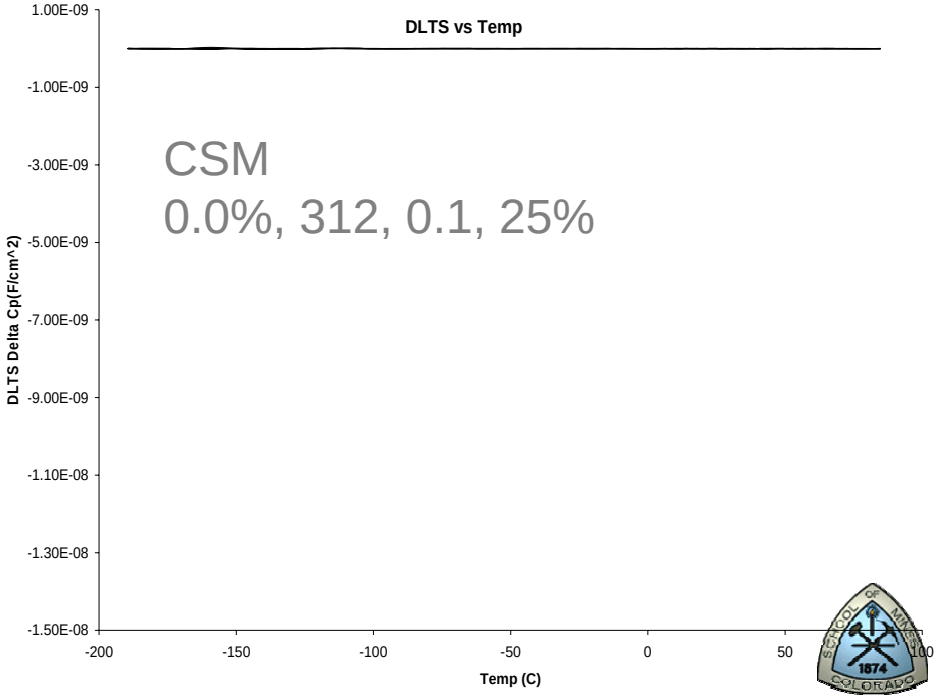

DLTS vs Temp
IEC 2.9%, 583, 10.1, 49%
DLTS Delta Cp(F/cm^2)
Temp (C)
Tref=2.2
Tref=4.3
Tref=8.7
Tref=13.0
Tref=19.5
Tref=26.0
Tref=32.5
Tref=43.3
Tref=54.1
Tref=64.9
Tref=86.6
Tref=108.2
Tref=129.8
Tref=162.3


DLTS vs Temp
IEC 2.1%, 599, 10.0, 35%
DLTS Delta Cp(F/cm^2)
Temp (C)
Tref=2.2
Tref=4.3
Tref=8.7
Tref=13.0
Tref=19.5
Tref=26.0
Tref=32.5
Tref=43.3
Tref=54.1
Tref=64.9
Tref=86.6
Tref=108.2
Tref=129.8
Tref=162.3


DLTS vs Temp
CSM
10.0%, 711, 24.4, 58%
H5
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100


DLTS vs Temp
CSM
5.6%, 612, 23.1, 41%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100


DLTS vs Temp
CSM
0.6%, 324, 4.7, 41%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100


DLTS vs Temp
CSM
0.0%, 312, 0.1, 25%
DLTS Delta Cp(F/cm^2)
Temp (C)
1.00E-09
-1.00E-09
-3.00E-09
-5.00E-09
-7.00E-09
-9.00E-09
-1.10E-08
-1.30E-08
-1.50E-08
-200
-150
-100
-50
0
50
100

Materials Science Perspective

Process

Cell Growers

TCO
CdS
CdTe
CSS
VTD
$CdCl_2$
Cu
Back Contact
…

relationships

Structure

Theorists

Hetero-junction
MIS
Band Diagrams
Doping
Defects
Transport
…

Properties

Experimentalists

J-V
QE
C-V
PL/EL
AS
CTr
EBIC
TRPL
SEM
AFM
Auger
NSOM
…

Performance

Engineers

η
V_{OC}
J_{SC}
FF
Costs
Scalability
Stability
…

PL Studies of CdTe Films and Junctions

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Clean Energy Research Center
Department of Electrical Engineering
University of South Florida, Tampa, FL 33620
*Moldova State University

Moldovan Research and Development Association & CRDF

Work performed under NREL Sponsorship

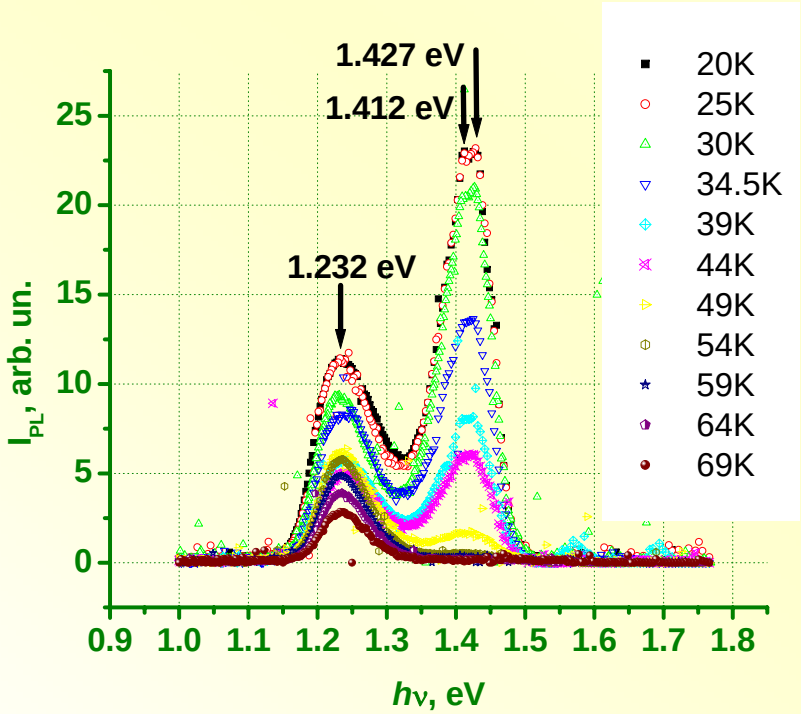
OUTLINE

(Work in Progress !)

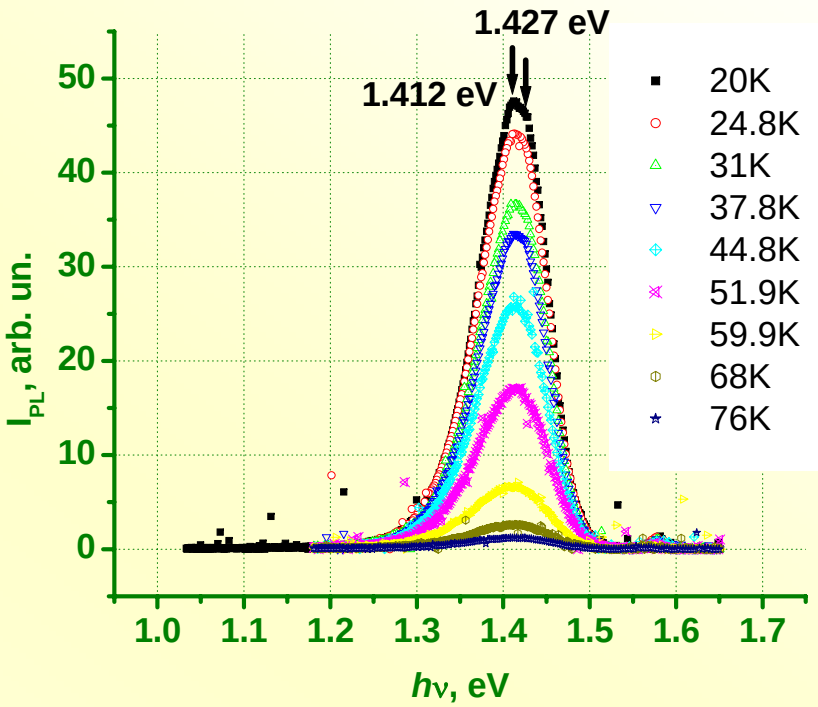
- **Processing**
  - As-deposited (AD)
  - $CdCl_2$ HT
  - $CdCl_2$ HT + Cu (deposited onto CdTe and diffused @ 250C)
  - CBD CdS (baseline devices)
  - CSS CdS (+Cu; CuCl "dip"; CdS-CuCl)
  - CdTe in O_2 or inert ambient (CSS); t=5-8 μm
  - Completed Devices (mapping)
- **Measurements**
  - Ar ion Laser (488 nm Line)
  - Intensity 50 mW (0.5 – 50 mW); spot size approx. 0.5 mm
  - T: 15 - 100 K (Closed loop He Cryostat)
  - Ge detector
  - Spectrometer 0.5 m (SPEX 500)

T-dependence of PL for CdTe

As-deposited



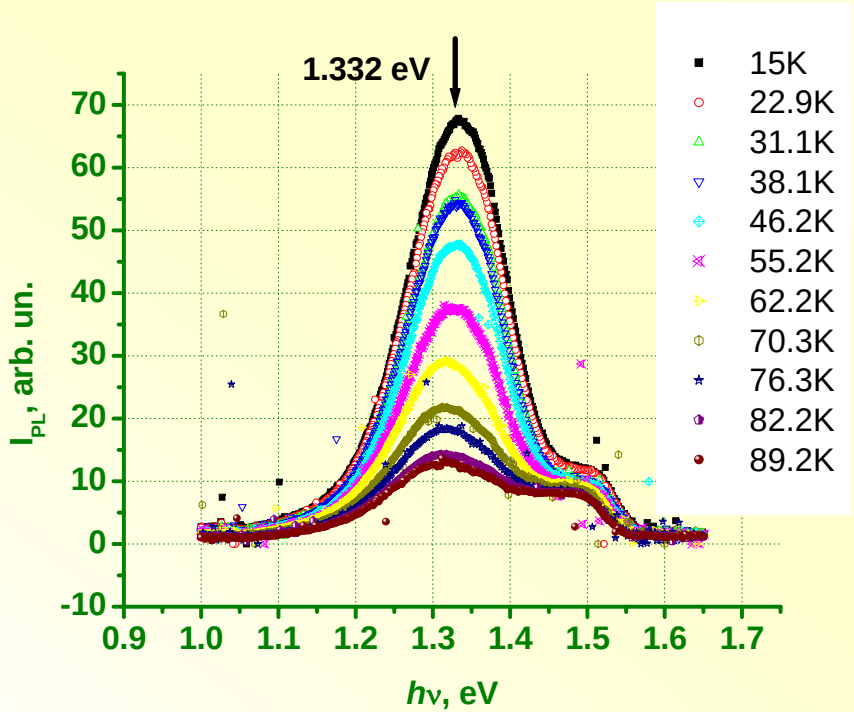
$CdCl_2$-Heat-treated



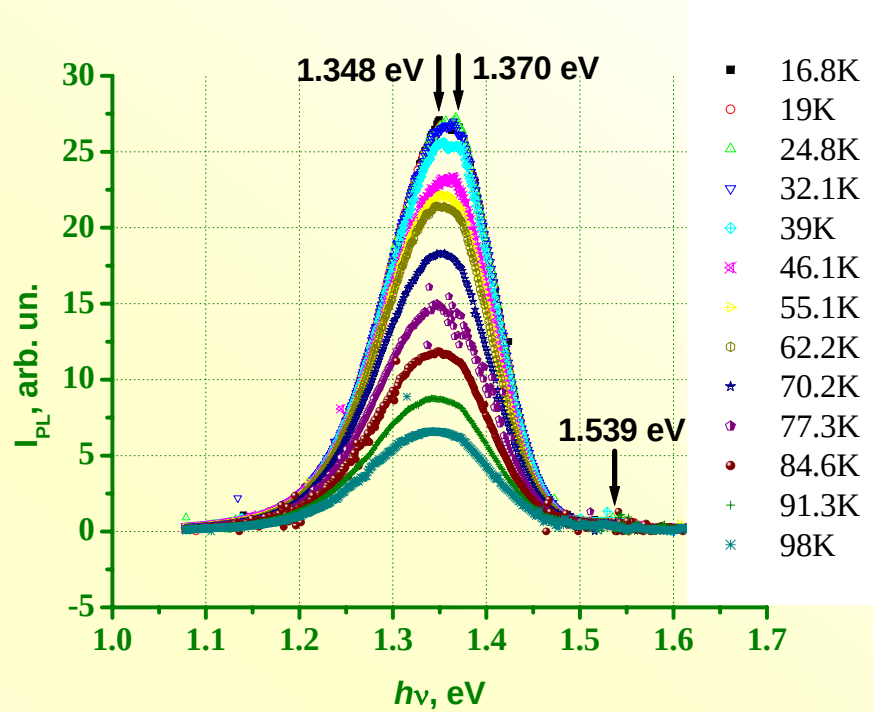
- 1.232 eV band: origin unknown at this time
- 1.427 eV band (potentially 2 bands or phonon replica); band to defect transition; Cd vacancy (spec.); O_2
- $CdCl_2$ heat treatment leads to "passivation" of 1.232 eV related defect
- Activation energies in 20-50 meV range (preliminary calculations)

T-dependence of PL for CdTe/CdS(CBD)

As-deposited

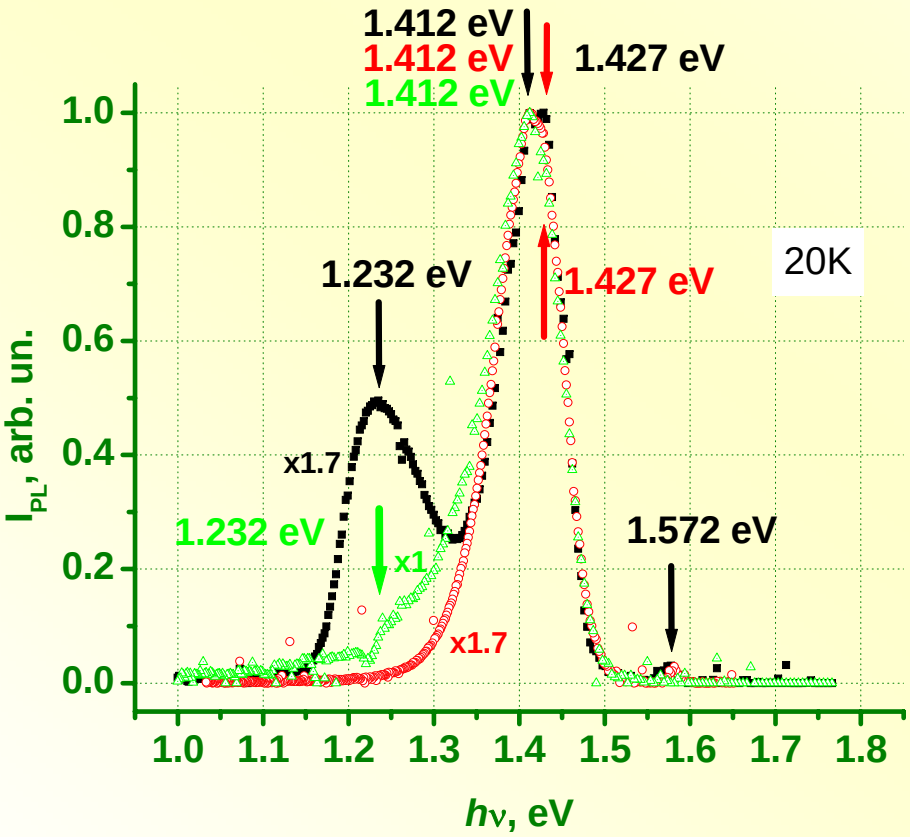


$CdCl_2$-Heat-treated (Cu-diffused)



- 1.511 and 1.332 eV bands in as-deposited
- 1.511 eV band not present in $CdCl_2$ HT sample; a new weaker 1.539 eV band appears
- Annealed samples w and w/o Cu "similar"

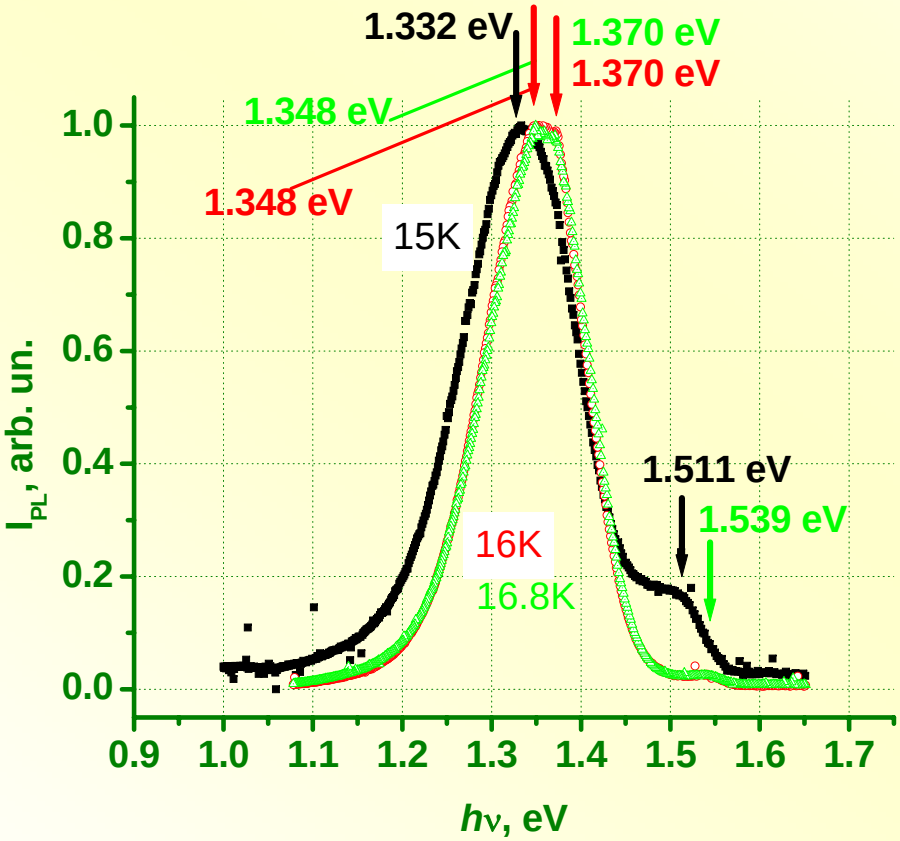
CdTe PL
AD vs. $CdCl_2$ HT vs. $CdCl_2$ HT w Cu



- AD
- $CdCl_2$ HT
- $CdCl_2$ HT + Cu

- 1.232 eV band "annealed out"
- Cu diffusion introduces a band at same energy (?)
- Excitonic band in as-deposited sample

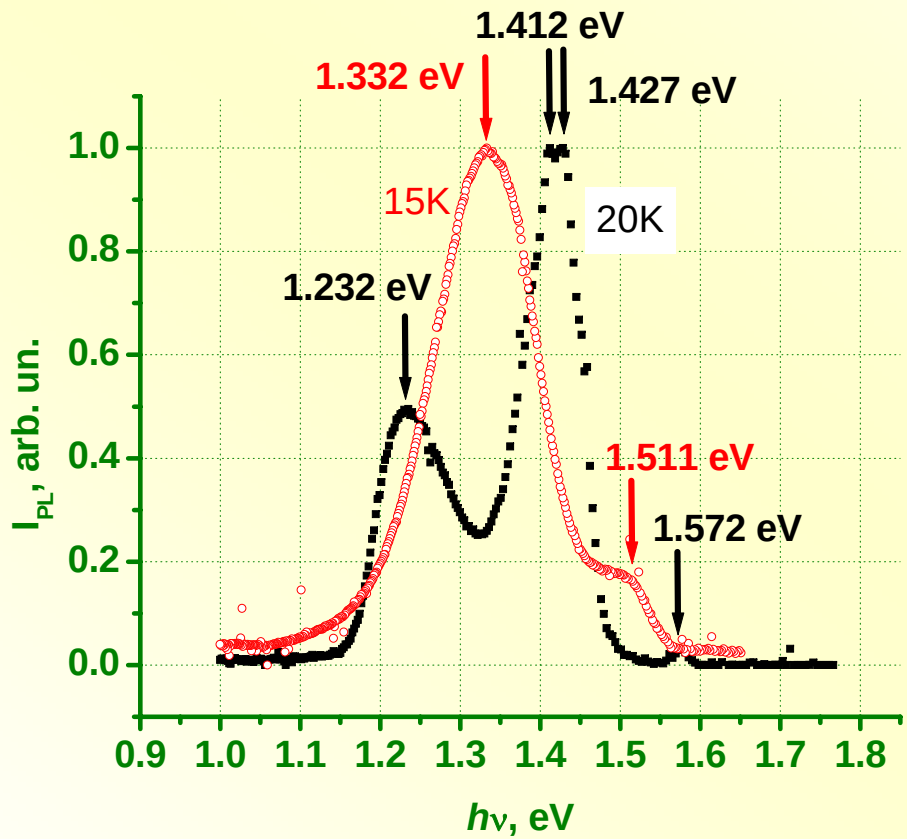
CdTe/CdS(CBD)
AD vs. $CdCl_2$ HT vs. $CdCl_2$ HT w Cu



- AD
- $CdCl_2$ HT
- $CdCl_2$ HT + Cu

- Shift in 1.332 eV band after $CdCl_2$ HT
- 1.511 eV band "annealed out" after HT
- 1.539 band appears with Cu

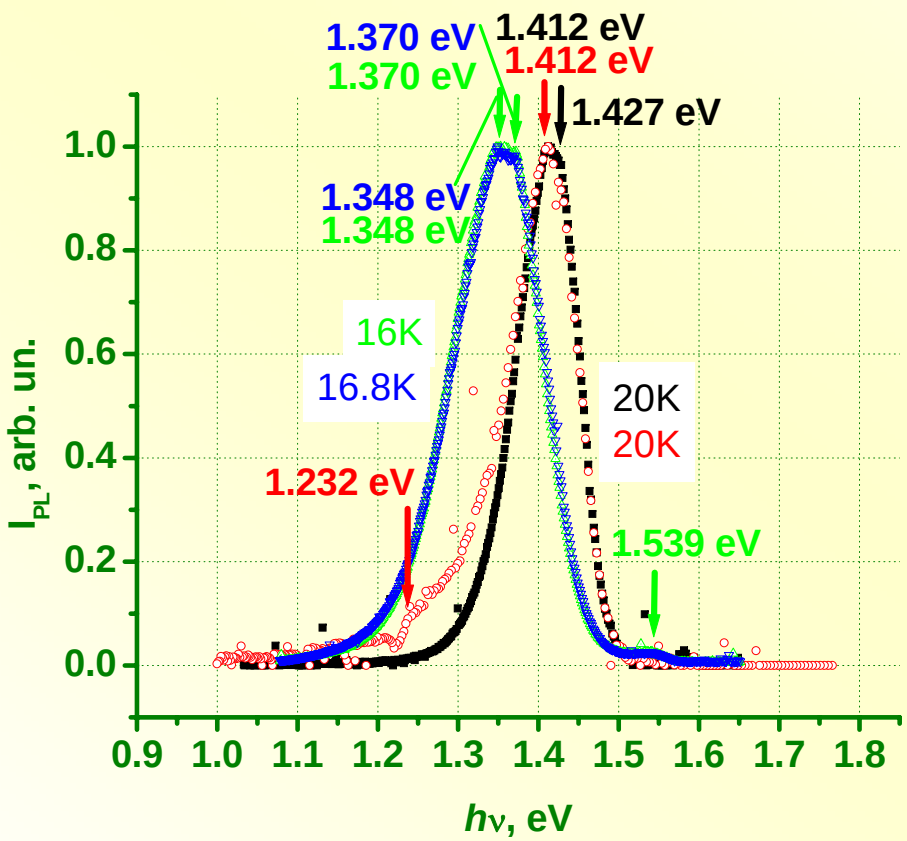
As-deposited CdTe vs. CdTe/CdS(CBD)



- CdTe
- CdTe/CdS(CBD)

- Distinctly different spectra due to CdSTe formation at interface

CdTe & CdTe/CdS $CdCl_2$ HT w & w/o Cu



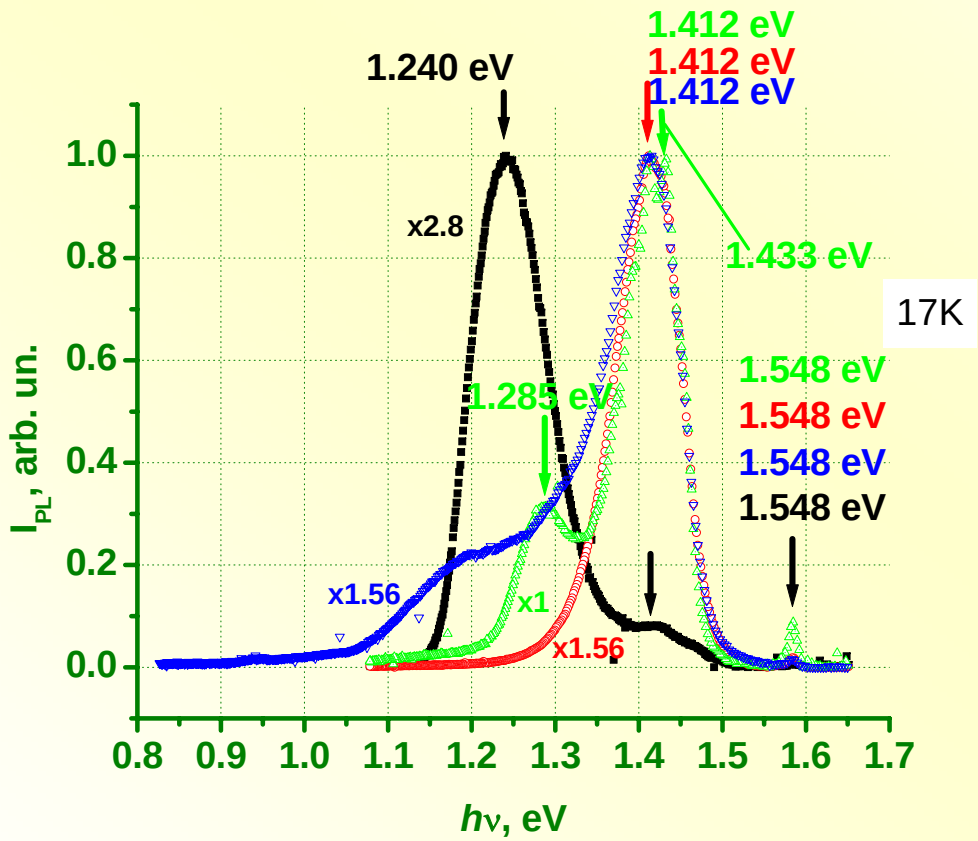
- CdTe $CdCl_2$ HT
- CdTe + $CdCl_2$ HT + Cu
- CdTe/CdS + $CdCl_2$ HT
- CdTe/CdS + $CdCl_2$ HT + Cu

- PL intensity from CdTe/CdS Interface 4x

SUMMARY Table (CdS-CBD)

BAND [eV]	CdTe AD	CdTe + $CdCl_2$	CdTe + $CdCl_2$ + Cu	CdTe/CdS AD	CdTe/CdS + $CdCl_2$	CdTe/CdS + $CdCl_2$ + Cu
1.232	X		X			
1.332				X		
1.348					X	X
1.370					X	X
1.412	X	X	X			
1.427	X	X				
1.511				X		
1.539						X
1.572	X					

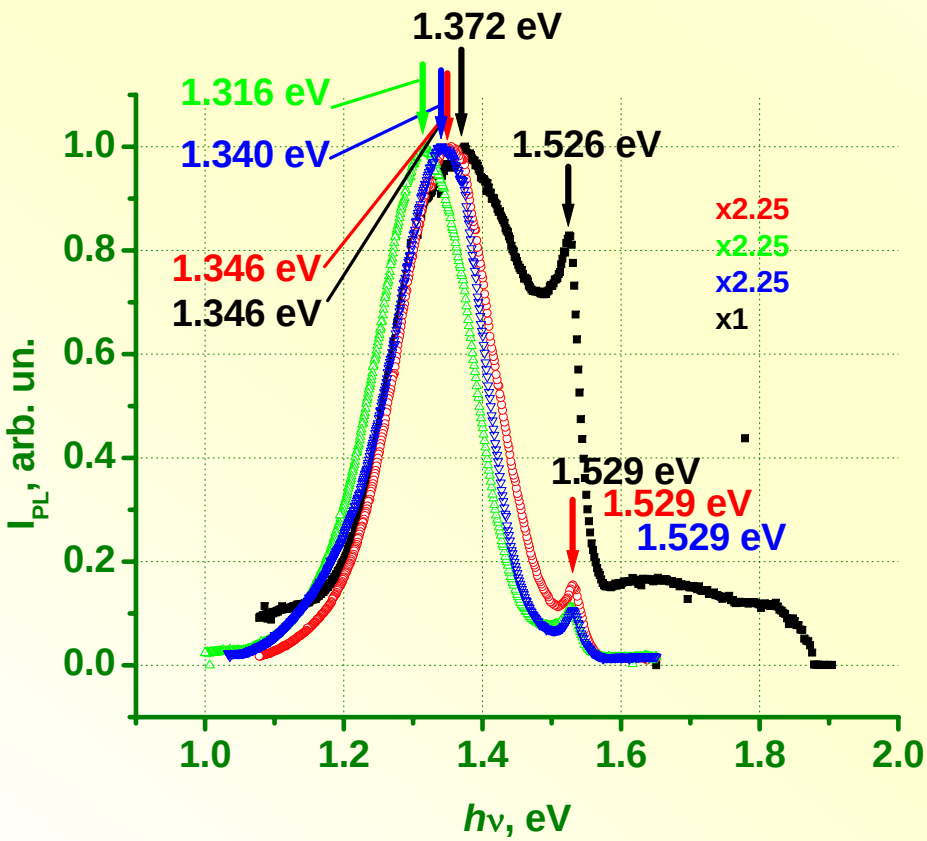
CdTe PL (CdS by CSS)
AD vs. $CdCl_2$ HT vs. CdS-CuCl



- CdTe AD (CdS NO CuCl)
- $CdCl_2$ HT (CdS NO CuCl)
- CdTe AD + CdS(CuCl-treated)
- CdTe $CdCl_2$ HT + CdS (CuCl-treated)

- 1.412 eV present in all samples (Cd-vacancy (?))
- 1.548 eV present in all samples – need to verify origin of this

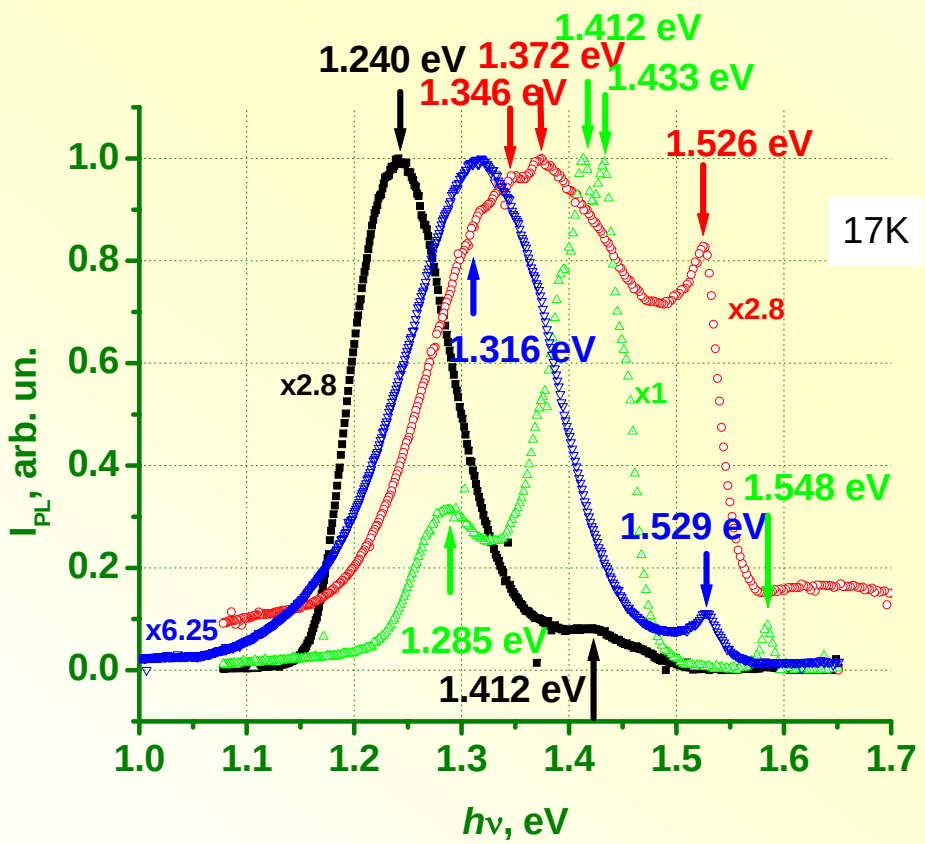
CdTe/CdS(CSS) PL
AD vs. $CdCl_2$ HT vs. CdS w and w/o CuCl



- AD (CdS NO CuCl)
- $CdCl_2$ HT (CdS NO CuCl)
- AD + CdS-CuCl
- $CdCl_2$ HT + CdS-CuCl

- All spectra seem to have the same two bands
- The various treatments lead to small shifts in energy and large intensity variations
- CdS PL also present

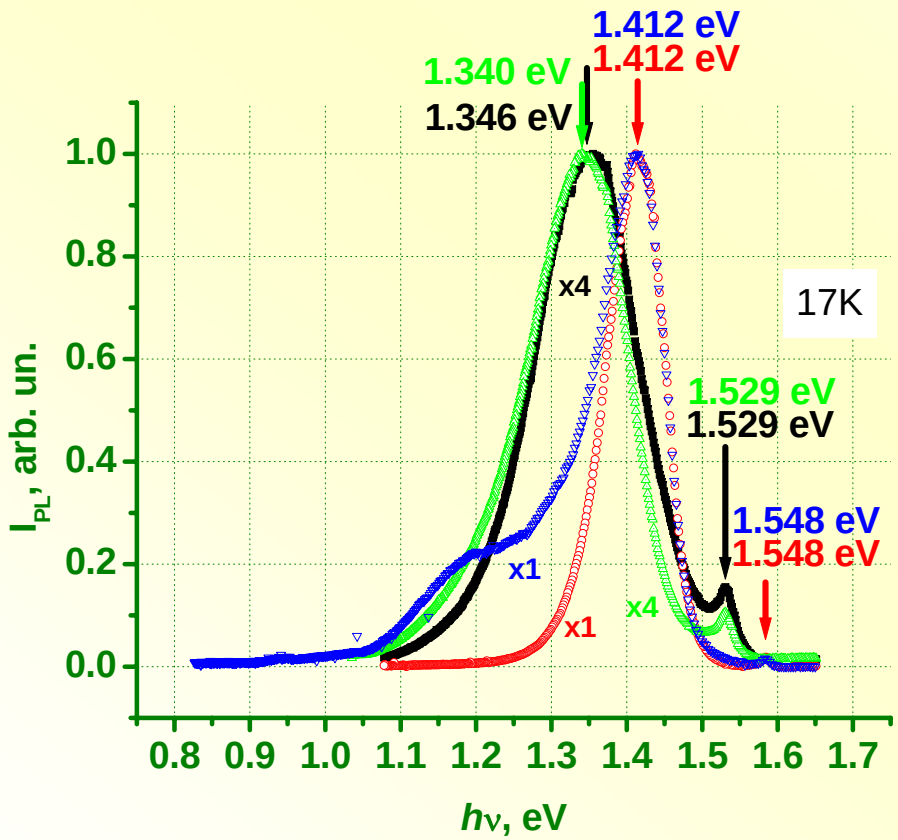
AD CdTe vs. CdTe/CdS
(w and w/o CuCl)



- CdTe AD NO CuCl
- CdTe/CdS AD NO CuCl
- CdTe AD + CdS-CuCl
- CdTe/CdS AD + CdS-CuCl

- No "new" PL bands – change in intensity

$CdCl_2$ HT
CdTe vs. CdTe/CdS(w and w/o CuCl)



- CdTe/CdS $CdCl_2$ HT NO CuCl
- CdTe $CdCl_2$ HT NO CuCl
- CdTe/CdS $CdCl_2$ HT + CdS-CuCl
- CdTe $CdCl_2$ HT + CdS-CuCl

SUMMARY Table CdTe PL (CdS-CSS)

BAND [eV]	CdTe AD	CdTe + $CdCl_2$	CdTe AD + CdS-CuCl	CdTe + $CdCl_2$ + CdS-CuCl
1.240	X			
1.285			X	
1.412	X	X	X	X
1.433			X	
1.548	X	X	X	X

SUMMARY Table CdTe/CdS PL (CdS-CSS)

BAND [eV]	CdTe/CdS AD	CdTe/CdS + $CdCl_2$	CdTe/CdS AD + CdS-CuCl	CdTe/CdS + $CdCl_2$ + CdS-CuCl
1.316			X	
1.340				X
1.346	X	X		
1.372	X			
1.526	X			
1.529		X	X	X

SUMMARY

PL signature from the interface due to CdSTe – 1,332 and 1.511 eV

Elimination of 1.232 eV band from CdTe as a result of the $CdCl_2$ HT

Cu diffusion in CdTe leads to the appearance of a band @ 1.232

CuCl treatment of CdS leads to significant change in PL intensities, in addition to the formation of new PL bands in CdTe spectra

WIP:

- Intensity dependence (@ all T) data being analyzed
- PL of CdS with and w/o Cu
- CdTe in inert ambient + HT + Cu etc.
- CdTe on TCO

Linking Defects Seen in PL to Device Performance

Caroline Corwine and Jim Sites (CSU)
Tim Gessert (NREL)

Collaborators: Wyatt Metzger, Sam Demtsu, Dave Albin, Pat Dippo, Jingbo Li, Su-Huai Wei, Manuel Romero, Glenn Teeter, Craig Perkins, Sally Asher, Anna Duda (NREL)

Colorado State University

March 9, 2006

NREL

Limitations in Device Performance

Parameters	Record Cell	Ideal Cell
J_{SC} [mA/cm^2]	25.9	30.5
V_{OC} [mV]	847	1070
FF	75.0	89.2
η [%]	**16.5**	**29.2**

Losses in J_{sc} understood

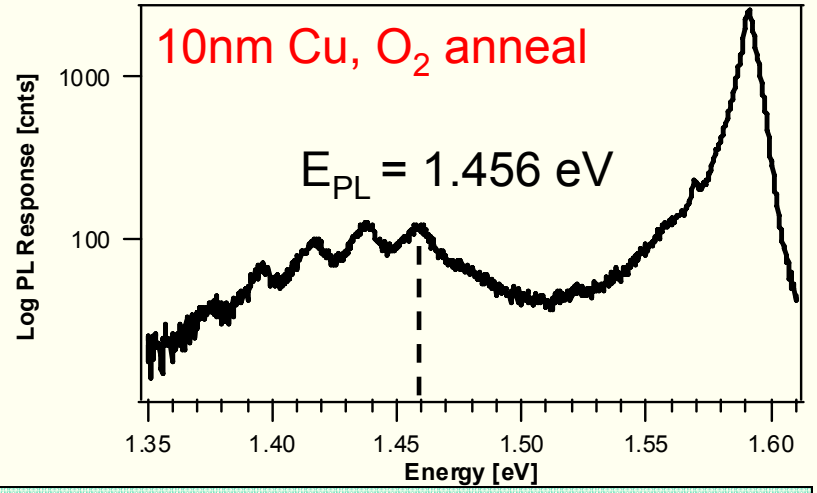
Possible causes of V_{oc}, FF limitations:

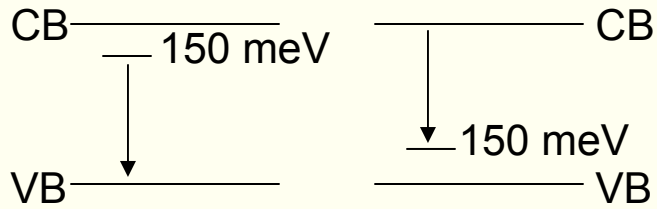
- Presence of deep-level defects
- Formation of compensating donors

Defect Studies with PL

The Challenge in Interpreting PL

Single-crystal CdTe





Look the same in PL

Possible Interpretation:

- Copper-oxygen D-center, Cu_i-O_{Te}
- Calc. energy → $E = E_c - 0.125$ eV

Donor

Another Suggested Interpretation:

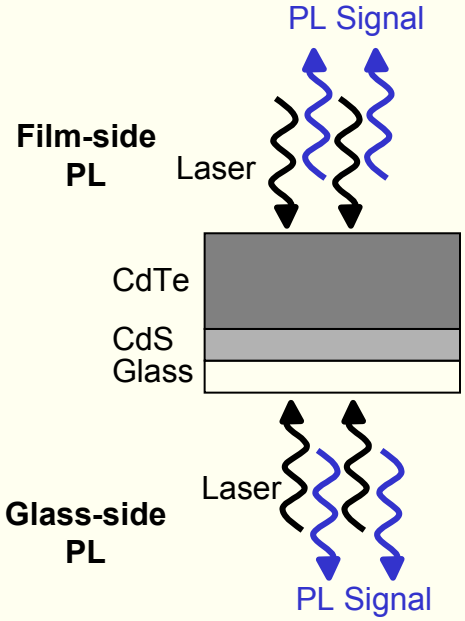
- Chlorine A-center, V_{Cd}-Cl_{Te}
- Calc. energy → $E = E_v + 0.140$ eV

Acceptor

C.R. Corwine *et al*, "CdTe photoluminescence: comparison of solar-cell material with surface-modified single crystals," App. Phys. Lett. **86** (2005) p. 221909.

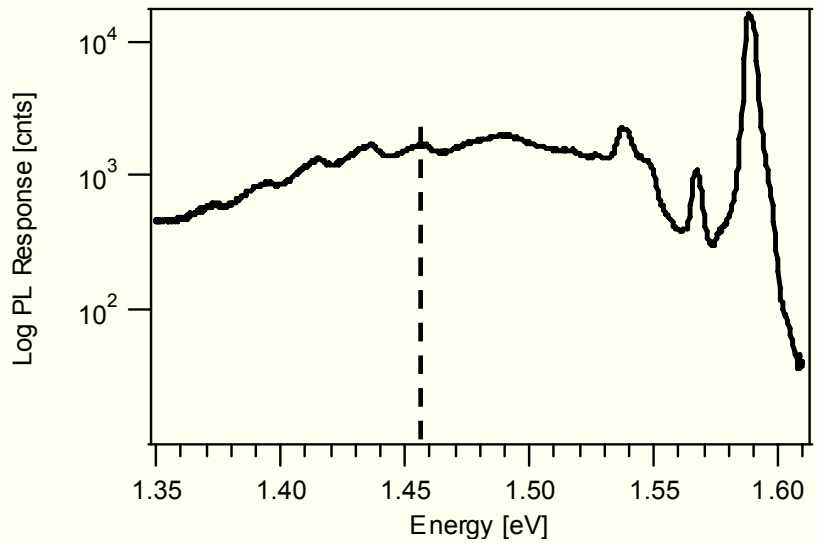
Samples Examined with PL

- As deposited
  - Intentional O
  - Cu impurities in CdTe source
- $CdCl_2$-treated
  - Intentional Cl and O_2
  - Cu impurities in $CdCl_2$ source
- Contacted Devices as a function of Cu
  - ZnTe contact
    - Industrial VTD, CSU CSS
  - Evaporated
    - NREL CSS



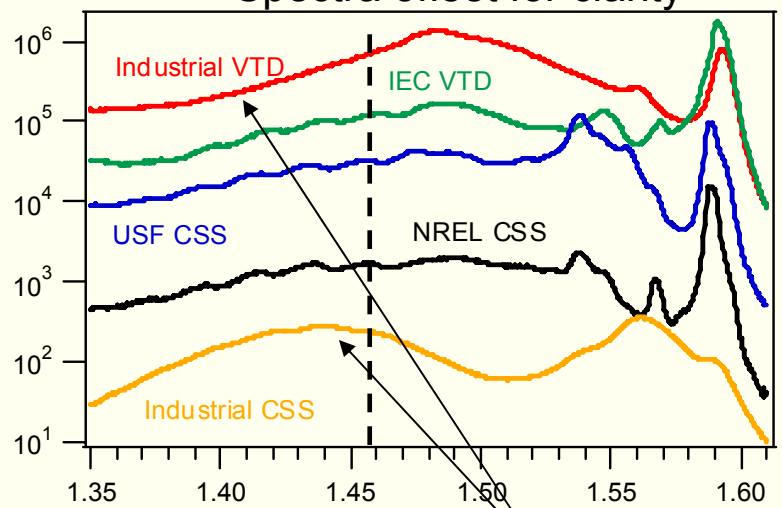
As Deposited CdTe

NREL only, Film-side PL, 4.25 K



All Materials, Film-side PL, 4.25 K*

*Spectra offset for clarity

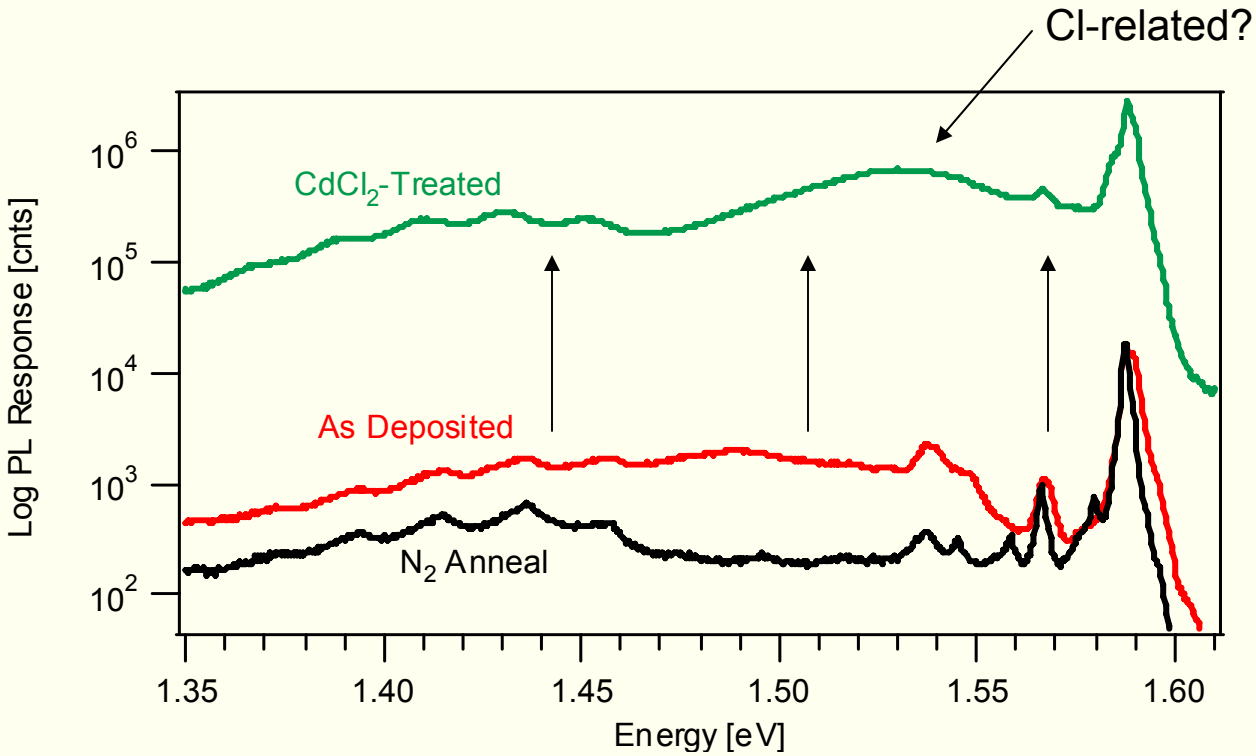


Phonon replicas seen on enhanced scale

- 1.456-eV peak forms during deposition
- Present in all Samples

$CdCl_2$-treated CdTe

NREL CSS Material

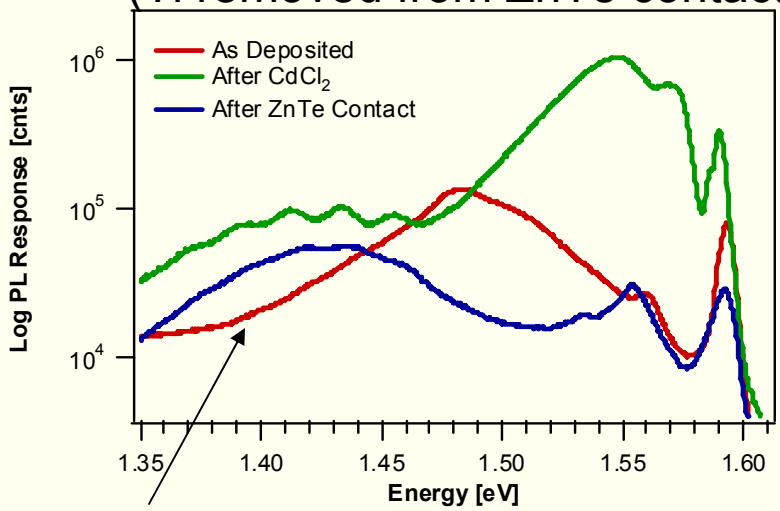


- $CdCl_2$ treatment at 400°C increases overall PL intensity
- N_2 anneal at 400°C decreases PL intensity

PL Throughout Processing

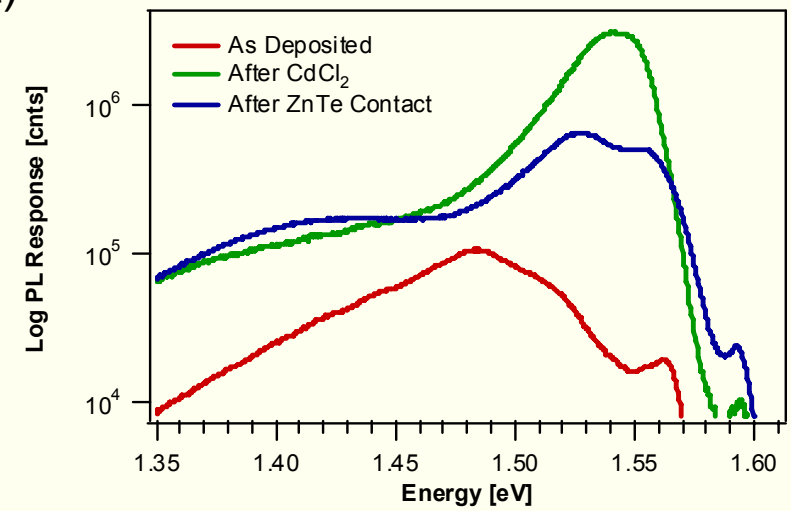
Industrial VTD Material

Film-side PL
(Ti removed from ZnTe contact)



Phonon replicas seen on enhanced scale

Glass-side PL

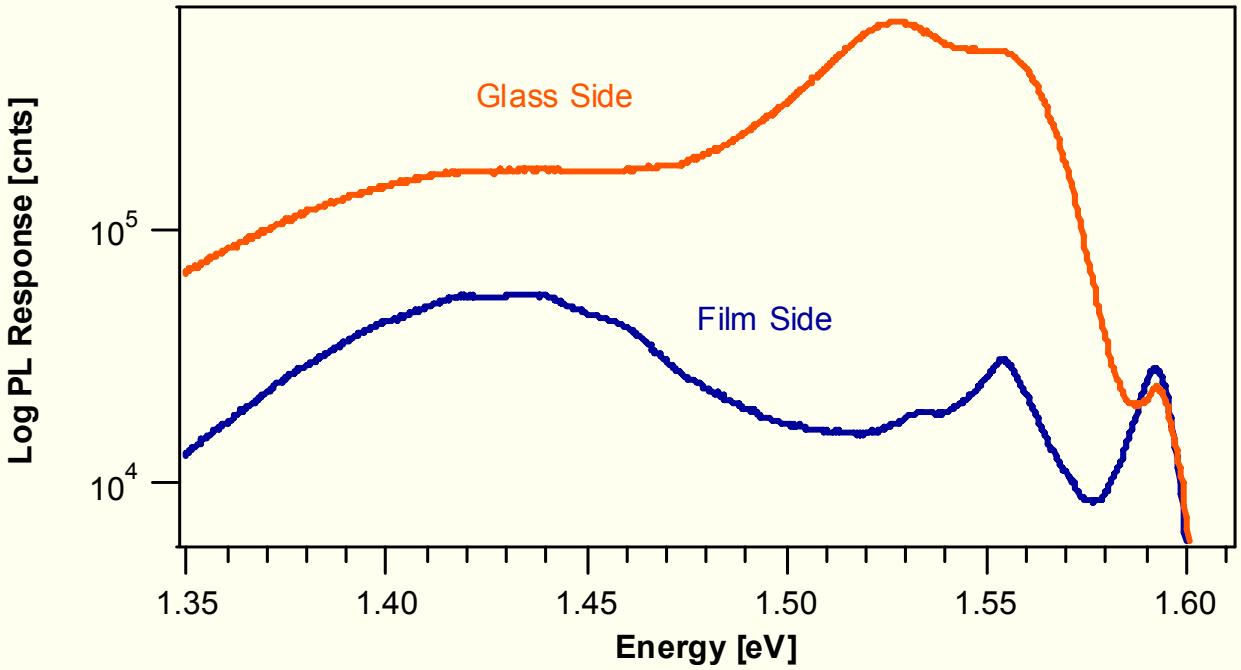


- 1.456-eV peak always seen from film side
- From glass side: Peak in same region appears after contacting*

*For samples with thinner CdTe, peak appears after deposition

Film vs. Glass-side PL After Contact

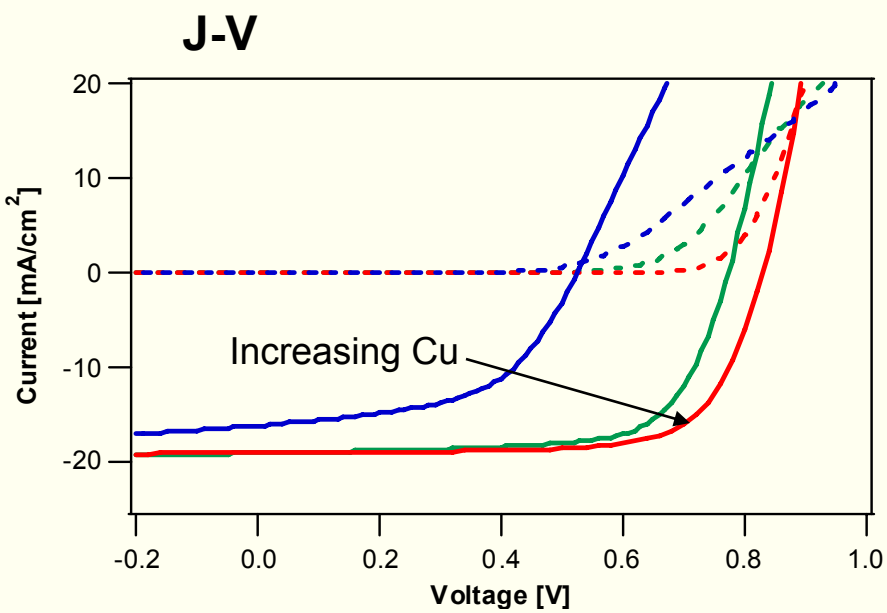
Industrial VTD Material

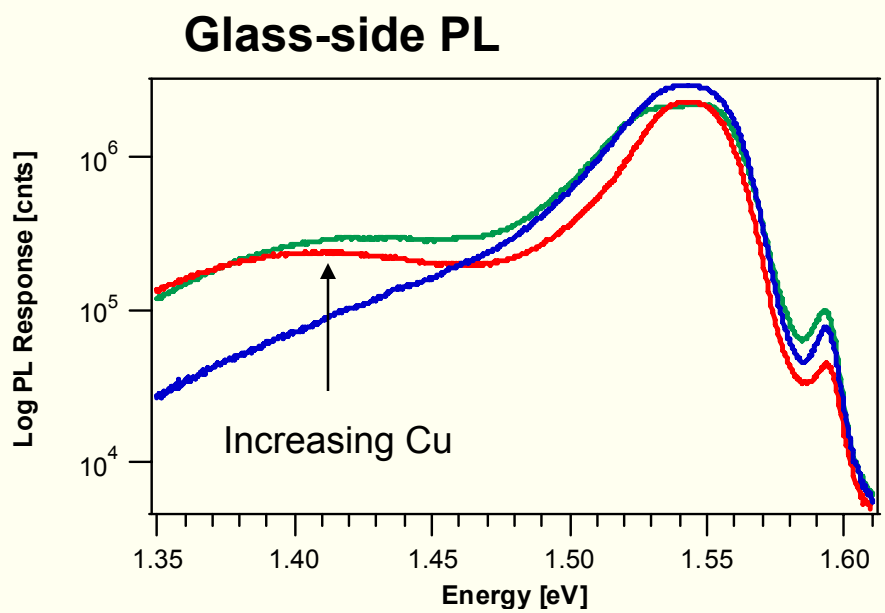


- Peak seen from glass side likely the same as that seen from the film side
- No distinct phonon replicas from glass side

J-V versus PL (Industrial VTD Devices, 4µm)

ZnTe Contact

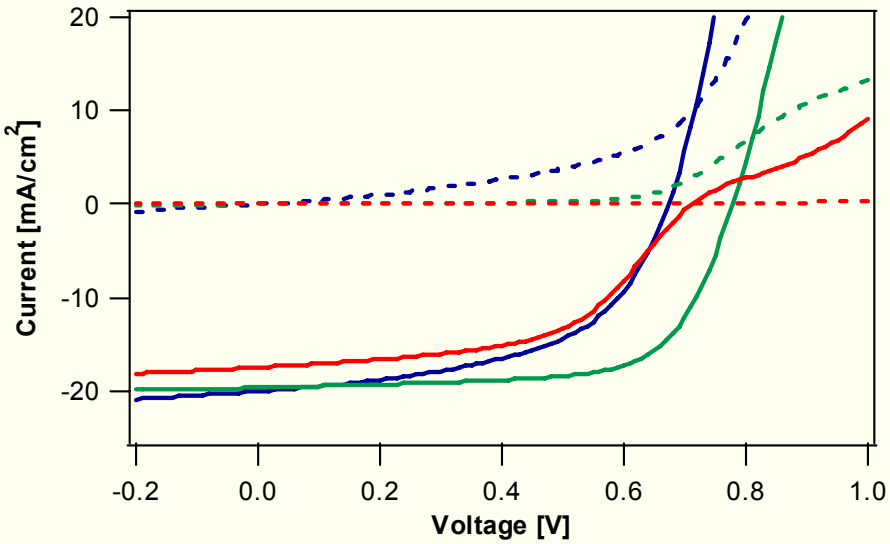


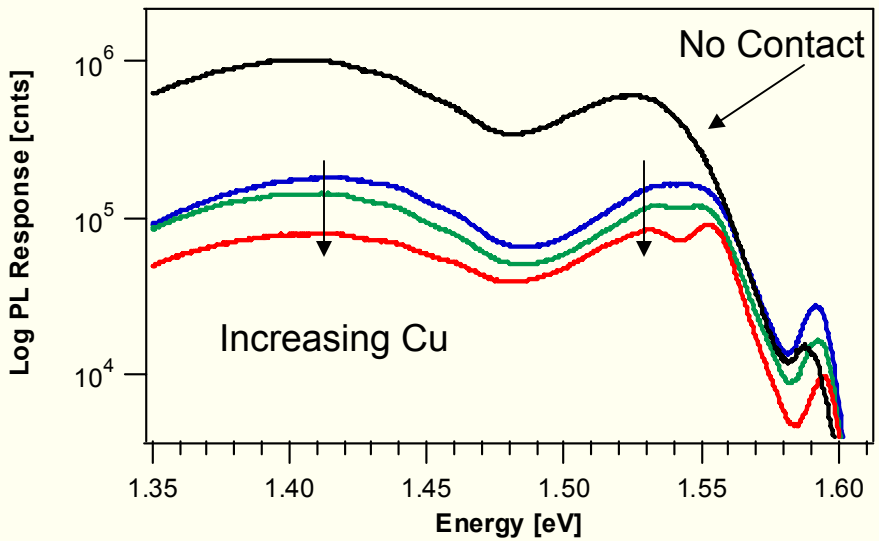


- Broad peak (1.456 eV?) is evident in good devices
- Good devices contain more Cu

J-V versus PL (Industrial CSS Devices, 2 µm)

ZnTe Contact

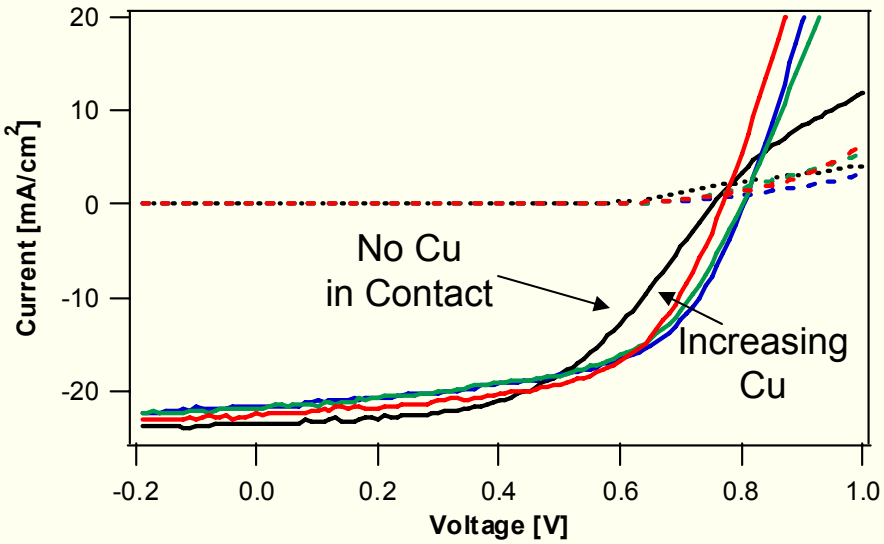


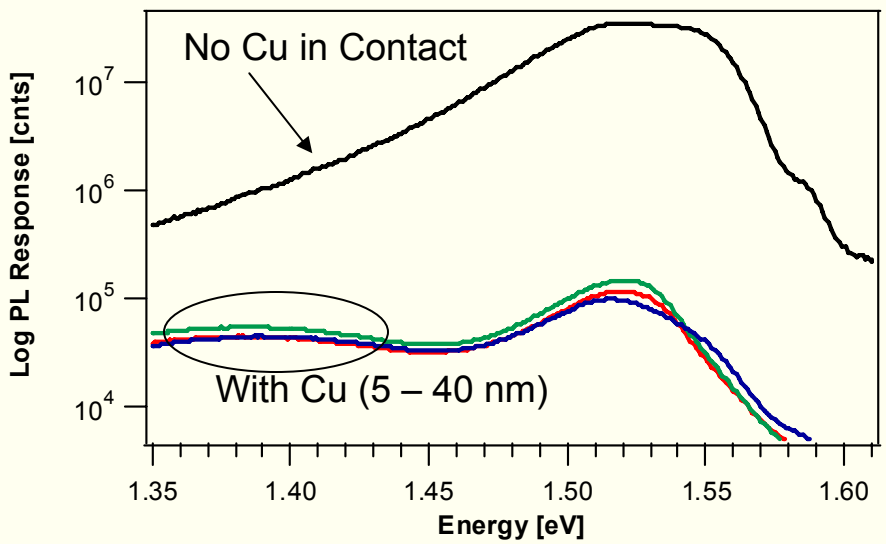


- Optimum Cu different than for 4 µm device
- Relative intensity of 1.456-eV peak does not change with Cu
- Overall PL decreases with increasing Cu, consistent with increase in junction field

J-V versus PL (NREL CSS Devices, 8 µm)

Evaporated Contact





- With Cu, overall PL decreases (increase in junction field)
- 1.456-eV peak appears when Cu is introduced
- Adding more Cu does not enhance the 1.456-eV peak

Summary

- Evidence of a compensating donor in CdTe (Cu_i-O_{Te})
- Link to device performance may depend on CdTe thickness
  - Thick Devices (8 μm):
    - After deposition: Film side only
    - After Contact (with Cu): Seen from glass side
  - Medium Thickness Devices (4 μm):
    - After deposition: Film side only
    - After contact: Seen from glass side
    - Correlates to increase in FF and V_{oc} in J-V
  - Thin Devices (2 μm):
    - After deposition: glass and film side
    - After contact: no change in 1.456-eV peak, but overall PL decreases
    - Optimum amount of Cu different than for thicker devices

Conclusions

- Cu_i-O_{Te} formation seems important to attain good devices
  - May be replacing mid-gap V_{Te} ($E = E_c - 0.750$ eV)
- Presence of a compensating donor may limit attainable V_{oc} and FF

Preferable Scenario:

- Find a better way to replace V_{Te}
  - Possibly Sb_{Te} or Cl_{Te}-V_{Cd}
  - Both are acceptors, and would not directly limit V_{oc} and FF
- BUT it would require development of new process space (perhaps incorporating Sb or Cl during growth)

Observations of Cu Diffusion in CdTe PV Devices

R. A. Enzenroth, K.L. Barth, and W.S. Sampath

National CdTe R&D Team Meeting
March 9 – 10, 2006 NREL

Colorado State University
Knowledge to Go Places

Materials Engineering Laboratory

Presentation Outline

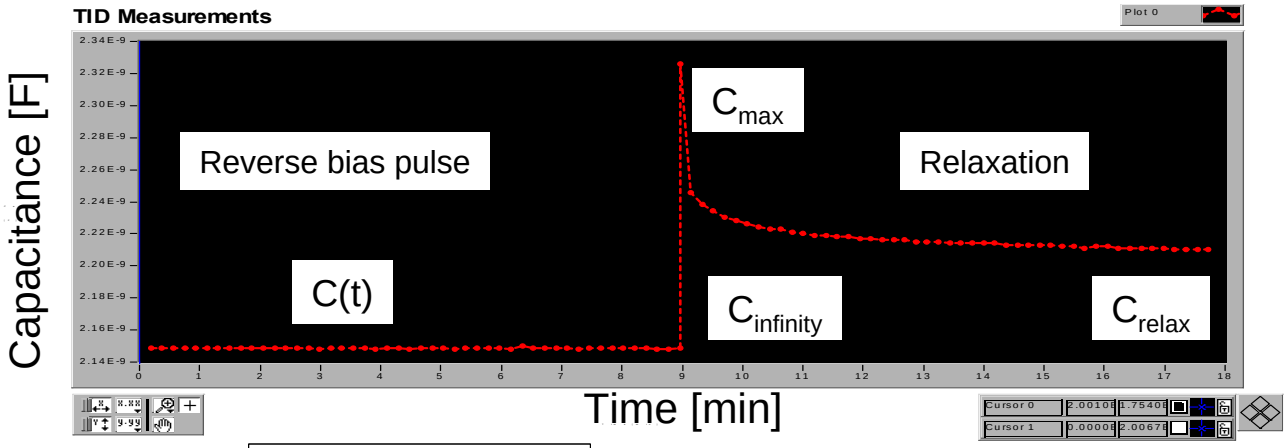
- GB diffusion not considered in this presentation
- Some agreement in the literature that there are two dominant Cu diffusion mechanisms in CdTe

1. Interstitial Cu diffusion:
   - Introduction to Transient Ion Drift (TID) method
   - Forward bias stress results
2. (Cu Impurity Interstitial – Cd Vacancy) pair diffusion:
   - (X_i - V) pair background from the literature
   - Thermal Admittance Spectroscopy (TAS)
   - Accelerated light soak stress results

- Discussion of Cu diffusion pathways and estimates of magnitude of energy barriers
- Summary and Conclusions

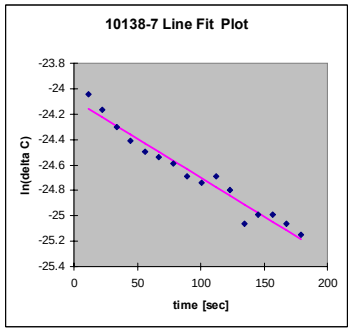
Transient Ion Drift (TID)

- **Well known technique used in measurement of ion diffusion in single crystal Si, CIGS and CdTe [1 - 4,14]**
- **Measure capacitance as reverse bias pulse is applied and removed**



Diffusion coefficient

$$\tau = \frac{k \cdot T \cdot \varepsilon_o \cdot \varepsilon}{q^2 \cdot D \cdot N_a}$$



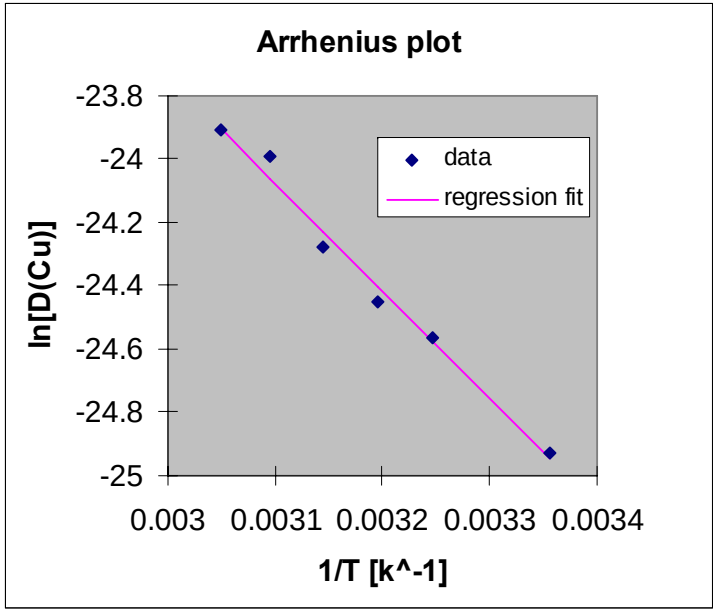
$$\Delta C(t) = Cinf - C(t) = \Delta Co \cdot \exp\left(-\frac{t}{\tau}\right)$$

Ion Density

$$N_{ion} = \frac{2 \cdot \left(C_{max} - C_{relax}\right)}{C_{infinity}} \cdot N_a$$

Mobile ion of interest is interstitial donor Cu_i^+

Preliminary Result
Diffusion Coefficient for Cu_i^+ in CdTe

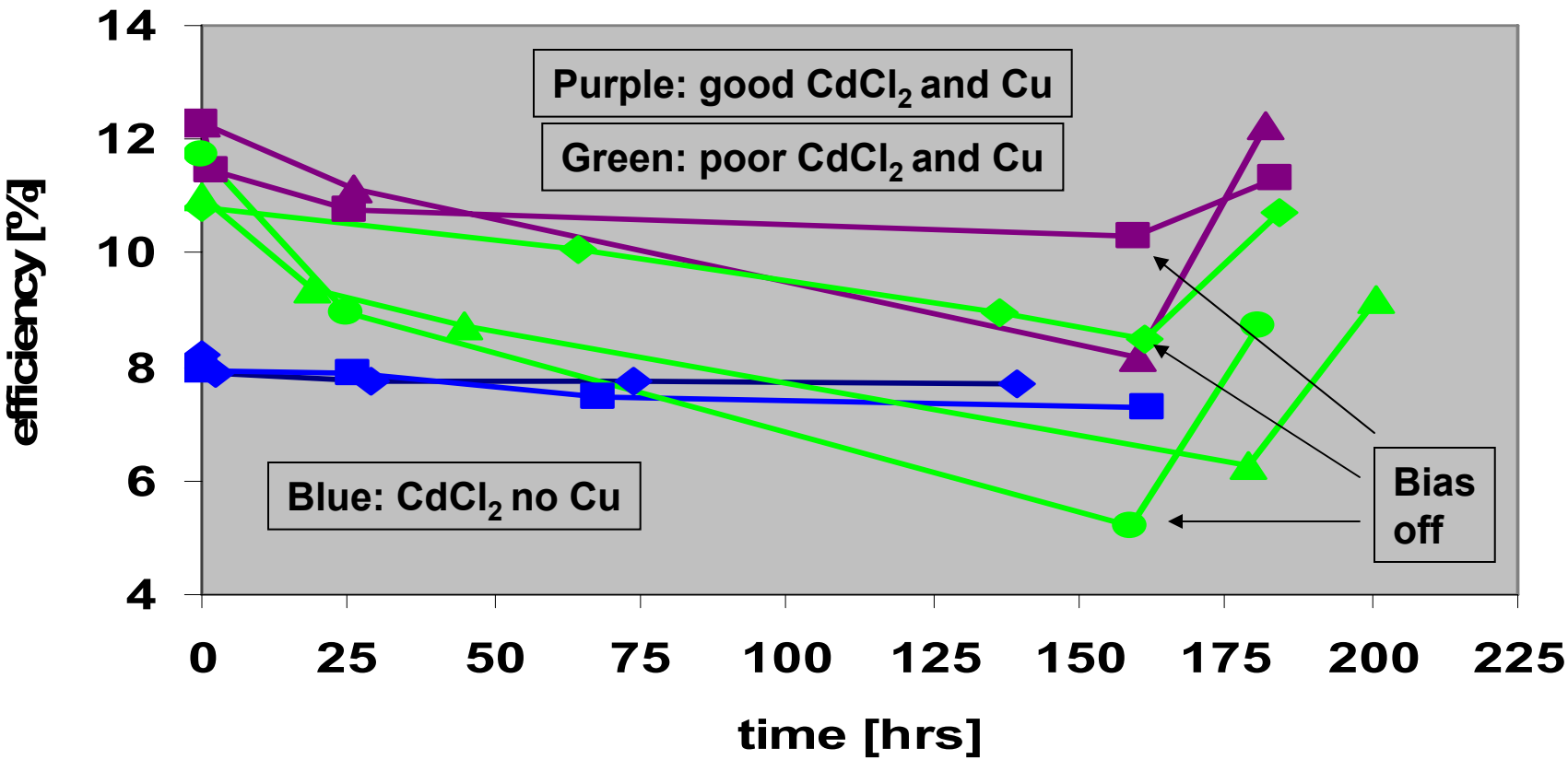


- **Effective coefficient:** $D(Cu_i) = 1.3E\text{-}6 \times \exp[-0.29\ eV/(KB*T)]$
  25° C to 55° C
- **B. O. Wartlick et al. [13]:** $D(Cu_i) = 1.7E\text{-}6 \times \exp[-0.24\ eV/(KB*T)]$
  about -13° C to 50° C
- $E_a = E_{bind} + E_{bI}$ [14] **where** E_{bI} **is the energy barrier to interstitial migration**
  - **The binding energy due to pairing with acceptors has not been quantified but seems to be small compared to theory [5] for temps 25° C to 55° C**

Forward bias performance

- Changes to the depletion width easily move Cu ions
- Any changes related to Cu ions must include periods of forward bias

- **Forward bias (VDC >Voc) applied at room temperature for ~ 160 hrs then removed**



Tabular Forward Bias Data

forward bias cells cell	type	delta eff end bias [%]	delta eff recover [%]	similarly processed cells TID Ncui [cm^-3]
6551-6	good CdCl2 and Cu	-16	-8	3.0E+13
7236-6	good CdCl2 and Cu	-34	0	1.6E+13
8734-6	poor CdCl2 and Cu	-21	-1	3.5E+13
8234-7	poor CdCl2 and Cu	-43	-16	1.8E+13
8332-9	poor CdCl2 and Cu	-56	-26	xxx
8122-3	no Cu	-6	xxx	xxx
6446-9	no Cu	-8	xxx	xxx

- Certain cells recover to > 90% initial η
  => Cu_i^+ diffusion has no significant effect on some cells
- 4 similarly processed cells had ~ same NCu_i^+
- It is proposed that poor bias performance is related a reaction between less mobile defects and Cu_i

(X_i – V) pair diffusion mechanism

- A (Cu impurity interstitial - Cd vacancy) pair mechanism was proposed by D. Shaw [6] as the pathway for Cu diffusion in CdTe with the surface acting as the source of vacancies [6]. Both Jones [10] and Shaw agree that D(Cu) is independent of $[V_{Cd}]$.
- Migration of (X-V) pair proceeds by 1) vacancy interstitial exchange 2) vacancy moves by ring mechanism. Implies relatively strong bond between impurity and vacancy [7].
- $(Cu_i^{+}\text{-}V_{Cd}^{2-})^{-}$ has been shown in the depletion region of CdTe cells with CL by M. Romero et al. [8] and after Cu diffusion with PL by Grecu and Compaan et al. [9]

If (X-V) pair is the dominant diffusion mechanism then:

- Jones proposes that $D(Cu) = \frac{[(Cui\text{-}VCd]'}{[Cu]} \times D(Cui\text{-}VCd)$ [10]
- What is the stability of CSU cells that have detectable densities of (X-V) pairs?

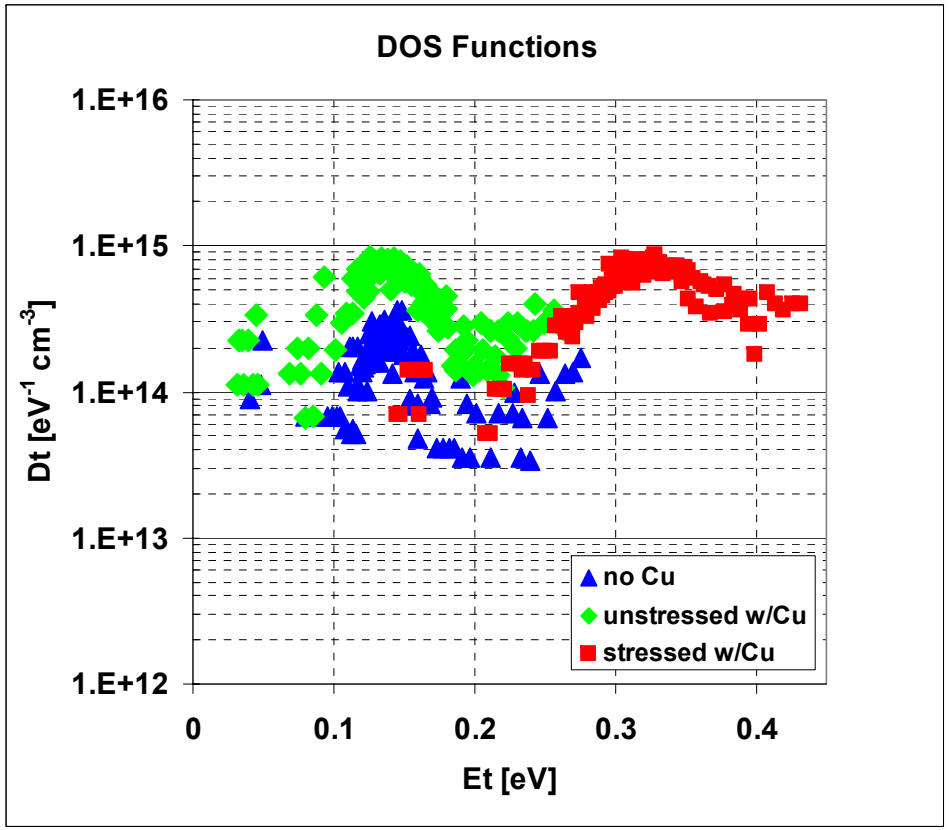
Evolution of DOS with Non Optimum Processing and Stress

Unstressed w/Cu

- Et = 133 ± 7 meV
- Nt ~ 8 x 10^{13} [15]
- Attributed to (X-V) pair

No Cu

- Et = 133 ± 7 meV
- Nt ~ 2 x 10^{13} cm^{-3} [15]
- Attributed to (X-V) pair



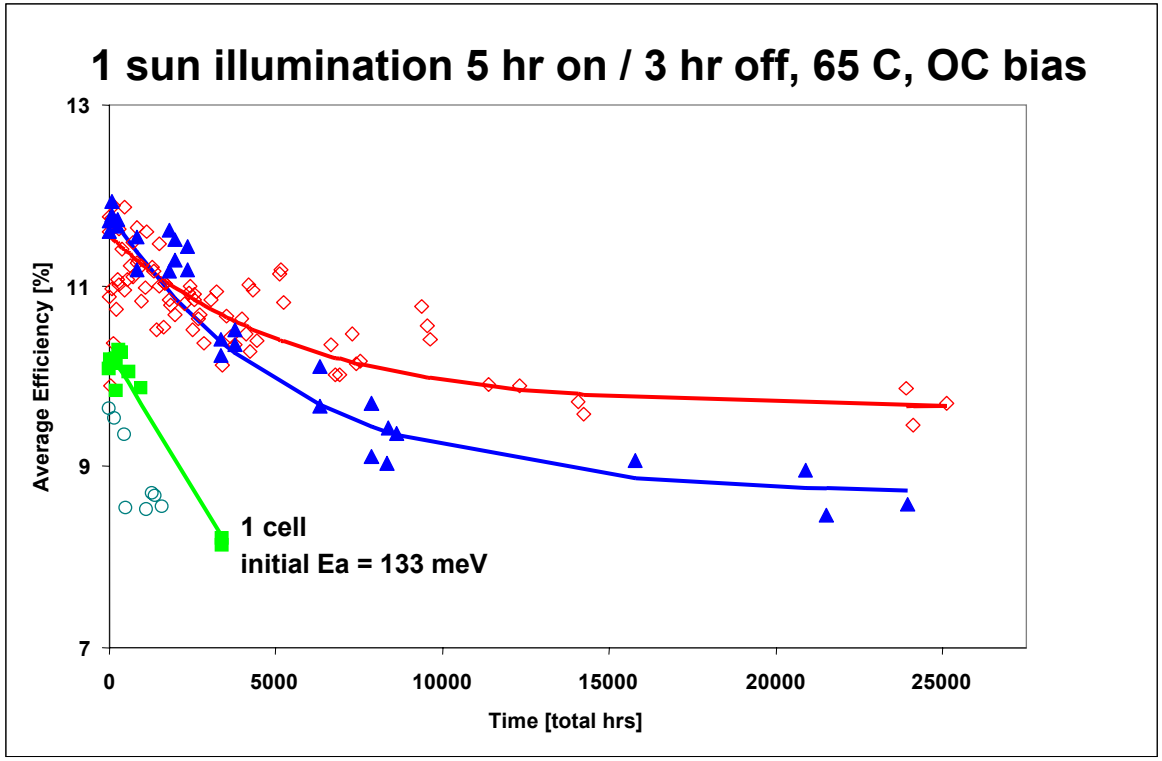
Stressed w/Cu

- Et = 321 meV
- Nt ~ 8 x 10^{13} from
- Attributed to Cu_{Cd}^{-}

- Grecu and Compaan et al. indicate that (X-V) pair has a lifetime ~ 5 days => PL quenches [9]

- DOS estimated by Walter's method from TAS dC/dF spectrum [15]
- Process conditions for run 103 given on appendix slide

Stability of Cells with Different Processing



- (X-V) pair associated with poor stability (green)
- Stable cells (red) have undetectable N_t by TAS

Energy Barrier to Interstitial Diffusion

$$E_a = E_{bI} + E_{bind} \quad [20]$$

Cu_i^+ => interstitial $E_a = 0.24 \sim 0.29$ eV

<u>field effect on migration</u> **[B. O. Wartlick et al. [13] and TID]**

equilibrium concentration of ions present => no formation energy

- E_{bind} (binding energy due to pairing with acceptors) seems to be small in temperature range 25° C to 55° C

Preliminary result: $E_a \sim E_{bI}$

E_{bI} is the energy barrier to migration of interstitials

Energy Barrier to (X_i - V) Pair Diffusion

$$E_a = E_{bI} + E_{bV} + E_{formation} \quad [7]$$

(1) (X-V) => pair migrates

<u>pair forms at surface</u>

$E_a = 0.65 \sim 0.67$ eV

[Jones[10], Woodbury and Avens [12]]

Point defect migration barrier energies

(could be less for vacancy exchange, ring mechanism)

Cu_i^+ : $E_{bI} = 0.29$ eV [13]; V_{Cd} : $E_{bV} = 0.60$ eV [6]

$(Cu_i - V_{Cd})^0$ **formation in bulk:** $E_{form} = 1.93$ eV

lowest possible energy (Cd poor conditions) [Wei and Zhang 12, Wei 16]

=> Pair formation at the surface: E_{form} **~ small**

- **Possibly non-equilibrium injection of vacancies and or Cu [7]**

E_{bV} is the energy barrier to vacancy migration

Energy Barriers to (X_i - V) Pair Diffusion

$$E_a = E_{bI} + E_{bV} + E_{formation} \quad [7]$$

(2) Cu_{Cd}^- => $(X\text{-}V)^-$ => pair migrates $E_a > 1.35$ eV

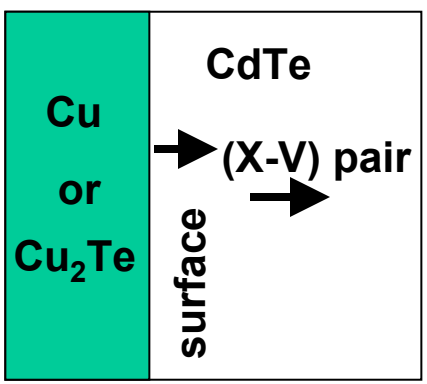
<u>reaction => form pair then migrate</u>

$E_{form} = E_{reaction} = 1.35$ eV at $E_f \leq 0.75$ eV

Cd poor conditions [Wei and Zhang 12, Wei 16]

---

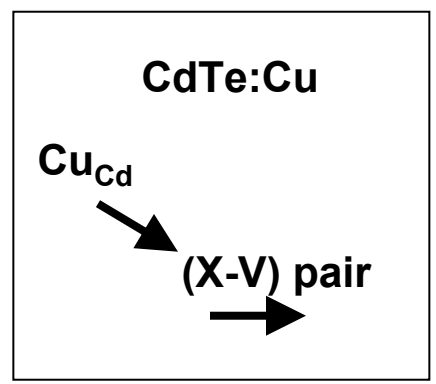
(1) Ea ~ 0.7 eV



(1a) Ea < 0.7 eV

- (X – V) pair formed during processing (slide 7)

(2) Ea > 1.35 eV



Schematic of (X-V) pair diffusion pathways with energy barrier estimates

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Summary and Conclusions

- **Interstitial Diffusion of Cu_i^+**
  - Energetically favored $E_a < 0.3$ eV
  - Highly field dependant
  - Proposed degradation mechanism involves reaction between Cu_i and other defects
- **(X_i - V) pair Diffusion**
  - Classic diffusion experiments: Ea ~ 0.7 eV
    - Propose that:
      - $E_{formation}$ is lowered by surface and/or interface
      - Cu or Cu_2Te reservoir enhances (X-V) pair formation
  - Cells with detectable concentrations (X-V) pairs have poor stability (Ea < 0.7 eV). $CdCl_2$ is the process variable.
  - If the pathway includes reaction {Cu_{Cd} => (X-V) pair} : $E_a > 1.35$ eV
- **Some components of stable CdTe:Cu cells:**

  Low N_t , no Cu reservoir, Cu_{Cd} dopant, non-detectable (X-V) pairs

Non-optimum Processing Of Run 103

- **O2 limited during CdCl2 anneal by graphite source design**
- **CdTe films were annealed at ~400 C without CdCl2 film => "bare heat"**

Why was GB diffusion not considered in this presentation:
• GB diffusion is most likely non-Fickian and very fast any gradients in the GB's are most likely eliminated at processing temperatures and times
• M. Romero et al. show that for well processed cells that diffusion of Cu_{Cd} and (X-V) pairs is not favored at GB's
• SIMS profiles of our devices after ~ 24000 hrs of lightsoak stress show essentially no increase of Cu counts in the CdS layer
• However GB's must be considered as important structures

References

1. "Room-temperature detection of mobile impurities in compound semiconductors by transient ion drift", Igor Lybommirsky, etal (Weizman Institute of Science), May 1997, J.Appl. Phys. 81 (10) 6684-6691
2. "Investigation of fast diffusing impurities in silicon by a transient ion drift method", A. Zamouche, etal, Jan 1995, Appl. Phys. Lett. 66 (5), 631-633
3. "Transient ion-drift-induced capacitance signals in semiconductors",T. Heiser and E.R. Weber, Aug 1998, Phys. R. B, 58 (7), 3893-3903
4. I. Lubomirsky, etal.,"Space charge effects on dopant diffusion coefficient measurements in semiconductors", J. Appl. Phys. (83) 9, 4678-4682, 1998
5. S. Wei, "Role of Defects and Grain Boundaries on Stability", N CdTe R&D Team Meeting minutes, Jan 25-26 (2001)
6. D. Shaw, "Diffusion Mechanisms in II-VI Materials", J. Crys. Growth, 86, 778-796, (1988)
7. C.S. Nichols et al.,"Mechanisms of dopant impurity diffusion in silicon", Phys. Rev. B, 40 (8), 1989
8. M. J. Romero et al.,"Cathodoluminescence of Cu diffusion in CdTe thin films for CdTe/CdS solar cells", Appl. Phys Let. 81 (16), 2002
9. D. Grecu, A. D. Compaan,"Photoluminescence of Cu doped CdTe and related stability issues in CdS/CdTe solar cells", JAP, 88 (5), 2000
10. E.D. Jones et al.,"A Comparison of the Diffusion of Copper, Gallium and Cadmium in Cadmium Telluride," Ad. Mat. For Optics and Electronics, 3, 209-215, (1994)
11. H. h. Woodbury and M. Aven, "Some Diffusion and Solubility Measurements of Cu in CdTe", JAP, 39 (12), 1968
12. S. Wei and S. B. Zhang, "Chemical trends of defect formation and doping limits in II-VI semiconductors: The case of CdTe", Phys. Rev. B, 66, 155211 (2002)
13. B.O. Wartlick et al.,"Study of silver and copper diffusion in p-type $Hg_{0.3}Cd_{0.7}Te$ and CdTe by capacitance measurements", Mat. Sci. and Eng. B71, 2000
14. A. A. Istratov,"Physics of Copper in Silicon", J. Elec. Chem. Soc., 149(1), G21-G30, 2002
15. R.A. Enzenroth et al., "Correlation of stability to varied $CdCl_2$ treatment and related defects in CdS/CdTe PV devices as measured by thermal admittance spectroscopy", J. Phys. And Chem. of Solids, 66, 2005
16. Suhuai Wei, personal communication with W. S. Sampath, 2003

The Thermal Decomposition Kinetics of Cu_2Te: Relevance to CdTe Devices

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This work was performed with the support of U.S. Department of Energy contract DE-AC36-99GO10337.

Outline

- Motivation for study of $Cu_2Te/CdTe$
- Reaction kinetics

$$2Cu + CdTe \rightarrow Cu_2Te + Cd$$

- Description of TDMS experiment
- Thermal decomposition kinetics

$$Cu_2Te \rightarrow 2Cu + Te$$

- Implications for CdTe devices
- Summary

Background: Back Contacts in Thin-Film CdTe Photovoltaic Devices

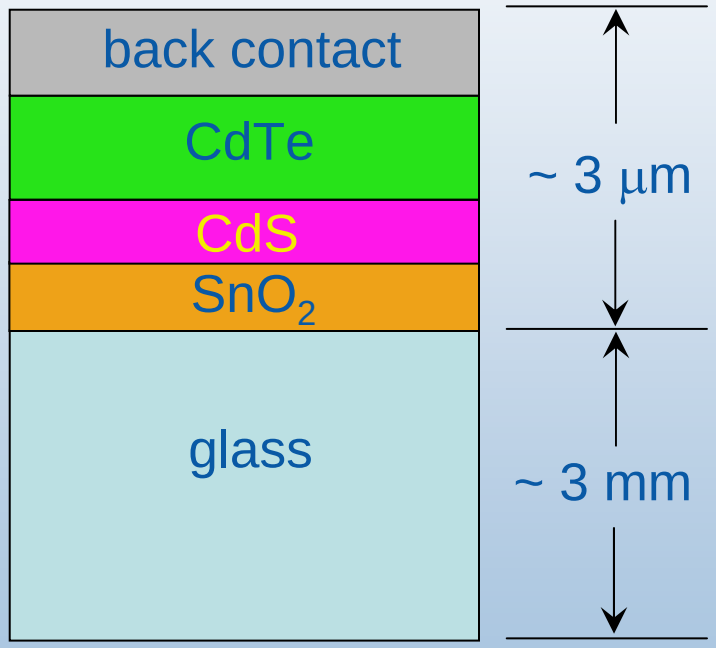
CdTe Back Contacts

- metal/CdTe
  - ➔ Schottky-barrier contact
- add Cu (or Cu_xTe)
  - ➔ ohmic contact
- Other effects of Cu in CdTe solar cells (beneficial or harmful) are not fully understood.

What processing conditions are required for Cu_xTe formation?

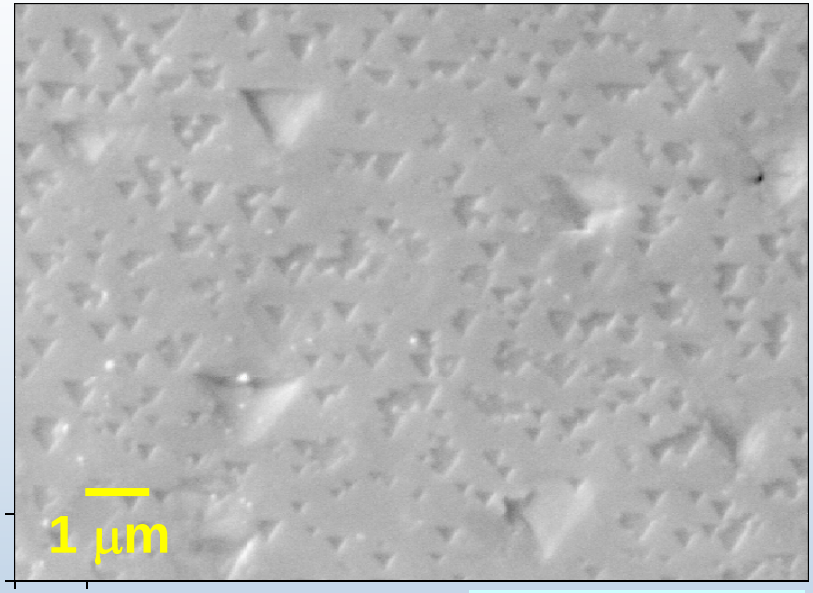
What is the thermal stability of Cu_xTe/CdTe?

Typical Device Structure

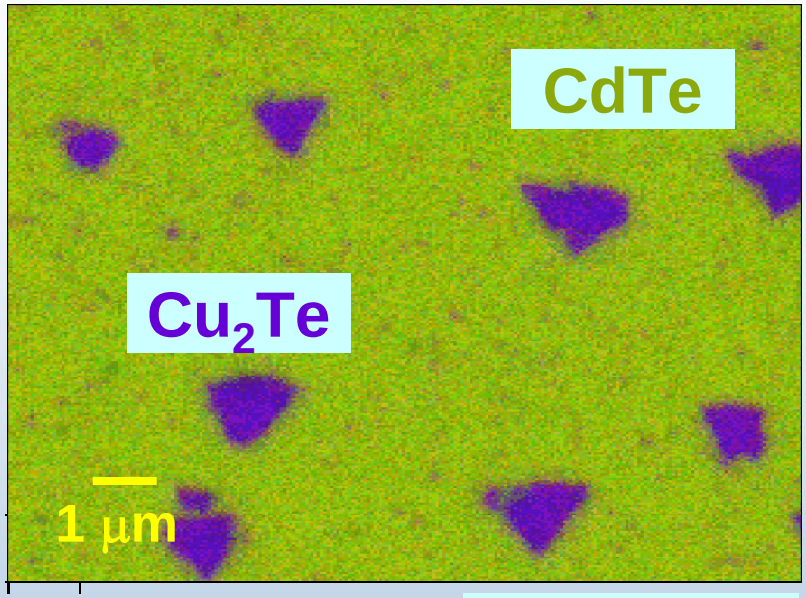


The approach is chemical kinetics.

Reaction Kinetics of Cu + CdTe(111)-B



SEM



AES map

$$2Cu + CdTe \rightarrow Cu_2Te + Cd$$

zero-order reaction $E_a = 180 \pm 5$ kJ mol^{-1}

G. Teeter, J. Chem. Phys. **123**, 184713 (2005).

Chemical Kinetics of Cu_2Te Decomposition

Two-step TDMS experiment in UHV with Cu-foil substrate:

1. ***Cu-foil tellurization:*** $Te(v) + 2Cu(s) \rightarrow Cu_2Te(s)$

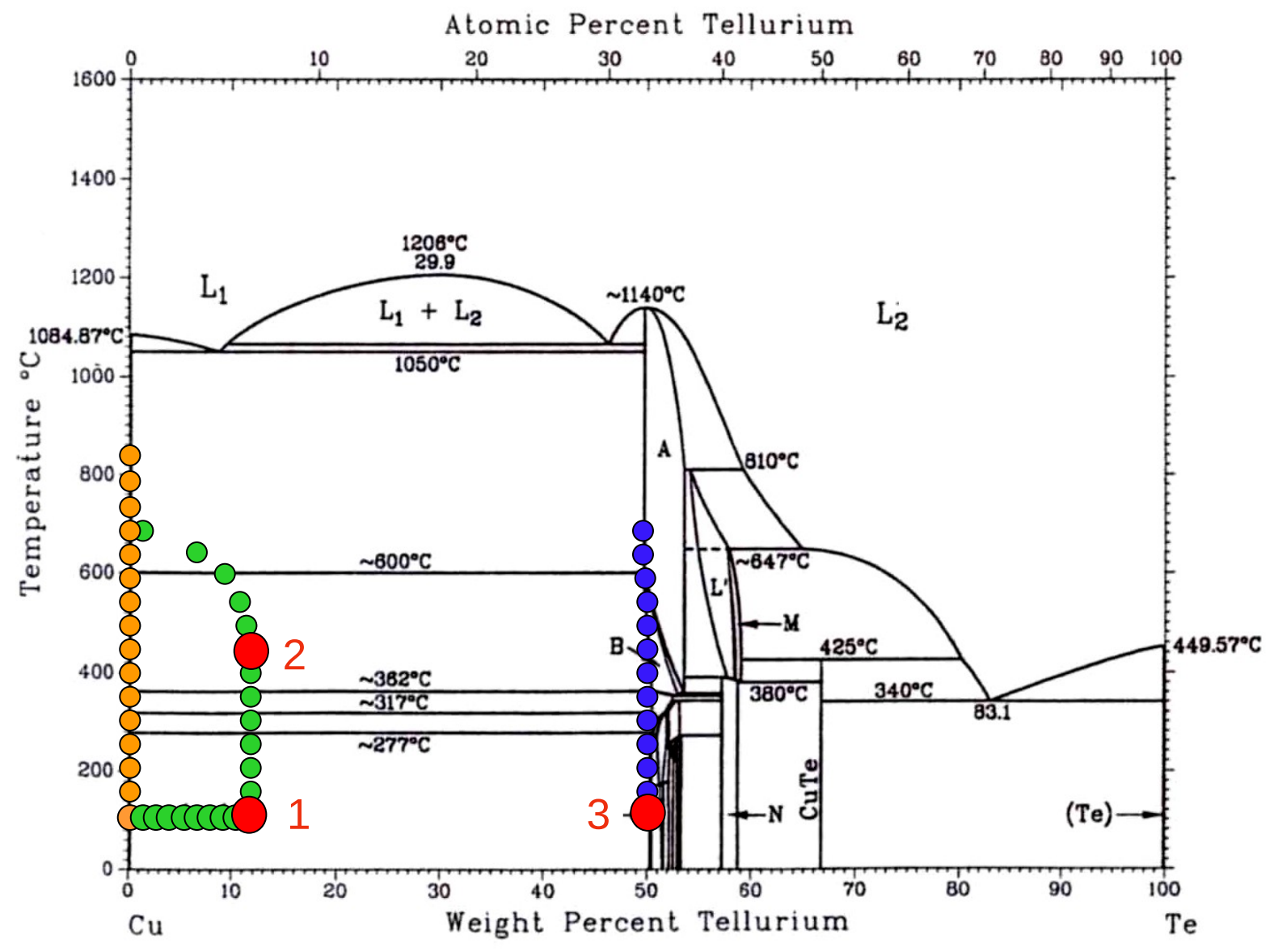
2. ***Thermal decomposition:*** $Cu_2Te(s) \rightarrow Te(v) + 2Cu(s)$

experimental reaction rate: $r = dN_{Te}/dt$

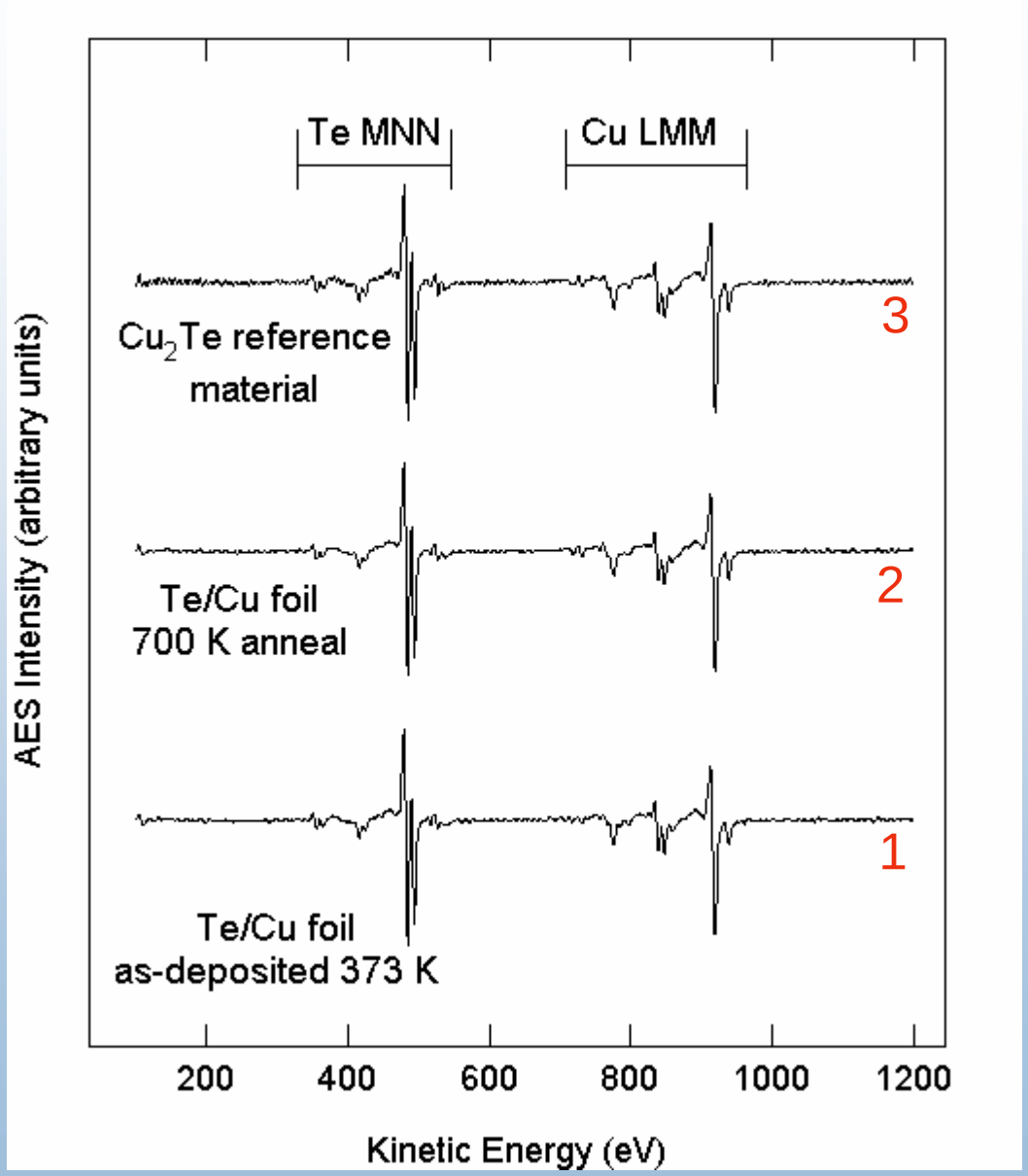
differential rate law: $r = k\,(N_{Cu2Te})^m$

Arrhenius rate constant $k = \nu \exp(-E_a/RT)$

Cu-Te Phase Diagram



Cu-Te Phase Diagram

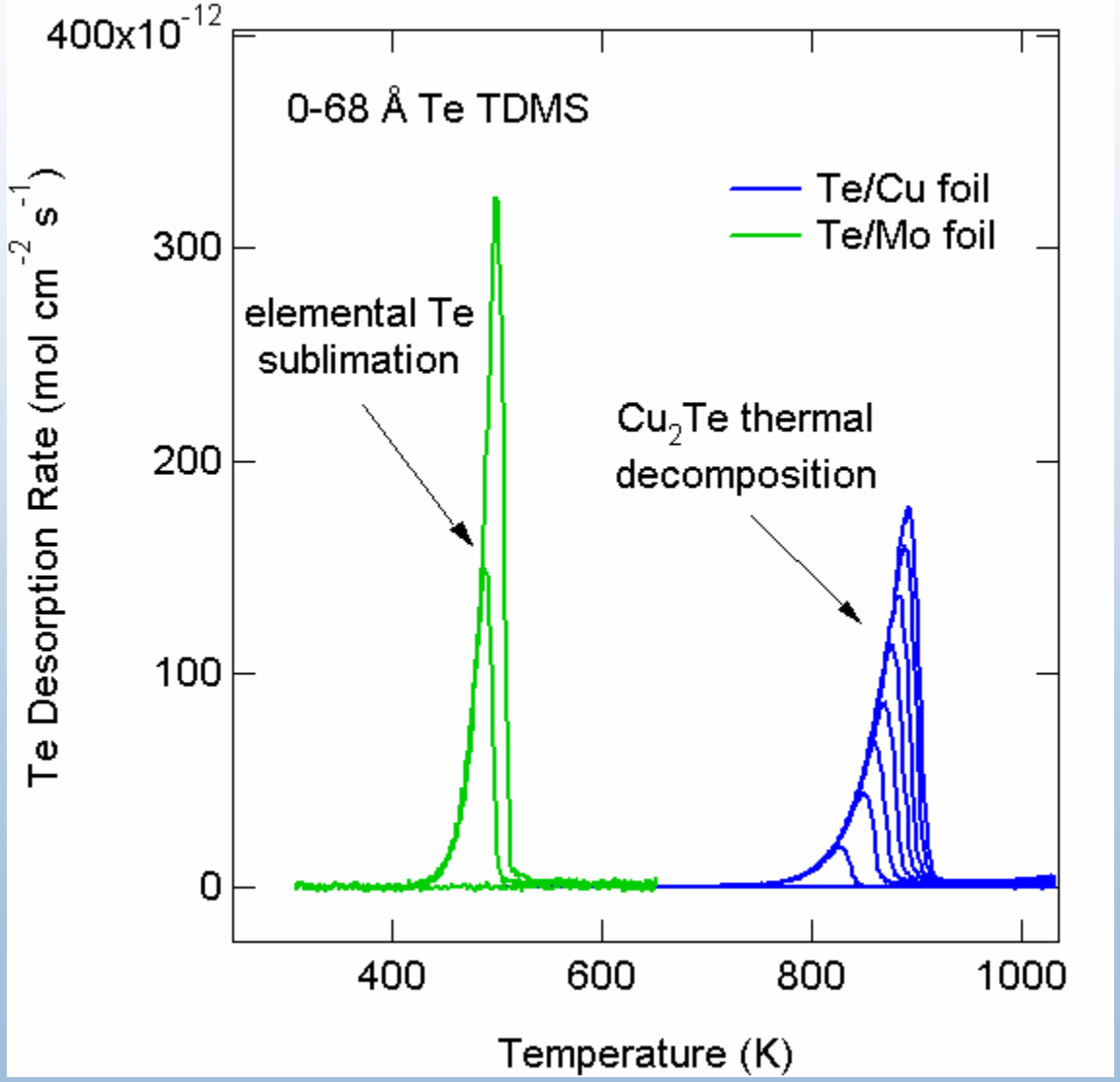


$$Te(v) + 2Cu(s) \rightarrow Cu_2Te(s)$$

Complete reaction for T ~ 373 K.

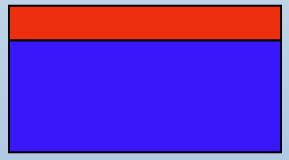
Cu-Te phase diagram predicts Cu_2Te phase.

Thermal-Decomposition Kinetics of Cu_2Te via Te TDMS



0-68 Å Te
Mo foil

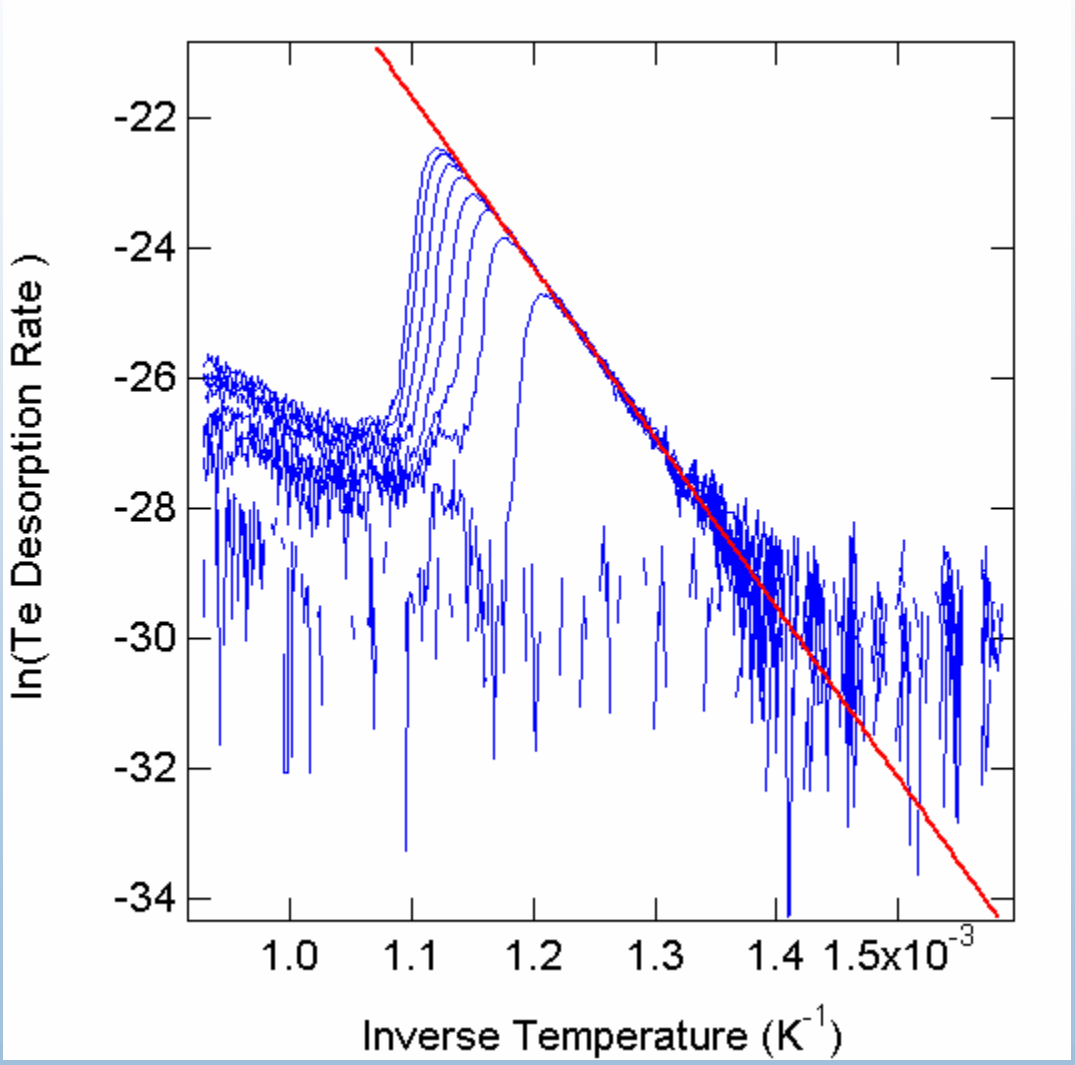
$$Te(s) \rightarrow Te(v)$$



0-68 Å Te
Cu foil

$$Cu_2Te \rightarrow 2Cu(s) + Te(v)$$

Thermal-Decomposition Kinetics of Cu_2Te via Te TDMS



0-68 Å Te

Cu foil

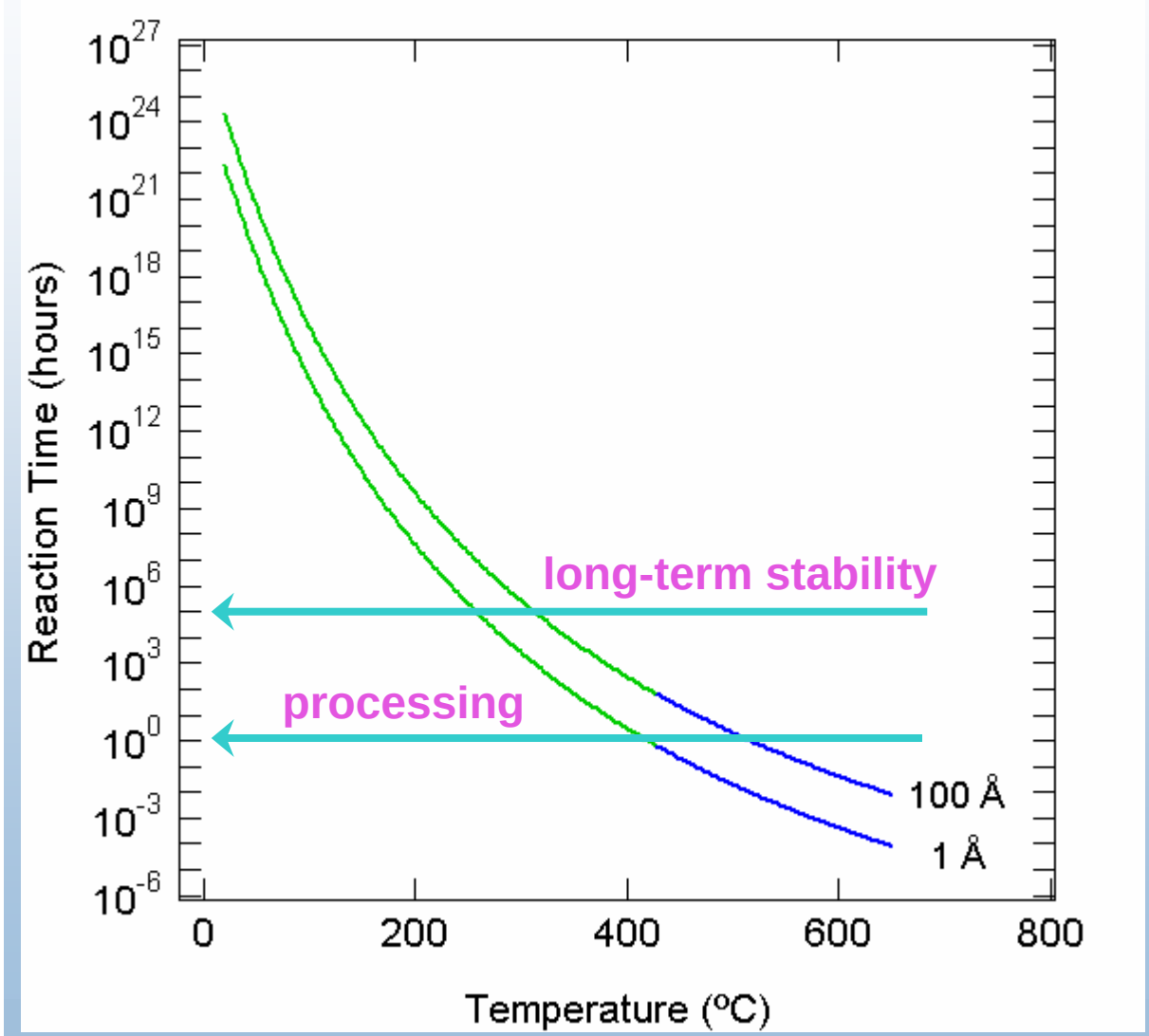
$$Cu_2Te \rightarrow 2Cu(s) + Te(v)$$

zero-order reaction:

$$rate = \nu \exp(-E_a/RT)$$

$$E_a = 217 \pm 3 \text{ kJ mol}^{-1}$$

Application to CdTe Devices



$$Cu_2Te \rightarrow 2Cu + Te$$

$$rate = \nu \exp(-E_a/RT)$$

$$time = thickness/rate$$

$T_{lts} > 250$ ºC

$T_{pr} > 400$ ºC

Summary

- Cu_2Te phase formation — $2Cu + CdTe \rightarrow Cu_2Te + Cd$
- Thermal decomposition of Cu_2Te — $Cu_2Te \rightarrow 2Cu + Te$
- Relevance to device processing — ***Cu_2Te is unstable above 400 ºC***
- Future work
  - All-vacuum Cu_xTe back-contact process (X. Wu and J. Zhou)
  - In-situ spectroscopic ellipsometry (D. Levi)

$$Cu_2Te + CdTe \rightarrow 2Cu_{Cd}Te + Cd$$

X-ray and electron spectroscopy of surfaces and interfaces in CdTe thin film solar cells

Clemens Heske, Lothar Weinhardt, Marcus Baer, Moni Blum

Department of Chemistry

University of Nevada, Las Vegas

heske@unlv.nevada.edu

Principle Approach

Combine a variety of surface and near-surface bulk spectroscopies to derive the electronic and chemical structure of interfaces

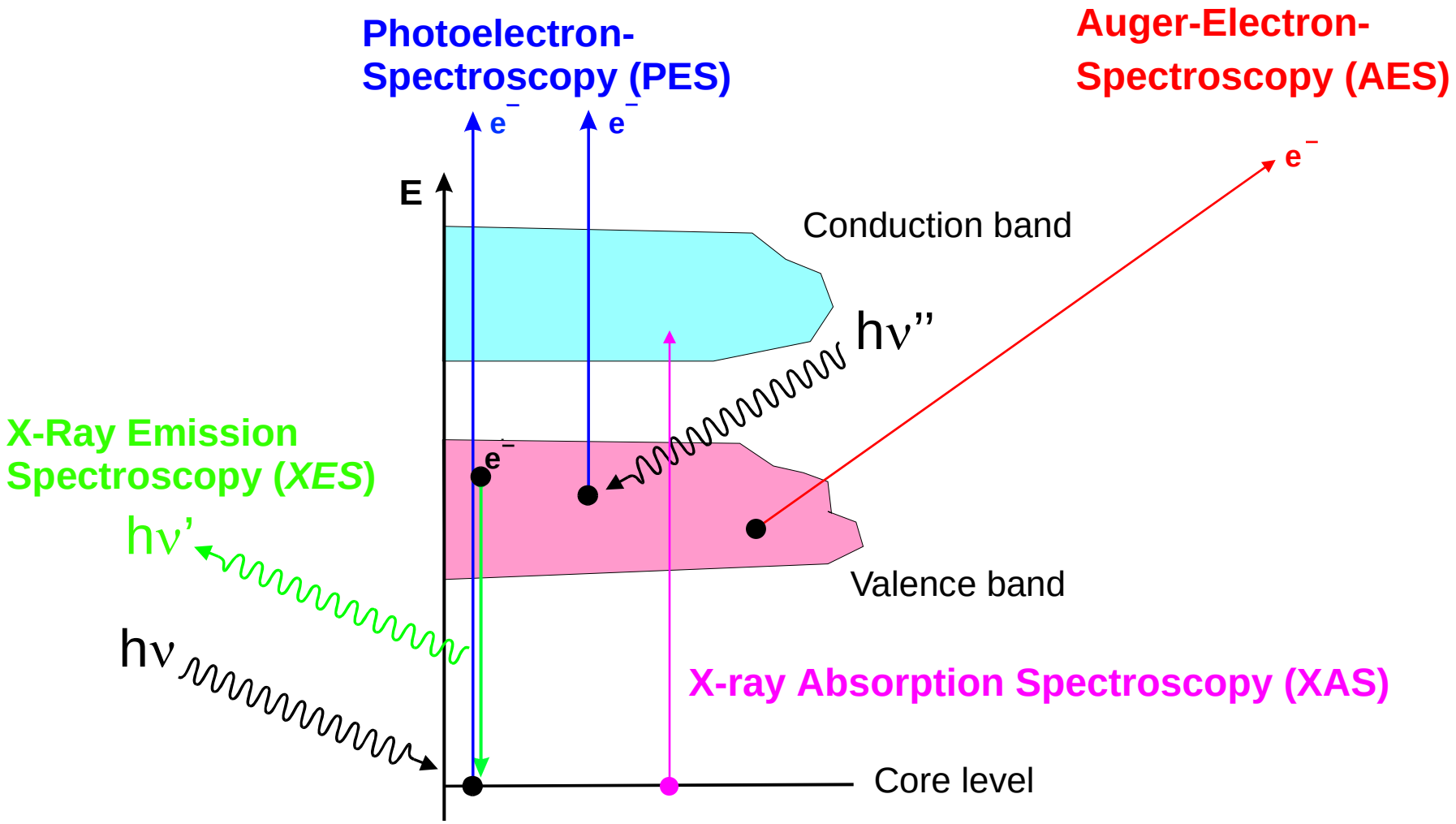
Team up with partners making state-of-the-art thin film solar cells

Methods

- **Photoelectron Spectroscopy (XPS, UPS, PES):**
  Chemical Environment, Valence Band and VB Offset (Surface)
- **X-ray excited Auger Electron Spectroscopy (XAES):**
  Chemical Environment (Surface)
- **Inverse Photoemission (IPES):**
  Conduction Band and CB Offset (Surface)
- **X-ray Emission Spectroscopy (XES):**
  Chemical Environment, Valence Band (Bulk, Buried Interface)
- **X-ray absorption spectroscopy (XAS = NEXAFS = XANES)**
  Chemical Environment, Conduction Band (Bulk, Buried Interface)
- **Near Future: Scanning Probe Microscopy and Spectroscopy**

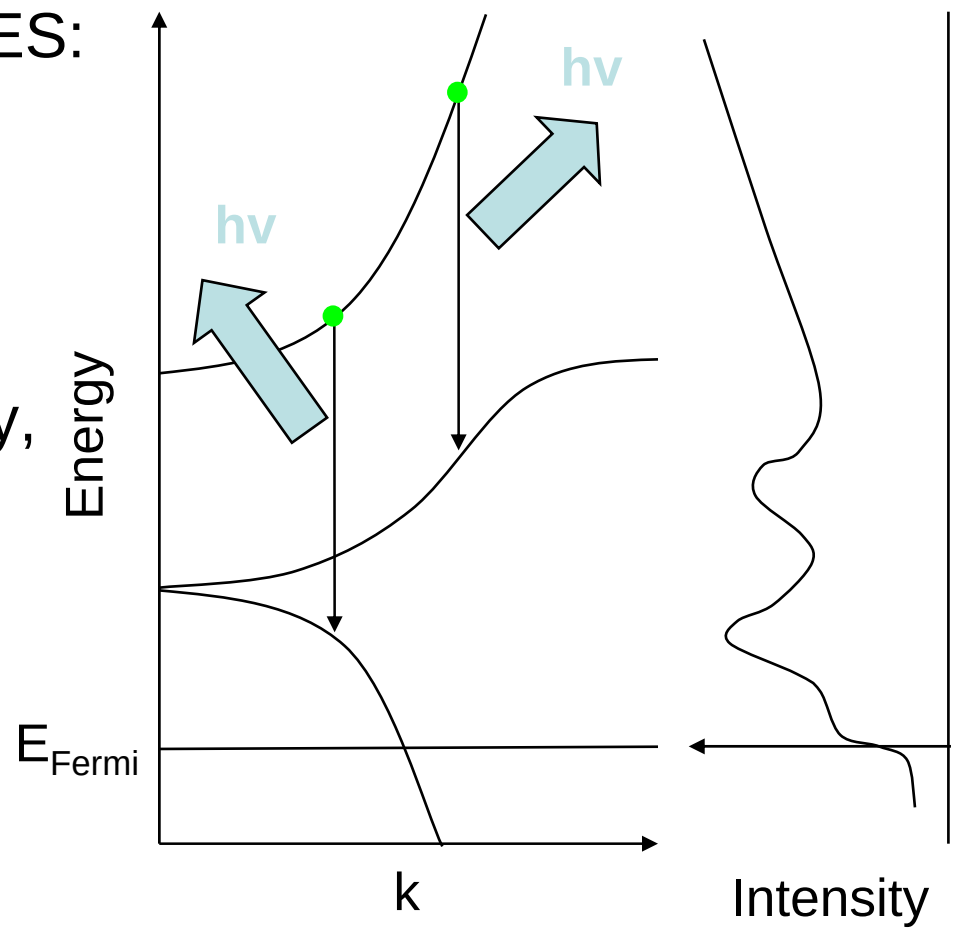
- **Electronic Band Gap Combinations: IPES+UPS and XES+XAS**

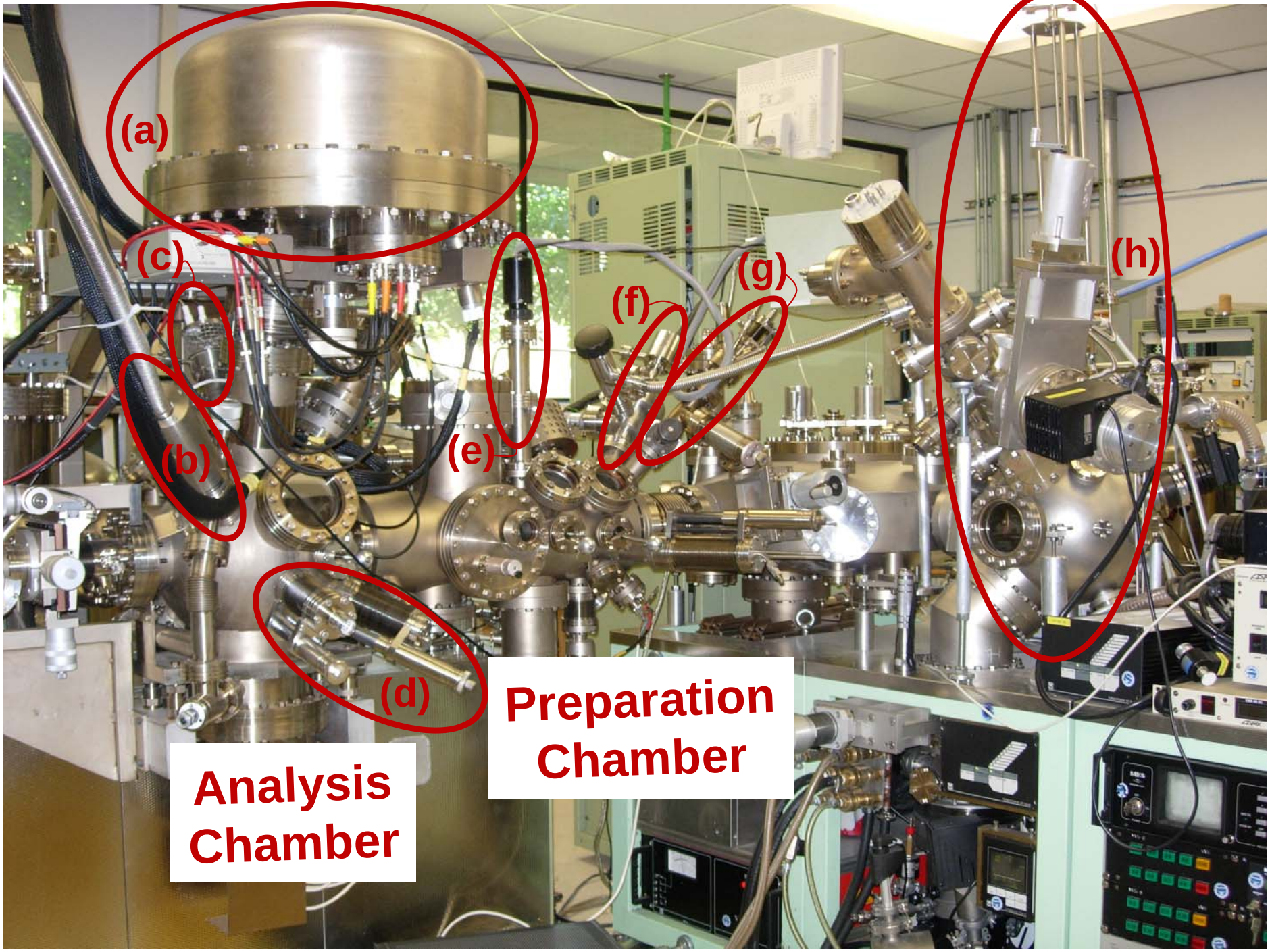
Methods I: Soft X-ray Spectroscopies

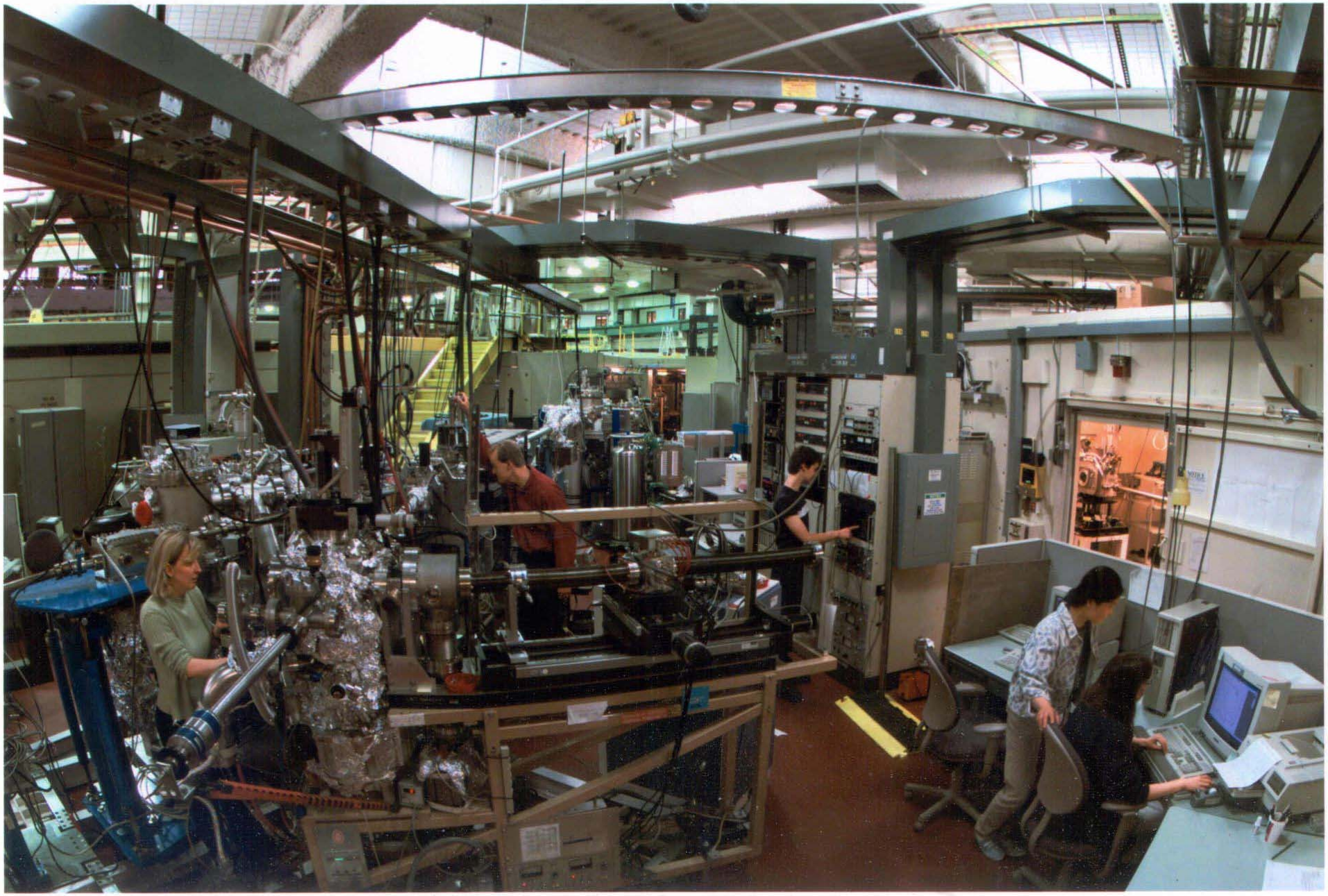


Methods II: Inverse Photoemission (IPES)
Spectroscopy of unoccupied states

- "Time-reversed" process of PES:
  - Excitation with electrons
  - Detection with UV-photons
- 2 modes:
  - Variation of electron energy, fixed hν (our case)
  - Fixed electron energy, hν-spectrometer
- Determination of the conduction band minimum !



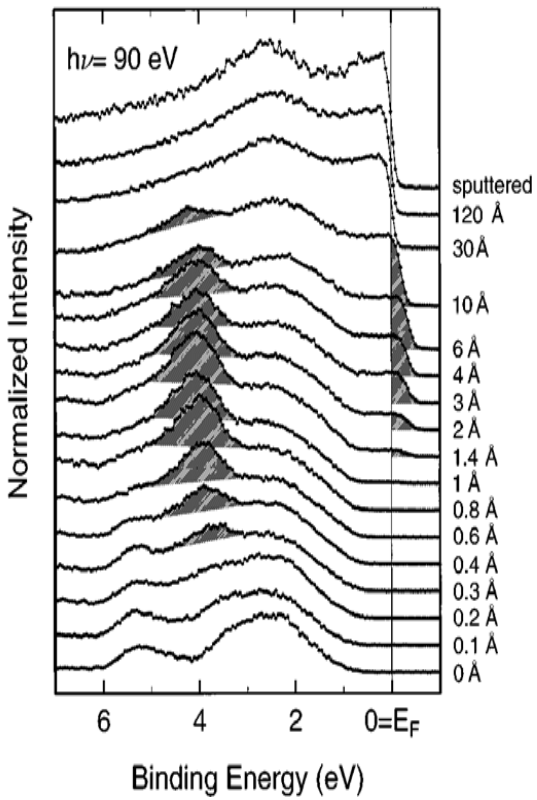

(a)
(b)
(c)
(d)
(e)
(f)
(g)
(h)
Analysis Chamber
Preparation Chamber



Beamline 8.0 – Advanced Light Source – Berkeley Lab

PES example: Mn on Cd(Zn)Te

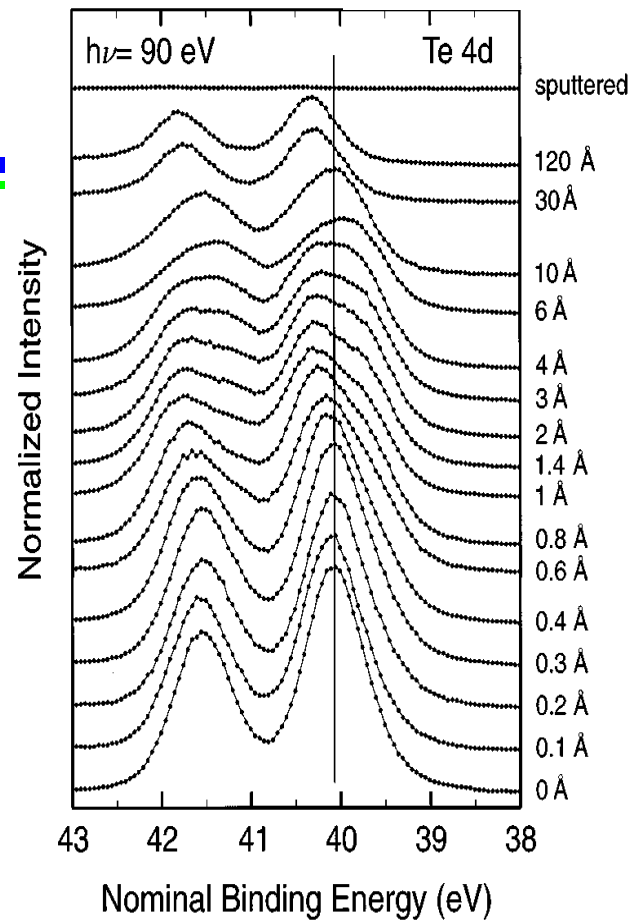
Valence Band

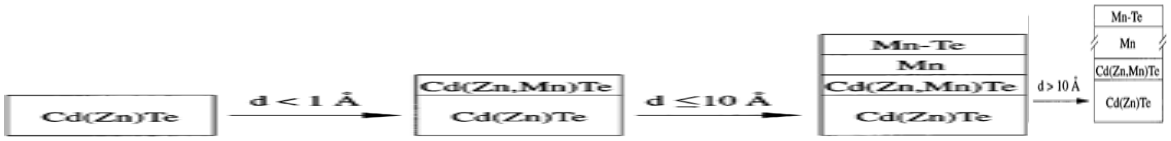


Mn

Core Level

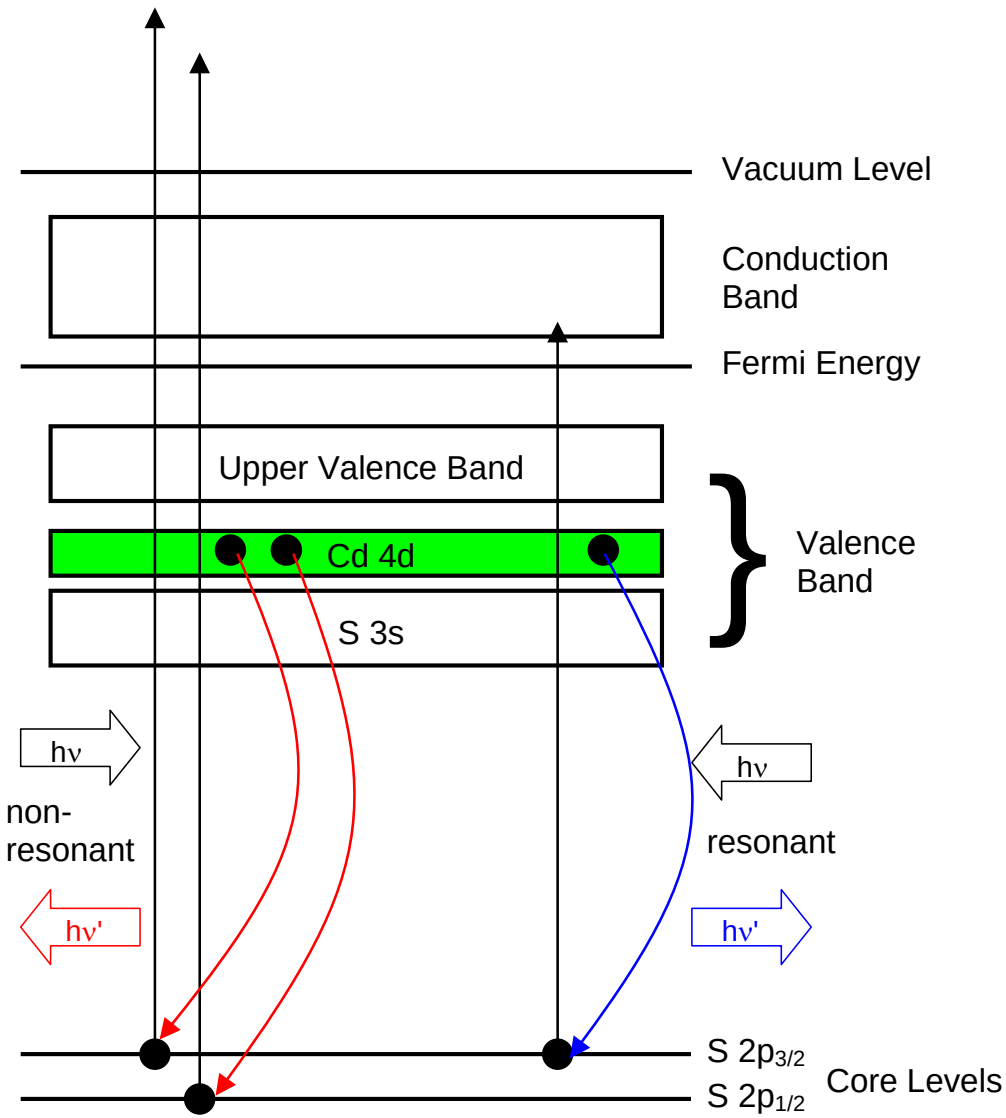
Mn

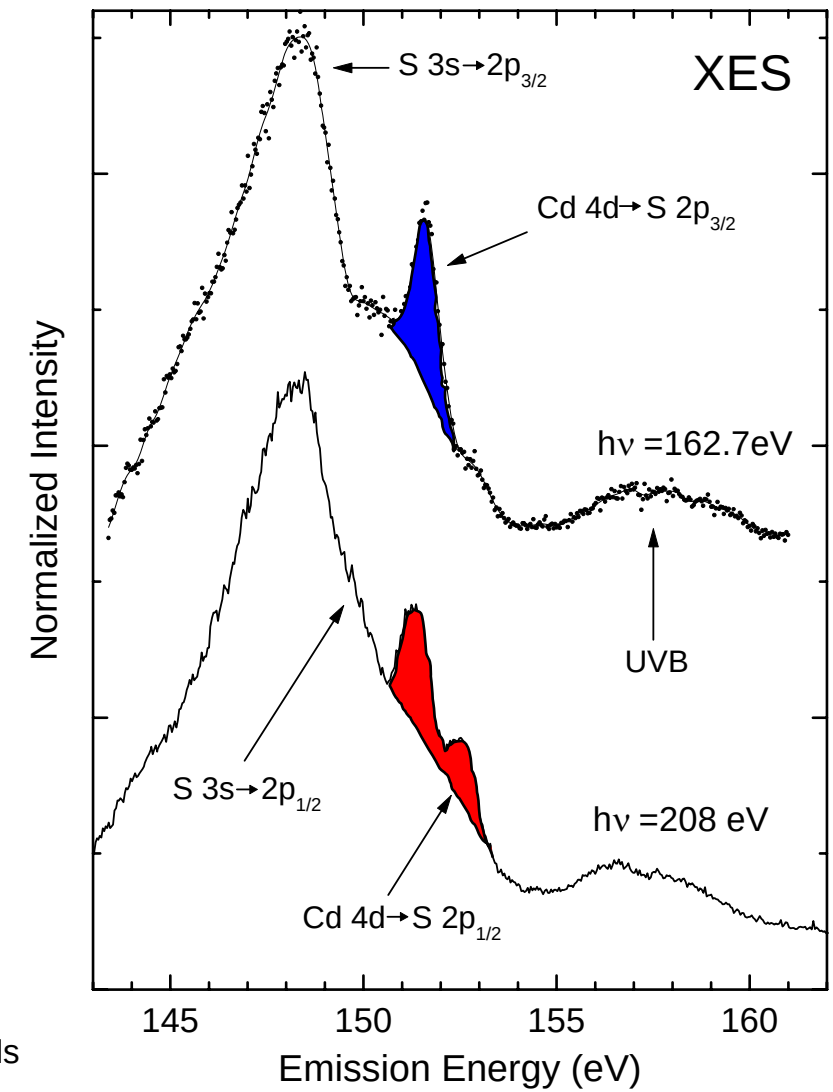




Phys. Rev. B 56, 2085 (1997)

Basic principle of X-ray emission: example CdS





XES of various sulfur compounds

Peak identification:

(1): S 3s → S 2p sulfide

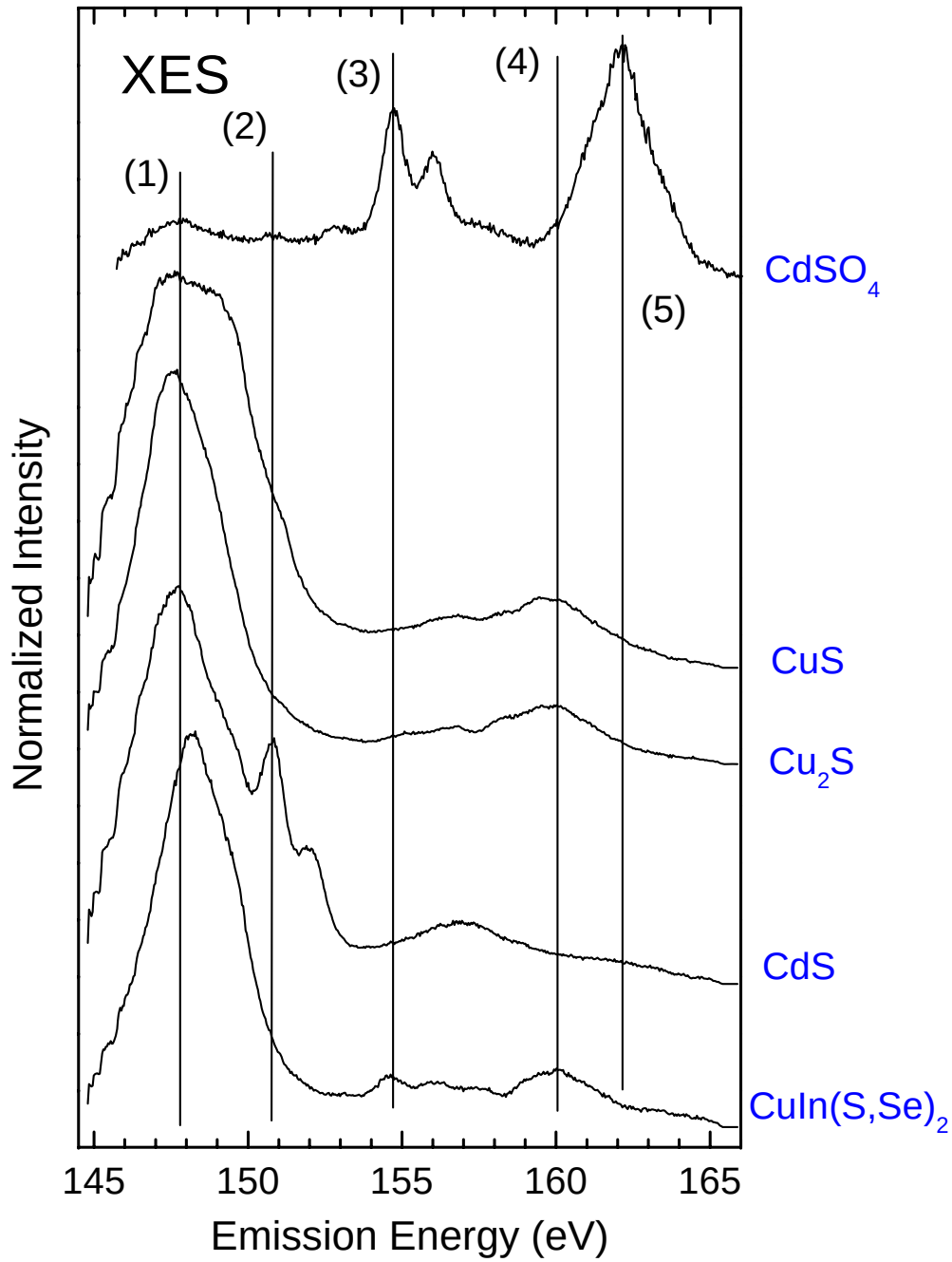
(2): Cd 4d → S 2p S-Cd bonds

(3): S 3s → S 2p S-O bonds
In 5s → S 2p S-In bonds

(4): Cu 3d → S 2p S-Cu bonds

(5): S 3d → S 2p S-O bonds

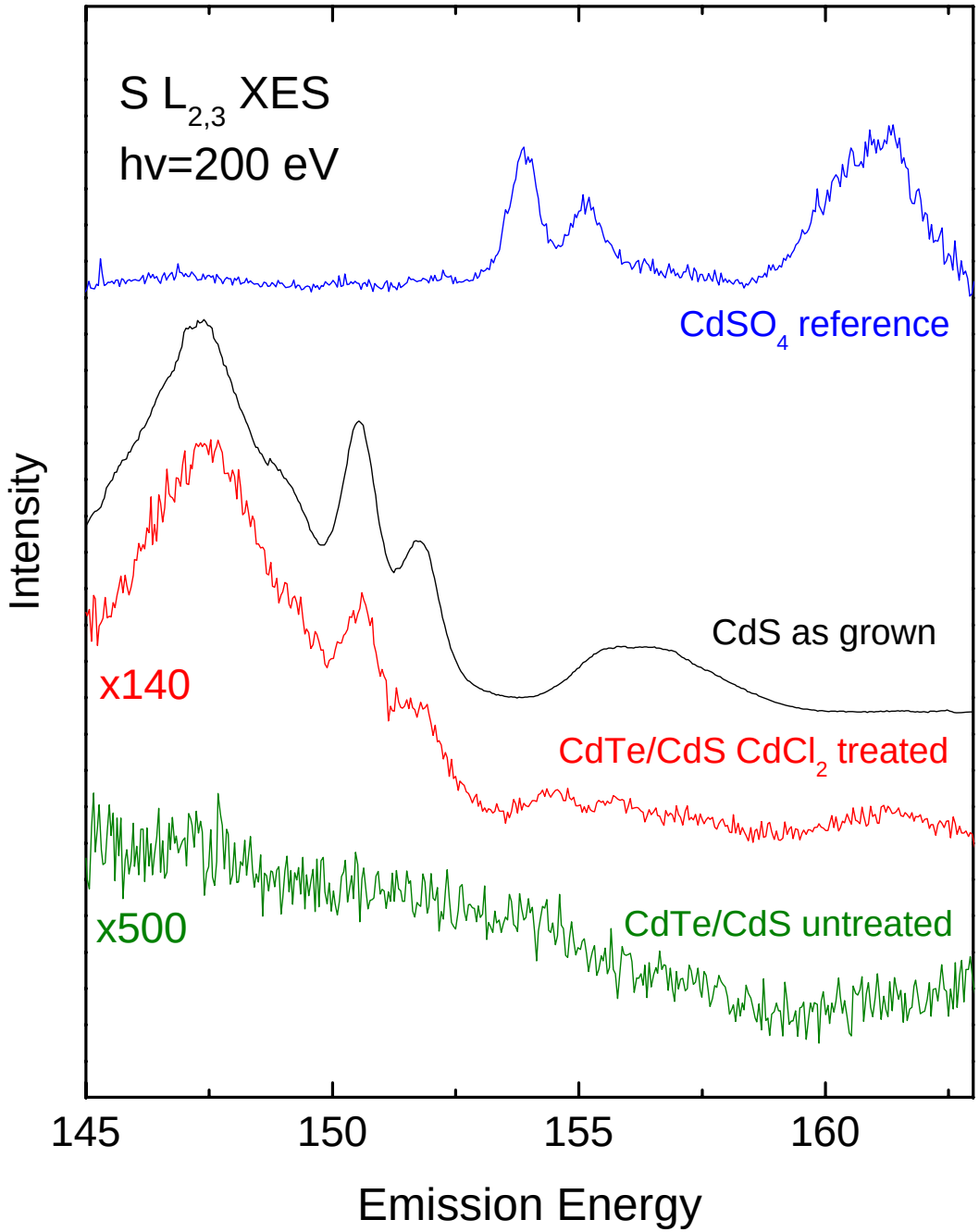
→ Local environment of sulfur atoms can be identified !



phys.stat.sol. (a) **187**, 13 (2001)

XES on CdTe/CdS (Al Compaan, UT)

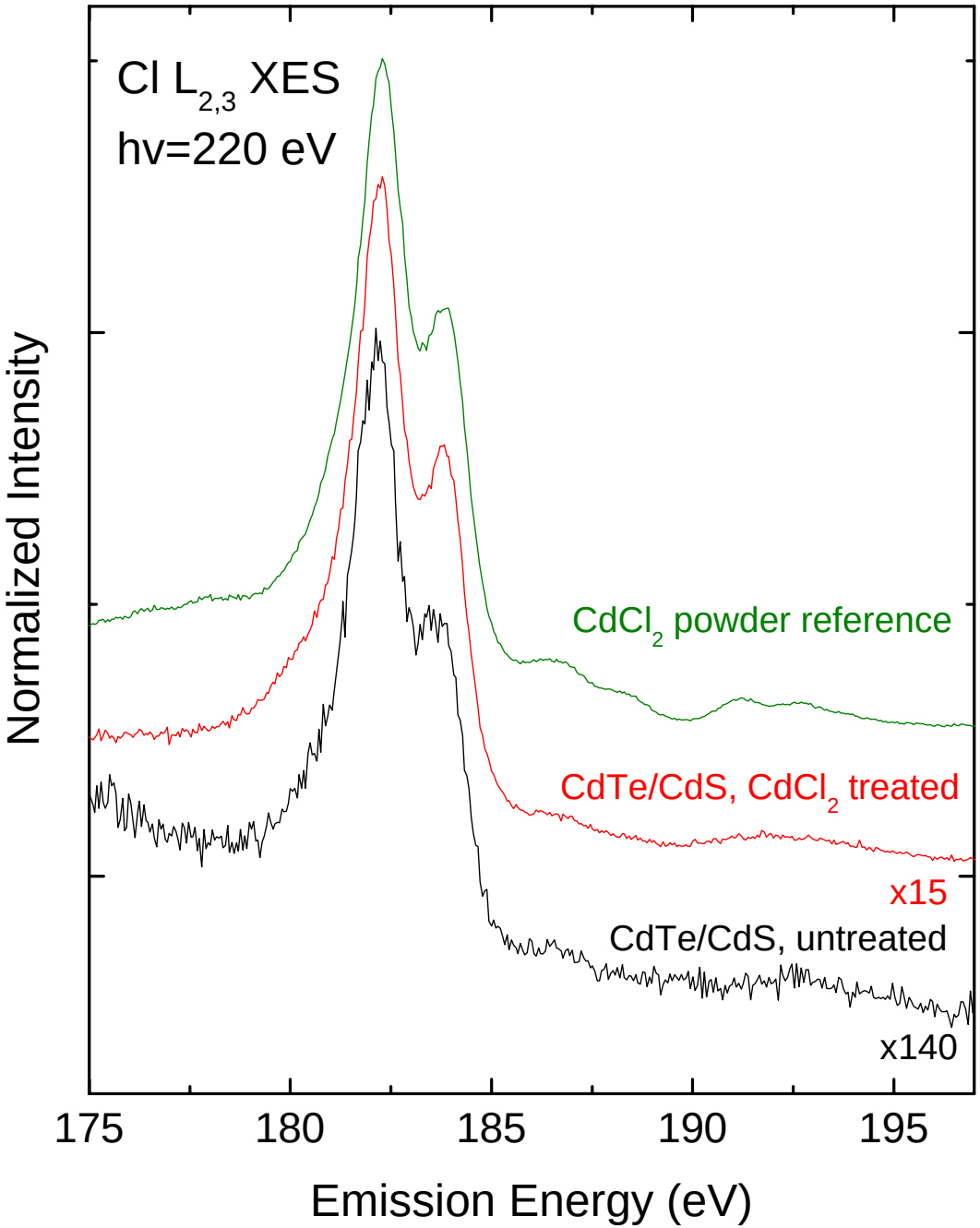
- No sulfur on the surface of untreated CdTe/CdS
- But: sulfur detectable after $CdCl_2$ treatment
- Two types of sulfur: CdS and SO_4^{2-}



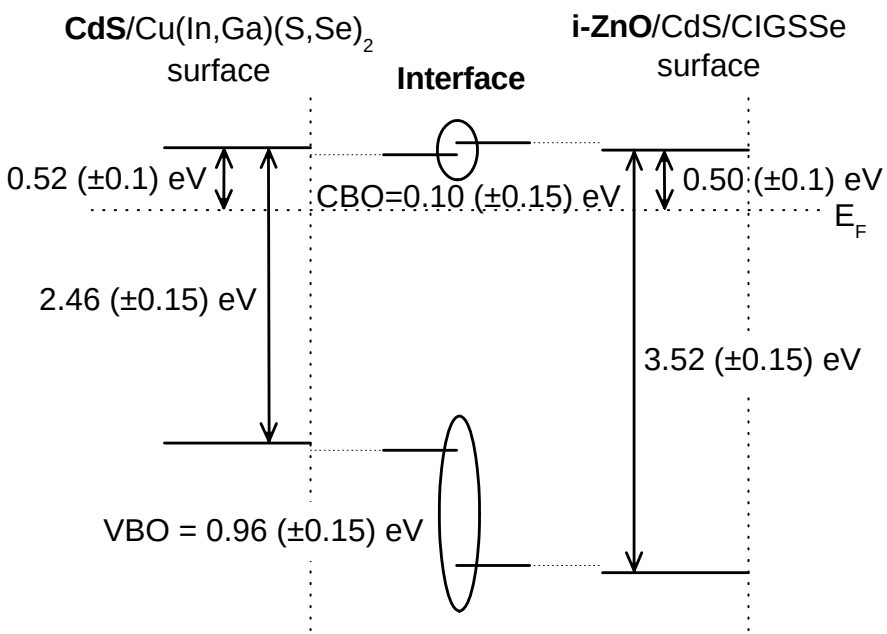
XES on CdTe/CdS (Al Compaan, UT)

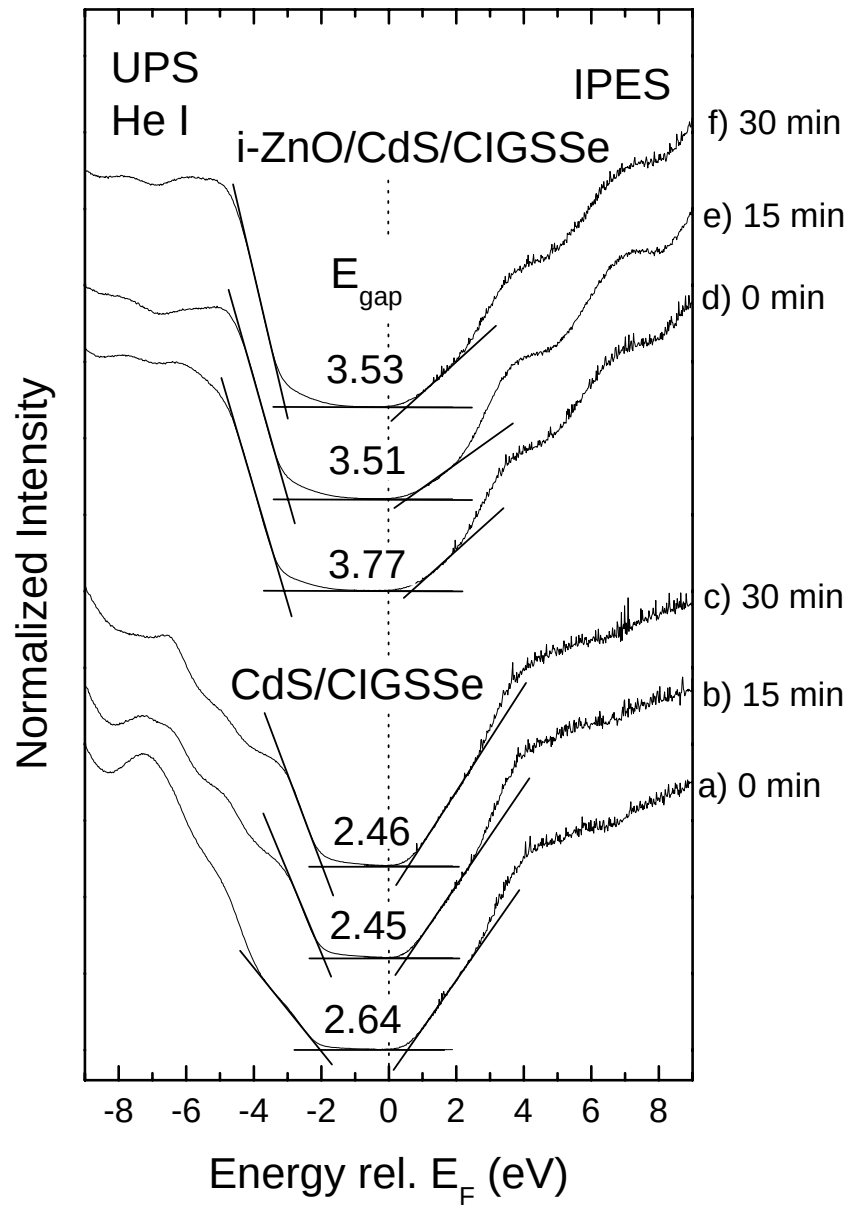
How about the Cl?

- Some Cl on the untreated CdTe surface
- Much more Cl on the treated surface
- On the treated surface: some Cl-Cd bonds



Combining UPS, XPS and IPES: ZnO/CdS (on CIGSSe)

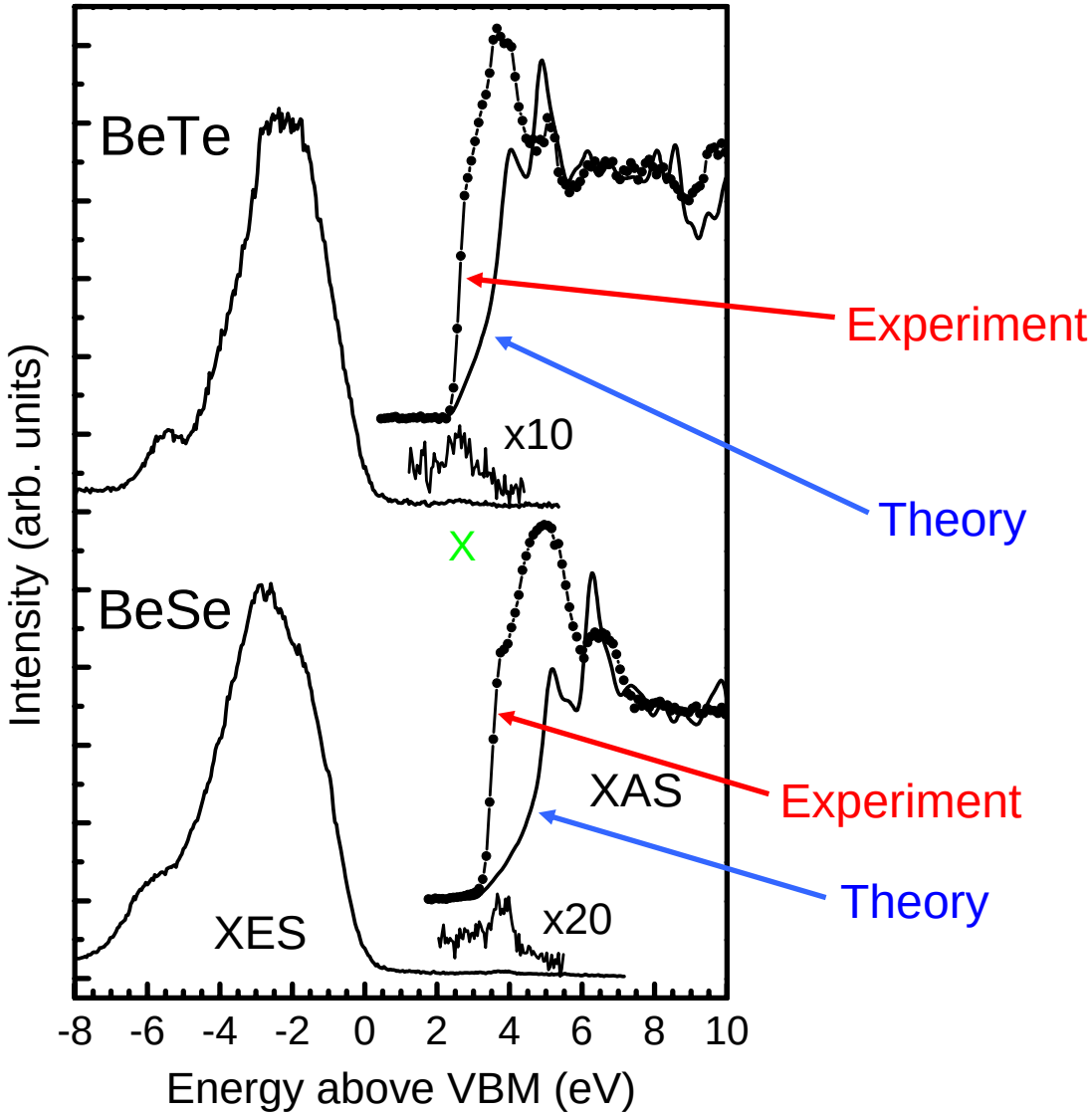




- Studies require clean surfaces and/or mild cleaning
- Conduction band is flat
- i-ZnO is not degenerate

APL **84**, 3175 (2004)

Combining XAS and XES to determine the (bulk) band gap (and more!)



Summary

Soft x-ray spectroscopy allows the investigation of surfaces and buried interfaces

- Atom-specific and chemically sensitive
- Surface and near-surface bulk information
- Variety of effects: reactions, intermixing, impurities, ...
- Detailed experimental picture of the electronic structure:
  Valence Band Offset, Conduction Band Offset, Band Gap

- Let‘s collaborate! (heske@unlv.nevada.edu)

Chemical Fluctuation-Induced Nanodomains in $Cu(In,Ga)Se_2$ Films

(implication on charge separation in the device)

Rommel Noufi

Yanfa Yan
Kim Jones
Manuel Romero
Mo Al-Jassim
Kannan Ramanathan
Billy Stanbery
Jehad AbuShama

Acknowledgement: Suhai Wei and the Polycrystalline Thin Film Group
DOE Contract No. AC36-99GO10337

Outline

- Background
- Our Findings
- Implication on the Process of Charge Separation
- Summary

New Insight

Intra-absorber junction (IAJ) model

…CIS absorbers are in fact two-phase mixtures and concludes that this heterogeneity is fundamental to charge separation in devices made from them

…V_{Cu} preferentially segregate to form the β-phase

…Ga preferentially segregates to α-phase

- B.J. Stanbery

Proceedings of the 31st IEEE PVSC, 2005

Peculiar Features of the $CuIn_xGa_{1-x}Se_2$ Devices

- High efficiency over a wide range of Cu-poor compositions: Cu/In+Ga = 0.95 to 0.85
- Composition for optimum device efficiency is in the $\alpha + \beta$ composition region of the phase diagram
- Tolerates extended defects, i.e., dislocations, grain boundaries, etc.
- Low V_{oc}/E_g compared to GaAs and Si. Performance is poorest for high Ga concentration
- Several junction partners yield high-efficiency devices, i.e., CdS, ZnS, In_2S_3, ZnSe, ZnO

Microstructural Implications

Film composition within the two phase $\alpha + \beta$ region:

– Local aggregation of the Neutral Defects Complex [$2V^{-}_{Cu} + In^{+}_{Cu}$], i.e., lattice comprising mixture of relatively Cu-rich and Cu-poor "*NANODOMAINS*"

– α and β are tetrahedral with almost identical lattice parameters

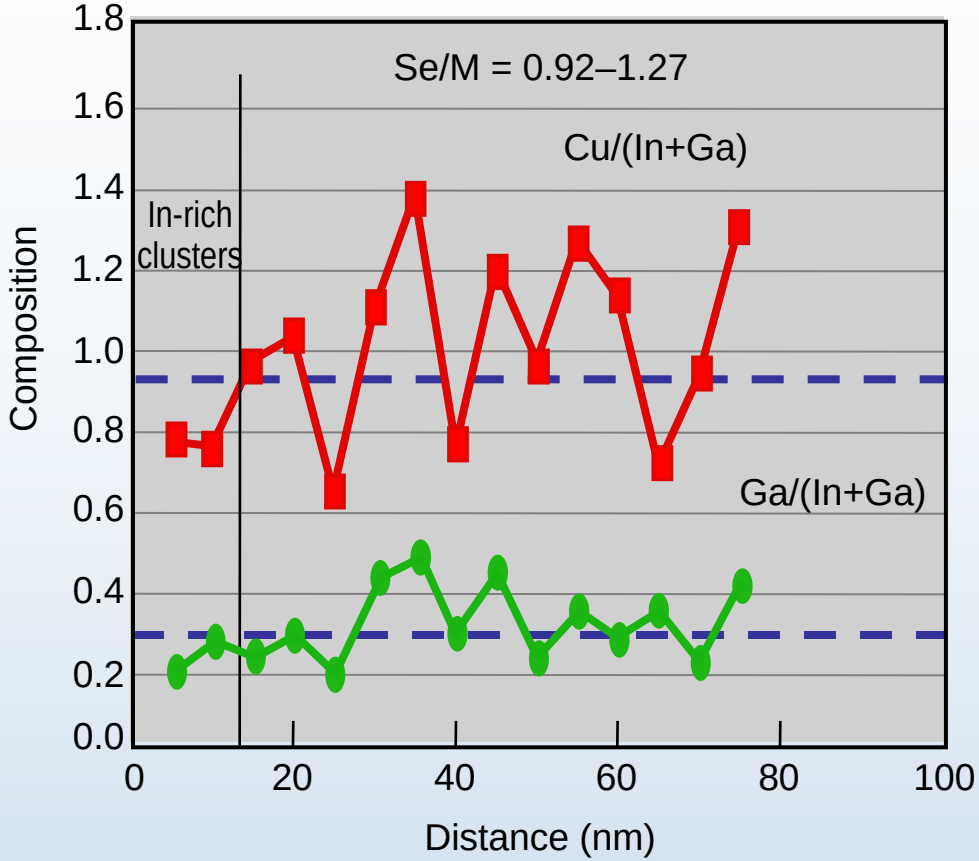
– Crystallographic coherence of the α and β phase boundary

– Therefore, no abrupt boundaries or lattice structural defects at the interface between the two is expected

– Nanodomains may form 3-dimensional interpenetrating percolation transport of both electrons and holes

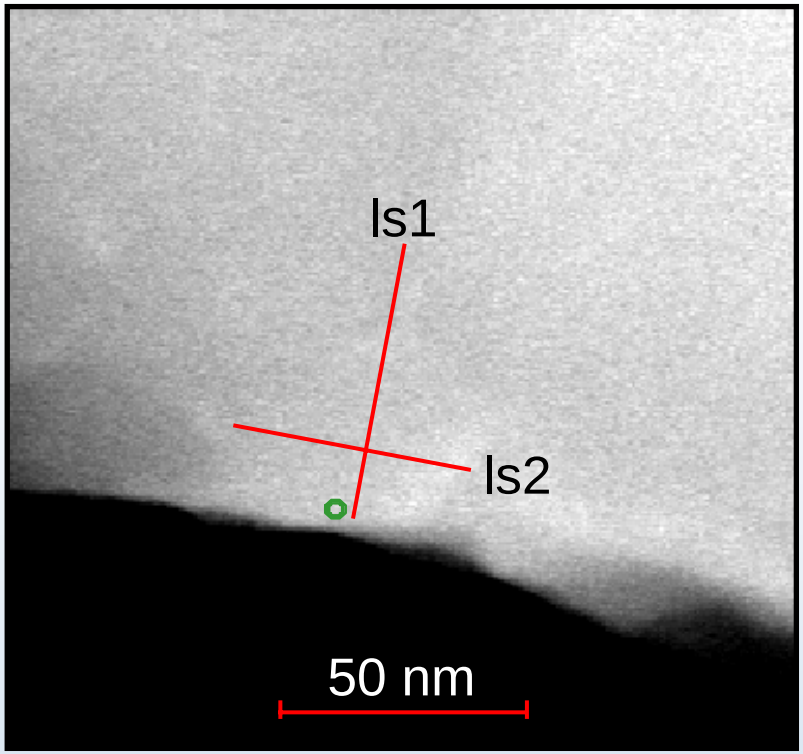
Chemical Fluctuation Determined by EDS

Nano EDS



e⁻ probe : 5 Å

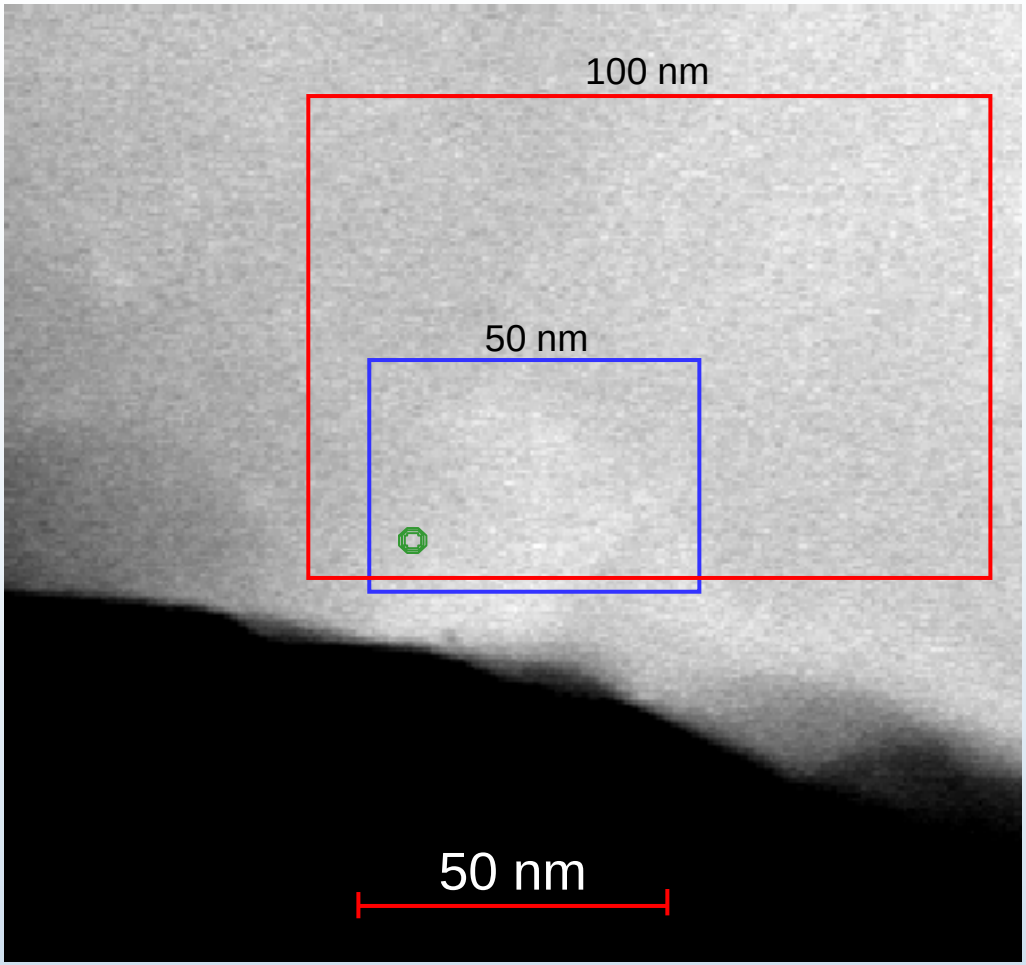
Z-contrast image



ls2: Cu/(In + Ga) = 0.8
Ga/In = 0.5

e⁻ probe : 1.4 Å

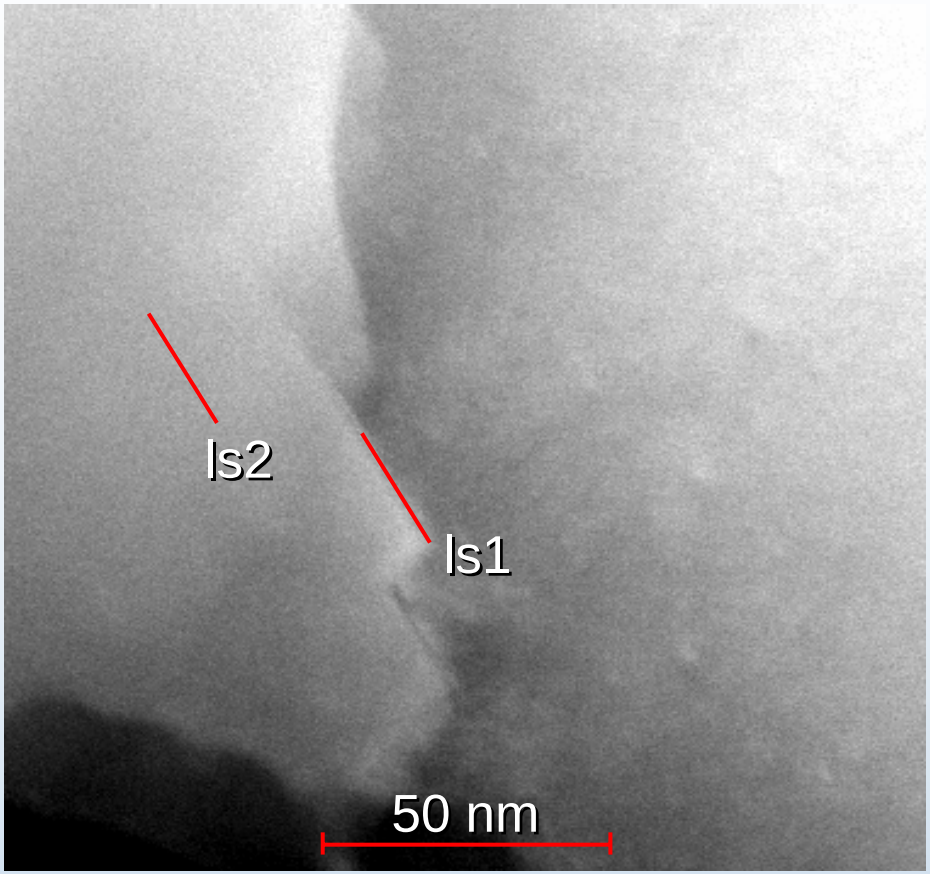
Composition from Large Area



	Point	50 nm Box	100 nm Box
Cu	21	23	23
In	21.5	14	18
Ga	8	8	7.5
Se	49.5	55	51.5

Fluctuation in GBs?

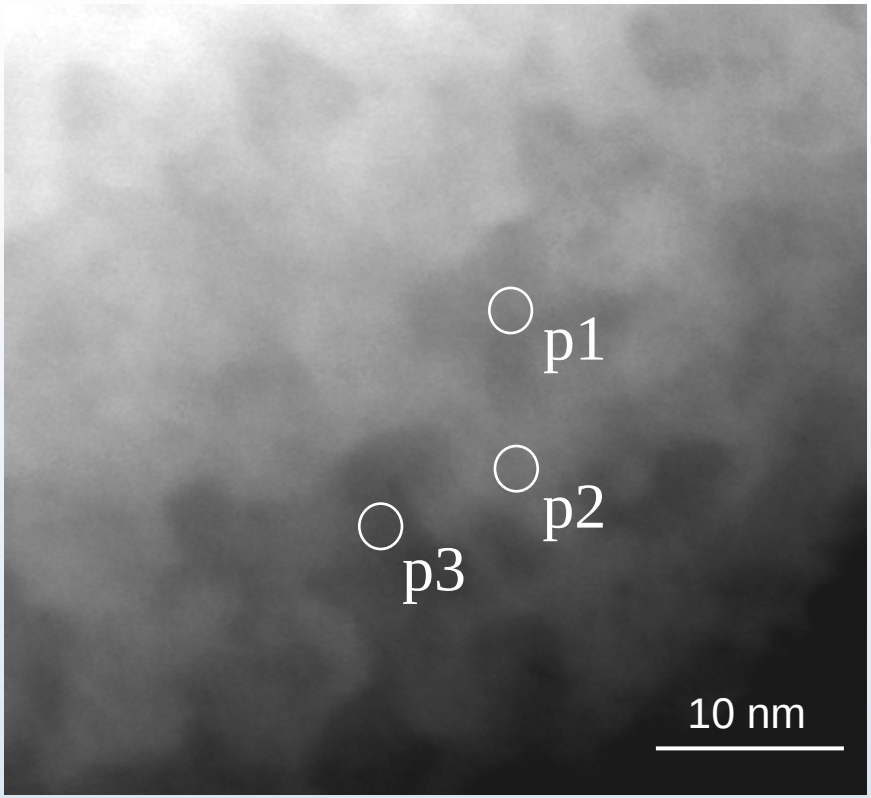
ls2
Compositional fluctuation like before



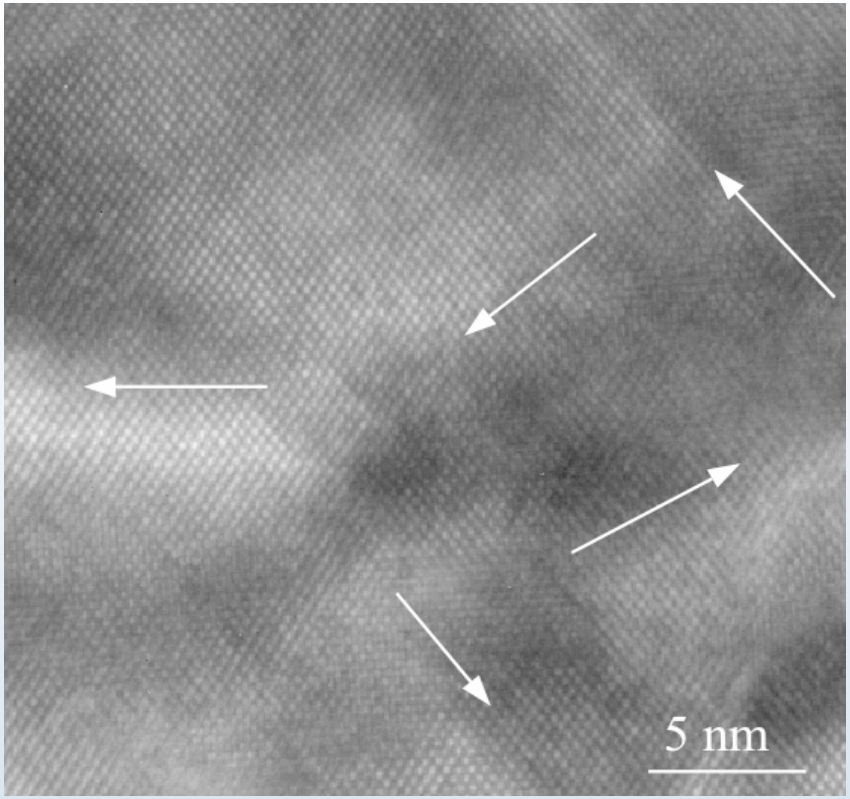
Ls1

Cu/In+Ga	Ga/In+Ga
0.7	0.15
0.74	0.12
1.0	0.22
0.7	0.16
0.71	0.13

Chemical Fluctuation-Induced Nanodomains

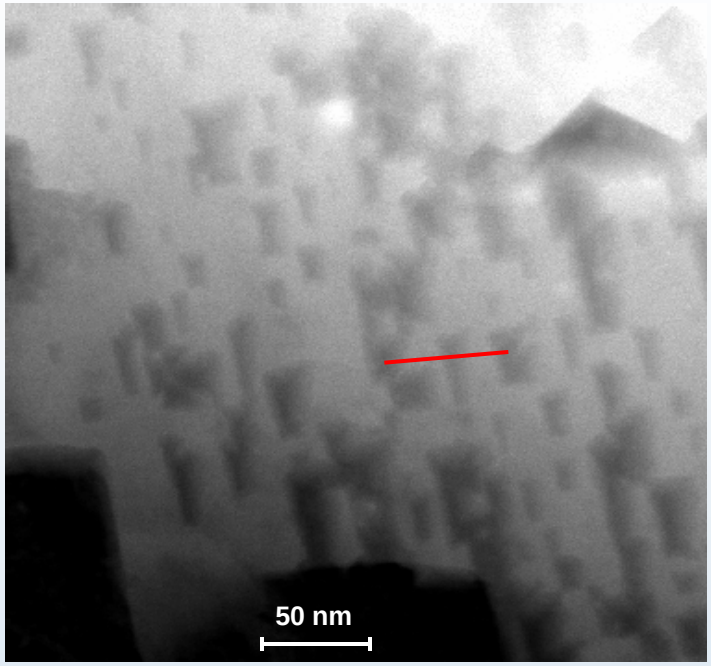


HRTEM Image of Coherent Domain Walls

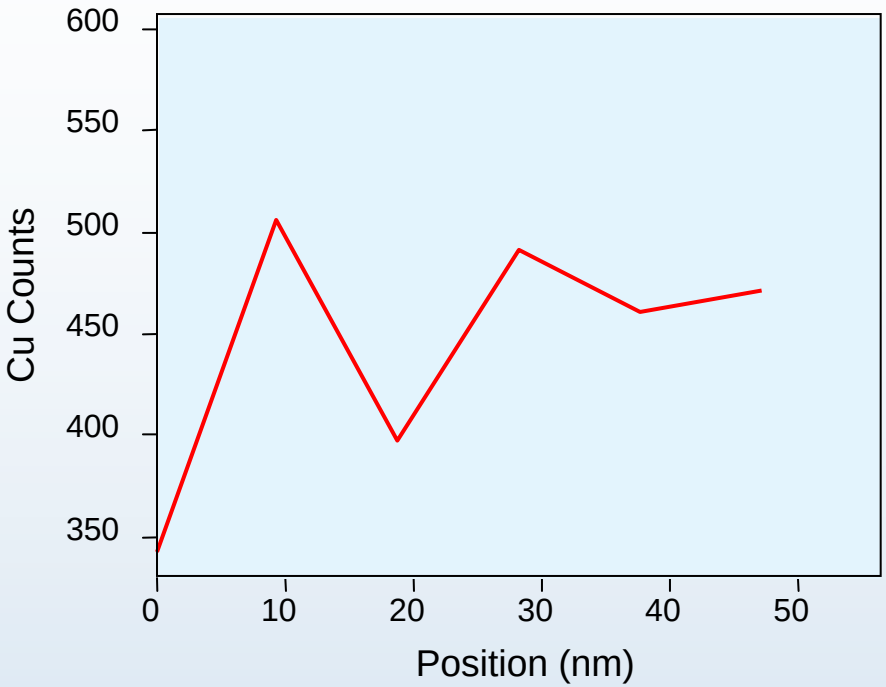


p1	p2	p3
31.3:14.3:6.3:48.1	26.7:15.7:9.6:48.0	30.0:15.2:5.8:49.0
Cu In Ga Se		

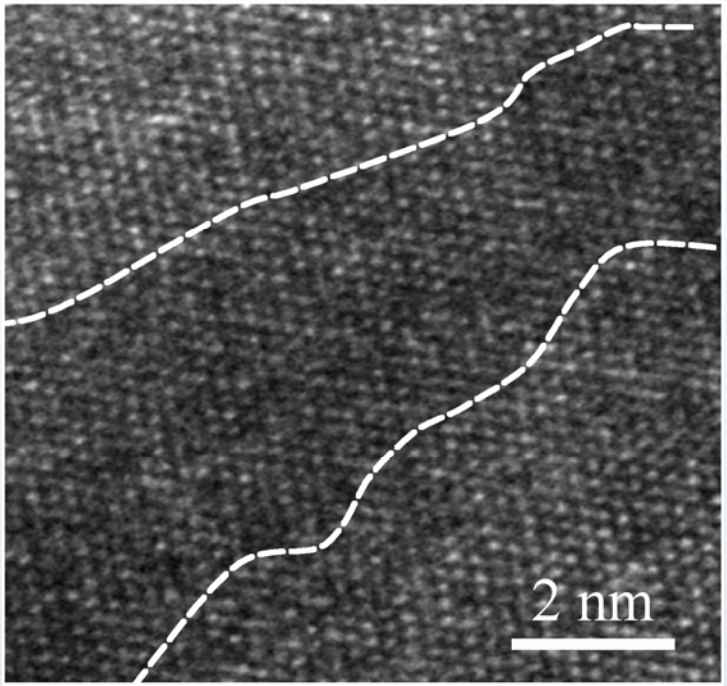
Large Domains



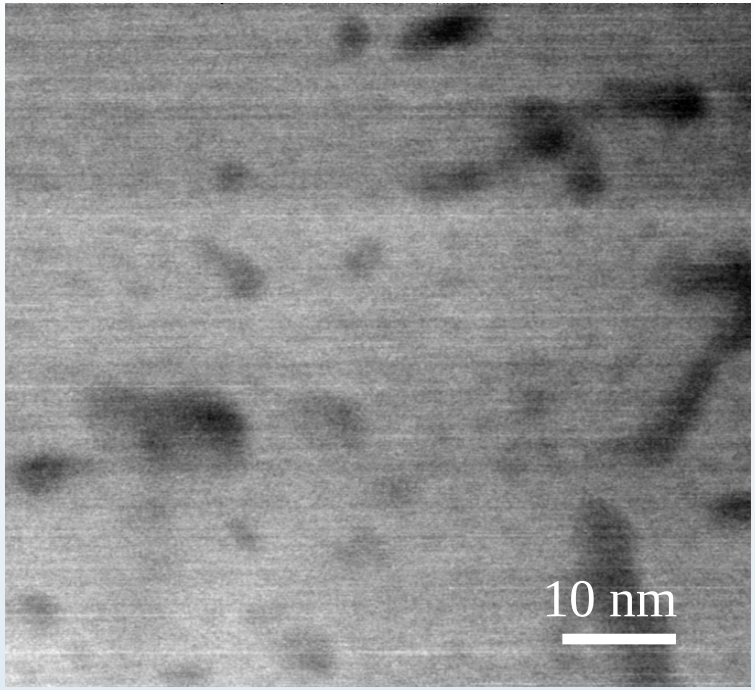
Z-contrast image



Single-Crystal CIS

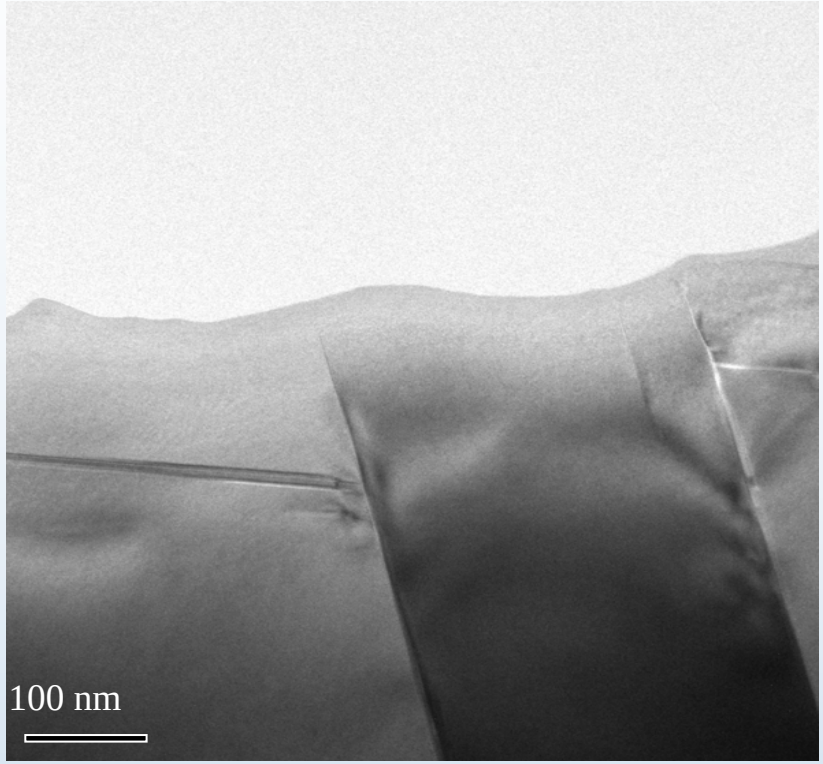


HRTEM

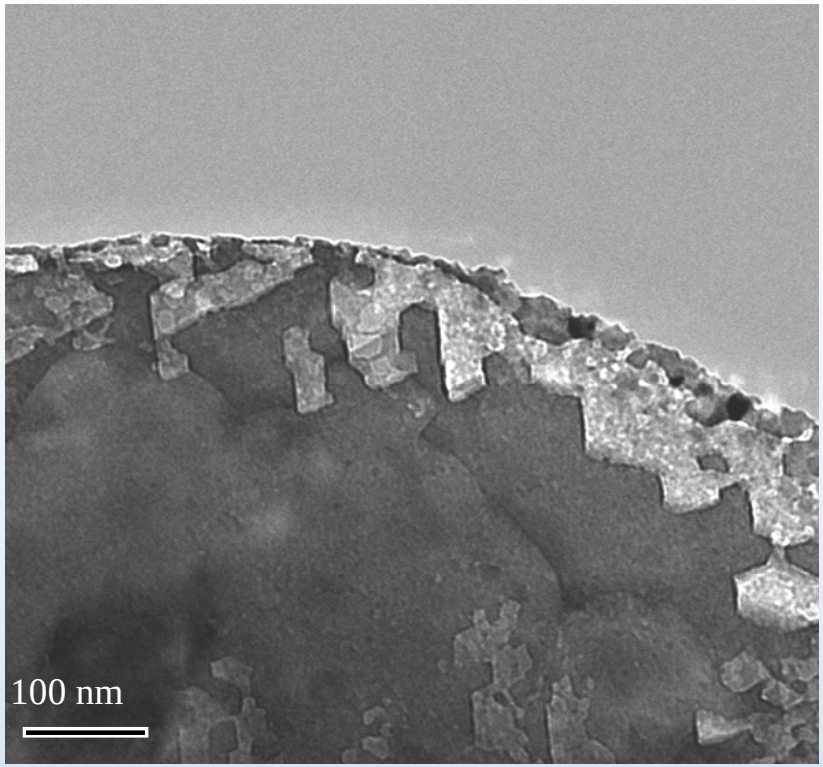


Z-contrast image

Ion-Beam-Induced Decomposition in CIGS



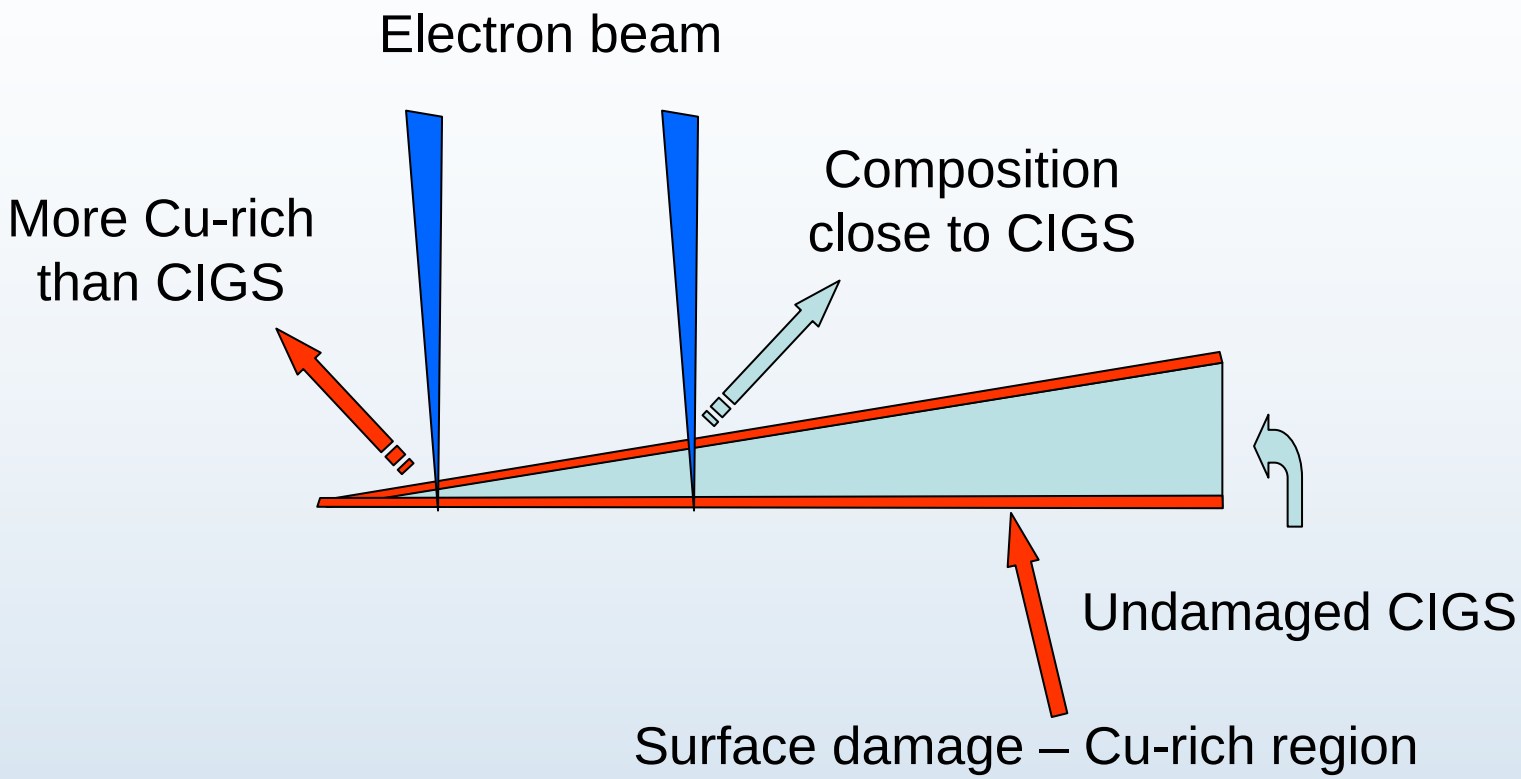
Thick region



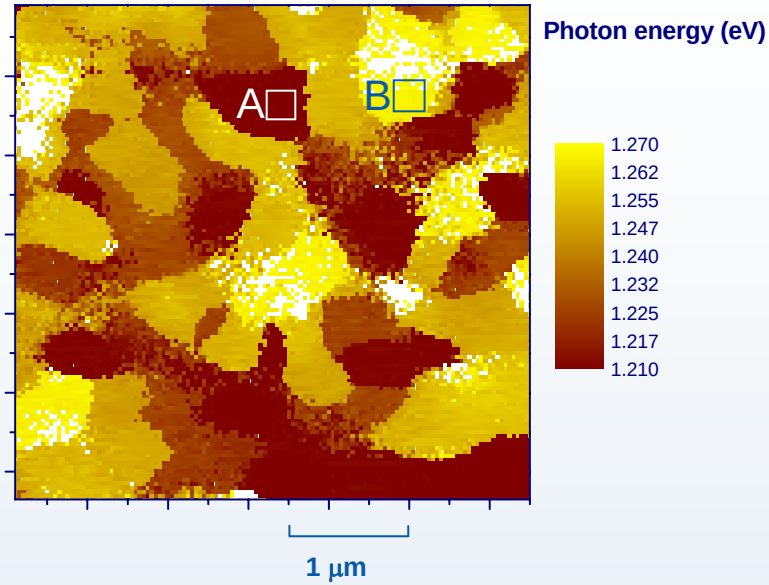
Thin region

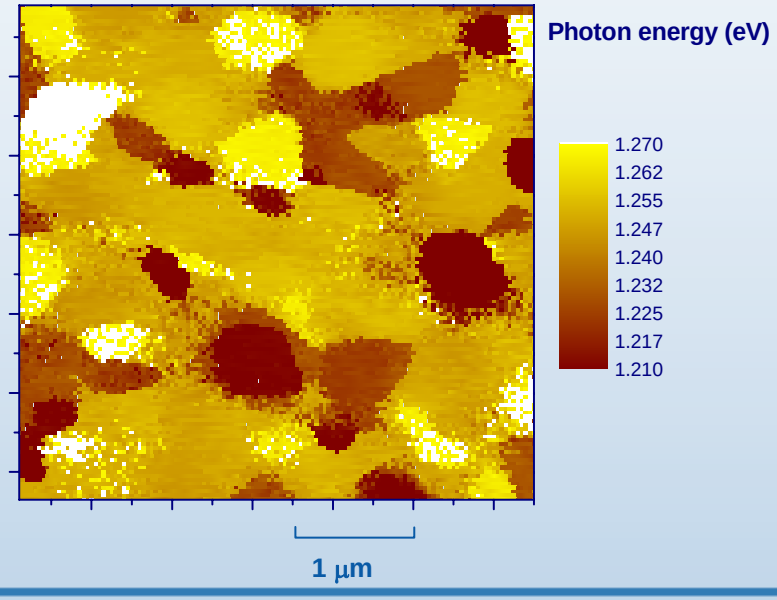
Dual Mill L-N_2, 2.4 kV, 7 degree

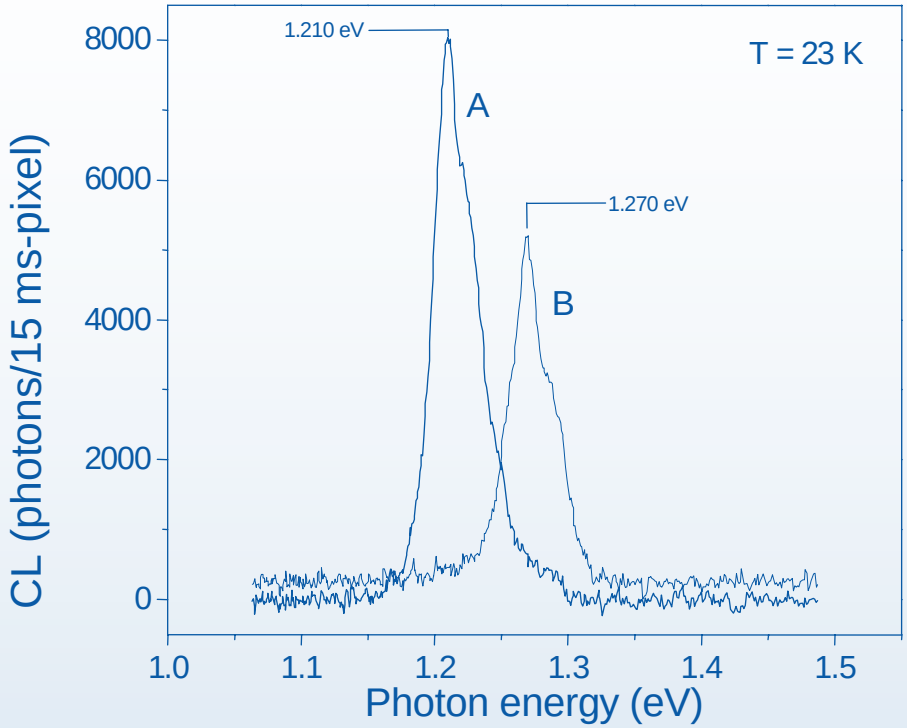
Surface Damage by Ion Beam



Cathodoluminescence of <112> CIGS Film







Spectrum imaging from C1899: CIGS thin film of <112> orientation.
E_b = 10 keV, I_b = 2 nA, T = 23 K.

Nanodomains in CIGS

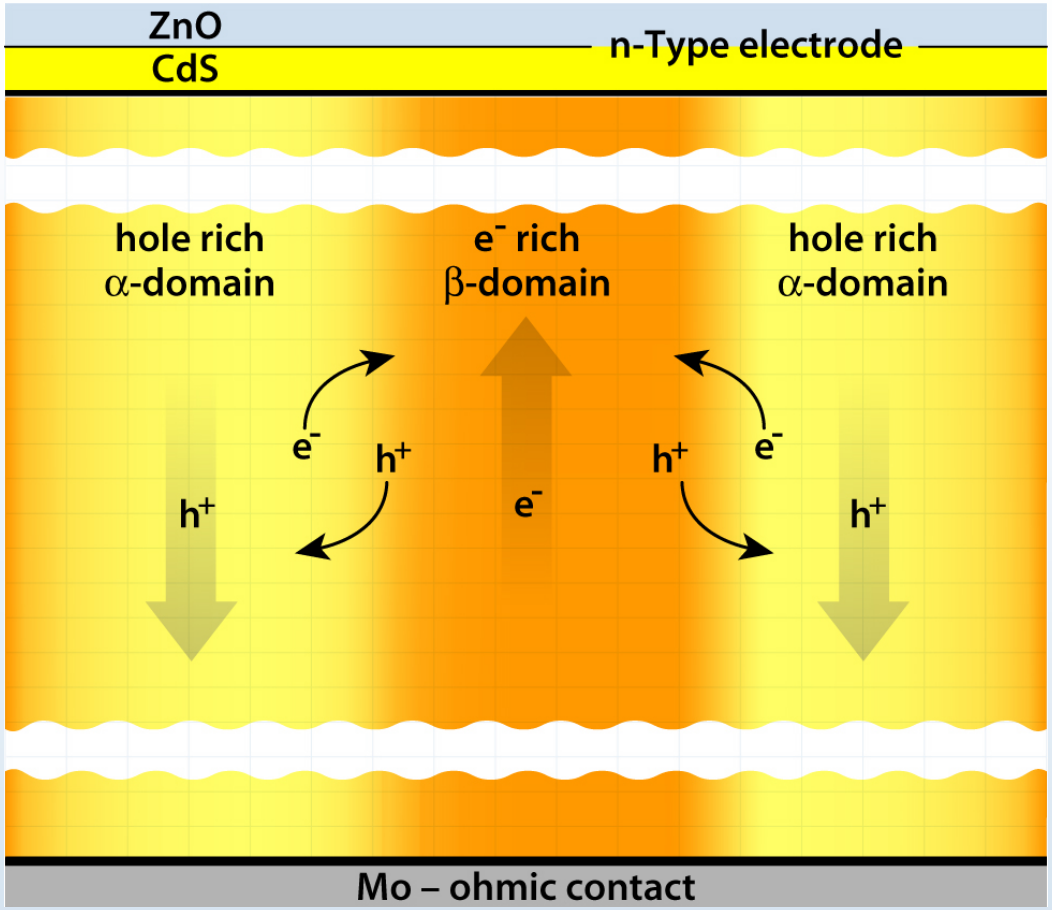
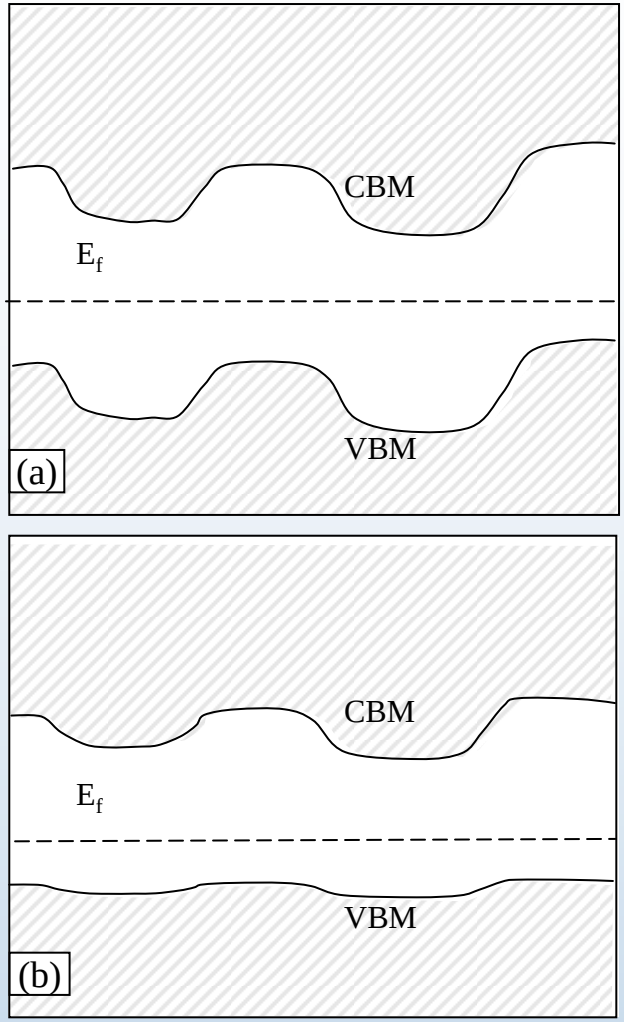


Illustration of α- and β-like nanodomains. The interior of the grain is composed of a network of domains in three dimensions.

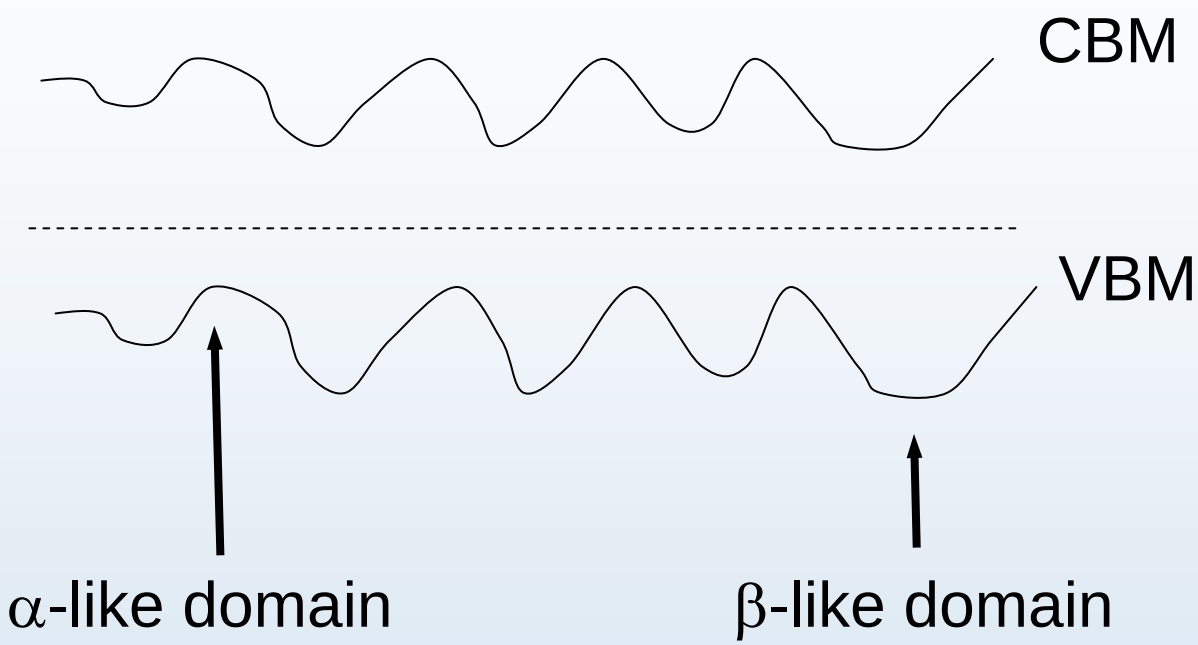
Fluctuations due to V_{Cu} and Ga



(a) V_{Cu} preferentially segregates to β-phase, lowering VBM

(b) Ga in CIS preferentially segregates to α-phase, raises CBM, increases E_g

Band Diagram for Nanodomains



Nanodomains may have different CBM positions and E_g, thereby inducing potential fluctuations

Summary

- We find chemical fluctuations at the nanoscale, which result in Cu-rich and Cu-poor nanodomains.
- Nanodomains are crystallographically coherent.
- The nanodomains may interconnect to form a three-dimensional network.
- Such nanostructures may play a role in device performance.

We encourage other laboratories to pursue similar investigations for corroboration.

PRESENTATIONS FROM

V_{OC} MINI WORKSHOP

PRESENTATIONS FROM

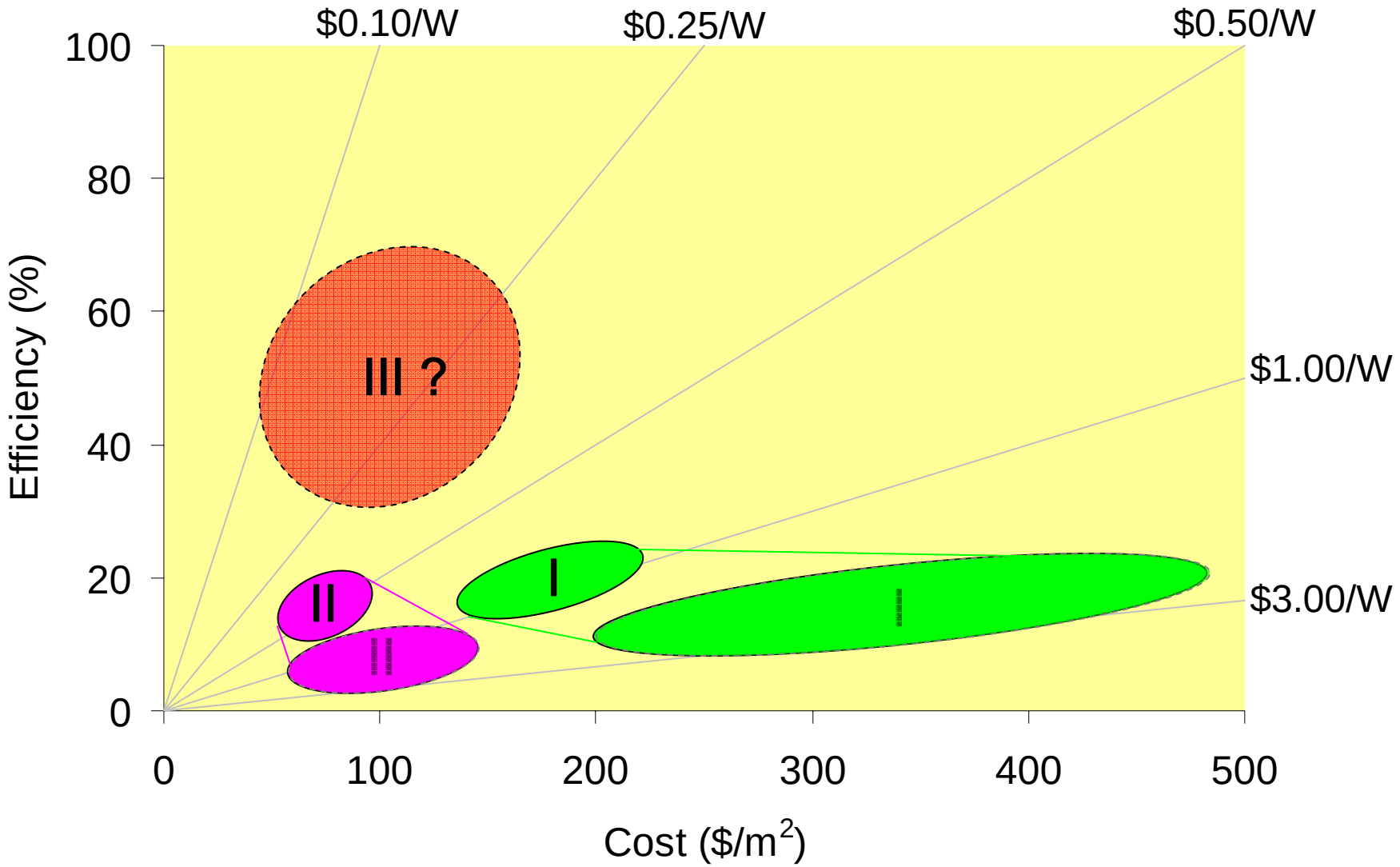
V_{OC} MINI WORKSHOP

CdTe
V_{OC} mini-workshop

Introduction

March 10, 2006

PV Technologies - Generations



V_{OC} mini-workshop

- Goals
  - Raise team awareness of V_{OC} limiting issues
  - Collectively develop list of ideas for raising V_{OC}
- Format
  - Device physics perspectives on V_{OC}
    - Limitation to V_{OC} and possible work-arounds
  - Cell fabrication perspectives on V_{OC}
    - Cell grower survey results
    - What has been tried to date and new ideas to try
  - Team discussion on raising V_{OC}
    - Elaborate and clarify ideas
    - Consensus on best ideas to try
      - Impact, likelihood of success, effort to try
      - Evolutionary vs revolutionary
    - Evaluation Survey

V_{oc} workshop: Back contact and Nonuniformity

University of Toledo

Presented by V. G. Karpov

Contributions by:

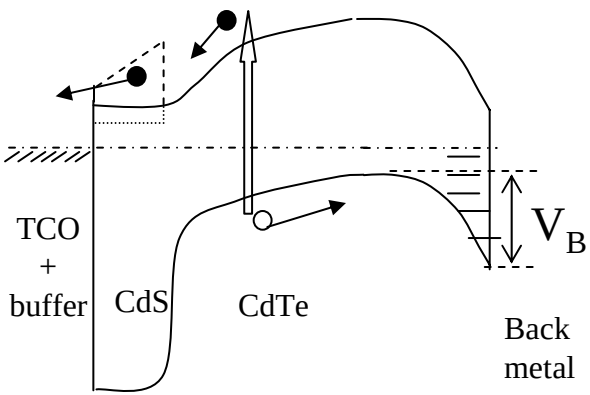
D. Shvydka, Y. Roussillon, J. Drayton,

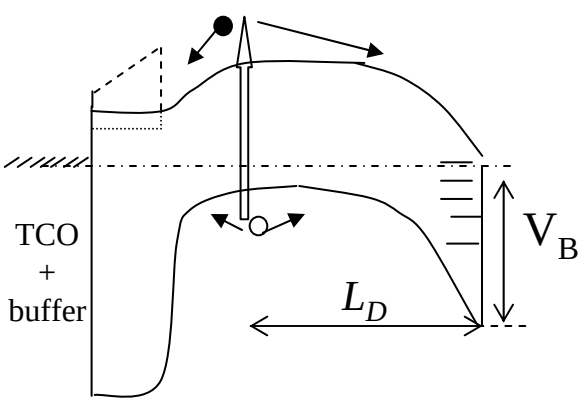
D. M. Giolando, and A. D. Compaan

Outline

- BC average parameters and effects on Voc
- Nonuniformity in general: weak diode
- Nonuniformity in BC: reach-through diodes
- Other Voc observations
  - Correlation Voc/FF/Eff
  - Surface doping
- Action items

BC as a classical Schottky barrier

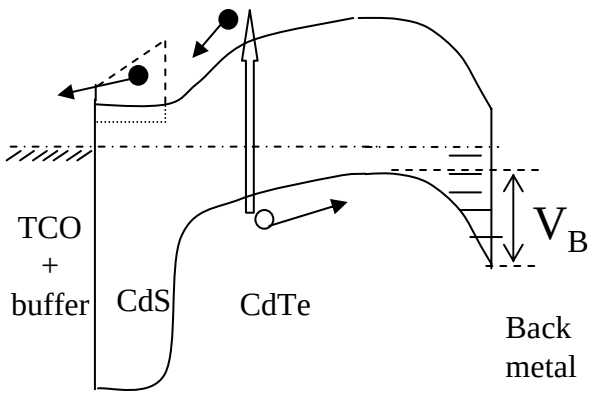




- BC => Back barrier => Loss
- V_B = W – work f-n difference
- L_D = depletion width
- Defects in BB help
- BC kills Voc when affects main junction

In reality all the metals are almost equally bad BC unless special treatments applied

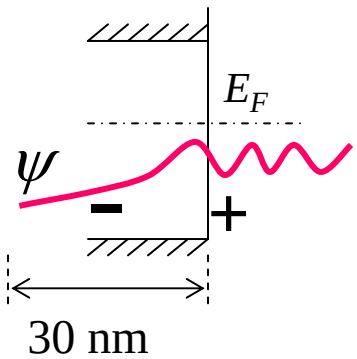
Work function may be irrelevant
Different physics



No V_B/W correlation : V_B=1 eV
(W. Jaegermann et. al. MRS, **865**, F6.1.1 (2005))

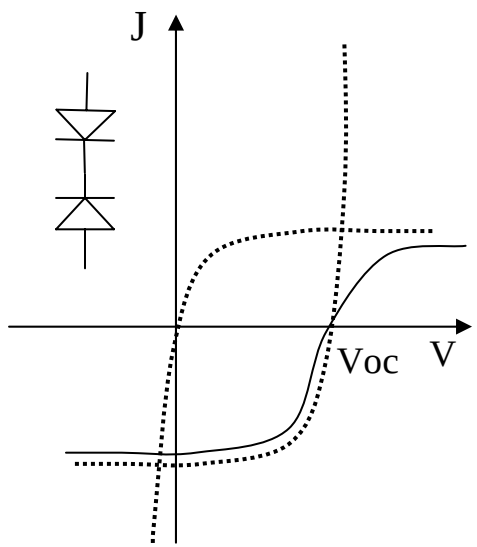
Interfacial defects? – possible

Metal Induced States – new insight
see T. C.G. Reusch et. al. PRL, **93**, 206801 (2004)



- Electron wave functions from metal into semiconductor
- Back barrier thinner than depletion width
- Electronegativity more relevant than W [J. X Tang et. al. APL, **87**, 252110 (2005)]

If so, BC shouldn't affect Voc. Facts

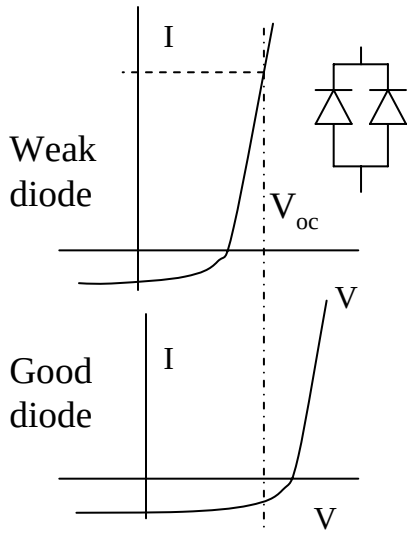


- BC affects Voc in devices with strong main junctions (high SPV):
~ 200 mV < Voc < ~ 850 mV,
Voc ≤ SPV

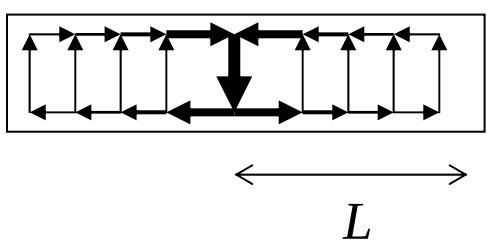
- BC is less important with weak junction devices (low SPV):
Voc = SPV, say 400-600 mV

Difference between SPV and Voc indicative

Voc loss can be nonuniform
General nonuniformity concept



- Weak diode is a sink for a large ($L^2 \sim 1\ cm^2$) area
- It does not shunt reverse bias (doesn't affect Rsh)
- Hurts Voc and FF, but not Jsc
- Steepness of JV curve matters

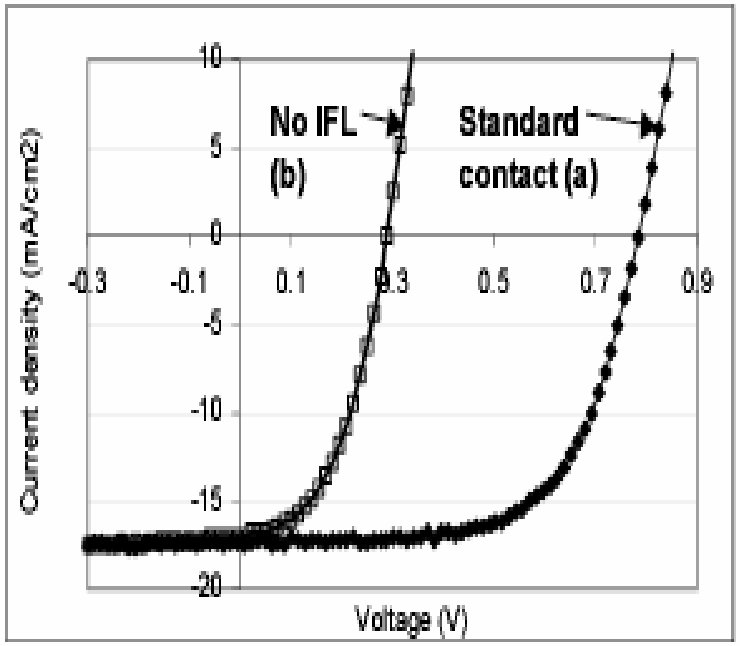


$$L = \sqrt{\frac{2kT}{j_0 \rho e} \ln\left(\frac{L}{l}\right)} \sim 5\text{–}10\text{mm}$$

V. G. Karpov, R. Harju, and G. L. Dorer
SPVC, IEEE Alaska, p. 555 (2000)

V. G. Karpov, A. D. Compaan and D. Shvydka,
PRB, **69**, 045325 (2004); Sub-team CDROM (2005)

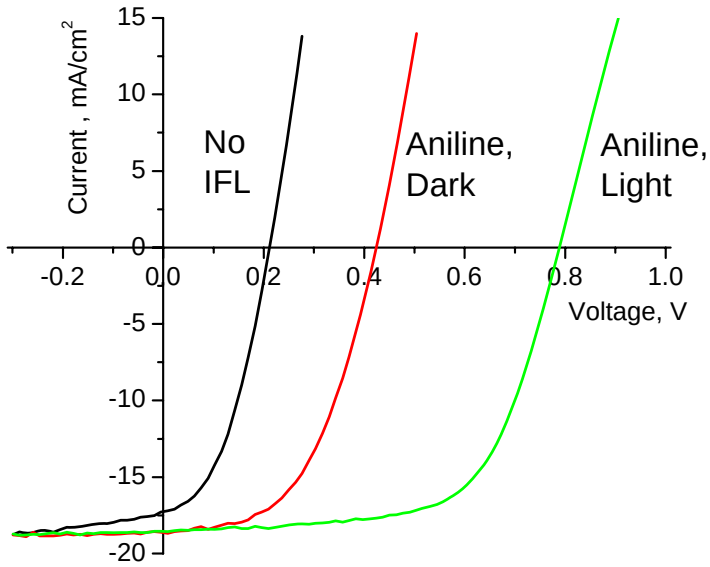
IFL effect and metal removal mystery

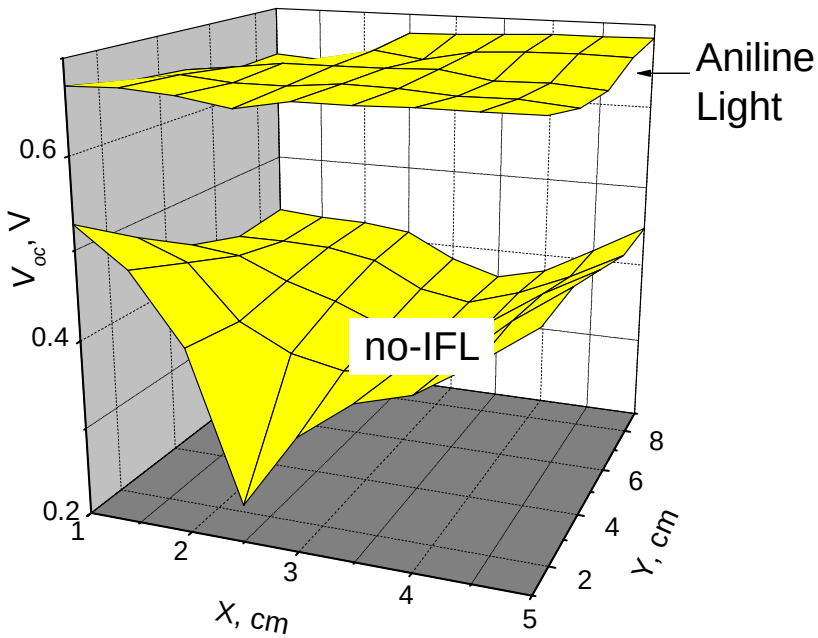


- ".. omission of IFL in BC results in Voc suppression of 500 mV.
- .. when the metal layers of the low Voc cell were physically removed, the SPV was ~780 mV.
- .. Voc suppression only occurred with the metal layers on.
- .. Voc suppression is from small areas with high forward current."

D. Rose, R. Powell, U. Jayamaha, and M. Maltby, SPVC, IEEE New Orleans, p. 555 (2002)

Similar results by red wine/aniline IFL: no-IFL samples nonuniform, low Voc



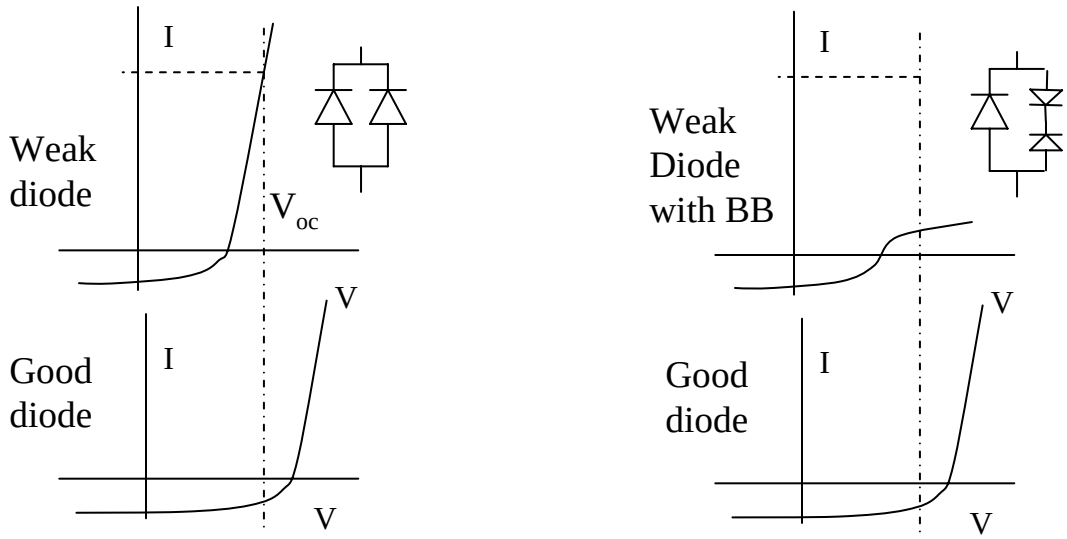


Aniline/red wine IFL effects on Voc

Y. Roussillon et. al. APL, **84**, 616 (2004)

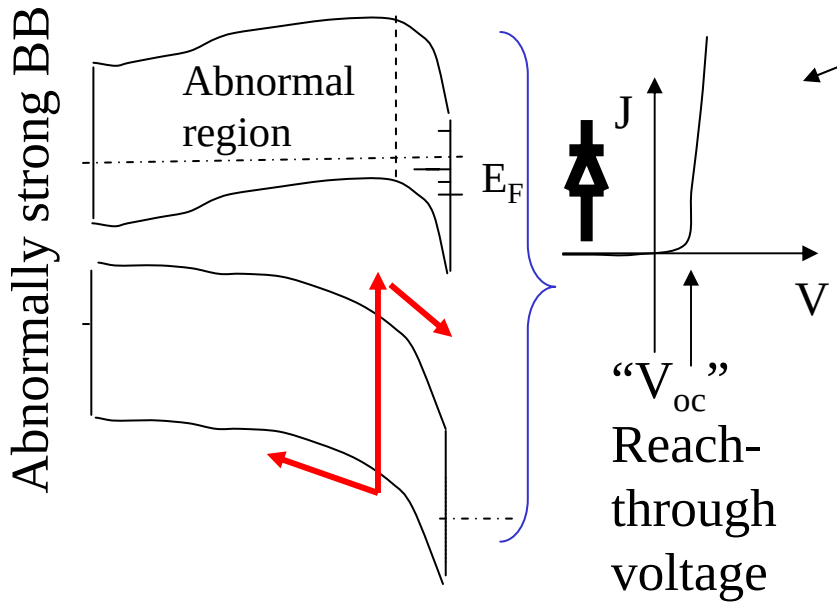
Voltage maps for two halves of the same substrate (5nm Cr BC). IFL vs. no-IFL

Moderate back barrier should help



Back diode helps by blocking forward current

Locally strong back barrier hurts: reach-through diode (RTD)



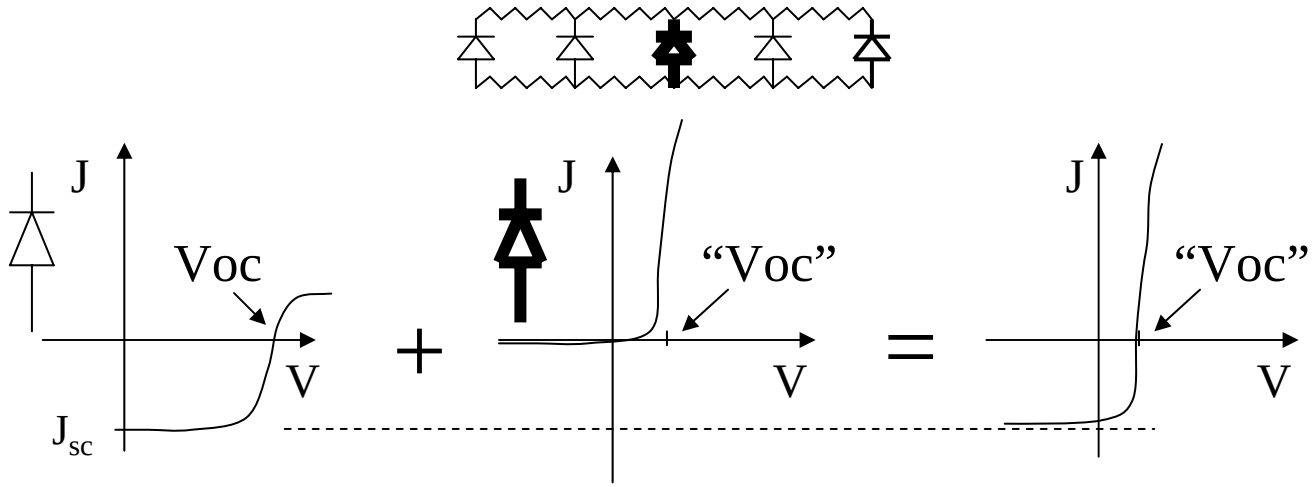
- Very high forward current (up to tenths of A)
- No rollover

Apparent "Voc":
- Doesn't depend on light intensity,
- Depends on BC treatments
- Lower than good device Voc.

High electron (not hole) forward currents in local spots of abnormally strong back barrier;

Y. Roussillon et. al, JAP, 96, 7283 (2004)

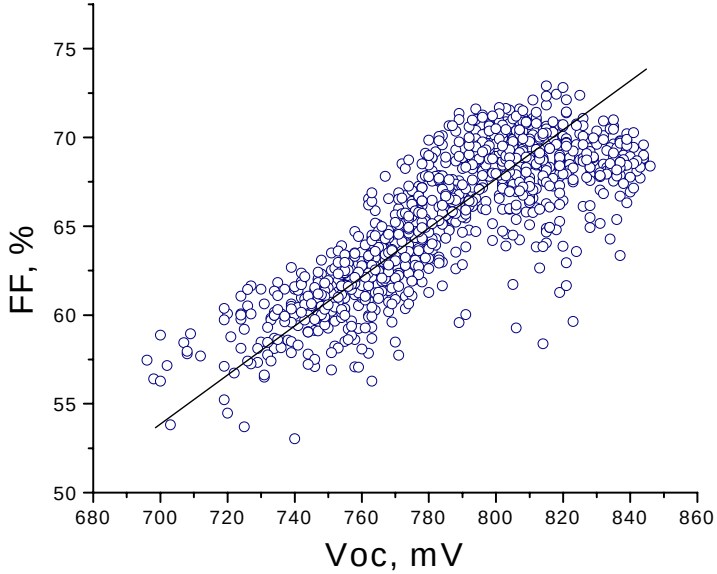
RTDs are very efficient weak diodes: avoid bad spots in the back surface



Predictions for RTD "bad" back contacts:	**Verification**
• Low Voc independent of light intensity;	yes
• No rollover;	yes
• Repealing metal returns high SPV;	yes
• No such effect for low Voc devices: Voc<"Voc".	yes

Y. Roussillon et. al, JAP, 96, 7283 (2004)

Other Voc observations: Voc/FF correlation and nonuniformity



~ 1000 fresh and degraded cells

[See: V. G. Karpov, A. D. Compaan and D. Shvydka, APL, 80, 4256 (2002)]

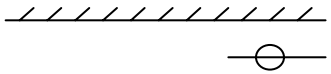
	EFF	*Voc*	*FF*	*Jsc*
EFF	1			
Voc	0.82	1		
FF	0.87	0.77	1	
Jsc	0.58	0.14	0.19	1

Correlation coefficients

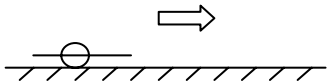
Correlation FF/Voc;
Disconnected Jsc.
Typical of weak diodes

Other Voc observations: surface doping

Doping problem: self-compensation. Too flexible atomic system: Low defect creation energy overbalanced by the hole deepening.

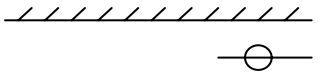


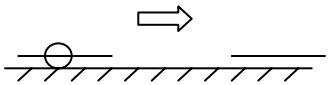
Either A



Shallow acceptor evolving into deep defect

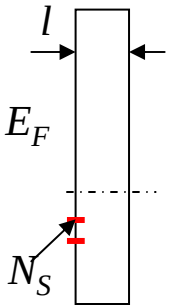
or B





Independent defects in response to extra holes

For thin films, surface states can be effective dopants in case A, provided the surface is less flexible.



$$N_A = N_S / l$$

See J. J. Boland, Nature, **439**, 671 (2006);
P. Zhang *et. al*., *ibid*., p. 773;
V. G. Karpov, NCPV 2004

Action items vs. device model

Nonuniformity, BC, Surface doping

↓

- Work on uniformity: avoid pinholes, wet treatment spots, etc.
- Passivate/dope surface
- Use buffers, IFLs

Defect chemistry, Bulk doping, SRH

↓

- Dope CdTe: try T, P, U, etc., co-dopants
- Think of SRH (?)
- Measure defect states (PL, CVF, etc)

These items are not mutually exclusive

Conclusions

- BC physics may be different (quantum mechanics, electronegativity, thinner barrier,…)
- Average BC parameters may be irrelevant to Voc
- Nonuniformities strongly affect Voc
- BC nonuniformities especially detrimental (RTD)
- Surface doping may be another venue to Voc
- Action items depend on device model

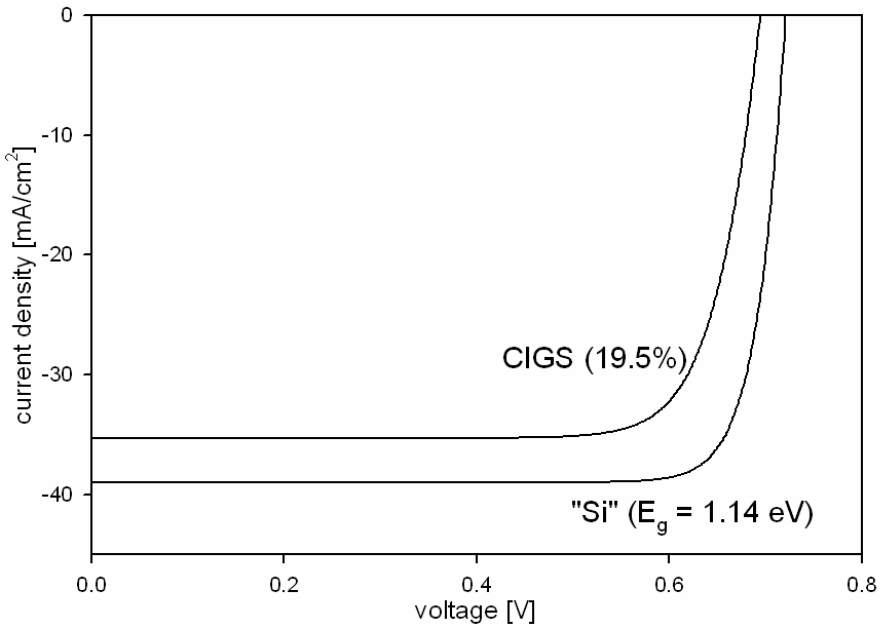
Can V_{OC} for CdTe Cells be Increased Significantly?

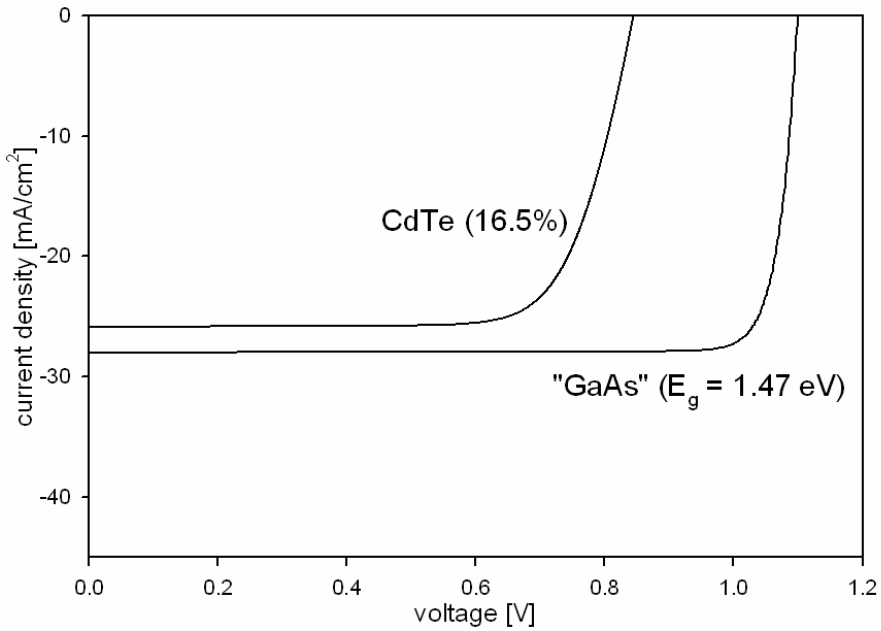
Jim Sites and Jun Pan
Colorado State University

with advice from Markus Gloeckler, First Solar

Comparison of CIGS and CdTe to Single X-tal Cells

Comparison of record efficiency cells



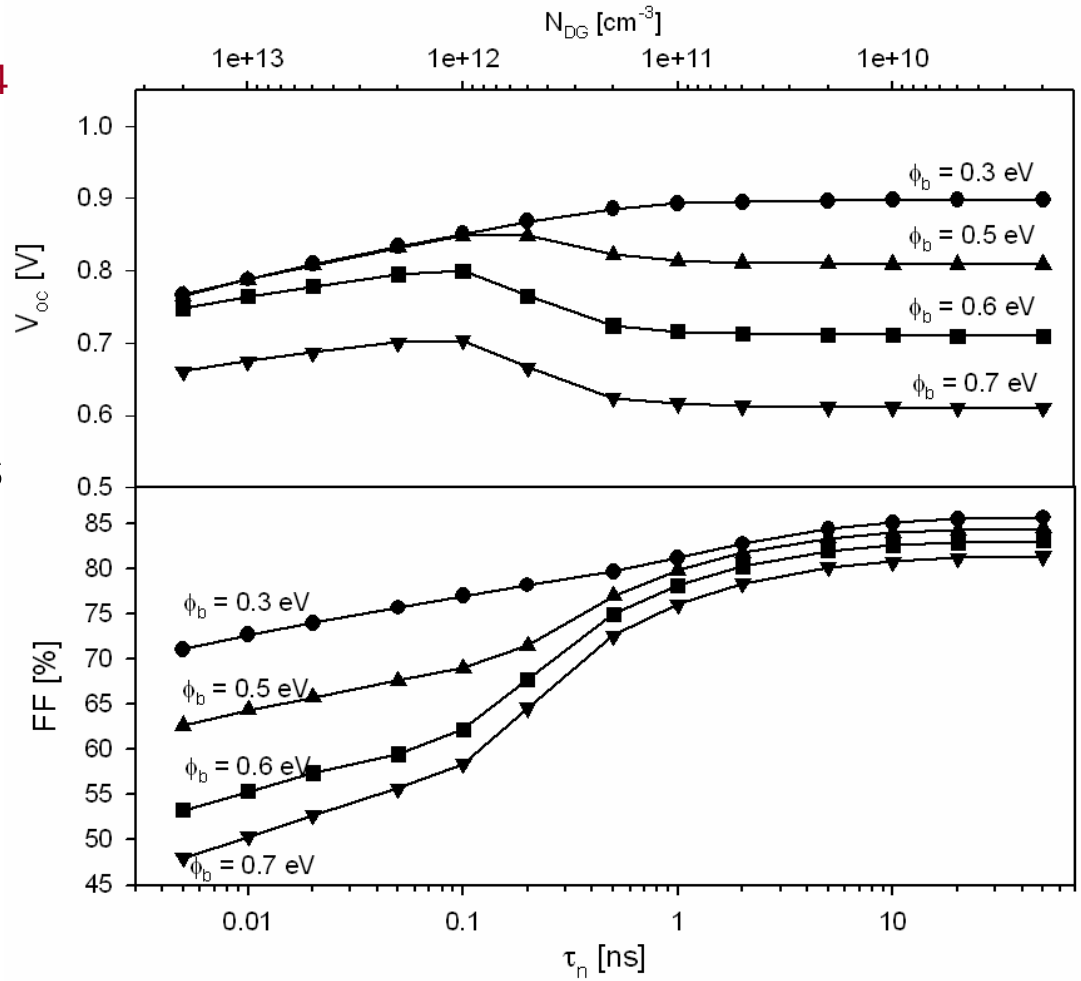


In both cases, the band gap of the crystalline cells was adjusted slightly to match CIGS and CdTe. Hence the labels “Si” and “GaAs”.

Variation in V_{OC} and ff with lifetime and barrier

Hole density: 2×10^{14}

Simulations used AMPS and assumed parameters similar to our baseline for high efficiency cells.



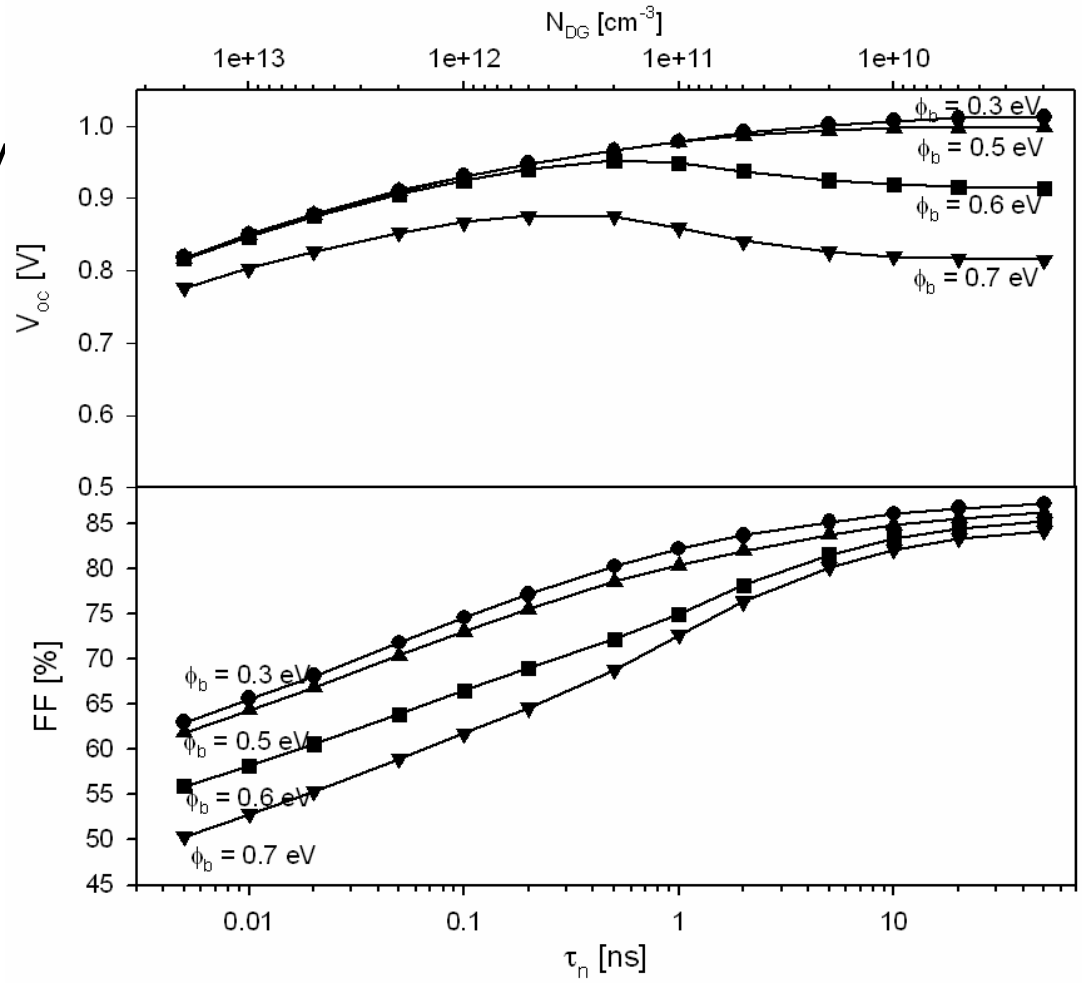
Variation in V_{OC} and ff with lifetime and barrier

Hole density: 2×10^{16}

Voltage increase >100 mV

Simulations used AMPS and assumed parameters similar to our baseline for high efficiency cells.

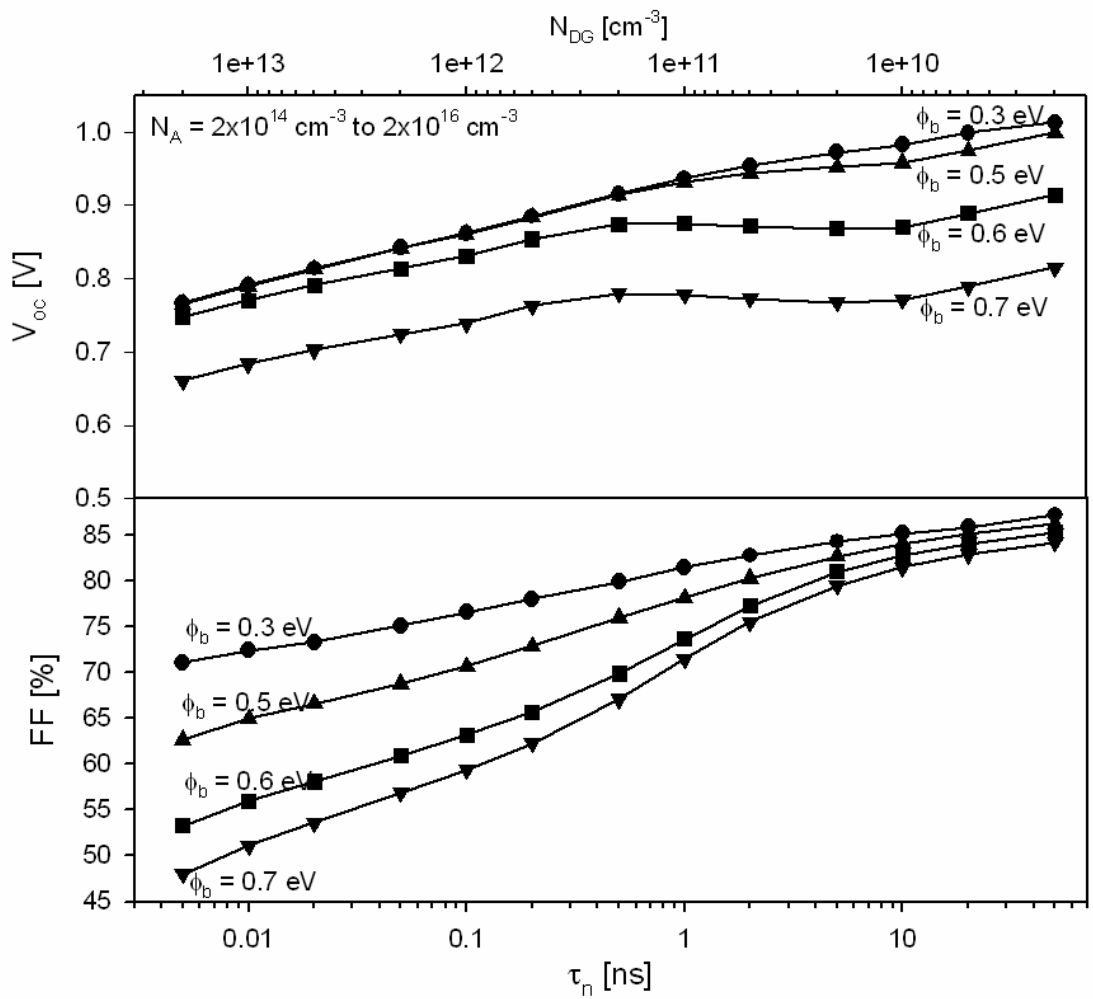
To get GaAs voltage, still higher hole density would be needed.



Variation in V_{OC} and ff with lifetime and barrier

Let the trap density determine p, i.e. let them track together.

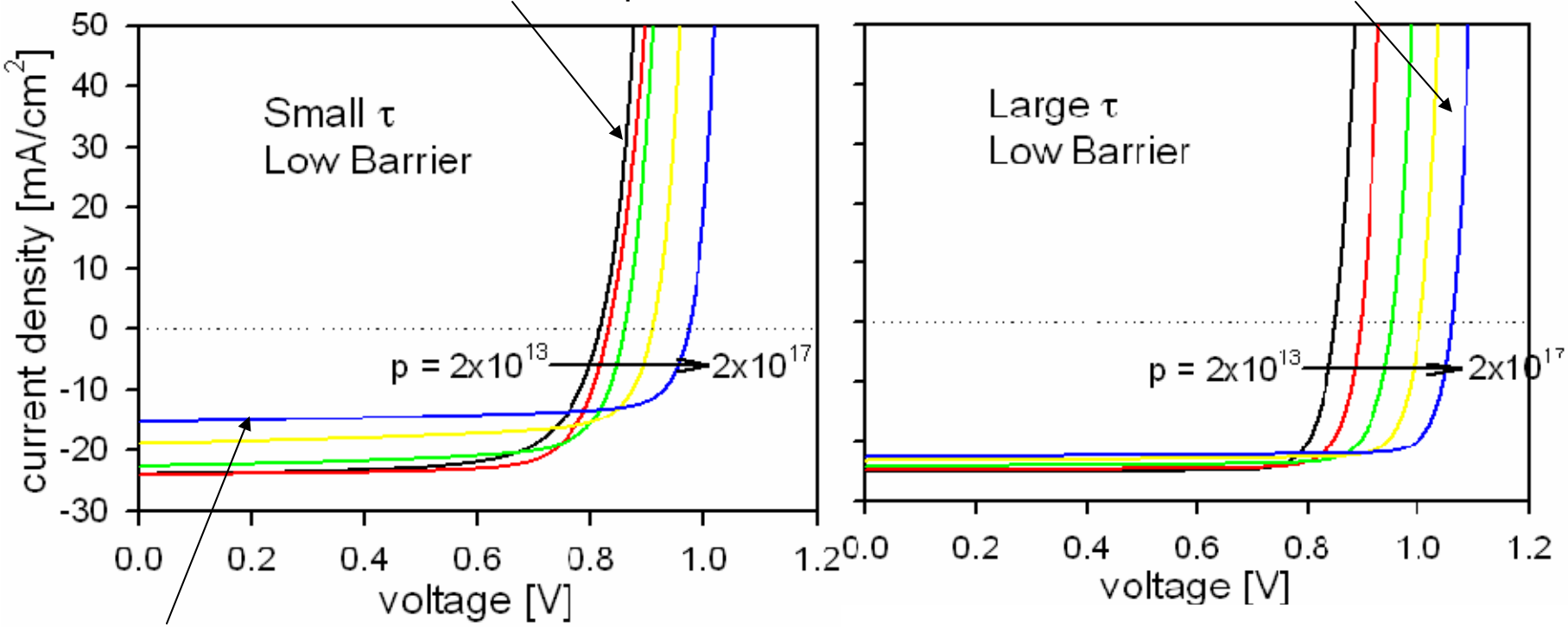
Probably more physical, because a decrease in trap density reduced compensation, and hole density should increase.



Full Current-Voltage Curves

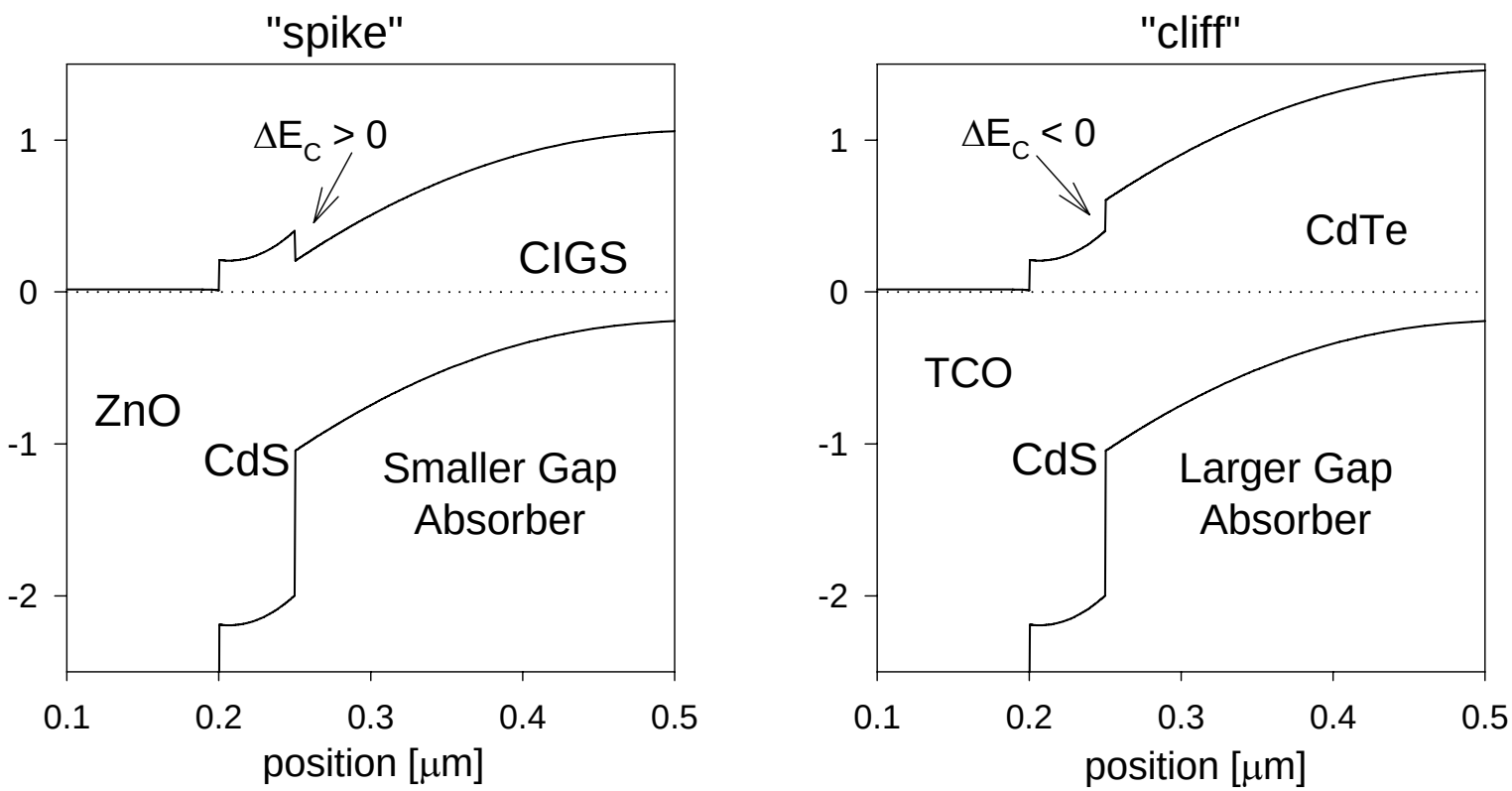
Starts at lower voltage; initial curves more bunched up.

Approaching GaAs



Small depletion width and small lifetime mean reduced collection.

Conduction-Band Offset ΔE_C



Spike can impede photoelectrons (bad if too big)

Cliff slows forward electrons in interfacial-recombination region (also may be bad)

Some consensus on ΔE_C magnitudes between theory, experiment, and numerical simulations of J-V curves

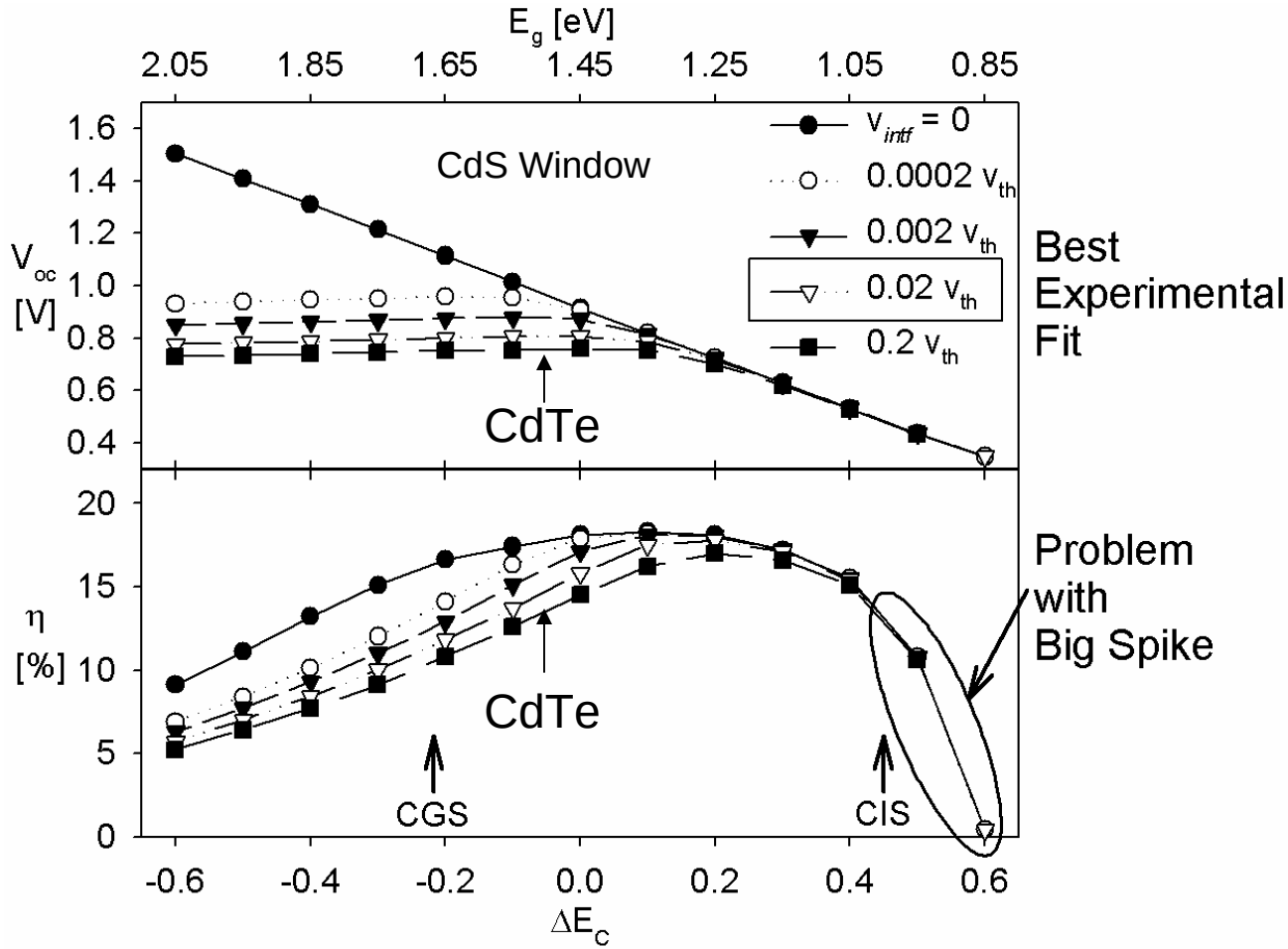
Effect of Interfacial Recombination on V_{OC}

Vary ΔE_C by expanding E_g (simulated)

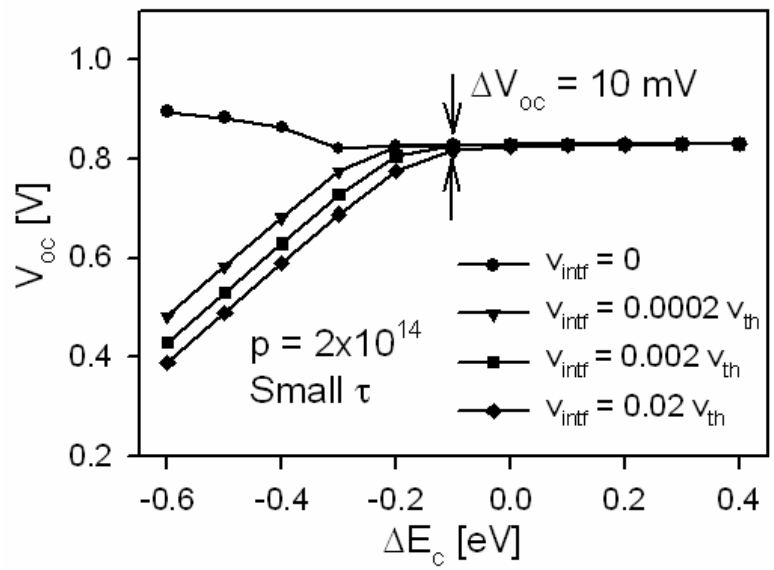
Lack of spike allows significant interfacial recombination

Effect of ΔE_C at constant E_g discussed by several groups

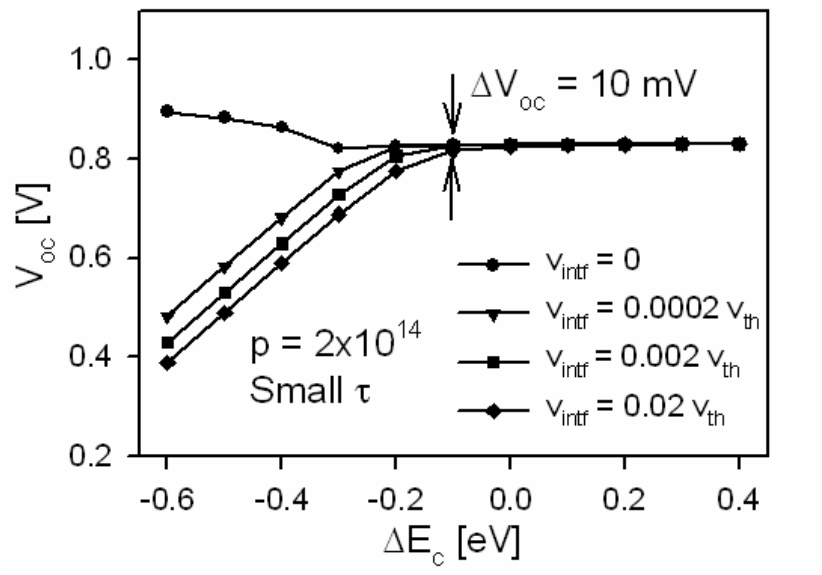
CIGS hole densities used here.

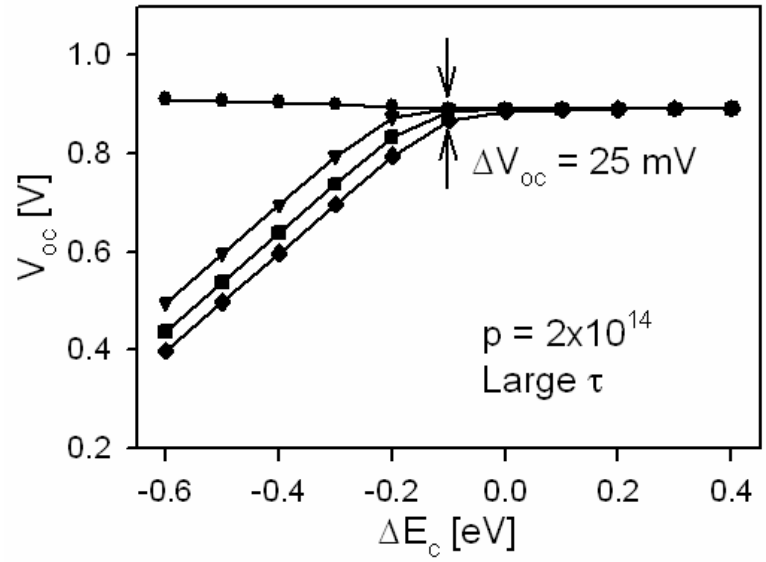


Effect of Conduction-Band Offset on V_{OC}

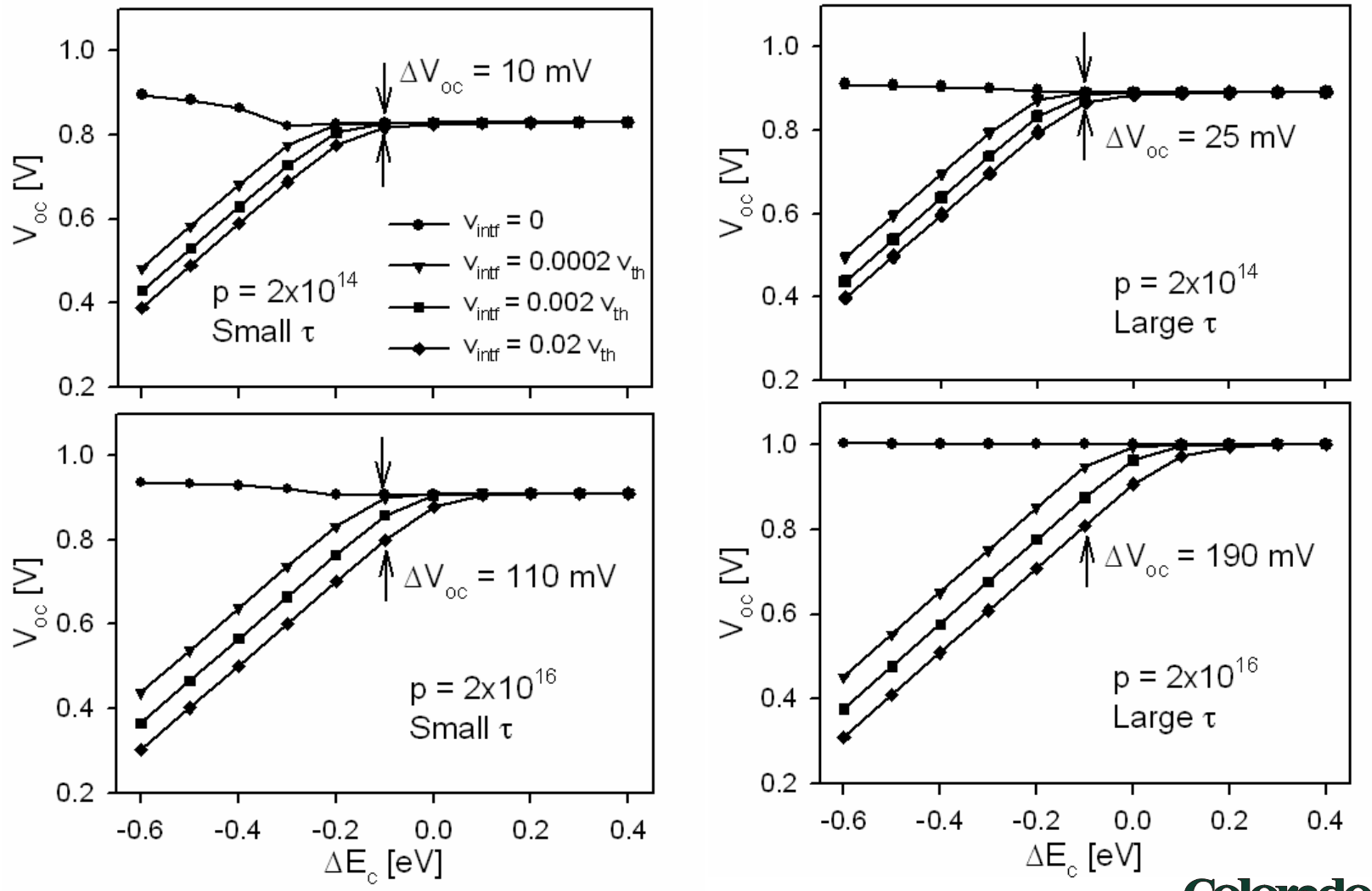


Effect of Conduction-Band Offset on V_{OC}





Effect of Conduction-Band Offset on V_{OC}



Thin CdTe?

If CdTe hole density can be increased to the CIGS range, is it possible to thin the absorber below one micron?

One issue, obviously is uniformity.

Another is whether an electron reflector can be constructed. With CIGS, nature is kind, and the pile up of Ga at the back produces an electron barrier. With CdTe, one needs an analog. ZnTe?

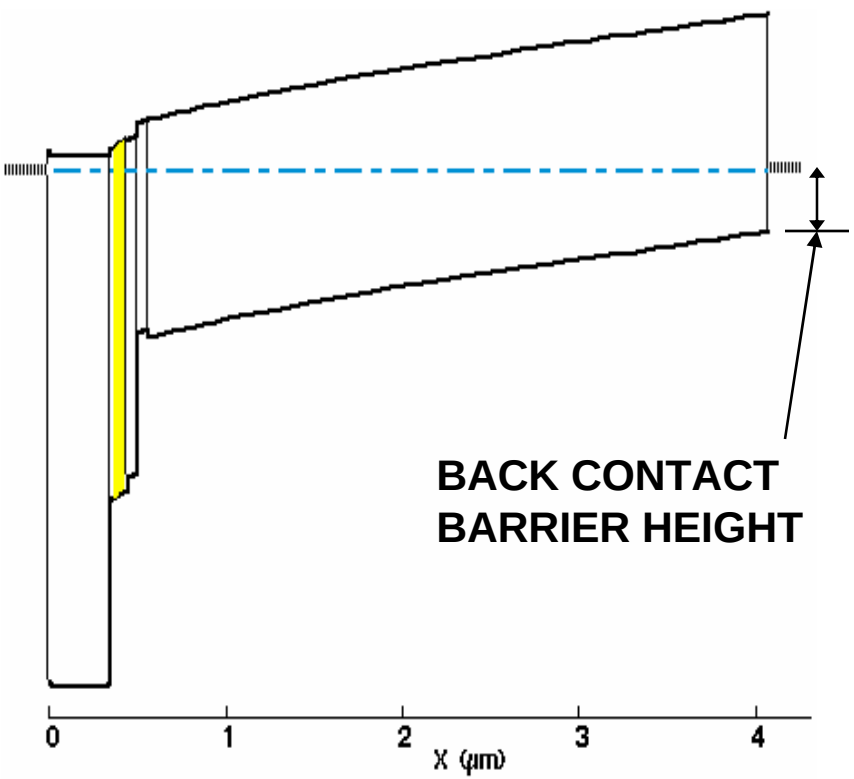
Conclusions

(1) CdTe voltage unlikely to increase very much unless hole density is increased.

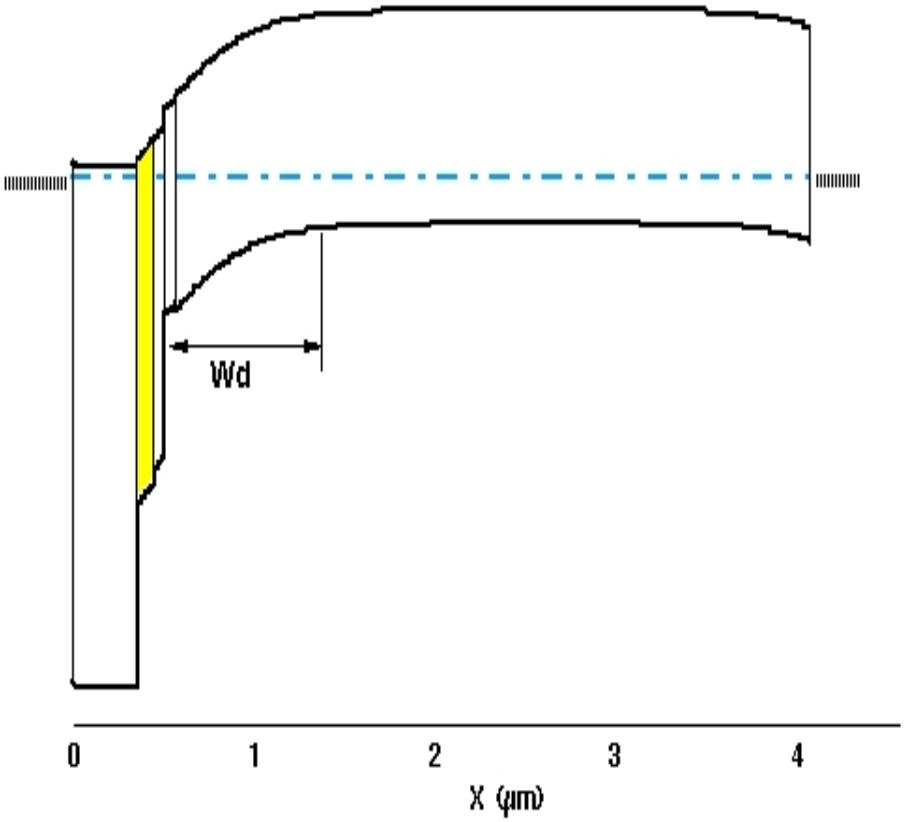
(2) High electron lifetime also needed, but fortunately a reduction in trap density should increase both lifetime and hole density.

(3) The CdS/CdTe conduction-band offset is not a significant voltage limitation at present. Unfortunately, it is predicted to become more of an issue if carrier density and voltage are increased.

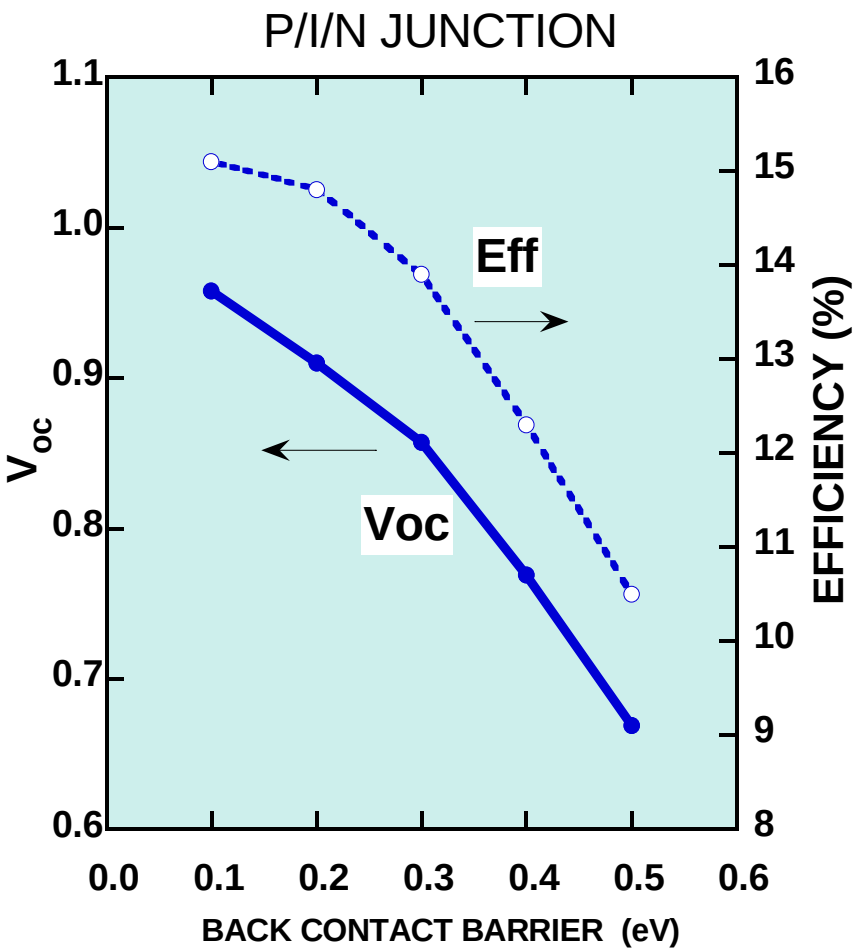
P/I/N JUNCTION

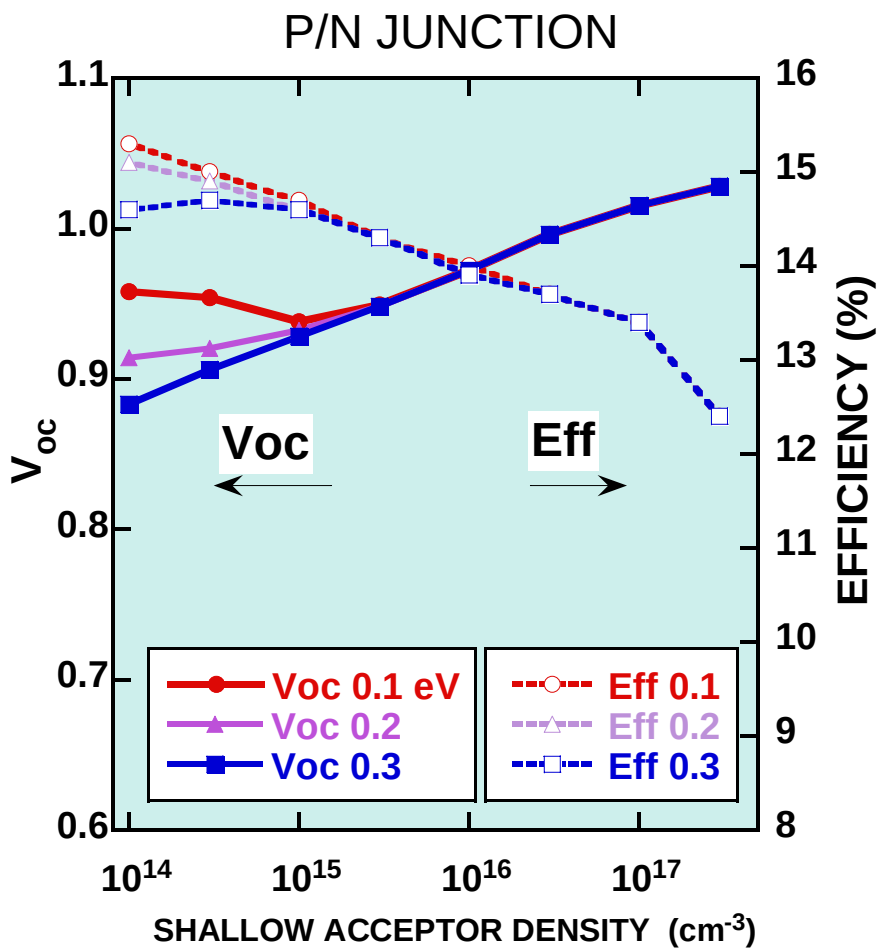


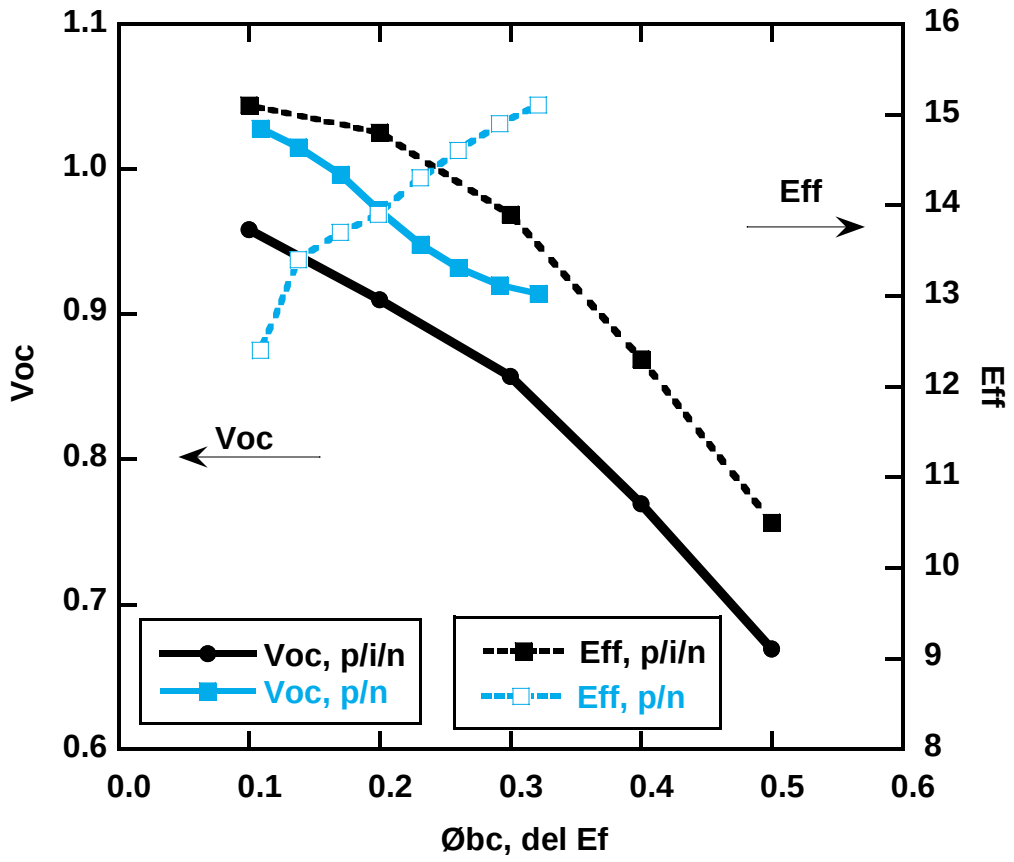
P/N JUNCTION



Both junctions have 1e14 acceptors and 1e14 donors at mid-gap (neutral recombination center set)
P/N junction also has shallow acceptors at 0.1 eV above valence band






1.1
1.0
0.9
0.8
0.7
0.6
Voc
16
15
14
13
12
11
10
9
8
Eff
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Øbc, del Ef
Eff
Voc
Voc, p/i/n
Voc, p/n
Eff, p/i/n
Eff, p/n

Fabrication perspective on open circuit voltage in CdTe/CdS thin film solar cells

Brian McCandless and Chris Ferekides

Voc survey questions

1. Where do you think the highest value lies with respect to attaining high Voc: defining realistic target Voc; achieving a single proof-of-concept result at-any-cost such as a loss in other J-V parameters or stability; establishing incrementally higher baselines and tightening distributions; developing more quantitative models to identify losses in present-generation devices; developing novel device designs; etc?
2. What do you feel are 1 or 2 approaches with the highest potential of success for attaining higher Voc in the near-term?
3. What do you believe limits Voc in present-generation devices (e.g., device design, uncontrolled parameters, fundamentals)?

Survey Responses - CSU AVA

1) Any increase in Voc should be achieved with manufacturing worthy process and hardware. In this mode 850 mV would be a good target.

2) HRT of buffer layers in production worthy low cost manner.

3) Possibly interface states pinning as shown by Darmstadt

Survey Responses - IEC

1) High priority in demonstrating control of properties to achieve Voc > 900 mV.

2) Doping.

3) Low doping and screening by back contact

Survey Responses - NREL (Albin)

1) There exists 2 major dichotomies in device structure/physics/behavior/stability. We have thin cells (1-2 um) and thick cells (>6 um) and also physical models we are centric to these as well as some differences as regards stability. We like thin devices in that they are more manufacturability and address availability issues, however the best performance is arrived at with the thicker cells. Can we blend what we know of these two approaches.

Survey Responses - USF

1) Voc at any cost = using potentially complex process.

2) Back contact (large work function).

3) $CdCl_2$-Cu-O based device has been fully optimized.

Survey Responses - CSM

V_{OC} challenges

Q.3: Complex interactions between processing steps front to back makes it difficult to identify root causes of V_{OC} limitations

Apparent ~850mV limit with current CdS/CdTe approach

Lack of run to run repeatability indicates V_{OC} sensitivity to parameters that are not well controlled

V_{OC} opportunities

Incremental/Optimization

Tighter controls on processing environment/parameters (T, P, concentrations, dust)

Reduce number of processing steps

Speed up fabrication turnaround time

Improve characterization diagnostics

Q.2. Possible ways to exceed 850mV

Alternate to CdS window layer

Surface/interface treatment to pin Fermi level

Increase absorber doping and passivate deep defects

Fabrication Survey Response

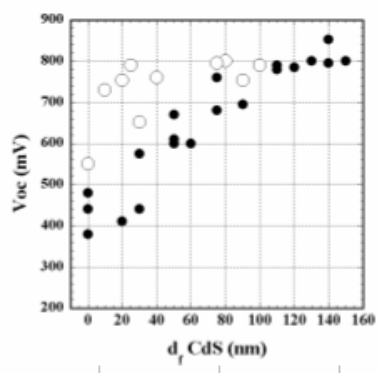
Microsoft Excel - ALL_Voc_Survey.xls

CdTe R&D Mini-Workshop on Voc

Survey of Solar Cell Fabricators: Superstrate CdTe/CdS Solar Cells
Experimental Evidence for Effect of Processing Parameters on Voc

ocessing Paramete	Glass	TCO (TEC15)	HRT	Process 1 (oxidation)	CdS (CSD/CBD)	Process 2 (treatment)	CdTe (VT)	Process 3 (treatment)	Process 4 (etch)	Cu (Evap)	Contact (Evap, printed)	Process 5 (treatment)
Phase/Material	SL	SnO2	SnO2, Ga2O3, In2O3		Hex/Cubic	Halide Vapor	Hex/Cubic	Group VIIA/VIA H	Surface Etch	Metal, CuI, CuCl, Ni, Au, ZnTe, ITO		
Effect on Voc	None	None	weak		Unknown	Strong	None	Strong	Weak	Weak	Weak	
How			unknown			Adhesion		Defect Chemistry	GB's, Bands?	Doping		
bient/Composition						CdCl2, Air	Oxygen	CdCl2/ZnCl2/O2	Many			
Effect on Voc					None	Moderate	Weak	Moderate	Weak			
How						Adhesion	Morphology	Defect Chemistry				
Sheet Resistance			>1000									
Effect on Voc	None	None	Weak		Unknown		Unknown					
How												
Thickness			10-100 nm		<100 nm		1.5-10 microns			1-10 nm		
Effect on Voc			Moderate		Strong		Weak			Weak	None	
How			Coverage		Coverage							
ocess Temperature				400-600C		350-450C	500-600C	350-500C				150-200C
Effect on Voc			None	Strong	None	Moderate	Weak	Strong				Weak
How				Oxidation		Adhesion		Time Dependent				Time-Dependent
Growth Rate							1-80 micron/min					
Effect on Voc					None		Weak					
How							Unknown					

Voc versus final CdS thickness in PVD CdS/CdTe cells: with HRT (open) and no HRT (solid)

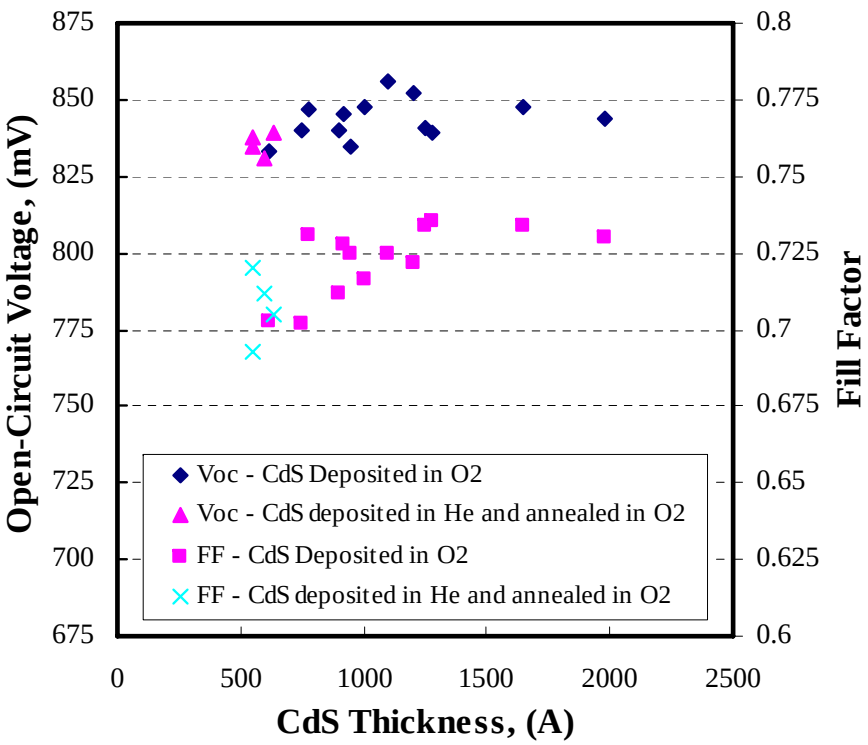


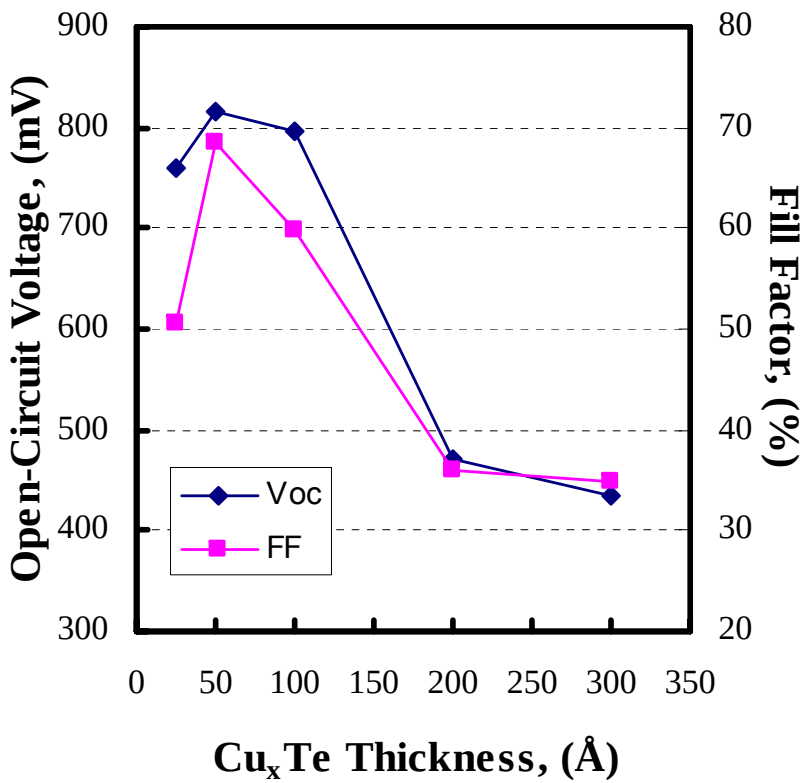
CSM-GasJet / CSM-Fig A / CSM-Fig B / CSM-Fig C / CSM-Fig D / CSM-Fig E / CSM-Fig F / IEC-VT / NREL-Albin / NREL-Wu / USF

Supporting slides

Survey Responses - USF

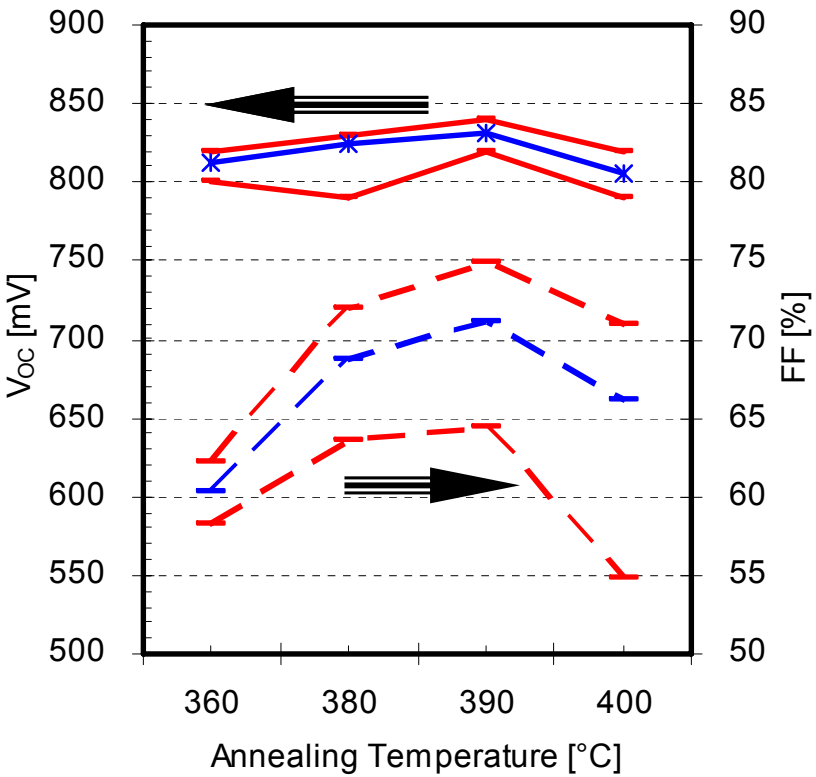
CdS Thickness ..... Cu

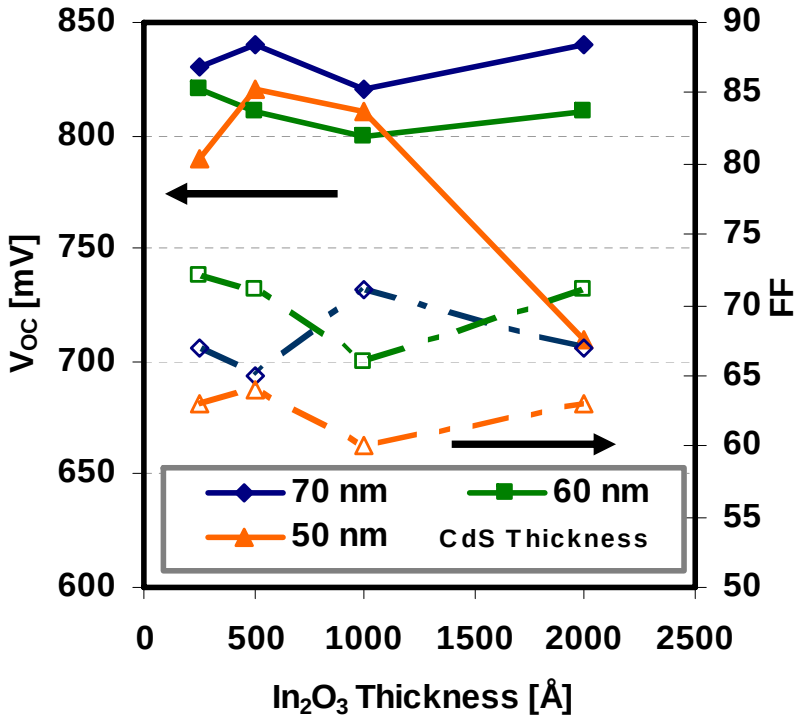




Survey Responses - USF

$CdCl_2$ Treatment ..... Buffer





Survey Responses - USF

Improving V_{OC}

Two options: (a) controlled (increased) doping or (b) better contacts

KEY DIFFICULTY with CdTe: Interdependence of essentially all processes

CdTe vs. CIGS

CIGS: co-evaporation allows precise control of stoichiometry/gradients etc. (Na effects)

CdTe: any deposition process + $CdCl_2$ leads to improved interface (low T processes) and CdTe bulk properties; simpler process BUT are the absorber properties "locked in"?

CIGS: once absorber is deposited/synthesized, remaining processing steps influence the junction region only (to first order) and back contact/absorber interface is unaffected.

CdTe: Back contact process (Cu based) has a significant impact on CdTe and CdTe/CdS interface (via Cu-diffusion). Cu works BUT adds to the complexity and difficulty of independently controlling the various device regions/properties.

Survey Responses - USF (contd)

How Do We Improve V_{OC} ?

Should we be talking about this without also considering options to decouple the various device processes ?

Controlling net ***carrier concentration*** in CdTe complex process:

- no evidence of effective doping of thin films to-date
- can we attain the necessary transport properties w/o $CdCl_2$
- possibly co-doping i.e. $CdCl_2$ + another impurity (?)
- effective in-situ doping may require the use of co-evaporation (i.e. CdTe+Cd) to achieve effective dopant incorporation conditions.

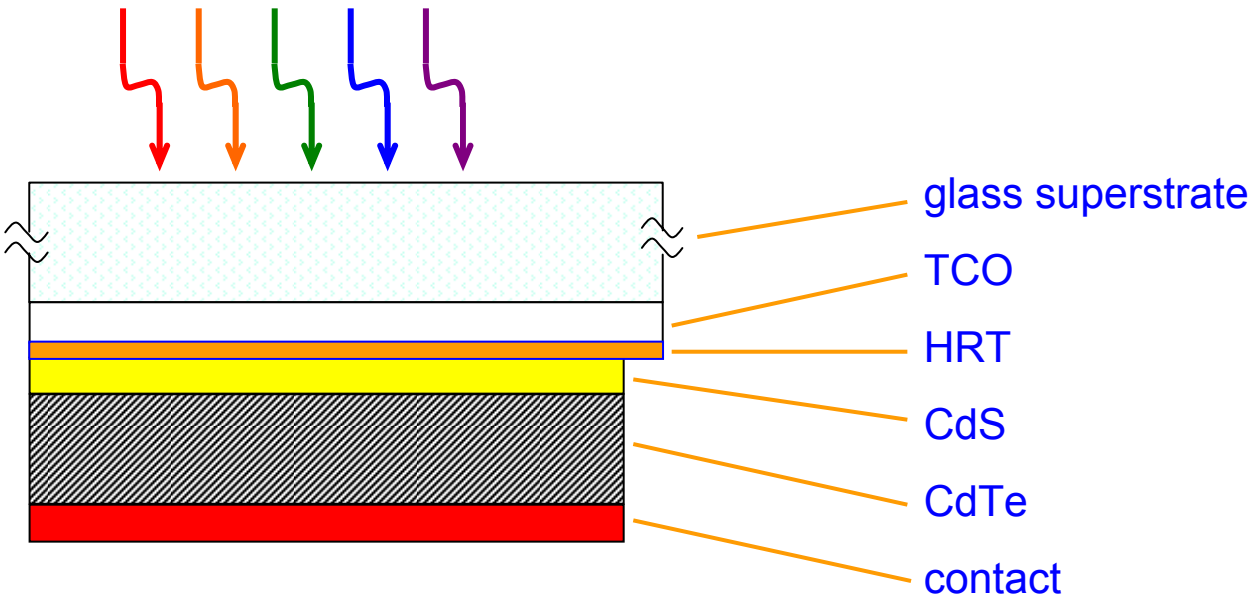
A "near term" goal for CdTe is thinner devices - 1-2µm!

As the CdTe thickness decreases the effect of the net carrier concentration diminishes and the contacts "take over".

Therefore: "Best Approach" is to pursue novel ***back contact*** materials and surface modification processes. Will avoid the use of Cu and potentially decoupled back contact process from absorber/junction. May not have to control doping concentration.

On the other hand: if increasing doping concentration is successful but ultimately thinner devices are needed a better contact must still be pursued.

Superstrate Configuration



Advantages:
- Successfully used
- Self-encapsulated junction
- Back contact available

Disadvantages:
- Beholden to the glass (melt T, optics)
- Control of junction difficult (CdS buried, diffusion)

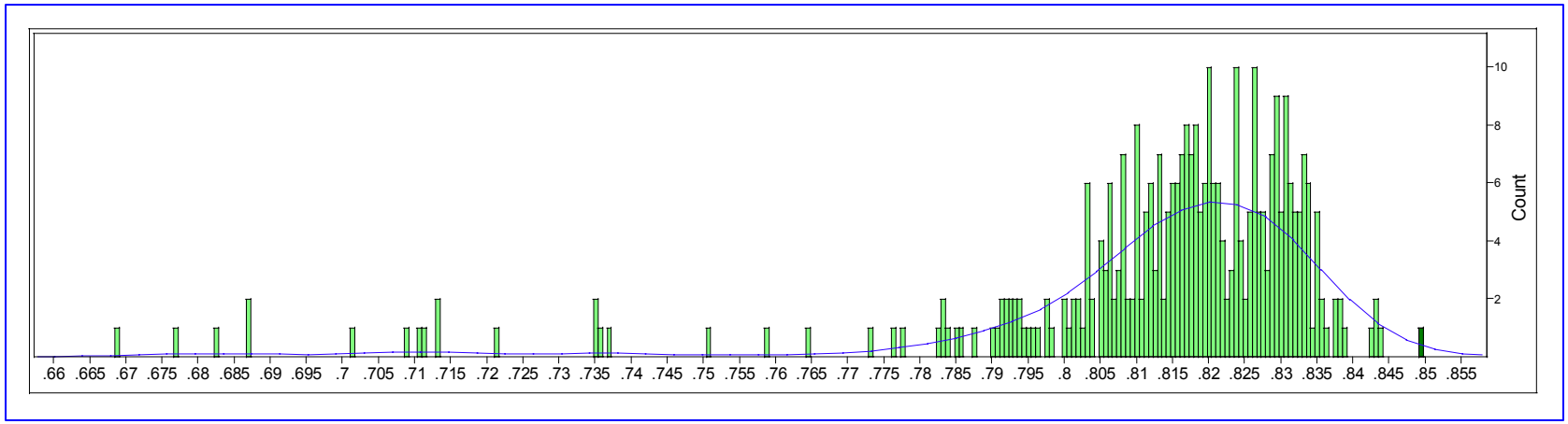
Post CdTe Processing
- $CdCl_2$ treatment
- Etch surface
- Apply contact materials
- Thermal treatment

Processing induced variations in V_{oc}

Dave Albin (NREL) and Samuel Demtsu (CSU)

Voc workshop – National CdTe Team Meeting (March 2006)

Unbiased bargraph of Voc's from 337 devices (last 2-3 years work)



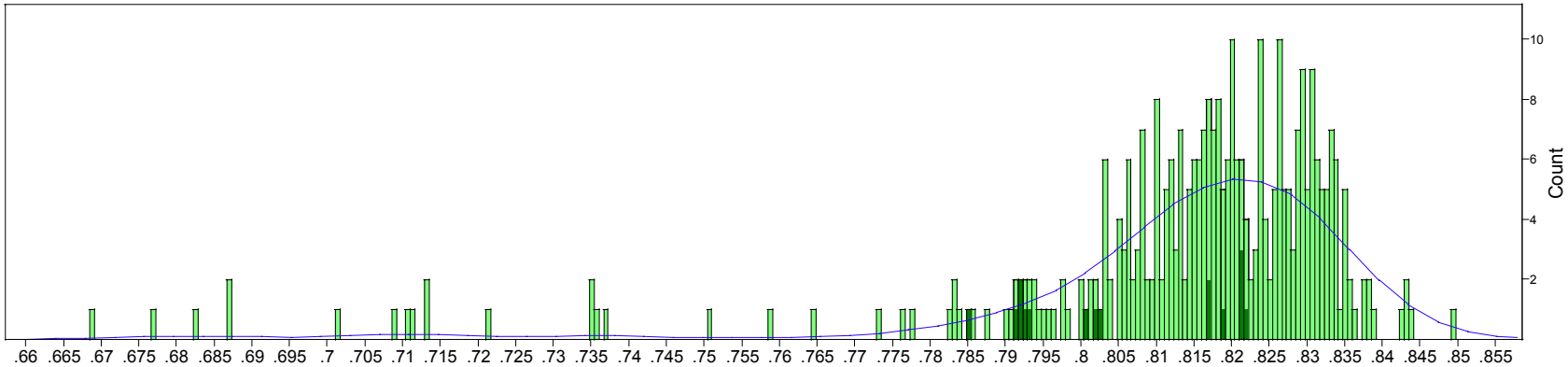
Quantiles		
100.0%	maximum	0.84932
99.5%		0.84556
97.5%		0.83804
90.0%		0.83259
75.0%	quartile	0.82763
50.0%	median	0.81812
25.0%	quartile	0.80803
10.0%		0.79176
2.5%		0.71081
0.5%		0.67455
0.0%	minimum	0.66867

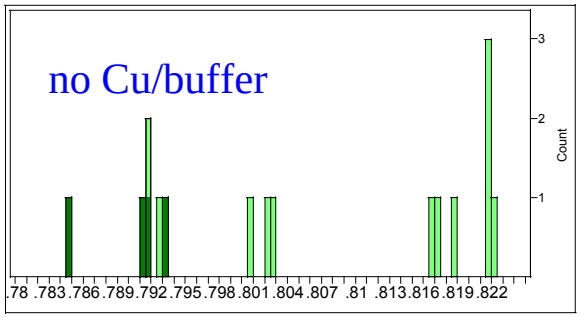
Note: Data included in this slide show taken from last 2-3 years of work in which my major task has been focused on developing correlations between processing and stability. Rather than look for systematic determinations of stability vs single parameters like temp, growth rate, pressure,..I have emphasized determinations based upon technological shifts like buffer, the use of oxygen, the presence of graphite, the use of Hg, etc.

Therefore, in this slide show, I attempt to show how these variations impact Voc.

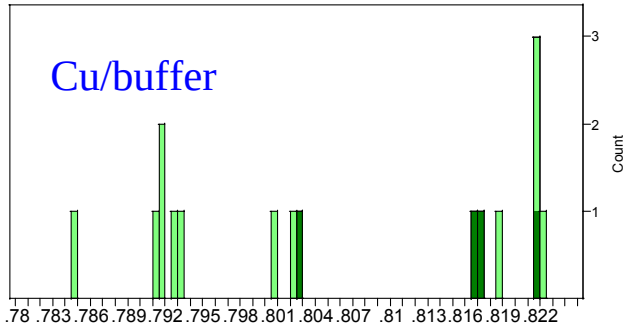
Again, this only represents the last 2-3 years of devices; Overall performance has dropped somewhat and is limited to about 14% at the high end, with average "baseline" levels around 13%. During this period V_{oc} has ranged from 0.669 to 0.849 V.

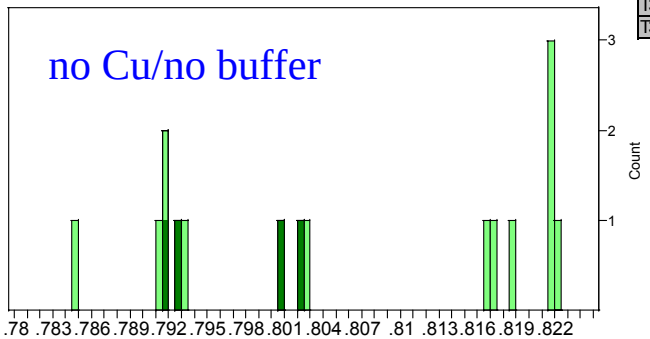
Experiment: Karpov_1 (2x2 matrix; devices with or without Cu in graphite paste contact; devices grown on either single layer SnO_2, or bi-layer "buffer" SnO_2)





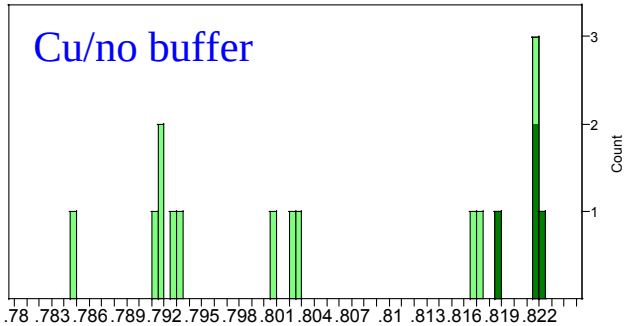
Device	Area	Voc	Jsc	FF	Eff	BC Paste	TCO type
T293_A1	0.472	0.795	23.083	62.618	11.487	no Cu	bilayer
T293_A2	0.497	0.797	22.439	64.496	11.528	no Cu	bilayer
T293_B1	0.446	0.793	22.435	59.374	10.567	no Cu	bilayer
T293_B2	0.451	0.792	22.732	61.699	11.106	no Cu	bilayer
T293_C1	0.461	0.814	22.153	63.02	11.368	w Cu	bilayer
T293_C2	0.505	0.803	21.653	65.462	11.381	w Cu	bilayer
T293_D1	0.454	0.817	23.613	64.308	12.41	w Cu	bilayer
T293_D2	0.498	0.803	22.598	61.376	11.132	w Cu	bilayer
T338_A1	0.475	0.802	23.476	61.764	11.625	no Cu	cond
T338_A2	0.478	0.792	23.587	62.64	11.703	no Cu	cond
T338_B1	0.539	0.801	22.598	59.985	10.853	no Cu	cond
T338_B2	0.589	0.792	22.667	60.662	10.889	no Cu	cond
T338_C1	0.515	0.821	22.223	63.128	11.516	w Cu	cond
T338_C2	0.466	0.819	22.676	64.564	11.991	w Cu	cond
T338_D1	0.458	0.819	22.379	64.556	11.832	w Cu	cond
T338_D2	0.487	0.822	22.391	68.539	12.608	w Cu	cond

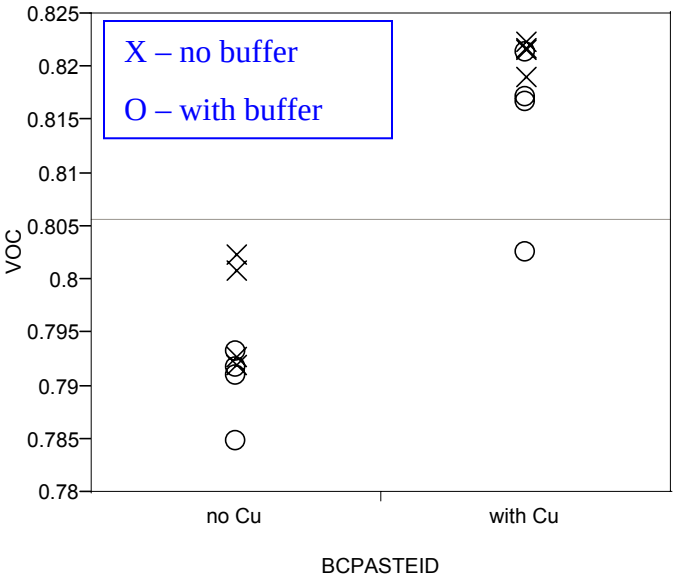




Voc (no buffer) slightly larger than Voc (buffer)

Voc (Cu) greatly larger than Voc (no Cu)





other processing conditions:

- CdS thickness = 80 nm

-CdTe thickness 8.9 to 19.2 um

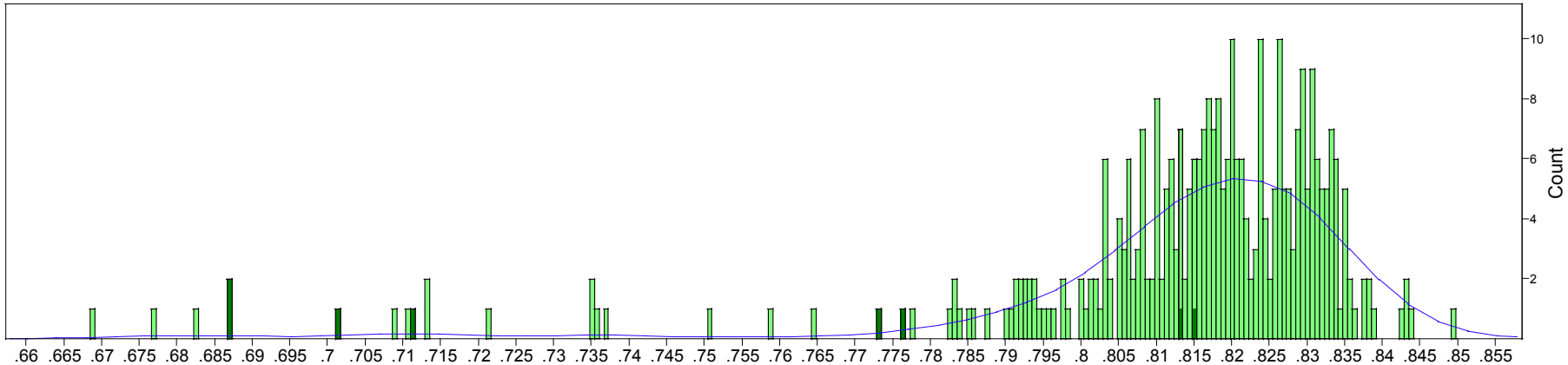
- vapor CdCl2 7m/100 torr O2/400 torr He

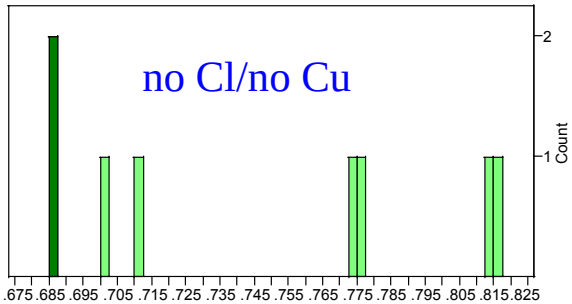
-NP etched

-std electrodag 114 graphite contact doped or undoped with Cu1.4Te

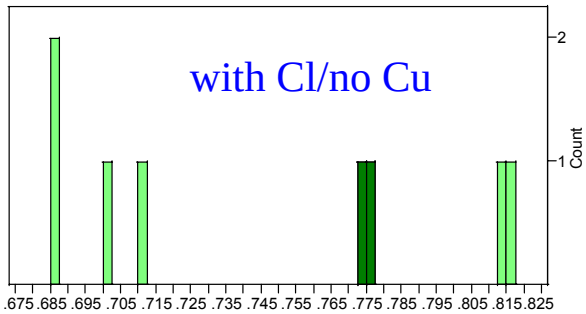
Increased Voc when using Cu slightly larger when “buffer” is absent

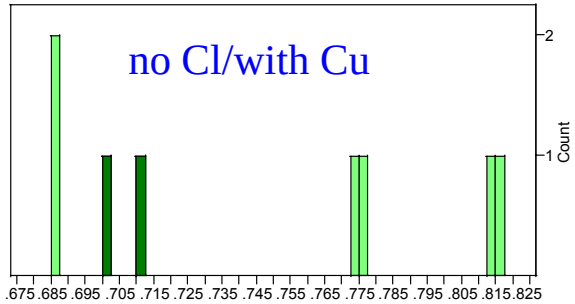
Experiment: Fred_1 (2x2 matrix; devices with or without Cu in graphite paste contact; with or without vapor $CdCl_2$ anneal process)





Device	Area	Voc	Jsc	FF	Eff	BC Paste	CdCl2 process
T365_A1	0.515	0.777	23.291	61.682	11.156	no Cu	7m VCC
T365_A2	0.532	0.774	23.916	63.569	11.760	no Cu	7m VCC
T365_B1	0.473	0.815	23.024	65.798	12.349	with Cu	7m VCC
T365_B2	0.566	0.813	23.112	66.820	12.554	with Cu	7m VCC
T365_C1	0.464	0.711	21.380	56.998	8.666	with Cu	none
T365_C2	0.437	0.701	21.413	57.536	8.639	with Cu	none
T365_D1	0.480	0.687	20.849	51.039	7.310	no Cu	none
T365_D2	0.439	0.687	20.842	54.145	7.755	no cu	none

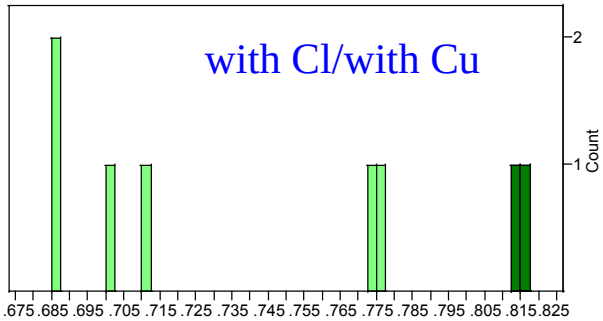


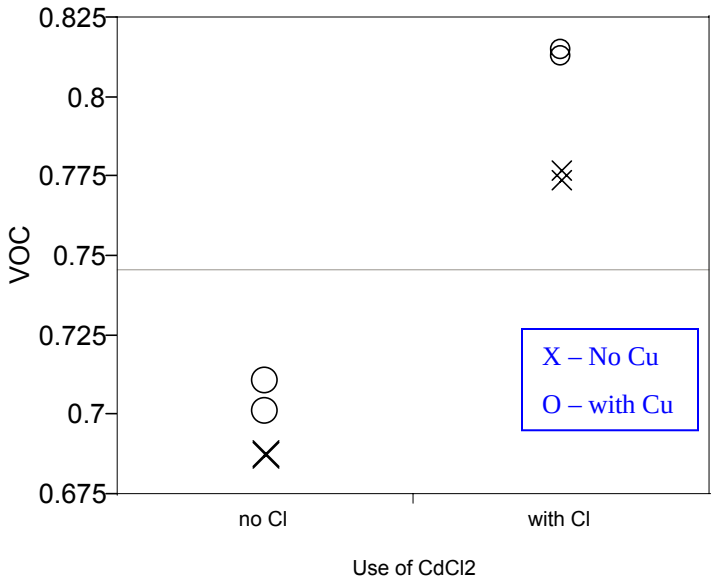


Voc (Cu) > Voc (no Cu)

Voc (with Cl) > Voc (no Cl)

Notice strong effect associated with Cl. Adding Cu to devices with no Cl increase Voc ~ 20 mV. Adding Cu to devices with Cl increases Voc ~ 40 mV





other process conditions:

- with buffer (insulating TCO + base conducting TCO)

-80 nm CdS

-11 um CdTe

-VCC treatment (7m with 100 torr O2/400 torr He)

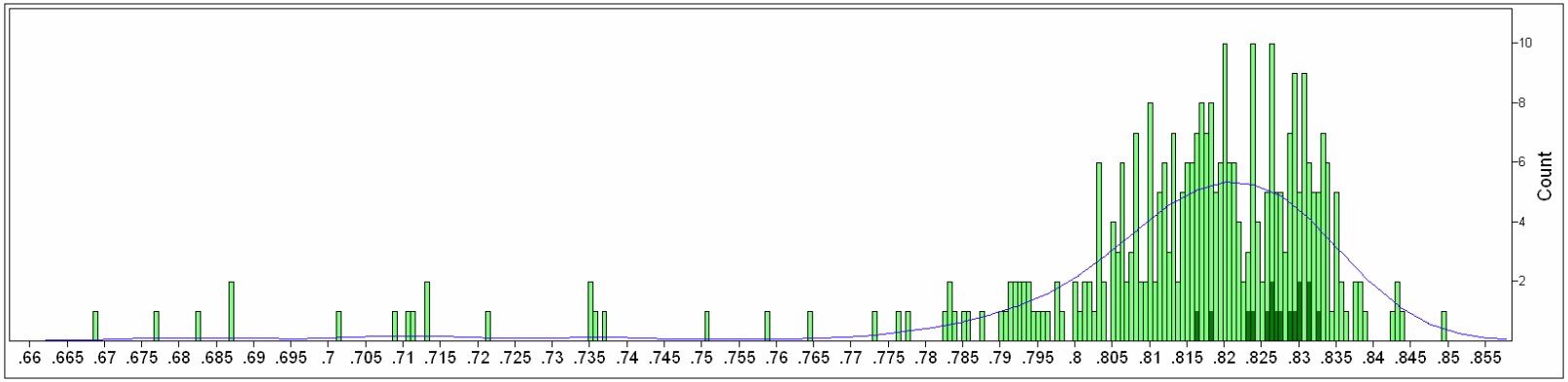
-NP etched prior to std Ag-paste contact

- used electrodag 114 doped or not doped with Cu1.4Te

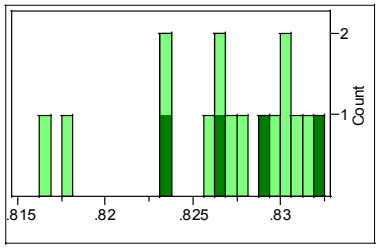
Cu-containing devices have larger Voc's.

The benefit of using Cu (e.g., increased Cu) greater when Cl is present.

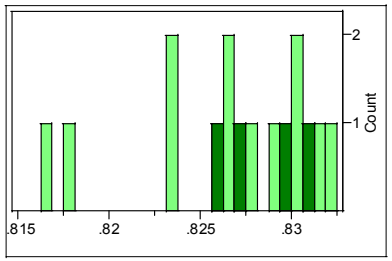
Experiment: Ag_Ni_1 (2x2 matrix; Ag vs Ni paste, with and without graphite layer between metal and NP-etched CdTe surface)



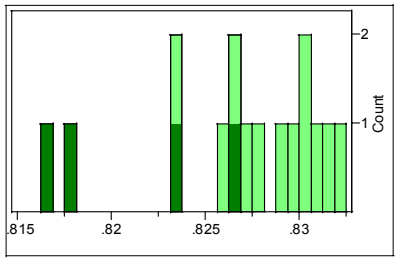
Ag paste on Cu:doped graphite



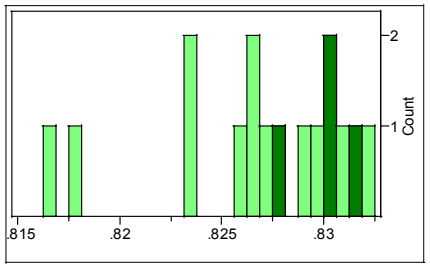
Ni paste on Cu:doped graphite



Ag paste/Cu:doped graphite removed

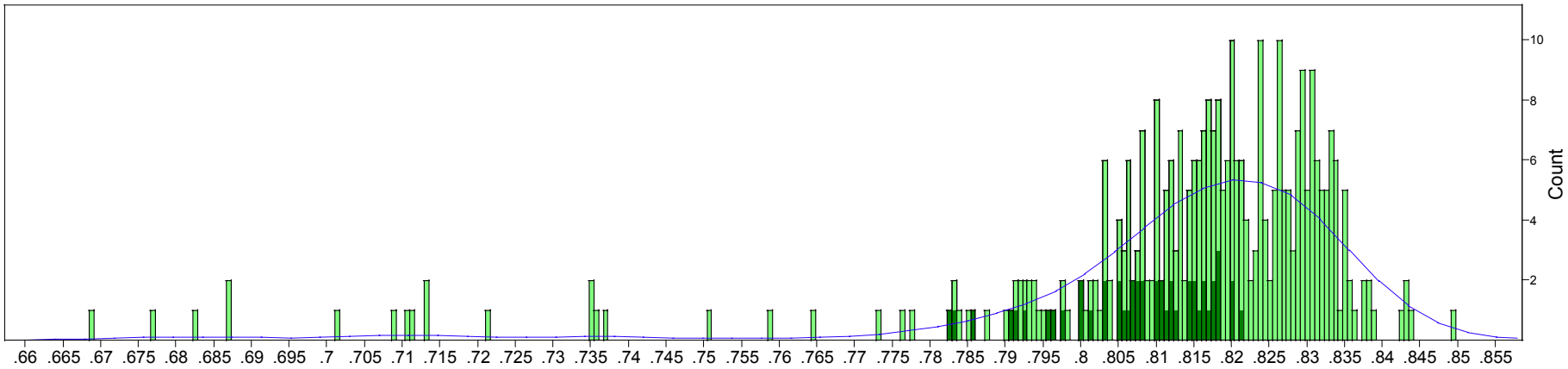


Ni paste/Cu:doped graphite removed

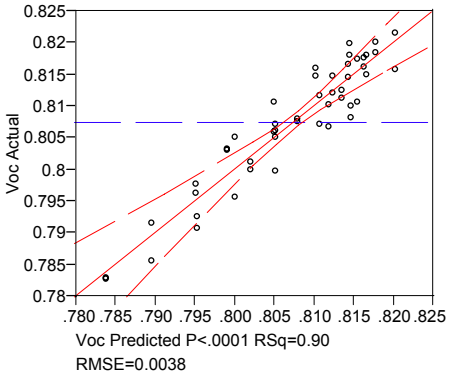


effect on Voc: small but definite. Graphite was beneficial towards Voc when using the Ag-paste,..somewhat detrimental when using the Ni-paste. Ni-pastes were in general better relative to Ag-pastes, however, this was artificial and more ociated with increased series resistance.

Experiment: VCC_O2_2 (4x2 matrix; 3 levels of CdS thickness, 2 levels of CdTe thickness, 2 levels of oxygen during VCC step, 2 levels of etching)

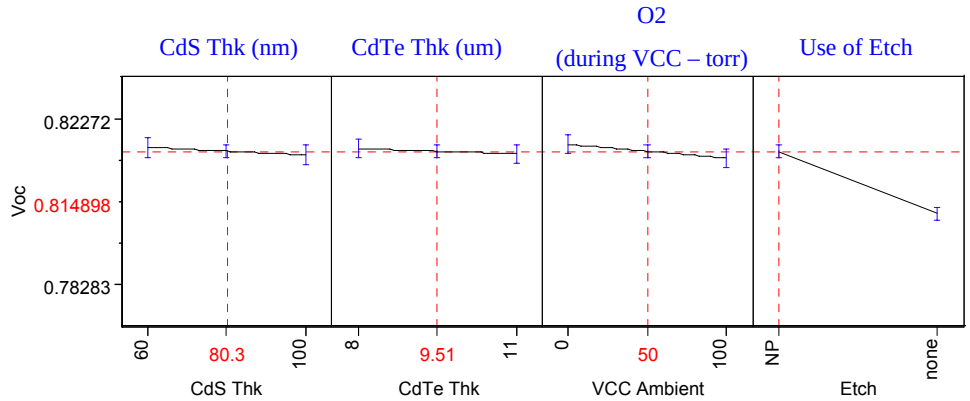


least-squares fit in 4 dimensions

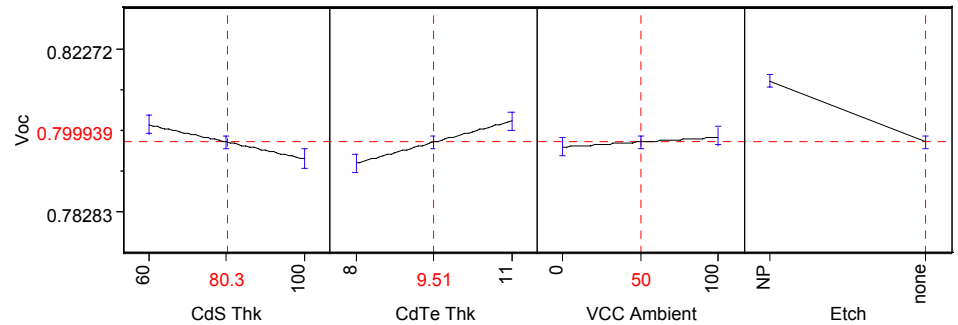


Summary of Fit	
RSquare	0.895932
RSquare Adj	0.856141
Root Mean Square Error	0.003793
Mean of Response	0.807441
Observations (or Sum Wgts)	48

with NP etch, Voc dependence on CdS thk, CdTe thick, and VCC oxygen is **slight**

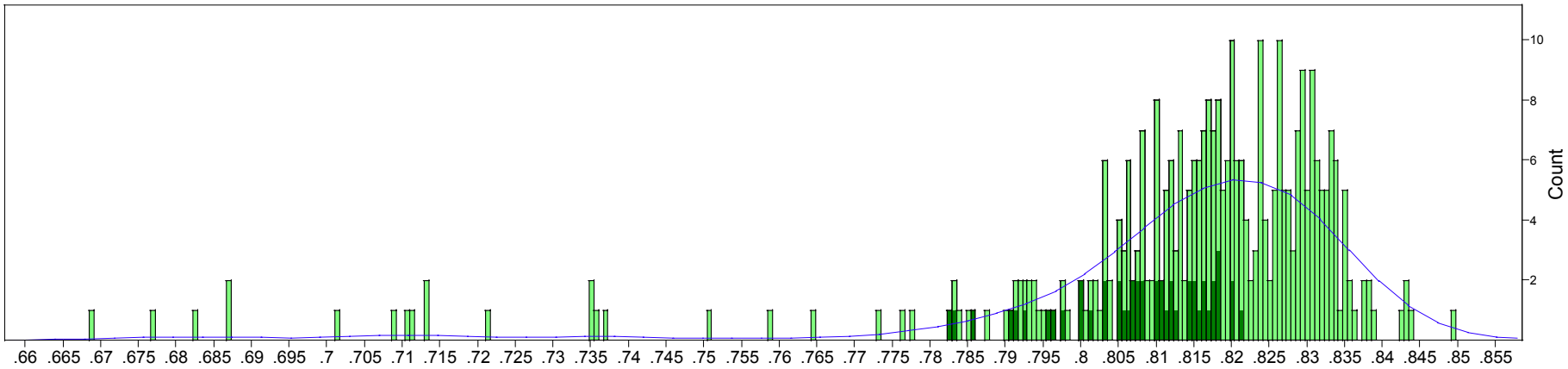


without NP etch, Voc denpendence on both CdS and CdTe thickness is **very strong**

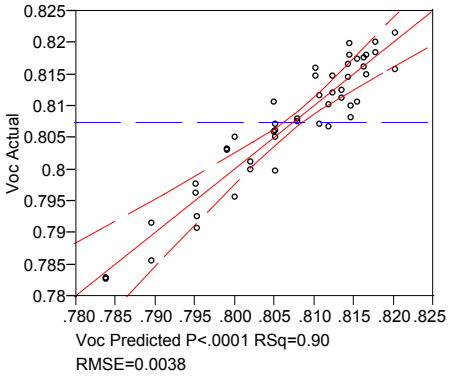


Strong effect: with NP, Voc does not vary much with film thickness (CdS and CdTe), and oxygen during VCC step. Without NP, *Voc is much more dependent* and can be quite large.

Experiment: VCC_O2_2 (4x2 matrix; 3 levels of CdS thickness, 2 levels of CdTe thickness, 2 levels of oxygen during VCC step, 2 levels of etching) - continued



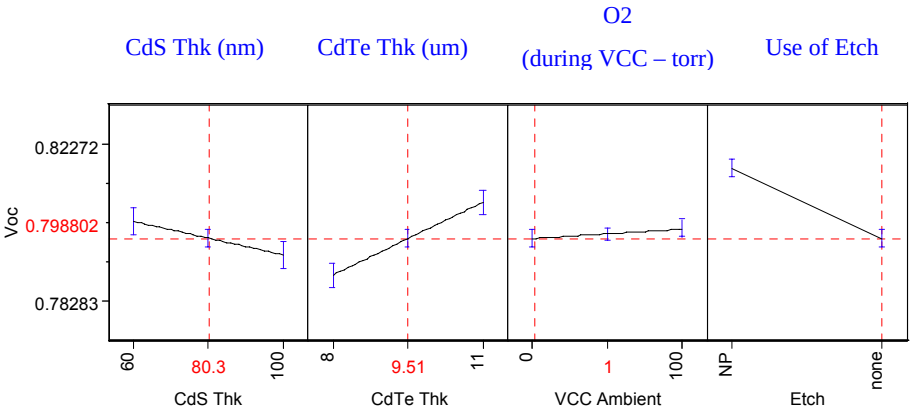
least-squares fit in 4 dimensions

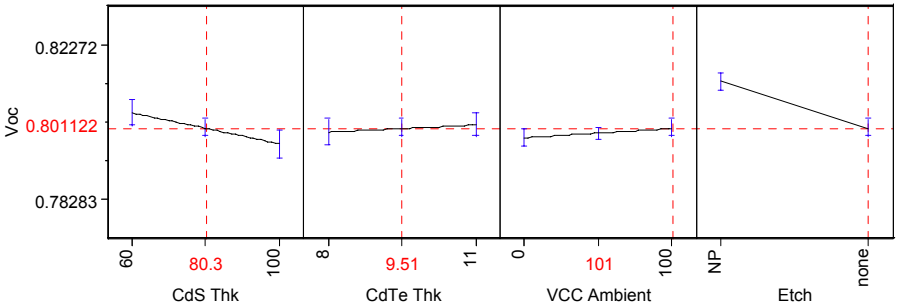


Summary of Fit	
RSquare	0.895932
RSquare Adj	0.856141
Root Mean Square Error	0.003793
Mean of Response	0.807441
Observations (or Sum Wgts)	48

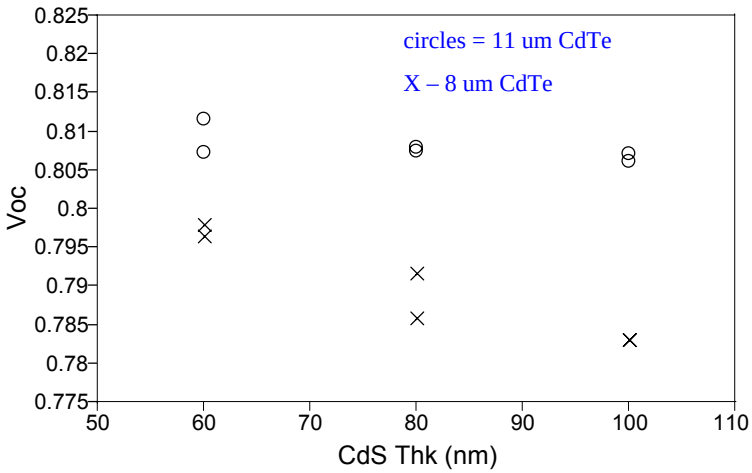
with no NP etch; variation in Voc strongly dependent on CdTe thickness if NO O2 is used during VCC step

with no NP etch; Voc does not vary with CdTe thickness if oxygen is used during VCC step

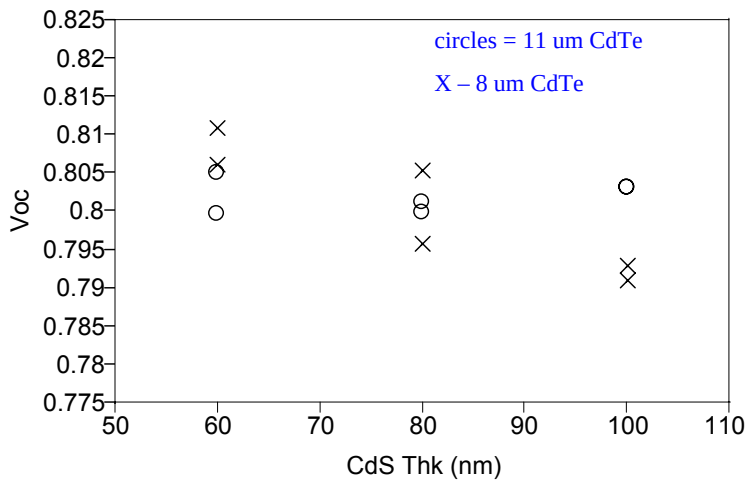




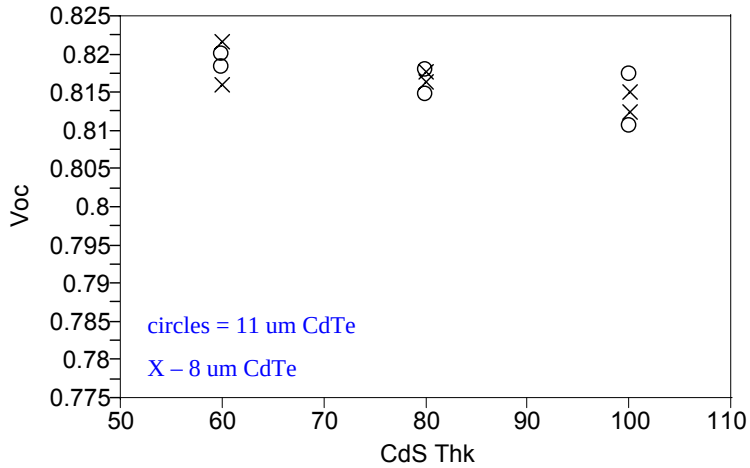
VCC ambient = 500 torr He

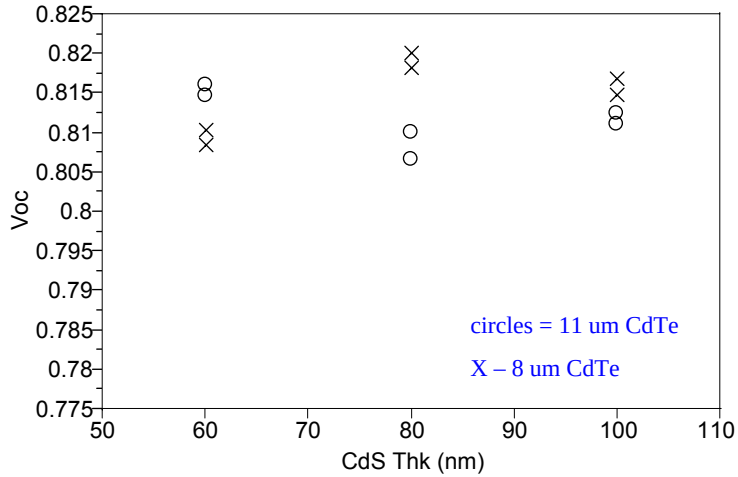


VCC ambient = 100 torr O2/400 torr He



NO NP Etch





NP Etch Prior to Contact

Fabrication perspective on open circuit voltage in CdTe/CdS thin film solar cells

Brian McCandless

Institute of Energy Conversion

Goal

Processing pathway to exceed 850 mV Voc

Questions

1. What limits Voc now? Is it possible to achieve Voc > 900 mV without sacrificing other cell parameters?
2. Can departure from equilibrium during deposition be quantified and controlled and related to fundamental CdTe properties affecting Voc?
3. Have we exhausted the utility of the Cl-Cu-O constituents for controlling properties? Are we near the ultimate limit for pure CdTe?
4. Can we modify absorber deposition to:
   a. control properties and reduce inter-step coupling
   b. reduce demands on post-deposition processing
5. Have we sufficiently explored window/buffer properties?

What primarily limits Voc now?

1. Built-in voltage, QFL pinning in absorber (Voc-T saturation, max ~ 1 V @ 200K)
2. Un-identified/un-specified recombination (A-factor:1 < A < 2, lifetime correlation with Voc)
3. Absorber conductivity (max ~10^{15} cm^{-3})
4. Window plays secondary role:
   a. CdS diffusion role for Voc is not the Eg reduction (buffer layer role, Golden Photon cells) but absorber-TCO interaction
   b. CdZnS and ZnS window layers haven't made a difference

Three avenues to consider

1. **Film equilibrium condition (defect chemistry-lifetime)**
   a. **superstrate and substrate configurations**
2. **Absorber bandgap**
3. **Absorber conductivity**

Departure from equilibrium

For present generation superstrate devices, state of the device established by post-deposition modifications:

1. non-uniform stoichiometric deviations (e.g., reduced Eg at grain surfaces and distribution of V_{Cd})
2. non-uniform distribution of extrinsic dopants (Cu, Cl, O)
3. strong chemical affinities (CdS-CdTe miscibility, oxidation, etc)

Radically different from substrate CIGS devices

Towards controlling equilibria in CdS/CdTe thin film devices

Focus on deposition rather than post-deposition:

1. Direct control of composition (defects)
   a. Cd/Te ratio
   b. in situ doping
   c. growth rate, temperature
2. Direct control of junction
   a. substrate configuration

How about alloy absorber to widen Eg?

CdZnTe (1.5 - 2.24 eV) → enhanced p-type conductivity

Proposal

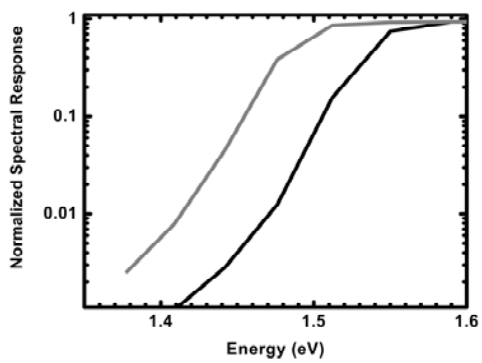
Alloy CdTe with ZnTe during deposition in N-containing ambient to manipulate defect chemistry during growth and widen absorber Eg, and use ZnS or other wide Eg window

1. N doping efficiency increases by >10X for 10 wt% cation substitution with Zn[1], resulting in NA > 10^{17} cm^{-3}
2. V_{Te} self-compensation mechanism energetically less favored in ZnTe and alloys thereof[2]
3. N_2 carrier gas improves device collection and Voc for cells with no $CdCl_2$; paths to increase in equilibrium constant for N from N_2 (10^{-34})
4. 10 wt% Zn incorporation increases Eg to 1.56 eV
5. Halide vapor processing of $CdS/Cd_{0.9}Zn_{0.1}Te$ at ~400ºC converts CdS layer to ZnS via grain boundary diffusion, Voc = 835 mV[3]: suggests start with ZnS or other window

[1] *T. Baron, et. al. Appl. Phys. Lett. 65 (1994) 1284*
[2] *Y. Marfaing, J. Cryst. Growth 161 (1996) 205*
[3] *B. McCandless and W. Shafarman, Annual Report, NREL High Performance (2006)*

$CdS/Cd_{1-x}Zn_xTe$ Solar Cells*

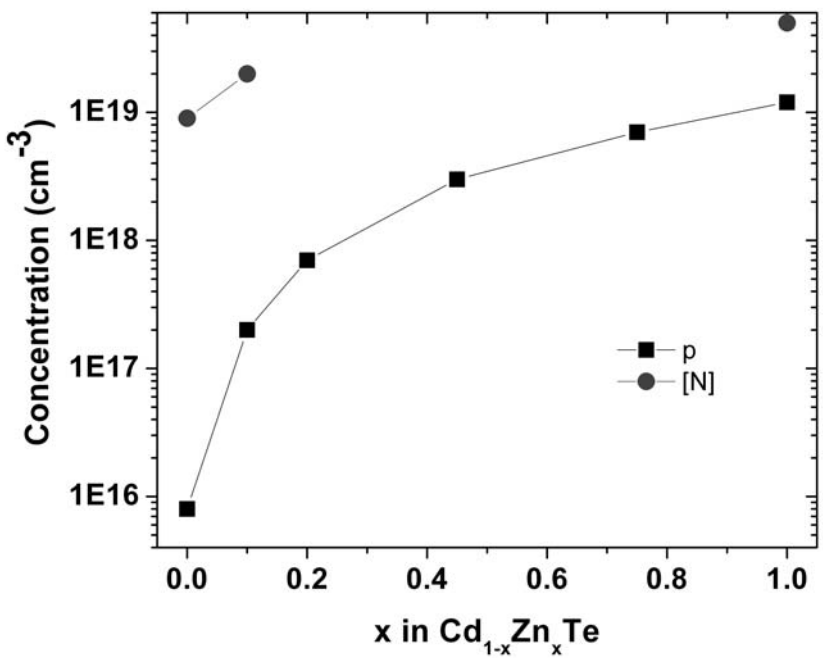
Sample	x (EDS)	Eg (eV)	Halide Vapor	Voc (mV)	Jsc (mA/ cm^2)	FF (%)	Eff (%)	QE @ 400nm (%)	QE λ_L (nm)
149.2	0	1.50	$CdCl_2$	840	24.4	65	13.3	50	825
127.2	0	1.50	$ZnCl_2$	746	23.0	62	10.5	45	825
124.6	0.05	1.53	$CdCl_2$	756	22.9	57	9.8	40	810
124.4	0.05	1.53	$ZnCl_2$	782	24.4	65	12.4	38	800
182.1	0.10	1.58	$ZnCl_2$	-	-	-	-	-	-
182.6	0.10	1.58	$CdCl_2$	835	20.0	66	11.0	50	790
182.5	0.10	1.58	$CdCl_2$	811	23.0	66	12.3	58	785
129.8	0.16	1.60	$CdCl_2$	783	22.2	56	9.7	62	790
129.6	0.16	1.58	$ZnCl_2$	754	23.0	49	8.5	55	790
152.4b	0.27	1.66	$ZnCl_2$	775	20.8	54	8.7	60	775
160.5	0.60	1.90	$ZnCl_2$	414	1.6	32	0.2	-	-



*Cells fabricated under NREL high performance project: XAT-4-33624-01

N-doped $Cd_{1-x}Zn_xTe$ Thin Films

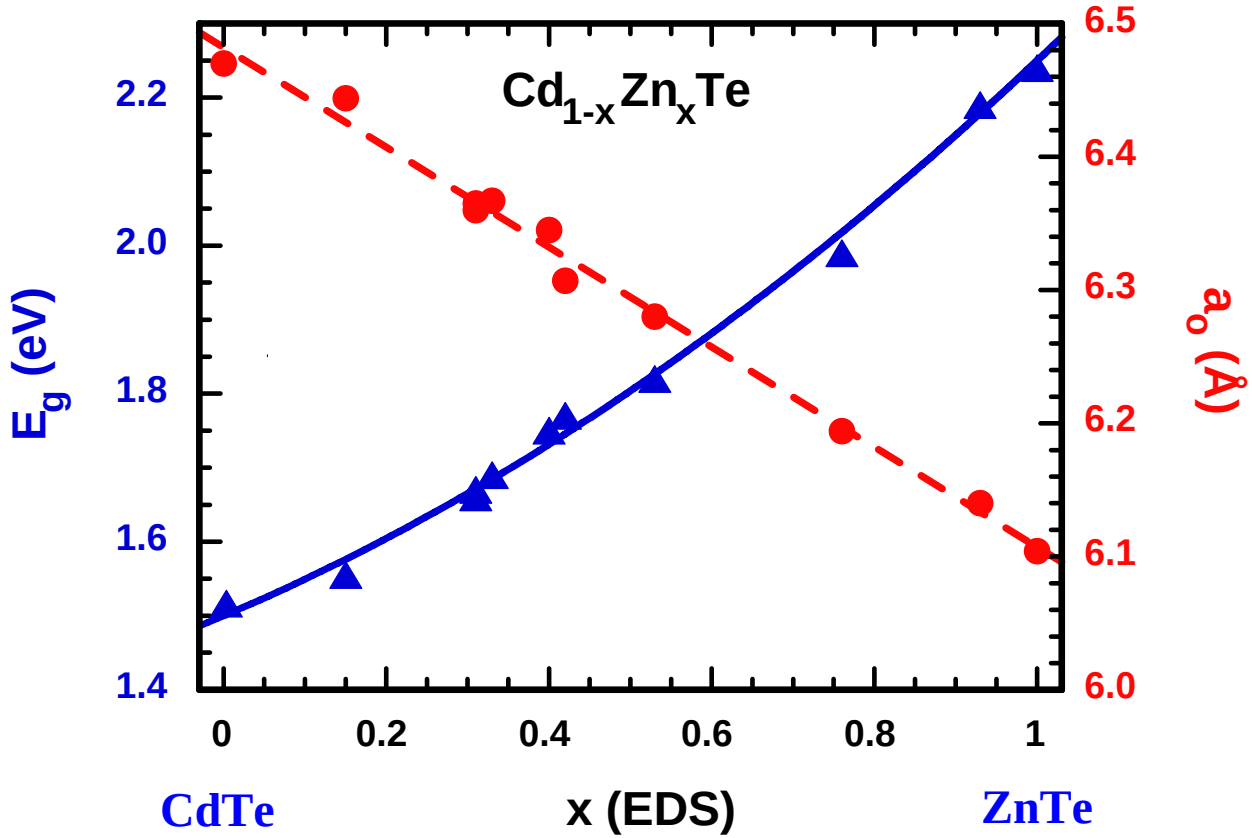
Effective hole concentration and [N] in plasma-enhanced MBE CZT films[1]



High Nitrogen doping efficiency also reported for p-ZnTe:N[2]

[1]*T. Baron, et. al. Appl. Phys. Lett. 65 (1994) 1284*
[2]*Y. Fan, et. al. Appl. Phys. Lett. 65 (1994) 1001*

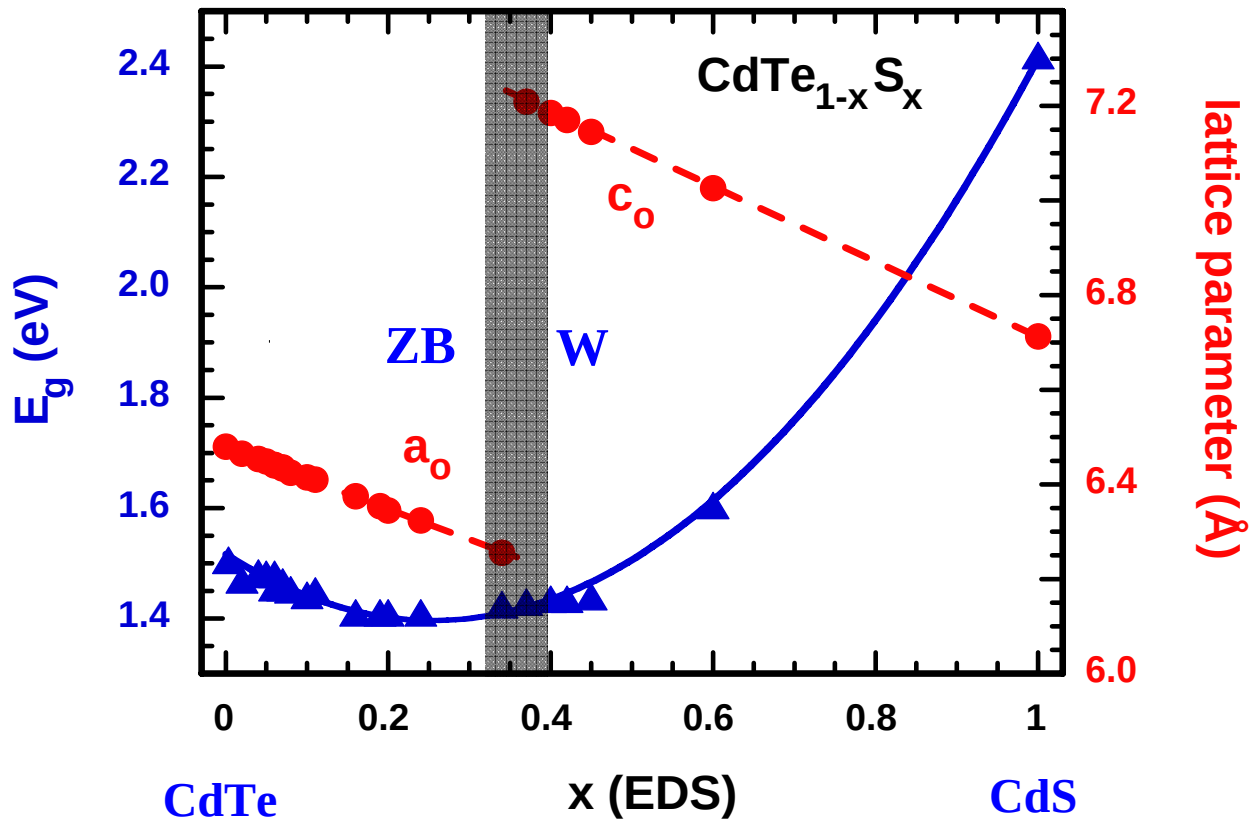
$Cd_{1-x}Zn_xTe$ Thin Films: As Deposited, 325ºC



Continuous solid solution

$$E_g = 1.51 + 0.44x + 0.30x(1-x)\ (b \sim 0.3,\ x\text{-}tal)$$

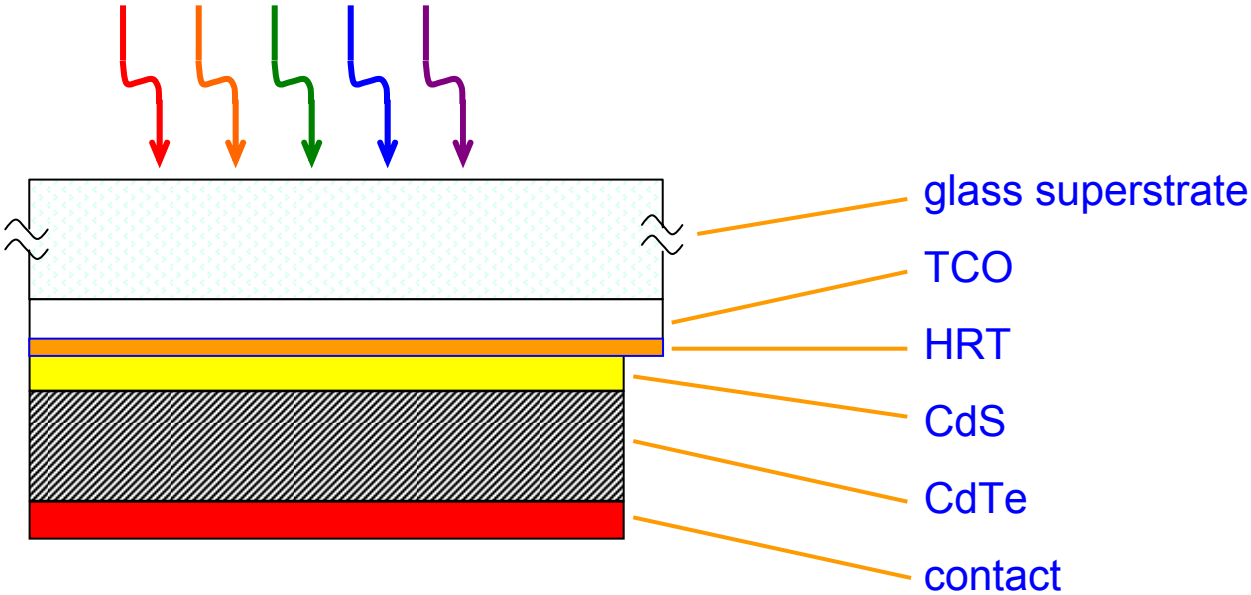
$CdTe_{1-x}S_x$ Thin Films: As Deposited, 200ºC



Continuous solid solution with structure change at x~0.35

$$E_g = 1.51 - 0.94x + 1.84x(1-x) \quad (b\sim 1.7,\ x\text{-}tal)$$

Superstrate Configuration



Advantages:
- Successful demonstration of η > 16%
- Self-encapsulated junction
- Back contact accessible

Disadvantages:
- Beholden to the glass/TCO (melt T, optics)
- Control of junction difficult (CdS buried, diffusion)
- Junction access difficult for diagnoses

Post CdTe Processing
- $CdCl_2$ treatment
- Etch surface
- Apply contact materials
- Thermal treatment

V_{oc} improvement

Xuanzhi Wu

March 10, 2006

Outline

- Why we need to focus on V_{oc} improvement for further improving device efficiency - only small room for J_{sc} and FF improvement
- How to improve V_{oc} in the past work

  1. Improve main junction and CdTe quality by integrating ZTO buffer layer and optimizing $CdCl_2$ treatment;

  2. Minimize non-uniformity problem by improving individual layer, junction and interface, and device area definition
- Future work

  1. Further improve junction and minimize non-uniformity through improvement of device fabrication processes;

  2. Study correlation between defects (& grain boundary) and V_{oc}, and find way to reduce the compensation and to increase lifetime of CdTe device (cooperation with CSM).

J_{sc} losses in a 16.1%-efficient CTO/ZTO/CdS/CdTe solar cell

	J_{sc} loss mechanism	J (mA/cm^2)	$J/J_{Theoretical}$ (%)
J_1	Absorption of CTO/ZTO	0.74	2.51
J_2	Absorption of CdS	1.40	4.75
J_3	Recombination in junction & CdTe	0.52	1.76
J_4	Reflection	1.19	4.03
J_{loss}	$J_1 + J_2 + J_3 + J_4$	3.85	13.05
J_{sc}		25.65	86.95
$J_{Theoertical}$ E_g~1.48 eV		29.5	100

High-efficiency CdTe cells with high fill factor

Cell #	V_{oc} (mV)	J_{sc} mA/cm^2	FF (%)	η□* (%)□	Area (cm^2)
1	842.1	24.12	**77.26**	15.7	1.001
2	848.1	23.97	**77.34**	15.7	0.976
3	842.7	25.24	**76.04**	16.1	1.116
4	835.6	25.25	**76.52**	16.2	0.961

*** NREL-confirmed efficiency**

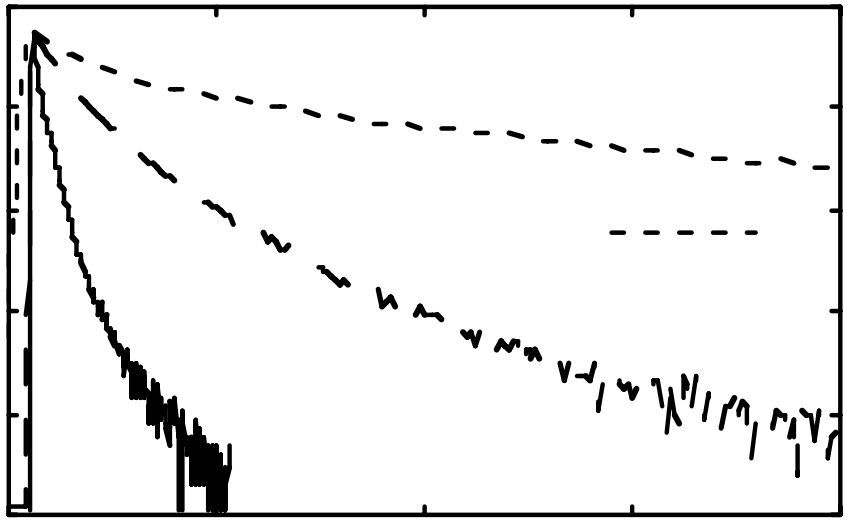
**** Device analyses indicate that the CdTe cells with high fill factor have lower R_s (~1 Ω cm^2), higher R_{sh} (3000-5000 Ω cm^2,) and modest A factor (1.6-2).**

CdTe cells with high V_{oc}

Cell#	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency * (%)	Area (cm^2)
1	**847.5**	25.86	74.45	16.4	1.131
2	**849.9**	25.50	74.07	16.1	1.029
3	**848.1**	23.97	77.34	15.7	0.976
4	**849.6**	25.25	74.17	15.9	1.236
5	**848.2**	25.55	73.55	15.9	1.040
6	**857.4**	24.92	72.98	15.6	1.008

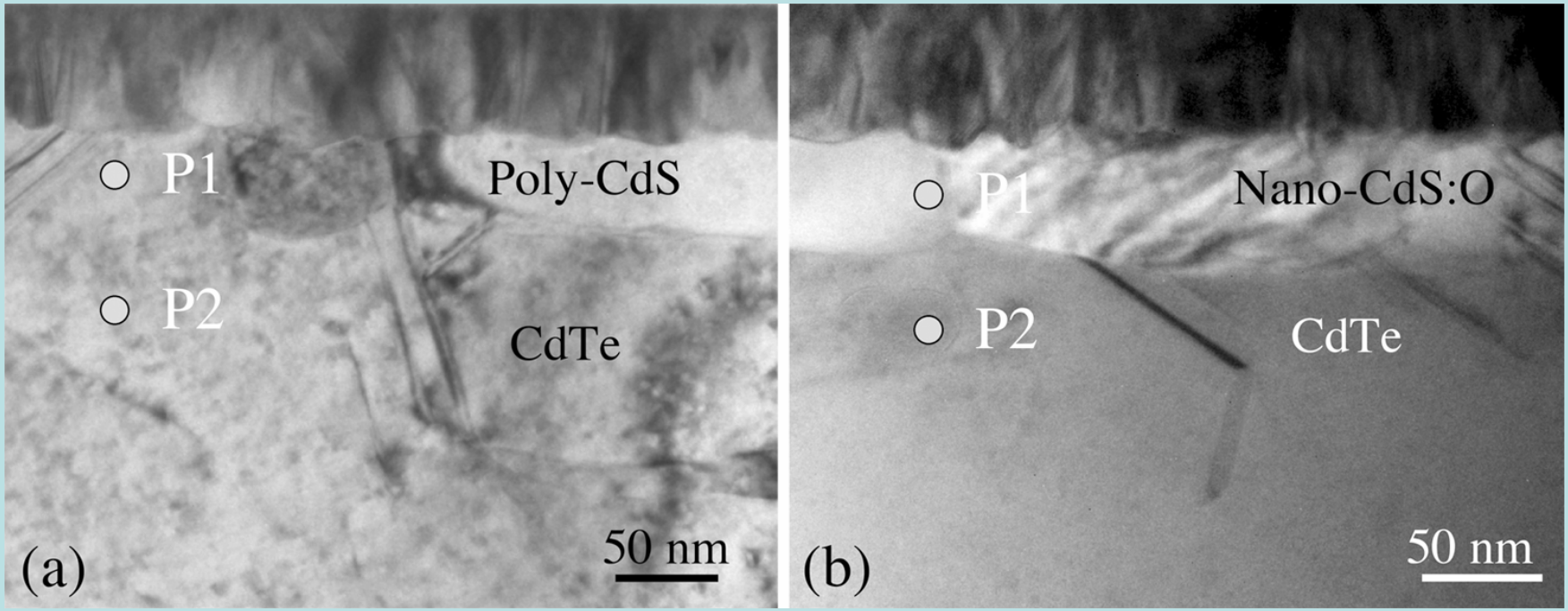
*** NREL-confirmed efficiency.**

Time-Resolved Photoluminescence



- **W380-A: CdTe cell with the optimum $CdCl_2$ treatment;**
- **W380-D: CdTe cell with normal $CdCl_2$ treatment;**
- **W380-C: CdTe cell without $CdCl_2$ treatment**

TEM



As an example, uniformity of junction has been improved by using a nano-crystalline CdS:O film.

Study correlation between V_{oc} and Cu, Cl and O related defects

- Defects in different $CdCl_2$-teated cells with Cu in back-contact;
- Defects in different $CdCl_2$-treated cells without Cu in back-contact;
- Defects in $CdCl_2$-treated cells with different Cu content in back-contact;
- Defects in cells deposited in different O_2 ambient;
- Defects in high-efficiency cells and low-efficiency cells.

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

A total of 37 ideas for increasing V_{OC} were obtained from the mini-workshop preparations, presentations, discussions, survey, and subsequent e-mails. Ideas range from emphasizing standard best practice processing procedures to those that have never been tried. The list is divided into six major categories of V_{OC} limiting problems. For each category the root causes, models/symptoms/effects, and possible remedies are listed. Within each possible remedy the institutions that are working on it or have worked on it along with a principal contact are also listed.

1. **Lateral non-uniformities.**
    a. Root causes
        1. Coating non-uniformity (thickness/morphology/dust)
        2. Non-uniform distribution of impurities
        3. Grain boundary versus grain bulk
    b. Models/Symptoms/Effects
        1. Weak diodes with lower turn-on voltage that drains current
        2. Local higher back contact barriers – increased recombination
        3. Shunting
    c. Possible remedies
        1. High Resistance buffer layer (IFL, HRT)
            i. NREL, Albin
            ii. IEC, McCandless
            iii. USF, Ferekides
        2. Self-healing treatment (aniline electrolyte).
            i. UT, Karpov
        3. Thorough surface cleaning prior to each deposition to avoid particulates
            i. ALL
        4. Avoid too much Cu (can cause localized shunting along GB)
            i. ALL
        5. Improve analysis and diagnostics
            i. LBIC, CSU, Sites
            ii. Kelvin Probe, IEC, McCandless
            iii. Spatially resolved EL/PL, CSM, Seymour
        6. Use surfactant to increase CBD CdS uniformity
            i. NONE

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

2. **Back contact barrier**
    a. Root causes
        1. High p-type CdTe work function ~5.5 eV
        2. CdTe/back contact interface pinned by interface states
    b. Models/Symptoms/Effects
        1. Impedes hole flow - increases recombination
        2. Reach-through diode effect
        3. For p/i/n structure, limits V_{OC} by limiting junction potential
    c. Possible remedies
        1. Cu doping in back contact region to allow tunneling/hopping through barrier
            i. ALL
        2. Back contact electron reflector – ZnTe layer
            i. IEC, McCandless
            ii. UT, Compaan
            iii. NREL, Gessert
            iv. CSM, Kaydanov
        3. Decrease effective back barrier height
            i. USF, Ferekides
            ii. NREL – ZnTe, Gessert
        4. Interfacial layer at back contact
            i. UT, Compaan/Karpov
            ii. IEC, McCandless
        5. Use higher work function back contact metals (Ni, Pt, Pd, ..) in order to better match high work function CdTe.
            i. NREL, Albin
        6. Improved characterization to better understand the problem, measurement of back barrier height with UPS and internal photoemission
            i. U. of Nevada, Los Vegas
        7. Increase back contact workfunction/electronegativity – surface doping that adds dipole layer to alter effective back surface electron affinity.
            i. NONE
        8. Reduced back contact area to lessen surface recombination
            i. NONE

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

3. Difficulty in obtaining higher doping concentrations

a. Root causes
   1. Self-compensation due to CdTe wide band gap and easily deformable lattice.
   2. High concentrations of compensating defects from high densities of impurities, Cu, Cl, O, and grain boundary states.

b. Models/Symptoms/Effects
   1. Net charge concentrations << dopant concentration
   2. Higher carrier concentrations unstable – leads to degradation

c. Possible remedies
   1. Cu doping (Cu has less self-compensation)
      i. ALL
   2. Stoichiometry optimization, Te enrichment during deposition, co-doping.
      i. IEC - McCandless
      ii. CSM – Beach
      iii. NREL - Albin
   3. Optimize $CdCl_2$ treatment - (creates dopant A-center V_{Cd}-Cl_{Te} complex)
      i. All
   4. Reduce bandgap S, Se, Hg (V_{OC}/J_{SC} tradeoff)
      i. UT, Compaan
   5. In-Situ doping with other dopants, Ag, P, Na, N, As, Sb
      i. P, NREL – Albin

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

4. High concentration SRH recombination center defects

a. Root causes
   1. Easily deformable lattice
   2. Grain boundaries of polycrystalline material
   3. Interface defects between layers
   4. High densities of impurities

b. Models/Symptoms/Effects
   1. Shortened diffusion length and minority carrier lifetime
   2. Defect generation, mutation, and migration with illumination and/or bias

c. Possible remedies
   1. Optimize oxygen concentration during deposition and anneal
      i. IEC, McCandless
      ii. CSM, Beach
   2. Optimize $CdCl_2$ treatment – (passivation effect)
      i. ALL
   3. Purification of starting CdTe material
      i. NONE

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

5. Losses in window layer and at heterojunction interface

a. Root causes
   1. Conduction band detrimental offset at junction
   2. Heterojunction lattice mismatch – high defect concentration

b. Models/Symptoms/Effects
   1. High recombination rates in interfacial region
   2. MIS (Metal-Insulator-Semiconductor) behavior

c. Possible remedies
   1. Cd_2SnO_4 TCO (enhances J_{SC} and yields high V_{OC})
      i. NREL, Wu
   2. Put CdS under compression (piezo-effect - depletion)
      i. UT, Karpov
   3. Efficient HRT with “right” CdS interfacial morphology
      i. USF, Ferekides
   4. Alternate window material Zn-, In-(S,O)
      i. NONE
   5. Surface doping to take advantage of MIS structure
      i. NONE
   6. p-n homojunction – requires n-type/p-type doping of CdTe
      i. NONE
   7. Impurity to passivate interfacial states
      i. NONE
   8. Dope CdS layer (In?)
      i. NONE

CdTe Team list of V_{OC} limitations and possible remedies
From V_{OC} mini-workshop, March 10, 2006

6. Other ideas with possible V_{OC} implications

a. Substrate growth – better access to main junction during deposition.
    1. NREL, Dhere
    2. IEC, McCandless
    3. UT, Compaan

b. Eliminate Cu in back contact
    1. USF, Ferekides
    2. IEC, McCandless
    3. UT, Compaan

c. Optimization of complex interaction from combined treatment with $CdCl_2$ – Cu – O_2
    1. NREL, Wu

d. Raise CdTe bandgap with ZnTe/CdTe alloy to raise V_{OC}/E_{GAP} or lower E_{GAP} – V_{OC}
    1. NREL, Dhere
    2. IEC, McCandless
    3. UT, Compaan

e. Interface pinning, front near E_C and back near E_V
    1. NONE

f. Intentional illumination during CdTe layer deposition.
    1. NONE

g. Sequential incorporation of dopant and Cl.
    1. NONE

h. Thick versus thin CdTe layer.

i. Insure that devices can withstand tape-pull adhesion test.