PROCESSING MATERIALS, DEVICES AND DIAGNOSTICS FOR THIN FILM PHOTOVOLTAICS: FUNDAMENTAL AND MANUFACTURABILITY ISSUES

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Summary

The IEC has continued its work on developing $CuInGaSe_2$-based, CdTe-based, and Si solar cells.

CdTe Solar Cells

The CdTe task focused on aspects of cell fabrication that can be used to improve module performance and utilize thin CdTe absorber layers, to increase processing throughput and reduce materials usage. Issues related to high throughput processing of and junction-limiting factors in CdTe solar cells are reported. Based on the effects of TCO/substrate cleaning described in the previous annual report, we continued with the study of uncontrolled impurities originating in the glass/SnO_2 substrate. Concerns over possible sources of impurity contamination of CdTe has prompted further analysis of the influence of soda lime glass (SLG) SLG/SnO_2 substrate preparation as well as the chemistry of the CdS growth and its effect on the CdS-CdTe junction region. It is vital that this source of variability in film morphology and device performance is eliminated prior to development of cells with sub-micron absorber thickness and evaluation of approaches for V_{OC} > 900 mV. In this report we present the details of procedures used to establish a performance baseline with cell efficiency >11% for processing CdTe/CdS cells with vapor transport deposited CdTe onto moving substrates at high growth rate (~10 μm/min) using rapid post-deposition processing, with less than 1 min per processing step. CdTe films having low pinhole density, $<10^{-6}$ fractional area, are routinely deposited by vapor transport over a thickness range from 1 to 10 microns. Issues related to high throughput and high temperature processing of and junction-limiting factors in vapor transport deposited thin film CdTe solar cells are reported. CdTe/CdS cells deposited onto commercial soda lime glass substrates films by vapor transport deposition and processed with 1 min $CdCl_2$ treatments with 3 micron and 1 micron thick CdTe have achieved AM1.5 conversion efficiencies of >11% and 7%, respectively.

CdTe Collaborations

IEC continued interaction and collaboration with (former) CdTe R+D Team members. Specifically, Brian McCandless provided guidance to Primestar Solar for materials and equipment needed to develop CdTe deposition and post-deposition processing. Brian McCandless continued collaboration with Alan Fahrenbruch regarding analysis of back contact barriers to CdTe and the sensitivity to composition for Cu-Te contacts.

CIS-based Solar Cells

In the subtask "In-Line Evaporation of $Cu(InGa)Se_2$" the research objective was to determine the limit of deposition time for $Cu(InGa)Se_2$ in-line evaporation in IEC's roll-to-roll process and the effects of higher speed deposition on device performance. Our approach was to deposit $Cu(InGa)Se_2$ with increasing web translation speed and source

effusion rate and characterize the resulting device performance as a function of thickness and growth rate.

A second sub-task focused on "Improved Performance with Absorber Thickness < 1 μm." In this area the objective was to develop methods to increase J_{SC} in devices using absorber layers with thickness $0.3 \leq d \leq 1.0$ μm. The approach was to develop methods to implement light scattering into $Cu(InGa)Se_2$ devices and determine its potential for increasing J_{SC}. Determine if the higher absorption coefficient in $CuInS_2$ or S-containing alloys can be used to increase J_{SC} with thin absorbers.

To further characterize films and devices with submicron $Cu(InGa)Se_2$ thicknesses, films were evaporated using constant deposition rates and varying times to form layers with thicknesses from 0.35 – 3.3 μm. Characterization of the films showed that the grain size decreases significantly as thickness is reduced less than 1 μm. Devices showed a decrease in performance with decreasing thickness attributed primarily to reduced J_{SC}. A device with $Cu(InGa)Se_2$ thickness 0.35 μm had $V_{OC} > 0.6$ V and FF > 70% but efficiency 7.9% due to the loss in J_{SC}.

Thin $CuInS_2$ absorber layers were deposited and compared to results with $Cu(InGa)Se_2$ to determine the effect of the higher absorption coefficient in the S alloy. The films had a similar reduction in grain size with decreasing thickness. The $CuInS_2$ devices had a loss in J_{SC} which was greater than expected from the optical absorption but the relative decreases in J_{SC} and long wavelength QE were less than with comparable thickness $Cu(InGa)Se_2$. To implement light scattering into $Cu(InGa)Se_2$ devices experiments were done to determine if ITO films could be sufficiently textured using a post-deposition etch. It was found that the films could be textured with HCl but efforts to implement this into processing of $Cu(InGa)Se_2$ cells was not successful with either shunting or very low current.

A third subtask on $CuInSe_2$-based solar cells has focused on "Increased V_{OC} for Improved Module Performance." In this effort our objective was to develop processes to increase V_{OC} in $Cu(InGa)(SeS)_2$ solar cells by controlling film growth and composition. This work has focused on controlling the composition of the pentenary $Cu(InGa)(SeS)_2$ in its formation by the reaction of Cu-Ga-In precursors in H_2Se and H_2S and in elemental co-evaporation to deposit $Cu(InGa)(SeS)_2$.

For $Cu(InGa)(SeS)_2$ films formed by 5-source elemental evaporation we have previously determined the effect of changes in [Cu]/[In+Ga] and [Ga]/[In+Ga] on the relative S incorporation at 550°C substrate temperature. In this work, the dependence of the relative Se and S incorporation chalcogen in $Cu(InGa)(SeS)_2$ on the substrate temperature was characterized with various [S]/[Se+S] flux rate ratios of at T_{SS}. The chalcogen incorporation is the same at 450 – 550°C for both Cu-excess and Cu-deficient growth. However, at 300°C the relative [S]/[Se+S] composition changes when films are grown without excess Cu. The chalcogen incorporation is compared to predictions from equilibrium thermodynamics and to an empirical kinetic model.

For $Cu(InGa)(SeS)_2$ films formed by the reaction of $Cu_{0.8}Ga_{0.2}$/In precursors, a sequential H_2Se/H_2S reaction process has been used to control through-film composition, avoiding the accumulation of Ga at the back of the film which occurs with reaction in only H_2Se. The effect of reaction temperature on film formation and compositional uniformity was evaluated in precursors first selenized in H_2Se at 450ºC for 15 minutes, then sulfized in H_2S for 30 minutes at fixed temperatures over the range 450 to 550ºC. An abrupt increase in the degree of Ga homogenization is observed for samples sulfized at temperatures of ~500ºC and above, along with a more general increase in S incorporation in the film with increasing temperature.

Finally, methods are being investigated to control through-film composition in the formation of $Cu(InGa)(SeS)_2$ films by the reaction of metal precursors by incorporating a copper selenide layer in the precursor to circumvent the formation of Cu-Ga-In intermetallic phases. CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors were formed by combinations of electrodeposition, annealing, and electron beam evaporation of Ga and In and compared to the sputtered $Cu_{0.8}Ga_{0.2}$/In precursors. The relative Ga distribution through the film was characterized by XRD and EDS measurements and shown to vary with the different precursor structures. Device results suggest that the precursors containing the binary Cu-selenide phases are reacted in less time than the metallic precursors.

CIS Collaborations

IEC has collaborated with, or provided assistance to, several other university of industrial groups working on $Cu(InGa)Se_2$ solar cells in the past year. These include:

<u>Ascent Solar, Dow Chemical, HelioVolt, Nanosolar, SoloPower, Solyndra</u>

IEC has leveraged its expertise, baseline processes, and characterization facilities to assist these $Cu(InGa)Se_2$ companies in a variety of ways, including:

- reacting precursor films to form $Cu(InGa)(SeS)_2$ and characterizing the resulting materials.
- fabricating cells to validate their cell fabrication processes.
- analysis of materials and devices supplied by the companies.
- supplying films or devices for comparison to their materials or calibration of their measurements.

<u>Battelle - Pacific Northwest National Laboratory</u>

Baseline IEC $Cu(InGa)Se_2$ devices were provided to Larry Olsen for encapsulation and stability studies including damp heat tests.

University of Florida

IEC prepared samples for studies of reaction chemistry and kinetics to the group of Tim Anderson. Specifically, stacked (Ga-Se)/(Cu-Se) samples along with control samples from the separate Ga-Se and Cu-Se runs were deposited.

University of Illinois

IEC provided $Cu(InGa)Se_2$ films to the group of Angus Rockett for photoluminescence measurements. These included different films with varying [Cu]/[In+Ga] and [Ga]/[In+Ga] composition ratios.

University of Nevada, Las Vegas

$Cu(InGa)Se_2$ and $Cu(InGa)(SeS)_2$ films were sent to the UNVL group of Clemens Heske for IPES/UPES measurements to characterize the electronic structure of the films. These include a wide range of different compositions including systematic variation in [Cu]/[In+Ga], [Ga]/[In+Ga], and [S]/[Se+S].

University of Oregon

IEC and Oregon continue to collaborate closely to characterize opto-electronic properties of solar cells with $Cu(InGa)Se_2$ as a function of absorber alloy composition, sodium incorporation, and other processing conditions, with IEC providing sample sets with different compositions or substrates for analysis. In this contract period IEC prepared and sent two sets of samples. The first was a set of $Cu(InGa)(SeS)_2$ devices with fixed [S]/[Se+S] ≈ 0.25 and varying [Ga]/[In+Ga] and the second was a set of devices with soda lime glass and Ti foil substrates to control the Na content.

Si-based Solar Cells

The Si effort has been directed towards fabricating, characterizing, and modeling Si solar cells based on n-type Cz wafers with deposited contacts and emitters with the goal of improving V_{OC}. Studies of deposition, structure and electrical properties of thin PECVD Si layers combined with "effective lifetime" measurements, and heterojunction modeling has given insight into mechanisms responsible for improving the effective Si wafer surface passivation.

Silicon surface passivation of hydrogenated silicon (Si:H) thin films deposited by radio frequency (RF) and direct current (DC) plasma process was investigated by measuring effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers and correlated with the silicon heterojunction (SHJ) cell performances. Apparently the higher ion bombardment in DC compared to RF plasma during growth of a-Si (a-Si:H) layer does not deteriorate Si surface passivation properties. Microstructural defects associated with SiH_2 bonding have only a weak influence on τ_{eff}. However, any epitaxial growth or presence of crystallinity in the Si:H i-layer severely degrades

passivation properties and SHJ cell performance. Excellent surface passivation ($\tau_{eff} > 1$ msec) and high efficiency SHJ cells are obtained by both RF and DC plasma-deposited intrinsic a-Si:H buffer layer. High efficiency (>18%) with open circuit voltage (V_{OC}) of 694 mV was achieved on n-type textured Cz wafer using DC plasma process.

Interpretation of photovoltaic cell performance through current-voltage testing depends largely on accurate representation of the band structure. This is especially true when considering the numerous interfaces found in a silicon heterojunction (SHJ) cell comprised of deposited a-Si:H emitter, passivation layers, and back contact with a crystalline silicon (c-Si) wafer absorber. Therefore, we determined the electronic levels of the valence and conduction bands, Fermi position, and electron affinity of thin film p-, i-, and n-type a-Si:H as well as (n)c-Si for use in SHJ modelling and performance optimization. Novel application of wet chemically H-terminated a-Si:H enables the study of device quality films to be studied via ultra-violet and X-ray photoemission spectroscopy. It is shown that this H-termination strategy effectively removes native oxide without introducing detectable surface states. The Fermi level varies within a bandgap of ~1.75eV from 1.3 – 0.70eV from the valence band maximum depending on doping and plasma conditions. The electron affinity is measured to be approximately 3.91eV for i-type films, 3.83 for n-type and a surprisingly low 3.37eV for p-type. Also the validity of Fermi level alignment of (p)c-Si/a-Si:H heterojunctions is called into question.

An interdigitated back contact silicon heterojunction solar cell has been developed. It combines the high voltage potential of heterojunction solar cells while avoiding the absorption losses in these structures which allows high short circuit currents. This structure has interdigitated p/n a-Si:H-films deposited by low temperature plasma enhanced chemical vapor deposition on the backside of crystalline silicon (c-Si) wafers, with the light irradiating the front surface. The device is attractive for manufacturing due to the all back contact design, the large tolerances in dimensions, low temperature of depositions, and the lack of shunting. Initial solar cells have open circuit voltages of 691 mV but low fill factors. A device was measured at NREL with 11.8% efficiency. High shunt resistance is evidence that the emitter and contact remain isolated despite the relatively simple masking procedure. Two-dimensional modelling is used to explain the present low fill factors obtained with the intrinsic a-Si buffer layer and demonstrates that the structure allows efficiencies in excess of 24%. Very good agreement is shown between measurement of the spatial variation of an LBIC signal across the interdigitated emitter and contacts and the 2D model confirming the assumptions about the device operation and the material parameters used in the model.

Si Collaborations

IEC continued support of Si wafer-based cell development at BP Solar. Deposition of various contact layers and characterization of optical, electrical and junction properties was carried out on their wafers. We assisted Advent Solar in evaluation of anti-reflection and passivation layers on their wafers as well.

Regarding a-Si based thin film PV companies, IEC is supporting Sencera and Sierra Solar in developing their process technology.

Diagnostics and Process Control

Process diagnostics are critical to evaluate and monitor the processing of thin film solar cells to maintain yield and avoid a large amount of off-spec production. To implement process diagnostics in real time requires both process and product monitoring as well as process control. Previous reports have contained our work on using contact wetting angle and X-ray diffraction as process monitors. During this period, graduate student Kapil Mukati completed his dissertation, "An alternative structure for next generation regulatory controllers and scale-up of $Cu(InGa)Se_2$ thin film co-evaporative physical vapor deposition process" awarded by the Department of Chemical Engineering for research conducted at IEC under the direction of Drs. Birkmire and Eser. It describes the process control needed to implement in-line real-time process diagnostics. A summary of that research is contained here. Further details may be found in his dissertation.

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Table of Contents

		Page
Summary		iii
	CdTe Solar Cells	iii
	CIS-based Solar Cells	iii
	Si-based Solar Cells	vi
	Diagnostics and Process Control	viii
List of Contributors		ix
List of Figures		xiii
List of Tables		xvii
1	Introduction	1
	1.1 CdTe-based Solar Cells	1
	1.2 $CuInSe_2$-based Solar Cells	1
	1.3 Si-based Solar Cells	2
	1.4 In-line Diagnostics	2
	1.5 Training and Education	3
	1.6 Publications	3
	1.7 Organization of the Report	3
2	CdTe Based Solar Cells	4
	2.1 Improving Module Performance	4
	2.2 Processing Devices with Thin CdTe Absorber	19
3	CIS-based Solar Cells	24
	3.1 In-Line Deposition of $Cu(InGa)Se_2$	24
	3.2 Improved Performance with Absorber Thickness < 1 μm	33
	3.3 Thin $CuInS_2$ Devices	35
	3.4 Textured TCOs for Light Scattering	37
	3.5 Composition Control for Increased V_{OC}	40

3.6 $Cu(InGa)(SeS)_2$ Formation by Cu-Ga-In Reaction in H_2Se/H_2S 42
3.7 $Cu(InGa)Se_2$ Formation by H_2Se Reaction of partially-selenized precursors 47

4 Si-Based Solar Cells 51
4.1 Surface Passivation Quality and Structure of Thin Si:H Layers on N-Type Crystalline Si (100) and (111) Wafers 51
4.2 Evaluation of HF Treated A-Si for Photoemission Determined Electronic Levels 56
4.3 A-Si/C-Si Heterojunction for Interdigitated Back Contact Solar Cell 65

5 Diagnostics and Process Control 73

6 Abstract 75

References 76

List of Figures

Page

Figure 1. Light AM1.5 and dark JV characteristics of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition. 7

Figure 2. Dark QE at 0V and -1V of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition. 7

Figure 3. GIXRD (1 deg incidence) of CdS/SnO_2/SLG before and after $CdCl_2$ vapor treatment. 10

Figure 4. Optical transmission of CdS films deposited by CSD onto SLG/SnO_2 after deposition (AD) and $CdCl_2$ vapor heat treatment (HT). 11

Figure 5. Sulfur on crystal CdS surface before sputter etching. Shading indicates peak fitting region for compositional analysis. 14

Figure 6. Sulfur on thin film CdS surface before sputter etching. Shading indicates peak fitting region for compositional analysis. 15

Figure 7. XPS spectrum of oxidized CdS film (sample 3) for Cd3d 5/2, showing multiple bond states attributed to Cd-S and Cd-O_2. 18

Figure 8. Optical micrographs of CdTe surface after deposition onto treated CdS. FOV in each image is 75 x 56 µm. 19

Figure 9. J-V plot of light and dark behavior of VT CdTe/CSD CdS sample VT279.1 with 1 micron thick absorber layer processed with vapor $CdCl_2$ and Cu/C contact. 23

Figure 10. QE versus wavelength of VT CdTe/CSD CdS sample VT279.1 with 1 micron thick absorber layer processed with vapor $CdCl_2$ and Cu/C contact. 23

Figure 11. Surface topography and cross-section of the Cu(InGa)Se_2 films deposited at a web speed of 0.75"/min (A) and 1"/min (B). 25

Figure 12. JV characteristics of devices fabricated on Cu(InGa)Se_2 film grown at a web speed of 0.75"/min. 26

Figure 13. JV characteristics of devices fabricated on Cu(InGa)Se_2 film grown at a web speed of 1"/min. 27

Figure 14. Surface structure of the Cu(InGa)Se_2 films deposited on SL glass at 550°C (left) and on Upilex at 450°C (right). Note the better developed grain structure at high temperature on SL glass. 29

Figure 15. Surface structure of the $Cu(InGa)Se_2$ films deposited at different speed on glass and on UpilexS substrates. 31

Figure 16. NaF deposition rate and correlation to published vapor pressure data. 33

Figure 17. AFM images of films with thickness (a) 2.2 µm, (b) 1.1 µm, (c) 0.5 µm, and (d) 0.35 µm. Each image shows a 10 x 10 µm area. 34

Figure 18. Relative loss in current due to incomplete optical absorption in $CuInS_2$ and $Cu(InGa)Se_2$ films. 36

Figure 19. Microstructure change with film thickness. 36

Figure 20. Spectral response depending on the absorber thickness. (a) external QE, (b) normalized internal QE, and (c) calculated from absorption coefficient of $CuInS_2$. 37

Figure 21. AFM images of (top) an as-deposited ITO film and (bottom) after etching in 10% HCl for 10 s at ~25°C. 38

Figure 22. J-V curves for 6 $Cu(InGa)Se_2$ cells on a sample with etch-textured ITO. 39

Figure 23. Relation between the [S]/[S+Se] ratios of the film composition (Y_{film}) and flux rate (Y_{flux}). The shape of symbol corresponds to the substrate temperature grown. Temperature: (■,□) 300°C, (▲,△) 450°C, (●,○) 550°. Open and closed symbols correspond to the Cu-poor and Cu-excess deposition condition, respectively. 41

Figure 24. Cross-sectional SEM images of reacted $Cu(InGa)Se_2$ (left) and $Cu(InGa)(SeS)_2$ (right) films. 43

Figure 25. Ga/III ratio measured by EDS at the $Cu(InGa)(SeS)_2$. "No" on the abscissa indicates selenization only. "Upstream" and "Downstream" indicate sample position for a given run. 44

Figure 26. $Cu(InGa)(SeS)_2$ (112) d-spacing for $Cu_{0.8}Ga_{0.2}$/In precursors selenized for 15 minutes at 450ºC then sulfized for 30 min at the indicated temperature. "No" on the abscissa indicates films processed by selenization only. 45

Figure 27. Residual Cu_9Ga_4 intermetallics on Mo back contact after delamination of $Cu(InGa)(SeS)_2$ formed by 15 min selenization at 450ºC followed by 15 minute sulfization at a temperature of 450ºC. 46

Figure 28. Cu-Ga phase diagram indicating transition of Ga-rich γ1 phase boundary from γ2 (solid) to a solidus line at 485ºC. 47

Figure 29. XRD scans of the $Cu(InGa)Se_2$ (112) peak after 90 min. selenization of CuSe/Ga/In, $Cu_{2-x}Se$/Ga/In, and $Cu_{0.8}Ga_{0.2}$/In precursors. Peak positions of $CuInSe_2$ and $CuGaSe_2$ are also indicated. 49

Figure 30. [Ga]/[In+Ga] ratios measured by EDS form the top and back sides of films selenized for different times. The dashed line shows [Ga]/[In+Ga] in the CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors and the solid line shows [Ga]/[In+Ga] in the $Cu_{0.8}Ga_{0.2}$/In precursor. 49

Figure 31. QE curves for devices with CuSe/Ga/In, $Cu_{2-x}Se$/Ga/In, and $Cu_{0.8}Ga_{0.2}$/In precursors after 90 min selenization. 50

Figure 32. Effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers after depositing 10 nm Si:H i-layer on both sides by RF and DC plasma CVD with varying hydrogen dilution (R). 52

Figure 33. Comparison of FTIR spectra of 10 nm thick Si:H i-layers grown by RF and DC plasma process with different R. 53

Figure 34. Imaginary part of pseudo-dielectric function, ε_2 as a function of photon energy for the Si:H i-layers deposited on Si(100) with R = 4 and 6 and on Si(111) with R = 6 in RF plasma process. 54

Figure 35. Open circuit voltage (V_{OC}) and fill factor (FF) of SHJ cells on Si (100) and (111) wafers with i-layers deposited at different hydrogen dilution (R) by RF and DC plasma process. 55

Figure 36. Surface atomic concentration from XPS. nox is the native oxide state, pox is post wet-chemical oxidation, HF is after HF dip. 58

Figure 37. UPS valence band spectra of RF (i)a-Si, 55eV photon energy probe beam. Bottom curve is untreated with native oxide surface, top curve is post HF-dip. Probed by 55eV radiation, curves vertically offset for clarity. 59

Figure 38. (a) Relative energy levels of the materials probed by UPS on the measured kinetic energy scale. (b) Schematic of band structure of Ag / c-Si / a-Si:H stack as probed assuming Fermi level alignment and absence of surface dipole. (c) Resulting electronic levels of isolated materials. Variables defined in body of text. 61

Figure 39. (a) Standard front junction design. (b) Rear junction design with interdigitated back contacts (IBC-SHJ). Devices are fabricated with and without the intrinsic buffer layers between the doped a-Si and c-Si. 66

Figure 40. Measured JV curves for front and rear junction solar cells. The i-layer has the same thickness of 10 nm in both devices. 68

Figure 41. Modelling of front and rear junction cell with Sentaurus. The loss in FF on the IBC-SHJ cell matches the experimental results in Figure 40. 69

Figure 42. Sentaurus modelling of an IBC-SHJ solar cell. The line with dots shows the fit to the 680 mV device indicating that the front surface recombination velocity is 80 cm/s. 70

Figure 43. Effect of the width of n-strips on J_{SC}. The total device dimension is fixed so wider n-strips result in narrower p-strips. 71

Figure 44. Comparison of the Sentaurus theoretical model to the experimental data from a LBIC scan. 71

List of Tables

Page

Table I. Summary of cleaning and rinsing procedures used for 10 cm x 10 cm TEC15 plates. 5

Table II. Best cell JV parameters for VT cells processed with different glass and window layer preparation. 6

Table III. Window layer processing procedures for 4 baseline CdTe depositions. 8

Table IV. Cell results for different window layer processing. 9

Table V. Surface photovoltage of as-deposited CdS films fabricated by different methods onto Ga_2O_3/SnO_2/SLG substrates. 12

Table VI. CdS single crystal and thin film surface composition determined by XPS. 14

Table VII. Measured oxidation rate for VT CdTe film surface at 400°C. 20

Table VIII. Best cell results for samples processed from a single VT plate with baseline (2 minute) $CdCl_2$ treatment time and reduced (30 second) treatment time. 20

Table IX. Yield and best cell for VT CdTe/CdS with 3 µm thick CdTe processed with and without pinhole mitigation technique. 21

Table X. W(V) obtained from SR_B analysis and C-V measurements for cells with ZnTe:Cu contacts, different CdTe thickness and having 11% conversion efficiency. 22

Table XI. Composition of the $Cu(InGa)Se_2$ films deposited at 0.75"/min and at 1"/min web speed. 24

Table XII. Deposition parameters and device performance of $Cu(InGa)Se_2$ deposited on SL glass and polyimide substrate using the substrate carrier. 28

Table XIII. Summary of the materials and device characteristics of $Cu(InGa)Se_2$ films deposited at different speed. 29

Table XIV. $Cu(InGa)Se_2$ films deposited for different times and rms roughness determined form AFM measurements. 34

Table XV. Device results (best and average of 6 cells per piece) using $Cu(InGa)Se_2$ with different deposition times and thicknesses. 35

Table XVI. Solar cell properties with thin $CuInS_2$ absorber layers. 37

Table XVII. Recent results on solar cell performance using evaporated $Cu(InGa)(SeS)_2$. 42

Table XVIII. Average EDS composition measurements of two $Cu(InGa)(SeS)_2$ films formed by 15 min selenization at 450ºC followed by 30 min sulfization at 450ºC. 46

Table XIX. Device parameters of solar cells made with 15 or 90 min selenized films. 50

Table XX. Summary of the SHJ cell performance on polished FZ (100), (111) and textured Cz wafers with the i-layers deposited by both DC and RF processes. The efficiency (η) values are not independently confirmed. 56

Table XXI. Electronic levels determined by UPS, all units in eV. Films on n-type substrates. 63

Table XXII. Electronic levels determined by UPS, all units in eV. Films on p-type substrates. 64

Table XXIII. Effect of intermediate buffer layers of V_{OC}'s on front and rear heterojunction devices. 67

1 Introduction

The primary objectives of this Institute of Energy Conversion (IEC) research are specific to the 3 types of thin film solar cells currently under commercial interest. In addition, generic process diagnostic and control tools will be developed. This report covers work performed from 4/01/07 to 12/31/07.

1.1 CdTe-based Solar Cells

The CdTe effort will address increased voltage and stability, the development of an in-line CdTe process to implement high rate and high throughput deposition on a moving substrate, and fundamental studies of CdTe surface chemistry. To meet these objectives, IEC will:

- Separate and quantify the effect on V_{OC} of high resistance (HR) buffer layers such as Ga_2O_3 and In_2O_3 and widening the CdS window layer bandgap with Zn.
- Develop and apply a transparent back contact to CdTe to probe back contact junction formation and degradation.
- Evaluate methods for increasing V_{OC} by reducing space charge recombination.
- Improve the stability of CdTe devices by developing alternative processing steps to 'stabilize' the junction and contact; and to compare the effects of well-controlled stress conditions on CdTe solar cells by performing detailed device analysis and relating results to differences in fabrication.
- Conduct detailed analysis of collection losses using conventional and bifacial devices, AMPS modeling, and JV measurements under different conditions.
- Develop the fundamental understanding needed for high throughput CdTe module fabrication by controlling high rate delivery of Cd and Te species to the moving substrate surface.
- Develop rapid and reproducible post-deposition processing alternatives to the current $CdCl_2$ vapor treatment.
- Determine relation between the contact processing and CdTe surface chemistry, and the device performance and stability.

1.2 $CuInSe_2$-based Solar Cells

The $CuInSe_2$-based effort will characterize fundamental properties of interfaces in $CuInSe_2$-based solar cells, develop approaches to improving V_{OC} including alloying with S and Al, and will also include the development of an in-line process for deposition on a moving substrate. To meet these objectives, IEC will:

- Develop the in-line deposition of $Cu(InGa)Se_2$ films from stationary elemental evaporation sources onto moving rigid (Mo coated glass) and flexible (Mo coated polyamide) substrates at rates commensurate with commercial manufacturing.

- Determine the relationship of the film properties, both compositional and structural, to the solar cell performance with particular emphasis on the effect of complex band-gap profiles due to the depth distribution of Ga and In and incorporation of Na.
- Increase the operating voltage by increasing the bandgap, E_g, in the absorber layer or in the space charge region using $Cu(InAl)Se_2$ alloys.
- Investigate the feasibility of controlled p–type doping of the $Cu(InGa)Se_2$ or $Cu(InAl)Se_2$ absorber layers to increase V_{OC}.
- Provide a fundamental understanding of surface reactions and interface chemistry in the fabrication of CIGS devices using atomic level surface characterization techniques to study the Mo surface, Mo/ $Cu(InGa)Se_2$ interface, the free $Cu(InGa)Se_2$ surface and $Cu(InGa)Se_2$/CdS interface.
- Determine reaction pathways for the formation of $Cu(InGa)Se_2$ and $Cu(InGa)(SeS)_2$ on H_2Se/H_2S time-temperature-gas concentration profiles using sputtered Cu/Ga/In precursors.
- Fabricate devices with CdS, ZnS, and CdZnS buffer layers and $CuInSe_2$ with Ga, S, and/or Al alloy absorber layers in order to characterize the effect buffer layers have on device behavior and fundamental interface properties.

1.3 Si-based Solar Cells

The Si-based effort will focus on increasing V_{OC} by improving surface passivation and the use of deposited amorphous Si layers to fabricate heterojunction solar cells. To meet these objectives, IEC will:

- Develop processing of c-Si heterojunction solar cells using PECVD deposited emitters and contacts with increased V_{OC}.
- Investigate alternative contact structures for c-Si solar cells utilizing improved passivation.
- Investigate chemical surface treatments leading to high effective lifetimes.
- Develop texturing approaches compatible with effective passivation.

1.4 In-line Diagnostics

The in-line process diagnostic effort will develop diagnostic tools needed for process control and the associated quantitative models that link sensor outputs to process variables and material properties. To meet these objectives, IEC will:

- Understand the fundamentals of thin film growth and identification of critical properties that lead to efficient solar cells, i.e., product specifications.
- Identify process parameters to which film properties are sensitive, i.e., process determinants.
- Develop robust, reliable and fast-response sensor equipment for in-situ applications in deposition reactors.

- Develop quantitative models that relate sensor output to process determinants and film properties for use in model based process control, i.e., intelligent process control.

1.5 Training and Education

During the period of this subcontract, IEC provided training and education for the following: 6 post-doctoral fellows; 8 graduate students; and 11 undergraduate students. Names are given in the list of contributors.

1.6 Publications

As a result of research performed under this contract, IEC published or submitted 17 papers.

1.7 Organization of the Report

This report is organized into four technical sections: CdTe-based solar cells, $CuInSe_2$-based solar cells, Si-based solar cells, and diagnostics. Each section describes the progress made at IEC in addressing the critical issues discussed above during the 18-month period of this contract.

2 CdTe Based Solar Cells

2.1 Improving Module Performance

2.1.1 Issues with Respect to Handling Commercial Glass

Experiments were conducted to isolate the effects on CdTe films and devices of the cleaning of the as received glass/SnO_2 prior to any other processing steps. None of the samples were pre-baked prior to cleaning. A gallium oxide (Ga_2O_3) buffer layer was formed on all samples by 1) electrodeposition of 15–20 nm Ga (ED Ga) followed by 2) oxidation for 15 minutes at 550˚C.

The method of cleaning and rinsing was varied to compare the length of time and type of solvent used for the wash, the purity of the water used for the rinse and the length of time and the temperature of the rinse (Table I). The solvent step was performed using our standard Crest cleaning system consisting of a 65˚C ultrasonic soap (Liquinox) wash or a room temperature ultrasonic methanol/isopropyl alcohol wash for the times indicated. The De-ionized water rinse was performed in our standard Crest cleaning system ultrasonic tank. The hot Nanopure water rinse was performed in a large clean beaker held within the ultrasonic tank at ~70˚C. For the 3 minute de-ionized water rinse the temperature of the tank water typically drops from 85˚C to 70˚C during that time period. For the 10 minute de-ionized water rinse, the temperature was maintained at 80˚C for the entire time. The water rinsed samples were dried in a forced hot air dryer while the methanol/isopropyl samples were dried with compressed argon gas. Following the oxidation step, all the samples received our baseline CdS and CdTe film deposition. Cells were processed with the established baseline vapor $CdCl_2$ treatment for 2 minutes at 480˚C and aniline treatment, with Cu/Ni contacts.

Table I. Summary of cleaning and rinsing procedures used for 10 cm x 10 cm TEC15 plates.

Run Number	CdTe Thickness (μm)	ED Ga Dep Time (min)	Ga Oxidation Time (min)	Solvent	Rinse	Comments
240	5.3	20	80	Ultrasonic Liquinox 3 min	Ultra DI 3 min	Control
267	5.9	e-beam	75	Ultrasonic Liquinox 3 min	Ultra DI 3 min	
268	8.7	10	15	Ultrasonic Liquinox 3 min	Hot Ultra Beaker Nanopure 3 min	
269	5.9	10	15	Ultrasonic Liquinox 3 min	Hot Ultra Beaker Nanopure 3 min	New N_2 cylinder
270	6.6	12.5	15	Ultrasonic MeOH/IPA 10 min each	none	New O_2/N_2
271		12.5	15	Mix Liquinox/IPA	Mix Ultra DI/None	6 I"X1" Substrates
272	7.9	12.5	15	Ultrasonic Liquinox 3 min	Ultra DI 3 min	Vacuum Stored after Ga_2O_3
273	9.4	12.5	15	Ultrasonic Liquinox 3 min Ultrasonic Liquinox 10 min	Ultra DI 3 min Hot Ultra DI 10 min	Cleaned twice (first time 8/06)
274	6.3	12.5	15	Ultrasonic Liquinox 10 min	Hot Ultra DI 10 min	

Table II summarizes the device performance obtained after different cleaning and rinsing procedures of the TEC15 substrates. Focusing first on the short circuit current (J_{SC}), a *dramatic* loss in photocurrent is obtained for 2 cases: 1) with standard detergent cleaning but rinsing in a fixed volume of clean water in a beaker; and 2) with a solvent-only clean (no water rinse). The JV and QE data for these low-J_{SC} cells is shown in Figures 1 and 2, respectively. The JV characteristics exhibit cross-over between the light and dark curves, with a soft diode and apparent voltage-dependent collection $J_L(V)$ effect. The QE, measured at 0V and at -1V, revealed only a weak dependence of collection with bias, with a constant ratio of the two measurements, suggestive of optical or interface loss. The correlation of this behavior with a low degree of rinsing strongly implicates electronic changes due to chemical contamination.

Table II. Best cell JV parameters for VT cells processed with different glass and window layer preparation.

Run Number	Glass/Window Clean and Ga deposition method	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
240.3	Control, ED Ga	782	24.8	68.8	13.3
267.3	Control, E-beam Ga	758	23.5	58.3	10.4
268.1	Beaker rinse, ED Ga	567	6.2	52.7	1.9
269.1	Beaker rinse, ED Ga	646	9.4	42.0	2.6
270.3	Solvent clean, ED Ga	666	2.1	49.9	0.8
272.1	Control, ED Ga	755	24.2	65.9	12.1
273.1	Long detergent step, ED Ga	707	18.8	55.7	7.4
274.1	Long detergent step, ED Ga	719	21.4	53.0	8.2

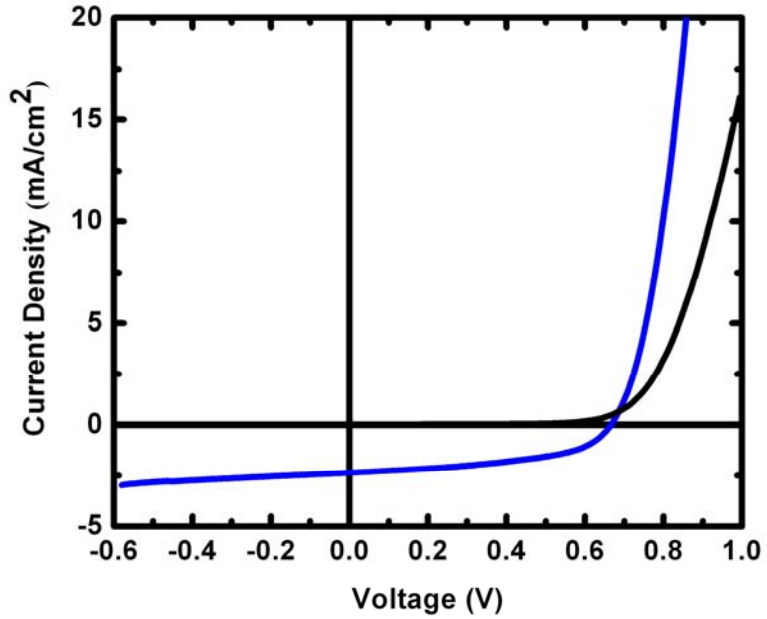


Figure 1. Light AM1.5 and dark JV characteristics of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition.

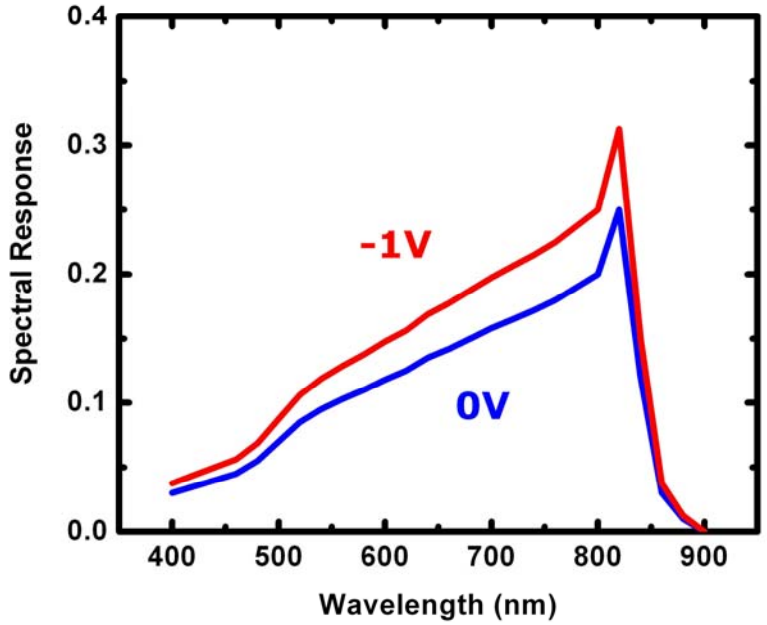


Figure 2. Dark QE at 0V and -1V of VT270, processed with solvent-only cleaning of the TEC15 superstrate glass/SnO_2 prior to ED Ga deposition.

Overall, the device results from Table II show that the most important glass handling step is the method of rinsing the glass after ultrasonic cleaning in Liquinox detergent, and that the detergent step is absolutely necessary for the TEC15 glass which has been cut by the supplier into 10 cm x 10 cm plates. The primary effect of insufficient rinsing in these samples is a loss in photocurrent and is likely due to low minority carrier lifetime, sufficient to kill transport through the film.

A further effort was initiated to examine the microscopic effects of different glass types, cleaning procedures and barrier layers on CdS film properties, with the goal of identifying the chemical agents responsible for reduced junction quality and transport. This will expand our understanding of the role of the buffer layer as both: 1) diffusion barrier against contaminants originating in different glass superstrates; and 2) electrical component in the device that reduces lateral effects from low quality, i.e., high recombination, junctions.

2.1.2 Comparison of Different TCO and Buffer Layers on VT CdTe/CdS Solar Cells

Based on earlier results evaluating baseline transparent conductive oxide (TCO) processing for CdTe/CdS thin film cells with vapor transport CdTe, we continued with the study of uncontrolled impurities originating in the TEC15 SLG/SnO_2 substrate. We examined variability of the TEC15 itself before comparing devices with identical processing but using different batches of glass/SnO_2. We also continued to examine ways to remove or bury the impurities from the glass and SnO_2 prior to any deposition by varying Ga thickness and adding an ITO barrier layer. The variations in TEC15 SLG/SnO_2 substrate preparation are listed in Table III.

Table III. Window layer processing procedures for 4 baseline CdTe depositions.

Run Number	TEC15 batch	Diffusion barrier	ED Ga Deposition Time (min.)	CdS Processing
272	current	none	15.0	
276	current	2200 Å ITO	12.5	
277	current	2200 Å ITO	12.5	Etch ½ CdS
278	2-year old	none	12.5	

One of the variations listed in Table III was the TEC15 TCO batch received from the supplier. We made a direct comparison of the TCO from our current supply to a piece saved from a batch we received two years ago. The substrates were cleaned using our standard Crest cleaning system consisting of a 65˚C ultrasonic soap (Liquinox) wash, followed by a de-ionized water rinse done in our standard Crest cleaning system ultrasonic tank. The water rinsed samples were then dried in a forced hot air dryer. A couple of substrates were coated with 220 nm thick ITO, deposited by rf sputtering. All samples then received an ED Ga coating and were oxidized for 15 minutes at 550˚C after cleaning. Following the oxidation step, all the samples received our baseline CdS and

CdTe film deposition. In one case (VT 277), half of the CdS film was immersed in glacial acetic acid for 1 minute; this is a selective etchant for the native oxide $CdSO_4$. Cells were processed with the established baseline vapor $CdCl_2$ treatment for 2 minutes at 480˚C and aniline treatment with Cu/Ni contacts. The best cell results are listed in Table IV.

Table IV. Cell results for different window layer processing.

Plate and Cell Number	TEC15 batch	Diffusion barrier	Ga dep (min)	CdS Etch	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)
272.1-7	current	none	15.0	N	755	24.2	65.9
276.2-3	current	ITO	12.5	N	526	17.1	45.3
277.1-6	current	ITO	12.5	Y	582	23.2	52.6
277.2-4	current	ITO	12.5	N	583	22.5	44.7
278.1-1	2-year old	none	12.5	N	704	25.5	65.2

Cells made with no special processing and with old and new batches of TEC15 TCO exhibit comparable performance. The device with longer Ga deposition (VT272) has slightly higher V_{OC}. The addition of an ITO layer to the TCO prior to Ga_2O_3 (VT 276 and VT 277) yielded lower V_{OC}, J_{SC} and FF. Thus, adding an ITO barrier coating had the unexpected effect of reducing V_{OC} and FF. The additional etch of CdS in glacial acetic acid prior to CdTe deposition did not affect the V_{OC} and marginally improved the other parameters.

2.1.3 Effects of CdS Processing

The baseline IEC CdTe cell process utilizes CdS deposited by chemical surface deposition (CSD) in a three-step process.[1] A detailed investigation of the CdS growth and materials properties such as surface chemical state was carried out to isolate potential effects on device operation and cell performance. The motivation for this work is to understand the influence of variations in CdS processing, such as oxidation, which results from high temperature environment of CdTe deposition and from long-term storage.

Using measured optical absorption in the high absorption regime of CdS (400 nm), each coat of CSD CdS is found to add ~40 nm. Thus, the growth is linear with time, corresponding to a rate of 8 nm per minute. The baseline process also utilizes a thermal treatment in $CdCl_2$ vapor and air. This treatment does not alter the measured CdS thickness of CdS but changes other properties, particularly the surface composition.

Atomic force microscopy was used to analyze the morphology of the terminating surface of the CdS film. The r.m.s. surface roughness and size of CdS features were insignificantly changed by increasing film thickness or heat treatment. This is consistent

with the conformal growth offered by the CSD process. Glancing incident x-ray diffraction (GIXRD) analysis indicates that the CdS film exhibits hexagonal structure (Figure 1). The strongest reflections belong to the (110) and (002) planes. After the heat treatment, all peaks sharpened, indicating a high degree of crystallization after heat treatment. Three additional reflections appear: CdS (100), (101) and (110) (Figure 3) and films become more randomly oriented after the treatment. This is verified by the calculation of the texture coefficient of different CdS planes. For all three samples, the coefficients are much closer to one after the heat treatment, indicating random orientation. Note that although GIXRD with two-circle goniometer cannot be used to accurately assess preferred orientation, it does permit verification of random orientation. From this result and that of grain size described above, it can be concluded that grain orientation occurs without grain growth, so the heat treatment provides sufficient energy for primary recrystallization but not grain coalescence. The tetragonal SnO_2 film was unchanged by the heat treatment.

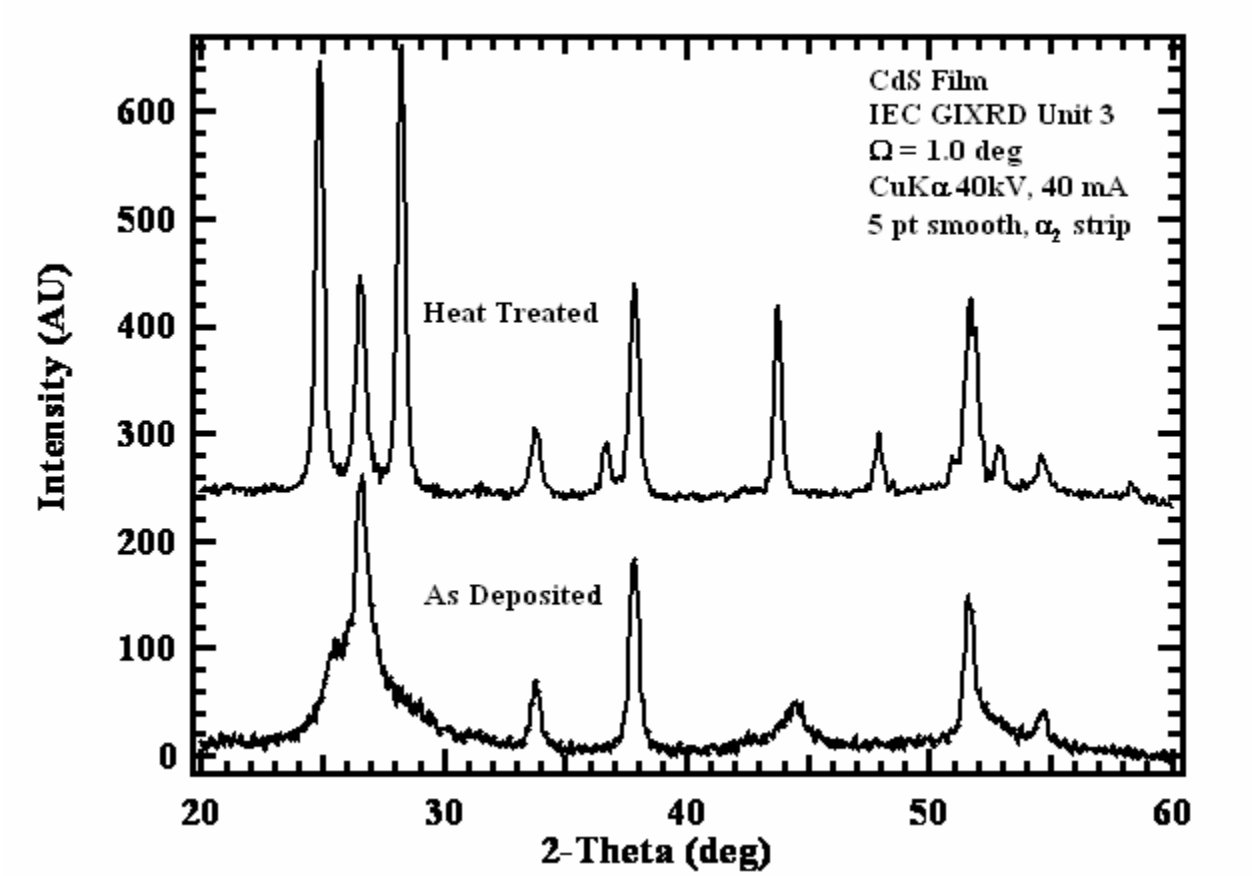


Figure 3. GIXRD (1 deg incidence) of CdS/SnO_2/SLG before and after $CdCl_2$ vapor treatment.

With increasing CdS thickness, the average optical transmission between 500nm (2.49eV) and 900nm (1.38eV) decreased from 90% (no CdS) to 82% (3 coats) (Figure 4). After heat treatment, the average film transmission in the red increased by approximately 1% and the transmission edge sharpened, consistent with enhanced crystallinity after the

heat treatment. A linear relation between $(\alpha h\nu)^2$ and $h\nu$ shows that as-deposited CdS is a direct band gap material with extrapolated band gap energy $E_G = 2.50$eV. After $CdCl_2$ heat treatment, the band gap decreased to about 2.40eV, close to the accepted value for single crystal CdS.

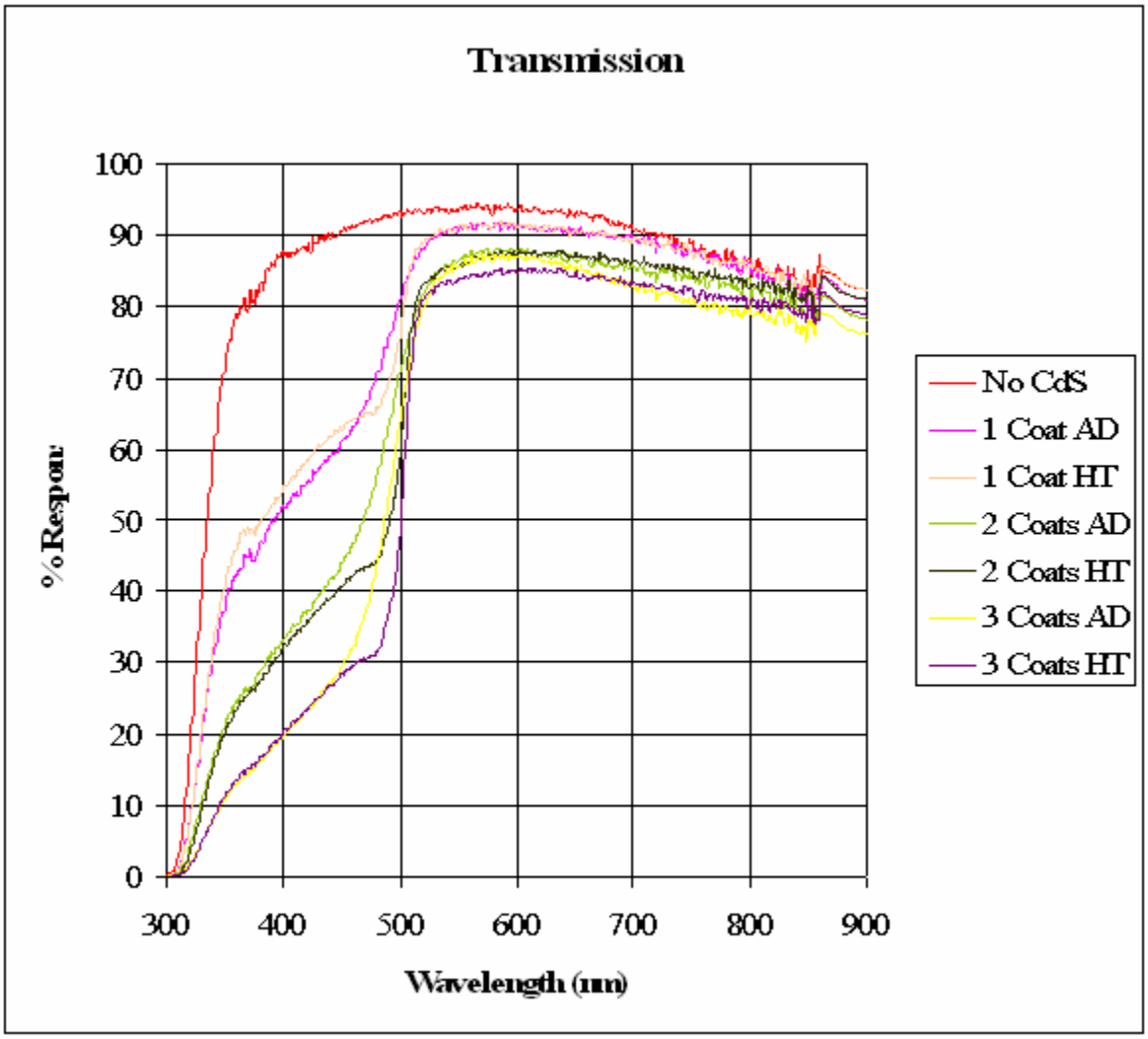


Figure 4. Optical transmission of CdS films deposited by CSD onto SLG/SnO_2 after deposition (AD) and $CdCl_2$ vapor heat treatment (HT).

X-ray photoemission spectroscopy (XPS) analysis was carried out on the sample receiving three coats of CdS. The atomic concentrations of deposited thin film showed that S/Cd = 1: 0.62, S/O = 1: 0.58 and S/C = 1: 0.97 indicating that the surface is sulfur rich. After heat treatment, the results were S/Cd = 1: 0.64, S/O = 1: 1.86, and S/C = 1: 5.31 indicating that the ratio of S to Cd stays the same before and after $CdCl_2$ heat treatment, while oxygen and carbon increased significantly. Further work is planned to examine the depth profile of composition, and the effects of surface treatment: 1) vacuum heat treatment to desorb excess oxygen, sulfur, carbon, etc., and 2) acetic acid etch treatment to remove compounds such as $CdSO_4$.

In thin film superstrate CdTe devices, CdS is the optimal heteropartner to obtain good junction performance. However, the CdS contributes negligible current to the total output and a fraction of the CdS film is lost during cell processing due to diffusion into the CdTe absorber layer; the precise quantity varies from 10-40 nm depending on the CdTe grain size distribution, deposition temperature and post-deposition treatment temperature-time conditions. The high degree of coupling between the CdS thickness and V_{OC} requires careful control of CdS thickness during the CdTe deposition and post-deposition processing. For high throughput processing of large area devices needed for modules, obtaining optimal performance and uniformity would furthermore require critical control of temperature uniformity and time. A poorly understood aspect of window layer processing for CdTe cells is the relationship between the CdS surface chemistry and electronic properties which can affect the junction. In particular, the role of native oxides on CdS, the effect of impurities from soda-lime glass on CdS and the electronic state of the CdS film is neither understood nor controlled. These issues are being addressed by characterizing the CdS surface chemistry using x-ray photoemission spectroscopy (XPS) and the electronic state by surface photovoltage analysis.

The surface photovoltage of CdS films was characterized by measuring the open-circuit voltage obtained with liquid junctions using aqueous quinhydrone (pH = 3.5) and polysulfide (pH = 12) electrolytes with platinum electrodes. The redox potentials of these electrolytes are favorable for comparative diagnostics of CdS electronic properties and surface states. The redox potentials of the quinhydrone and polysulfide solutions were 4.65 V and 4.91 V, respectively, with respect to vacuum level. Measurements were made using 0.02 cc drops of electrolyte applied to the CdS surface followed by insertion of a Pt wire. The device configuration was illuminated with an ELH tungsten filament lamp at 80 mW/cm^2. CdS films deposited by different techniques were compared in as-deposited conditions with the two electrolytes (Table V). The deposition methods evaluated were chemical surface deposition (CSD) at 55°C, physical vapor deposition (PVD) at 200ºC, and close space sublimation (CSS) at 600°C. All films were deposited at IEC using ACS grade $CdSO_4$ and thiourea for CSD films and GE high purity CdS powder (6N purity) for PVD and CSS films.

Table V. Surface photovoltage of as-deposited CdS films fabricated by different methods onto Ga_2O_3/SnO_2/SLG substrates.

Sample	Deposition Method	Temperature (C)	V_{OC} Quinhydrone (mV)	V_{OC} Polysulfide (mV)
P175	CSD	55	-300	-400
41242	PVD	200	-505	-750
CdS001	CSS	600	-550	-650

In Table V, higher surface photovoltage was obtained with polysulfide electrolyte than with quinhydrone, in part due to the higher redox potential of the former, which

allows for a greater built-in potential for junctions with CdS. The measured potential difference (typically 100 mV) is less than the redox potential difference of the electrolytes (260 mV), indicating different flat-band potentials for these electrolytes in contact with CdS. The surprising difference is the nearly consistent increase in surface photovoltage obtained at progressively higher deposition temperatures. While the results for the CSD films in polysulfide electrolyte are consistent with those reported for CdS single crystal in similar solution[23], the evaporated films yielded significantly higher photovoltages, which is consistent with a shift on the CdS Fermi level towards the conduction band, i.e., greater n-type conductivity, or a reduction in the density of surface states. We will continue to employ this simple technique as a tool for correlating changes in CdS processing with surface chemistry and performance of CdTe/CdS solar cells.

The surface composition of single crystal CdS and thin film CdS deposited by chemical surface deposition (CSD) was measured by x-ray photoemission spectroscopy (XPS) using a Physical Electronics system with Al x-ray source. As shown in Table VI, the single crystal and CSD thin film compositions are very similar (Table VI first two rows) with the atomic concentration ratio of Cd/S close to unity. Physically adsorbed carbon comprises about 20% of the surface and slightly lower oxygen quantity was detected. For the sulfur component peaks at 168.997eV (Figure 5 crystal CdS) and 169.077eV (Figure 6 thin film CdS) are found on each specimen. The positions of the peaks show that part of the sulfur is bound as sulfate, likely due to native oxides formed on the surfaces of both crystal and thin film CdS during storage. The atomic concentration ratio of sulfur in sulfate state to oxygen is about 1:5.

After 10 minutes of Ar^+ ion milling of the single crystal CdS surface, oxygen and carbon signals decreased and the Cd/S ratio did not change. For the sulfur, the peak around 169 eV disappeared, indicating removal of sulfate below the crystal surface. The etching of thin film CdS produced similar results and we determined the thin film CdS etch rate in Ar+ to be about 4-5 nm per minute. However, after etching 30 seconds, the carbon signal on the thin film CdS reduced to the detection limit.

Table VI. CdS single crystal and thin film surface composition determined by XPS.

CdS Samples	Cd (3d5/2)		S (2p3/2)		O (1s)		C (1s)	
	Position (eV)	At. Con. (%)	Position (eV)	At. Con. (%)	Position (eV)	At. Con. (%)	Position (eV)	At. Con. (%)
Crystal (surface)	405.495	31.4	161.791 (168.997)	31.3	532.019	13.8	285	23.5
Thin film (surface)	405.724	31.2	161.964 (169.077)	31.0	532.359	17.7	285	21.1
Crystal (10 min etching)	405.000	41.0	161.319	40.3	531.462	4.3	285	14.4
Thin film (30 sec etching)	405.564	47.9	161.826	46.0	531.725	6.1	No Carbon	0
Thin film (60 sec etching)	405.481	49.2	161.744	48.7	531.867	2.1	No Carbon	0

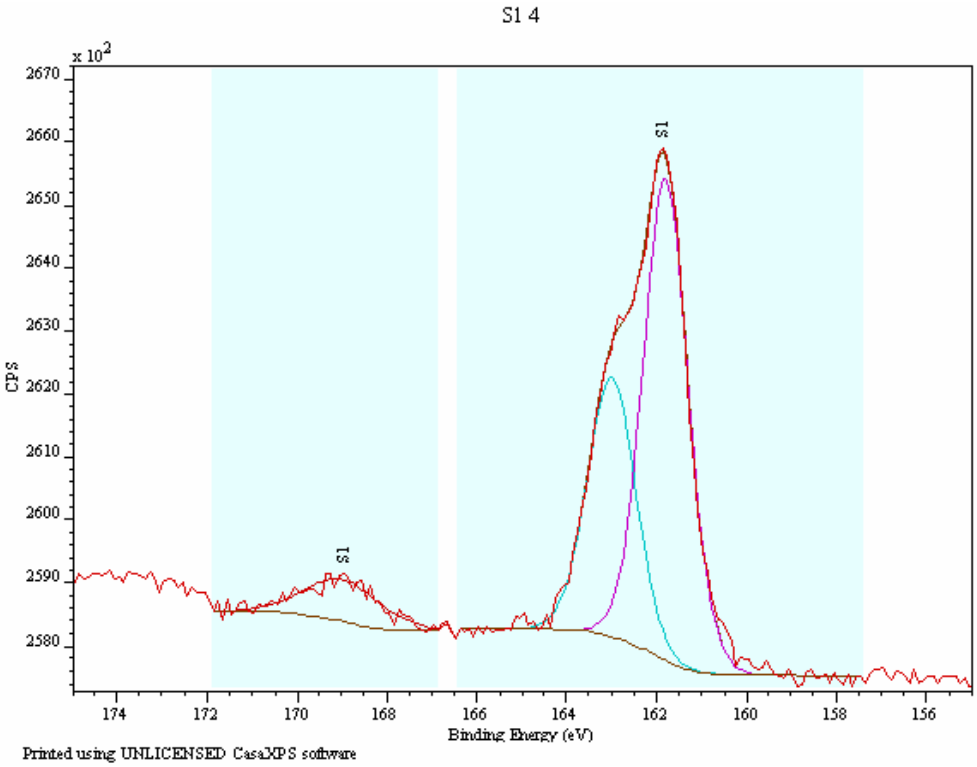


Figure 5. Sulfur on crystal CdS surface before sputter etching. Shading indicates peak fitting region for compositional analysis.

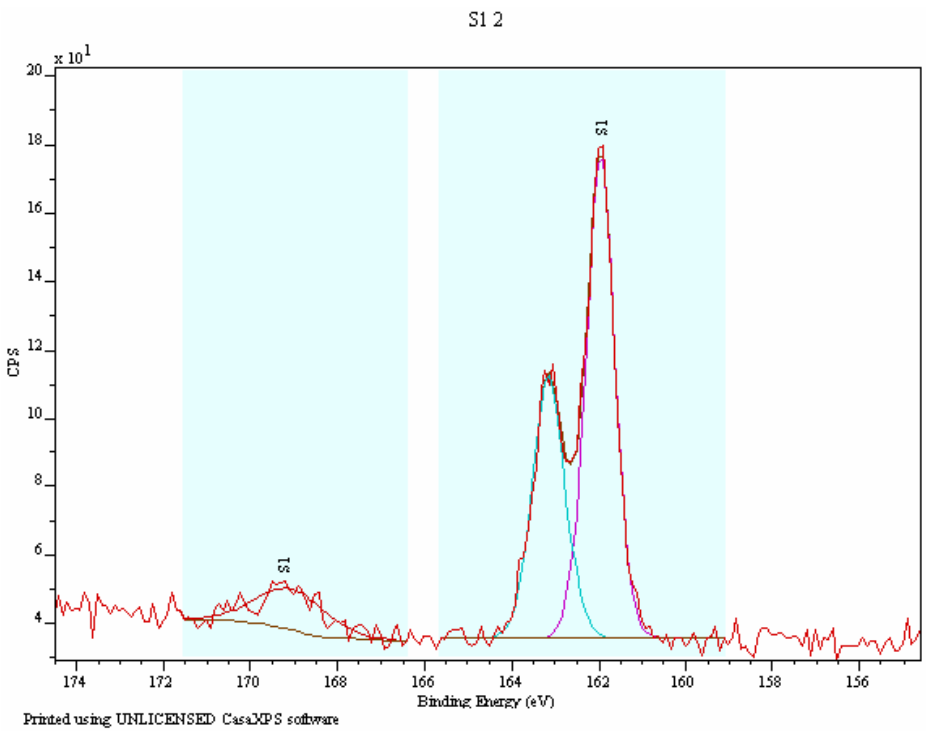


Figure 6. Sulfur on thin film CdS surface before sputter etching. Shading indicates peak fitting region for compositional analysis.

Two thin film samples deposited by CSD were analyzed by glancing incidence x-ray diffraction (GIXRD) to determine the crystalline phase content of the near-surface region for different processing methods. Samples were deposited with single and double concentrations of NH_4OH in otherwise similar solutions at 55°C. Both samples exhibited similar patterns, with a surface phase of $CdSO_4$.

Two identically deposited CdS films (single ammonia concentration) were then treated and analyzed. One sample was immersed in acetic acid at temperature 60°C for 10 minutes, while the other sample was heat treated in the air at a temperature of 450°C for two hours. Then both samples were analyzed by GIXRD within 10 minutes following each treatment, with the measurement taking 60 minutes. While the purpose of acetic acid treatment was removal of $CdSO_4$, the GIXRD results showed no difference with respect to before treatment, indicating either that acetic acid did not remove any oxides on the surface, or the oxide formation is so rapid that no difference can be detected by XRD, since XRD analysis took one hour to finish. The heat treatment should increase surface oxidation and the GIXRD results exhibit three additional peaks, corresponding to $Cd_3O_2SO_4$ and $CdSO_3$. In addition, recrystallization of CdS film was detected. From XPS results discussed above, the ratio of sulfur in sulfate state to oxygen is about 1:5. Therefore, it seems likely that both $CdSO_4$ and $Cd_3O_2SO_4$ phases may exist on the surface of the CdS thin film samples. The GIXRD data also suggests that a small quantity of $CdSO_3$ resides on the surface too; the particular oxides phases may form on different terminating surfaces of the CdS allowing oxides with different stoichiometry to form in addition to the widely cited stable $CdSO_4$ phase. Further information about

$Cd_3O_2SO_4$ and $CdSO_3$ is needed to determine the stability of this compound and if it can exist on the surface of CdS and this will be presented below.

GIXRD analysis of CSD CdS films deposited in the standard bath and then treated with $CdCl_2$ in air ambient at 450°C for 20 minutes also shows: $Cd_3O_2SO_4$, $CdSO_4$ and $CdSO_3$ phases before treatment and additional $Cd_3O_2SO_4$ after the treatment. Thus, for annealing with $CdCl_2$, additional oxides form on the surface. Experiments were conducted to try to modify the phase content of the surface using vapor anneal treatments.

Two fresh CSD CdS film samples were treated in 4% hydrogen-argon at temperature 500°C for 30 minutes to attempt to remove oxides from the surface. Calculation shows that the diffusion of O into bulk CdS is about 1.8×10^{-3}Å per hour. The GIXRD analysis duration is about 50 minutes, so CdS bulk should be slightly oxidized during the analysis. The first sample (718-15) was analyzed by GIXRD immediately following the hydrogen treatment, while the other sample (314-4) was stored in argon for 1 hour. The GIXRD analysis for both samples shows that two peaks corresponding to $Cd_3O_2SO_4$ were indeed reduced. Together with the results after heat treatment, we can see that the oxidation of CdS and reduction both occur in the form of oxide $Cd_3O_2SO_4$. Thus the problem now is controlling $CdSO_4$ and $CdSO_3$. Two CSD CdS films after $CdCl_2$ heat treatment were treated in hydrogen-argon at 600ºC for 60 minutes, with the result that both $CdSO_3$ and $Cd_3O_2SO_4$ were significantly removed from the GIXRD pattern.

An additional experiment was conducted to evaluate the effects of the CdS surface state (oxidized versus reduced) on the CdTe film properties and CdTe/CdS solar cell performance. Four different CdS surface conditions were evaluated: 1) standard CSD CdS with $CdCl_2$ treatment; 2) standard CdS with $CdCl_2$ followed by treatment at 600°C for 60 min in 4% H_2 balance argon; 3) standard CdS with $CdCl_2$ followed by treatment at 600°C for 60 min in dry air; and 4) standard CdS with $CdCl_2$ followed by treatment in glacial acetic acid. GIXRD and XPS were used to determine the surface chemical conditions; AFM and optical microscopy are used to study the surface topography; and optical T&R is used for the optical properties and the thickness of the thin film CdS. The results are summarized below.

Sample 1 is the standard CdS used in CdTe/CdS solar cell. Three coats CSD CdS provides 154 nm thickness. The surface roughness is 23 nm, and CdS grain size is about 0.6um. GIXRD indicates that in addition to CdS, $CdSO_4$, $Cd_3O_2SO_4$ and $CdSO_3$ may exist on the sample surface in trace quantities. XPS analysis of S 2p 3/2 and O 1s bond states confirms that there are indeed sulfates on the surface but not sulfite. So the first sample has CdS, $CdSO_4$ and/or $Cd_3O_2SO_4$ on its surface.

Sample 2 is sample 1 further treated with H_2 to remove any oxides or sulfates on the surface. The treatment reduced the CdS thickness to 109 nm, 45 nm thinner than before the treatment and the optical properties are otherwise nearly the same as sample 1, with the only change being with the transmission at short wavelengths, due to the reduction of CdS thickness. The mean roughness is 31 nm and the CdS grain size is 0.6 um. GIXRD

shows that the positions of peaks do not change, but the relative intensities of three main CdS peaks reduce to 60% of their original intensities, consistent with the thickness reduction. XPS analysis indicates dramatic reduction in O concentration and loss of sulfate bonding - sulfur 2p 3/2 spectra show absence of sulfate peaks (~169 eV). The O 1s peaks show that the remaining oxygen may be due to the substrate materials Ga_2O_3 and SnO_2 and is detectable due to the possible thinning/removal of CdS by the high temperature reactive treatment. Thus, $CdSO_4$ and $Cd_3O_2SO_4$ are removed by the H_2 treatment.

Sample 3 is sample 1 treated with dry air at 600°C for 60min to form heavy oxidation surface condition. The purpose of this treatment is to produce a thick layer of oxides to evaluate their effect on the primary junction in the device. The CdS thickness of the third sample is 102 nm, which is 52 nm thinner than sample 1. The AFM and optical microscopy both show that there are more large grain features on the CdS surface, and the mean roughness of this sample increased to 103 nm, compared with 23 nm for the standard sample. Optical transmission of this sample is quite low: Average transmission in the wavelength range 500-900 nm is 68.6%, compared with 84.6% of the standard sample. The band gap, evaluated by plotting $\alpha^2 h\nu$ versus $h\nu$, reduced from 2.46 eV to 2.15 eV, consistent with a phase change. GIXRD results show that 7 CdS disappear after dry air treatment and the remaining peaks correspond to the substrate materials, such as SnO_2 and Ga_2O_3. Five new peaks appear after the dry air heat treatment, which do not corresponding to either substrate materials or CdS and are due to $CdSO_4$, $Cd_3O_2SO_4$, and CdO. From XPS analysis of the Cd 3d 5/2 state (Figure 7), peaks are found consistent with Cd-S and Cd-O_2 bonding, suggesting the presence of CdS and CdO_2. The sulfur spectrum only shows the sulfate peaks, indicating a higher concentration of sulfate than CdS. Oxygen appears to exist as sulfate peak, CdO_2 or SnO_2 or Ga_2O_3, and CdO. So on sample 3 surface, there are CdS, $CdSO_4$ and/or $Cd_3O_2SO_4$, CdO and CdO_2.

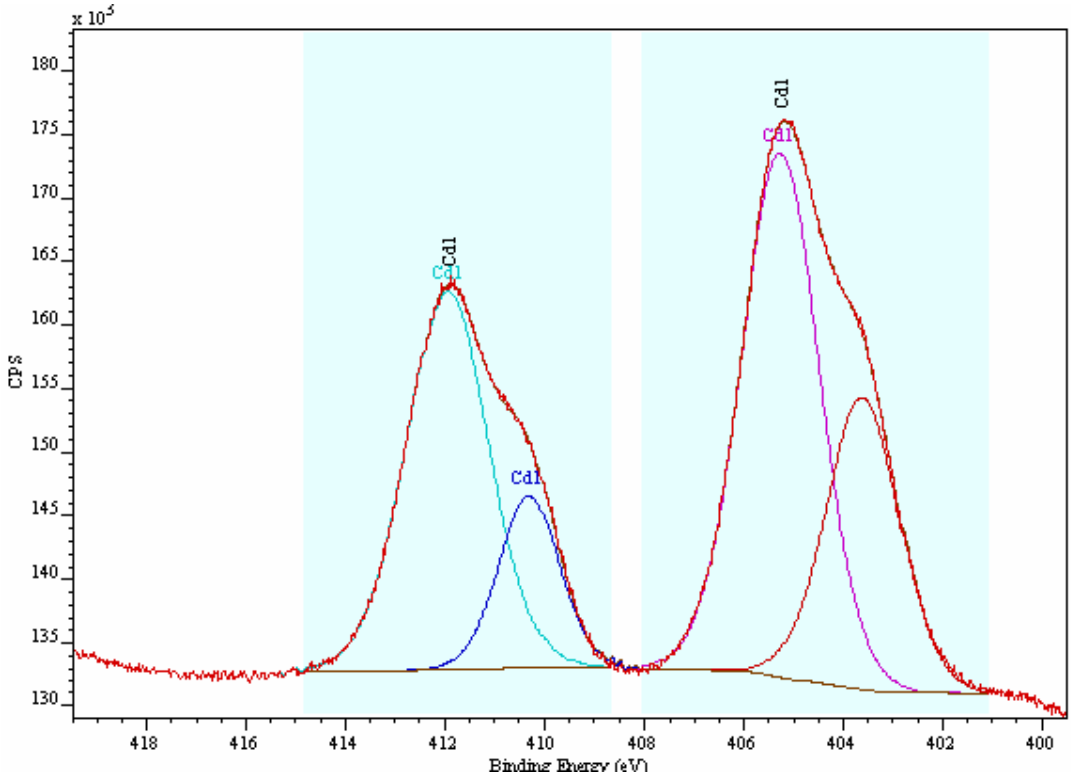


Figure 7. XPS spectrum of oxidized CdS film (sample 3) for Cd3d 5/2, showing multiple bond states attributed to Cd-S and Cd-O2.

Sample 4 is sample 1 treated with acetic acid to dissolve any sulfates on the CdS surface. The treatment was performed at 80~90°C for 20 min. The CdS thickness was reduced 22.4 nm to give a final thickness of 132 nm, with no detectable change in optical transmission. The CdS surface roughness increased slightly and the grain size did not change. The GIXRD results show the peak positions and relative intensities do not change after the acetic acid treatment. The XPS sulfur spectrum only has CdS peaks shown, no sulfate peak. Analysis of the O 1s peak shows oxygen is not in the sulfate state, nor in Ga_2O_3 or SnO_2 state. The oxygen may come from CdO or adsorbed O_2. So on the surface of sample 4, only CdS exists. The acetic acid treatment therefore removed the sulfate, $CdSO_4$ and/or $Cd_3O_2SO_4$.

VT CdTe was deposited on four samples immediately following each treatment with thickness 4-5 μm at a substrate temperature of 550°C and a growth rate of 10 μm/min. The surface morphology and grain features are evident in high magnification optical micrographs (Figure 8). Sample 1 has surface r.m.s. roughness 115 nm and CdTe grain size 3 μm. Samples 2 and 4 have similar results, with roughness 157 nm and 162 nm and average CdTe grain size 3 μm. Sample 3 has comparable roughness 113 nm, but significantly smaller CdTe grain size about 1.5 μm. The results show that CdTe crystallization is strongly influenced by the oxidized surface.

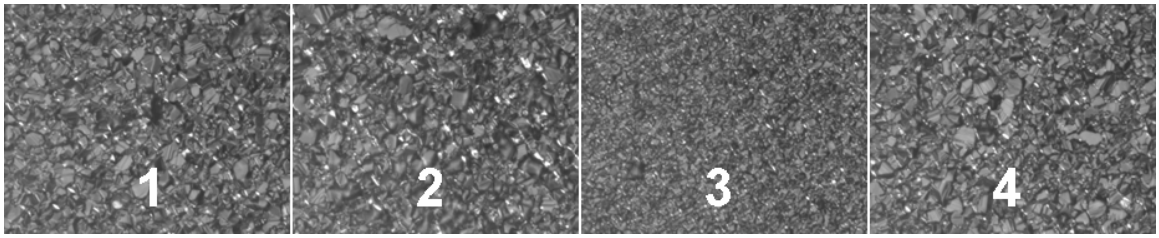


Figure 8. Optical micrographs of CdTe surface after deposition onto treated CdS. FOV in each image is 75 x 56 μm.

The performance of VT CdTe/CdS devices using these CdS films as well as additional samples treated at shorter times to prevent near-total conversion of CdS to oxides is being analyzed. Preliminary device analysis using liquid junction contacts show that samples 1 and 4 have baseline V_{OC}. Sample 2 (H_2 treated) has 100 mV lower V_{OC}, and sample 3 (oxidized) has the 500 mV lower V_{OC} than baseline.

2.2 Processing Devices with Thin CdTe Absorber

Over the past year, we have demonstrated the ability to maintain 11% baseline cell performance for cells with CdTe films deposited at ~10 microns per minute onto a moving substrate using reduced post-deposition processing time. Vapor $CdCl_2$ processing time was reduced to 1 minute, while aniline etching was reduced to 2 minutes. During the present reporting period, experiments were conducted to further reduce processing time, to less than 1 minute for these two post-deposition treatments. Modification of the treatment protocol for reduced time was guided by our knowledge of the diffusion and oxidation processes in the CdTe/CdS thin film structures. The solid state diffusion which consumes CdS via CdTeS alloy formation is a critical aspect of processing, whereby V_{OC} is reduced when the CdS film is consumed sufficiently to create discontinuities; 3D modeling of the diffusivity of interstitial Cd through the polycrystalline film, the limiting process, taking into account the grain size distribution, allowed equivalent temperature-time configurations to be determined.[4] Furthermore, oxide formation on films processed at 350°C to 500°C in air or in $CdCl_2$ vapor proceeds approximately linearly for times up to ~30 minutes, and the oxide composition and formation rate are both strong functions of the relative humidity of the ambient. Using GIXRD with *in-situ* heating plus atmospheric control and using XPS for *ex-situ* surface analysis, the oxidation rates, expressed as equivalent film accumulation rate, were determined for different temperatures and atmospheres (Table VII).

Table VII. Measured oxidation rate for VT CdTe film surface at 400°C.

Ambient P_T = 760 Torr $Ar/(Ar+O_2)$ = 0.80	Relative Humidity (%)	Crystalline Phases	Equiv film oxidation rate (nm/min)
$Ar + O_2$	<1	$CdTeO_3$	0.004
$Ar + O_2 + H_2O$	80	$CdTe_2O_5$	0.022
9 mTorr $CdCl_2$ + Ar+ O_2	<1	CdO, $CdTeO_3$	0.007
9 mTorr $CdCl_2$ + Ar + O_2 + H_2O	80	$CdTe_2O_5$	>0.050

By raising the sample treatment temperature, reducing the $CdCl_2$ vapor concentration, by reduction of source temperature, and reducing the oxygen concentration in the ambient mixture, we achieved samples which yielded no detectable surface oxide phases for treatments of 30 sec and 1 minute: GIXRD analysis of samples treated in $CdCl_2$:Ar:O_2 vapor for 1-2 minutes at 480°C and at 500°C for 30 seconds revealed no detectable oxides. In such cases, the back contact etch step can be completely eliminated while maintaining device performance (Table VIII). The samples all exhibited identical current densities but with slightly lower V_{OC} and FF for cells treated for 30 seconds.

Table VIII. Best cell results for samples processed from a single VT plate with baseline (2 minute) $CdCl_2$ treatment time and reduced (30 second) treatment time.

Run Number	$CdCl_2$ Step	Etch Step	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
240.3	2 min 480°C	2 min	782	24.8	68.8	13.3
240.4a	30 sec 500°C	1 min	744	24.8	62.2	11.5
240.4b	30 sec 500°C	none	741	24.8	66.8	12.3

Vapor transport depositions with reduced CdTe thickness have been carried out to provide plates to use post-deposition optimization experiments. Continuous films with thickness from 1 to 3 microns have been deposited onto CdS coated Ga_2O_3/TEC15 superstrates. Simple approaches for mitigating the effects of pinholes in CdTe are being developed to allow large area cells to be fabricated having comparable performance to small area cells. The pinhole mitigation treatment (PMT) relies on preferential formation of polymer insulators in pinhole regions. Table IX shows cell yield and performance data for samples with 3 micron thick CdTe deposited onto non-optimal CdS films; these films had been rejected for baseline processing due to the presence of a surfacial powdery CdS residue that often leads to pinholes in the CdTe film. The plates selected had >1 micron wide pinholes in the CdTe film at an area density exceeding 100 per cm^2. Sample 195.4 was processed without the PMT and only yielded one cell out of eight that was not shorted. An adjacent piece, VT195.2, was processed with the PMT and yielded six out of eight with similar performance to the only live cell on VT195.4. Finally, an entire plate, VT268, received the PMT and one 8 cm L x 0.9 cm W cell was fabricated, with

comparable V_{OC} to the small area cells made on the VT195 samples. The current and FF are low on this sample due to series loss, from non-optimized point contacts. The V_{OC} results, on materials with known mechanical deficiencies, demonstrate the efficacy of the PMT process for improving device yield in cases where marginal lateral film density has been obtained.

Table IX. Yield and best cell for VT CdTe/CdS with 3 μm thick CdTe processed with and without pinhole mitigation technique.

Run Number	PMT ?	Cell Area (cm^2)	Cell Yield	V_{OC} (mV)	J_{SC} mA/cm^2	FF (%)	Eff (%)
195.4	N	0.4	1/8	778	23.7	58.7	10.8
195.2	Y	0.4	6/8	778	24.0	50.0	9.4
268.1	Y	7.0	1/1	781	7.1	28.3	1.6

Exploratory vapor transport depositions in other growth regimes than baseline are being conducted to facilitate deposition of dense pinhole-free CdTe films with sub-micron thickness. According to the VT growth model, several methods can be employed to reduce thickness: 1) increase translation speed; 2) decrease source temperature and linear flow velocity through the source; and 3) raise total system pressure. Baseline deposition of 6-7 micron thick films is carried out at a source temperature of 850ºC, total pressure of 20 Torr, and flow rate of 20 sccm in N_2 carrier gas and N_2:O_2 ambient. We have found that decreasing source temperature is not easily controlled and the carrier gas can become under-saturated, which yields non-uniform deposits. Increasing translation speed has yielded films with good thickness control and uniformity but with excessive pinholes. During this period, depositions were carried out at higher pressure, 100 Torr and lower flow rate, 2 sccm. For a weakly reactive carrier gas, such as N_2:O_2, these conditions are expected to increase doping effects from CdTe-gas interactions than at lower pressure. The obtained films were 0.7 micron thick and exhibited very low pinhole density and good uniformity. The improved quality of the deposit is attributed to uniform reduction of growth rate, obtained by increasing diffusion kinetics within the source.

The IEC VT deposition process is being used to deposit CdTe films with thickness approaching 1 micron suitable for cells with 11% conversion efficiency. However, the thickness uniformity of the obtained deposit is more difficult to control in the high deposition rate regime (10 μm/min) than for baseline thickness ~5-7 μm. Also, the films are more prone to having voids in the CdTe layer, which become shunt paths in devices. The post-deposition processing becomes more critical since thinner films have smaller grains and are therefore more sensitive to grain boundary-enhanced processes such as interdiffusion of CdS-CdTe, oxide penetration, and penetration from any etchants used to process the back contact. In the previous year of work, we showed that 11% baseline performance could be maintained with 1.5-3 micron thick CdTe by reducing the $CdCl_2$ vapor treatment processing time, using milder etchants, and reducing the Cu quantity at

the back contact, either by depositing a thinner layer or by incorporating the Cu into the ZnTe contact. Bifacial spectral response (SR) and capacitance voltage (C-V) analysis of CdTe devices with optimized performance at different CdTe thickness allowed the depletion width W and diffusion length L to be evaluated. The values for W and L deduced from SR_B analysis and W values measured by C-V are shown in Table X. There is excellent agreement for W from SR and C-V measurements for devices with different absorber thicknesses.

Table X. W(V) obtained from SR_B analysis and C-V measurements for cells with ZnTe:Cu contacts, different CdTe thickness and having 11% conversion efficiency.

Sample	Thickness (μm)	L(μm)	W(μm)			
			@ (-1.0V)		@ (0V)	
			SR	CV	SR	CV
B	8	0.76	5.5	5.4	4.8	4.8
C1	5	0.72	2.6	2.4	2.4	2.0
D	3	0.6	1.8	1.7	1.3	1.4

This data shows that the depletion width in optimized cells is approximately half the CdTe thickness, which is a result of the combined processing changes of reducing the $CdCl_2$ vapor treatment time, using a milder etch, and reducing the Cu quantity. This is the starting point for experiments using devices with VT deposited CdTe with 1 micron film thickness. VT CdTe depositions were carried out at a growth rate of ~6 microns/minute at a substrate temperature of 525ºC onto $CdS/Ga_2O_3/SnO_2$/SLG (TEC-15). The $CdCl_2$ treatment was carried out with the CdTe sample at 480ºC and the $CdCl_2$ source at 425ºC for 1 minute. A dilute hydrazine solution was used to remove oxides and form a thin Te layer. The back contact was fabricated by deposition of 2 nm Cu, reaction at 180ºC to form Cu_2Te and application of graphite paste. The best cells obtained had AM1.5 conversion efficiencies up to 7%, typified by low V_{OC} but good photocurrent and complete consumption of the CdS film, as shown in the J-V and QE plots below. In this device, the low V_{OC} and FF are undoubtedly related to the loss of CdS, with the primary junction now between the $CdTe_{1-x}S_x$ absorber and the Ga_2O_3/SnO_2 buffer layer. The QE data shows good photogeneration with the 1 micron absorber layer and relatively flat response from 550 to 820 nm. Effort is on-going to optimize the post-deposition treatment and evaluate the effect of CdS thickness and buffer layer properties in cells with thin CdTe absorber layers.

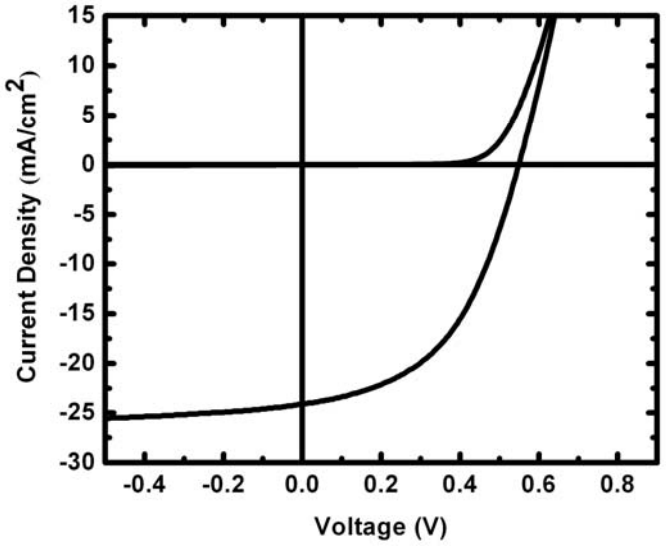


Figure 9. J-V plot of light and dark behavior of VT CdTe/CSD CdS sample VT279.1 with 1 micron thick absorber layer processed with vapor $CdCl_2$ and Cu/C contact.

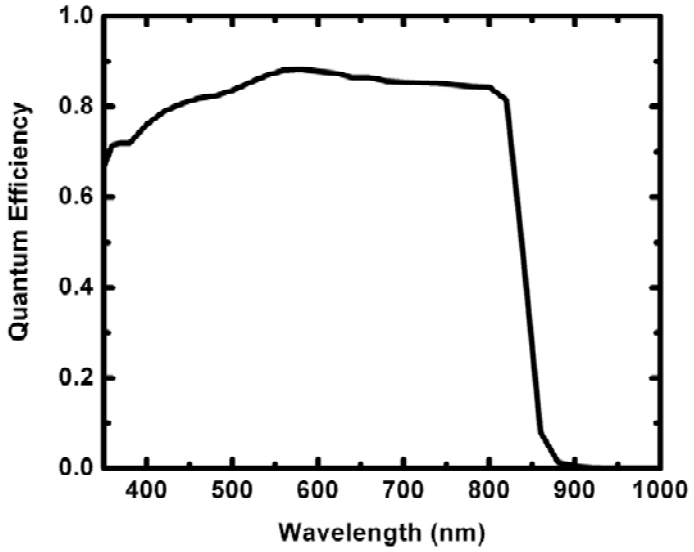


Figure 10. QE versus wavelength of VT CdTe/CSD CdS sample VT279.1 with 1 micron thick absorber layer processed with vapor $CdCl_2$ and Cu/C contact.

3 CIS-based Solar Cells

3.1 In-Line Deposition of $Cu(InGa)Se_2$

Two aspects of the in-line deposition of $Cu(InGa)Se_2$ films were investigated during this program. In the first case, the effect of the substrate translation speed, a measure of the deposition rate and film thickness was studied. In the second case, work was performed in developing a Na source to be installed into the in-line system for evaporative incorporation of Na into the $Cu(InGa)Se_2$ films on non-Na containing substrates such as UpilexS polyimide.

3.1.1 Effect of Substrate Translation Speed

Early experiments in the in-line system focused on determining the effect of web transport speed on the $Cu(InGa)Se_2$ film quality both in terms of the materials characteristics and device performance for 2 web transport speeds. The web used as substrate was 50 μm thick UpilexS polyimide coated with 0.2 μm Mo(O). The baseline web speed has been 0.75"/min, corresponding to an apparent deposition time of 15.2 min for the deposition zone of 11.4".

As a first experiment, a deposition was started at a web speed of 0.75"/min and after 4' of deposition the web speed was raised to 1"/min for another 5' of deposition. Samples taken at 2' and 7' from the leading edge, corresponding to web speeds of 0.75 and 1"/min were investigated. Table XI gives the compositions of the $Cu(InGa)Se_2$ films so sampled. Figure 11 shows the surface topography and cross section of the films taken from the same locations above. The data shows that the compositions are similar to within the measurement accuracy as expected. The thickness, on the other hand, shows a variation of 33% for the web speed changes of 32% which is also what one would expect.

Table XI. Composition of the $Cu(InGa)Se_2$ films deposited at 0.75"/min and at 1"/min web speed.

Web Speed (inch/min)	Cu (at%)	Ga (at%)	In (at%)	Se (at%)	Cu/III	Ga/III
0.75	22.6	7.6	19.1	50.7	0.84	0.28
1.00	22.5	8.8	18.6	50.1	0.82	0.32

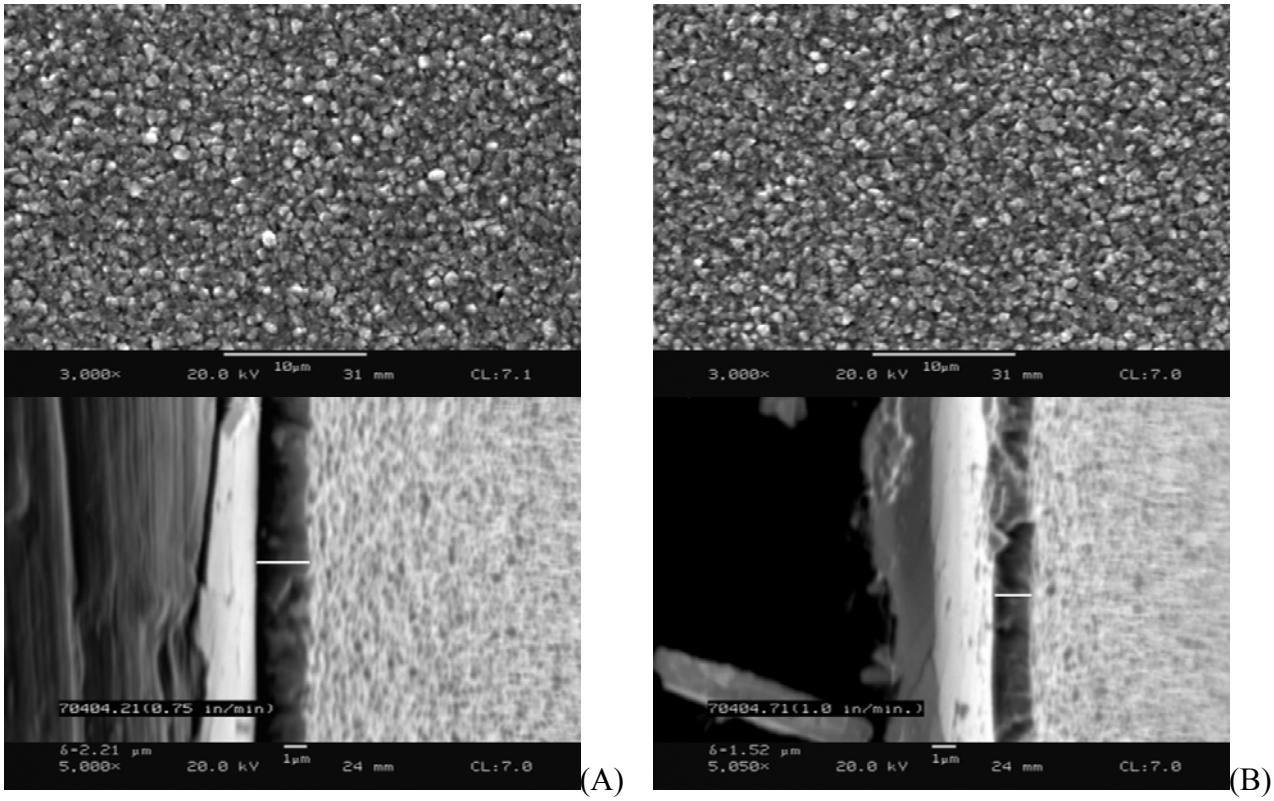


Figure 11. Surface topography and cross-section of the $Cu(InGa)Se_2$ films deposited at a web speed of 0.75"/min (A) and 1"/min (B).

The operational quality of the $Cu(InGa)Se_2$ films from these two locations were evaluated by fabricating devices and comparing their performances. Figures 12 and 13 show the JV data on these devices. The data gives a better performance for $Cu(InGa)Se_2$ films grown at 1"/min web speed than the films grown at 0.75"/min. In view of the compositional and structural similarities this difference at the present time could not be explained.

70404.21d **Upilex/Mo/CuInGaSe2/CdS/ZnO/ITO/Ni-Al grids**

100 mW/cm2 oriel *Initial test.*

Area: 0.56 *16:09 26-Feb-2007* *Settings: Ron*

Cell	Voc	Jsc	FF	Eff	Roc	Gsc	Vmp	Jmp	Temp	Filename	
001	**0.546**	**25.7**	**28.7**	**4.0**	**11.1**	**25.5**	**0.278**	**14.5**	**24.6**	**070226_160903**	**70404.21d-001.jvtst**
001	0.539	28.3	36.9	5.6	9.8	12.5	0.298	18.9	24.9		
002	**0.529**	**26.5**	**31.7**	**4.5**	**8.9**	**21.1**	**0.278**	**16.0**	**24.7**	**070226_161217**	**70404.21d-002.jvtst**
002	0.526	28.6	38.3	5.8	9.1	12.6	0.299	19.3	24.8		
003	**0.537**	**26.0**	**30.4**	**4.3**	**10.9**	**23.3**	**0.274**	**15.5**	**24.7**	**070226_161538**	**70404.21d-003.jvtst**
003	0.534	28.6	38.2	5.8	9.2	10.4	0.301	19.4	24.9		
004	**0.516**	**26.9**	**32.1**	**4.5**	**10.6**	**22.5**	**0.277**	**16.1**	**24.5**	**070226_161859**	**70404.21d-004.jvtst**
004	0.518	29.0	38.0	5.7	8.7	14.5	0.295	19.3	24.7		
average	*0.531*	*27.4*	*34.3*	*5.0*	*9.8*	*17.8*	*0.287*	*17.4*	*24.7*		
stdev	*0.01*	*1.215*	*3.71*	*0.727*	*0.89*	*5.5*	*0.011*	*1.89*	*0.13*		

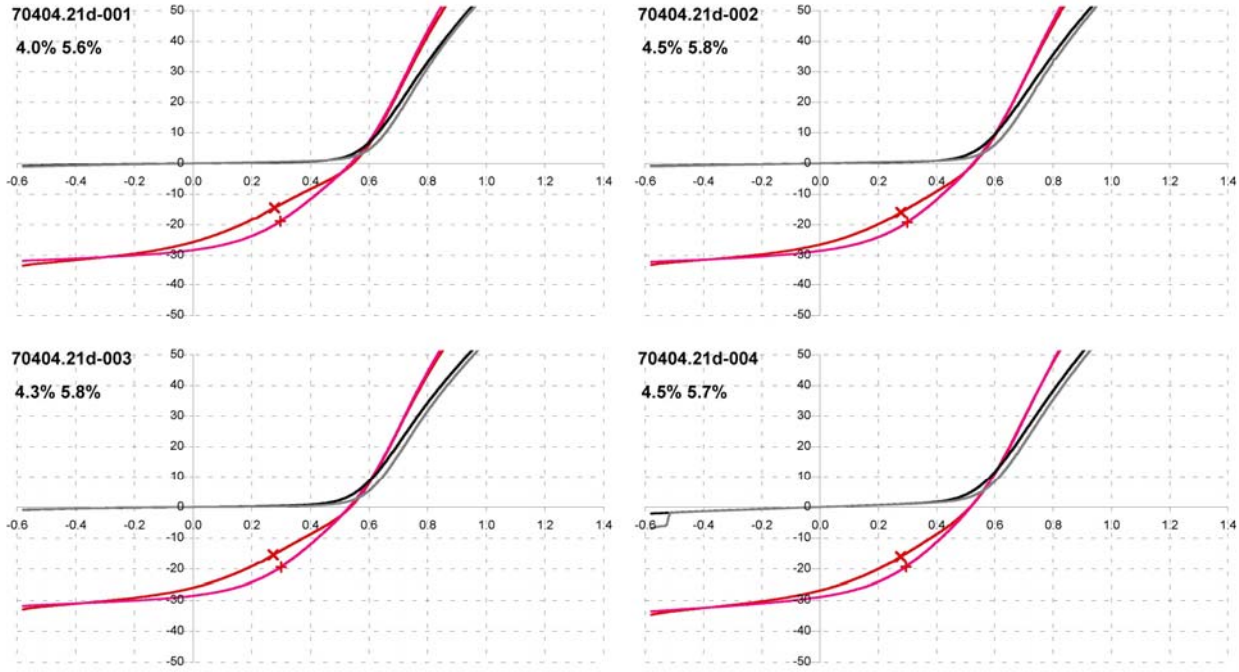


Figure 12. JV characteristics of devices fabricated on Cu(InGa)Se_2 film grown at a web speed of 0.75"/min.

70404.71d **Upilex/Mo/CuInGaSe2/CdS/ZnO/ITO/Ni-Al grids**

100 mW/cm2 oriel *Initial test.*

Area: 0.56 *15:00 27-Feb-2007* *Settings: Ron*

Cell	Voc	Jsc	FF	Eff	Roc	Gsc	Vmp	Jmp	Temp	Filename	
001	**0.532**	**31.8**	**51.9**	**8.8**	**5.5**	**2.5**	**0.348**	**25.3**	**25.2**	**070227_150000**	**70404.71d-001.jvtst**
001	0.533	31.7	52.8	8.9	5.3	2.7	0.350	25.4	25.5		
002	**0.529**	**30.3**	**55.3**	**8.9**	**4.7**	**2.5**	**0.364**	**24.3**	**24.9**	**070227_151453**	**70404.71d-002.jvtst**
002	0.530	30.3	55.3	8.9	4.6	2.7	0.362	24.5	25.6		
003	**0.530**	**31.1**	**51.7**	**8.5**	**5.5**	**3.6**	**0.348**	**24.5**	**25.1**	**070227_151807**	**70404.71d-003.jvtst**
003	0.530	31.2	51.9	8.6	5.4	3.7	0.347	24.7	25.4		
004	**0.532**	**32.3**	**53.8**	**9.2**	**4.4**	**3.2**	**0.363**	**25.4**	**25.3**	**070227_152234**	**70404.71d-004.jvtst**
004	0.532	32.4	54.3	9.4	4.4	4.6	0.360	26.0	25.7		
average	*0.531*	*31.4*	*53.4*	*8.9*	*5.0*	*3.2*	*0.355*	*25.0*	*25.3*		
stdev	*0.001*	*0.766*	*1.41*	*0.272*	*0.45*	*0.7*	*0.0072*	*0.57*	*0.25*		

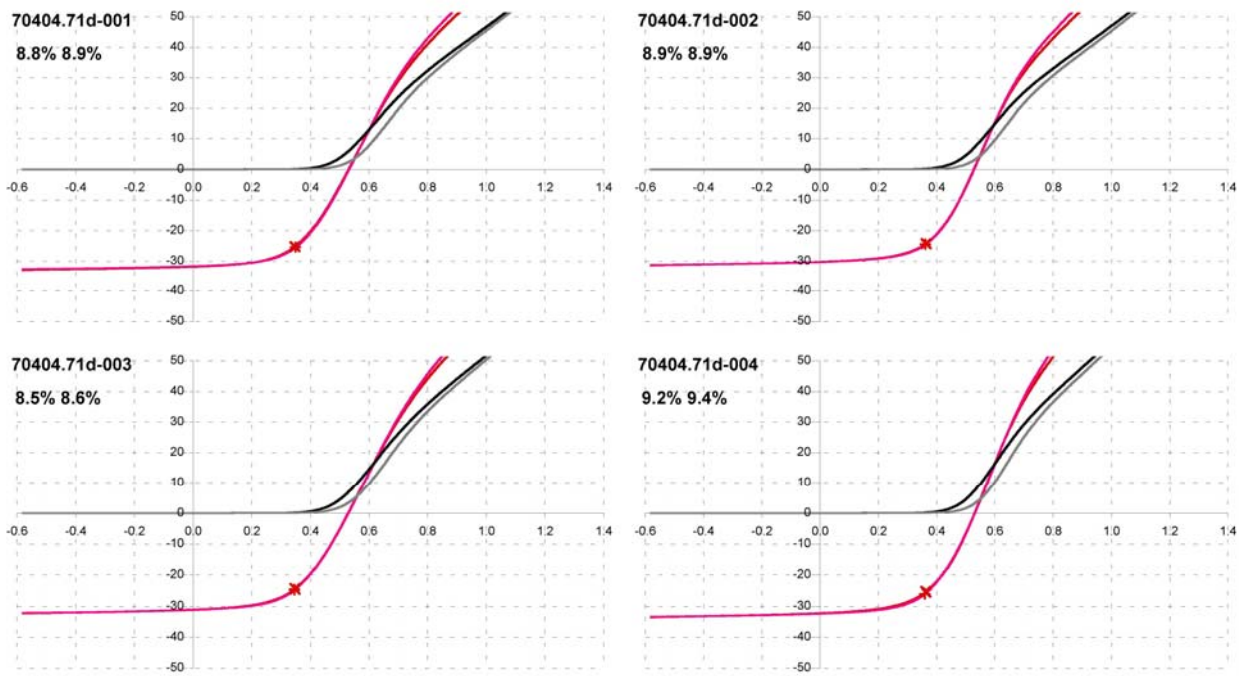


Figure 13. JV characteristics of devices fabricated on Cu(InGa)Se_2 film grown at a web speed of 1"/min.

At the conclusion of these early studies, the in-line system showed a major leak. The leak was traced to the ferrofluidic rotary feedthrough driving the pick-up roll. Delivery time of a new feedthrough was quoted to be 4 to 6 weeks. Order was placed for two new feedthroughs. Because of such a long down time it was decided to perform a long overdue overhaul of the system.

Following system upgrades were performed while waiting the delivery of the feedthroughs:

- Fabrication, installation and testing of new substrate heating assembly.
- Putting in service a back-up computer system to operate the reactor in case the main computer malfunctions.

- Upgrade In source to the design being used in the Cu and Ga sources.
- Replace all the control thermocouples in the sources. The new thermocouples are HfO_2 insulated rather than BeO since the latter type is not being manufactured anymore due to the health considerations. Because of the new type of insulator the temperature offset on the thermocouples has to be determined again.
- Diffusion and mechanical pumps were serviced.

When the feedthroughs were received it was decided to have them water cooled to increase operational lifetime. They are installed on the reactor with water cooling lines. Leak checking of the system found other leaks that were repaired. The system was finally brought to full operational status after going through rigorous testing and calibration.

About the same time, it was also decided to install a substrate carrier in the system and operate the system as an in-line deposition system rather than roll-to-roll system. The purpose of the carrier was to allow in-line deposition on both glass and polyimide substrates simultaneously. Furthermore, using 4" to 6" of polyimide coupon in each run is more cost effective than using 5' to 6' of material in each experiment. The carrier was tested with soda lime (SL) glass substrate at a temperature of 550°C and with polyimide substrate at a temperature of 450°C keeping the source temperatures constant and at a translational speed of 1"/min. Table XII, below, gives the device efficiencies and the deposition parameters for the two substrates. On SL glass substrate Cu/(Ga+In) and

Table XII. Deposition parameters and device performance of $Cu(InGa)Se_2$ deposited on SL glass and polyimide substrate using the substrate carrier.

Run Number	Substr. Material	Speed (in./min.)	CIGS Thick. (□m)	Eff %	Subs. T (°C)	Cu T (°C)	Ga T (°C)	In T (°C)	Se T (°C)
70455.1	SL glass	1.0	2.06	15.8	550	1364	1133	1053	350
70471.2	Upilex	1.0	1.54	9.1	450	1374	1133	1033	350

Ga/(Ga+In) were measured to be 0.9 and 0.3, respectively. These ratios on the polyimide substrate were found to be 0.95 and 0.35, respectively. V_{OC}, J_{SC}, and FF of the devices were 0.619V, 34.5 mA/cm^2, and 74.1% on SL glass while they were 0.575V, 28.4 mA/cm^2, and 55.8% on polyimide. Surface structure of the $Cu(InGa)Se_2$ films are shown in Figure 14.

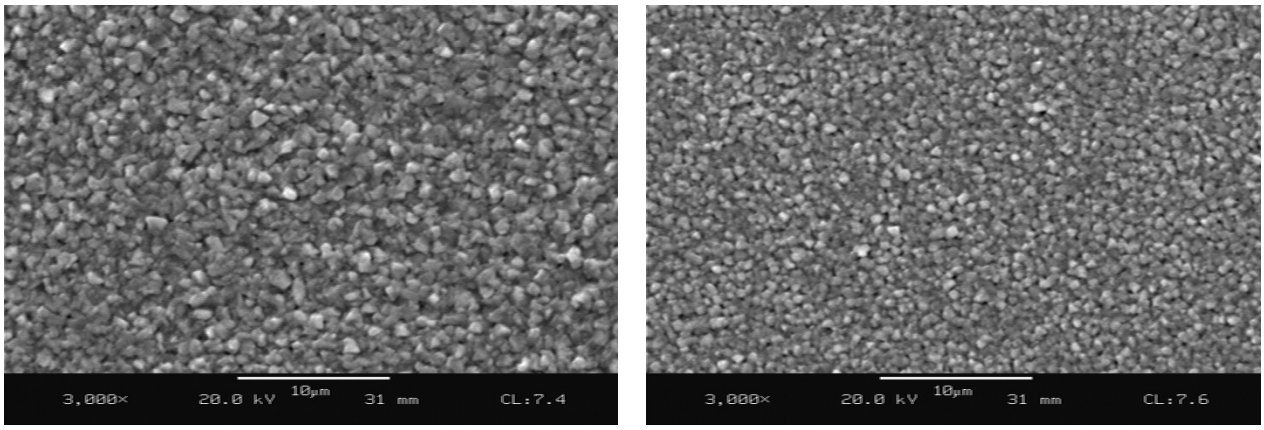


Figure 14. Surface structure of the $Cu(InGa)Se_2$ films deposited on SL glass at 550°C (left) and on Upilex at 450°C (right). Note the better developed grain structure at high temperature on SL glass.

In the next series of experiments $Cu(InGa)Se_2$ films were deposited simultaneously on both SL glass and UpilexS substrates. Substrate translation speed was varied from 1”/min to 2”/min. Substrate temperature was kept constant at 450°C. Source temperatures were also kept constant at values given in Table XI. $Cu(InGa)Se_2$ films were characterized compositionally by EDS, structurally by SEM. Solar cells were also fabricated on the materials. Table XIII, below summarizes the materials characteristics and device performance of the films.

Table XIII. Summary of the materials and device characteristics of $Cu(InGa)Se_2$ films deposited at different speed.

Run Number	Substr.	Speed ("/min.)	Subs. T (°C)	Thick. (□m)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Eff (%)	Cu/ Ga+In	Ga/ Ga+In
70471.1	glass	1.0	450	1.7	0.540	26.6	50.3	7.2	0.97	0.36
70471.2	upilex	1.0	450	1.5	0.575	28.4	55.8	9.1		
70475.1	glass	1.25	450	1.6	0.483	29.3	30.2	4.3	0.84	0.39
70475.3	upilex	1.25	450	1.4	0.535	26.8	59.8	8.6	0.85	0.40
70476.2	glass	1.5	450	1.2	0.529	21.9	55.2	6.4	0.80	0.44
70476.3	upilex	1.5	450	1.0	0.534	25.4	29.3	4.0	0.79	0.42
70477.1	glass	2.0	450	0.8	0.532	19.8	59.6	6.3	0.77	0.44
70477.3	upilex	2.0	450	0.9	0.552	17.9	21.5	2.1	0.76	0.43

As can be seen, the film thickness decreases, as expected, proportionally to the speed. As far as device performance is concerned there is no clear trend mainly because there is a measurable decrease in the Cu/Ga+In in the two highest speed runs. Films in these two runs are thin enough that EDS spectrum includes signal from the Mo substrate. However, since the compositional data is normalized it should still give the correct information. It

should be concluded that during the last two runs the source effusions had drifted relative to the previous runs and such conclusion on the device performance would be rather weak.

Surface structures of the films are shown in Figure 15. There is no dramatic difference between the two substrates at a given translational speed. However, there is gradual decrease of the grain size with speed most probably associated with decreasing thickness.

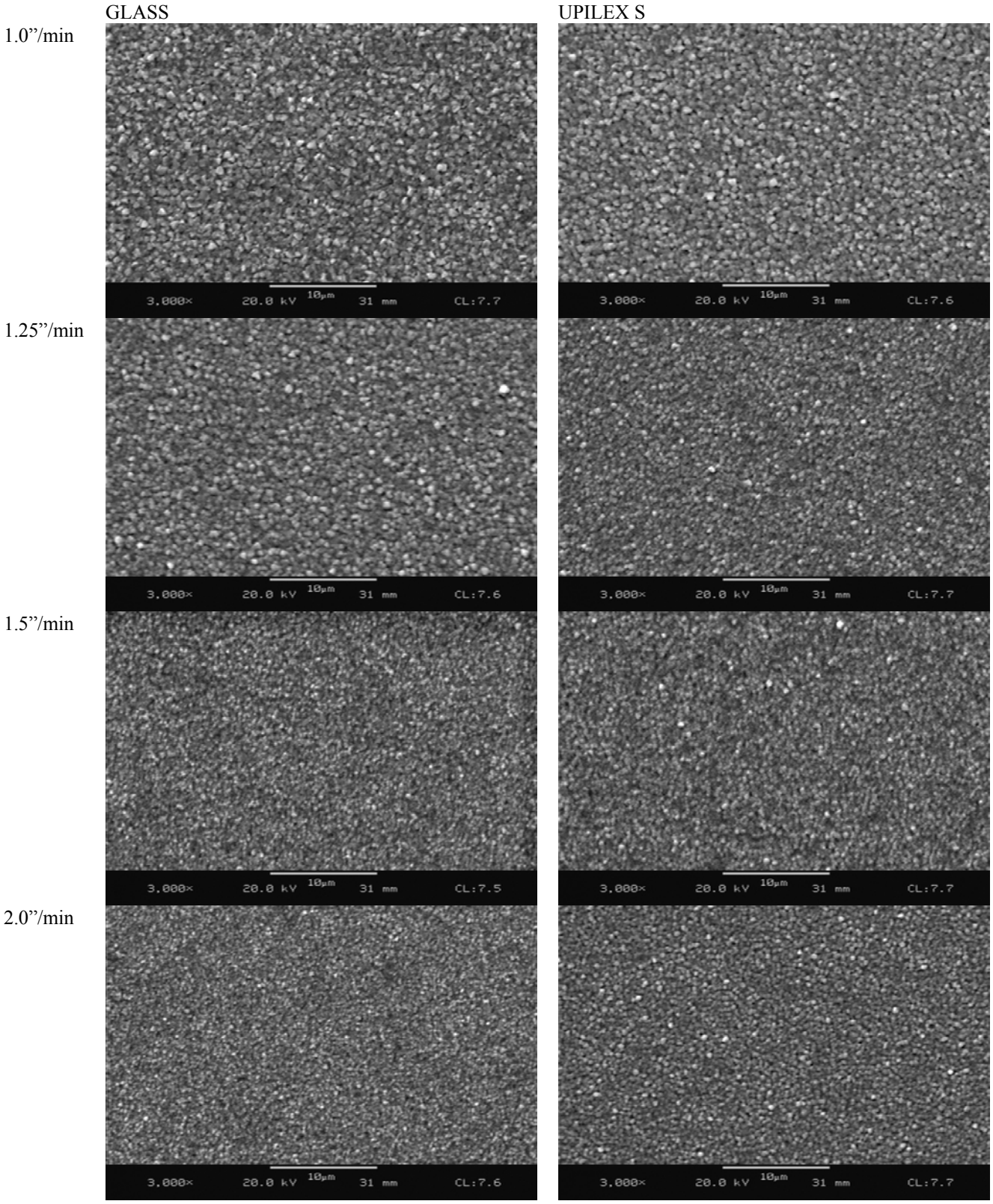


Figure 15. Surface structure of the $Cu(InGa)Se_2$ films deposited at different speed on glass and on UpilexS substrates.

3.1.2 Development of Sodium Source

The other direction the effort was pursued was in the development of Na source to be incorporated into the in-line system. To that effect, an evaporation source identical to those used in the in-line system was installed in a bell-jar type vacuum system. The evaporative characteristics of the source has been evaluated utilizing NaF as the source material. In parallel with that a new evaporation source, to be used for Na, has been installed in the in-line system. The source has been wired to its power supply and the computer program, operating the in-line system, has been modified to include this new source.

The NaF depositions were conducted in the test bell-jar system at a base pressure under 10^{-6} torr. The source, as previously stated, was a standard 2-nozzle effusion boat used in IEC in-line evaporation work. The source was charged with Alfa Aesar #12964 NaF (99.995% purity). Soda-lime glass strips (1" x 12") were used as substrates and were mounted 6 inches above the source. A shutter was used to shield the substrate from deposition during source heat-up and cool-down, and a QCM was mounted adjacent to the substrate to ensure that a stable deposition rate had been achieved before opening the shutter.

The glass strip substrates were masked lengthwise with Kapton tape so that peeling of the tape would leave an NaF edge measurable by profilometry. After evacuating the bell jar to under 10^{-6} torr, the NaF source was heated to the desired temperature (between 750ºC and 900ºC). After a stable deposition rate was achieved, the shutter was opened to perform the deposition.

Thickness was measured in 2 cm intervals over a 20 cm range in order to observe the deposition profile. The thickness was generally uniform over a 15 cm width centered above the source, with the thickness dropping off at the edges. The thickness of each sample was averaged and divided by the deposition time to generate a correlation between source temperature and deposition rate. The deposition rate data were regressed to the published vapor pressure model according to:

$$r_{dep}(T) = CP_{NaF}^{sat}(T)$$

where $r_{dep}(T)$ is the measured deposition rate in Å/sec, $P_{NaF}^{sat}(T)$ is the literature vapor pressure in Pa, and $C = 7.01 \times 10^{-5} \frac{\text{Å}}{\text{Pa} \cdot \text{sec}}$. The experimental data and regressed model are shown in Figure 16. The observed data show that the deposition rate is proportional to the published vapor pressure data, and indicate good predictability of the source behavior.

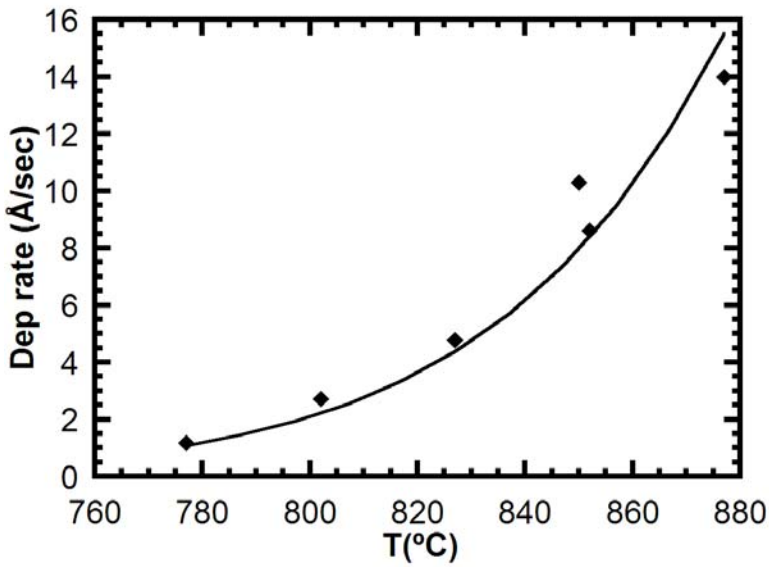


Figure 16. NaF deposition rate and correlation to published vapor pressure data.

3.2 Improved Performance with Absorber Thickness < 1 µm

The overall objective of this task is to develop methods to increase J_{SC} in devices using absorber layers with thickness d ≤ 1.0 µm. $Cu(InGa)Se_2$ cells have been demonstrated with no significant loss in V_{OC} and FF using absorber layers ≤ 0.7 µm and low J_{SC} has been identified as the primary loss and [5,6,7]. In this report we have investigated: (1) additional characterization of $Cu(InGa)Se_2$ films deposited with different thicknesses, (2) the behavior of devices with thin $Cu(InGa)S_2$ which has a higher absorption coefficient than $Cu(InGa)Se_2$, and (3) preliminary results on the implementation of light scattering in $Cu(InGa)Se_2$ devices.

Characterization of Submicron $Cu(InGa)Se_2$ Films

The effect of thickness (d) on morphology has been characterized for $Cu(InGa)Se_2$ films evaporated for different times using a single-layer uniform flux process. Parameters for 6 runs with different times are listed in Table XIV. This includes the thickness measured by the mass increase of the substrate which is decreases linearly with deposition time. Evaporation source temperatures were the same for all the runs so they should have the same compositions. The compositions measured by EDS show a decrease in [Cu]/[In+Ga] but this may be an artifact of the measurement as the d becomes less than the penetration depth of the electrons.

AFM images with decreasing thickness are shown in Figure 17 for four of the films. This shows a change in morphology and decrease in grain size and the grain size with submicron thicknesses is significantly reduced. The relationship between grain size and current generation or collection is not yet established.[8]

Table XIV. $Cu(InGa)Se_2$ films deposited for different times and rms roughness determined form AFM measurements.

Run #	Dep. time (min)	d (µm)	[Cu]/[In+Ga]	[Ga]/[In+Ga]	R_{ms} (nm)
34144	90	3.5	0.97	0.29	38
34143	60	2.2	0.95	0.32	45
34145	30	1.1	0.90	0.31	29
34148	20	0.76	0.89	0.31	28
34153	15	0.50	0.92	0.31	29
34149	10	0.35	0.85	0.31	16

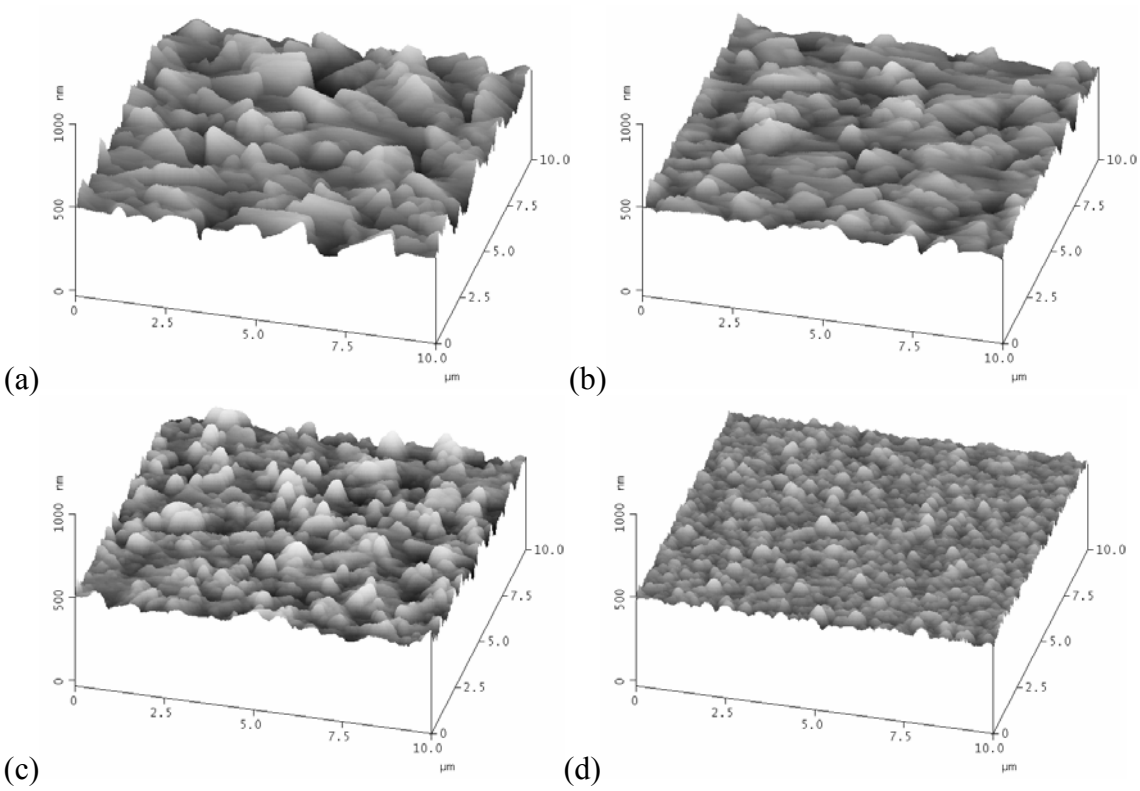


Figure 17. AFM images of films with thickness (a) 2.2 µm, (b) 1.1 µm, (c) 0.5 µm, and (d) 0.35 µm. Each image shows a 10 x 10 µm area.

Solar cells were fabricated using $Cu(InGa)Se_2$ from the runs listed in Table XIV and the J-V results are summarized in Table XV. In each case, the cells were processed using baseline IEC processes to give a structure of soda lime glass / Mo / $Cu(InGa)Se_2$ / CdS / ZnO / ITO / (Ni-Al grid) and no AR layer. On each piece 6 cells with nominal area 0.47 cm^2 were delineated and Table XV includes both the best cell and average for each piece.

The general trends for device parameters versus thickness are consistent with previous results[5,6], even though the J-V parameters are not completely monotonic. Of particular note is the device with d = 0.35 µm which has V_{OC} > 0.6 V and FF > 70%. The primary loss is J_{SC} which decreases monotonically for d ≤ 1.1 µm. An increase in $G_{SC} \equiv dJ/dV(V=0)$ indicates an increase in shunt conductance with decreasing thickness. In addition to comparison to the microstructure described above, these cells are being used for additional device characterization including detailed analysis of quantum efficiency to help understand the current losses.

Table XV. Device results (best and average of 6 cells per piece) using $Cu(InGa)Se_2$ with different deposition times and thicknesses.

Sample #	d (µm)	cells	Eff (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	Gsc (mS/cm^2)
34144.23	3.5	best	13.7	0.622	30.9	71.1	2
		avg.	13.3	0.621	30.1	71.0	1
34143.23	2.2	best	15.8	0.670	31.1	75.6	1
		avg.	15.5	0.670	30.7	75.3	0
34145.32	1.1	best	12.7	0.645	27.1	72.8	2
		avg.	11.4	0.633	25.8	69.6	2
34148.23	0.76	best	10.1	0.624	24.0	67.7	3
		avg.	10.0	0.622	23.6	68.1	3
34153.23	0.50	best	7.3	0.560	22.0	59.5	5
		avg.	6.5	0.557	21.6	53.9	5
34149.23	0.35	best	7.9	0.605	18.6	70.1	3
		avg.	7.2	0.590	18.9	65.1	3

3.3 Thin $CuInS_2$ Devices

Models of device behavior with thin $Cu(InGa)Se_2$ indicate that the drop in J_{SC} cannot be explained simply by incomplete optical absorption and low optical reflection at the Mo/$Cu(InGa)Se_2$ back contact.[7] Experiments were done to determine if the higher absorption coefficient in $CuInS_2$ or S-containing alloys[9] can be used to increase J_{SC} with thin absorbers and to determine the extent to which unexplained losses in J_{SC} with absorber layers < 1 µm thick are due to the generation depth as opposed to losses at interfaces or from scattering. Using the absorption coefficients measured by spectroscopic ellipsometer for evaporated $Cu(InGa)Se_2$ and $CuInS_2$ films, the relative loss in current due to incomplete absorption as a function of thickness was calculated and is shown in Figure 18. With d = 0.4 µm, 96 % of the incident light (above the E_g = 1.5 eV) is absorbed in a $CuInS_2$ films while only 91% is absorbed in a $Cu(InGa)Se_2$ with E_g = 1.3 eV.

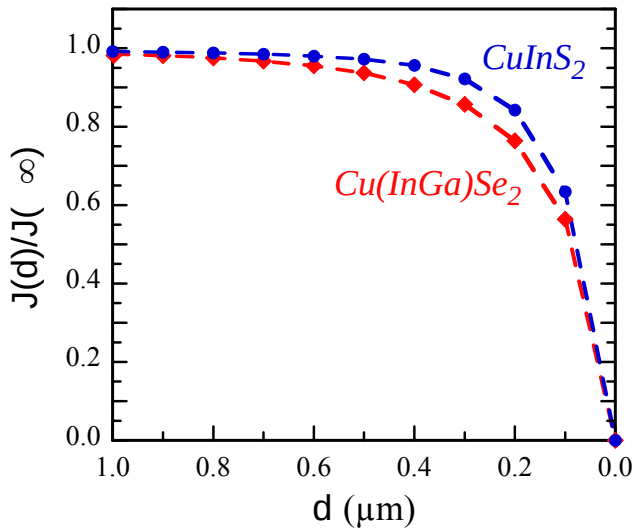


Figure 18. Relative loss in current due to incomplete optical absorption in $CuInS_2$ and $Cu(InGa)Se_2$ films.

$CuInS_2$ films were deposited by uniform co-evaporation under Cu-excess conditions with thicknesses 1.9, 0.9, and 0.5 µm. Figure 19 shows SEM images of the as-deposited films which shows the grain size decreases with changes with the film thickness similar to thin $Cu(InGa)Se_2$ films.

The films were etched in a 0.5 M KCN aqueous solution to remove Cu_xS_y prior to the CdS layer deposition and solar cells with soda lime glass / Mo / $Cu(InGa)Se_2$ / CdS / ZnO / ITO / (Ni-Al grid) structure were fabricated. The J-V parameters of the cells are listed in Table III and QE curves shown in Figure 20. Figures 20(a) and 20(b) show external QE and normalized internal QE, respectively. For comparison, the calculated spectral response from absorption coefficient for each thickness absorber is shown in Figure 20(c). Compared with the calculated QE curves, the decrease in QE in the range 600 – 800 nm with thickness is greater than expected. This decrease may be caused by the decreasing grain size with film thickness.

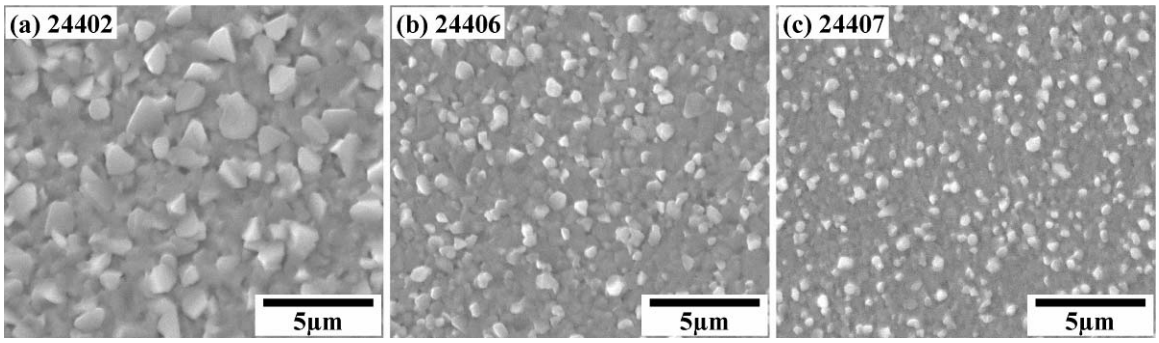


Figure 19. Microstructure change with film thickness.

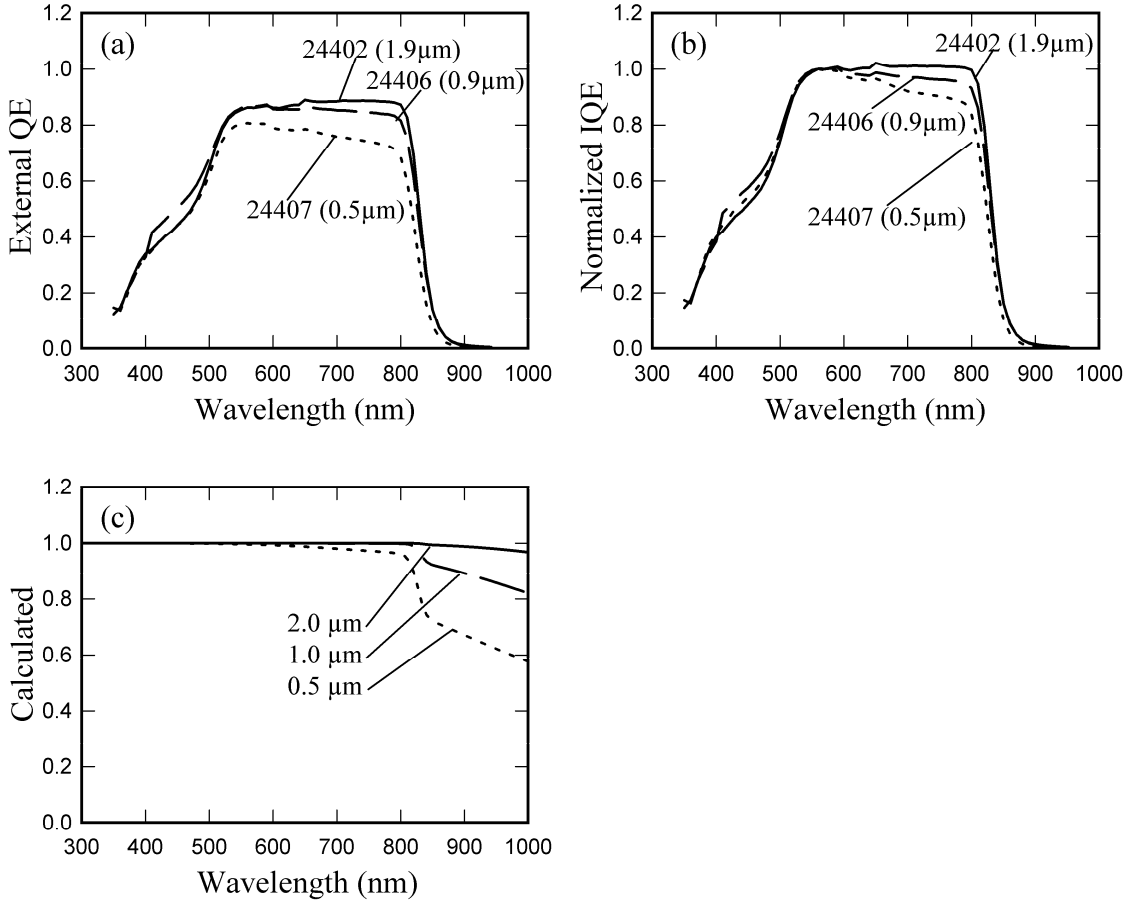


Figure 20. Spectral response depending on the absorber thickness. (a) external QE, (b) normalized internal QE, and (c) calculated from absorption coefficient of $CuInS_2$.

Table XVI. Solar cell properties with thin $CuInS_2$ absorber layers.

Sample	thickness (μm)	Eff. (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)
24402	1.9	8.22	0.619	22.07	60.0
24406	0.9	7.41	0.608	20.81	58.4
24407	0.5	5.39	0.553	19.79	49.1

3.4 Textured TCOs for Light Scattering

Preliminary experiments were done to investigate the implementation of light scattering to improve J_{SC} in devices with submicron $Cu(InGa)Se_2$. Our approach for light scattering was to texture the TCO layer using a post-deposition etch of sputtered ZnO films as has been implemented for a-Si devices.[10] For $Cu(InGa)Se_2$ solar cells, TCO deposition or post-deposition treatment should be performed at temperatures no higher than 200°C to maintain the integrity of the underlying junction. In this report we show

that ITO films can be textured using an HCl etch and report efforts to implement this into processing of $Cu(InGa)Se_2$ cells.

ITO films were deposited on glass substrates using rf sputtering with thickness ~ 500 nm and sheet resistance 10 - 12 Ω/sq. This is triple the thickness used for baseline device processing at IEC. Films were etched in dilute HCl and etch conditions were varied with concentrations from 5 – 50%, temperatures from 25 – 60°C, and times up to 120 s. Films were characterized by sheet resistance (R_{sh}), optical transmittance (T), and AFM to determine surface morphology. Optical scattering is determined by the haze factor defined by $T_{diffuse}$ / T_{total} which were measured using an integrating sphere attachment on the optical spectrophotometer and averaged over the wavelength range $600 \leq \lambda \leq 1000$ nm. AFM images are shown in Figure 21 for the as-deposited ITO and after etching in 10% HCl for 10 s at ~25°C. This etched film had R_{sh} =19 Ω/sq and haze = 9.7% compared to haze = 2.3 % in the as-deposited film. Similar values of R_{sh} and haze could be obtained with different concentrations and temperatures.

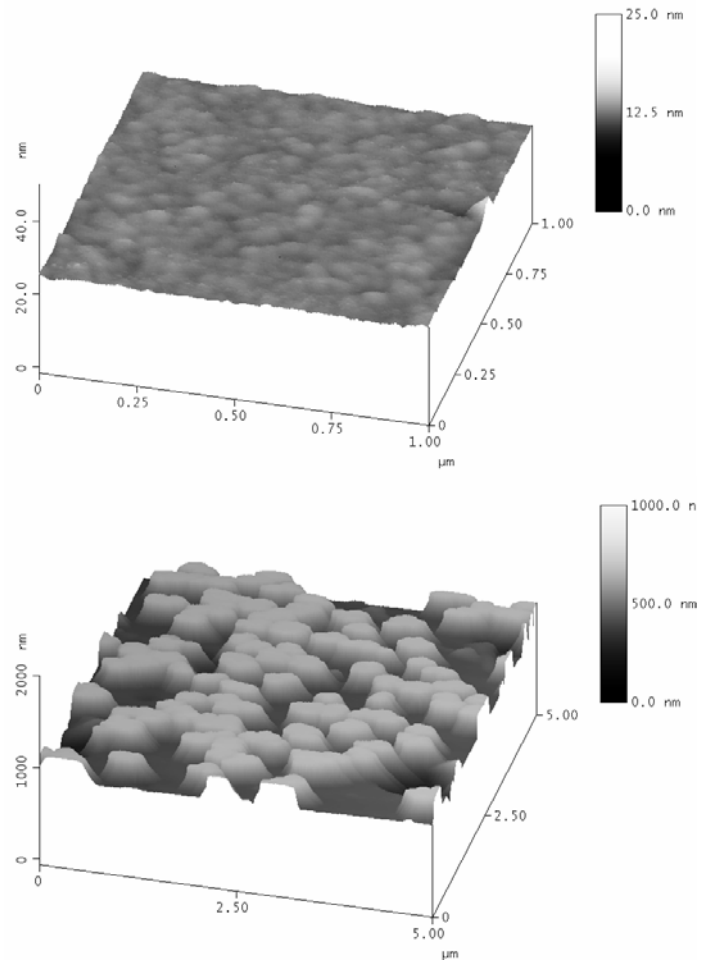


Figure 21. AFM images of (top) an as-deposited ITO film and (bottom) after etching in 10% HCl for 10 s at ~25°C.

Preliminary tests were done to determine if the etching could be successfully done on devices. For this the baseline glass / Mo / $Cu(InGa)Se_2$ / CdS / ZnO / ITO / grid device structure was used with the as-deposited ITO thickness increased to 500 nm. After ITO deposition the edges of the sample were masked using nail polish and then the samples were etched under different conditions. Then the nail polish was removed and grids were deposited. All devices were either shorted or had very low current as shown, for example, for the 6 devices on one sample in Figure 22. The cause of the low current has not yet been determined.

Experiments were also done with etching ZnO films. However, these were less successful than ITO in producing a significant increase in haze. The films used were deposited at room temperature and had poor crystallinity, unlike the films deposited in ref. 22 which were deposited at temperatures up to 300°C.

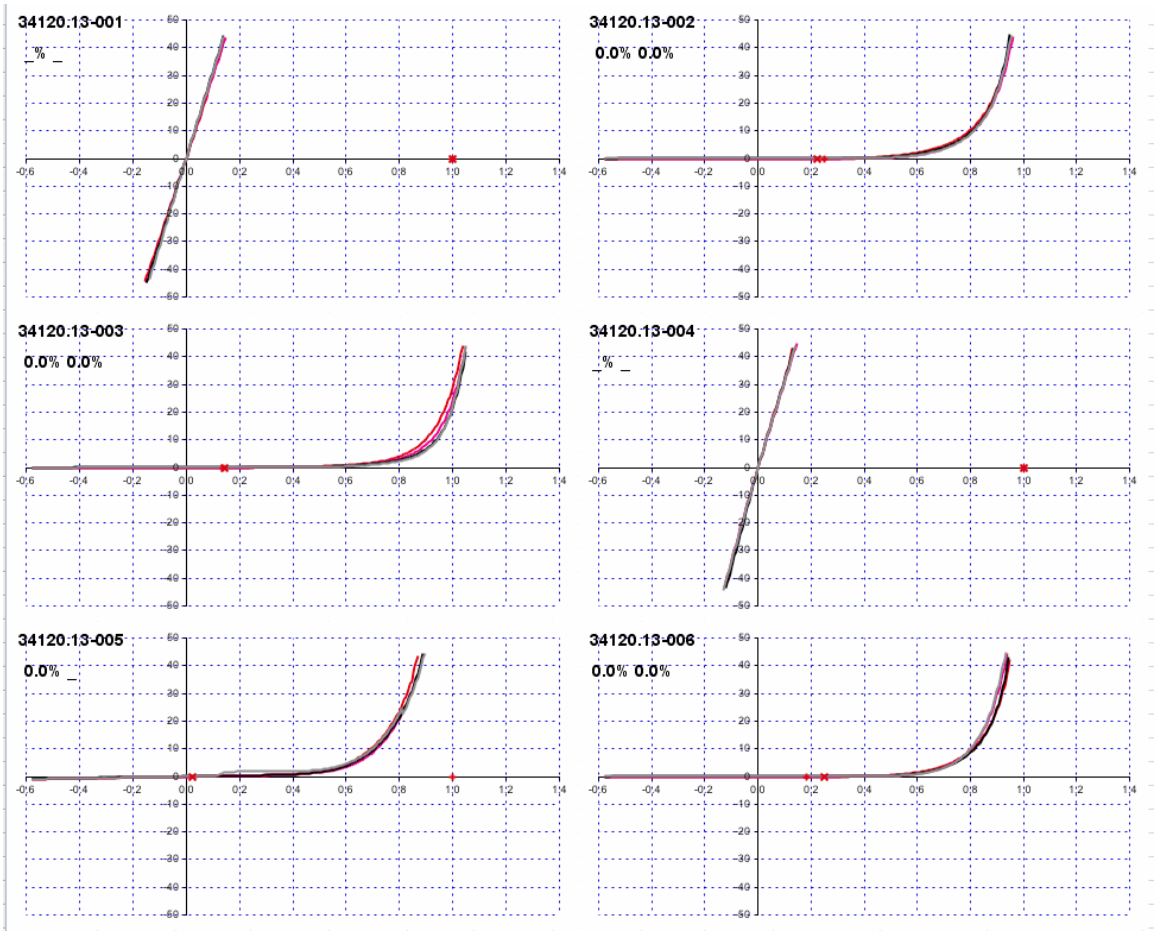


Figure 22. J-V curves for 6 $Cu(InGa)Se_2$ cells on a sample with etch-textured ITO.

3.5 Composition Control for Increased V_{OC}

Efforts on wide bandgap $Cu(InGa)(SeS)_2$ alloys for increased V_{OC} have focused on controlling the composition of films formed by elemental evaporation and by the reaction of Cu-Ga-In precursors. This control is necessary to enable the effects of different compositions and through-film compositional profiles on devices to be characterized.

Composition Control for $Cu(InGa)(SeS)_2$ Evaporation

Efforts on wide bandgap $Cu(InGa)(SeS)_2$ alloys for increased V_{OC} have focused on controlling the composition of evaporated films to enable the effects of different compositions and through-film compositional profiles on devices to be characterized. We have previously determined the effect of changes in [Cu]/[In+Ga] and [Ga]/[In+Ga] on the relative S incorporation at substrate temperature (T_{SS}) = 550°C. In this work, the dependence of the relative Se and S incorporation chalcogen in $Cu(InGa)(SeS)_2$ on the substrate temperature was characterized with various [S]/[Se+S] flux rate ratios at T_{SS} = 300°C, 450°C, and 550°C. All films were grown with excess chalcogen species in the flux with [S+Se]/[Cu+In+Ga]~10, and both flux rate ratios of [S]/[Cu+In+Ga] and [Se]/[Cu+In+Ga] were greater than unity throughout all experiments. The Ga content was adjusted to be [Ga]/[In+Ga]=0.55 ±0.05. For Cu-excess grown films, KCN (aq.) etching to remove $Cu_x(SeS)_y$ was performed before analyses, while as-grown films were used for the analyses of Cu-poor grown films.

Figure 23 shows the relation between the concentration ratios of Y≡[S]/[Se+S] in the flux and in the film. The distinct change in Y_{film} from Cu-poor grown (open symbol) to Cu-excess grown (close symbol) films has previously been reported.[11,12] The solid lines are drawn by fitting the data to:

$$[S]_{film}/[Se]_{film} = C\cdot[S]_{flux}/[Se]_{flux} \quad (1)$$

or

$$Y_{film}/(1-Y_{film}) = C\ Y_{flux}/(1-Y_{flux})$$

where C is a constant for given temperature, which is based on a reaction model proposed for Ga(AsP).[13] For Cu-poor grown films, the behavior of the preferred chalcogen incorporation is fit well by Eq. 1. reaction model. At T_{SS} = 450°C (△) or 550 °C (○), all data are on the line with C=0.32. At T_{SS} = 300°C (□), C=0.67 is found. On the other hand, for films grown with [Cu]/[In+Ga] > 1, the departure from the line with C = 4.2 is shown for the films grown at 300°C (■) with Y_{flux} > 0.3 although the others are on that line. This suggests that a difference in the reaction process determining the incorporation reaction of chalcogen between at 300°C and at higher temperatures.

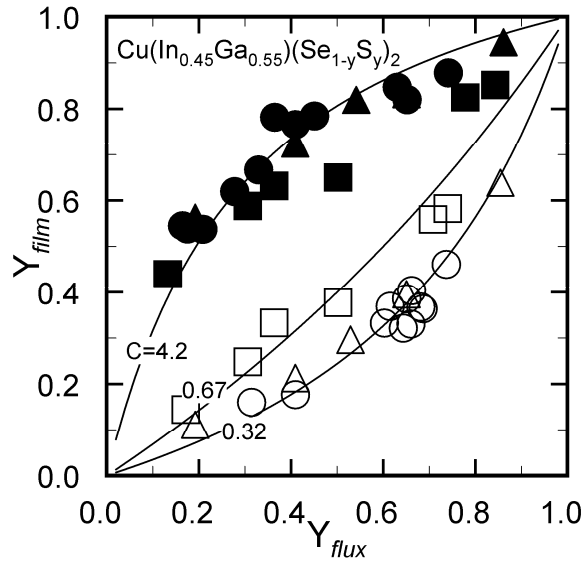


Figure 23. Relation between the [S]/[S+Se] ratios of the film composition (Y_{film}) and flux rate (Y_{flux}). The shape of symbol corresponds to the substrate temperature grown. Temperature: (■,□) 300°C, (▲,△) 450°C, (●,○) 550°. Open and closed symbols correspond to the Cu-poor and Cu-excess deposition condition, respectively.

We have previously characterized the relation of Y_{film} to Y_{flux} for different compositions and T_{SS} = 550°C and showed that Y_{film} varies with the relative [Ga]/[In+Ga] only for films with excess Cu. To understand this result and the data in Figure 11 it is necessary to consider the relative kinetic and thermodynamic effects on the reactions. To consider the thermodynamics of chalcogen incorporation in $Cu(InGa)(SeS)_2$ formation reaction the following equilibrium is considered:

$$S_2 + Cu(InGa)Se_2 \leftrightarrows Se_2 + Cu(InGa)S_2 \qquad (2)$$

The equilibrium constant K for this reaction is given by

$$K = [Se_2][Cu(InGa)S_2] / [S_2][Cu(InGa)Se_2], \qquad (3)$$

where the reaction constant K is understood using the Gibbs free energy difference ΔG as:

$$K = \exp(-\Delta G/kT) \qquad (4)$$

Furthermore, eq. 3 can be rewritten in the same form as eq. 1 as:

$$Y_{film}/(1-Y_{film}) = K\, Y_{flux}/(1-Y_{flux}). \qquad (5)$$

Unfortunately, complete free energy data covering the $Cu(InGa)(SeS)_2$ alloy system is not available. Nevertheless, tendencies from the literature [14,15,16,17] can be considered. Comparing the effect of the chalcogen species on the free energy of formation of its chalcopyrite, the sulfide tends to have lower energy than the selenide, while the energies of S_2 and Se_2 are similar. Furthermore, the Gibbs free energies of the Ga species are more negative than with In. Therefore, the tendency of the chalcogen incorporation

under Cu-excess grown condition is consistent with the thermodynamics of the $Cu(InGa)(SeS)_2$ system.

On the other hand, the lack of dependence on [Ga]/[In+Ga] and preference for Se relative to S in the Cu-poor films is inconsistent with the thermodynamics. Thus, the chalcogen incorporation in the Cu-poor case may be controlled mainly by kinetics. The difference between the Cu-excess and Cu-poor cases must be closely related to the formation of Cu-(SeS) phases during the reaction process.

In Table XVII, the performance of some $Cu(InGa)(SeS)_2$ solar cells fabricated during this work are listed using $Cu(InGa)(SeS)_2$ films with various compositions and bandgaps from 1.3 – 1.6 eV. All samples were prepared by uniform deposition at about 550°C of substrate temperature. Cells with ~1.5 eV have good reproducibility with efficiency over 11% demonstrated.

Table XVII. Recent results on solar cell performance using evaporated $Cu(InGa)(SeS)_2$.

Cell	Eff. (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	E_g (eV)
24428.22.6	11.0	0.848	17.8	0.732	1.57
24429.12.4	10.3	0.851	17.7	0.683	1.60
24430.12.6	11.1	0.844	18.2	0.722	1.58
24433.12.4	11.9	0.827	19.8	0.727	1.51
24434.22.4	11.4	0.849	19.3	0.695	1.53
24439.22.5	12.7	0.818	21.6	0.719	1.44
24440.32.4	14.5	0.776	24.3	0.767	1.37
24442.22.1	14.9	0.725	26.1	0.787	1.32

3.6 $Cu(InGa)(SeS)_2$ Formation by Cu-Ga-In Reaction in H_2Se/H_2S

The formation of $Cu(InGa)(SeS)_2$ absorber layers by the 2-step H_2Se/H_2S reaction of sputtered Cu-Ga-In precursor films has been previously demonstrated to yield homogenous Ga distribution and high device efficiency.[18,19] Recent work at IEC has indicated that the preferential reaction of Se with In and S with Ga plays a significant role in the 2-step reaction process.[20] At the end of the selenization (first) step, the film is primarily composed of $CuInSe_2$ and a Cu_9Ga_4 intermetallic, which then reacts with S and incorporates into the chalcopyrite phase during the second step.

A typical 2-step H_2Se/H_2S baseline process consists of a 15 minute reaction in 0.35% H_2Se/0.0035% O_2 at 450 ºC followed by either 15 or 30 minute reaction in 0.35% H_2S/0.0035% O_2 at 550 ºC. This process results in $Cu(InGa)(SeS)_2$ films with uniform Ga composition and high S concentration near the film surface. Devices fabricated on these absorber layers have achieved efficiencies in excess of 13%. $Cu_{0.8}Ga_{0.2}$/In precursor bi-layers are deposited onto 1" x 1" Mo/soda-lime glass substrates by sputter deposition from $Cu_{0.8}Ga_{0.2}$ alloy and elemental In targets, respectively. The thickness of

the soda-lime glass and Mo back contact are 2 mm and 0.7 μm, and the $Cu_{0.8}Ga_{0.2}$ and In film thicknesses are 3490 Å and 4890 Å, respectively. The chalcogen reactions are carried out in an externally-heated atmospheric-pressure quartz tube reactor used extensively in previous work.[21] After reaction temperature and gas concentration are established, the chalcogen reactions were commenced and terminated by sliding the samples between the heated reaction zone and an unheated portion of the quartz tube. Two 1" x 1" samples, positioned side-by-side in the reaction tube, were chalcogenized per run.

In addition to previously presented XRD, SEM, EDS, and Auger characterization of baseline IEC films, cross-sectional SEM images are shown in Figure 24 for $Cu(InGa)Se_2$ and $Cu(InGa)(SeS)_2$ films formed by precursor reaction. These images were provided by Bobby To at NREL. The $Cu(InGa)Se_2$ film, reacted at 450°C for 60 min to fully consume intermetallic phases, has small grains and periodic voids at the back of the film. The $Cu(InGa)(SeS)_2$ film reacted in H_2Se for 15 min at 450°C, then H_2S for 15 min at 550°C has much larger grains but still has the voids. The increase in grain size results from the reaction at higher temperature with H_2S but the relative importance of the thermal and chemical effects are not yet know. The voids are consistent with previous IEC observations of the backsides of delaminated $Cu(InGa)(SeS)_2$ films.

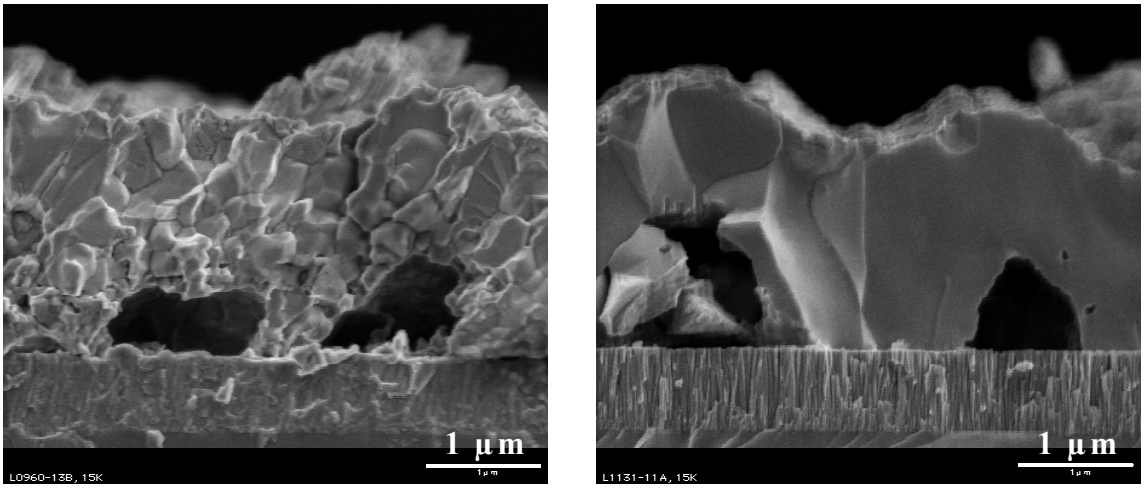


Figure 24. Cross-sectional SEM images of reacted $Cu(InGa)Se_2$ (left) and $Cu(InGa)(SeS)_2$ (right) films.

Experiments have been performed to determine the effect of sulfization temperature on the Ga distribution to gain further insight into the Ga incorporation into the chalcopyrite. Films were reacted by the 2-step H_2Se/H_2S process, with the selenization carried out at 450 ºC for 15 minutes and the sulfization carried out for 30 minutes at temperatures ranging from 450 ºC to 550 ºC. Films were characterized by EDS and XRD to measure the degree of Ga homogenization within the films. Two samples were reacted side-by-side per run, and are designated "upstream" or "downstream" to indicate their relative positions.

The results indicate an expected increase in the measured [Ga]/[In+Ga] ratio with increasing temperature, as shown in Figure 25. The XRD results, shown in Figure 26, however, indicate a discontinuity at approximately 500 ºC of the maximum-intensity d-spacing of the chalcopyrite (112). It should be noted, however, that the d-spacings presented in the figure are somewhat oversimplified, as a number of the XRD patterns, especially those taken of samples sulfized at temperatures below 500 ºC, possessed broadened peaks indicating some degree of composition grading. Nevertheless, the observation of an absence of d-spacings from 3.302 to 3.316 Å is a potentially significant result.

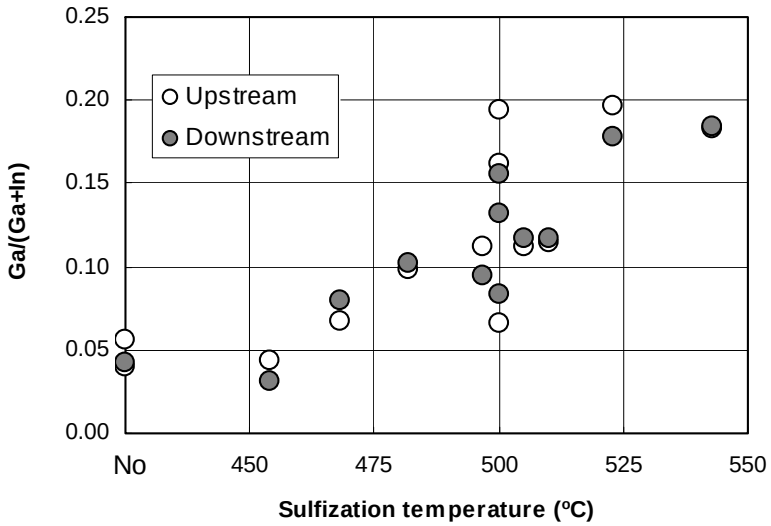


Figure 25. Ga/III ratio measured by EDS at the $Cu(InGa)(SeS)_2$. "No" on the abscissa indicates selenization only. "Upstream" and "Downstream" indicate sample position for a given run.

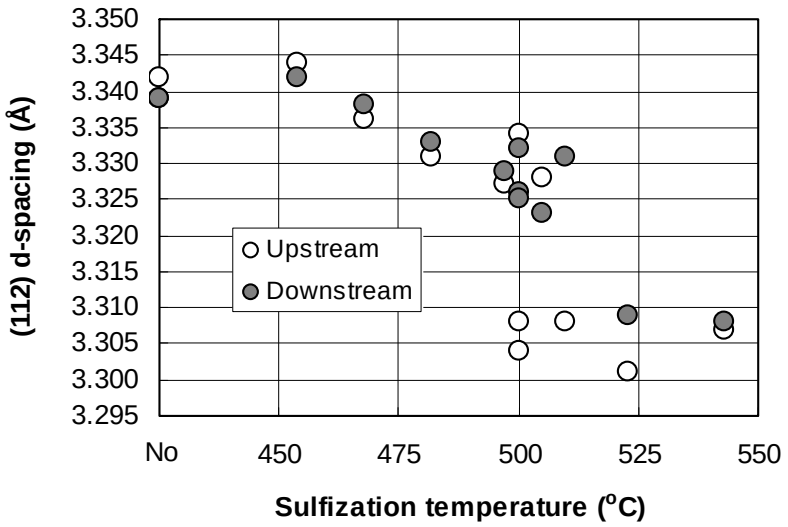


Figure 26. Cu(InGa)(SeS)2 (112) d-spacing for $Cu_{0.8}Ga_{0.2}$/In precursors selenized for 15 minutes at 450ºC then sulfized for 30 min at the indicated temperature. "No" on the abscissa indicates films processed by selenization only.

Figure 27 shows residual Cu_9Ga_4 intermetallics on the Mo back contact after delamination of a $Cu(InGa)(SeS)_2$ film that was selenized for 15 min at 450ºC in H_2Se, followed by a 15 minute sulfization at a temperature of 450ºC. The presence of the Cu_9Ga_4 intermetallics, verified by EDS and XRD measurement, was unexpected given the previous IEC result indicating the complete reaction of Ga from intermetallic precursors at a temperature of 450ºC in less than 10 minutes. The overlying chalcopyrite film is apparently acting as a diffusion barrier at these reduced temperatures, slowing the delivery of S to the Cu_9Ga_4 intermetallic.

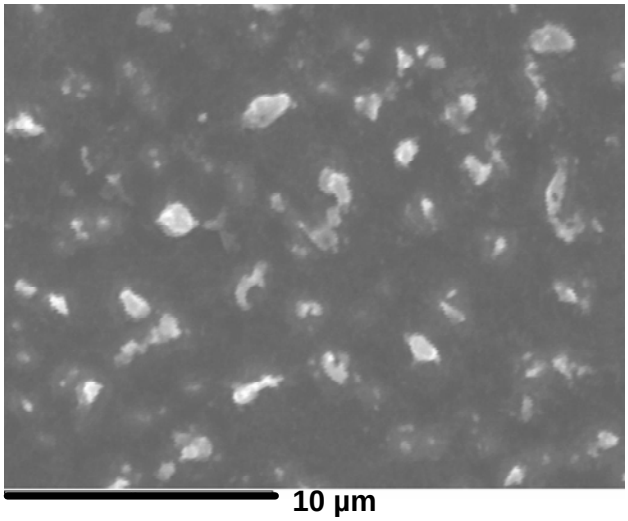


Figure 27. Residual Cu_9Ga_4 intermetallics on Mo back contact after delamination of $Cu(InGa)(SeS)_2$ formed by 15 min selenization at 450ºC followed by 15 minute sulfization at a temperature of 450ºC.

Not unexpectedly, given the observation of unreacted Cu_9Ga_4 intermetallics at the back contact after sulfization at 450ºC, XRD and EDS measurements indicated negligible Ga incorporation into the overlying $Cu(InGa)(SeS)_2$ film. The peak maximum of the $Cu(InGa)(SeS)_2$ (112) peak possessed a d-spacing of 3.334, whereas a "baseline" (550ºC sulfization temperature) $Cu(InGa)(SeS)_2$ film would possess a d-spacing of approximately 3.300 Å, and pure component $CuInSe_2$ possesses a d-spacing of 3.351 Å. The EDS data are shown in Table XVIII, and indicate composition ratios of Ga/(In+Ga) = 0.05,effectively below the detection limit, and $0.05 < S/(Se+S) < 0.10$. These ratios in a "baseline" $Cu(InGa)(SeS)_2$ film are Ga/(In+Ga) = 0.18 and $0.20 < S/(Se+S) < 0.30$.

Table XVIII. Average EDS composition measurements of two $Cu(InGa)(SeS)_2$ films formed by 15 min selenization at 450ºC followed by 30 min sulfization at 450ºC.

Element	Atomic %
Cu	24.5
In	24.6
Ga	1.1
Se	46.0
S	3.5

The Cu-Ga phase diagram, reproduced in Figure 28, indicates that at a temperature of 485ºC, the high-Ga boundary of the γ_1 phase (γ_1-Cu_9Ga_4) transitions from a solid-solid boundary with the γ_2 phase to a solidus. The 485ºC temperature at which this occurs is very close to the 500ºC at which the discontinuity in d-spacing is observed in the present

study. It is hypothesized that at temperatures above 485 – 500ºC, the γ_1 phase is be more prone to decompose into a Cu-rich solid and Ga-rich liquid phase that effects a step increase in Ga mobility and produces a higher degree of Ga homogenization. It should also be noted that 485ºC represents the maximum concentration of Ga in the γ_1 phase, and increases in temperature past this point produce a thermodynamic driving force for the expulsion of Ga from the γ_1 phase.

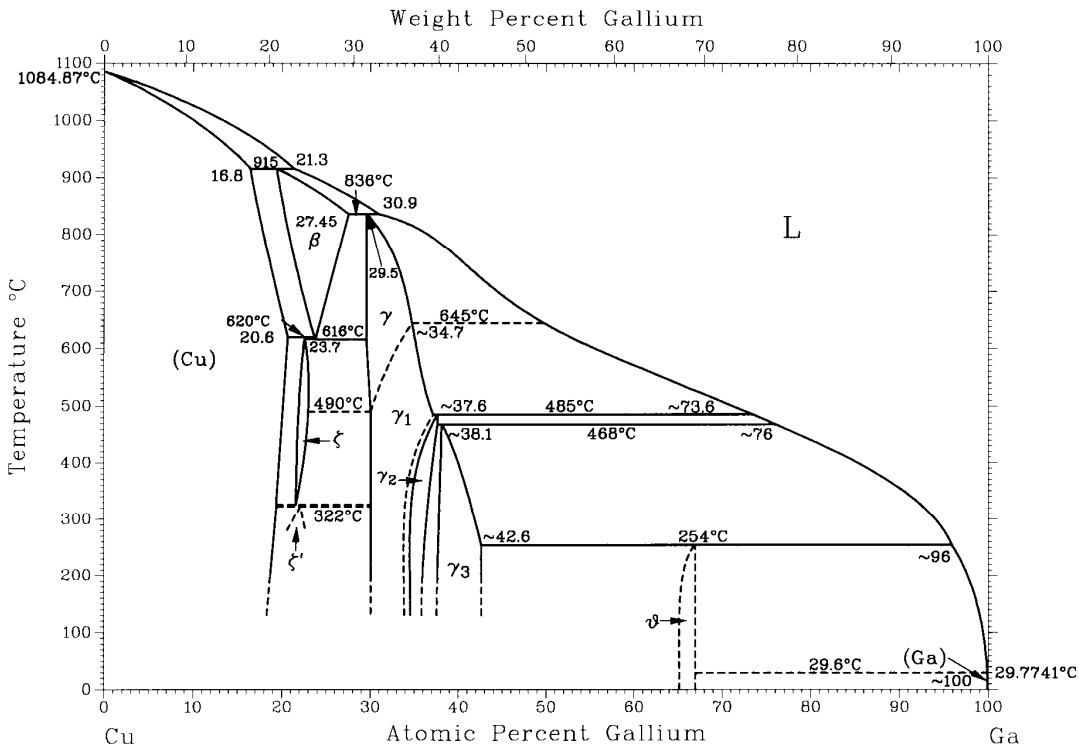


Figure 28. Cu-Ga phase diagram indicating transition of Ga-rich γ1 phase boundary from γ2 (solid) to a solidus line at 485ºC.

3.7 Cu(InGa)Se_2 Formation by H_2Se Reaction of partially-selenized precursors

In this task we are investigating the processes to increase V_{OC} in Cu(InGa)$(SeS)_2$ solar cells by controlling film growth and composition. Specifically methods are being developed to control the relative through-film Ga composition in the formation of Cu(InGa)$(SeS)_2$ films from the reaction of metal precursors by circumventing the formation of Cu-Ga-In intermetallic phases using mixed metal/metal-selenide precursors.

In this report, precursors containing copper selenide were prepared. Films with the CuSe phase were formed by electrochemical deposition onto Mo-coated soda-lime glass substrates. To obtain the $Cu_{2-x}Se$ phase, a 60 minute anneal at 300ºC under vacuum was conducted. Ga and In were e-beam evaporated onto the copper selenide films to yield Cu/(In+Ga) = 0.9 and Ga/(In+Ga) = 0.3 in the precursors. As a control, $Cu_{0.8}Ga_{0.2}$/In

precursors with a composition of Cu/(In+Ga) = 0.9 and Ga/(In+Ga) = 0.2 were prepared by sequential sputtering. In all films, thicknesses were chosen to give a final 2 μm thick $Cu(InGa)Se_2$ film. The precursors were selenized for 5, 15 or 90 min at 450ºC at atmospheric pressure in a quartz tube reactor using a 0.35at% H_2Se/0.0035at% O_2/Ar gas mixture.

The selenized films were characterized by scanning electron microscopy (SEM), energy dispersive x-ray spectroscopy (EDS) and x-ray diffraction (XRD) using CuKα1 incident radiation from the top surface of the films. The backside of the films and Mo surface were analyzed after peeling the films at the interface between $Cu(InGa)Se_2$ and Mo. Solar cells with a device structure of glass/Mo/$Cu(InGa)Se_2$/CdS/ZnO:ITO/Ni:Al grid were fabricated. Current-voltage (J-V) characteristics and external quantum efficiency (EQE) curves of the solar cells were measured.

XRD measurements indicate that the selenization reaction rates for the two copper selenide precursors are faster than for the $Cu_{0.8}Ga_{0.2}$/In precursor. After 5 min selenization, intermetallic Cu_3Ga and $Cu_9(GaIn)_4$, as well as InSe and $Cu(InGa)Se_2$ phases were identified by XRD for the films made from $Cu_{0.8}Ga_{0.2}$/In precursors. In contrast, only the InSe phase was identified along with $Cu(InGa)Se_2$ for the films made from CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors. After 15 min selenization, only $Cu(InGa)Se_2$ was seen in the XRD plots for the two copper selenide precursors, but Cu_9Ga_4 was still present for the $Cu_{0.8}Ga_{0.2}$/In precursor. After 90 min selenization, a $MoSe_2$ phase was seen for the CuSe/Ga/In precursor in addition to $Cu(InGa)Se_2$.

$Cu(InGa)Se_2$ (112) peaks from XRD plots of films after 90 min selenization are shown in Figure 29. Broader peaks indicate a broader Ga distribution in the $Cu(InGa)Se_2$ chalcopyrite structure for the films made from CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors compared to the control with $Cu_{0.8}Ga_{0.2}$/In precursors.

Ga/(In+Ga) ratios measured by EDS from the top and backside of the films after 5, 15, and 90 min selenizations are shown in Figure 30. The films made from $Cu_{2-x}Se$/Ga/In precursors show a more homogeneous Ga distribution than the control. In contrast, the films made from CuSe/Ga/In precursors show a higher Ga concentration in the front half of the film than in the back. While the high Ga concentration at the back for metallic precursors can be explained by the reaction preference of Se with the Cu-In intermetallic over that of Cu-Ga, the higher Ga at the front for CuSe/Ga/In precursors is not understood.

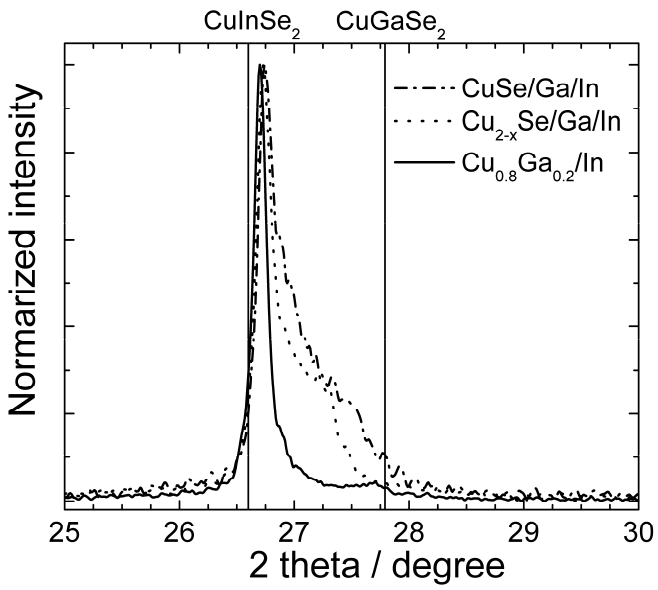


Figure 29. XRD scans of the $Cu(InGa)Se_2$ (112) peak after 90 min. selenization of CuSe/Ga/In, $Cu_{2-x}Se$/Ga/In, and $Cu_{0.8}Ga_{0.2}$/In precursors. Peak positions of $CuInSe_2$ and $CuGaSe_2$ are also indicated.

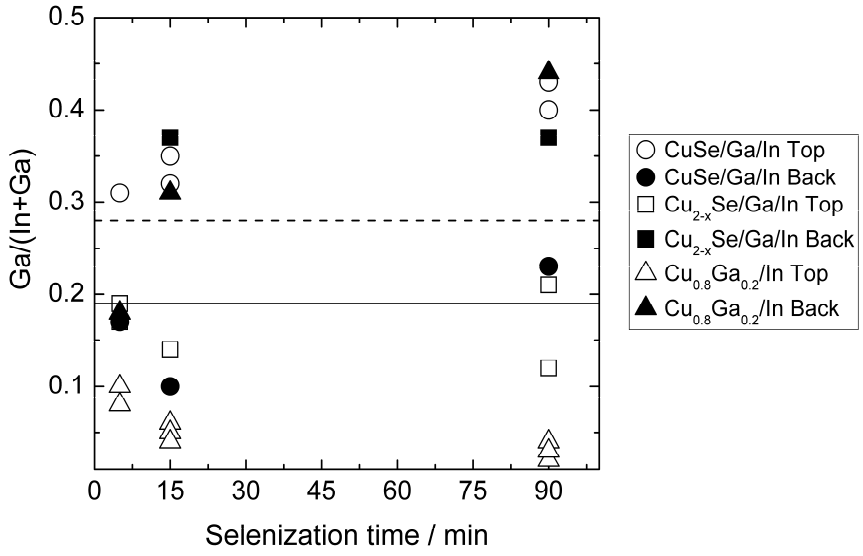


Figure 30. [Ga]/[In+Ga] ratios measured by EDS form the top and back sides of films selenized for different times. The dashed line shows [Ga]/[In+Ga] in the CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors and the solid line shows [Ga]/[In+Ga] in the $Cu_{0.8}Ga_{0.2}$/In precursor.

Device results of the solar cells made from the precursors following 15 min and 90 min selenization treatments are shown in Table XIX. After 15 min selenization, devices made from CuSe/Ga/In and $Cu_{2-x}Se$/Ga/In precursors showed higher performance than the control. This is consistent with faster selenization rates for the copper selenide precursors compared to $Cu_{0.8}Ga_{0.2}$/In precursor. After 90 min selenization, comparable conversion efficiencies were obtained from CuSe/Ga/In and $Cu_{0.8}Ga_{0.2}$/In precursors but no improvement in V_{OC} was seen.

Table XIX. Device parameters of solar cells made with 15 or 90 min selenized films.

Precursor	Selenization time (min)	J_{SC} (mA/cm^{-2})	V_{OC} (mV)	FF (%)	η (%)
CuSe/Ga/In	15	30.8	460	44.8	6.4
$Cu_{2-x}Se$/Ga/In	15	16.4	408	42.5	2.9
$Cu_{0.8}Ga_{0.2}$/In	15	18.3	81	26.3	0.4
CuSe/Ga/In	90	28.9	498	61.8	8.9
$Cu_{2-x}Se$/Ga/In	90	19.6	492	60.5	5.8
$Cu_{0.8}Ga_{0.2}$/In	90	36.8	474	50.5	8.8

Figure 31 shows EQE curves of the solar cells. The shift of the long wavelength edge of the EQE towards shorter wavelengths implies a wider bandgap consistent with the increased Ga near the front of the $Cu(InGa)Se_2$ for the films made from the copper selenide precursors.

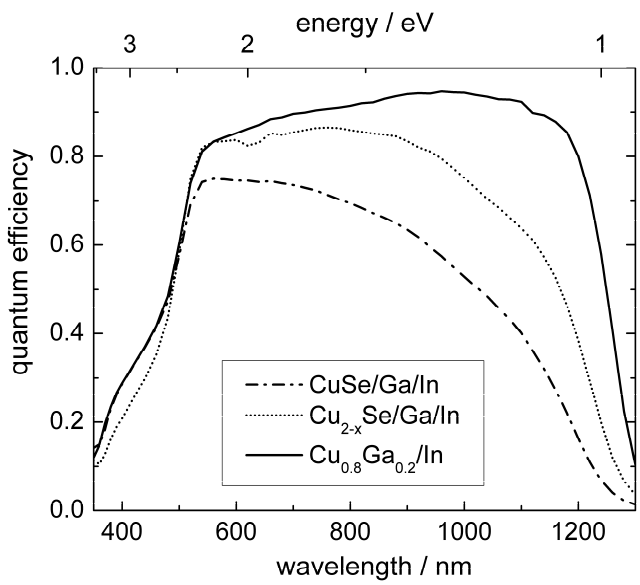


Figure 31. QE curves for devices with CuSe/Ga/In, $Cu_{2-x}Se$/Ga/In, and $Cu_{0.8}Ga_{0.2}$/In precursors after 90 min selenization.

4 Si-Based Solar Cells

4.1 Surface Passivation Quality and Structure of Thin Si:H Layers on N-Type Crystalline Si (100) and (111) Wafers

4.1.1 Background

The key aspects of high efficiency (>21%) crystalline silicon (c-Si) heterojunction (SHJ) solar cells are reduced surface recombination and low emitter saturation currents using a thin (< 10 nm) intrinsic a-Si (a-Si:H) buffer (i-layer) on both surfaces of the c-Si wafer.[22] The reduction of surface recombination by minimizing structural and electronic defects at the interface between a-Si:H and c-Si increases cell open circuit voltages (V_{OC}). However, the deposition of thin a-Si:H films in radio frequency (RF) plasma enhanced chemical vapor deposition (PECVD) or hot wire (HW) CVD on clean hydrogen terminated single crystalline Si wafer often starts with an unintentional epitaxial layer, which adversely affects the cell performances with low V_{OC}.[23,24] Such epitaxial Si growth has been found to be dependent on the doping level and prior surface treatment of the c-Si wafers.[24,25] Additionally, surface crystallographic orientation can be altered by surface conditioning- e.g., Si(100) surface changes to Si(111) after texturing. It is therefore imperative to study the structure of the deposited hydrogenated silicon (Si:H) layer and to correlate it with the passivation quality of the Si surface with different wafer orientations.

In this work, we studied the surface passivation quality of Si:H intrinsic (i-) layers deposited with varying hydrogen dilution in RF and direct current (DC) PECVD process on float zone (FZ) n-type single crystalline Si (100) and (111) wafers and correlate with the device performances of SHJ cells. Comparison between the DC and RF processes elucidates the effect of ion bombardment, if any, on Si surface passivation and cell performances during growth of these thin layers. The SHJ cells were also fabricated on n-type textured Czochralski (Cz) Si wafers, where (100) surface changes to (111) after texturing to realize the benefit of light scattering.

4.1.2 Experimental Procedure

The n-type Si wafers (~300 μm) with resistivity of 1.0 Ω.cm for (100) and 2.5 Ω.cm for (111) were cleaned for 5 mins in a mixture of H_2SO_4:H_2O_2 (4:1) followed by 5 mins rinse in de-ionized water and in 10% HF for 30 sec prior to each Si:H deposition. The Si:H i-layers (10 nm) were deposited on both sides by RF and DC plasma process using a six-chamber large area (30 × 35 cm²) deposition system. The substrate temperature, deposition pressure and SiH_4 flow rate were fixed at 200°C, 1250 mTorr and 20 sccm, respectively. The primary variable in the i-layer process is the H_2 flow rate, which was varied from 0 to 200 sccm and characterized by the dilution ratio $R = H_2/SiH_4$. The RF power of 30 W and a DC plasma current of 123 mA were maintained constant. The quality of surface passivation was determined by measuring effective minority carrier lifetime (τ_{eff}) using photoconductive decay method.[26] In this work, all τ_{eff} values are reported at a carrier density of 10^{15} cm^{-3} in the Si wafer. Additionally, Brewster Angle Fourier Transformed Infrared Spectroscopy (FTIR) and variable angle spectroscopic

ellipsometry (VASE) measurements were used to characterize the hydrogen bondings and film structure respectively of the thin i-layers and are discussed with respect to their surface passivation quality of c-Si wafer. Thin layers (10 nm) of p-type a-Si:H emitter followed by 70 nm Indium Tin Oxide (ITO) with metal grids in the front and n-type a-Si:H followed by evaporated Al contact on the rear were deposited to fabricate SHJ cells. The SHJ cells are characterized by J-V measurement with AM1.5 illumination.

4.1.3 Results and Discussion

Figure 32 shows the τ_{eff} as a function of R for i-layers deposited on (100) and (111) wafers by DC and RF plasma after annealing the samples at 280°C for 10 mins. It is worth noting that the DC plasma process will have a significantly higher ion bombardment compared to RF in otherwise similar plasma parameters due to higher plasma potential. Three distinct regions can be identified in the variation of τ_{eff} with R (Figure 1). In region I (R < 2), τ_{eff} shows plasma process dependence, namely, DC plasma deposited i-layer at R = 0 show slightly lower lifetime (~ 500 μsec) compared to RF plasma deposited i-layers (> 1 msec) irrespective of the wafer surface orientation. The τ_{eff}, however, becomes similar for both RF and DC plasma deposited i-layers at R > 2 (region II and III in Figure 32), implying little / no deleterious effect of ion damage in DC process on Si surface passivation.

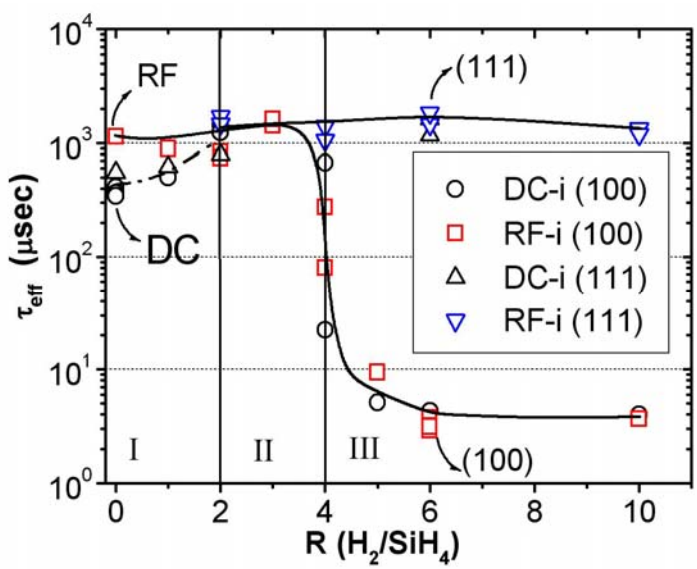


Figure 32. Effective minority carrier lifetime (τ_{eff}) on Si (100) and (111) wafers after depositing 10 nm Si:H i-layer on both sides by RF and DC plasma CVD with varying hydrogen dilution (R).

In region III (R > 4), however, the measured τ_{eff} exhibits a pronounced Si surface orientation dependence. The values of τ_{eff} sharply decreases to < 10 μsec on (100) wafers for i-layers deposited with R > 4, while on (111) wafers remains > 1 msec even at R = 10 for both RF and DC process. In order to get more insight about the variation of τ_{eff} and hence the surface passivation quality of i-layers with R, we have performed structural

characterization of the same thin i-layers on Si (100) and Si (111) wafers.

FTIR spectra provide important information about the hydrogen bonding structure in the film. Hydrogen bonded as di-hydride (SiH_2) is believed to produce micro voids and defects in a-Si:H film, while the mono-hydride (SiH) bonding is preferred for good quality films.[27,28] Figure 33 shows the comparison of FTIR spectra for i-layers grown by RF and DC plasma process at different R to understand the process dependence of passivation quality (region-I in Figure 32).

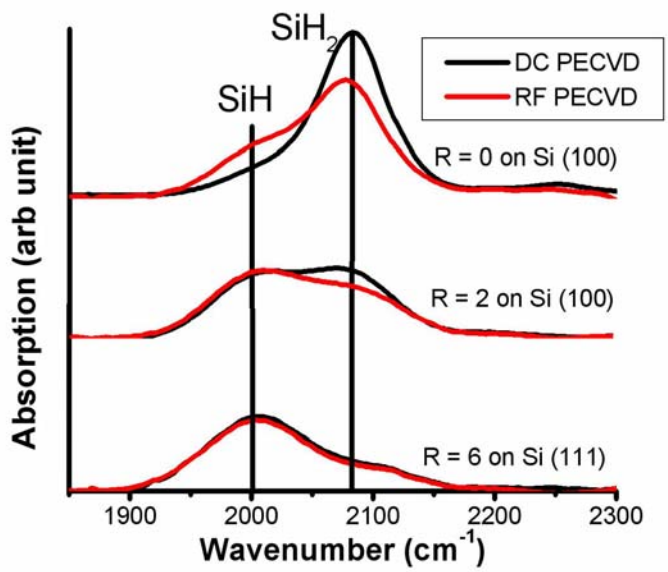


Figure 33. Comparison of FTIR spectra of 10 nm thick Si:H i-layers grown by RF and DC plasma process with different R.

The peak intensities at 2090 cm^{-1} and 2000 cm^{-1} in FTIR spectra (Figure2) are due to SiH_2 and SiH stretching vibration respectively. The intensity of SiH_2 increases monotonically with the decrease of R, and at low hydrogen dilution ($R \leq 2$), DC plasma deposited i-layer has more SiH_2 compared to RF process, thereby reduces τ_{eff}. At R = 0, it is likely to have significant poly-silane formation in the plasma, which contributes to the film growth for both DC and RF processes with comparatively higher in DC due to presence of a larger amount of reactive ionic species. Poly-silane in the plasma is known to produce a-Si:H films with more microvoids and SiH_2. Formation of poly-silane decreases with an increase of R in DC plasma[29] and the resulting film exhibits comparable SiH_2 bonding at R = 6. However, despite a large variation of SiH_2 bonding in the film deposited by both RF and DC plasma with different R, rather small changes in τ_{eff} (only by a factor of 2 for R = 0) as shown in Figure 32 suggest that the passivation quality of a-Si:H i-layers is only weakly dependent on the amount of SiH_2 and defects in the i-layer. On the other hand, the τ_{eff} decreases more than two orders of magnitude on (100) compared to (111) wafers at $R > 4$.

To understand the wafer surface orientation dependence of τ_{eff}, film structure was determined from VASE measurements on the same samples used for lifetime testing. The imaginary part of pseudo dielectric constant, ε_2 is plotted as a function of photon energy in Figure 34 for Si:H films deposited on (100) and (111) wafers at different R.

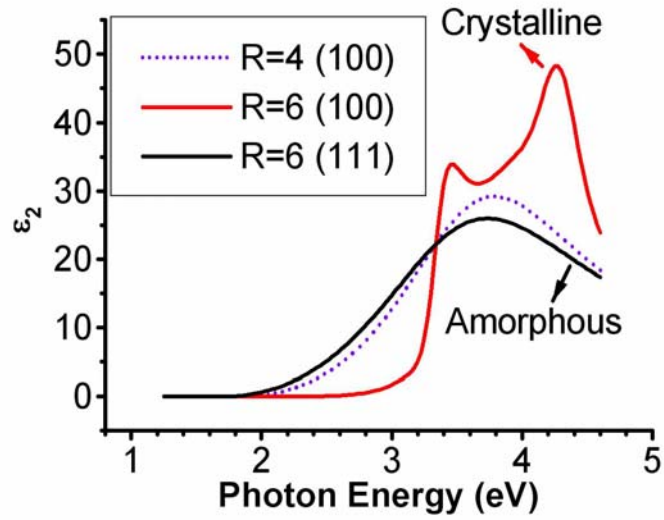


Figure 34. Imaginary part of pseudo-dielectric function, ε_2 as a function of photon energy for the Si:H i-layers deposited on Si(100) with R = 4 and 6 and on Si(111) with R = 6 in RF plasma process.

A broad featureless spectra for R = 6 i-layer on Si (111) wafer are indicative of amorphous Si:H structure; however, the Si:H layer deposited with R = 6 on (100) wafer exhibit the same optical constants as crystalline silicon, which implies that the film is completely epitaxial. A narrower peak width for i-layer grown at R = 4 on Si (100) wafer suggest that the film contains some fraction of crystallinity in largely amorphous phase. Therefore, the variation of τ_{eff} with R on Si (100) surface in Figure 32 indicates that any crystallinity or epitaxial growth of i-layer severely deteriorates the surface passivation quality of the deposited layer. Low value of τ_{eff} and loss of surface passivation on (100) wafers by R > 4 i-layers are likely due to the low band gap of epitaxial or nanocrystalline Si layers.

After completion of lifetime testing and detail structural characterizations, the same samples were converted into SHJ cells by depositing p- and n-type a-Si:H including the ITO and metal contacts. Therefore, the results allowed a direct comparison of the surface passivation quality of i-layers and their influences on the SHJ cell performances. The short circuit current density (J_{SC}) values were rather similar for all the devices, while the cell efficiency changes with R in i-layers due to changes in V_{OC} and fill factor (FF). Figure 35 shows the variation of V_{OC} and FF of the cells as a function of R for i-layers deposited on (100) by DC and on both (100) and (111) wafers by RF plasma.

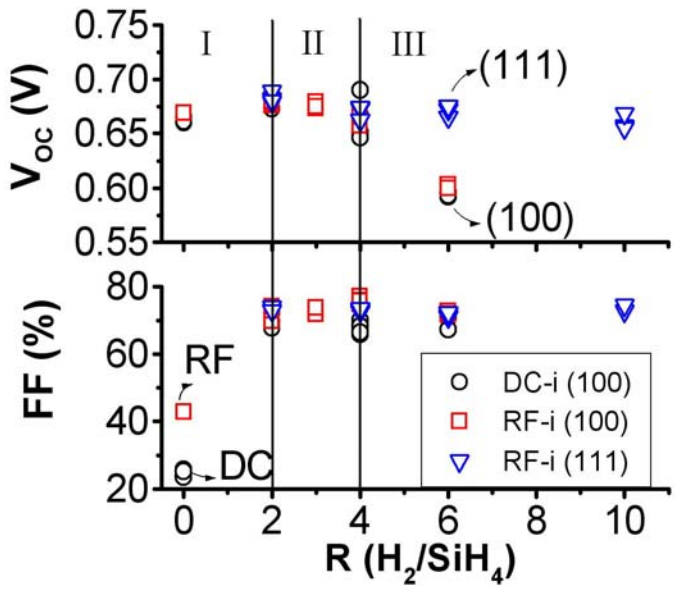


Figure 35. Open circuit voltage (V_{OC}) and fill factor (FF) of SHJ cells on Si (100) and (111) wafers with i-layers deposited at different hydrogen dilution (R) by RF and DC plasma process.

The figure clearly demonstrates that the V_{OC} exhibits pronounced wafer orientation dependence in region III (R = 6), while FF exhibits only plasma process dependence in region I (R = 0). The cell V_{OC} roughly correlates to the variation of τ_{eff} with R as shown in Figure 1, and decreases to ~ 600 mV for the i-layer deposited with R = 6, demonstrating the necessity of high τ_{eff} and good surface passivation quality to achieve high V_{OC}. However, high value of τ_{eff} alone does not insure a high efficiency device because the FF decreases drastically to < 50% with an "S" shape J-V for the i-layers grown at R = 0, despite exhibiting τ_{eff} of > 1 msec in the RF process in Figure 32. The poly-silane contribution in the film growth at R = 0 forms a wider band gap layer, as estimated from the Tauc's plot (the result is not shown here and will be reported elsewhere) with higher SiH_2 bonding and microstructural defects for both processes with an enhanced effect in DC discharge. Such a wide band gap defective a-Si:H film severely inhibits carrier transport across the i-layer, particularly the hole transport over a large valence band offset in the emitter side and reduces FF. On the other hand, epitaxial / nanocrystalline growth at R = 6 narrows the band gap of the deposited layer and therefore does not affect hole transport and cell FF, but results in low V_{OC} due to insufficient surface passivation. Consequently, the highest SHJ cell efficiency was obtained for i-layers deposited with R = 2.

Table XX summarizes the device performances on n-type polished FZ (100), (111) and n-type textured Cz wafers with i-layers deposited by DC and RF processes with R = 2. Both plasma processes demonstrate SHJ cells with high efficiency and high V_{OC}, therefore, seemingly higher ion bombardment in DC process have neither any effect on surface passivation nor in the cell performance. The SHJ cell efficiency of 18.8% with V_{OC} of 694 mV was achieved on a textured Cz wafer due to efficient light scattering and

additional MgF_2 anti-reflection (AR) layer in the front light illuminating surface.

Table XX. Summary of the SHJ cell performance on polished FZ (100), (111) and textured Cz wafers with the i-layers deposited by both DC and RF processes. The efficiency (η) values are not independently confirmed.

n-type Wafer	a-Si:H i-layer process	V_{OC} (mV)	FF (%)	J_{SC} (mA/cm^2)	η (%)
FZ (100)	DC	686	72.2	32.8	16.2
	RF	680	74.1	32.6	16.4
FZ (111)	RF	689	74.0	33.8	17.2
Text. Cz with MgF_2	DC	694	74.4	36.4	18.8

4.1.4 Conclusions Regarding Dependence of Wafer Orientation on Passivation and Structure

Excellent surface passivation and high effective minority carrier lifetime (> 1 msec) is achieved by depositing thin a-Si:H i-layers using both RF and DC plasma process with hydrogen dilution. Any epitaxial growth or presence of crystallinity in the i-layer severely reduces minority carrier lifetime and cell V_{OC}. The structure of thin Si:H layer depend on the surface orientation of single crystalline Si. Undesirable epitaxial growth of Si:H films is more likely to occur on Si (100) compared to (111) surface. The SHJ cell efficiency approaching 19% with V_{OC} of 694 mV was achieved on textured Cz wafer using DC plasma deposited i-layer.

4.2 Evaluation of HF Treated A-Si for Photoemission Determined Electronic Levels

4.2.1 Background

Silicon heterojunction (SHJ) solar cells have stimulated much attention due to their numerous attractive features such as deposited junctions, open circuit voltages above 700mV and conversion efficiencies above 21%.[30] The archetypical SHJ cell utilizes a c-Si wafer as the absorber passivated by thin intrinsic a-Si:H. Doped (p) and (n)a-S:H are utilized to generate the front junction and rear back surface field. A-Si and its alloys have been extensively studied. Films with a range of electrical and material properties such as band gaps, doping levels, defect densities, and microstructure are well documented. However, there has not been sufficient effort to bridge film properties to SHJ cell performance, even though band offsets and defect densities will largely determine cell performance.[31] In this section, we report quantification of the electronic levels of device quality doped and intrinsic a-Si:H films as determined from ultra violet photoemission (UPS) using the Brookhaven National Laboratory Synchrotron Light Source.

Due to the extreme surface sensitivity of the photoemission process (10-50Å sampling depth), any surface modification that results in surface band bending, defect

related Fermi pinning or introduction of states at the top (bottom) of the valence (conduction) band will render the measurements of dubious value. To our knowledge, only a single group has been able to perform *in situ* yield spectroscopy analysis of doped and intrinsic a-Si:H films prepared by PECVD.[31] *Ex situ* deposited doped films subsequently bombarded by Ar ions for surface cleaning have also been studied.[32] It was demonstrated, however, that substantial Fermi level pinning results due to the high density of defect states introduced by ion damage rendering Ar sputtering inappropriate for the purpose of this experiment.

To overcome these potential pitfalls, a novel strategy for sample preparation relying on H-termination of the a-Si:H films by wet-chemical treatment with final dilute HF dip was used. This surface passivation has been widely employed for c-Si wafer preparation but less is documented regarding its application to amorphous Si films. A separate report has shown the effectiveness of this treatment with regards to native oxide removal and resistance to contamination on short time scales.[34]

4.2.2 Experimental Methods

The sample set is comprised of PECVD deposited 150nm thick a-Si:H films deposited on H-terminated 2.5Ωcm (n)c-Si and (p)-c-Si of (111) orientation. The present study will focus on DC and RF plasma deposited (i)-type films as well as DC plasma (p)- and (n)-type films with 2% dopant precursor (B_2H_6 and PH_3, respectively) to SiH_4 gas phase concentration. These same deposition conditions were used to fabricate an 18.8% SHJ photovoltaic cell.[33] Very little dependency on material properties and passivation quality has been detected between the RF and DC i-layers at the deposition conditions used, so comparison of their results will provide a self-consistency check. Co-deposited films on 7059 glass substrates were used for optical reflection and transmission measurements in order to estimate the band gap from Tauc's plot.

A specific cleaning procedure was developed for this study to provide H-terminated a-Si:H surface and resistance to contamination within the 5 min time frame required for loading into vacuum systems. Firstly, 4 min ultrasonic baths in acetone, methanol, and then deionized water (DIH_2O) removes debris and hydrocarbon contamination. This is followed by a wet-chemical oxidation step of 3:1 H_2SO_4:H_2O_2 at 70-80°C which grows and densifies the film's oxide surface. After another 3 min DIH_2O rinse, the films are dipped in 10%HF solution for 60 sec, dissolving the oxide and, ideally, saturating the surface with hydrides (≡SiH, =SiH_2, –SiH_3). A final 3 sec DIH_2O dip serves to improve sample handling safety and dissolve adsorbed F ions and HF molecules. XPS with Al Kα X-rays at 1487eV is used for chemical analysis of the wet-chemical clean. For more complete detail of the cleaning procedure the interested reader is directed to ref.[34]

For UPS measurements beamline U4A of Brookhaven National Laboratory Synchrotron Light Source is utilized providing photon energies from 10eV up to the soft x-ray range of 200eV. Due to the large photon flux and the flexibility to adjust for photon capture cross section as a function of probe beam energy one is able to perform a thorough analysis of the density of valence states (300meV resolution) and precisely

determine a surface valence band maximum relative to the Fermi level (90meV resolution). This work uses a beam energy of 55eV.

4.2.3 Results and Discussion

4.2.3.1 Cleaning Procedure Evaluation

Confirmation of oxide removal and surface state passivation by hydride bonding is achieved by XPS and UPS. Figure 36 shows the surface composition of the four a-Si:H films of interest, and for comparison, n-c-Si at three processing stages: as received, post wet-chemical oxidation, and post HF dip. Good control of surface composition is achieved as C drops to below 4%, O below 2.2%, and residual F below 0.8% for the three films (n)a-Si:H, RF (i)a-Si:H, DC (i)a-Si:H and the (n)c-Si wafer. Interestingly the (p)a-Si:H has slightly higher contamination levels with C, O, and F at 4.9%, 4.6%, and 3.1%, respectively. There is also a visible decrease in hydrophobicity post HF dip in the (p)a-Si:H case due to the increased fraction of highly electronegative species (O and F) on the surface. This would create a surface with a relatively higher degree of polar bonding and hence water molecule attraction through dipole interaction.

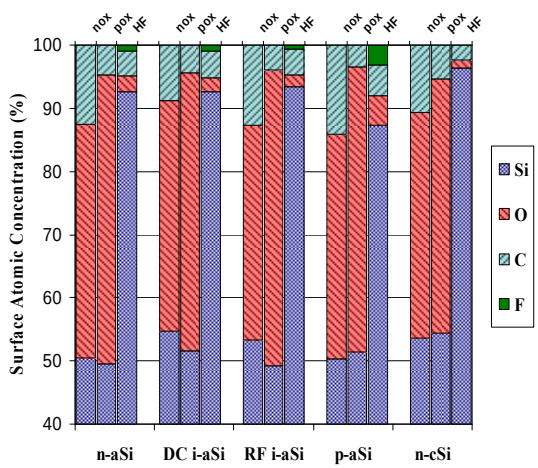


Figure 36. Surface atomic concentration from XPS. nox is the native oxide state, pox is post wet-chemical oxidation, HF is after HF dip.

Valence band spectra from UPS confirm the effectiveness of oxide removal and passivation of surface states post HF dip. Figure 37 shows a clear difference between native oxide covered RF (i)a-Si:H film before and after HF treatment. Due to the extreme surface sensitivity of photoemission carried out at 55eV photon energy the oxide states dominate in the untreated sample. A triplet of peaks are identified as OI, OII, and OIII. OI is the O 2*p* non-bonding pair of electrons at a binding energy of 7.1eV (from E_F), OII and OIII at 11.4eV and approximately 14eV correspond to O 2*p* electrons bonded to Si 3*p* and 3*s* states.[35] After HF dip three dominant peaks are readily observed at 2.8eV, 6.8eV, and 9.8eV labelled as α, β, and γ respectively. The lowest energy state that defines the top of the valence band centered at 2.8eV is derived from Si 3*p* states. The peaks at 6.8eV and 9.8eV are both Si 3*s* related bonded both to Si and H.[36] No Si-F derived states are detected and surface defect states are below detection levels estimated

to be 10^{13}-10^{14}cm^2. A future publication will delve into further detail regarding valence band spectra of HF treated (a)-Si:H films. To surmise: the valence band spectra post HF dip is dominated by Si—Si and Si—H in mono and di-hydride configuration. It is argued that during the dissolution of the native oxide on a-Si in HF potential, un-reacted surface states are passivated by hydrogen similar to the crystalline silicon case.

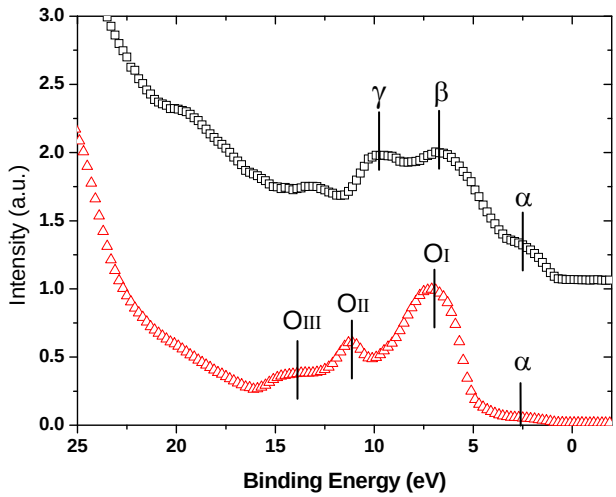


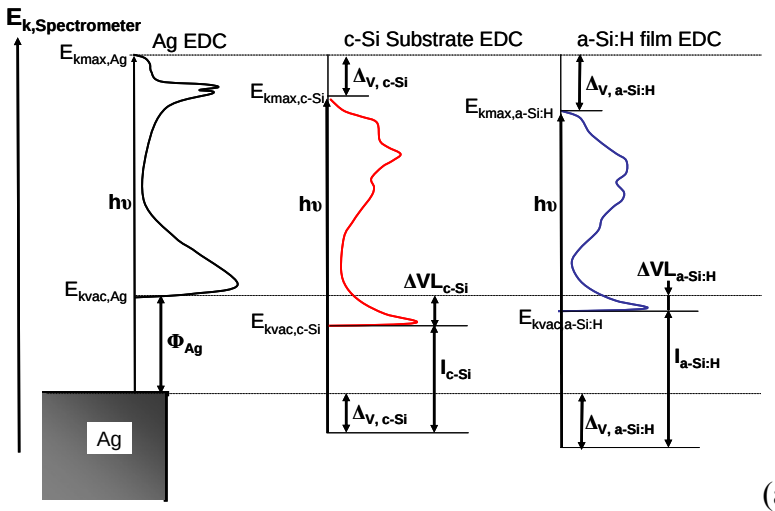
Figure 37. UPS valence band spectra of RF (i)a-Si, 55eV photon energy probe beam. Bottom curve is untreated with native oxide surface, top curve is post HF-dip. Probed by 55eV radiation, curves vertically offset for clarity.

4.2.3.2 Electronic Level Determination by UPS

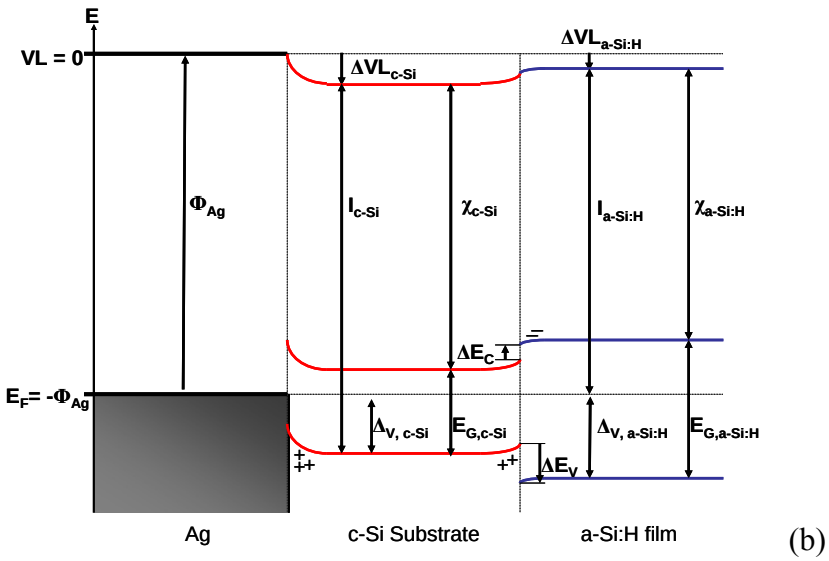
Electronic levels obtained by photoemission are determined by the measurement of five values: 1) hυ, the photon energy; 2) $E_{kmax,met}$; and 3) $E_{kvac,met}$, the highest and lowest kinetic energy electrons emitted from a noble metal surface (Ag or Au); 4) $E_{kmax,sc}$; and 5) $E_{kvac,sc}$, the highest and lowest kinetic energy electrons emitted from the semiconductor surface. The photon energy is precisely determined as the difference of $E_{kmax,met}$ from photons of the first and second order reflection off the diffraction grating. The Fermi energy of the system, $E_{kmax,met}$, is determined using the point of steepest descent of the step-like edge at the metal's maximum kinetic energy. The top of the valence band of a semiconductor, $E_{kmax,sc,}$ is the intersection of a linear extrapolation of the onset of the enegy distribution curve (EDC) to background noise level. Finally, E_{kvac} is the point of steepest descent of the lowest kinetic energy electrons detected; the secondary electrons generated from inelastic electron collisions within the material. The sample structure as probed is grounded by a metallic back plate held at a -5V bias to enable accurate detection of $E_{kvac,sc}$.

Full analysis must account for the interface between the metal, crystalline substrate, and amorphous film as well as potential surface dipoles. The simplest interpretation involves two assumptions: Fermi level alignment and absence of surface band bending. It can be argued that neither of these assumptions is unreasonable as it is expected that charge transfer across the two interfaces (metal/substrate and substrate/film) can reach

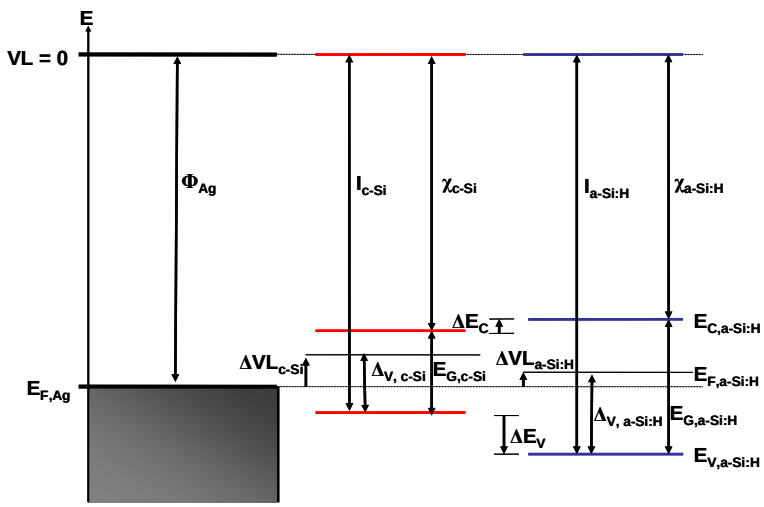
equilibrium due to sufficient conductivity. Plus the amorphous nature of the film surface and additional H-termination should reduce surface defect density to match bulk levels.



(a)



(b)



(c)

Figure 38. (a) Relative energy levels of the materials probed by UPS on the measured kinetic energy scale. (b) Schematic of band structure of Ag / c-Si / a-Si:H stack as probed assuming Fermi level alignment and absence of surface dipole. (c) Resulting electronic levels of isolated materials. Variables defined in body of text.

Figure 38(a) is a schematic that shows the relative levels of the spectrometer measured kinetic energies of the metal, c-Si substrate, and a-Si:H film. Making use of the four measured values using only the spectrometers kinetic energy scale; a number of important parameters can be defined, including:

$$\Phi_{met} = h\upsilon - (E_{kmax,met} - E_{kvac,met}) \quad (1)$$

$$I_{sc} = h\upsilon - (E_{kmax,sc} - E_{kvac,sc}) \quad (2)$$

$$\Delta_{V,sc} = E_{kmax,met} - E_{kmax,sc} \quad (3)$$

$$\Delta VL_{sc} = E_{kvac,met} - E_{kvac,sc} \quad (4)$$

where Φ_{met} is the work function of the metal used to define the Fermi level, I_{sc} is the ionization energy of the semiconductor, $\Delta_{V,sc}$ is the difference between E_F and the valence band maximum of the semiconductor, and ΔVL_{sc} is the change in the work function cut off. Specifically ΔVL_{sc} represents the shift in the vacuum level from that of the metal to the semiconductor.[37] Also since the band gap (E_G) has been determined by optical measurements, it follows:

$$\chi_{sc} = I_{sc} - E_G \quad (5)$$

$$\Delta_{C,sc} = E_G - \Delta_{V,sc} \quad (6)$$

χ_{sc} is the electron affinity of the semiconductor and $\Delta_{C,sc}$ is the difference between the conduction band minimum and E_F. Finally, as shown in Figures 7 (b) and (c), the conduction and valence band offsets can be calculated. Anderson's model[38] is often applied for the c-Si / a-Si:H heterojunction and predicts :

$$\Delta E_C = \chi_{a\text{-}Si:H} - \chi_{c\text{-}Si} \quad (7)$$

$$\Delta E_V = E_{G,a\text{-}Si:H} - E_{G,c\text{-}Si} - \Delta E_C \quad (8)$$

ΔE_C is the conduction band offset and ΔE_V the valence band offset. It is vital to the analysis is to separate which of the above equations depend on the assumptions of Fermi level alignment and absence of surface band bending. Equations (1), (2), and (5) depend only on a single material and do not depend on Fermi level alignment. Also it is understood that any surface dipole that would shift $E_{kmax,sc}$ from a bulk value will similarly effect the $E_{kvac,sc}$ and thus I_{sc} and χ_{sc} remain well defined values.

4.2.3.3 Implications of UPS Results

Table XXI shows the UPS results of films deposited on (n)c-Si substrate plus that of HF treated (n)c-Si itself and Table XXII contains the results of films deposited on (p)c-Si substrate. Encouragingly, the measured $\Delta_{V,(n)c\text{-}Si}$ and $\chi_{(n)c\text{-}Si}$ values are in excellent agreement with literature for 2.5Ωcm resistivity wafer.[39] The (n)c-Si / (n)a-Si:H sample is expected to be in nearly flat band condition which should lend itself to Fermi level alignment and thus accurate measurements of not only I and χ, but also Δ_V. Again acceptable agreement with literature values is observed compared to *in situ* deposited films studied by constant final state yield spectroscopy,[31] namely $\Delta_{V,(n)a\text{-}Si:H} = 1.30$–1.40eV. Considering the i-type films, there is good agreement for I and χ, independent of substrate and $\chi_{(i)a\text{-}Si:H} = 3.85$–3.91eV is in the expected range. However, there is a large Δ_V substrate dependency which is a very strong indication that the Fermi level alignment assumption is not satisfied as might be expected. If Fermi level alignment is achieved

through the probed stack (see Figure 7 (b)) $\Delta_{V,a\text{-}Si:H}$ would not vary depending on c-Si substrate doping, or equivalently, shifting the Fermi level up or down within the c-Si band gap. Further doubt of Fermi alignment comes from the (n)a-Si:H which also demonstrates Δ_V substrate doping dependency. Thus our results indicate the possibility of fixed interface charge at the c-Si / a-Si:H junction. It is beyond the scope of this project to fully consider these implications; however, initial investigations indicate that the (p)c-Si / (n) and (i)a-Si:H junctions do not achieve Fermi alignment and a compensating interface dipole exists. Also note that several measurements were repeated with the same sample on difference occasions with nearly identical results. This indicates that the results are not skewed by sample handling or poor grounding contacts that could result in large scatter within the data.

Table XXI. Electronic levels determined by UPS, all units in eV. Films on n-type substrates.

	I	E_G	χ	Δ_V
(n)c-Si	5.16	1.12	4.04	0.86
(n)a-Si:H	5.61	1.78	3.83	1.30
DC(i)a-Si:H	5.66	1.75	3.91	1.28
RF(i)a-Si:H	5.61	1.75	3.86	1.23

Table XXII. Electronic levels determined by UPS, all units in eV. Films on p-type substrates.

	I	E_G	χ	Δ_V
(n)a-Si:H	5.52	1.78	3.74	1.14
DC(i)a-Si:H	5.60	1.75	3.85	1.00
RF(i)a-Si:H	5.60	1.75	3.85	0.88
(p)a-Si:H	5.09	1.72	3.37	0.70

The calculated electron affinity of the p-type a-Si at 3.37eV is much less than expected. There exists fewer literature results reported for $\chi_{(p)a\text{-}Si:H}$ as it is often assumed to behave similarly to more thoroughly studied intrinsic a-Si. Rhaman and Furukawa report on a 1.8eV band gap (p)a-Si_xC_{1-x}:H (a small bandgap for silicon carbide near that of pure (p)a-Si:H suggesting comparability) with an electron affinity of 3.24eV.[40] If $\chi_{(p)a\text{-}Si:H} < 3.7$eV the majority of the band offset resides in the conduction band, an occurrence which has indeed been reported[41] and references therein. Unold *et al.* estimate from capacitance measurements of (p)a-Si:H / (n)c-Si devices a $\Delta E_C = 0.35 \pm 0.05$eV and suggest caution when applying intrinsic derived band offsets to doped a-Si and possible breakdown of the Anderson model.[42] Another consideration would be the use of DC plasma in the *doped* film deposition, the implications for which have not been reported. Further work will be required to fully explain this surprising result but it seems a strong indication that highly doped p-type a-Si has higher energy levels for the conduction and valence bands compared to i- and n-type.

4.2.4 Conclusions about Si Surface Passivation and Heterojunction Band Alignments

Oxide dissolution and H-termination of a-Si:H films by HF-dip has been demonstrated. Surface O plus F contamination was held below 3% for (n) and (i)a-Si:H and 7.7% for (p)a-Si:H. A clear derivation of energy level determination from measured kinetic energy values is laid out. Measured values of χ are independent of Fermi alignment and between 3.74–3.91eV for (n) and (i)a-Si:H, but only 3.37eV for (p)a-Si:H. Also it is concluded Fermi alignment is not achieved as indicated by Δ_V dependency on substrate doping. The initial investigation indicates the Fermi alignment is broken by fixed charge at the (p)c-Si / a-Si:H interface. Further study by electrical characterization and confirmation by modeling is required.

4.3 A-Si/C-Si Heterojunction for Interdigitated Back Contact Solar Cell

4.3.1 Background

Rear junction, interdigitated back contact (IBC) solar cells shown in Figure 39b have several advantages over the more common front junction solar cell with contacts on either side (Figure 39a). Moving all the contacts to the back of the cell eliminates contact shading, leading to a J_{SC}. With all the contacts on the back of the cell, series resistance losses are reduced as the trade-off between series resistance and reflectance is avoided and contacts can be made far larger. Having all the contacts on the one side simplifies cell stringing during module fabrication and improves the packing factor. The reduced stress on the wafers during interconnection improves yields, especially for large thin wafers. The more uniform appearance of the PV module is desirable for architectural applications.

While the advantages of rear junctions are well known, their implementation is hindered by several design constraints, which are circumvented by a-Si on crystalline silicon heterojunctions. First, since rear junction cells require diffusion lengths greater than twice the device thickness, thin wafers are attractive. Using low temperature depositions rather than high temperature diffusions decreases the thermal stress and reduces the bowing in thin wafers. Second, rear junction designs require low front surface recombination velocities, which can be provided by deposited passivation layers. Thirdly, the central challenge in rear junction solar cells, patterning the rear, is easier in silicon heterojunctions since it is much easier to mask and etch depositions than diffusions, and further isolation between p/n a-Si layers is not always necessary.

All back contact cells are particularly suited to heterojunctions as they eliminate the costly front transparent conductive oxide (typically indium-tin-oxide) along with its absorption losses. Interestingly, with the heterojunction material on the rear, it no longer needs to be transparent and thus there is a wider flexibility in choosing heterojunction partner materials.

The interdigitated back contact silicon heterojunction (IBC-SHJ) devices described in this section potentially combine the advantages of the two leading high efficiency technologies, namely, the high V_{OC} of heterojunction cells and the high J_{SC} and FF of rear junction cells.

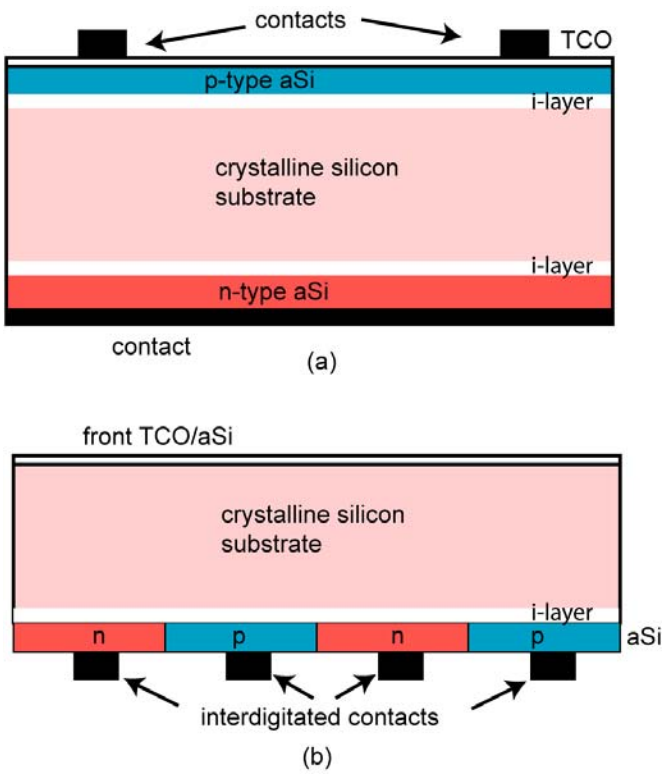


Figure 39. (a) Standard front junction design. (b) Rear junction design with interdigitated back contacts (IBC-SHJ). Devices are fabricated with and without the intrinsic buffer layers between the doped a-Si and c-Si.

4.3.2 Device Structure and Fabrication

The IBC-SHJ device consists of a 1-3 ohm.cm, 300µm thick, n-type float zone c-Si substrate with rear interdigitated strips of n and p a-Si, with widths of 0.5 mm and 1.2 mm, respectively. The a-Si is covered with aluminium metal as robust contacts. The front surface of the substrate is passivated with intrinsic a-Si layer followed by anti-reflection coating. All a-Si depositions are performed in DC plasma enhanced chemical vapour deposition (PECVD) system at 170°C. We have also used RF plasmas (13.56 MHz) but find little practical difference.[43] Presently the interdigitation is achieved through the use of photolithography, but the large millimeter-sized dimensions allow for other options to be investigated.

4.3.3 Device without Rear Intrinsic Layer

Initial heterojunction back contact cells were fabricated using doped layers only on the back. Without an intermediate intrinsic a-Si buffer layer, the V_{OC} is limited to around 600 mV[44,45], but the cell optimization is more straightforward since the i-layer often reduces the FF (see Section 4.3.4). Using the doped only contacts, the device had an efficiency of 11.8%, V_{OC} of 602 mV, J_{SC} of 26.7 mA/cm^2 and FF of 73%.[46] Notably the device has a high shunt resistance, showing that it is easy and straightforward to separate the heavily doped p and n contact regions with a silicon heterojunction, unlike the diffused-junction devices[47] where shunting is more likely to happen.

Texturing the substrate and improving the front AR coating (presently absorbing ITO) will increase the current. We have applied texturing to our front junction cells and increased the current by 10% but the V_{OC} only decreases by 10 mV.

4.3.4 High V_{OC} with Intrinsic Layer

The device reported in the previous section was fabricated without the use of an intrinsic a-Si buffer layer. The absence of the buffer layer simplifies fabrication, and ensures a high FF, but increases the recombination at the a-Si/crystalline silicon interface. Much higher V_{OC}'s are attainable if an intrinsic buffer layer is inserted between the doped a-Si and the c-Si substrate. For example, on standard front junction SHJ devices at IEC (Figure 39a), we have obtained a V_{OC} of 703 mV with an intrinsic buffer layer, but only 622 mV without the buffer layer. For IBC device, inserting an i-layer at the rear increased the V_{OC} from 602 mV to 691 mV (Table XXIII), and compares favorably with the 681 mV obtained by Sunpower on their record rear junction device. However, a disadvantage of inserting the intrinsic buffer layer is that it can reduce conduction of carriers and lead to low fill factors. Front junction cells fabricated at IEC initially had the same problem of very low FFs; however, optimization of the i-layers enabled the FFs to exceed 70 % with only a slight drop in V_{OC}, from 703 mV to 693 mV, and efficiency of 18% has been obtained.

Table XXIII. Effect of intermediate buffer layers of V_{OC}'s on front and rear heterojunction devices.

Cell	V_{OC} (mV)
Front Junction (no i-layer)	622
Front Junction (i-layer)	703*
IBC (no i-layer)	602
IBC (i-layer)	691

*Textured Cz substrate. Other substrates are planar FZ.

4.3.5 Two-Dimensional Cell Modeling

The interdigitated back-contact heterojunction device combines two technologies with challenging modelling requirements. Firstly, an all back contact device is an inherently two-dimensional structure that is difficult to model analytically or using a standard one-dimensional program such as PC1D. Secondly, heterojunction devices incorporating a-Si have also proven difficult to model, often requiring the development of new modelling programs.

The Sentaurus device modelling package is extensively used for modelling opto-electronic devices and is suited for modelling solar cells through the inclusion of DESSIS. The latest version includes complex defect models allowing the simulation of devices including a-Si. The critical parameters included in our study are energy distribution of the exponential band tails, and the Gaussian distribution of the mid-gap trap states. These are essential for the accurate modelling of any a-Si device. In

simulation, they are chosen based on reference[48] and were tuned to fit the experimental properties (e.g. band gap, dark and light conductivity) of deposited a-Si layers. A further benefit of the Sentaurus pack is that it includes realistic optical effects such as absorption in the amorphous layer.

To determine the origin of the fill factors in the back contact cells with i-layers, two cells following the schematics of Figure 39 were made with identical a-Si deposition conditions. In both cells, there is a 10 nm i-layer inserted between the doped a-Si layers and the c-Si substrate.

It is well established that the insertion of an intrinsic layer at the heterojunction interface increases the V_{OC} for both the front and rear junction devices. However, while the FF of front junction cells are relatively unchanged, the FF on IBC-SHJ devices dropped dramatically from 73% to 37%. The loss of FF is shown in the JV curves of Figure 40. The JV curve is flat into reverse bias indicating that the loss in FF is not due to shunting between the n and p-strips. Successive runs using similar conditions showed that low FFs are more of a problem with IBC-SHJ cells than with the front junction devices.

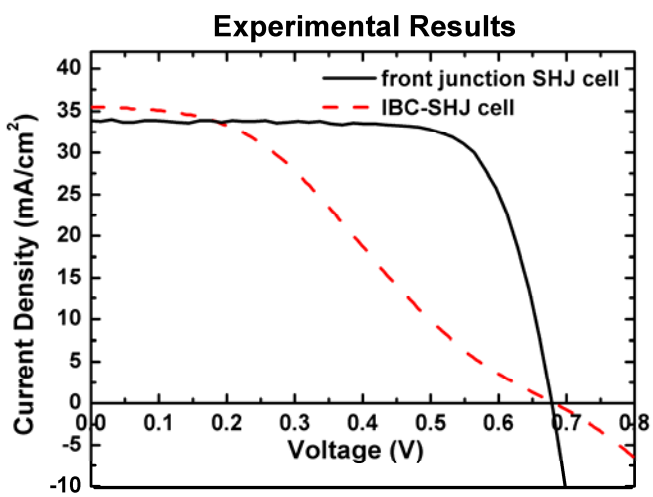


Figure 40. Measured JV curves for front and rear junction solar cells. The i-layer has the same thickness of 10 nm in both devices.

The front-junction and IBC devices of Figure 40 were both modelled with Sentaurus and are presented in Figure 41. The simulation conditions, hetero-interface model and the material properties of doped a-Si, intrinsic a-Si, c-Si wafer, for both devices are identical except the structure itself. The results match the experimental data with a FF drop evident in the IBC cell but not in the front junction cells.

There are a number of possible causes for the large difference in FF between the two devices. The current density is higher at the interface in the IBC cells as the interdigitation of the contacts means that approximately half the area is available to each contact. A more likely cause is the effect of the illumination on the i-layer due to

photoconductivity of the intrinsic a-Si or changing the band alignment at each interface. Most of the light is absorbed at the front surface, so that the carrier concentration at the junction in a front junction device is far larger than the carrier concentration at the junction for the IBC cell.

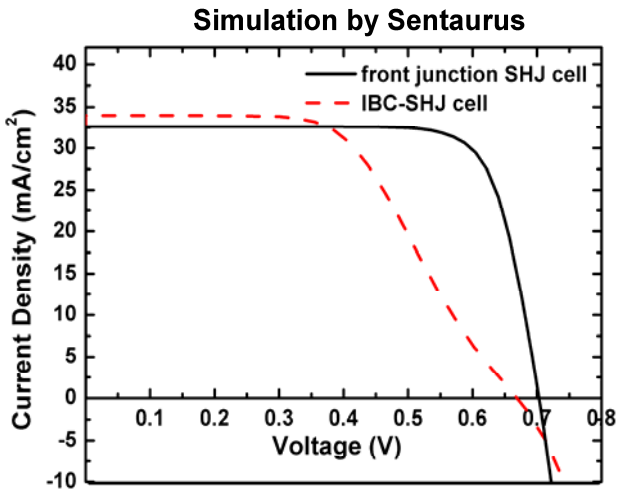


Figure 41. Modelling of front and rear junction cell with Sentaurus. The loss in FF on the IBC-SHJ cell matches the experimental results in Figure 40.

The S-shaped curve present in the IBC-SHJ cell is similar to those seen for front junction cells that were obtained when the i-layer is too thick or the surface at the interface is contaminated. We achieved an improvement in the front junction cells by changing the processing steps and deposition conditions of the a-Si layers. Similar optimizations of IBC-SHJ solar cells are ongoing.

4.3.6 Front Surface Passivation

It was noticed that the performance of IBC-SHJ solar cell depends on the front surface passivation.[46] Simulation of an IBC-SHJ solar cell without back surface intrinsic a-Si layer but with different front surface recombination velocity S was performed, and the resulting J-V curves are shown in Figure 42. As seen, both J_{SC} and V_{OC} increase as S decreases, resulting in higher cell efficiency. Since most carriers are generated near the front surface, while the p-n junction is far at the back surface, high front S would cause carrier recombination before they reach the back junction.

Further, the Sentaurus modelled JV curve can also be used to extract the front surface recombination velocity if good back surface passivation is assumed instead of inserting the i-layer. In Figure 42, the front surface recombination velocity S of 80 cm/s (line with dots) provides a good match to the experimental 680 mV high voltage. This S value is consistent to the surface recombination velocity of 82 cm/s extracted from IQE curve by using PC1D.[46]

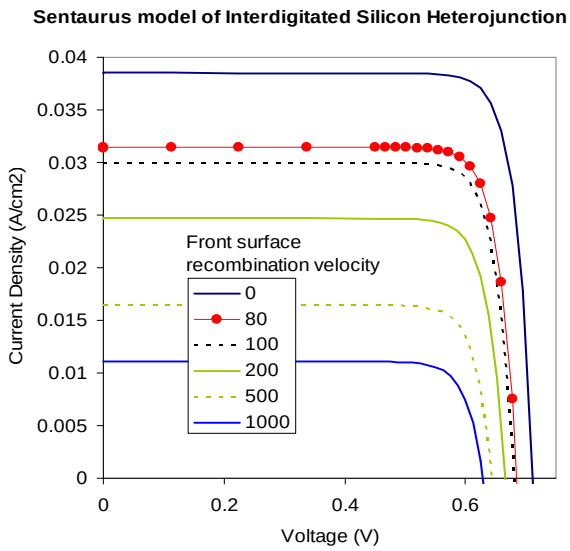


Figure 42. Sentaurus modelling of an IBC-SHJ solar cell. The line with dots shows the fit to the 680 mV device indicating that the front surface recombination velocity is 80 cm/s.

4.3.7 Effect Of Strip Dimensions On Ibc-Shj Performance

Sentaurus modelling was also used to assist in the optimization of the dimensions of the back contact strips. There is a trade off in the relative sizes of the strips. The recombination at the p-type collecting junction is higher than at the n-type passivation but carriers generated above the n-type strips have to travel further to reach the collection junction. There is thus a trade off in the relative sizes of the p an n strips. Due to resistive parastics caused by the i-layers, the strip optimization was performed on devices without the intermediate i-layer on the back of the cells. J_{SC} is normalised to account for differences in front surface reflection and absorption in the ITO which is present in the actual cells but not in the model.

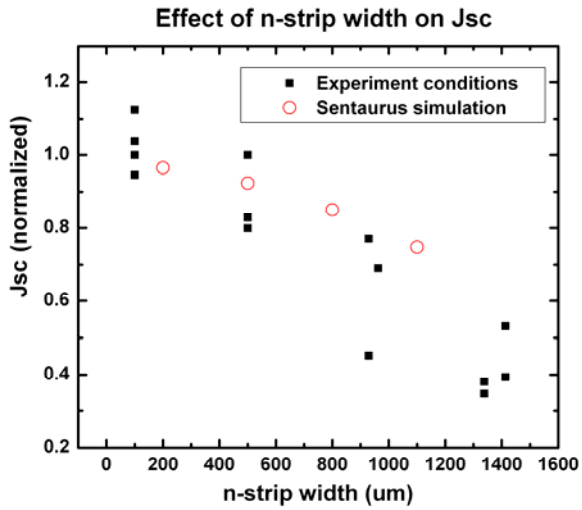


Figure 43. Effect of the width of n-strips on J_{SC}. The total device dimension is fixed so wider n-strips result in narrower p-strips.

The optimization of the strip width is shown in Figure 43. The simulation was performed by keeping the total device dimension fixed, hence wider n-strips result in narrower p-strips. It can be seen that for the passivation conditions used in simulation (which matches experiments), as n-strip width increases, J_{SC} decreases, resulting in lower cell efficiency.

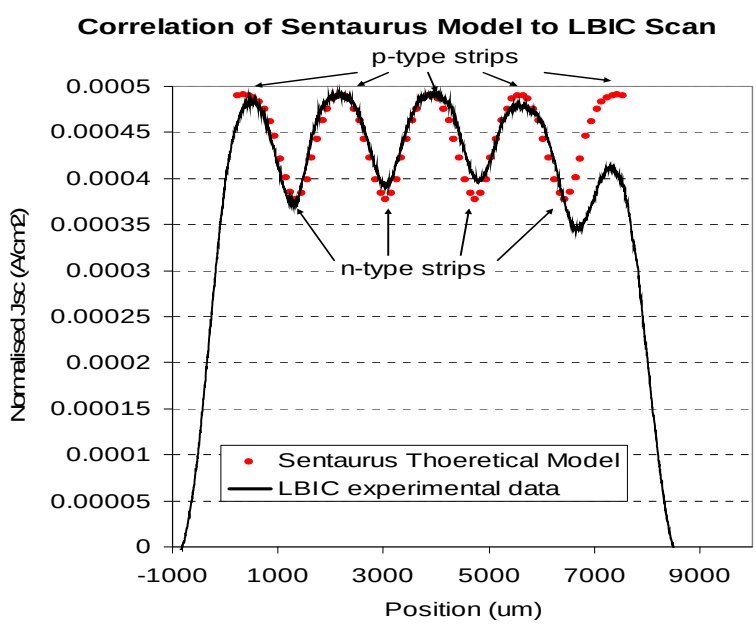


Figure 44. Comparison of the Sentaurus theoretical model to the experimental data from a LBIC scan.

To further investigate the device performance, the 680 mV cell was measured using light beam induced current (LBIC) and compared to the theoretical calculations from the

Sentaurus two-dimensional computer simulation as shown in Figure 44. The base wafer is n-type so carriers generated at the p-type strips with the collection junction are much more likely to be collected than carriers above the n-type strips, which have to diffuse laterally to a p-type strip. The high degree of correlation between the LBIC measurement and the Sentaurus model further confirms the validity of the determination of the front surface recombination velocity at 80 cm/s.

4.3.8 Efficiency Potential Of Interdigitated Back Heterojunction

Finally, Sentaurus modelling are used to estimate the efficiency potential of the IBC silicon heterojunction device. By using the present device dimensions, results from Section 4.3.6 (Figure 42) shows that an efficiency of 22.7% can be reached if front surface recombination velocity is reduced to 10 cm/s, a value consistent with our lifetime measurements of 2.2 milliseconds on amorphous passivated wafers. Additionally, by reducing n-strip width to 200 μm with fixed total sum of p- and n-strip based on Figure 36, J_{SC} can be increased and the efficiency will be enhanced to 23.6%. Also the total dimension of p- plus n- strips can be optimized, which is being studied. Since the junction is at back surface for IBC-SHJ cell, the thinner wafer thickness would give higher current due to less carrier recombination in the wafer, but light trapping will be required. Finally, the material properties of a-Si layers used in simulation is fit to the experiments, and might not be ideal. Further optimization to the a-Si properties could also improve the cell performance. In accounting all the above, an efficiency over 24% can be expected for IBC-SHJ solar cells.

4.3.9 Conclusions About Heterojunction IBC Cells

Interdigitated back contact solar cells using heterojunctions are a potentially low cost method for fabricating high efficiency solar cells. Present devices show a high voltage of 691 mV but low FFs limit performance. Devices show little shunting between the n and p regions. Further device performance improvements are expected through the use of thinner wafers, texturing and the optimization of the i-layer deposition profiles.

5 Diagnostics and Process Control

Process diagnostics are critical to evaluate and monitor the processing of thin film solar cells to maintain yield and avoid a large amount of off-spec production. To implement process diagnostics in real time requires both process and product monitoring as well as process control. Previous reports have contained our work on using contact wetting angle and X-ray diffraction as process monitors. During this period, graduate student Kapil Mukati completed his dissertation, "An alternative structure for next generation regulatory controllers and scale-up of $Cu(InGa)Se_2$ thin film co-evaporative physical vapor deposition process" awarded by the Department of Chemical Engineering for research conducted at IEC under the direction of Drs. Birkmire and Eser. It describes the process control needed to implement in-line real-time process diagnostics. A summary of that research is contained here. Further details may be found in his dissertation.

Process control systems have three key performance attributes: Set-point tracking (T) is ability to cause the process output to follow set-point changes rapidly and faithfully; Disturbance rejection (D) is the ability to counteract the effects of external disturbances; and Robustness (R) the ability to remain stable and perform well in the face of inevitable plant/model mismatch. A controller whose tuning constants are related directly to these performance attributes will have definite advantages over other controllers. However, the popular PID controller, even though simple, has an intrinsic structure that results in a complicated, hence non-transparent, relationship between its tuning parameters and the three controller performance attributes, limiting the controller's achievable performance and making tuning more complex than necessary. In order to overcome the weaknesses of the PID controller, we have developed an alternative regulatory controller [the Robustness, Tracking, Disturbance rejection, and overall Aggressiveness (RTDA) controller] having the following salient features: it requires precisely the same information that is required for tuning PID controllers; its tuning parameters are directly related to the three key controller attributes of R, T, and D [an auxiliary fourth parameter, influences the overall controller aggressiveness (A)]; all four tuning parameters are normalized to lie between 0 and 1; and the magnitude of a tuning parameter is related to performance aggressiveness, where the higher magnitudes signify conservative performance in the attribute of interest. In addition, the proposed predictive controller is not any more complicated to implement, in either software or hardware, than the PID controller.

In order to study how the choices of various RTDA controller parameter values jointly and individually affect closed-loop stability, a theoretical robust stability analysis is performed. The results of this analysis are subsequently used to develop systematic strategies for choosing the RTDA controller parameters that provide the best possible trade-off between robust stability and performance. The design and implementation of the RTDA controller in practice are illustrated experimentally using two processes: a lab-scale four-tank process with time delay and a pilot-scale physical vapor deposition process with nonlinear dynamics. These experiments demonstrate the RTDA controller's

improved performance over PID controllers. The RTDA control scheme is also extended to integrating and open-loop unstable processes.

A pilot-scale co-evaporative physical vapor deposition (PVD) process for manufacture of copper indium gallium diselenide ($Cu(InGa)Se_2$) thin films is chosen to validate the proposed RTDA controller experimentally, since robust control of film thickness and composition set-points for long deposition times cannot be achieved without effective base regulatory control. However, unlike film thickness and composition *set-points* that can be achieved with proper process *control*, achieving film thickness *uniformity* across large area substrates is a process *design* issue. To achieve good process performance, the process design issues are addressed first, and then the regulatory controller design is improved.

The work presented in Part II of this thesis is focused mainly on the evaporation source design. Such a study requires not only the detailed knowledge of the evaporation source temperature profile, but also accurate estimation of nozzle flow properties (effusion rates and vapor flux distribution). A three-dimensional first-principles electro-thermal model of the source is developed using the COMSOL Multiphysics™ finite-element method, and the Direct Simulation Monte Carlo (DSMC) technique is employed to predict accurately the nozzle flow properties for any given nozzle geometry and evaporant. These models are validated experimentally, and subsequently used to design evaporation sources that not only achieve the targeted film thickness uniformity, but also maximize the material utilization efficiency. Results of this work were reported in IEC's previous annual report.

6 Abstract

This report describes results achieved during phase V of a V-phase subcontract to develop and understand thin film solar cell technology associated to $CuInSe_2$ and related alloys, a-Si and its alloys and CdTe. This includes application of a-Si to c-Si wafer-type cells as well. Modules based on all these thin films are promising candidates to meet DOE long-range efficiency, reliability and manufacturing cost goals. The critical issues being addressed under this program are intended to provide the science and engineering basis for the development of viable commercial processes and to improve module performance. The generic research issues addressed are: 1) quantitative analysis of processing steps to provide information for efficient commercial scale equipment design and operation; 2) device characterization relating the device performance to materials properties and process conditions; 3) development of alloy materials with different bandgaps to allow improved device structures for stability and compatibility with module design; 4) development of improved window/heterojunction layers and contacts to improve device performance and reliability; and 5) evaluation of cell stability with respect to illumination, temperature and ambient and with respect to device structure and module encapsulation.

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