

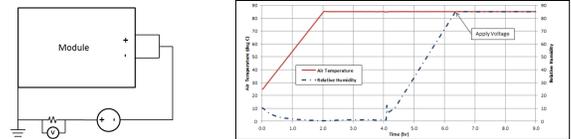
# 600 Hour Potential Induced Degradation (PID) Testing on Silicon, CIGS and HIT Modules

Nicholas Riedel\*, Larry Pratt\*, Erica Moss and Michael Yamasaki  
CFV Solar Test Laboratory, Inc., Albuquerque, NM

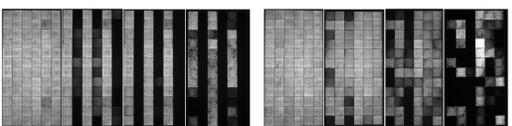
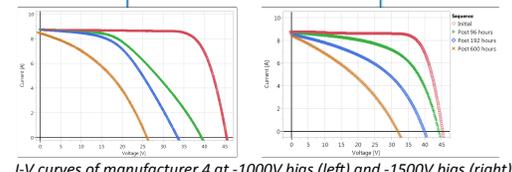
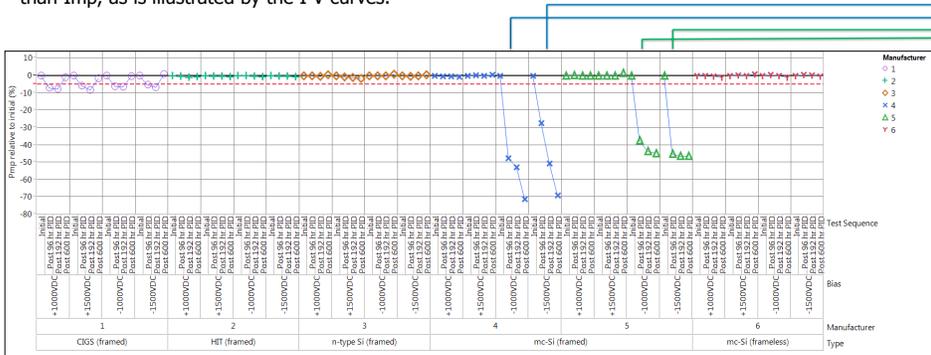
**Introduction** Potential induced degradation (PID) tests are performed on Silicon, CIGS and HIT modules in accordance with the IEC 62804 DTS, with slight modifications. Four PV modules from six manufacturers are tested (24 test samples) under biases of -1000 VDC, +1000 VDC, -1500 VDC or +1500 VDC for a total stress duration of 600 hours. The electrical bias represents a potential to ground. Module performance is characterized at STC in a h.a.l.m. class A+A+ flash solar simulator before PID testing, after 96 hours of PID tests, after 192 hours tests and after 600 hours of PID tests.

**Procedures** The PID tests were performed in an Espec environmental chamber. The PID test conditions were set as outlined in IEC 62804 DTS : 60° C air temperature, 85% relative humidity, voltage biases of +1000 V, -1000 V, +1500 V or -1500 V for a total test duration of 600 hours. The temperature and humidity were applied according to First Solar's guidelines for PID testing. The intention of this profile is to prevent condensation from forming on the module. The electrical bias was turned off at the end of the stress dwell (i.e. before temperature and humidity were ramped down). Leakage current was monitored throughout the test.

**Results** The Silicon modules from manufacturers 4 and 5, when placed in negative bias, are the only samples that show greater than 5% Pmp degradation. Both of these modules are framed multi-crystalline (mc-Si) with glass/polymeric backsheet construction. The final degradations of manufacturer 4 and 5 are nearly the same regardless of whether the bias is set to -1000V or -1500V. The degradations in Pmp are mostly due to degradation of Vmp rather than Imp, as is illustrated by the I-V curves.

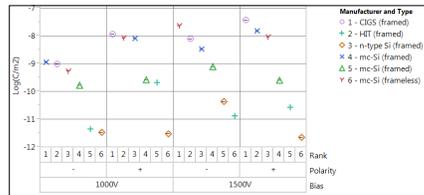


Wiring diagram of a test module in negative bias (left) and the temperature/humidity profile prescribed by First Solar's Testing Guidelines (Rev 4) used in this study (right)



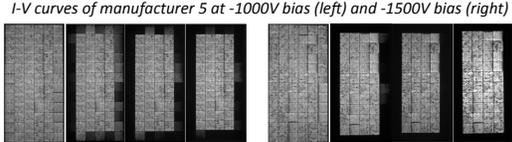
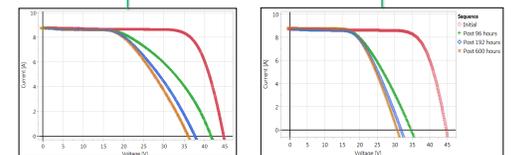
EL images of manufacturer 4 at -1000V bias (left) and -1500V bias (right). The initial, post 96 hour, post 192 hour, and final images are shown.

- The mc-Si modules with significant PID show dissimilar patterns in EL images.
- CIGS module 'Manufacturer 1' shows final Pmp losses of 0.8 and 1.6% at +1000V and +1500V bias, respectively. Note: These modules were only preconditioned before the initial and final characterizations.
- HIT module 'Manufacturer 2' shows 0.6% final Pmp loss, on average, regardless of bias or polarity.
- Manufacturer 3 shows 1.6% Pmp loss after 600 hours at +1500V. No losses observed at other test biases.
- Frameless mc-Si 'Manufacturer 6' shows 1% final Pmp loss at -1000V and +1000V.



Leakage current density (Coulombs/m²) measured during the initial 96 hour PID tests.

- All modules passed dry insulation (per IEC 61215 § 10.3) and wet leakage (per IEC 61215 § 10.15) before and after the 600 hour PID tests.
- The average leakage current of the test samples is 65% higher at 1500V than at 1000V bias.
- The leakage current density of Manufacturers 1, 4 and 6 is higher by two to three orders of magnitude than that of Manufacturers 2 and 3.



EL images of manufacturer 5 at -1000V bias (left) and -1500V bias (right). The initial, post 96 hour, post 192 hour, and final images are shown.

## Conclusions

- Two of the six manufacturers show critical power loss from PID, but only when in negative bias. Both of these modules are framed mc-Si with glass/polymeric backsheet construction.
- The range of final Pmp measured on the four samples of each manufacturer is less than 2% regardless of which electrical potential (1000 V vs 1500 V) was applied.
- Two manufacturers (no. 1 and 6) show considerable leakage current, but Pmp loss was less than 2%.

## References

- First Solar, "Testing Specifications and Guidelines for CdTe Modules (Rev 4)", 2014.
- P. Hacke, et al., "System Voltage Potential-Induced Degradation Mechanisms in PV Modules and Methods for Test" in 37th IEEE PVSC, 2011
- IEC 61215, Edition 2.0, 2005
- IEC 60904, Photovoltaic Devices, Parts 1-10
- IEC 62804, CDV Draft, Aug 2014