

Deep Level Transient Spectroscopy of CdTe/CdS Thin Film Solar Cells

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ABSTRACT

Knowledge and understanding of defect levels in thin film CdTe solar cells is limited and often difficult to obtain due to the complexities associated with these devices, such as grain boundaries and interdiffused/graded interfaces. In this paper results obtained using double boxcar and correlation deep level transient spectroscopy (DLTS) are presented, and the limitations of each technique as dictated by the polycrystalline nature of the CdTe/CdS heterostructure are discussed. Dark and illuminated J-V and dark C-V measurements were performed in order to monitor any changes in solar cell performance during the DLTS studies. The DLTS measurements were carried out in the 90-450°K temperature range, and the CdTe solar cells studied were exposed to CdCl₂ heat treatments in the range of 360-390°C. Hole traps with activation energies of 0.32, 0.45, and 0.73 eV were found in most of the samples studied. An electron trap with $E_A \approx E_C - 0.14$ eV was observed only in samples with low open-circuit voltages and fill factors, and is believed to be a performance-limiting defect. The effect of the above defect levels on device performance was modeled using AMPS.

1. Introduction

CdTe/CdS based thin film solar cells fabricated on float glass continue to be one of the most promising technologies for low cost terrestrial applications. Although much is known about the properties of the individual semiconductors, the CdTe/CdS heterojunction is often difficult to characterize due to the complexity associated with its polycrystalline nature and the creation of interdiffused regions such as Cd_{1-x}S_xTe, which lead to structural, compositional, and electronic variations along all directions. A critical process that has proven to considerably enhance the performance of CdTe/CdS solar cells is a heat treatment in the presence of CdCl₂. Although the details of the process itself may vary, its effect on the device performance is always beneficial regardless of the semiconductor deposition process. The performance enhancement is partly due to the recrystallization of both CdTe and CdS layers and the creation of an interdiffused region, at the CdTe/CdS interface. This paper summarizes our efforts to evaluate CdTe/CdS heterojunctions using deep level transient spectroscopy (DLTS). The devices were exposed to the CdCl₂ treatment in the temperature range of 360-390°C. The higher values are close to what is believed to be the most widely used range of optimum temperatures

of 390-410°C. Additional information on sample preparation can be found elsewhere [1].

2. Deep Level Transient Spectroscopy

Deep level transient spectroscopy was originally developed by Lang [2], and is a powerful technique widely used to identify deep levels in Schottky and p-n junction structures. Different modifications of DLTS have been developed to resolve issues such as the multi-exponential behavior of the capacitance transient [3,4]. Conventional (boxcar) DLTS has been used to study deep levels in CdTe/CdS heterojunctions, however, identification of the chemical nature of the impurities has not been done for many of the observed levels. In many instances Cd vacancy related defects have been assigned. For this work both the boxcar and correlation DLTS approaches were utilized for studying CdTe/CdS solar cells. More details on this can be found elsewhere [1].

3. Results and Discussion

3.1 Effect of Boxcar DLTS Experimental Conditions on Device Performance

It was observed, as illustrated in table 1, that the exposure of devices to the boxcar DLTS conditions i.e. temperature sweeps/electrical bias, had a significant impact on device performance. The devices shown in table 1 were exposed to several temperature cycles from 100-450°K and were held at a reverse bias of 1 volt. Additional experiments suggested that the observed changes were due to the combined effect of temperature cycling and reverse bias. The effect of exposing the samples to temperature cycling or electrical bias alone, did not significantly affect device performance.

Table 1. Effect of boxcar DLTS on solar cell performance.

	Initial	After 1 st run	After 2 nd run	After recovery
V _{OC} ; (V)	0.841	0.813	0.805	0.813
FF	0.684	0.641	0.638	0.665
Eff.; (%)	10.58	9.81	9.69	10.18

Figures 1 and 2 show CdTe/CdS DLTS spectra and the corresponding Arrhenius plots obtained using the boxcar method. This data set demonstrates another limitation of the boxcar approach: the difficulty resolving to resolve overlapping peaks. The peak associated with a defect level labeled H7 overlaps with the peak labeled H8, which is of

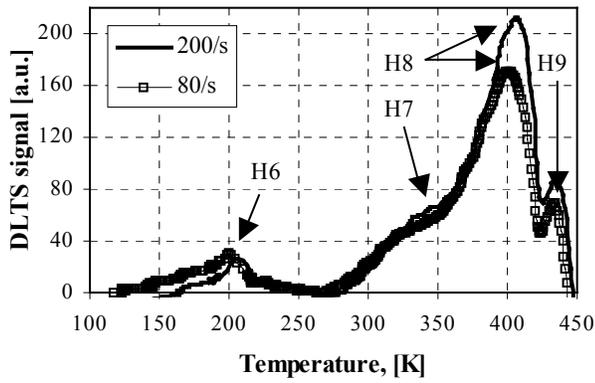


Fig 1. DLTS spectra obtained by the boxcar method.

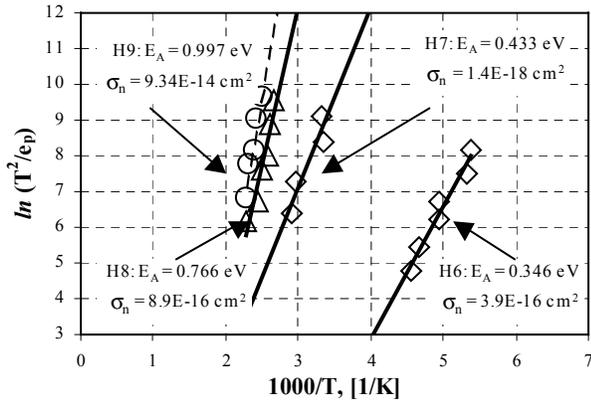


Fig 2. Arrhenius plots derived from the boxcar DLTS spectra shown in Fig. 1.

greater amplitude. It should be noted that even small uncertainties in the determination of the position of a DLTS peak could cause significant errors in determining the defect level parameters. In an effort to obtain more reliable data and improve the resolution of DLTS, the correlation DLTS approach was implemented.

3.2 Results of Correlation DLTS

The correlation DLTS method provides several advantages: (a) since the trap information is extracted directly from capacitance transients it is not necessary to thermally cycle the device several times, therefore not exposing the samples to excessive stresses that lead to changes in device performance; (b) the maximum temperature can be limited to lower levels than those required by the boxcar method, again limiting any performance changes during the measurement; (c) overlapping peaks such as those shown in fig. 1 can be more accurately resolved. Additional information on the correlation DLTS method can be found elsewhere [5].

Table 2 lists the solar cell performance of a set of devices and the deep levels obtained for each cell using the correlation DLTS technique. Missing concentration data are due to too high capacitances that lied outside our instrument's range. The primary difference between these samples is the presence of electron trap E1 in the first two.

The temperature for the CdCl₂ treatment of these samples was 360 and 370°C respectively. The electron trap is absent from the samples annealed at 380 and 390°C.

Table 2. Deep levels found in CdTe/CdS solar cells; CdCl₂ T_{ANNEALING}: 360, 370, 380, and 390°C from top to bottom.

Solar Cell Characteristics	Trap ID	E _A [eV]	□ _n [cm ²]	N _T [cm ⁻³]
V _{OC} = 0.818 V	E1	E _C - 0.14	9.0×10 ⁻¹⁸	3.5×10 ¹²
FF = 0.65	H7	E _V + 0.45	2.4×10 ⁻¹⁴	6.0×10 ¹²
Eff = 8.4 %	H8	E _V + 0.72	4.2×10 ⁻¹³	8.3×10 ¹³
V _{OC} = 0.827 V	E1	E _C - 0.14	1.9×10 ⁻¹⁸	4.8×10 ¹²
FF = 0.68	H4-6	E _V + 0.32	3.5×10 ⁻¹⁸	2.7×10 ¹²
Eff = 11.0 %	H8	E _V + 0.72	9.1×10 ⁻¹³	-
V _{OC} = 0.839 V	-	-	-	-
FF = 0.69	H4-6	E _V + 0.36	4.8×10 ⁻¹⁸	7.2×10 ¹²
Eff = 11.2 %	H8	E _V + 0.76	2.1×10 ⁻¹²	-
V _{OC} = 0.843 V	-	-	-	-
FF = 0.67	H4-6	E _V + 0.34	6.1×10 ⁻¹⁸	3.4×10 ¹²
Eff = 11.0 %	H8	E _V + 0.72	8.1×10 ⁻¹²	-

In order to determine the influence of the above traps on device performance, AMPS 1-D was utilized to calculate solar cell efficiency as a function of the concentration of these traps. Although hole traps H4-H8 affect the device performance, their influence is only significant at relatively high concentrations (>10¹⁴ cm⁻³). However, the presence of electron trap E1 results in lower efficiencies even at low concentrations (<10¹⁴ cm⁻³). The modeling results are summarized in fig. 3

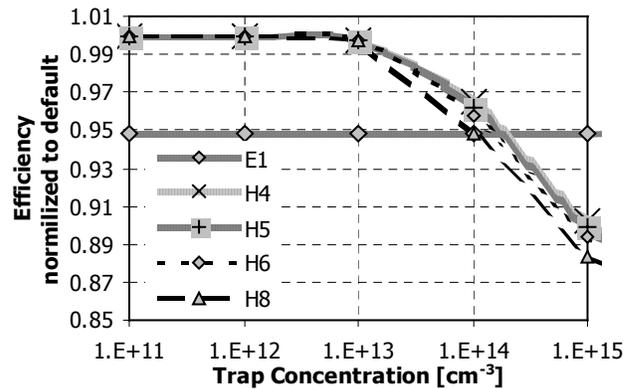


Fig 3. The influence of the traps listed in table 2 on device efficiency as determined using AMPS 1-D

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