

Progress in Apollo Technology through the Thin Film PV Partnership Program

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ABSTRACT

1. Introduction

BP Solar started its Thin Film PV Partnership Program (Contract number ZAK-7-17619-27) for the Apollo CdTe technology in May 1998. The program focused on three main tasks, semiconductor characterization and advancement, reliability and testing, and health, safety and environmental (HSE) aspects of CdTe. This paper will describe the advances made in the technology during the period of this subcontract.

2. CdS and CdTe characterization and improvements.

As described in previous papers (1,2,3), the Apollo technology uses chemical bath deposition for the formation of the CdS window layer and a proprietary electrochemical deposition technology for its CdTe absorber layer. At the start of the contract, the process had been defined using small area plates of 0.09m² (1square foot) in size. A small number of substrates were produced with areas as high as 0.6m². These were produced in order to prove concepts of large area CdTe electro-deposition but no photovoltaic device was obtained. While the 0.09m² devices had been characterized, the large area deposits needed extensive optimization. In addition to this, there was a strategic requirement for the ultimate plate size to reach approximately 1m² in order for the module power to compete with crystalline silicon technologies. The area scale up equated to an order of magnitude increase in the substrate size. In addition to this, an efficiency stretch was also required which would ultimately take the aperture area efficiency from 6% to more than 10%.

The approach for this significant undertaking focused on the substrate and semiconductor film and can be summarized as follows:

Tin oxide. Performed substrate analysis to determine loss mechanism that limits electroplating size.

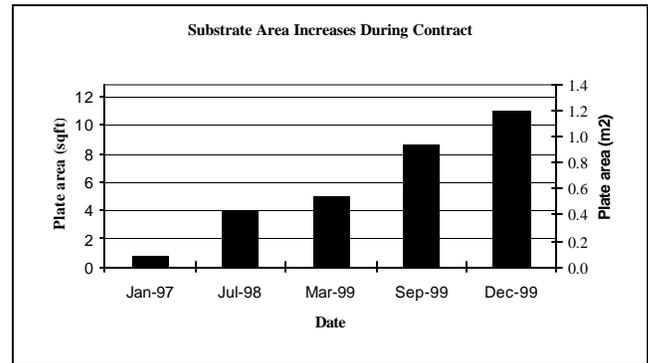
CdS. Undertook full characterization of CdS window layer and determined losses affecting efficiency.

CdTe. Performed full morphological characterization of film. Determined performance limitations of the absorber layer with respect to film thickness, grain boundary activity, and crystal structure.

3. Substrate area improvements.

The advances made in substrate size can be shown in figure 1.

Figure 1. Advances in Plate Size.



Significant increases have been made in the size of the substrate. In January 1997, the laboratory scale size was 0.09m². By July 1998, prototype plates were produced at just over 0.4m². This led to a further increase to 0.59m², which was the interim size used to demonstrate the efficiency stretch. September 1999 saw the breakthrough to 0.94m², which was the target size for the high power product. By December 1999, CdTe deposition was demonstrated on a 1.2m² substrate.

The main driving force was the optimization of the tin oxide resistivity. Resistivities of approximately 6 ohm/sq. were required to deposit CdTe on 0.61m wide substrates. However, optical transmission was compromised in order to obtain the resistivity. Typical optical transmission was in the order of 75%.

4. CdS Improvements.

CdS improvements, in particular the reduction of the CdS thickness, were made possible by electrical and optical characterization of the window layer. Collaboration with NREL to determine the electrical properties of the CdS film and IEC (UOD) for loss analysis in the CdS/CdTe layers help optimization. Table 1. shows CdS electrical properties as measured by NREL.

Table 1.

CdS Electrical Properties.	
Sheet resistance	7.00E+09 ohm/sq.
Resistivity	7.00E+04 ohm.cm.
Mobility	2.86 cm ² /V.s
Doping density	-3.12E+13 /cm ³

Of interest is the measured sheet resistance and doping density. Loss analysis by IEC on a 1000Å CdS layer showed more than 3mA.cm⁻² in current density could be gained by approximately halving the CdS thickness. An experimental investigation showed the model was correct. These results are shown in figure 2.

Figure 2.

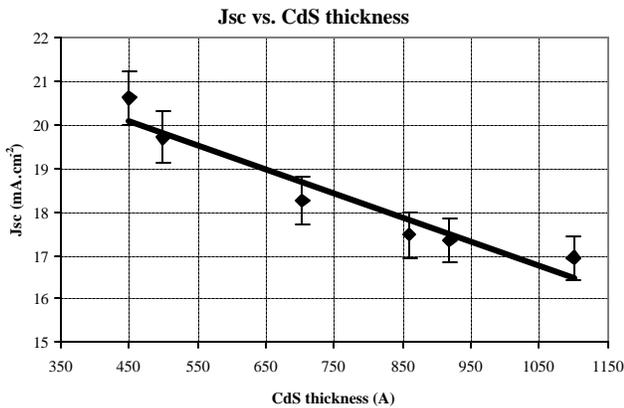


Figure 4. Efficiency Improvements

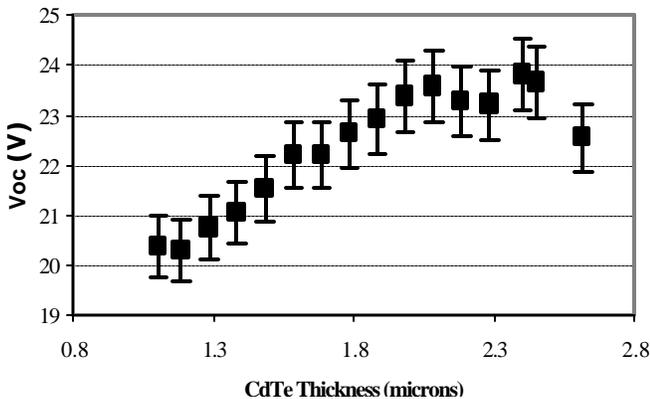
5. CdTe Improvements and Characterization

The focus of the work in this area can be categorized as the following:

- CdTe thickness optimization
- Grain orientation and crystallographic properties.
- Heat treatment optimization.
- Chloride doping profile intrinsic and impurity analysis.

Electrochemical deposition allows for very good control of CdTe thickness due to the slow deposition rate. Because of this, the effect of average CdTe thickness can be determined over a relatively small range (0.5 microns to 3 microns) with a high level of confidence. Figure 3 shows the effect of CdTe thickness on module Voc.

Figure 3. Effect of CdTe thickness on module Voc.



This study was important in determining the thickness limit for Apollo modules and, as a result the deposition time required to produce optimum devices.

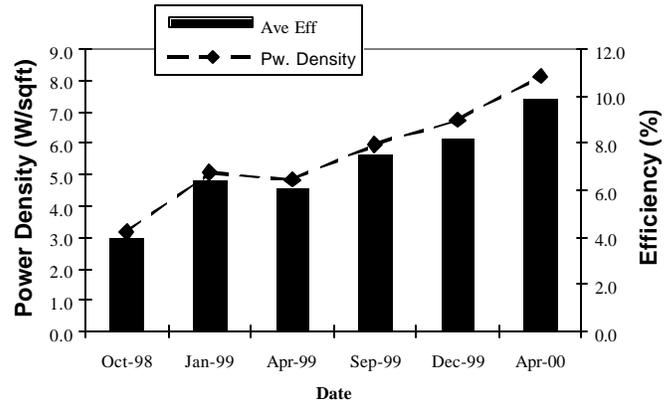
Collaborative work with IEC in the area of crystallographic research greatly increased the knowledge and understanding of the role of post deposition heat treatments for

electrodeposited CdTe. IEC used XRD (x ray diffraction) and GIXRD (glancing incidence x ray diffraction) to successfully characterize grain structure changes and resultant oxide species generation during heat treatment.

6. Improvement in Device Performance.

Significant improvements in device performance have occurred over the contract period. The figure 4 below illustrates these improvements.

Figure 4. Efficiency Improvements



The improvements in performance are a culmination of optimization of the window layer and absorber layers as described in the earlier sections of the paper. The results clearly demonstrate the versatility of the CdTe technology. Also, it has been shown to produce 10% efficient devices on areas of 0.94m². The grain structure of electrodeposited CdTe is very different to films formed by close space sublimation and other deposition techniques. These techniques produce very different grain structures. Equally, light stability has been demonstrated to be very good and the program allowed for 2 beta test sites to be established. The sites are located at the BP Solar facility, Fairfield CA and at the Western Area Power Administration building in Folsom, CA.

7. Summary

The Apollo team has made considerable progress during the period of contract ZAK-7-17619-27. A ten-fold increase in substrate area has been demonstrated as well as 10% efficient modules. Within the program, substrate, window layer, and absorber layer were all characterized and optimized. BP Solar would like to acknowledge technical contributions from the Institute of Energy Conversion (University of Delaware) and NREL.

8. References.

- [1] J M Woodcock et al, Proc. 12th EC PV Solar Energy Conf. (1994).
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- [3]] D W Cunningham, K Davies, L Grammond, J Healy, E Mopas, N O'Connor M Rubcich, M Sadeghi, D Skinner, T Trumbly, 28th IEEE PV Specialists Conference, September 2000. Anchorage, AK, pp13-18