

# CIS Manufacturing R&D Achievements and Challenges

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## ABSTRACT

Outstanding progress has been made in the initial commercialization of high performance CIS thin film photovoltaics. Market acceptance has been good for the ST line of products that include 5, 10, 20, 36 and 40-watt modules. All of these products are fabricated from large ~30x120 cm circuit plates that are used intact or cut into smaller circuit plates for the smaller products. Production rates are being continually increased and now exceed 500 kW per year. Electrical performance has proven to be quite predictable with aperture efficiencies over 10%. Prerequisites have been demonstrated for the continued systematic scale up of present processes. Further device and production R&D will lead to higher efficiencies, lower costs, and improved package designs. This paper will discuss Siemens Solar Industries's (SSI's) progress in commercialization of CIS-based thin-film PV and present efforts to scale equipment and processes to higher capacities, to improve device efficiencies and to improve module durability.

## 1. Introduction

The primary objectives of the SSI "Commercialization of CIS-Based Thin-Film PV" subcontract are to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing Siemens Solar's first CIS-based products. An additional mid- to longer-term objective is to advance CIS based thin-film technology, thereby assuring future product competitiveness, by improving module performance and reliability while reducing cost. These combined objectives are pursued to fabricate efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. The following briefly describes major CIS module process steps and highlights present and future R&D efforts.

## 2. SSI Process and Process R&D

The SSI CIS process starts with ordinary soda-lime window glass. This glass is cleaned then an SiO<sub>2</sub> barrier layer is deposited to control sodium diffusion and to improve adhesion between the CIS and the molybdenum (Mo) base electrode. The Mo base electrode is sputtered onto the SiO<sub>2</sub>. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Scale up efforts have included the implementation of a new sputtering system for increased capacity and research and development of a high throughput base electrode and precursor sputtering process. Poor P1 quality was initially an issue. Successful process R&D has included development of a Mo deposition process that consistently produces quality scribes using a process that

achieves high throughput with minimal complexity and minimal potential for process drift.

Copper, gallium and indium precursors to CIS formation are deposited on the Mo base electrode by sputtering. Precursors deposited in a new high throughput sputtering system have led to lower module performance than precursors deposited in our older sputtering system. Process R&D has decreased but not eliminated this difference; precursors deposited in the new sputtering system lead to efficiencies that are about 5 points lower than for precursors sputtered in our old system. Differences between the morphology of precursors for some deposition conditions have been identified with help from NREL [1].

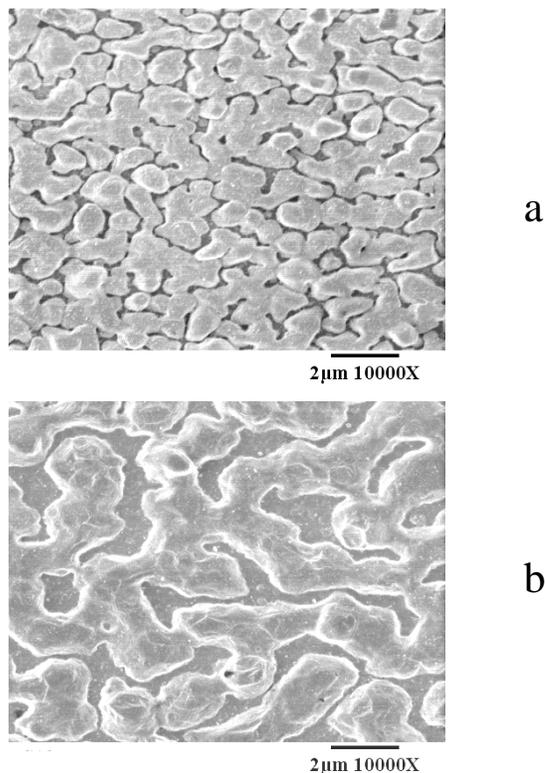


Figure 1. Precursor morphology;  
a – older equipment, b – new equipment

However, these differences in morphology do not lead to significant differences in the elemental profiles of the absorbers as determined by Auger depth profiling studies by NREL [2]. Precursor deposition determines the relative copper, gallium and indium content in the absorber as well as the overall thickness. Process R&D has demonstrated that increasing the absorber thickness relative to the baseline thickness by 125% and 150% leads to an efficiency improvement of 12% and 15% respectively. Additional

precursor deposition or absorber formation R&D will optimize this improvement and avoid poor adhesion associated with the thicker absorber layer.

CIS formation is accomplished by heating the precursors in H<sub>2</sub>Se and H<sub>2</sub>S to form the CIS absorber. SSI has found that materials of construction and physical reactor design influence absorber layer properties and cell performance [3]. Reactor process development has increased batch size and has been used to obtain good absorber properties in the new reactors. The issues addressed include obtaining consistent performance for all reactors, minimizing warping and minimizing poor CIS to Mo adhesion as a function of substrate location within the reactors. For the future, the need for increased capacity and improved performance dictates consideration of new reactor designs capable of processing larger circuit plates with further improvements in uniformity and more circuit plates in each batch.

Elemental profiles in the absorber are determined by the precursor deposition and absorber formation processes and to a large extent dictate electrical and mechanical properties. Improved CIS-to-Mo adhesion has been demonstrated for alterations in the absorber formation process, yielding a reduction in film peeling scrap. Absorber formation process changes have produced Voc and efficiency gains. This increase in Voc per cell led to decreasing the number of cells in a module from 50 cells to 42, a lower temperature coefficient for power and a decrease in active area lost to patterning. Improvements in the precursor deposition and absorber formation reaction processes continue to demonstrate decreased cost, increased capacity and improved efficiencies.

A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This "buffer layer" deposition process uses relatively low cost equipment and has proven to be very reliable. The amount of Cd in a module is miniscule; however, elimination of Cd from the factory is desirable. SSI has worked with NREL and the National CIS R&D Team to eliminate Cd and explore alternative buffer layers to mitigate transient effects [4, 5, 6].

A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact or "window layer" is made by CVD of ZnO. Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the P2 interconnect via thereby connecting the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) isolating adjacent cells is performed by mechanical scribing through the ZnO and CIS absorber. Process development for these processes is primarily directed toward increased capacity. Further, an approximately three-point improvement in efficiency is possible by decreasing pattern dimensions and decreasing pattern spacing.

EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a moisture barrier. Aluminum extrusions are used to build frames for the modules. In addition to providing a moisture seal, the combination of the TPAT backsheet and the offset between the circuit plate and

the frame provides electrical isolation from the frame. A glass/glass package with no TPAT back sheet is under development to decrease cost and further improve durability.

### 3. Status

Circuit plate production capacity has increased by more than an order of magnitude since the beginning of this subcontract while circuit and module efficiencies have steadily improved, as summarized in the following table. Initially lower performance when using new absorber formation reactors or new base electrode and precursor sputtering equipment is responsible for the temporarily lower efficiency last year. Process development at SSI and in conjunction with the National CIS R&D Team will lead to further process and capacity improvements [7].

Year	Module Production (kW)	Average Aperture Efficiency	
		Unlaminated Circuit	Laminated Module
97-98	15 *	10.8%	10.3%
98-99	68	11.2%	10.7%
99-00	294	11.6%	10.9%
00-01	482 **	10.9%	10.6%
Present		11.3%	10.9%

\* Estimated based on circuit plate data

\*\* Using estimations for Sept. 01

Figure 2. Production capacity and efficiency progress.

### 4. Summary & Outlook

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. Further device and production R&D can lead to higher efficiencies, lower cost, and even longer product lifetime. Prerequisites have been demonstrated for scale up of present processes. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service durability over even longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of further efficiency improvements for future products. SSI's thin-film CIS technology is poised to make very significant contributions to DOE/NREL/NCPV long-term goals - higher volume, lower cost commercial products.

### REFERENCES

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- 5 Alex Pudov, et. al. paper at this meeting
- 6 Kannan Ramanathan, et. al. paper at this meeting
- 7 Angus Rockett, et. al. paper at this meeting