

III-V Compound Photovoltaics on Si Using GeSi-Based Virtual Substrates

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ABSTRACT

This paper outlines the objectives and early results of a new program to explore and develop III-V solar cells grown on Si substrates using compositionally-graded GeSi buffer layers. Record material quality using this approach is described, and the potential for converting this to future opportunities for achieving new, high efficiency cell designs and advancing the science behind integrating high efficiency cell materials with diverse substrates is discussed.

1. Introduction and Program Objectives

The ability to epitaxially integrate optimum solar cell designs based on III-V compounds such as GaAs, InGaP, and advanced multi-bandgap structures, with cheap, abundant, large, strong and lightweight substrates such as Si would offer tremendous advantages in the power output/cost metric for photovoltaic system implementation in a variety of applications. As a result, the notion of III-V/Si integration has been explored for decades [1]. Unfortunately, the material perfection required to achieve the highest performance III-V solar cells had not been achievable due to the basic differences in lattice constant and other key structural properties between the III-V solar cell materials and the Si substrate wafer that generate lifetime-limiting defects (4% misfit between GaAs and Si). While significant efforts have been undertaken to mitigate these effects, until recently none had achieved the breakthrough necessary to allow photovoltaic quality III-V material to be achieved over any useful area.

This new NREL program will focus on exploiting the use of GeSi graded alloy buffers to accommodate lattice differences between epitaxial III-V layers and Si substrates. Our early work has shown this approach to have great potential for photovoltaics, breaking through a fundamental material quality barrier and resulting in record-high carrier lifetimes for GaAs on Si that can enable reproducibly high efficiency III-V cells grown on Si substrates for the first time [2]. The objectives of this new program are of two types. First is the demonstration that GeSi graded layers will provide a virtual Ge substrate with the mechanical, structural, and thermal properties of Si that can substitute for conventional Ge in PV technologies. This will be accomplished by fabricating “standard” III-V cell designs, both single (GaAs) and multijunction (InGaP/GaAs), on these novel substrates. The second type of objective is to investigate how to exploit the new lattice-engineering and bandgap-engineering possibilities opened up by the use of GeSi-based virtual substrates that essentially act as a

“tailored” lattice constant template for optimum, “metamorphic” III-V multijunction overgrowth on Si wafers. This opportunity is more easily seen in fig. 1. Accomplishing both objectives will generate new science focused on the general problem of integrating dissimilar materials, the results of which will help guide how to achieve next generations of optimum cell/substrate combinations while maintaining high efficiencies.

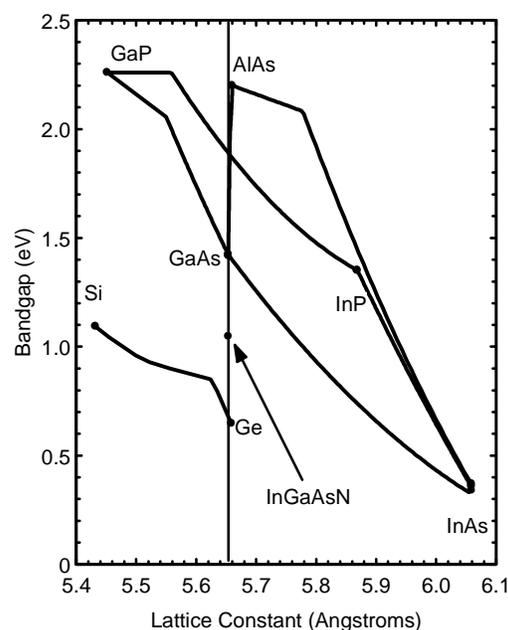


Fig. 1. Bandgap-lattice constant map for III-V/GeSi integration. Note the lattice matching possibilities for various III-AsPs and the use of GeSi bottom cells.

2. GaAs Material Quality Grown on GeSi/Si Substrates

Growth of device-quality GaAs onto Si requires control of both dislocation density and anti-phase domain (APD) formation. The effect of high dislocation density on material quality is well known, manifesting as lifetime killing defects and also providing potential paths for enhanced leakage currents. APDs are somewhat more insidious as they are a consequence of a mismatch in crystal symmetry, not lattice constant [3]. Hence, APDs are a known issue even for GaAs on Ge and their presence can dramatically increase shunt currents in solar cells. The first main challenge for GaAs grown on Si via GeSi graded buffers is to simultaneously maintain the low threading dislocation density (TDD), which we had already demonstrated for relaxed Ge layers grown on graded

GeSi/Si substrates, within the III-V overlayers while simultaneously inhibiting APD formation, even at the monolayer scale. Figure 2 shows our ability to accomplish

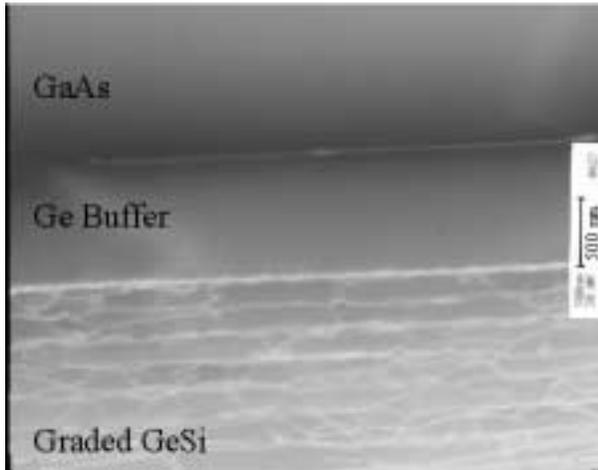


Fig. 2. XTEM image of an AlGaAs/GaAs cell grown on GeSi/Si. At this scale, no dislocations in the GaAs are evident, and even at high resolution we see no evidence of APD disorder at the GaAs/Ge interface.

both of these goals for structural quality. Lower resolution measurements (EPD and EBIC) confirm that the TDD within relaxed III-V overlayers are equivalent to that of the Ge cap with values in the range of $7-9 \times 10^5 \text{ cm}^{-2}$ as the lowest achieved to date, with no evidence of APD formation [2]. Figure 3 shows that the excellent structural quality

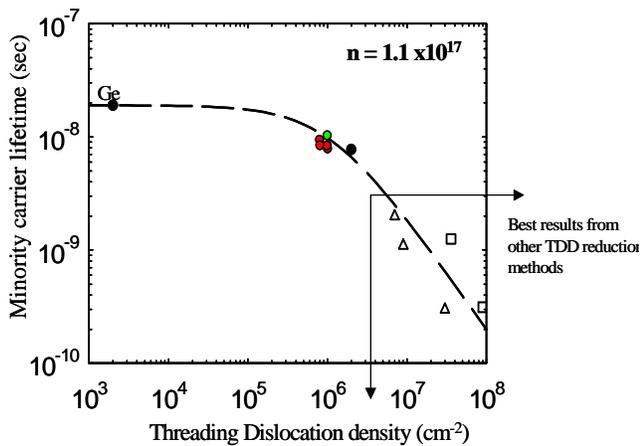


Fig. 3. Measured and calculated (lines) lifetime vs. TDD behavior for GaAs on Si. OSU data are the filled circles, showing reproducibly high lifetimes between 8-10.5 ns achieved using GeSi buffers. Other data are from earlier approaches using III-V buffers [2,4].

translates directly into high lifetimes, as obtained via growth of AlGaAs/GaAs double heterostructures of varying thickness in order to separate contributions from bulk and interface recombination using time resolved

photoluminescence. Room temperature lifetimes in excess of 10 ns have been achieved [2]. Prior record lifetimes have been in the range of 2-4 ns for GaAs on Si, for which the lattice mismatch was accommodated within III-V buffers of various kinds. Strain relaxation within the substrate wafer itself, prior to PV layer growth, is therefore believed to be an important advantage since the thermal budget and dislocation nucleation and flow mechanics are handled prior to any III-V epitaxy. Hence, this approach is truly that of an alternative substrate. Moreover, the fact that our lifetime data correlates closely with theoretical expectations (fig. 3) indicates that it is only the residual TDD of the substrate cap layer that controls lifetime below the knee (which is determined by the balance between dislocation-limited and non-dislocation-limited recombination processes). This indicates that our approach does not introduce other lifetime-limiting defects, in contrast with prior work where lifetime and TDD values were often found not to correlate.

Preliminary single junction GaAs cells are already very encouraging [5]. AM0 tests reveal Voc values in excess of 1 V for a large number of cells, with Jsc and QE values matching that of identical control cells grown on both GaAs and Ge substrate controls. All past attempts have never exceeded 940 mV AM0, and Voc values are typically $\sim 900 \text{ mV}$ [4]. The large improvement in Voc results from the high lifetime leading to reduction in leakage current. AM0 efficiencies in excess of 17% have recently been verified, being limited by the large, 11% metal coverage for these basic cells. This has been verified by comparing with cells grown on Ge and GaAs substrates that display the same Jsc, QE and Voc values. The only parameter observed to be impacted by the substrate at this point is fill factor, which is 0.805 for our best cell to date. Hence, we project that even at this early point of development, 19% AM0 and $> 22\%$ AM1.5 GaAs/Si cells are feasible by using a more appropriate contact grid. Immediate plans are to generate dual junction InGaP/GaAs cells on GeSi, which will lead into the core of our program to exploit the GeSi buffer for advanced cell concepts.

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