

Photovoltaic Manufacturing Technology Report, Phase 1

Final Technical Report
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MASTER

On September 16, 1991 the Solar Energy Institute was designated a national laboratory, and its name was changed to the National Renewable Energy Laboratory.

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1.0 EXECUTIVE SUMMARY

Spectrolab is pleased to participate in Phase I of the Department of Energy's Photovoltaic Manufacturing Technology program. This report addresses the tasks outlined in SERI's letter of solicitation RC-0-10057. Spectrolab is eager to participate in cooperative activities with DOE and SERI to work towards the common goal of making photovoltaics a more affordable energy source as set forth as the goal of the PVMat program.

Hughes Aircraft Company owns and operates Spectrolab to provide high quality space solar cells and panels to the satellite industry. Spectrolab has successfully engaged in the design, development, fabrication and test of photovoltaic energy conversion systems since 1957. Our experience in this area encompasses over 370 different satellite programs, including three GaAs based flight programs, on which production solar cells have been flown. The bulk of present satellite power systems is serviced with silicon technology. However, increased power requirements for spacecraft have required us to develop GaAs and GaAs/Ge cells with conversion efficiencies substantially higher than silicon. This mission has enabled Spectrolab to develop versatile solar cell and module processing techniques and innovative cell and module designs suitable for low cost terrestrial PV application also.

1.1 CURRENT CAPABILITIES

Spectrolab's silicon product line encompasses solar cells from 64 to 200 microns thickness in sizes from 2 cm x 2 cm to 8 cm x 8 cm, the largest cell that can be produced from a four inch diameter wafer. Some cells are texture surface etched to provide the highest conversion efficiency while others have a

planar surface. Details of the process flow are discussed as part of Task 1. In addition, Spectrolab manufactures large area wrapthrough solar cells with coplanar back contacts for several flight programs including cells for the Space Station Freedom solar array.

Spectrolab is the only United States manufacturer of both GaAs and Silicon solar cells and panels. This capability has broadened Spectrolab's solar cell technology base in understanding the specific requirements associated with solar cells in system applications.

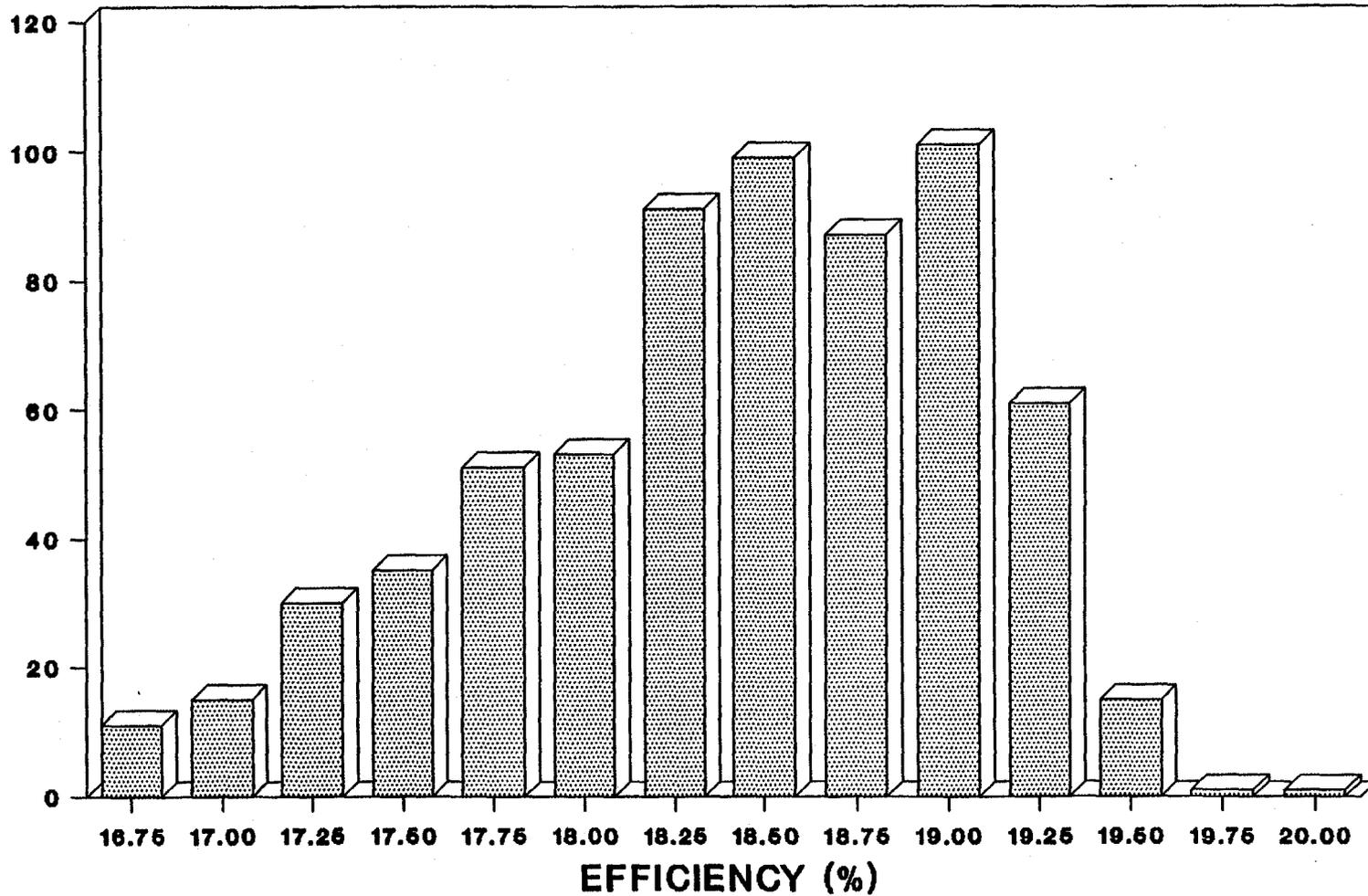
A partnership between Spectrolab and Microwave Products division provides the facilities for a state-of-the-art GaAs manufacturing facility. At MPD, over 3000 sq ft of Class 100 clean room area have been allocated for up to 10 production reactors. Currently this area houses two MOCVD machines for research and development and a CVD Equipment production reactor. Each of these reactors has produced GaAs solar cells with an AM0, 1 sun efficiency in excess of 20% (or 23% 1 sun AM1.5).

In addition to the MOCVD facility, Spectrolab commissioned in 1985, a 4,000 sq ft GaAs processing site to accommodate the production of up to 400,000 sq cm of GaAs or GaAs/Ge solar cells per shift per year. This represents a capability of about 3MW of GaAs concentrator solar cells assuming 300X concentration and a solar cell efficiency of 25% AM1.5D.

Approximately 10,000 2 cm x 4 cm GaAs and GaAs/Ge solar cells have been processed in this area over the last 3 years. Figure 1.1 is a distribution of 650 GaAs/Ge solar cells recently produced in this facility.

UoSAT EFFICIENCY DISTRIBUTION

NUMBER OF CELLS



651 CELLS > 16.5% (18.27% AVG)

Figure 1.1 ELECTRICAL DISTRIBUTION OF GaAs/Ge CELLS

AM0 28°C

1.2 PROPOSED TECHNOLOGY FOR IMPROVED PERFORMANCE AND COST

Spectrolab believes that the DOE cost goals can be met using silicon concentrator cells, high efficiency GaAs concentrator cells and mechanically stacked multijunction cells. The main features of these cells will be summarized here, further details can be found within this report.

Silicon Concentrator Cells

The use of silicon concentrator cells is a viable solution to meeting the DOE short term cost goal of \$.12 kWh with today's technology. These solar cells also have great potential to meet the long term goal of \$.06 kWh. Spectrolab is currently working under SANDIA contract no. 54-2191A to develop the manufacturing technology for a silicon concentrator cell suitable for the SBM3 module operating at 200X to 300X AM1.5D. We expect to produce a production ready 20% 250X AM1.5D Si concentrator cell during 1991.

GaAs Technology Improvements

Improvements in GaAs MOCVD growth, automated processing and innovative cell designs are needed to meet the cost goals using gallium arsenide cells. Currently, material costs are a major component of the GaAs cell cost. Improvements in MOCVD growth technology are crucial to reduce the cell cost. Spectrolab, in conjunction with a large MOCVD equipment manufacturer is developing an improved design MOCVD reactor which is expected to be on line in 1992. This reactor will improve the uniformity and quality of GaAs layers. It will also reduce the cost of the growth through better utilization of source gases and reduced cycle time.

GaAs Concentrator Cells on Ge Substrates

We believe that elimination of the GaAs wafer will reduce the cost of GaAs solar cells. Currently, substrate cost is a

significant cost component of the GaAs and GaAs/Ge solar cell. Figures 1.2 and 1.3 show the historical cost of GaAs and Ge substrates over the last 2 - 3 years. Particularly noticeable from Figure 1.3 is the significant drop in Ge wafer cost during the last 2 years. Bulk substrate costs can be reduced to \$.5/cm² if 4 inch diameter germanium wafer can be used instead of GaAs.

The cost and production volume of GaAs/Ge concentrator cells as a function of time and technology development are plotted in Figure 1.4. This figure assumes the production of 28% 300X AM1.5D GaAs/Ge concentrator cells. Clearly both of the goals described, improved GaAs MOCVD growth technology and germanium wafer technology, contribute significantly to reducing the final cost of the solar cell. Spectrolab proposes that DOE initiate MANTECH programs addressing both of these issues.

Multijunction Concentrator Solar Cells

We believe that very high efficiency mechanically stacked multijunction cells may be fabricated cost effectively. This technique has the advantage that it allows each cell to be independently optimized and allows the choice of many more cell combinations since current matching is no longer required. Modeling of this cell using a GaAs top cell and a Ge bottom cell gives an estimated 33% AM1.5D efficiency at 300X. This cell can be assembled using hybrid technology already demonstrated at Spectrolab.

1.3 DEVELOPMENT SCHEDULE

A multifaceted approach is required to attain the goals described above. Figure 1.5 shows Spectrolab's technology roadmap for terrestrial photovoltaics production. Mantech

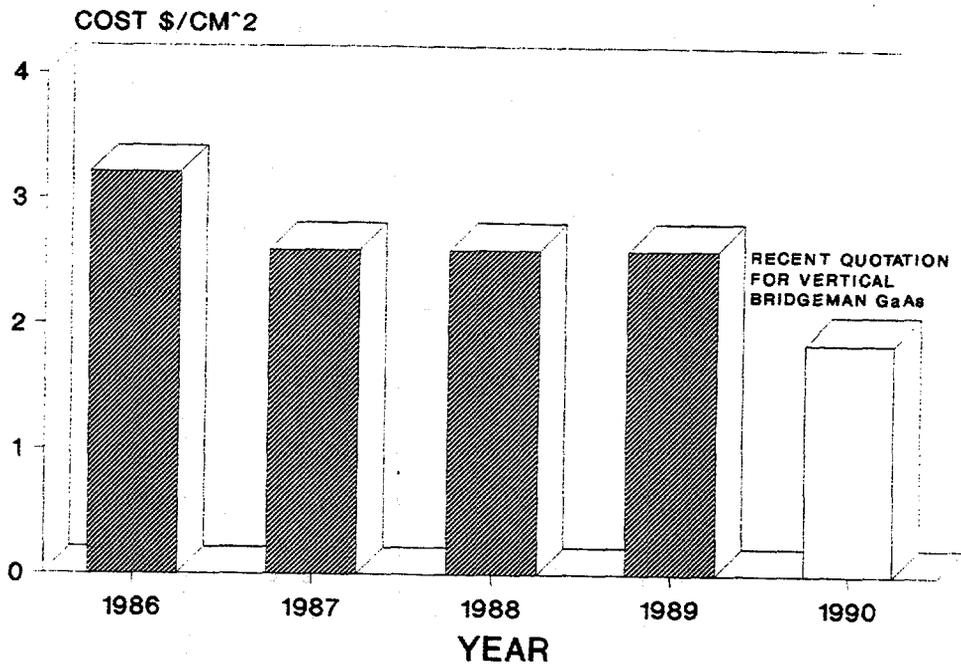


Figure 1.2 RECENT PRICE HISTORY OF 12 mil THICK GaAs SUBSTRATES IN HIGH QUANTITY

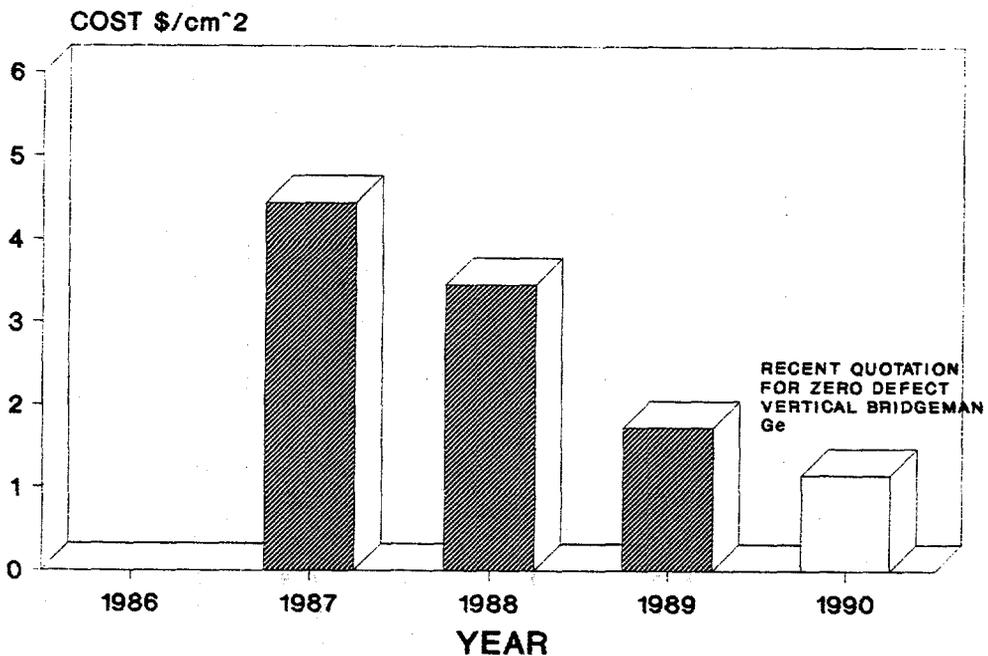


Figure 1.3 RECENT PRICE HISTORY OF 8 mil THICK Ge SUBSTRATES IN HIGH QUANTITY

GaAs/Ge CONCENTRATOR CELLS

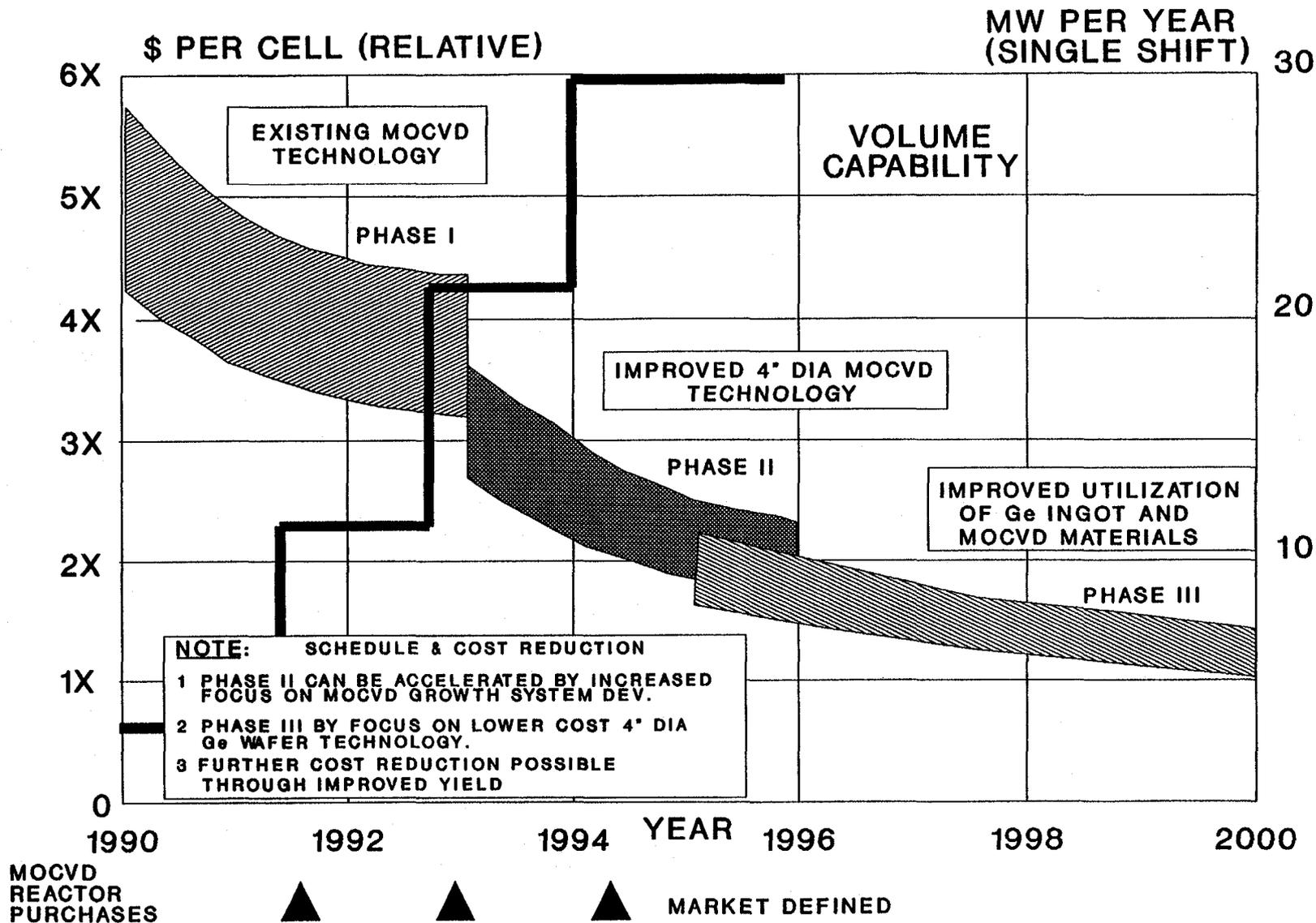


Figure 1.4 COST AND PRODUCTION VOLUME OF GaAs/Ge CONCENTRATOR CELLS

programs for GaAs/Ge concentrator cells, 4 inch Ge development, mechanically stacked multijunction concentrator cells and Si concentrator cells are shown on the roadmap.

The MANTECH programs specified on the roadmap will bring us closer to making photovoltaic concentrator power generation a viable economic energy source. The goals identified by DOE of \$.12/kWh in the near term and \$.06/kWh by the year 2000 appear to be reasonable planning targets.

2.0 TASK 1: CURRENT CELL AND PROCESSING CAPABILITIES

Spectrolab has developed versatile silicon and GaAs manufacturing lines for fabricating a variety of solar cell types. Silicon solar cell manufacturing is performed on a semiautomated four inch production line. Most process operations have been mechanized to achieve critical process control.

Work Center Teams have been established at Spectrolab to allow for decentralized decision making in manufacturing and product design. The teams use statistical process control for process, labor content, cost and yield control. This method of statistical control is a factor in routinely achieving high yield, high volume manufacturing. The concept and practice of teaming is extended to quickly solving performance and manufacturing problems and is instrumental in designing producible devices.

This section will review Spectrolab's capabilities in Silicon and GaAs processing. Silicon and GaAs cell designs and performance characteristics will also be described.

2.1 SILICON CELL DESCRIPTION

Spectrolab manufactures a complete product line of silicon cells for space applications. Table 2.1 lists the performance characteristics of each cell type. This section briefly describes typical cell designs and performances.

2.1.1 Planar Cell (K4)

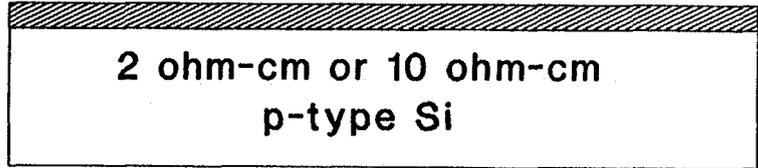
A cross-section of a planar silicon solar cell (designated as K4) is shown in Figure 2.1. The substrate is nominally 10 ohm-cm or 2 ohm-cm p-type silicon and between 65 and 200 microns thick. A .15 micron deep n+ junction is diffused into the front surface to form the n-p junction. The front metallization grid is optimized to minimize series resistance and maximize the efficiency of the solar cell. Cells with this configuration have a typical efficiency of 12.3% (AMO, 28°C) or approx. 15% (AM1.5, 28°C) for 10 ohm-cm and 13.3% (AMO, 28°C) or 16% (AM1.5, 28°C) for 2 ohm-cm substrates. Full cell characteristics are summarized in Table 2.1.

2.1.2 Textured Cell (K5)

Textured surfaces are added to the basic n on p configuration to form the textured, K5, cell. This feature improves the final efficiency and the radiation hardness of the cell by improving light scattering and hence increasing the current density. The full cell characteristics are summarized in Table 2.1.

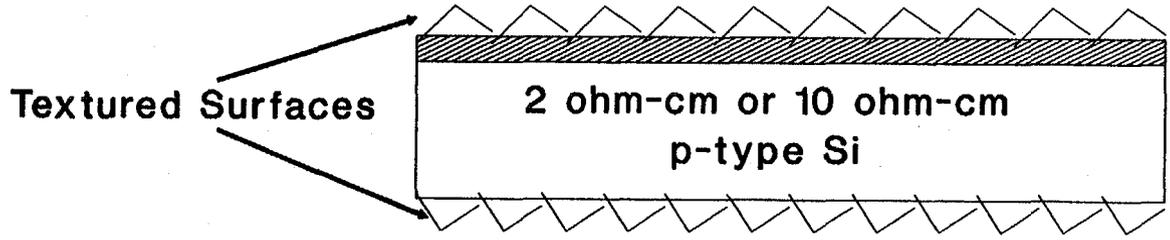
2.1.3 Back Surface Field (BSF) Cell (K6 and K7)

Spectrolab manufactures silicon cells that use a back surface field to increase the cell efficiency. Cross-sections of a planar BSF cell (K6), and a textured BSF cell (K7) are shown in Figure 2.2. The addition of a back surface field improves cell efficiency from 12.3% to 14.6% (AMO, 28°C) for a 200 micron thick 10 ohm-cm substrate. Thin, 62 micron, cells have been fabricated with efficiencies of 13.7%. Full cell characteristics are summarized in Table 2.1.



n Diffused Region

K4 Solar Cell



n Diffused Region

Textured Surfaces

K5 Solar Cell

Figure 2.1 CROSS-SECTION STANDARD K4 AND K5 SILICON CELLS

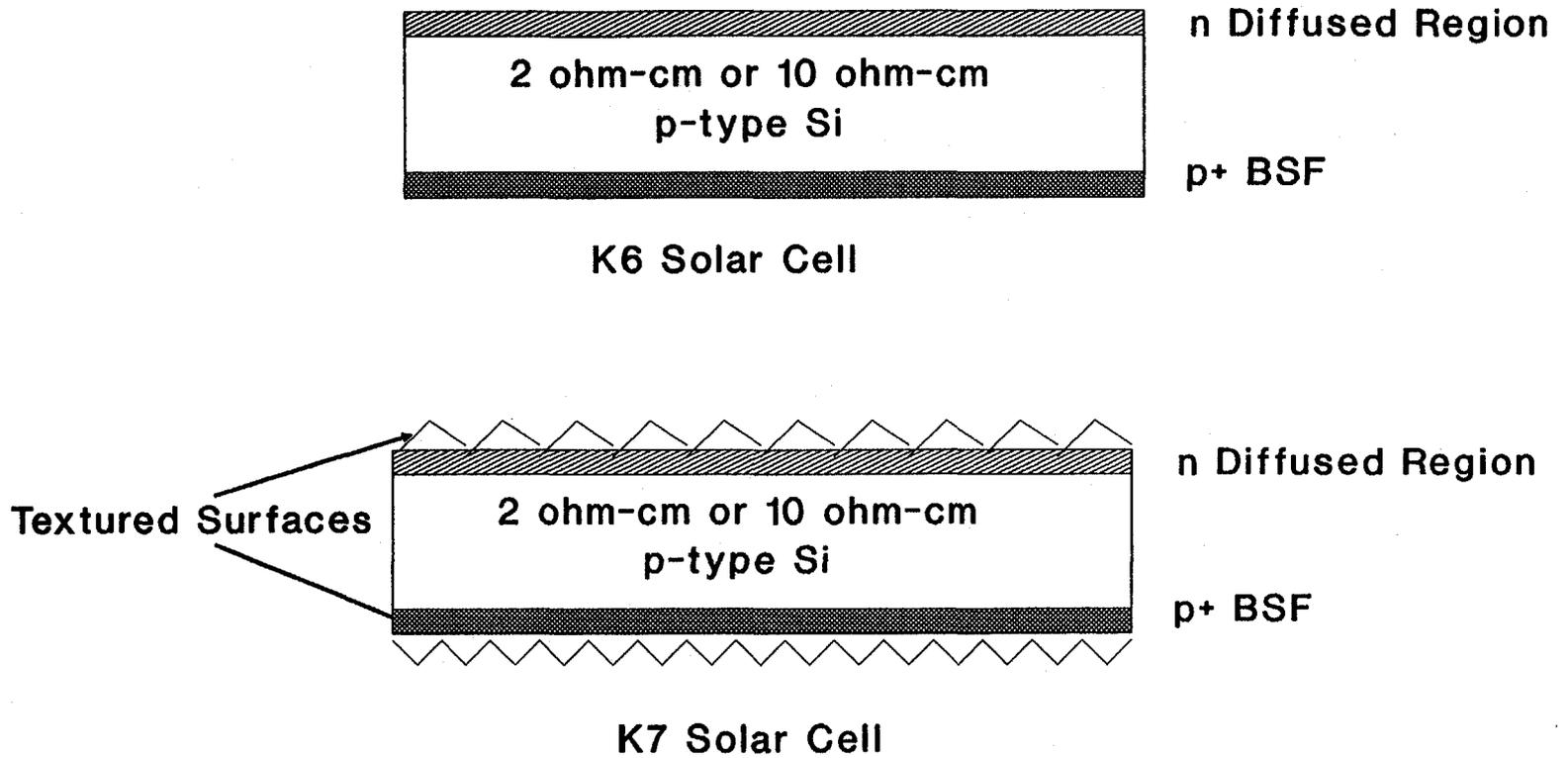


Figure 2.2 CROSS-SECTION STANDARD K6 AND K7 SILICON CELLS

Table 2.1 PERFORMANCE CHARACTERISTICS OF SILICON CELLS

SPECTROLAB - TYPICAL CELL PERFORMANCE								
CELL TYPE	K7700 SILICON	K7700 SILICON	K6700 SILICON	K6700 SILICON	K4700 SILICON	K4700 SILICON	K6700 SILICON	GaAsGe
STANDARD/SPECIAL PRODUCT	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD	FREEDOM	STANDARD
RESISTIVITY - OHM-CM	10	10	10	10	10	2	10	0.1
SCULPTURED FRONT SURFACE	YES	YES	YES	YES	NO	NO	YES	NO
BACK SURFACE FIELD TYPE	ALUM	BORON	ALUM	BORON	NO	NO	BORON	N/A
BACK SURFACE REFLECTOR	YES	YES						
THICKNESS - MICRONS	200	62	200	62	200	200	200	200
CONTACT TYPE - TiPdAg - SOLD/WELD	TOP/BOT	TOP/BOT	TOP/BOT	TOP/BOT	TOP/BOT	TOP/BOT	WRAPTHRU	TOP/BOT
Isc - BARE MILLIAMPS/CM SQ	46.0	42.5	42.5	39.0	38.5	39.2	41.9	30.20
Imp - BARE MILLIAMPS/CM SQ	41.6	40.2	39.6	37.8	36.6	36.8	38.4	28.70
Vmp - BARE VOLTS	0.500	0.490	0.500	0.490	0.454	0.490	0.500	0.870
Voc - BARE VOLTS	0.600	0.600	0.605	0.605	0.545	0.585	0.618	1.015
Pmp - BARE MILLIWATTS/CM SQ	20.8	19.7	19.8	18.5	16.6	18.0	19.2	24.80
EFFICIENCY AMO(135.3mW/CM SQ),28C	15.4%	14.6%	14.6%	13.7%	12.3%	13.3%	14.2%	18.3%
CURVE FILL FACTOR	0.75	0.77	0.77	0.78	0.79	0.79	0.74	0.81
MASS - MILLIGRAMS/CM SQ	55.0	24.0	55.0	24.0	55.0	55.0	55.0	118.0
ALPHA (CMX)	0.91	0.91	0.79	0.75	0.71	0.71	0.65	0.89
ALPHA (FS)	0.89	0.89	0.77	0.73	0.69	0.69	0.63	0.87
EMISSIVITY, NORMAL (CMX)	0.85	0.85	0.85	0.85	0.85	0.85	0.85	0.85
EMISSIVITY, NORMAL (FS)	0.81	0.81	0.81	0.81	0.81	0.81	0.81	0.81
TEMP COEFF - Isc MICROAMPS/CM SQ/	27.5	27.5	22.0	22.0	20.0	20.0	20.00	20
TEMP COEFF - Vmp - mV/C	-2.15	-2.15	-2.15	-2.15	-2.33	-2.20	-2.15	-1.80
TEMP COEFF - Voc - mV/C	-2.00	-2.04	-1.96	-1.96	-2.20	-2.08	-1.96	-1.80

The K7 cell incorporates both a back surface field and textured surfaces. These additions serve to increase the efficiency of a cell on a 200 micron thick 10 ohm-cm substrate to 15.4% (AMO, 28°C). A sixty-two micron thick cell has a nominal efficiency of 14.6% (AMO, 28°C).

2.1.4 Specialty Cells

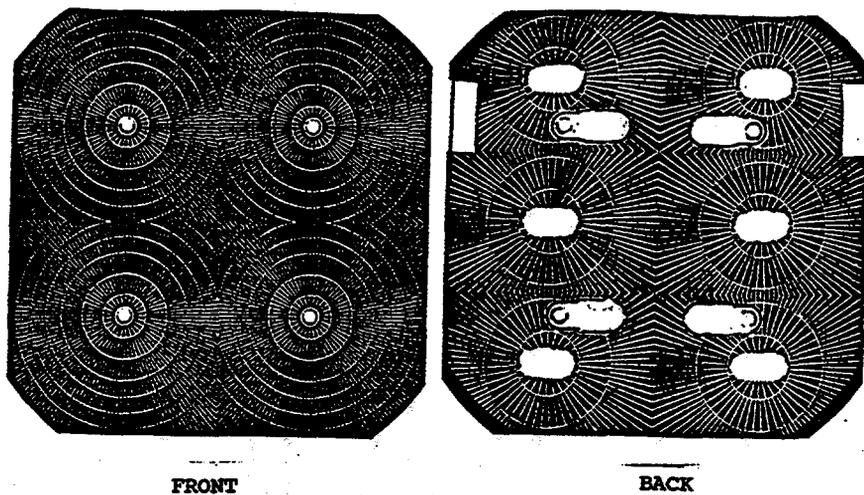
Coplanar Contact Cells

Solar cells with coplanar contacts were developed in response to customer desires to simplify solar cell interconnection. Solar cells with coplanar contacts have both the n and p contacts on the same side of the wafer.

Spectrolab has manufactured both wrapthrough and wraparound cells. In wrapthrough cells, holes are laser scribed in the wafer to form vias through which the n contact can be brought to the back. Contacts for wraparound cells are wrapped around the edge of the cell. Pictures of both type of cell are shown in Figure 2.3. A cross-section of the hole edge region is shown in Figure 2.4. LPCVD deposited SiO₂ insulates the hole edge from the n contact. Away from the wrapthrough region this cell is the same as the K6 cell described earlier. The Nominal efficiencies of 14.2% (AMO, 28°C) are obtained for 200 micron thick 10 ohm-cm planar BSF cells up to 8 cm x 8 cm in size.

Terrestrial Concentrator Cells

Spectrolab is currently working under SANDIA Contract No. 54-2191A to develop the manufacturing technology for a silicon concentrator cell suitable for the SBM3 module operating at 200X to 300X. A cross-section of this cell is shown in Figure 2.5. Prototype cells are being fabricated in a production environment and are expected in mid 1991. We anticipate that these cells will have a 20% 200x AM1.5D efficiency.



FRONT

BACK

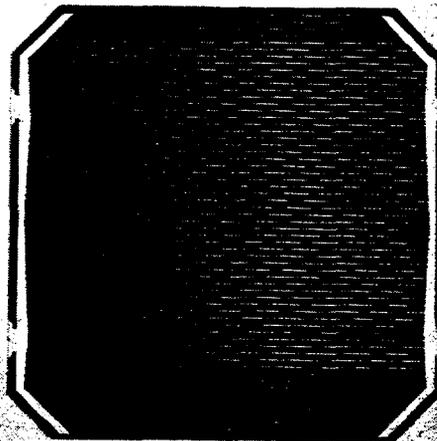
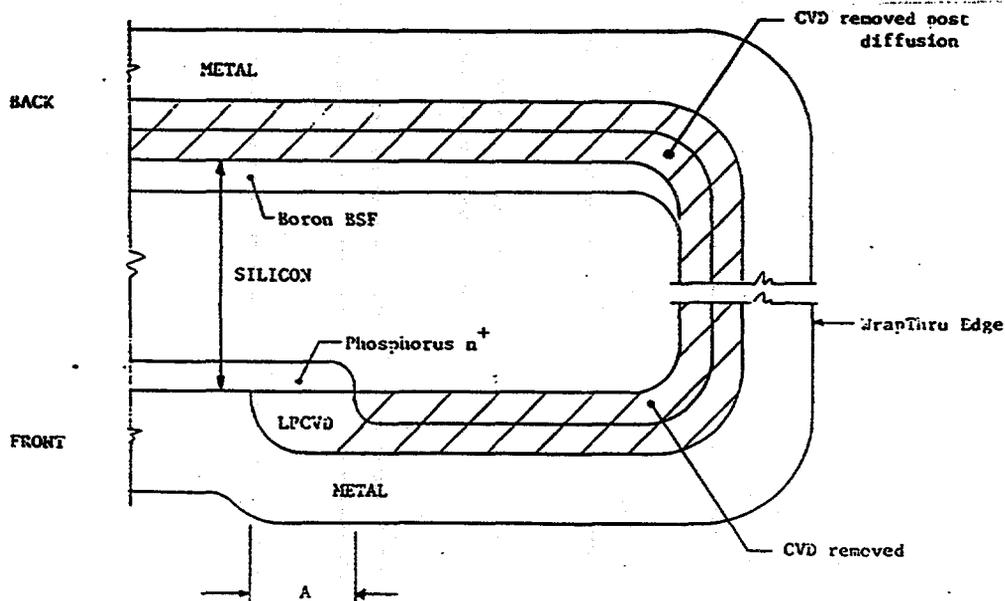


Figure 2.3 CELL DESIGN WRAPTHROUGH AND WRAPAROUND CELLS



'A' indicates area of junction buried by LPCVD after CVD mask is removed

Scale: all scales arbitrary

Figure 2.4 CROSS-SECTION OF HOLE EDGE

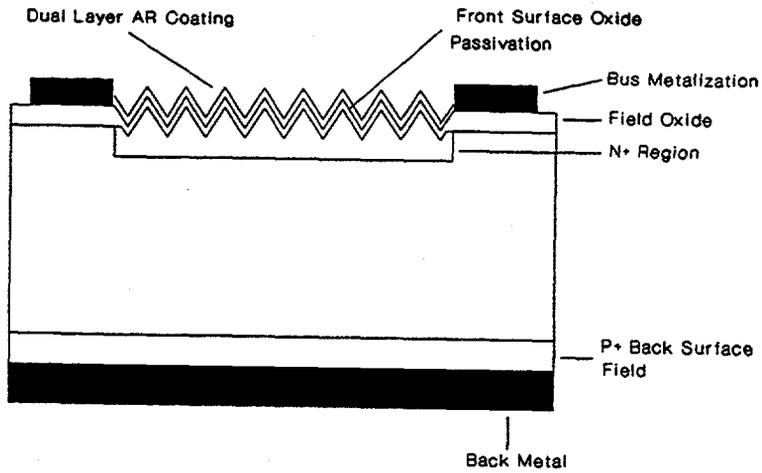


Figure 2.5 CROSS-SECTIONAL DIAGRAM OF BASIC CELL STRUCTURE

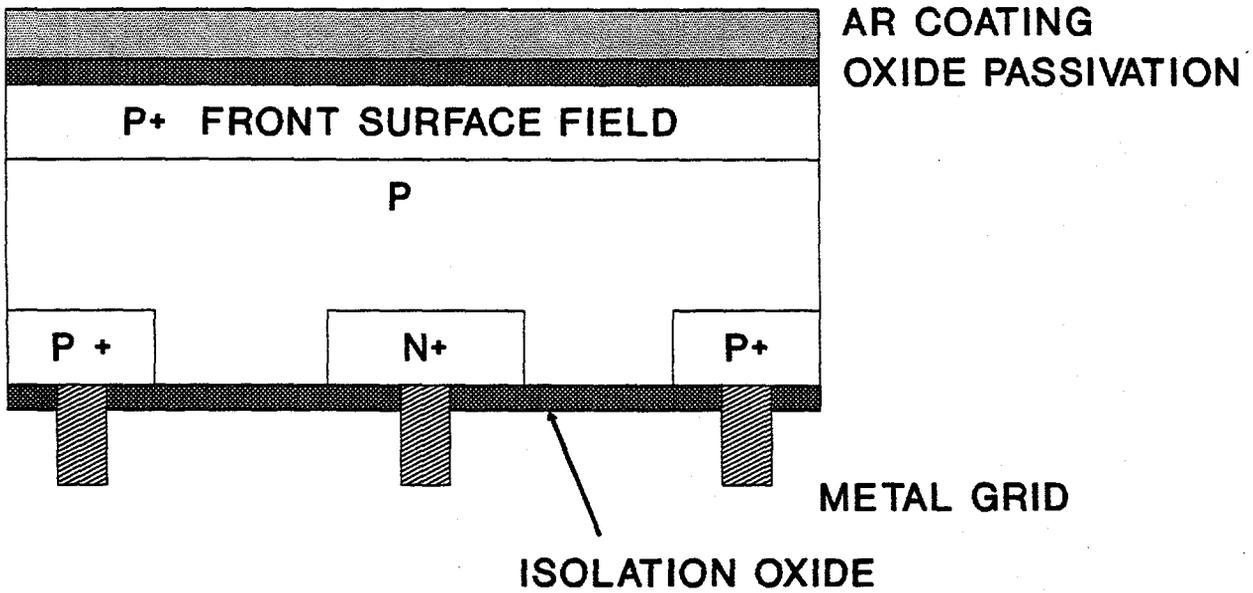


Figure 2.6 CROSS-SECTION IBC CELL

Interdigitated Back Contact Cells (IBC)

Spectrolab has fabricated 2 cm x 6 cm silicon cells for space applications with interdigitated back contacts. A cross-section of the cell structure is shown in Figure 2.6. The device structure uses a P+ or N+ front surface field for minority carrier reflection from the front surface. The back of the device consisted of alternating N+ and P+ regions separated from one another by oxides which also serve to passivate the undoped surfaces between the collector regions. Production methodology has been applied in the fabrication of 900 cells.

2.2 STANDARD SILICON SOLAR CELL PROCESSING

The Spectrolab facilities specially designed for solar cell manufacturing occupy approximately 37,690 square ft. This modern mechanized facility with a single shift capability of 5000 wafers/week is divided into eleven operational manufacturing modules:

- 1) Surface Preparation
- 2) Diffusion
- 3) Back Surface Field Formation and Annealing
- 4) Oxidation
- 5) Wet Chemical Etching
- 6) Evaporation (Metal and Antireflective Coatings)
- 7) Photoresist Operation
- 8) Plating
- 9) Dicing: Laser Scribing and Saw Dicing
- 10) Electrical Testing
- 11) Low Pressure Chemical Vapor Deposition

Within this clean room area four process rooms are separately controlled to Class 10,000 level. These areas are diffusion, oxide deposition, evaporation and photoresist operations.

2.2.1 Process Flow Outline

This section will describe the process flow for standard K4, K5, K6 and K7 silicon cells. A flow diagram of the processing sequence is drawn in Figure 2.7.

Solar cell manufacture is initiated with the procurement of silicon wafers. Standard wafers are 4 inch diameter, 15 mils thick, and 10 ohm-cm or 2 ohm-cm. Several vendors have been identified for wafer manufacture, including Crysteco, and Wacker. A Spectrolab specification has been written to ensure high quality material.

Each process station has been mechanized for processing of 4 inch diameter silicon wafers from which individual cells are diced at the end of the line. The equipment can accommodate wafers as thin as 65 microns.

Processing of the wafers into solar cells begins with the assignment of lots. Each lot consists of 50 wafers that receive all processing steps together. Each lot is traceable to the silicon ingot the wafers were cut from.

2.2.2 Surface Preparation

A basic, NaOH, etch is performed on the "as received" wafers to bring the thickness close to the final cell thickness of 64 to 200 microns. Several lots are etched concurrently. The etch process is computer controlled to yield the correct final wafer thickness. The final thickness is measured on 3 wafers per lot and recorded on a Statistical Process Control chart to monitor etching variability.

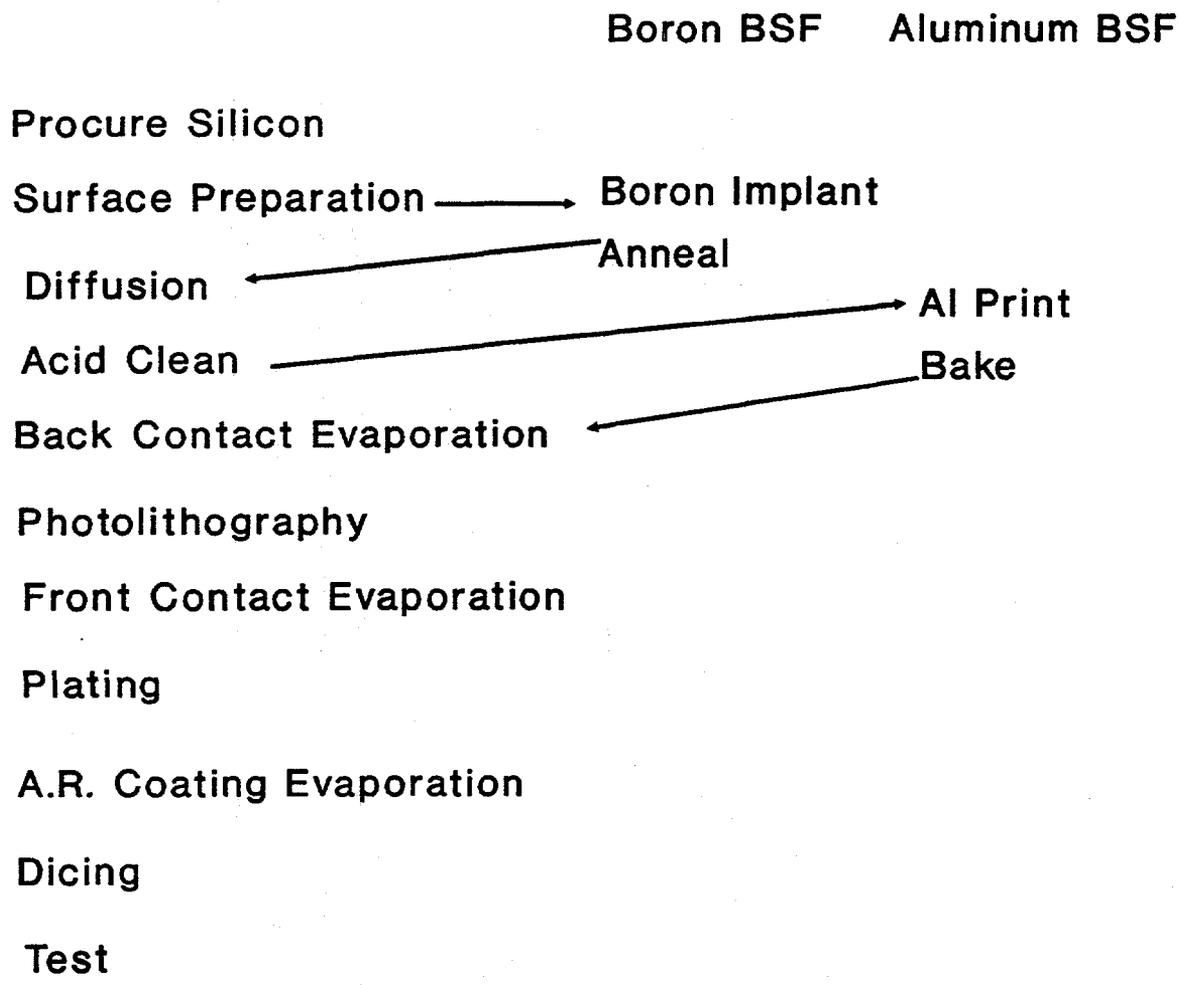


Figure 2.7 PROCESS FLOW STANDARD SILICON CELLS

The sculpture or texture etch is used to produce textured surfaces. This feature enhances current collection by reducing reflection off the surface and increasing light scattering in the base and emitter. The sculpture etch consists of an IPA/NaOH etch performed using the robotic equipment described for basic etch. This process is used for both the K5 and K7 cells.

The polish etch consists of a mixed acid etch of HF, HNO₃ and CH₃OOH acids. The thinning operation for planar cells is completed with a polish etch to smooth the surface left from the basic etch. Wafers are etched within their Flouroware cassettes to achieve a large throughput and excellent mechanical yield.

2.2.3 Back Surface Field (BSF) Formation

The use of a back surface field is determined by customer, cell, and mission requirements. Two processes are currently used to produce a back surface field: Aluminum print and bake, and Boron implant and anneal. Both of the processes create a P+ region in the back of the cell resulting in a back surface field.

The sequence of the back surface field processing within the process flow depends on the technique chosen. The aluminum print process is performed after diffusion. The boron implant and anneal process is completed prior to diffusion.

2.2.3.1 Aluminum Print and Bake

Aluminum paste is screen printed and fired into each wafer to create an alloyed region in the back that is highly p doped. Each wafer is automatically loaded onto a screen printer that coats the back of the wafer with aluminum paste (Figure 2.8).

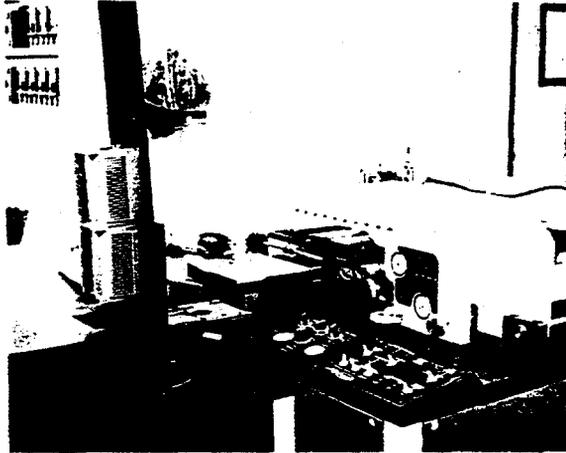


Figure 2.8 WORK STATION ALUMINUM PRINT

A metal belt transports the wafers into a furnace where it is air dried and subsequently alloyed into the substrate. Subsequent acid cleans are used to remove residual aluminum from the surface. The open circuit voltage is measured under a light source on sample wafers to verify that an effective back surface field has been formed.

2.2.3.2 Boron Implant and Anneal

Boron Implant

A Boron back surface field is chosen for thin cells, less than 200 microns thick, and infrared transparent cells. A P+ back surface field is created by a boron implant/anneal sequence.

Ion Implantation is performed by an outside vendor to a fixed specification. The procurement specification was developed to guarantee Spectrolab consistent product performance. Typically the implant uniformity will vary by no more than 2% between wafers. The purity of the boron dopant source is verified through the use of a mass analyzer. Spectrolab wafers are processed in one of two Varian Ion Implanters.

The quality of the ion implant is monitored through the use of n type wafer controls. These controls are annealed as described below and monitored for junction quality and doping profile.

Ion Implant Anneal

Wafers are annealed to remove implant induced defects and to form the P+ junction. Wafers are annealed in a Thermco 4-stack production diffusion furnace. A microprocessor is used to control gas flows and temperature changes. Figure 2.9 shows a typical junction profile after the anneal.

PROCESSED DATA
15 SEP 68 02

CHARLES EVANS AND ASSOCIATES
FILE 32

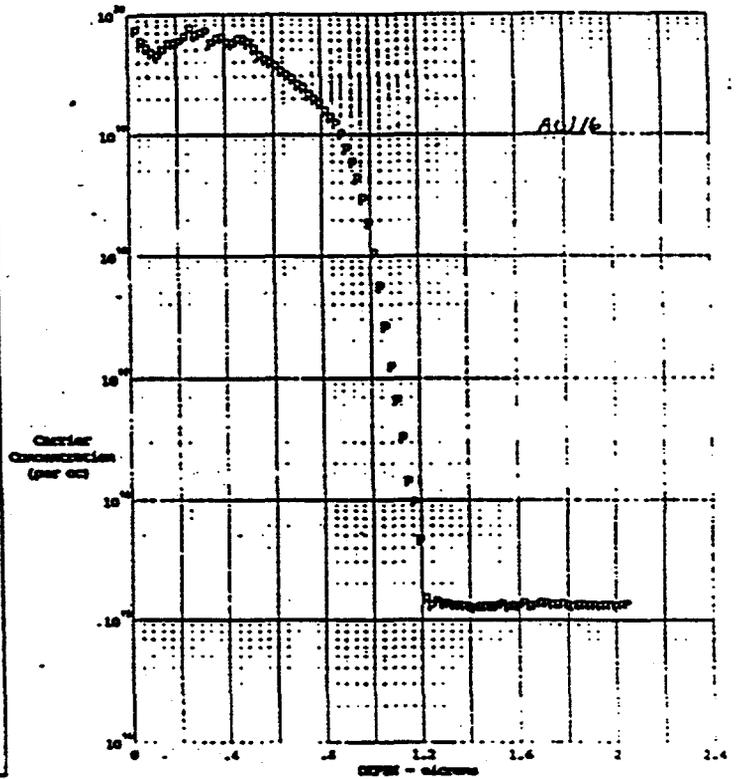
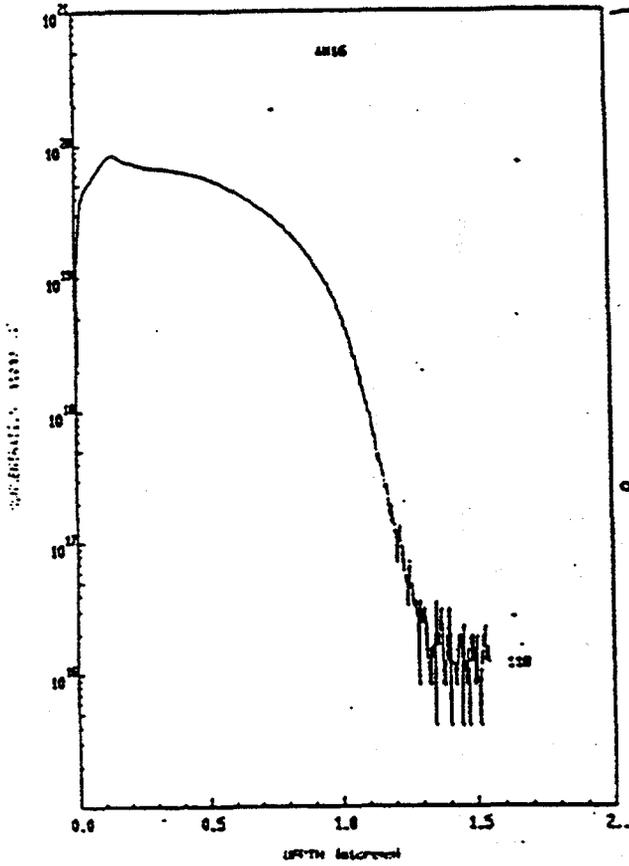


Figure 2.9 JUNCTION PROFILE FROM BORON IMPLANT PROCESS

2.2.4 Diffusion

In the diffusion process, wafers are placed into quartz boats in batches of 300 then automatically loaded into a quartz tube. (as shown in Figure 2.10) The n doped region is formed using a gaseous phosphine diffusion process. Thermco 4-stack production diffusion furnace is used for this operation. In this automated procedure, each batch is exposed to the phosphine gas for the same period of time, providing the environment needed for a thin and uniform N/P junction. The diffused layers are tested for sheet resistivity to be sure the proper diffusion has been achieved. A typical junction profile is shown in Figure 2.11.

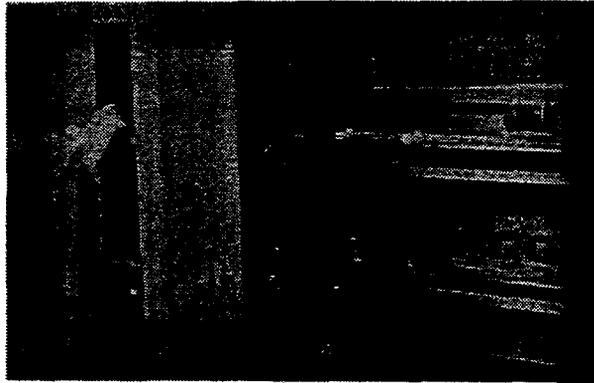
2.2.5 Contact Evaporation

After the diffusion process, wafers are cleaned using a HF etch to ensure low contact resistivity. A CHA electron beam evaporator is used to deposit layers of Al, Ti, Pd, and Ag. The use of rotating planetaries ensures uniform deposition on all parts. The thickness is controlled with a crystal thickness monitor and periodically measured with a profilometer.

The back contact is sintered in a nitrogen atmosphere to ensure good contact adhesion. Wafers are transferred into quartz boats from their cassettes and sintered in batches.

2.2.6 Photolithography

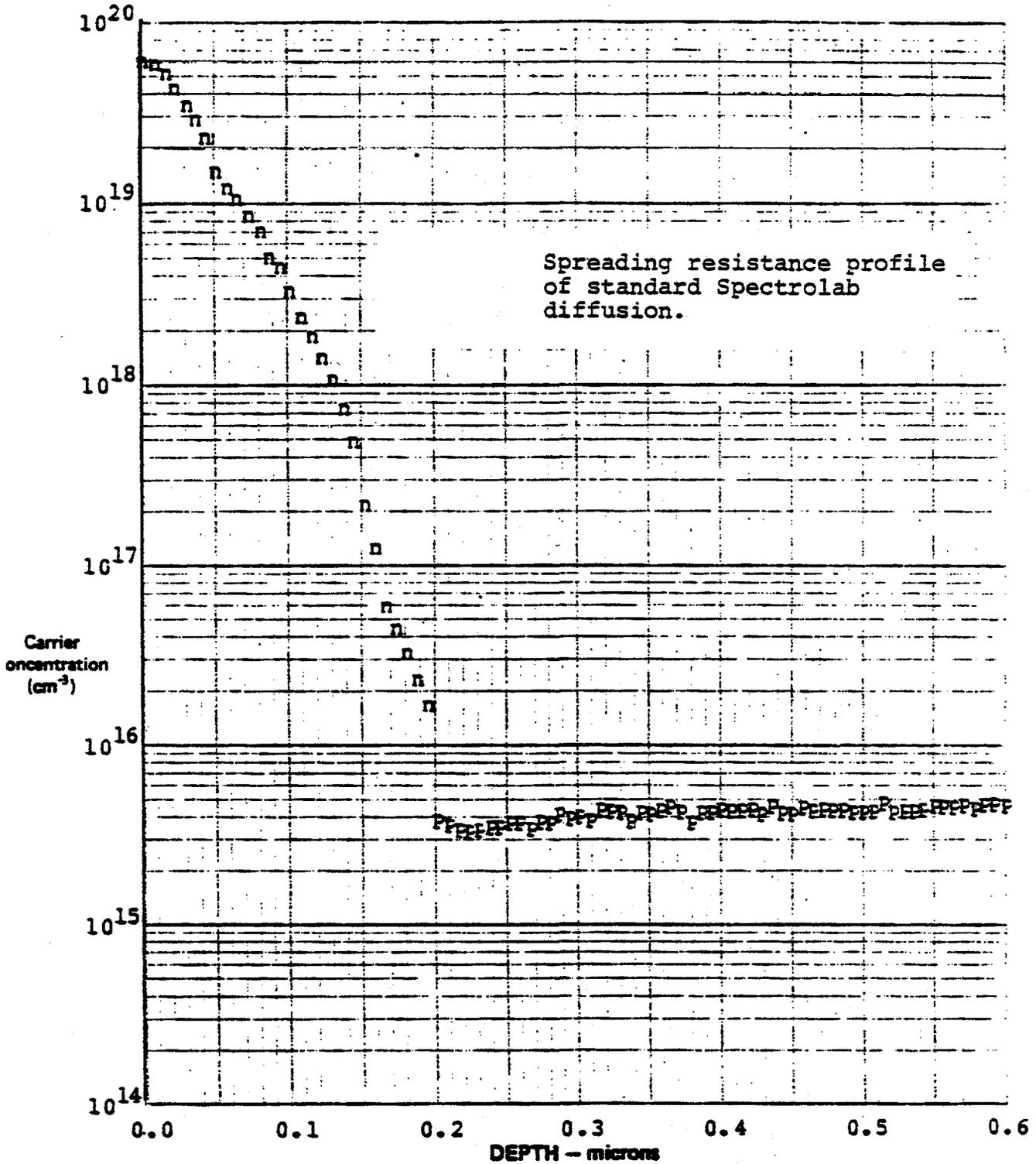
Photolithography is used to define the grid contact structure. Photoresist is spun onto each wafer using a cassette to cassette production photoresist deposition system (Figure 2.12) . A Mimir batch exposer exposes each lot to the photomask in a batch size of 25 wafers per exposure. A Ti/Pd/Ag front contact is deposited using electron beam evaporation as described in 2.2.5.



DIFFUSION

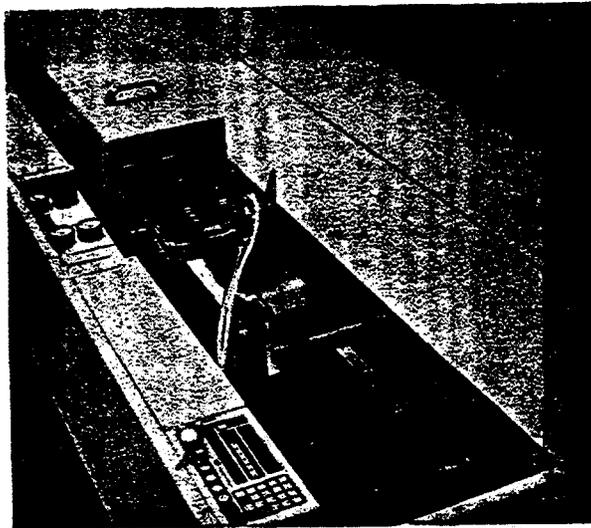
Figure 2.10 DIFFUSION FURNACE

SPREADING RESISTANCE ANALYSIS



DATE	1/22/86	PROBE LOAD	5g	ORIENTATION	<100>Si
COUNTER	282459	BEVEL ANGLE	0.0028		
SOURCE	SPECTROLAB	STEP INCREM.	2.5μ	SAMPLE #	CONTROL/C-A

Figure 2.11 JUNCTION PROFILE FROM DIFFUSION PROCESS



PHOTORESIST COATER

Figure 2.12 AUTOMATIC WAFER PHOTORESIST COATER



Figure 2.13 PLATING BATH

2.2.7 Plating

Silver may be plated on top of the previously deposited metal structure by immersing a rack of wafers into an electrically active silver plating solutions (Figure 2.13). Plating improves the performance of cells with wrapped contact structures and large area cells by reducing the series resistance of the contacts.

2.2.8 Antireflective Coating Deposition

A two layer antireflective coating is evaporated onto the active cell area to maximize the electrical performance of the cell by increasing the current output. Silicon cells receive dual layers of TiO_x and Al_2O_3 . Optical models are used to determine the optimal thicknesses of the layers.

The dielectrics are deposited using reactive evaporation. The composition of the film is fixed by controlling the oxygen pressure in the chamber. Uniform deposition is assured through the use of rotating planetaries. The antireflective coating is densified through the use of a post deposition sinter in a nitrogen atmosphere.

2.2.9 Dice

Two methods are used for dicing individual cells from a wafer: laser scribe and saw dice. The laser scribe is used for thick, 200 micron, cells. Saw Dicing is preferred for thin cells.

Laser Scribe

A YAG laser scribe is used to scribe cells from a wafer (Figure 2.14). After cutting through approximately 70 percent of the silicon thickness, the operator physically snaps the



Figure 2.14 LASER SCRIBE

wafer along the laser cut lines which accurately cleaves it into the final cell size. The scriber's programmability makes it very versatile for cutting any shape.

Saw Dice

A Disco Saw dice is used to dice cells for thin ,<200 microns, cells. A diamond impregnated saw is used to dice cells out of the wafer. Cutting parameters have been optimized to minimize chipping of the edges and breakage of wafers.

2.2.10 Test

Completed cells are tested under Spectrolab XT-10 and X-25 simulators. The light level is calibrated to a balloon standard with the same spectral response as the cell under test. Spectral irradiance measurements of the simulator are available to translate AM0 measurements to AM1.5.

2.3 CELL PROCESSING DESCRIPTION: Specialty Silicon Solar Cell Processing

Process flows for the specialty cells described in Section 2.1.4 are shown in Figures 2.15 and 2.16. The wrapthrough cell is now a production solar cell at Spectrolab. Currently Spectrolab has fabricated over 30,000 200 and 100 micron wrapthrough cells. Additional processes needed for this product are described in Sections 2.3.1 and 2.3.2.

Silicon concentrator cells are being developed as part of the SANDIA concentrator initiative. All of the processes needed are available with current manufacturing equipment. The proposed process flow is shown in Figure 2.16. Additional processes needed for this product are described in Sections 2.3.4 - 2.3.5.

Procure Silicon
Surface Preparation
Hole Formation
Hole Smoothing
Boron Implant
Anneal
Diffusion
Acid Clean
Deposit SiO₂ Via Insulator, LPCVD
Photolithography
Contact Evaporation
Plating
A.R. Coating Evaporation
Dicing
Test

Figure 2.15 PROCESS FLOW: WRAPTHROUGH

Thin wafer to 4 mils

Deposit oxide

Pattern

Texture

Remove oxide

Grow field oxide

Form back surface field

Pattern front oxide

Diffuse

Deglaze

Grow passivation oxide

Pattern thin oxide

Deposit front contact metal and lift-off

Deposit rear contact metal

Plate Ag

Apply dual AR

Sinter

Figure 2.16 ENVISIONED PROCESSING SCHEME SILICON CONCENTRATOR

Spectrolab has fabricated prototype and production interdigitated back contact cells. These cells are fabricated on 50 micron thick silicon substrates. Special care is taken throughout to prevent breakage.

2.3.1 Hole Definition and Smoothing

The wrap through hole and dielectric allow the n+ front contact to be passed through to the back of the cell so that both n+ and p+ contacts are coplanar. The design and manufacture of this hole is one of the most critical aspects of the coplanar cell. It is important to obtain a smooth profile hole.

Four holes are defined using a laser scribing process. A YAG laser is used to scribe the holes. Immediately after laser scribing the material within the hole is highly damaged and the edge is very jagged. These characteristics would result in excessive junction leakage. Spectrolab has developed an etching procedure based on both alkaline and acid etching that results in a very smooth profile as shown in Figure 2.17.

2.3.2 Hole Insulation

The insulating oxide electrically isolates the n+ from the p+ contact. The integrity and density of the dielectric oxide itself plays a critical role in achieving good device performance. Currently this layer consists of one micron thick LPCVD SiO₂ layer. This layer is defined by mechanical masking to minimize pinholes due to etching processes.

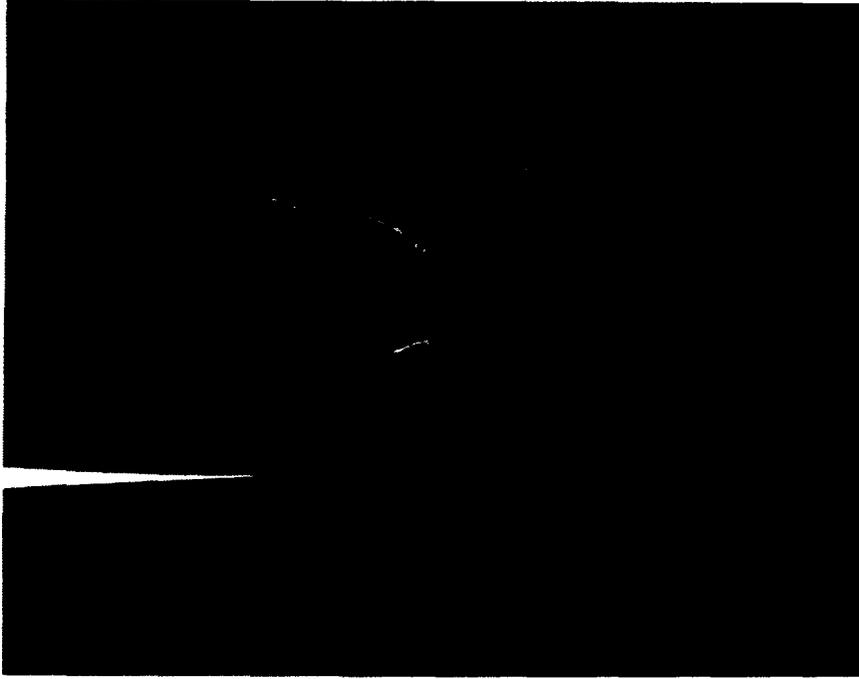


Figure 2.17 CROSS-SECTION OF SMOOTH WRAP EDGE

2.3.3 Oxidation

A thermal oxidation process is used to passivate surfaces of the silicon concentrator and interdigitated back contact cells. For the concentrator cell, this layer insulates the n+ contact from the p+ substrate (see Figure 2.5).

The oxidation process is performed in a 4- stack production Thermco diffusion furnace. The temperature and gas profiles are microprocessor controlled. Typically 1000 Å of SiO₂ are grown on the wafers.

2.3.5 Photolithography

Special photolithography techniques are required for wrapthrough, interdigitated back contact and concentrator cells. For wrapthrough cells Spectrolab has developed a technique to deposit uniform coating of photoresist on both sides of the wafer and inside the hole area. The exposure of the wafer is performed on the Mimir batch exposer as described in Section 2.2.6.

The interdigitated contact and concentrator cells require fine alignment of the contacts to other features on the wafer. These cells are exposed using a Kasper aligner fitted with a microscope stage aligner. Fine grid lines, 6 to 8 microns wide, have been achieved by optimizing photolithography processing.

2.4 GaAs Cell Description

Spectrolab manufactures planar and concentrator GaAs solar cells. Cells have been fabricated on both Ge and GaAs substrates.

2.4.1 Single Junction GaAs/Ge Cell

Spectrolab has developed a production ready GaAs/Ge single junction solar cell. The germanium substrate is cheaper and sturdier than gallium arsenide. Recent production experience on 2 cm by 4 cm cells has yielded an average efficiency exceeding 18% (28°C AM0) or 21% (28°C AM1.5). Figure 2.18 shows the distribution of over 650 cells that were manufactured at Spectrolab for the UOSAT-F program. Typical cell characteristics are:

$$\begin{aligned}V_{oc} &= 1023 \text{ mV,} \\J_{sc} &= 29.6 \text{ mA/cm}^2 \\C_{ff} &= 81.7\% \\eff. &= 18.3\%\end{aligned}$$

Details of the cells processing are discussed in Section 2.5.

Several large area cells, up to 4 cm by 4 cm, have also been manufactured with an average efficiency of 18.3%. Prototype 6cm x 6cm cells of over 18% (28°C, AM0) efficiency have also been made.

2.4.2 GaAs/GaAs Cell

Planar Gallium Arsenide cells have similar electrical characteristics as single junction GaAs/Ge cells. The GaAs/GaAs cell is used as the top cell in a multicell mechanical stack due to its infrared transparency. To minimize absorption in the substrate a low doped, mid 10^{17} cm^{-3} or high 10^{16} cm^{-3} , n- type substrate is used. Cells have been manufactured with an efficiency exceeding 19% (28°C, AM0).

UoSAT EFFICIENCY DISTRIBUTION

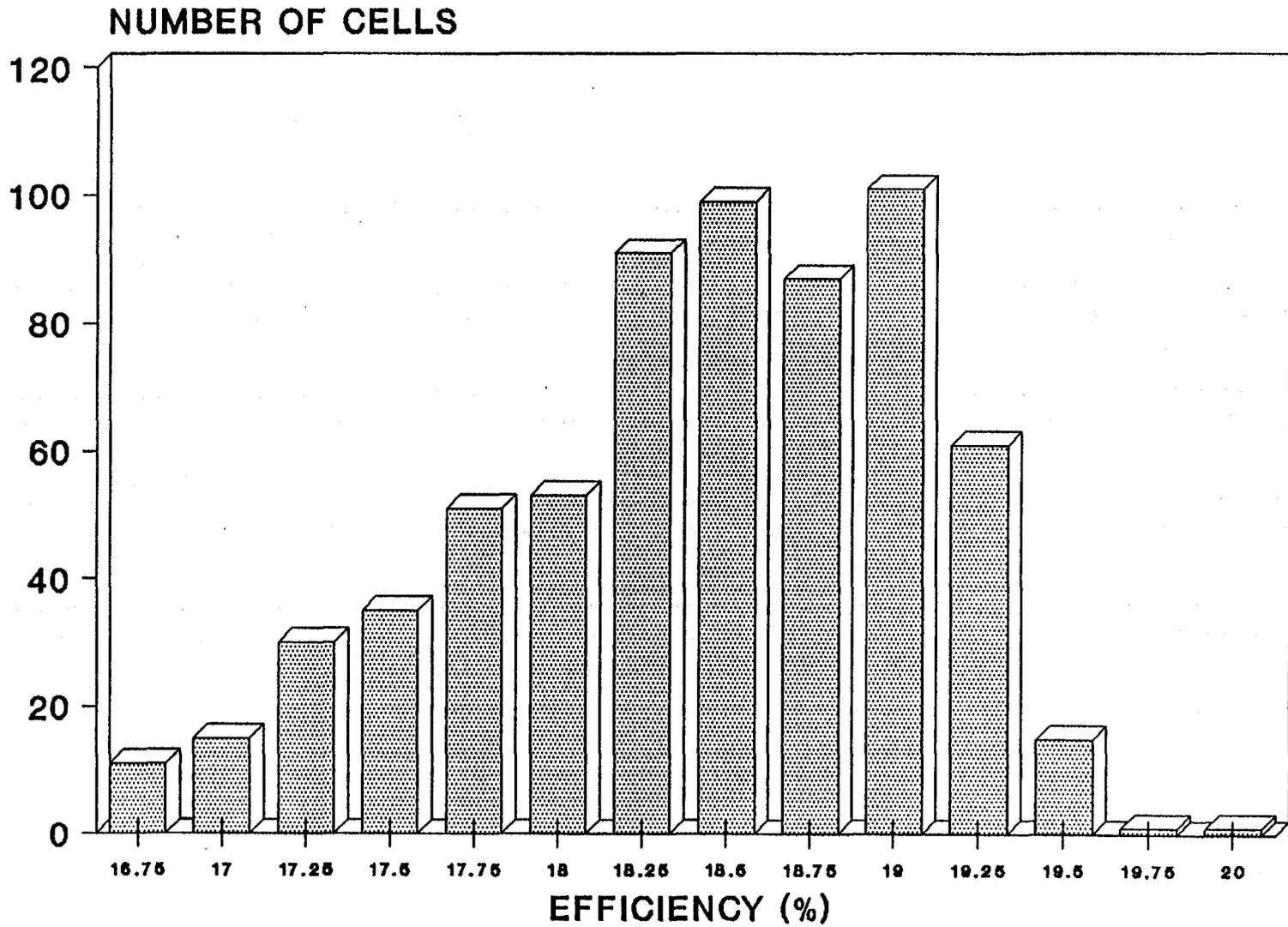


Figure 2.18 UOSAT EFFICIENCY DISTRIBUTION

2.4.3 Mechanical Stacked GaAs/Si cell

In a mechanically stacked multijunction cell the component cells can be processed and optimized independently for maximum efficiency. Spectrolab has produced a prototype voltage matched 2cm x 4cm mechanically stacked device. An optical coupling liquid was used between the cells to enhance current collection in the silicon bottom cell. Current vs voltage characteristics for the individual cells and the mechanical stack are shown in Figures 2.19 and 2.20 respectively. The efficiency of this device at 28°C, AM0 is 22.2%, 19.9% from the GaAs cells and 2.3% from the silicon cells.

A prototype 4 cm x 4 cm mechanical stacked GaAs on silicon cell was fabricated to gain experience with the assembly of mechanical stacks. It was constructed in the four terminal configuration to accurately measure each cell component. The mechanical integrity of the assembly is assured by bonding of the cells to a substrate.

2.4.4 III-V Multijunction Cells

Spectrolab has developed multijunction solar cell prototypes based on GaAs, Si and Ge cell components. The projected efficiency is calculated to be over 32% at 300X AM1.5D. Spectrolab has retained the technology rights for this concept pending an application for patent coverage.

2.4.5 GaAs/GaAs Concentrator Cells

Spectrolab has manufactured over 400 GaAs space concentrator cells for operation at 15X, AM0. The cell processing is described in Section 2.5. A distribution of the cells manufactured is shown in Figure 2.21. The best cells manufactured exceeded 21% at 15X AM0 28°C.

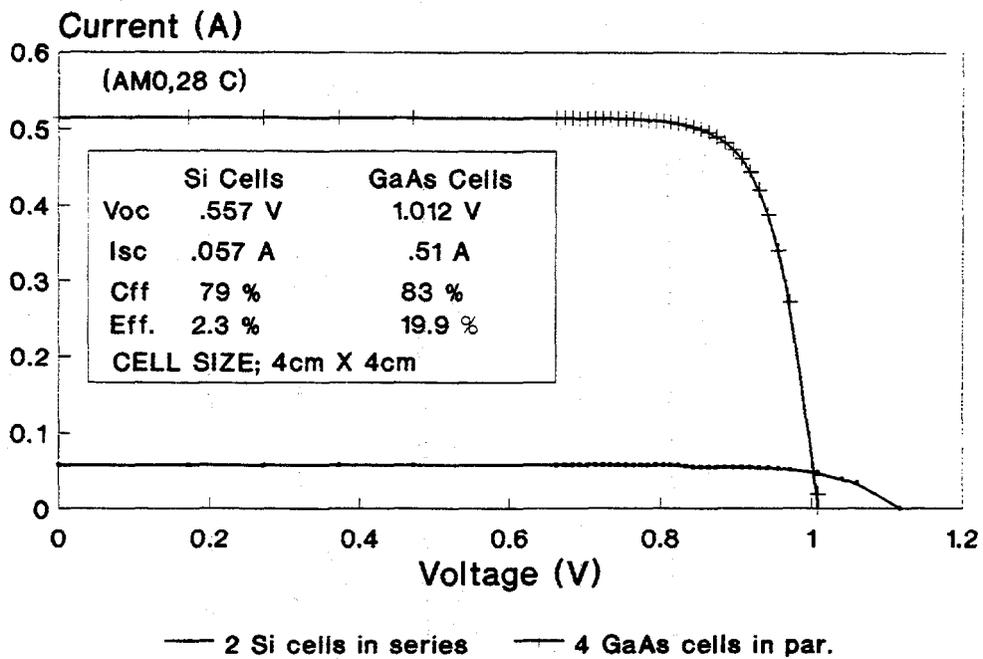


Figure 2.19 IV CURVES OF COMPONENT CELLS IN MECHANICAL STACK

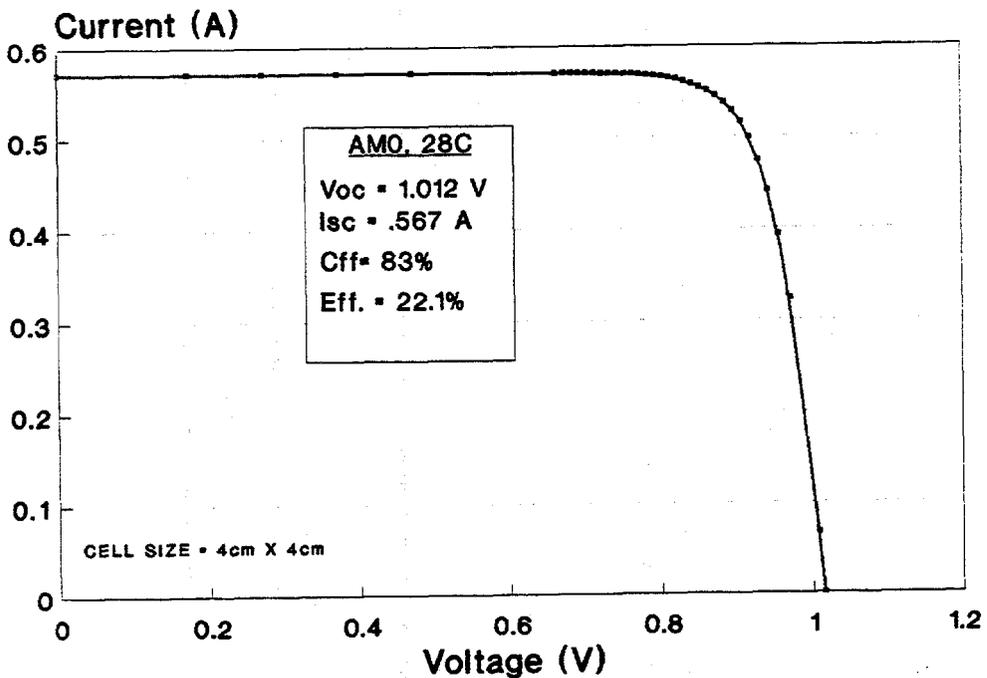


Figure 2.20 IV CURVE MECHANICAL STACK

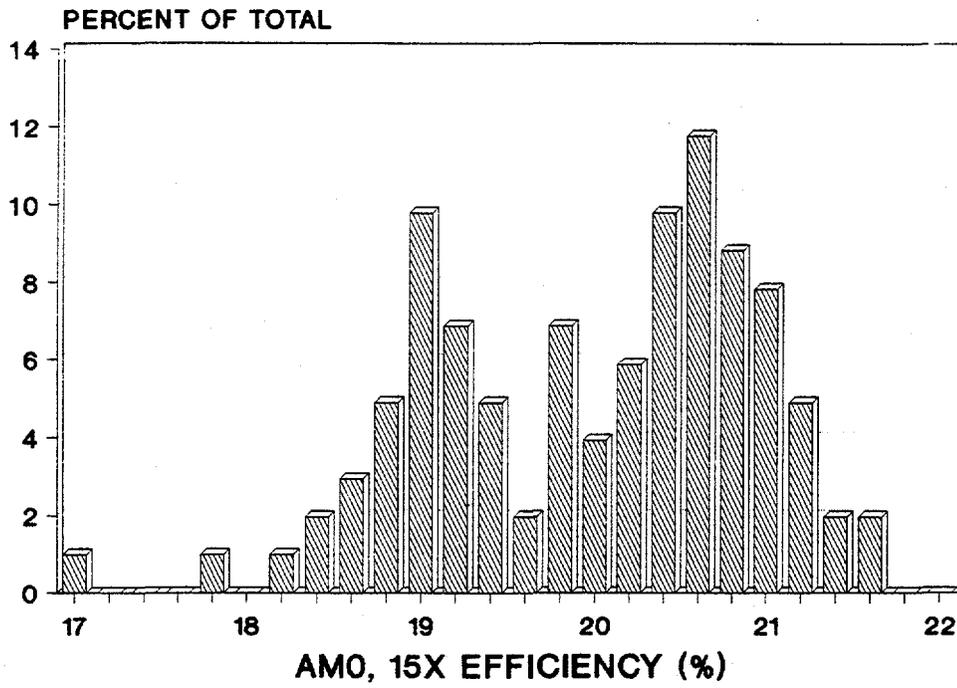


Figure 2.21 DISTRIBUTION GaAs SPACE CONCENTRATOR CELLS

2.5 GaAs/GaAs and GaAs/Ge Processing

Spectrolab has a dedicated GaAs solar cell processing facility comprising approximately 4,000 sq. ft. of temperature and humidity controlled Class 100,000 and 10,000 clean room area. MOCVD GaAs/GaAs and GaAs/Ge flat plate and concentrator solar cells and panels are manufactured in these facilities. Process flows for GaAs/GaAs and GaAs/Ge cells are shown in Figure 2.22. Specific process descriptions are also included in this section.

Solar Cell processing performed for GaAs/GaAs and GaAs/Ge solar cells are similar. Each process will be described and specific differences between processing cells on germanium and GaAs substrates will be identified.

2.5.1 Wafer Procurement

Gallium Arsenide wafers are purchased epi-ready. Sumitomo has developed a cleaning procedure that allows wafers to be placed directly in the reactor. Standard GaAs substrates are n type doped to $1 - 4 \times 10^{18} \text{ cm}^{-3}$. Substrates for the Infrared transparent cell are chosen to minimize absorption. Low doped material, 10^{16} to 10^{17} cm^{-3} is chosen for this purpose.

The starting germanium wafer is 4.5 cm x 4.5 cm, 200 microns thick, n-type and polished on the front side. The wafer is doped to $5 \times 10^{17} \text{ cm}^{-3}$ with Sb (antimony) and oriented 6 degrees off $\langle 100 \rangle$ towards the nearest $\langle 111 \rangle$ plane. Germanium wafers are purchased primarily from Crystal Specialities. Other manufacturers are under evaluation.

Receive Wafers
MOCVD Growth
Plating Mask Deposition
Back Contact Evaporation
Photolithography
Front Contact Sputter
Plating
Cap Etch
Sinter
AR Coating Deposition
Saw Dice
Test

Figure 2-22 PROCESS FLOW FOR GaAs SOLAR CELLS



Figure 2.23 CVD EQUIPMENT MOCVD REACTOR

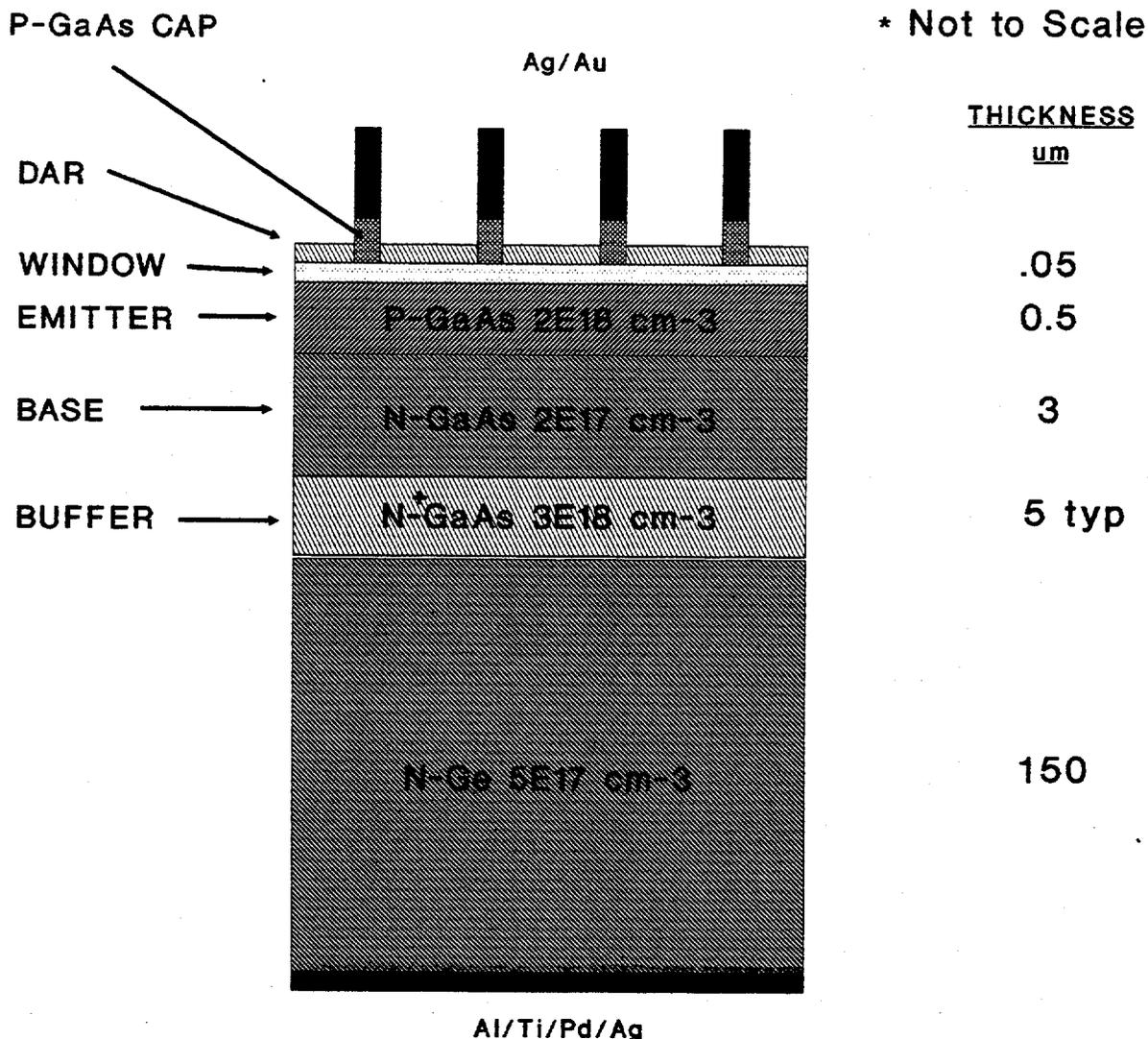


Figure 2.24 GaAs/Ge SOLAR CELL STRUCTURE

2.5.2 MOCVD GaAs Growth

Spectrolab has established a MOCVD manufacturing facility for GaAs/Ge and GaAs/GaAs cells at Hughes Aircraft Company Microwave Products Division (MPD) in Torrance, California. MPD has a team of engineers dedicated to supporting Spectrolab in all of its MOCVD growth requirements for photovoltaics. It has supported Spectrolab for the last three years and will continue to be the center of excellence for GaAs MOCVD growth operations.

Currently GaAs growth is performed on two research and development reactors and a medium scale CVD Equipment reactor (Figure 2.23). Each reactor has produced GaAs solar cells with a 1 sun, AM0, 28°C efficiency in excess of 20%. The reactors are housed in over 3,000 sq ft of clean room area where space has been allocated for up to 10 production MOCVD reactors.

Figure 2.24 shows the solar cell structure grown using these reactors.

Gallium Arsenide growth on germanium substrates starts with the nucleation of GaAs on the substrate. An N+ type buffer between 2 to 6 microns thick and doped to $3E18 \text{ cm}^{-3}$ with silicon is grown using a specific nucleation/growth procedure designed to minimize the diffusion of gallium into the wafer. The purpose of the buffer is to reduce the relatively dense network of defects in the GaAs and provide the low defect layer on which to grow the solar cell structure.

The next layer to be grown is the base. This layer is typically 2 to 3 microns thick and doped to $2 \times 10^{17} \text{ cm}^{-3}$ with silicon. It serves as the absorbing region for longer wavelength photons and is the active n-type region of the P-N junction.

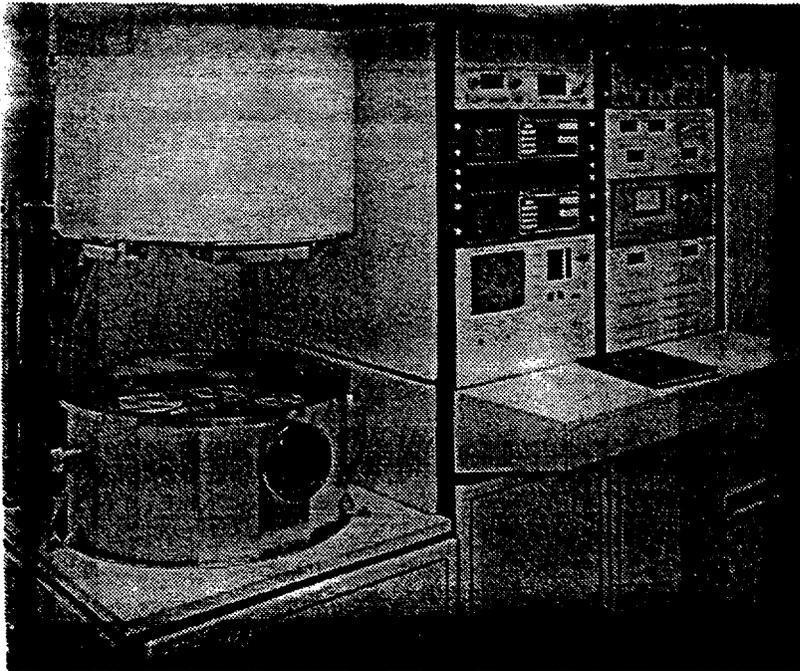


Figure 2.25 AIRCO ELECTRON BEAM EVAPORATOR

The p-type emitter is doped to 2 to 4 x 10¹⁸ cm⁻³ with zinc. The boundary between the base and emitter forms the other half of the active photovoltaic junction. The emitter is typically .5 microns thick.

The AlGaAs window serves to passivate the surface of the emitter by providing a transparent heteroface at the cell surface. It is typically 500 Å thick and is heavily doped to 2 x 10¹⁸ cm⁻³ with zinc. The aluminum concentration is critical for high performance and environmental stability.

A unique feature of our cell design is the GaAs cap structure. This provides a effective barrier against metal diffusion into the sensitive region. The cap is typically .3 to .5 microns thick and is heavily doped (>1 x 10¹⁹ cm⁻³) with zinc. The cap layer allow good ohmic contact to be achieved between the grid and the front of the cell. It also allows higher efficiencies to be achieved, compared to other designs, since it reduces the recombination velocity under the contact, allowing higher Voc's to be achieved.

2.5.3 Wafer Thinning

The transparent GaAs cell is thinned to a maximum thickness of 125 microns to maximize transmission to bottom cells. Spectrolab has demonstrated wafer thinning using either chemical or mechanical means. A Strassbaugh cassette to cassette wafer grinding machine, located at Microwave Products Division, has been successfully used to thin GaAs and Ge wafers to 2 mils. Mixed acid etches consisting of mixtures of H₂O₂ and NH₄OH are also used to thin gallium arsenide wafers. Germanium wafers are thinned in a solution of H₂O, HF and H₂O₂.

2.5.4 Back Contact Deposition

The back contact is applied in an Airco electron beam evaporation system (Figure 2.25). The back contact to GaAs substrates consists of layers of gold, germanium and nickel. Cells using germanium substrates receive a back contact of aluminum, titanium, palladium and silver. The infrared transparent GaAs cell receives a photolithography step prior to back contact deposition to define the back grids (described in Section 2.5.6).

2.5.6 Photolithography

Front and back grids are defined using a photolithography process. To facilitate the throughput of cells a batch exposer is used to expose several wafers at a time, as described in Section 2.2.6. An etch is used to remove a plating mask from the grid region. This process has been optimized to prevent the undercutting of the mask, and to keep the integrity of the photoresist. Current techniques have produced 15 micron line widths. Lines as narrow as 8 microns have been produced using reverse image lithography.

2.5.7 Sputter Front Contact

The ohmic contact to the gallium arsenide cap layer is formed with sputtered layers of titanium and gold. A Bosch four target automated sputtering system is used to deposit the titanium and gold. This system is shown in Figure 2.26.

2.5.8 Plate-Up

The contacts are completed by plated layers of silver and gold. A thick layer of silver is needed to reduce series resistance.

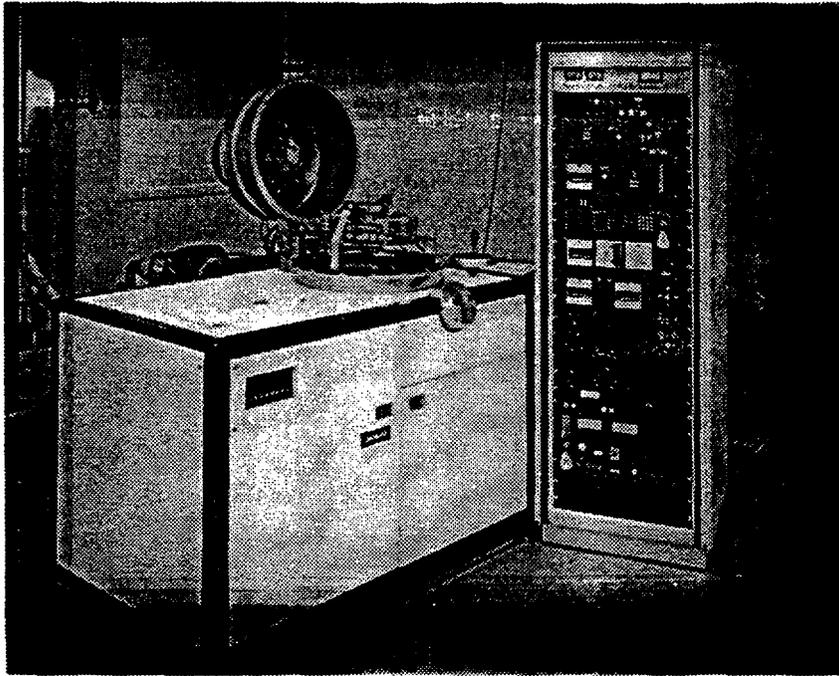


Figure 2.26 BOSCH SPUTTERING SYSTEM

The gold layer is required to mask the silver grids during the GaAs cap etch operation.

2.5.9 GaAs Cap Etch

The final MOCVD growth is a highly doped p++ GaAs layer. Its purpose is to reduce the contact resistance to the solar cell and to separate the metal grid from the emitter, thus increasing thermal stability and assembly hardness. The cap is removed from active area regions after the contact is formed. An etch solution of H_2O_2 and NH_4OH removes the cap layer. The previously described gold plating operation protects the silver from the cap etch solution.

2.5.10 Sinter

Front and back contacts are sintered in a reducing hydrogen atmosphere. This process alloys the gold and silver in the contact and improves the contact adhesion.

2.5.11 Antireflective Coating Deposition

The Antireflective coating is deposited using reactive evaporation in a CHA evaporator. Layers of Al_2O_3 and Ta_2O_5 , tuned to optimize current collection, are deposited. Spectrolab has developed computer software to aid in optimizing the thicknesses of the antireflective coatings for maximum current collection.

The evaporators utilize rotating planetaries that ensure that the thicknesses of the films are uniform from part to part. Glass slides serve as monitors to aid in process control.

2.5.12 Saw Dice

Individual cells are cut out of gallium arsenide and germanium wafers using a Disco dicing saw with a diamond coated blade. The saw is aligned to features on the wafer and the dicing program is activated to cut the cell.

This process has been optimized to minimize the formation of cracks and chips at the edge that could result in later breakage. The quality of the edge has been found to be particularly important to prevent breakage during subsequent welding and soldering of cells.

2.5.13 Testing

Individual cells are tested on under a X-25 solar simulator calibrated to a GaAs balloon standard. This test yields a cell characteristic under AM0 conditions. Spectral correction can be performed to calculate efficiencies under AM1.5 conditions.

2.6 MODULE PROCESSING DESCRIPTION

Spectrolab engages in the design, development, fabrication, and test of silicon and gallium arsenide solar cell panels in many varieties and configurations. This capability has broadened Spectrolab's solar cell technology base of understanding the specific requirements associated with solar cells in systems applications.

The panel area occupies 21,000 square feet of clean room-type conditions and is equipped with a five-zone electronically controlled humidity and temperature control system. An additional 14,000 square foot high bay area was completed in October 1989 was added for solar array manufacturing.

Perimeter utilities include drops for vacuum, nitrogen, air and DI water. Separate operational areas are provided for coverslide bonding, interconnect forming, solar cell circuit assembly, bonding, wiring, final assembly and inspection, and electrical performance testing using a Large Area Pulse Solar Simulator.

Many of the processes used in the manufacture of flight panels could be applied to the manufacture of terrestrial solar modules. This section describes generic processes which are used to produce flight panels that could easily be transferred to terrestrial module manufacture.

2.6.1 Interconnect Attachment

Interconnects are attached to the top contact of the cells for later connection to the back contact or substrate and assembly into a module. Soldering, parallel gap welding and wire bonding are used for both front and back contact attachment to gallium arsenide and silicon cells. The choice of method is dependent upon customer requirements and the system design.

2.6.1.1 Parallel Gap Welding Process

Parallel gap welding is an established production process on silicon, gallium arsenide and germanium. Spectrolab has developed techniques for successful welding to the front and back contacts of silicon, GaAs/GaAs and GaAs/Ge cells with no measurable electrical degradation.

The welding process uses parallel gap electrodes powered by a constant voltage DC power supply which supplies a current pulse to the parts being welded. This process is computer controlled to ensure consistently welded joints.

2.6.1.2 Soldering Process

The soldering process also uses the parallel gap configuration but lower integrated energy is supplied to the electrode tips. Quality joints are ensured by inspecting each joint for conformance with MIL specification and NASA requirements. The soldering machine output is set for a fixed voltage and duration based on set-up procedure test data.

2.6.1.3 Wire Bonding

Wire bonding has been used on gallium arsenide programs where space constraints on the contact area require wire connections. Connections are made using a thermosonic bonder at the Microelectronics Circuits Division of Hughes Aircraft Company and at Microwave Products Division.

2.6.2 Cover Glass Application

Spectrolab has extensive experience bonding coverglass to silicon and gallium arsenide solar cells. Techniques are available that allow for coverglassing of silicon cells with thicknesses down to 62 microns and in large areas, up to 8 cm x 8 cm. The process flow is as follows:

- 1) Application of adhesive
- 2) Aligning of coverglass to cell
- 3) Curing of adhesive in oven
- 4) Cleaning excess adhesive and inspection

Gallium Arsenide cells on GaAs and Ge substrates have been successfully filtered using techniques developed for silicon cells.

The coverglass is made from CMX or fused silicon and may have a antireflective coating. Dow Corning 93-500 is used to bond the coverglass to the cell. Curing sequences have been developed that result in flat durable assemblies. For example, silicon cells assemblies consisting of a 100 micron thick 7 cm x 7 cm cell, 25 microns adhesive and an 125 micron thick CMX coverglass have a bow of less than 25 microns.

2.7 MODULE DESCRIPTIONS

2.7.1 GaAs Concentrator Cell Receivers

Spectrolab in partnership with other Hughes divisions under USAF funding has manufactured GaAs concentrator cell receivers capable of withstanding very high temperatures. The cells were optimized for operation at 12X AM0 in a linear array. The cell performance is discussed in Section 2.4.5 and processing in 2.5.

Receivers were assembled using expertise from other Hughes divisions: Microwave Circuits Division (MCD) and Microwave Products Division (MPD). All members of the "Hughes team" worked together to produce a linear array of solar cells that met high temperature requirements and were delivered on schedule. Techniques were developed to assemble the linear array. This processing included:

- Attaching a conducting bus bar to the substrate.
- Attaching leads to the bus bar.
- Attaching GaAs cells to the substrate.
- Wire bonding from the cell to the bus bar.

Techniques developed during this program are available for use on the proposed cell designs described in Section 2.4.

2.7.2 Assembly Description: GaAs/Si Multijunction Planer Solar Cells

Spectrolab has all of the assembly technologies in place to manufacture mechanically stacked solar cell assemblies. An advantage of a mechanically stacked multijunction cell over a monolithic cell is that component cells can be processed independently for maximum efficiency. A prototype mechanically stacked assembly was built to determine current cell capabilities. In building the prototype we drew on Spectrolab's extensive panel assembly experience. Fabrication details and the electrical performance of this cell are included in Section 2.4.3.

2.7.3 GaAs Panel Experience

Spectrolab has over ten years experience in manufacturing GaAs/GaAs and GaAs/Ge solar cells and panels. Recent results are listed in Appendix A.

2.8 CURRENT COST ESTIMATES

2.8.1 GaAs Cell Manufacture

We have made cost estimates of the current market price (in \$ per cm^2 fully burdened) of GaAs and GaAs/Ge concentrator cells assuming manufacturing at about the 1 MW level and a cell efficiency of 25% AM1.5D at 300X concentration. Estimates of the contribution to the total cost from each element is shown below:

Cell Type	Eng. Support	Admin.	Cell Mfg.	Wafer	MOCVD Growth
GaAs/GaAs	6%	1%	38%	26%	28%
GaAs/Ge	7%	1%	44%	14%	33%

The allowable cell costs to meet the DOE short term goal of \$.12/kWH for mid and high concentration ratios, assuming an indirect cost of 50% (DOE five-year research plan) are:

Cell Efficiency (%)	Conc. Ratio (suns)	Estimated Cell Cost (\$/cm ²)
24-30	200-400	1.3 - 3.7
30-36	700-1000	6.5 - 12

Current costs are too high to meet the cost goals using GaAs/Ge and GaAs/GaAs concentrator cells. The costs come from several sources. The current level of engineering support is too high to support a cell price of \$10 cm². As the GaAs concentrator production technology matures, and the volume increases, the amount of manufacturing line support per cell will be reduced.

The cell's manufacturing cost is too high to meet DOE goals. This is partly a result of the high capital expense of MOCVD reactors and their present under-utilization resulting in high overhead rates. The high manufacturing cost is also the result of labor intensive test techniques to measure cell performance at 300X. Test methodology improvements will reduce these costs.

A major source of the high cost is the wafer cost. We expect the germanium wafer cost to fall at least 50% from current levels as the demand increases.

Finally, MOCVD costs need to be significantly reduced from present levels. Currently MOCVD reactors are under-utilized and are operated by skilled personnel. Increased usage by production operators will reduce the MOCVD growth costs. Spectrolab's philosophy toward improved MOCVD reactor development with cycle times one third of current values will also substantially reduce cost by reducing the amortization of the reactor per unit cell.

2.8.2 Silicon Cell Manufacture

Spectrolab has performed a detailed analysis of the projected price for the silicon concentrator cell described in Section 2.1.4 and 2.3. The cost analysis assumes a 20% efficiency when tested at 250X AM1.5, 25°C. A cell price of \$1.7/cm² was determined based on a production rate of 1 -10 MW/year, projected labor rates, overhead and G & A.

The DOE cost goal of \$.12/kWH can be met today using a silicon concentrator cell. Spectrolab will have the capability to produce these cells in the near term as a result of the Sandia Mantech program mentioned earlier.

3.0 TASK 2: POTENTIAL IMPROVEMENTS IN COST AND PERFORMANCE

In this section, Spectrolab will identify potential module and cell manufacturing processes that can lead to improved performance and reduced manufacturing costs. Manufacturing costs can be reduced through minimizing documentation requirements and automation of processes. Cell efficiencies can be improved through the use of the cell designs described herein.

3.1 PLAN FOR COST REDUCTION: GENERAL PROCEDURES

Production of space qualified cells requires complete traceability from the silicon ingot to finished product. Currently MIL specifications are followed throughout for in process tests and final testing. These requirements assure the reliability that is needed for space applications. However, terrestrial cells have different requirements that may not necessitate the use of costly MIL spec. requirements. The final cost of the cell can be reduced by eliminating unnecessary paperwork that is currently performed to document cell pedigree.

3.1.1 Inspection Requirements

The inspection criteria for space solar cells are designed to avoid failures in use. One hundred percent of the cells are inspected at 3X to 10X for customer designated imperfections. Strict criteria are set for edge chips, metal voids and integrity to avoid reliability problems in space. Typically flaws such as small edge chips and pin holes, mean rejection of an otherwise acceptable cell.

Terrestrial cells could be inspected at 1X for gross flaws, such as cracked cells and large edge chips. Electrical testing would be used as the primary criteria for acceptance. It is expected that loosening the inspection criteria will result in a reduction of the net cost per cell by increasing the mechanical yield.

3.1.2 Paper Work Reduction

Concern over the reliability of components for space use has led to the institution of traceability requirements for solar cells. The pedigree of each cell is known from its beginning as a silicon ingot to its completion as a solar cell. Each cell is marked with a lot code which provides the link to its paper trail.

A reduction in cost could be obtained by eliminating these traceability requirements. A small reduction in labor would also occur by eliminating the lot coding operation.

3.1.3 Qualification and In-Process Tests

Space qualified solar cells go through a rigorous testing program to assure they will survive their planned mission. Qualification tests are specified by each customer and are overseen by product and test engineers. These include environmental tests such as; radiation testing, temperature cycling and humidity testing. Most of the tests are determined by the harsh space environment and are not relevant for terrestrial use. Environmental tests designed to simulate terrestrial conditions will be performed to assure a 30 year module life. Spectrolab suggests that this work be performed as part of Phase 2.

In-process tests are performed on test structures to verify that the cells will meet the requirements. Some of the current in process tests are: tape test, pull test, and AR coating integrity. The cost of the cell would be reduced by eliminating or reducing in-process tests performed. These tests will be evaluated in light of the requirements for terrestrial solar cells.

3.1.4 Large Volume Production

The institution of large volume production of cells will reduce the final cost of the cell. The piece price reduction comes from a number of sources: fixturing, such as photomasks, are amortized over a larger number of cells, yields improve due to operator familiarity with a product line and material costs will decrease due to volume discounts. A Sandia study showed that with a 50% indirect cost factor, the goal of \$0.12/kWh can be met using current technology with a production rate of 100 MW per year. When a 30% indirect cost factor is assumed the production rate needed to meet \$0.12/kWh is reduced to 10 MW/year (Ref. 1).

3.2 PLAN TO MEET DOE COST GOALS: Si CONCENTRATOR CELLS

The technology is currently available to fabricate silicon concentrator cells that meet the short term DOE cost goals of \$.12 /KWH. This section will describe current work of silicon concentrator cells and ways to reduce the cell cost.

3.2.1 Sandia Contract Silicon Concentrator

Spectrolab is currently developing the manufacturing technology for a silicon concentrator cell projected to have a 20% efficiency at 250X AM1.5D. Current projections indicate that a

cost target of less than \$1.7/cm² will be achieved. Figure 3.1 shows a cross-section of the basic device structure. The features of this cell are:

1. Sculptured surface
2. Shallow N+ emitter
3. Back Surface Field
4. Back Surface Reflector
5. Front Surface Passivation
6. Dual A.R. Coating

The cell will be processed using 4" diameter .2 - .5 ohm-cm p-type 4 mil thick FZ silicon wafers.

3.2.2 Alternate Silicon Concentrator Designs

To achieve an even lower cell cost some of the features, described above, may need to be eliminated. The final cell efficiency will decrease but that may be offset by the net savings.

Potential savings could be achieved by eliminating the following features:

1. Sculpturing
2. Back Surface Field
3. Front Surface Passivation

The elimination of the back surface field would have the greatest impact on cost. It is also uncertain at this stage that the BSF will be effective on low resistivity material. Currently, the back surface field is achieved using an off site implant process. Costs would be reduced through the use of an alternative technique for forming the back surface field, such as aluminum print (Section 2.2.3.1), if it is required.

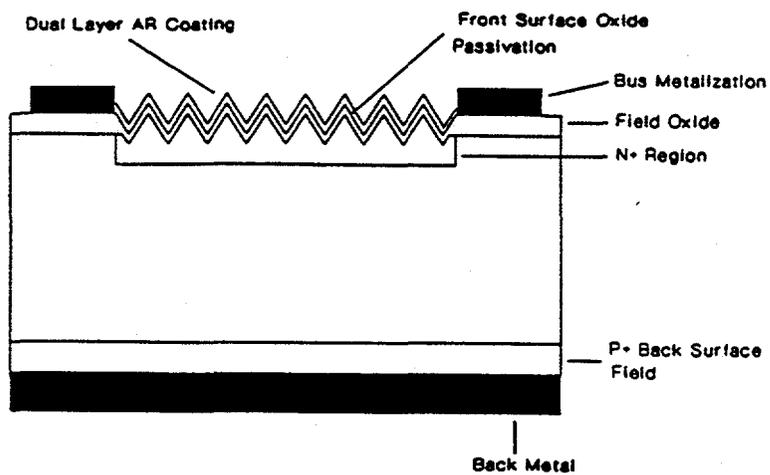


Figure 3.1 CROSS-SECTION Si CONCENTRATOR CELL

Spectrolab could manufacture cells both with and without these features to determine to the net efficiency gain. The cost of manufacturing the cell would be reduced if either both the back surface field or front surface passivation are eliminated.

3.3 PLAN FOR COST REDUCTION: GaAs CELLS

Processing and material costs comprise a large portion of the cost of GaAs/Ge and GaAs/GaAs cells. This section describes approaches to reduce the cost of GaAs solar cells.

3.3.1 MOCVD Process Cost Reduction

High volume production of GaAs/GaAs and GaAs/Ge cells requires that GaAs MOCVD layers be deposited reproducibly, uniformly and at a low cost over large areas. In the following sections potential cost reductions and cell improvements that result from an improved MOCVD reactor design will be discussed. A summary of the impact of a reduction in MOCVD cost per four inch wafer cost is shown in Figure 3.2. The cost of MOCVD growth on a four inch wafer is expected to be reduced 8 fold by the year 2000.

3.3.1.1 Improved MOCVD Reactor Design

Currently the cost of performing MOCVD growth of GaAs is high. This occurs not only because of the size limitation imposed on existing reactor designs to achieve material uniformity but also because of the gas flows of source gases, TMGa, TMAI etc, in conventional barrel reactor systems. Key to the successful implementation of larger MOCVD systems is the achievement of laminar gas flow over the susceptor area.

In large scale vertical barrel design MOCVD systems, several (up to three) rows of wafers are placed on a "near vertical"

PER 4" WAFER COST

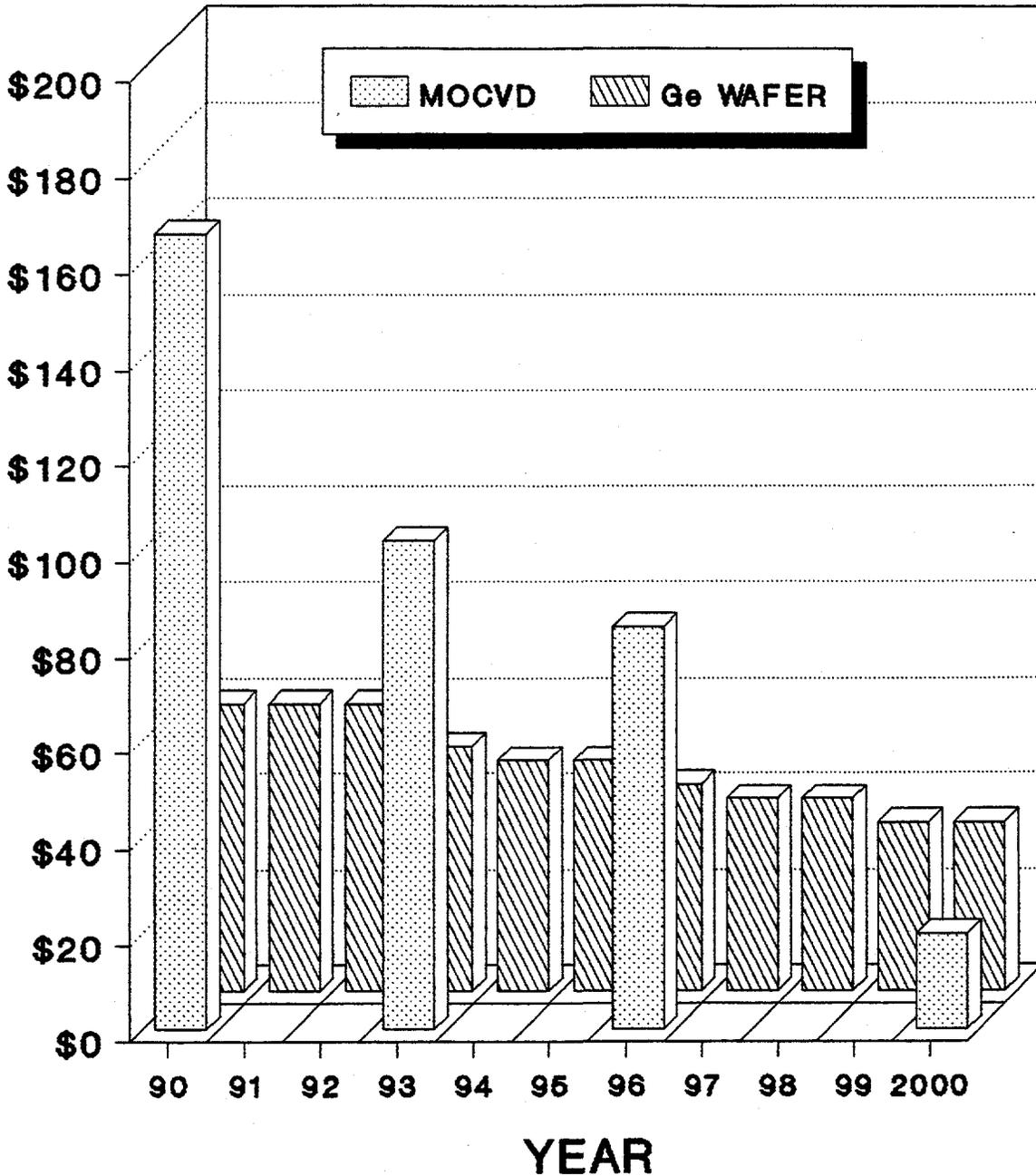


Figure 3.2 IMPACT OF REDUCTION IN MOCVD COST ON FOUR INCH WAFER

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susceptor and dead volumes will act as sources of unwanted materials which cannot be removed easily. This is shown schematically in Figure 3.3. Also during the growth of a sharp heterojunction of a steep doping profile, the original gas composition in the vortices will cause a smearing out of the doping or heterojunction compositional profile making the material unusable for many applications.

In order to achieve compositional, thickness and doping uniformity across the entire three rows of wafers, not only does the requirement for laminar flow have to be met but also the depletion of reactants from the gas flow must be achieved in an orderly manner. Slightly angled susceptor designs assist in this regard but the net requirement is that extremely high hydrogen carrier gas velocities must be used, resulting in poor utilization of metal alkyls and excessive waste of hydrogen.

Based on the above discussion we are convinced that improved MOCVD systems are possible using novel chamber designs to replace barrel systems. We have developed, in conjunction with a major MOCVD equipment manufacturer, an improved high volume, load locked MOCVD system design to replace the conventional barrel design.

Spectrolab will shortly begin the fabrication of this MOCVD system, which is scheduled for delivery in the first quarter of 1992. This machine will be operational by the third quarter of 1992.

3.3.1.2 MOCVD Cost Reduction

Currently the cost of performing MOCVD growth of GaAs is high. This occurs not only because of the size limitation imposed on existing reactor designs to achieve material uniformity but also

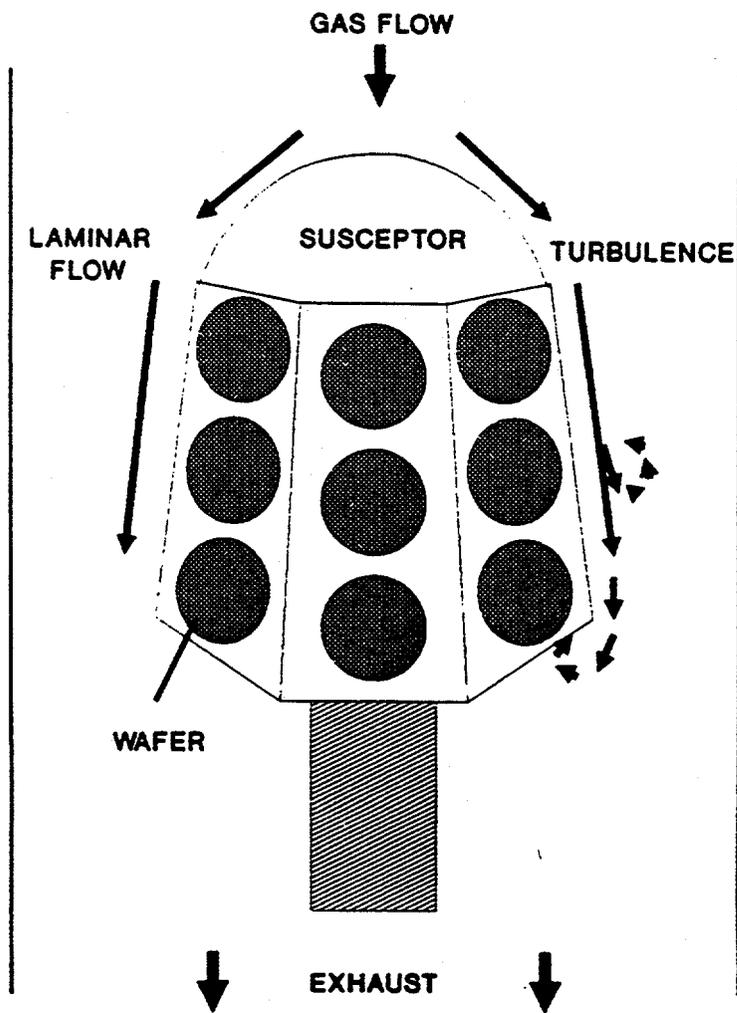


Figure 3.3 BARREL DESIGN MOCVD REACTOR

because of the efficiency of utilization of the metal alkyl source gases. The reactor described in 3.3.1.1 is being designed to meet the need for better source gas utilization to reduce MOCVD costs.

Cost reduction is also obtained by reducing the cycle time. The cycle time will be reduced to 2 hours from 6 hours for a conventional barrel reactor. This is a result of the use of the unique load lock nature of the reactor vessel which is kept under a controlled gas environment at all times. The need to incorporate long bakeout cycles to desorb water vapor from the susceptor prior to growth is eliminated. The quality and reproducibility of MOCVD AlGaAs which is highly reactive with water vapor. This feature improves the device performance since the recombination velocity at the window/emitter interface is a strong function of contamination at that interface.

3.3.2 Wafer Cost Reduction

The cost of the wafer upon which the concentrator cell is grown is a significant portion of the total cell cost. Figures 3.4 and 3.5 show the historical cost of GaAs and Ge substrates to Spectrolab over the last 2 - 3 years. GaAs substrate costs have not fallen significantly in recent years. However, the current cost of approximately \$2.5 /cm² is not inconsistent with cost goals particularly since new ingot growing techniques such as vertical Bridgemen techniques promise to provide additional cost savings. The use of a CLEFT GaAs top cells have also shown potential for GaAs cell cost reduction.

Particularly noticeable from Figure 3.5 is the significant drop in Ge wafer cost during the last 2 years. The current cost of approximately \$1.48/cm² will decrease through improvements to ingot growth and slicing technology. The bulk substrate costs

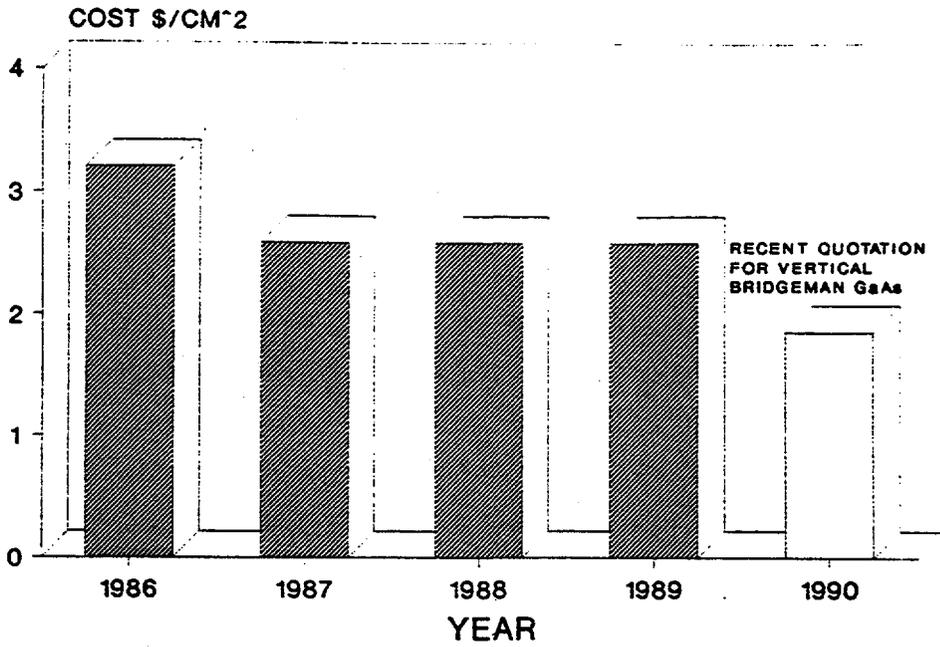


Figure 3.4 HISTORICAL COST OF GaAs SUBSTRATES

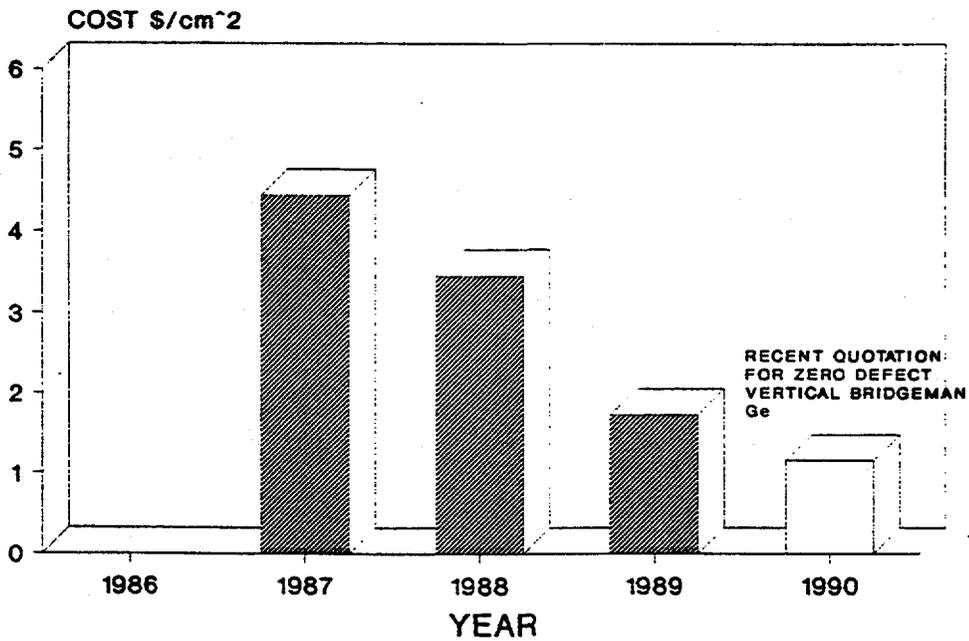


Figure 3.5 HISTORICAL COST OF Ge SUBSTRATES

can be reduced to \$.5 per cm² if a 4" diameter germanium wafer can be used instead of GaAs. Four inch wafers are becoming available and can currently be provided polished at .008" thickness. Substantial cost reductions are also expected as a result of using a four inch diameter wafer compared to 4.5 cm x 4.5 cm. If requested by SERI, Spectrolab will determine the effect of the use of a 4 inch germanium wafer on cell efficiency and processing in Phase 2 of PVMaT. A manufacturing cost analysis for the cell could be performed based on the revised material cost and the known labor standard for 4" diameter silicon processing.

It may become apparent that the use of germanium substrates for GaAs/Ge concentrator cells limits the final efficiency of the cell. In this case, a gallium arsenide substrate may be needed. The increased efficiency may compensate for the higher material cost.

3.3.3 Implementation of Batch Processing

The increased use of automated processing in fabricating GaAs/Ge and GaAs/GaAs cells will reduce the cost of the cell. Processing time and breakage are reduced since individual wafers are not handled.

The GaAs cap etch is currently performed on individual wafers. This is required due to variation in the cap layer thickness and as a consequence the needed etch time. MOCVD layers deposited using the improved MOCVD reactor described in Section 3.3.1.1 will be more uniform than obtained with the reactor currently in use. Consequently, the etch times should be more consistent, and the cap etch could be performed on a lot basis.

Another solution to making the cap etch a batch process is the use of reactive ion etching (RIE). A planar etch system is available at SPL for developing the etch process. Larger scale production would require additional production equipment.

3.3.4 Large Volume Production

The implementation of large volume production of GaAs/GaAs and GaAs/Ge cells would require the use automated equipment in processing. Key processes that are amenable to automation are:

- Wafer Thinning
- Plating
- Cap Etch

Due to the brittle characteristics of gallium arsenide wafers caution is required prior to mechanization to prevent increased breakage. Trade-offs would be made between potentially increased risks of breakage vs increased through-put. The availability of round four inch germanium wafers will aid in the implementation of automation due to the use of standard tooling available for four inch round wafers currently in use for silicon cells.

3.4 PROPOSED CELL DESIGNS FOR IMPROVED EFFICIENCY AND COST

This section will describe several candidate cell designs for improving the performance and reducing the cost of GaAs solar cells. Both single and multijunction cell designs will be discussed.

3.4.1 GaAs Concentrator Cells formed on Germanium Substrates

A candidate structure to meet DOE cost goals is a GaAs concentrator cell fabricated on a germanium substrate. Gallium arsenide concentrator cells have demonstrated an efficiency of 28% at 400X AM1.5 (Ref. 2). Both n/p and p/n cells have shown an efficiency over 25% at moderate concentrations, Figure 3.6. At high concentrations, (1000X), the p/n cell configuration gives an efficiency of 27.5%. Figure 3.7 shows a cross-section of the n/p and p/n cell developed at Varian. This structure would be modified for growth on four inch germanium substrates. Technical issues regarding the use of germanium substrates at these concentrations, such as the formation of a tunnel junction and material morphology, may limit the final efficiency of the cell.

The elimination of the GaAs wafer will reduce the cost of GaAs solar cells. As described in Section 3.3, the cost of a GaAs/Ge concentrator cell can be reduced dramatically through the use of improved reactor technology, four inch germanium wafers and implementation of batch processing. Current projections for the cost per cm^2 in the year 2000 assuming 1MW production is roughly $\$2.5/\text{cm}^2$. At an anticipated efficiency of 26 to 28% at 200X AM0 the GaAs/Ge concentrator will meet the DOE cost goals.

3.4.2 GaAs/GaAs Concentrator Cells

GaAs concentrator cells formed on GaAs substrates also show potential for meeting the DOE cost goals. The gallium arsenide concentrator could be constructed in the n/p or p/n configuration, as described in section 3.4.1. The use of high concentrations (1000X) will allow the GaAs/GaAs cell to be cost competitive. GaAs 1000X concentrator modules have been demonstrated with an efficiency of 22.7% (Ref.3).

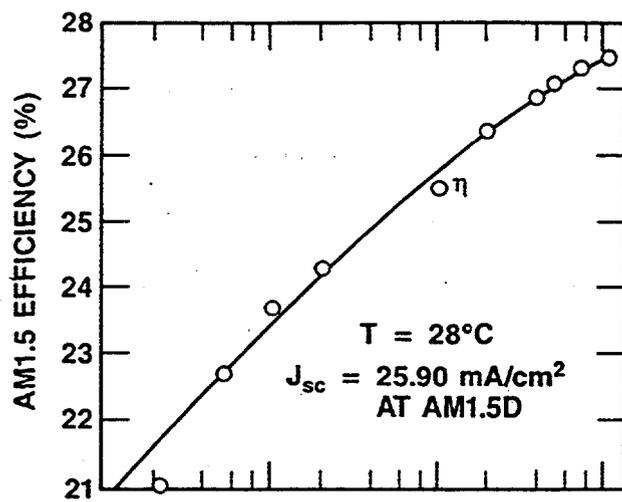
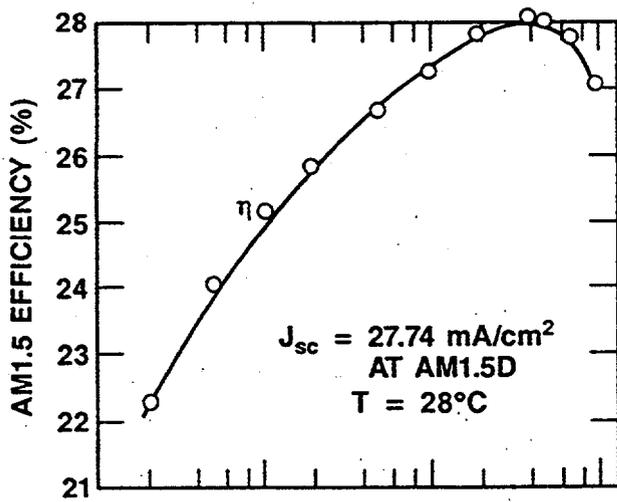


Figure 3.6 PERFORMANCE OF GaAs CELLS IN n/p AND p/n AT MODERATE CONCENTRATIONS (MacMillan)

FRONT CONTACT		
0.6 μm	GaAs n^+ (p^+)	AR COATING
400 \AA	$\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$	WINDOW
0.2 μm	GaAs $1 \times 10^{18} n$ ($0.7 \mu\text{m}$ $2.5 \times 10^{18} p$)	EMITTER
3.8 μm	GaAs p (n) 5×10^{17}	BASE
0.2 μm	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	MIRROR
0.6 μm	GaAs	BUFFER
350 μm	GaAs	SUBSTRATE
BACK CONTACT		

Figure 3.7 CROSS-SECTION OF VARIAN n/p AND p/n CELLS

The cost of the GaAs substrate and unavailability of 4 inch GaAs substrates makes this a less desirable choice than GaAs/Ge concentrators. However if technological problems associated with the germanium substrate (Section 3.6.2) prove insurmountable this may be the most cost effective GaAs Cell.

3.4.3 Silicon Concentrator Cell

Studies show that silicon concentrator cells can indeed meet the short term DOE goals. They also have great potential to meet the long term goal of \$.06kWH. The basic design of a low resistivity concentrator would be optimized for operation at 200X. An efficiency of 20% AM1.5 is anticipated. Figure 2.5 shows a cross-section of the cell design. The process flow is described in Section 2.3.

3.4.4 Multijunction Concentrator Mechanically Stacked Cell

Our projections show that high efficiency mechanically stacked cells have the potential to be manufactured cost effectively. In Figure 3.8 we show a cross-section of a voltage matched GaAs/Ge cell combination consisting of one GaAs cell and four Ge cells. We have conservatively modeled this cell at 33% efficiency at 200X, AM1.5D. The cell assembly could also be operated at higher concentration with approximately the same efficiency allowing it to meet DOE cost goals. The cell can be assembled using hybrid technology already demonstrated at Spectrolab on concentrator cell receivers (Section 2.7.1) and stacked GaAs on Si cells (Section 2.7.2). Figure 3.9 shows schematically the fabrication sequence for assembly. The conducting layers are defined on an insulating substrate, germanium cells are bonded onto the substrates and interconnected, finally the top GaAs cell is attached.

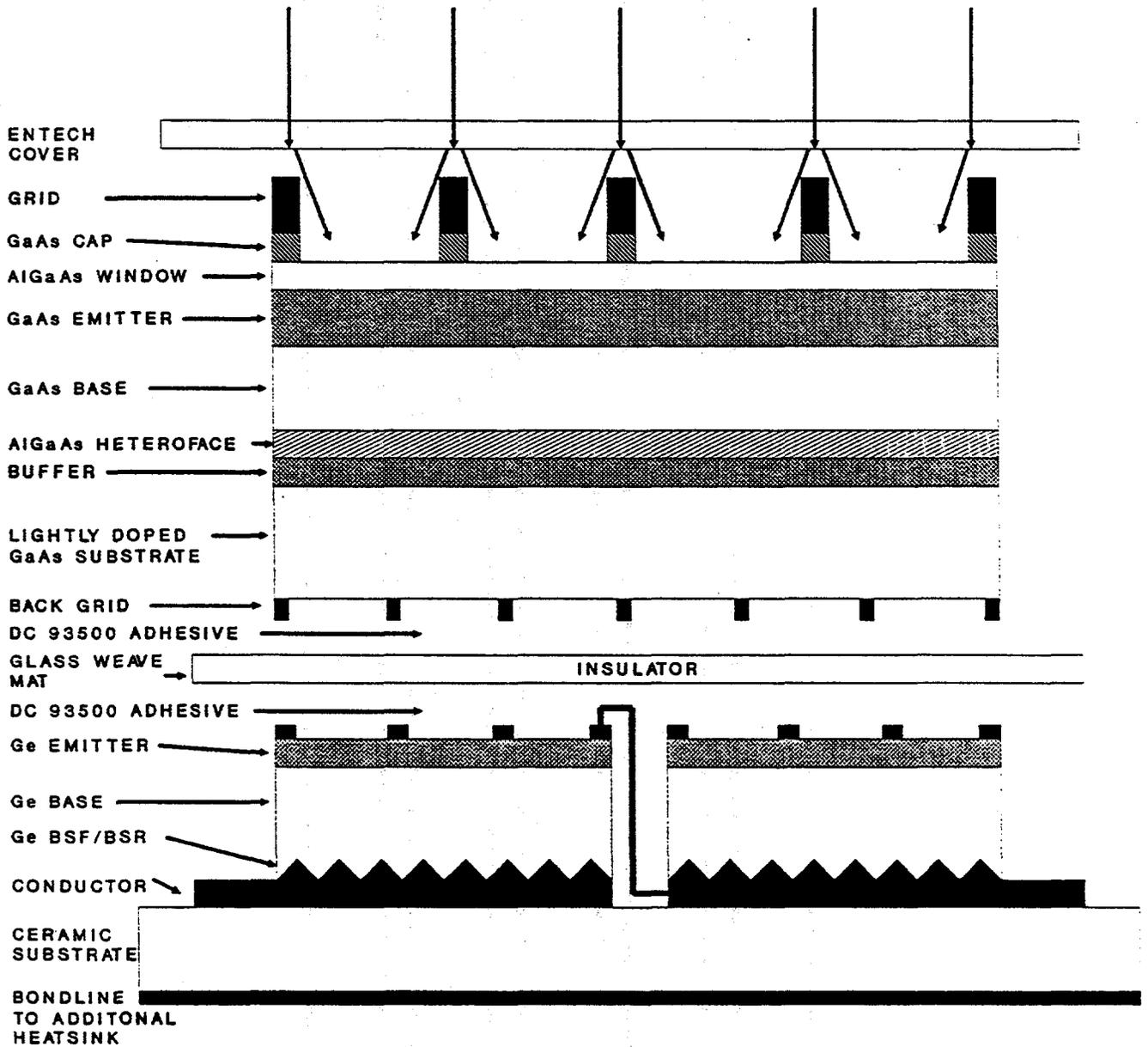
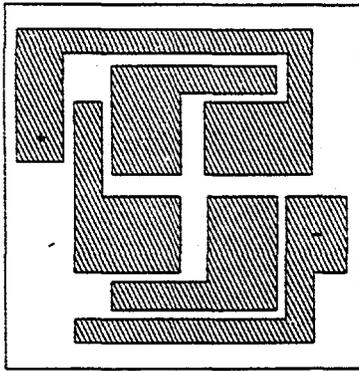


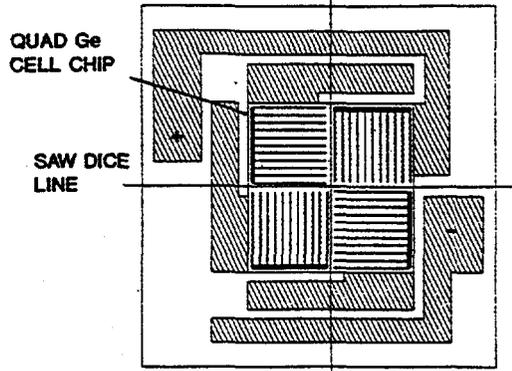
Figure 3.8 CROSS-SECTION OF VOLTAGE MATECH GaAs/Ge STACK

ALUMINUM OXIDE OR ALUMINUM NITRIDE CERAMIC SUBSTRATE



STEP 1. DEFINE CONDUCTORS ON INSULATING SUBSTRATE

SAW DICE LINE

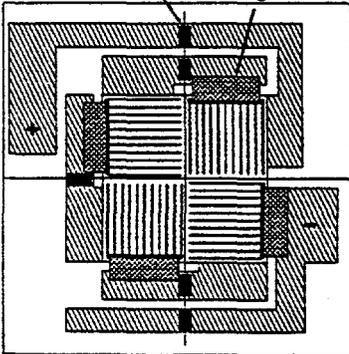


STEP 2. BOND Ge CHIP TO SUBSTRATE

STEP 3. DICE TO ISOLATE Ge CELLS

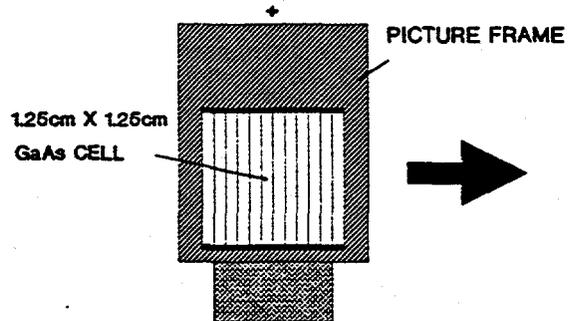
TRACK REPAIR

SERIES INTERCONNECTION BY WELDED Ag MESH OR Ag WIRE BALL BONDING



STEP 4. REPAIR BROKEN TRACKS

STEP 5. SERIES INTERCONNECT Ge CELLS USING Ag MESH OR BALL BONDING



STEP 6. ATTACH PICTURE FRAME TO GRIDDED BACK GaAs CELL

Figure 3.9 FABRICATION SEQUENCE FOR MECHANICAL STACK

The germanium cell would be processed in a similar fashion as standard silicon cells. Problems particular to germanium cell manufacture are discussed in Section 4.3.2. Germanium cells would be optimized to operate at a concentration ratio of 200X AM1.5D under a gridded GaAs cell. The efficiency goal is 5% minimum at an operating voltage of .25V. Four germanium cells would be connected in series to give an operating voltage of 1.0V. The germanium cell could be optimized for use at a higher concentration ratio if desired.

Silicon cells could be used in place of the germanium cells. The efficiency goal for a silicon bottom cell is 3% under GaAs. The silicon cell has the advantage of a lower material cost and known processing. This cell will probably cost approximately the same as the concentrator cell under development described in sections 2.1.4 and 2.3, \$1.7/cm². Currently the processes for germanium cell fabrication are under development at Spectrolab.

The top cell will be constructed from a low cost high efficiency GaAs cell, designed to operate at 200X AM1.5D. The cell would be designed to maximize light transmission into the underlying Ge cells without sacrificing top cell efficiency. The efficiency goal of this cell is 28% at the maximum power point of 1V. The top cell could also be designed to operate at higher concentrations if needed to meet the cost requirements. The cost of the GaAs cell will be determined in part by the cost of GaAs. If the current cost of \$2/cm² is used, and MOCVD improvements and batch processing techniques as described earlier are implemented, then the cost for the top cell will be approximately \$4.25/cm².

To determine the approximate cost of the mechanical stack, values for individual cells are combined and the interconnection costs are estimated. A dual cell concentrator utilizing GaAs

and Silicon cells will cost approximately \$6/cm² for the cells alone. Interconnection and substrate costs will add to the final cost. At high concentrations allowable cell cost can be as high as \$12/cm² and still meet the DOE cost goals. Therefore the mechanical stack provides a viable alternative for meeting the cost goals.

3.4.5 Other Multijunction Cell Designs

Spectrolab is also developing concepts for multijunction cell assemblies in which the problems due to thermal dissipation and MOCVD material compatibility in a monolithic stack are eliminated. The design is currently the subject of a patent submission and is not disclosed here. This technique allows each cell to be independently optimized and allows the choice of many more cell combinations since current matching is no longer required. A prototype constructed using GaAs and Si cells obtained 21% AMO efficiency at one sun concentration. Modeling performed on a GaAs/Si/Ge assembly predicts a total efficiency of 32% at 300X AM1.5D. At higher concentrations it is anticipated that the assembly will have a comparable or better efficiency. As part of phase 2 of the PVMat program, Spectrolab suggests that a trade study be performed to determine the cost and efficiency benefits of several different multijunction cell designs against the single junction GaAs/GaAs, GaAs/Ge and Si concentrator cells.

4.0 POTENTIAL PROBLEMS AND ROADBLOCKS TO ACHIEVING GOALS

The gallium arsenide, germanium and silicon solar cells and assemblies designs described in task 2 present Spectrolab with challenges in their development and implementation. Potential problems include cell development, interconnection and environmental issues. Some of these points have already been mentioned in section 3, further discussion of roadblocks will be discussed within this section.

4.1 GaAs PROCESSING

Two major issues will be addressed to reduce the cost of GaAs processing. These are GaAs MOCVD growth cost and uniformity improvements, and the implementation of automated batch processing to GaAs cell processing. Both of these issues will be addressed in this section.

4.1.1 MOCVD Growth Characteristics

Key to the implementation of cost savings and efficiency improvements is the installation of a improved MOCVD reactor, as described in Section 3.3.1. Thickness and doping uniformity are required from wafer to wafer and across a four inch wafer. Spectrolab's planned purchase of this reactor is crucial to meeting these requirements.

On receipt from the manufacturer, MOCVD growth engineers at MPD will perform experiments to verify system performance. In particular, we will work to produce GaAs layers with uniform doping and thickness. In addition work to determine the tolerable amount of non-uniformity allowable in the GaAs growth will be performed.

4.1.2 Batch Processing

Germanium Substrates

As discussed in Sections 3.3.3 and 3.3.4 batch processing is essential to meet cost goals for the production of GaAs solar cells. The use of four inch germanium wafers facilitates the use of batch processing and permits the use of the equipment developed for silicon cell manufacture.

GaAs Substrates

GaAs substrates are much more delicate than germanium substrates and require additional care in handling. When the GaAs substrate is thinned it becomes particularly susceptible to breakage. In order to implement automated batch processing new fixturing needs to be designed, purchased and tested. We may find that even with new fixturing the thin GaAs substrates are too fragile for automated processing.

Cap Etch

The cap etching step may be simplified by the use of Reactive Ion Etching (RIE). This process may be easier to adapt to batch processing than the current wet etching process. RIE of GaAs layers uses Freon based gases that are highly regulated due to their environmental effects. The Air Quality Management District (AQMD) of Los Angeles County and Federal environmental agencies limit the amount of these materials in use. These issues would need to be resolved prior to implementing large scale processing.

4.2 GERMANIUM WAFER READINESS

Key to the cost reduction of GaAs/Ge cells is the availability of high quality, large area germanium substrates. Spectrolab has funded the development of four inch diameter germanium wafers at

Crysteco. This program demonstrated the feasibility of Cz four inch germanium. Slippage was identified as a problem in the growth of large diameter wafers. Proper control of the growth and temperature resulted in four inch diameter sliced and polished wafers. The etch pit density of the wafers was non-uniform, though there were regions with less than 10^4 EPD.

Improvements in growth and slicing methods are needed to obtain high quality, large area germanium wafers. Germanium manufacturers are investigating growth on the <100> crystal plane using vertical bridgeman and liquid encapsulated Cz techniques. They are also attempting to reduce the thickness of the wafer through the use of wire saws. This technique would replace the current inner diameter slicing method and would reduce the amount of kerf loss during the slicing process.

4.3 MULTIJUNCTION CELL COMPONENT CELL DESIGN

4.3.1 GaAs Cell Optimization

In the multijunction cell the top GaAs cell produces approximately 80% of the total power. To meet the efficiency goals of the cell, it is essential that the GaAs cell be produced from high quality materials and be properly designed to extract the maximum energy from incident light. Features that are important to study and optimize are:

1. Antireflective coating to couple .35 - 1.85 micron energy into the cells.
2. Optimized front and back collector to minimize transmission losses.
3. Back surface reflector/scavenging AlGaAs layer to increase minority carrier lifetime.

4. Transparent GaAs substrate to transmit below GaAs band edge energy.
5. Dielectric coating on the back to couple unused photons out of the GaAs cell.

A candidate cell cross-section is shown in Figure 4.1. Each of these items would be studied to determine the best solution.

4.3.2 Germanium Cell Optimization

The proposed multijunction design requires the fabrication of a high quality germanium cell. Spectrolab has been actively developing germanium cells under other programs. A cross-section of a candidate germanium cell is shown in Figure 4.2. The important elements of this structure are:

1. A 4-5 mil thick germanium substrate.
2. A diffused, implanted or epitaxially grown emitter region, forming the PN junction.
3. A Back Surface Field (BSF) region
4. A Back Surface Reflector (BSR) for enhancement of photon absorption around the Ge band gap.
5. Antireflective coating optimized for maximum current generation in the germanium cell.

Germanium Wafer

Firstly, the quality of the germanium wafer is critical to the cell performance. Spectrolab's procurement specification requires an etch pit density of less than 10^4 cm^{-2} .

However our experience to date is that it can be substantially higher on certain parts of the wafer surface making large area cell fabrication difficult. The doping type of the base can be either p or n type. P-type material has the advantage of the availability of phosphorus diffusion process for n+ junction formation.

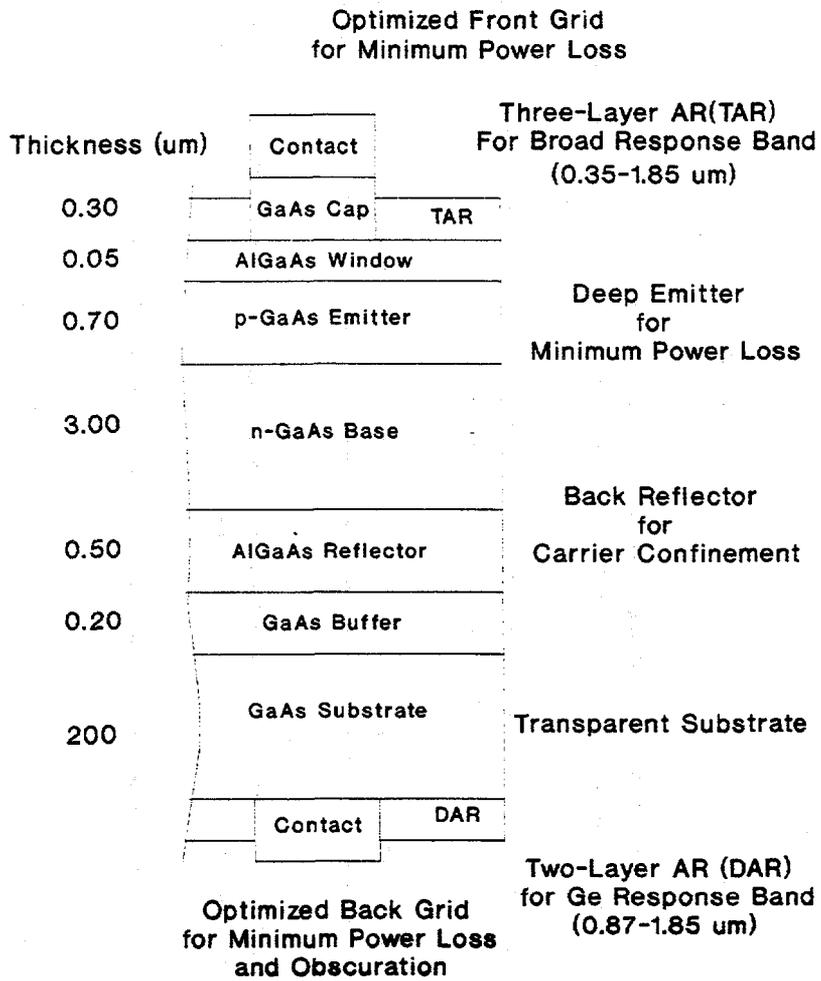


Figure 4.1 CROSS-SECTION OF CANDIDATE GaAs TOP CELL STRUCTURE

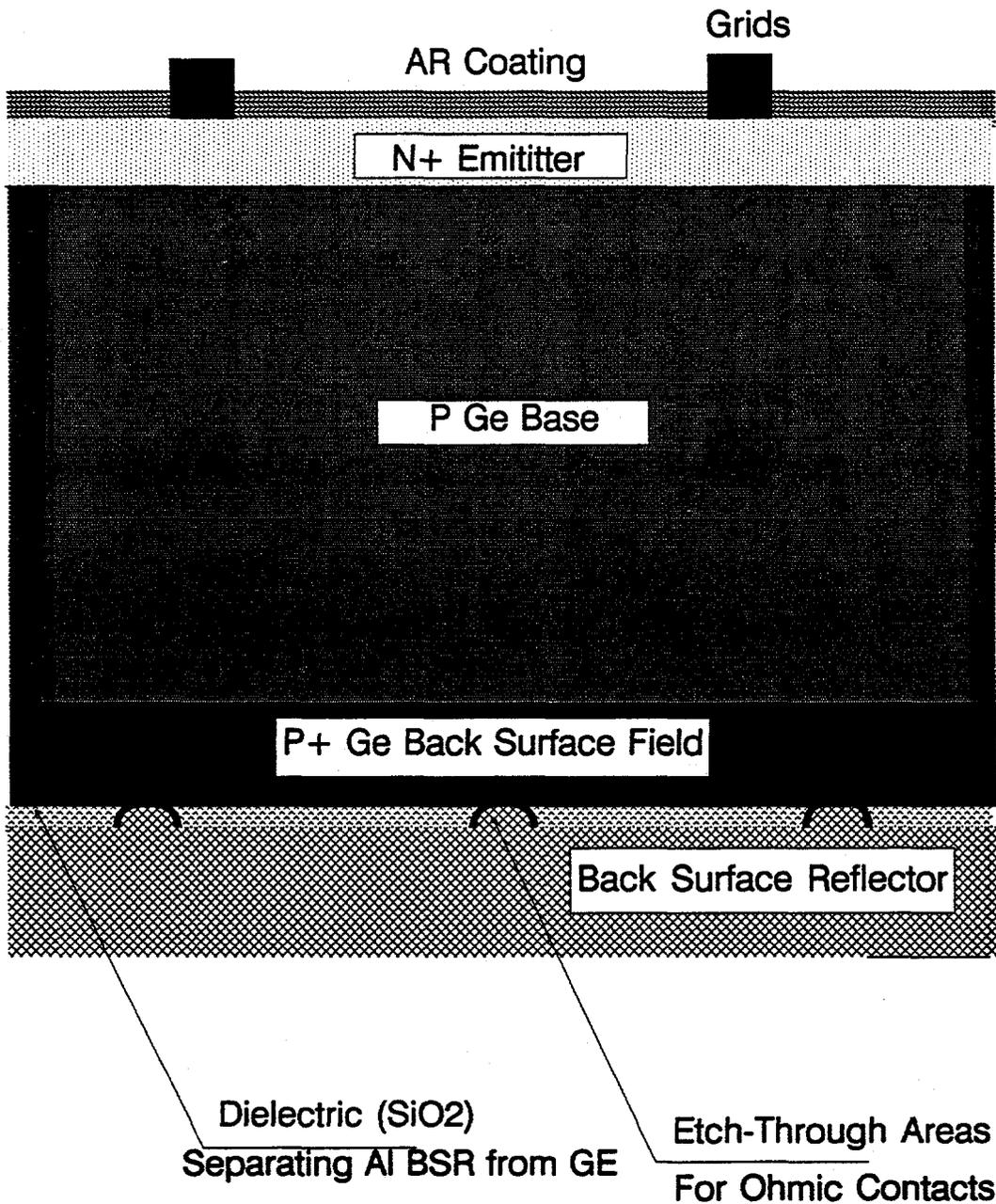


Figure 4.2 CROSS-SECTION OF CANDIDATE Ge CELL

Diffusion Length

The germanium minority carrier diffusion length also has a dominant influence on this device especially in the red end of the spectrum. In Figure 4.3 we demonstrate the influence of germanium base diffusion length and surface recombination velocity on the internal quantum efficiency. A high diffusion length of at least 50 microns is required in order to maintain good quantum efficiency near the germanium band edge.

Surface Recombination

Surface/Interface recombination processes play an important role in determining Voc and Isc parameters. Figure 4.4 shows the influence of surface recombination velocity on germanium cell efficiency under a GaAs filter for 200X AM1.5 illumination. A recombination velocity of less than 10^4 cm/sec is required for high efficiency to be achieved.

Emitter Depth Effects

Germanium cell performance is effected by the emitter depth. Figure 4.5 shows modeled performance of germanium cells under GaAs filtered 200X AM1.5. A thin junction primarily improves current generation. Methods to create a thin highly doped junction will be investigated.

Light Trapping

Light trapping is incorporated in the front of the Ge cell through the use of texturing and at the back from a back surface reflector. The methods of texturing for silicon cells cannot be applied directly to germanium cells due to differences in the chemistry of the materials. Preliminary etching experiments performed at Spectrolab have demonstrated that standard silicon anisotropic etches do not work for germanium. Additional work needs to focus on developing appropriate etches for germanium.

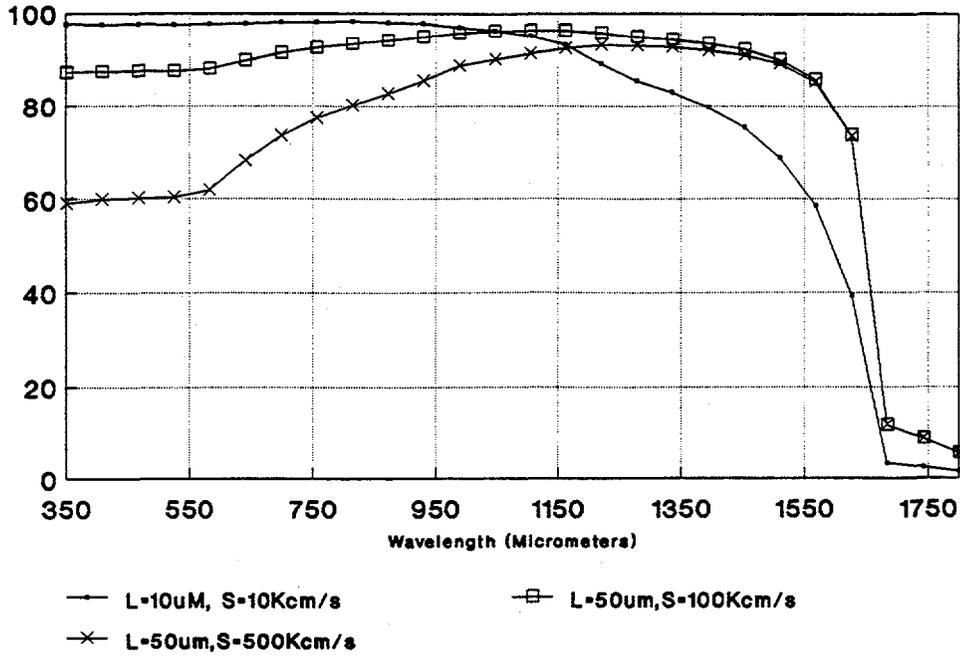


Figure 4.3 EFFECT OF DIFFUSION LENGTH ON Ge CELL QUANTUM EFFICIENCY

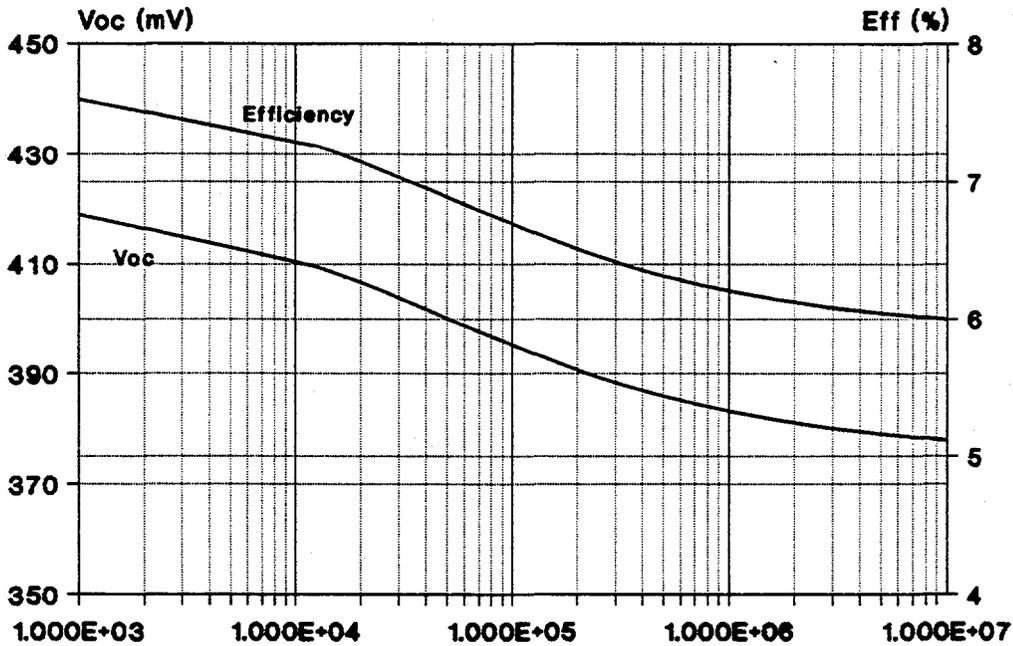


Figure 4.4 EFFECT OF SURFACE RECOMBINATION ON Ge PERFORMANCE

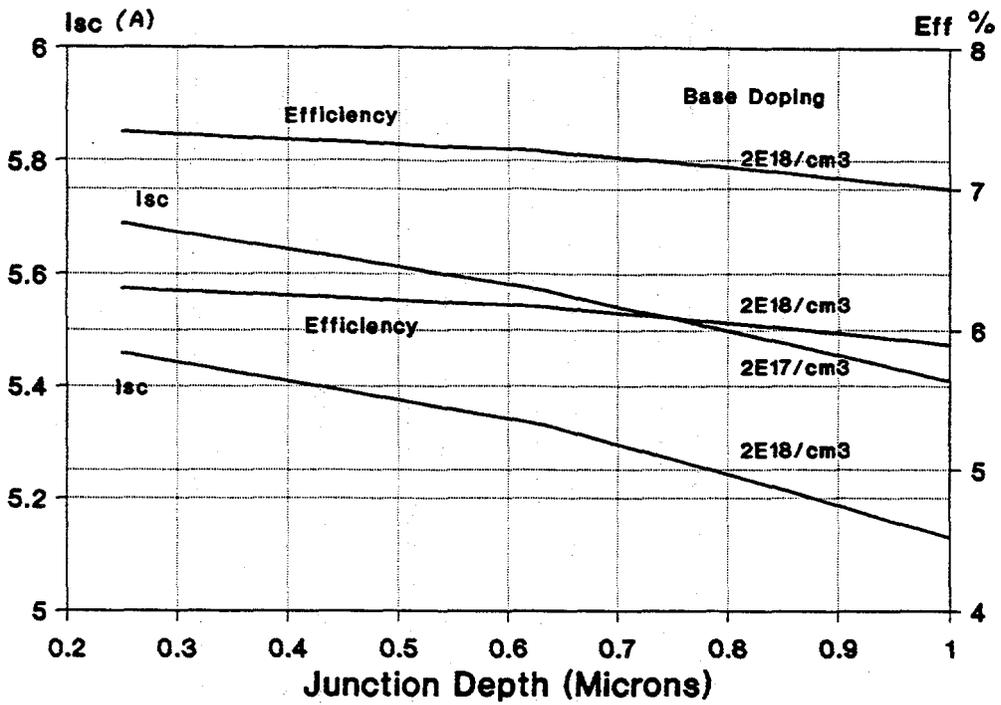


Figure 4.5 EFFECT OF EMITTER DEPTH ON Ge PERFORMANCE

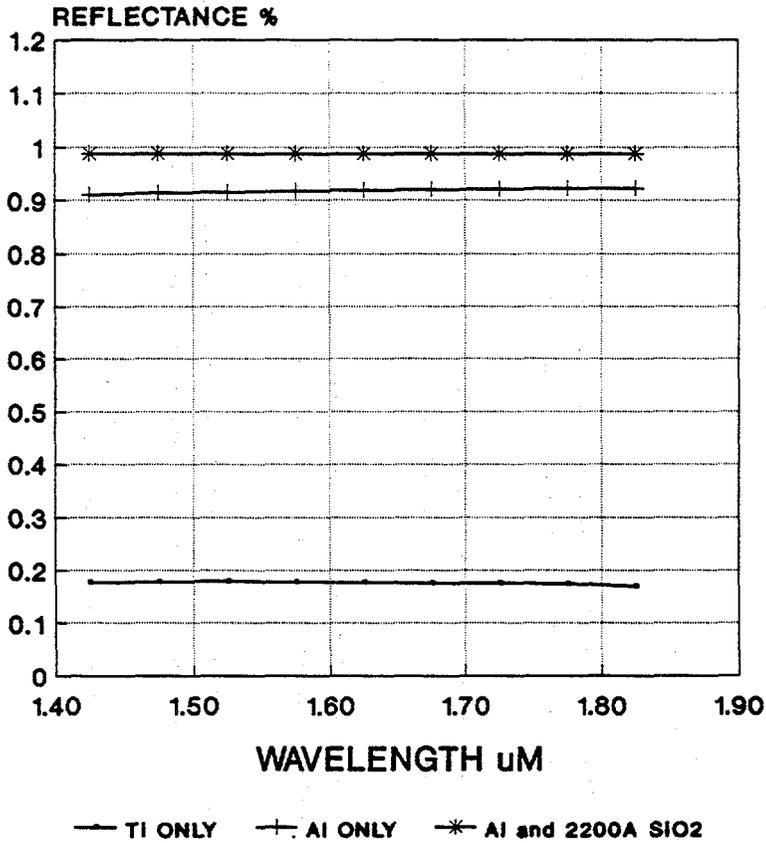


Figure 4.6 COMPUTED REFLECTANCE FROM BACK WITH Ti AND Al REFLECTOR

Spectrolab has modeled the effect of various back surface reflectors on the germanium cell. The back surface reflector is important because germanium is weakly absorbing beyond 1.5 microns wavelength. The computed reflectance from the back contact when a titanium or aluminum reflector is used is shown in Figure 4.6.

4.3.3 Silicon Cell Optimization

A silicon cell could be used as a middle cell in a three junction cell or the second cell in a dual-junction cell. This cell would be designed to maximize the absorption of the I.R.

Texturing

Texturing of the surfaces may be used to increase current generation of the silicon cell. Space applications commonly require chemical texturing process. In this process a mixture of 2-propanal and NaOH anisotropically etches the surfaces. Increased production of textured cells will require the approval of local environmental agencies to use the quantities of 2-propanal required. Spectrolab production planners will allow for at least 6 months permitting time in their projections.

Cell Design

The basic cell design for a silicon concentrator cell was described in Sections 2.1.4 and 2.3. When used as a bottom cell, some features may need to be changed to maximize absorption of the I.R. These include: substrate thickness, substrate resistivity, antireflective coating, texturing, emitter profile, back reflector and back surface field. The chose of the optimal design will take into consideration the additional cost vs. the marginal efficiency improvement.

4.4 STACKED MULTIJUNCTION CELL INTERCONNECTION AND PACKAGING

The design of the multijunction cell should be compatible with current module designs for mid or high concentration modules. This facilitates a "plug-in" high efficiency replacement for current technology cells. Figure 4.7 shows a cross-section of a candidate cell package. This design consists of four Ge bottom cells and one GaAs top cell.

4.4.1 Bottom Cells Interconnection

Various interconnection techniques would be investigated in a pre-production phase. The bottom germanium cells are bonded to a ceramic substrate. The choice of the ceramic would be based on cost and thermal conductivity. The top to the substrate would be patterned, using .25 mm of bonded copper, with the cell bond pads and interconnect scheme shown in Figure 4.8. Alternatively the conductors may be a thick film silver, since 10 mil silver conductors are possible using multiple screen printing techniques.

When the germanium cell is bonded to the ceramic substrate it will have the configuration shown in Figure 4.9. Each chip will have four mesa isolated cell structures. After bonding, the germanium cell will be physically and electrically separated into four individual cells by dicing through the ceramic substrate. This should be more cost effective than bonding individual cells since only one cell needs to be handled when bonding.

The series connection of the germanium bottom cells is shown in Figure 4.10. One potential material is silver wire mesh soldered or welded to the top bus of each cell and then to the base pad of the cell adjacent to it.

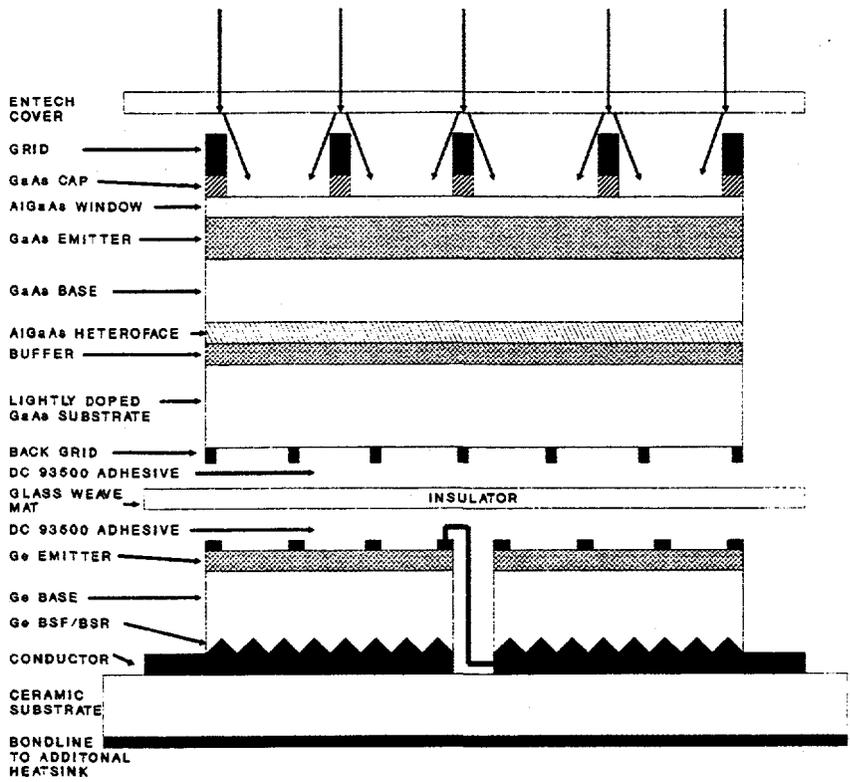


Figure 4.7 CROSS-SECTION OF GaAs/Ge STACKED CONCENTRATOR

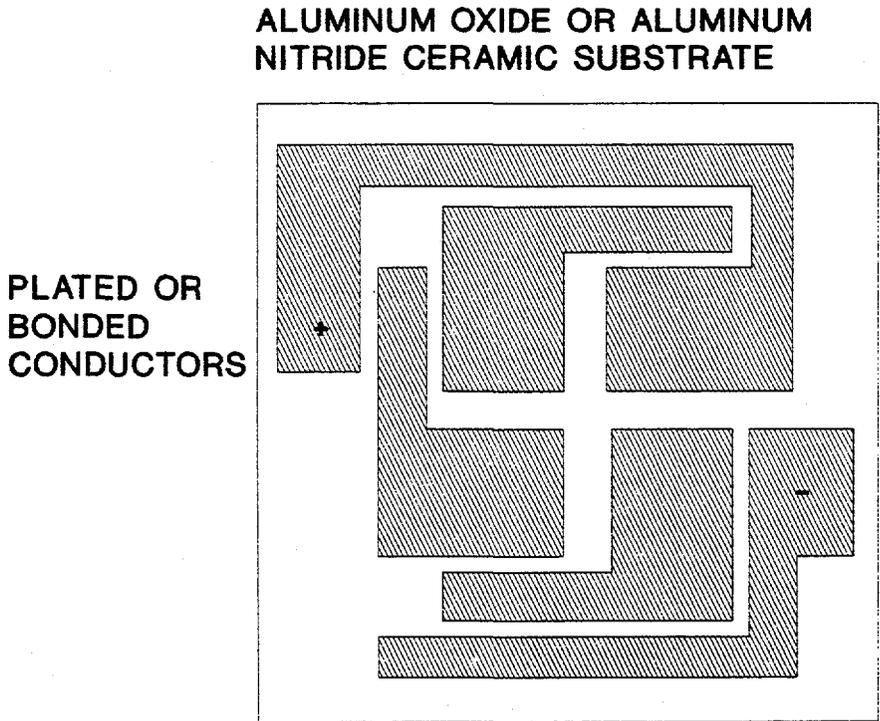


Figure 4.8 SUBSTRATE PATTERNING

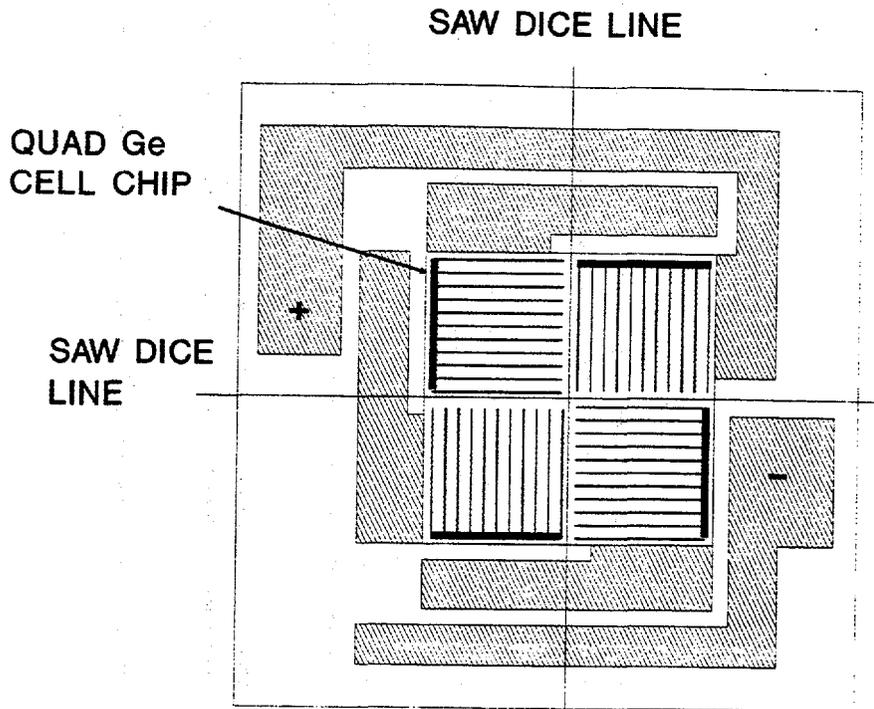


Figure 4.9 BONDING OF Ge CELL TO SUBSTRATE

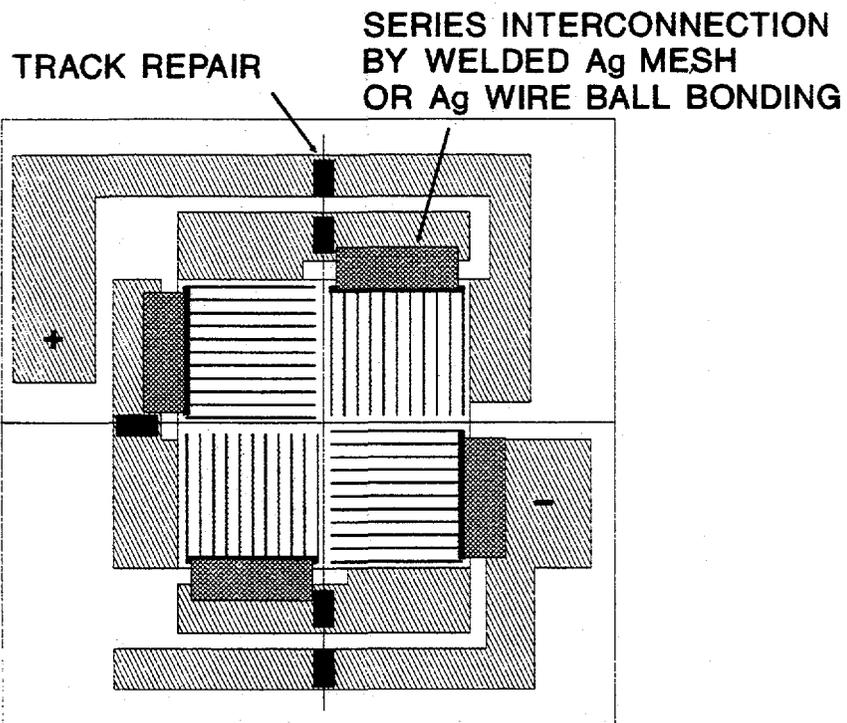


Figure 4.10 SERIES CONNECTION OF Ge CELL

4.4.2 Top and Bottom Cell Interconnection

Techniques to attach the top GaAs cell to the bottom cells must fulfill the following requirements:

1. Good adhesion of one cell to another without failing during thermal cycling.
2. Provide good transmission of light energy from the top cell to the bottom cells.
3. Provide electrical insulation between the stacked cells.
4. Allow for thermal conduction from the top to the bottom cells.
5. Perform interconnection in the most cost effective way, to minimize the cost of the cell.

One proposed method for attaching the top cell to the bottom cells is shown in Figure 4.7. The glass or quartz cloth between the two cells will allow for good electrical isolation and excellent adhesion. DC93-500 adhesive has very good optical transmission over the wavelengths of interest. Another method for providing good electrical separation of the top and bottom cells would be the use of a glass coverslide.

Prior to bonding the GaAs cell to the Ge bottom cells, silver interconnects will have been soldered to each bus on the front and back as shown in Figure 4.11. A "picture frame" arrangement could be used for both top and bottom contacts thus allowing current to be drawn from each end of the grid. The completed GaAs/Ge concentrator assembly is shown in Figure 4.12.

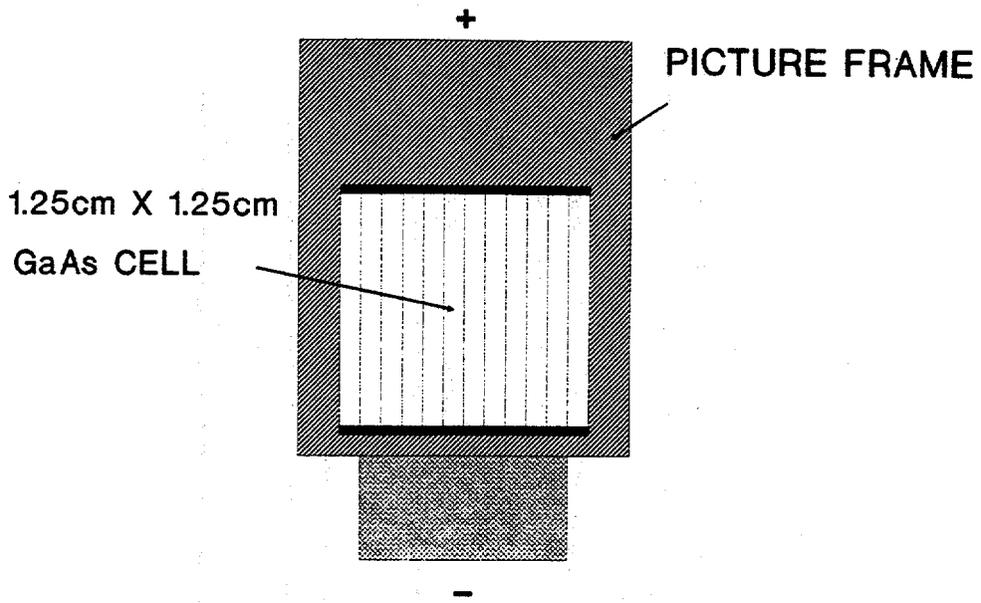


Figure 4.11 "PICTURE FRAME" ARRANGEMENT FOR TOP AND BOTTOM CONTACTS

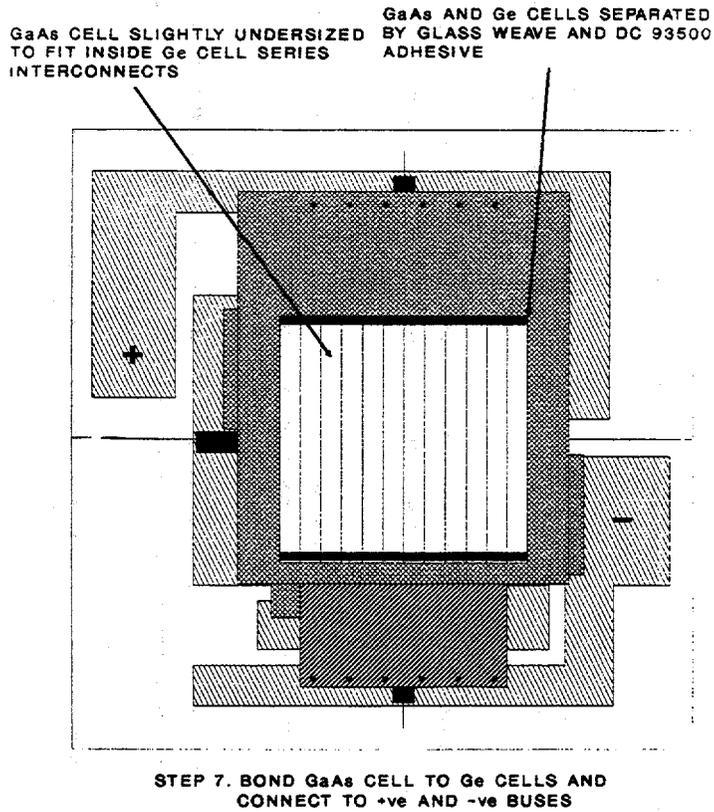


Figure 4.12 COMPLETED GaAs/Ge CONCENTRATOR ASSEMBLY

4.4.3 Compatibility with Module Manufacturers

The above described design is compatible with current concentrator module technology. At this time, concentrator modules for concentrations greater than 150 suns consist of a metal housing which supports the concentrating fresnel lens over the cell package mounted directly beneath it. The cell package typically consists of the cell, an alumina substrate (for cell to cell interconnection) and a copper heat spreader to dissipate heat away from the cell, all bonded together. The heat spreader is usually then bonded to the module base which anchors the assembly in place and helps to further dissipate heat away from the cell. A secondary optical element (SOE) is then bonded to the cell to redirect stray flux into the cell.

The cell assembly will consist of the mechanically stacked GaAs/Ge or GaAs/Si cell bonded to a ceramic substrate for interconnection. The assembly can then be provided to the module manufacturer who will then integrate the assembly into a cell package which includes the heat spreader and SOE. Spectrolab will consult with a module manufacturer to ensure that the cell assembly design is compatible with their design. Since multijunction cell assemblies must be operated at high concentration to mitigate their relatively high cost, module manufacturers may need to modify their current design to handle the higher currents and the heating produced.

4.4.4 Environmental Stability

Many unanswered questions remain regarding the environmental stability of the mechanical stack assembly. The reliability of the interconnection techniques proposed is untested. Environmental tests may reveal reliability issues that need to be addressed.

Sandia, in "Qualification Tests for Photovoltaic Concentrator Cell Assemblies and Modules" (Ref. 4), describes several tests for cell assemblies. Potential tests include thermal cycling, humidity testing and hi-pot tests. If the assembly does not pass, it would be evaluated for the cause of the failure and appropriate changes made to the cell design.

4.6 GaAs/Ge AND GaAs/GaAs CONCENTRATOR CELL

4.6.1 Processing Issues

Substrate

The use of high quality four inch diameter germanium wafers will reduce the cost of a GaAs/Ge solar cell by decreasing the substrate cost and will facilitate the implementation of batch processing. Section 4.2 describes work currently underway at germanium manufacturers to fabricate high quality large area germanium.

Cells fabricated on a GaAs substrate will cost more than those made on germanium substrate due to the higher material cost. However, if a GaAs substrate is required for high efficiency cells the cost may be offset by the resulting higher performance.

MOCVD Issues

The cost and efficiency of GaAs/Ge and GaAs/GaAs concentrator cells are effected by the MOCVD growth characteristics and the implementation of batch processing as described in Sections 4.1.1 and 4.1.2 respectively. MOCVD growth uniformity is crucial for successful batch processing, especially for sensitive etching processes such as the cap etch process.

Metallization Design

The grid design is dictated by the desire to maximize the current generated while minimizing the series resistance. Spectrolab has developed grid design programs to determine the optimal metallization pattern.

At concentration levels of 200X or higher, we may find that the metal coverage is high enough so that the cell would benefit from the use of an prismatic coverglass (Ref. 5). The use of a prismatic coverglass allows a greater metal coverage to be used without sacrificing the current generated by redirecting light rays that would hit a grid line to active area. In this instance a trade study would be performed to determine if the marginal efficiency increase is worth the increase in cost.

4.6.2 Effect of Germanium Substrate on Performance

Germanium wafers are routinely used as substrates for one sun GaAs/Ge solar cells. The electrical performance of these cells is comparable to GaAs cells grown on GaAs substrates. For one sun operation, series resistance at the GaAs/Ge interface does not degrade the solar cell's performance. It may be found that series resistance becomes a factor when an higher current density is generated.

4.7 STAND-ALONE SILICON CONCENTRATOR CELL

4.7.1 Sculpturing Process

Spectrolab has developed a sculpturing process that results in a textured surface silicon. A major component of this etch is 2-propanol. Isopropanol alcohol is a volatile organic compound and its use is regulated by the Air Quality Management Board

(AQMD). If large numbers of cells were produced, Spectrolab would be required to apply for additional permits to allow an increase in the use of isopropanol alcohol. The application process could delay the start of large scale production of this product.

4.8 ENVIRONMENTAL STABILITY

Solar cells have been developed at Spectrolab that are reliable in the harsh space environment. The tests performed for space conditions are different than those used to verify terrestrial reliability. In many cases the tests are similar enough that one can assume that the cells would pass the terrestrial tests.

Below are typical environmental tests and conditions that may apply to terrestrial conditions:

Test	Conditions	Pass
1. Temperature Cycling	-80 to 100C	<3 % degradation
2. Humidity	95% RH, 45C, 30 days	< 3 % degradation
3. Pull Test	welded or soldered tabs pulled	

Prototype cells would be prepared to verify that they pass the relevant tests outlined in "Qualification Tests for Photovoltaic Concentrator Cell Assemblies and Modules" (Ref. 4).

5.0 TASK 4 APPROACHES AND SOLUTIONS TO PROBLEMS

In Section 4.0, problems related to meeting the cost and efficiency goals were discussed.

In this section we describe the development and manufacturing technology approaches which we believe should be undertaken both in the near and long term in order to solve these problems and assure the viability of photovoltaics for terrestrial applications. The approximate level of effort required (in man months) and the program schedule outline are shown in Figure 5-1.

A promising technology for meeting the DOE cost goals in the near to intermediate term is GaAs/Ge. GaAs/Ge technology has been matured to production over the last two years and several hundred thousand GaAs/Ge planar space cells have been built within the U.S. in a production environment. Although current estimates for GaAs/Ge cells do not meet the DOE cost goals we believe that a manufacturing technology program directed specifically toward reducing the cost of MOCVD growth in addition to certain specific processing areas would enable the DOE goals to be attained.

Given the encouraging work currently being performed by many R&D laboratories, it is also likely that efficiencies well in excess of 30% will be provided through the use of concentrator multijunction cells based on III-V materials. Our belief is that multijunction cells will be mechanically stacked in the near term and probably monolithic in the long term although there are still substantial hurdles to be overcome to achieve current and lattice matching in the volume production of monolithic devices.

TECHNOLOGY ROADMAP FOR TERRESTRIAL PV PRODUCTION

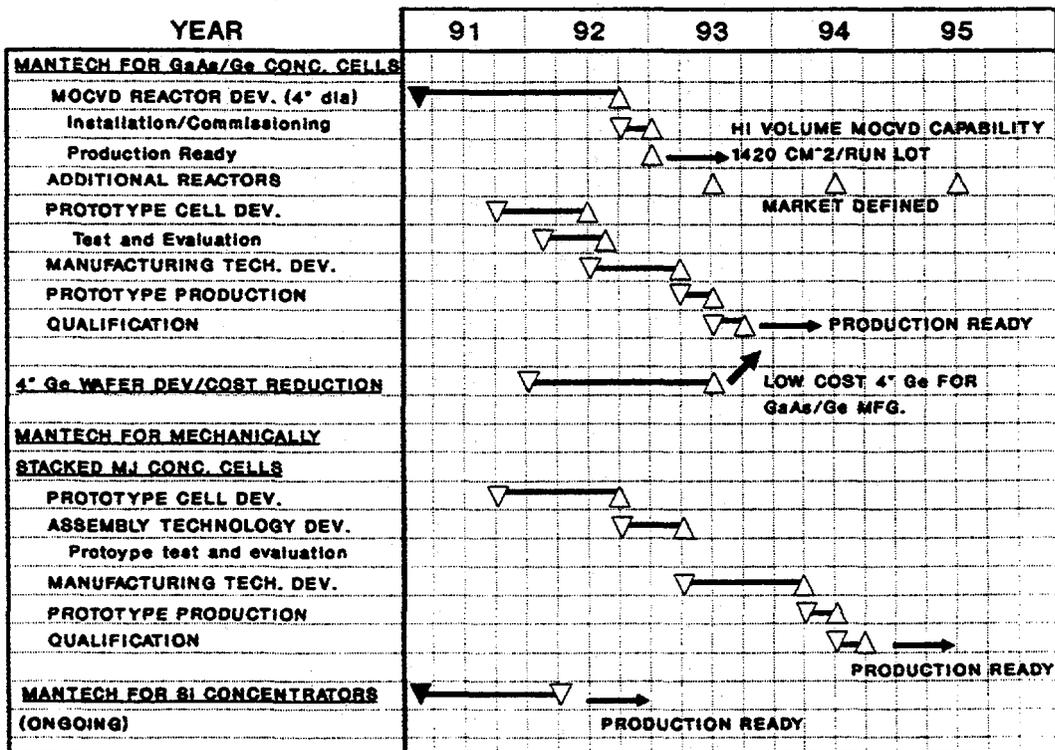


Figure 5.1 PROGRAM SCHEDULE

5.1 MANUFACTURING TECHNOLOGY PROGRAM FOR GaAs/Ge CONCENTRATOR CELLS

In order to achieve the most timely cost reduction for GaAs/Ge concentrator cells, Spectrolab recommends that a manufacturing technology program for GaAs/Ge concentrator cells be performed. A potential cell design is shown in Figure 5.2 although alternative grid designs and cell sizes would be accommodated to meet the needs of specific module manufacturers.

The estimated cost and duration of this program would be approximately 10 man years covering a period of two years. The elements of this program are described below.

5.1.1 Large Area MOCVD Growth

Key to meeting the DOE cost and efficiency goals is the development and installation of large area MOCVD reactors with improved thickness, compositional and doping uniformity. This will provide the capability to grow GaAs cost effectively, in addition to other advanced materials such as GaInP and InGaAs in a high volume manufacturing environment. This was discussed in Section 3.3.1.

Because of the many process factors that can affect the uniformity, this program is well suited for the application of Taguchi Methods. Taguchi's approach to statistical design of experiments allows a large number of factors to be evaluated with a minimum number of experimental runs, thus reducing the cost of the research.

Spectrolab will team with Hughes Aircraft Company, Microwave Products Division to apply Taguchi principles to MOCVD growth

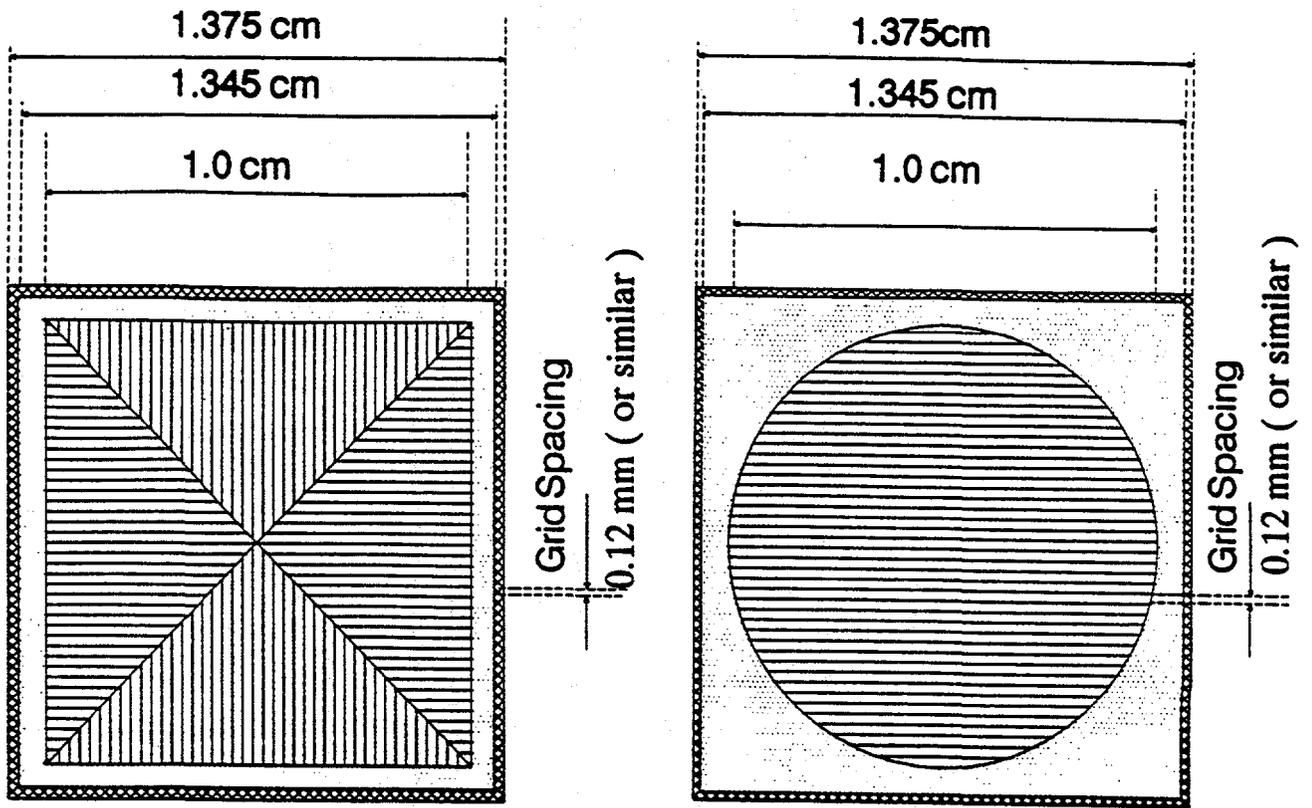


Figure 5.2 CANDIDATE GaAs/Ge CONCENTRATOR DESIGNS

experiments and will apply its extensive experience with solar cell production, Statistical Process Control and design of experiments using Taguchi and classical methods.

Taguchi methods would be used for analysis of the data to determine the relative effects of eleven factors on MOCVD uniformity (thickness and doping concentration), and boundary abruptness. The data will be in graphical form to facilitate interpretation and analysis. In addition, data will be collected on the cycle time and operating cost of each combination of factors to allow for design trades for ease of manufacture and overall cost effectiveness.

The factors to be evaluated will be:

1. V/III Mole Ratio
2. Susceptor Temperature
3. Total H₂ Flow Rate
4. Reactor Pressure
5. Substrate Surface Preparation
6. H₂ Blank of Flow Rate
7. Susceptor Rotation Speed
8. TMG Flow Rate
9. TMA Flow Rate
10. Silane Flow Rate
11. DMZ Flow Rate

This effort will improve the effective yield of MOCVD growth to over 70% thereby reducing cost considerably.

The GaAs/Ge interface may also be important in obtaining a high performance solar cell. Experiments will be performed to

optimize MOCVD growth conditions to minimize series resistance effects at the GaAs/Ge interface which would otherwise cause resistive losses at high concentrations.

5.1.2 Batch Processing Improvements

The application of batch processing techniques to GaAs/Ge and GaAs/GaAs processing will reduce the cost of the final product by reducing the time to fabricate the cells and minimizing breakage.

Spectrolab has extensive experience in translating prototype R&D devices into manufacturable products. Fixturing and processing techniques have been developed to minimize the breakage of thin, delicate solar cells. These techniques will be particularly important in fabricating thin cells where wafer thicknesses may be only 4 to 6 mils to achieve the maximum number of wafers per inch of ingot. The following methods have been used on silicon cells and may be applied to GaAs or Ge substrates to facilitate batch processing:

1. Attachment of a sturdy substrate during processing.
2. Protection of the edge during etching to prevent the formation of sharp edges and to form a sturdy frame for subsequent processing.
3. Use of cassette to cassette processing equipment to minimize handling.

Germanium wafers are much sturdier than GaAs. We expect to be able to use current silicon manufacturing equipment with little or no modification. A brief verification program would examine each process for its manufacturability.

Reactive Ion Etching of the GaAs cap layer must also be evaluated as a potential replacement for the current aqueous process. Initial work will be performed using a planar RIE system already in use at Spectrolab.

5.1.3 Germanium Wafer Readiness

Spectrolab has evaluated 4.5 cm x 4.5 cm germanium substrates from a number of vendors including MHO, Crystal Specialties, Laser Diode and Eagle Picher. Our experience is that substantial differences in quality can exist between vendors which translates, ultimately, to differences in cell performance.

Our experience with silicon manufacturing has also shown that significant cost reduction can be achieved using 4" diameter technology instead of using square or smaller diameter wafers. A focussed program to develop 4" diameter germanium wafers with reduced defect density and a reproducible epi-ready polish is therefore required. Manpower estimates from germanium vendors to achieve 4" inch diameter capability vary between two to five man years over approximately a 1 year period. Part of the program would be the development of improved slicing techniques to yield more wafers per inch and the investigation of vertical Bridgeman and encapsulated Cz techniques for larger ingot diameters.

5.2 GaAs/Ge CELL PERFORMANCE PREDICTIONS

Spectrolab's experience with GaAs/GaAs and GaAs/Ge cells for planar space applications indicates that the Ge substrate has little or no effect on cell performance if the correct growth temperature and crystal orientation are used.

Using known, and readily achievable, material parameters and assuming negligible losses from resistive effects at the GaAs/Ge interface we predict an efficiency of 27.9% for a 1.25 cm x 1.25 cm GaAs/Ge cell operating at 200 X AM1.5D.

5.3 MULTIJUNCTION CELL DEVELOPMENT AND MANUFACTURING TECHNOLOGY

Our approach to increase cell efficiency above 30% is to develop multijunction cell assemblies based on mechanical stacking techniques. Two approaches show potential for meeting the DOE cost targets. The development schedule and implementation into production is shown in Figure 5-1.

The first approach utilizes a transparent GaAs cell mechanically stacked in a voltage matched configuration on four Ge cells as shown in Figure 4.12.

The second approach utilizes a proprietary design applicable to many cell types of differing band gaps and does not require voltage matching between cells. The design is currently proprietary to Spectrolab, it being the subject of a patent application.

A description of the development and manufacturing technology activities required to produce the voltage matched, mechanically stacked GaAs/Ge cell is given below.

We believe that to bring a cell of this technological complexity from conception to full production status requires a combined development and manufacturing technology program of approximately 15 man years, covering a period of three years.

5.3.1 Mechanically Stacked, Voltage Matched GaAs/Ge Cell

5.3.1.1 GaAs Cell Optimization

In Section 4.3.1 we described several features of the GaAs cell that are important to maximize the stack performance. This section will discuss potential process and material improvements to optimize the performance of the GaAs top cell.

5.3.1.1.1 Materials Optimization

The AlGaAs window layer must be optically transparent for good blue response of the GaAs cell. This is accomplished by using a 500 angstrom thick layer with a 85% AlAs fraction. Experience has shown that decreasing thickness or increasing the AlAs content beyond these values results in processing and environmental stability problems.

Emitter sheet resistance losses in the concentrator are significant and must be minimized. To achieve this, the emitter depth is increased to 0.7um to 0.8 um from the standard 0.5 μ m, thereby decreasing sheet resistance to approximately 250 ohms/sq.

The base doping level is chosen to minimize the concentration of thermally generated minority carriers while at the same time achieving adequate diffusion lengths to ensure the collection of the photo-generated carriers. The thickness of the base is designed to take advantage of a back surface heteroface reflector. The Al₂ Ga₈ As layer is used to create a field to confine minority carriers to the base (Ref. 6). However, there is some evidence that the AlGaAs layer may actually behave more as a gettering layer for oxygen and water vapor, which

improves subsequently grown layer quality, than as a minority carrier reflector (Ref. 7). In either case, enhanced performance is generally obtained with its use.

Substrate doping is dictated by the need to minimize free-carrier absorption of the below band edge photons. Absorption can also be minimized by using a thinner substrate. In Figure 5.3 we show the transmission through GaAs as a function of doping level (Ref. 8). The transmission is plotted for several different thicknesses. We have adopted a design criterion of less than 5% substrate absorption loss. From Figure 5.3 we see that at a wafer thickness of 0.01 cm, only 3% of the incident light is absorbed with a doping level of $1 \times 10^{17} \text{ cm}^{-3}$. GaAs substrates are readily available with this doping and at a thickness of 0.02 cm. The use of these substrate parameters will result in absorption of 5%, which meets our design requirements.

The design of the cell's active regions is aided by computer models developed at Spectrolab which utilize the material parameters of layer thickness and doping levels, carrier mobilities and lifetime, and recombination in the space-charge region and at surfaces. The calculated values for the first and second diode dark currents and the spectral response are then used in a diode network model of the cell to optimize collector designs.

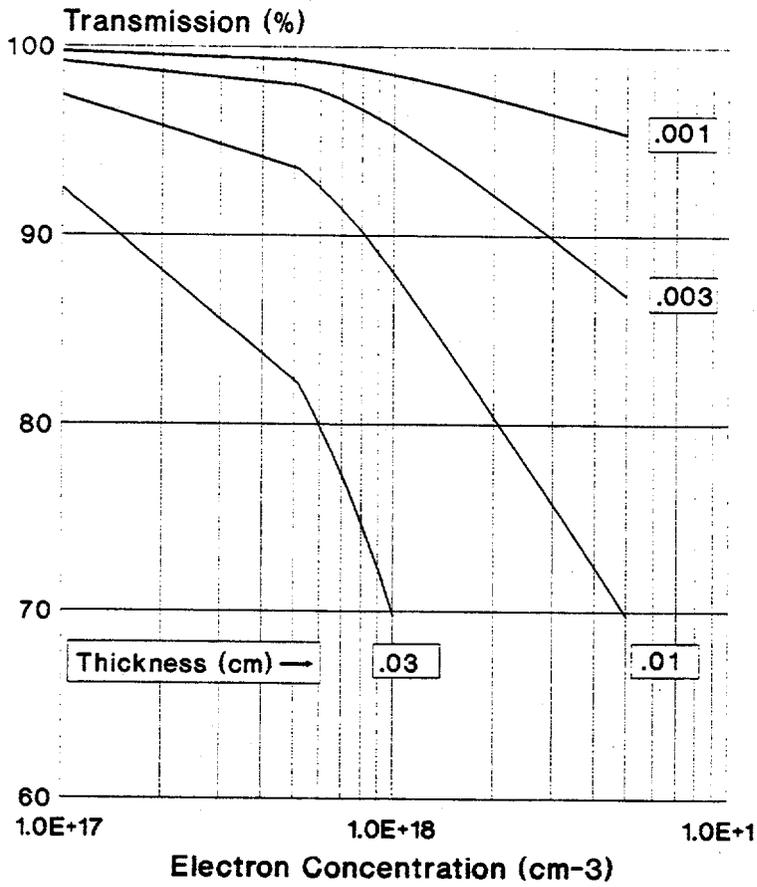


Figure 5.3 TRANSMISSION THROUGH SUBSTRATE AS A FUNCTION OF DOPING AND THICKNESS

Preliminary design optimization has been performed using the parameters given in the table below:

Layer	Thickness (μm)	Diff. L (μm)	Diff. CFT (cm^2/s)	Rec. Velocity (cm/s)	Doping Conc ($1/\text{cm}^3$)
Window	0.05	0.2	0.27	1×10^6	2×10^{18}
Emitter	0.7	5.0	90	1×10^4	2×10^{18}
Base	3.0	2.0	5.0	100	4×10^{17}

5.3.1.1.2 Optical Coating Design

A three layer anti-reflection coating is used to achieve a low front surface reflectance from 0.35 to 1.85 microns. Spectrolab has developed optical codes to aid in designing antireflective coatings. These codes have been used to design a coating which when coupled into a silicone based adhesive ($n=1.42$) produces the reflectance shown in Figure 5.4. In the inescapable trade-off between top and bottom subcell performances the design is biased to the GaAs cell. Even so, near optimum GaAs cell currents of 29.15 mA/cm^2 (active area) can be achieved with less than 1% loss in Ge cell performance.

An AR coating must also be used on the back of the cell to couple the below GaAs band edge energy out of the cell. A coating must also be present on the Ge cell surface to accept the incoming radiation. The coating design is simplified because of the narrower wavelength band and a two layer coating is effective. The reflectance from the back surface into an index of 1.42 is also included in Figure 5.4.

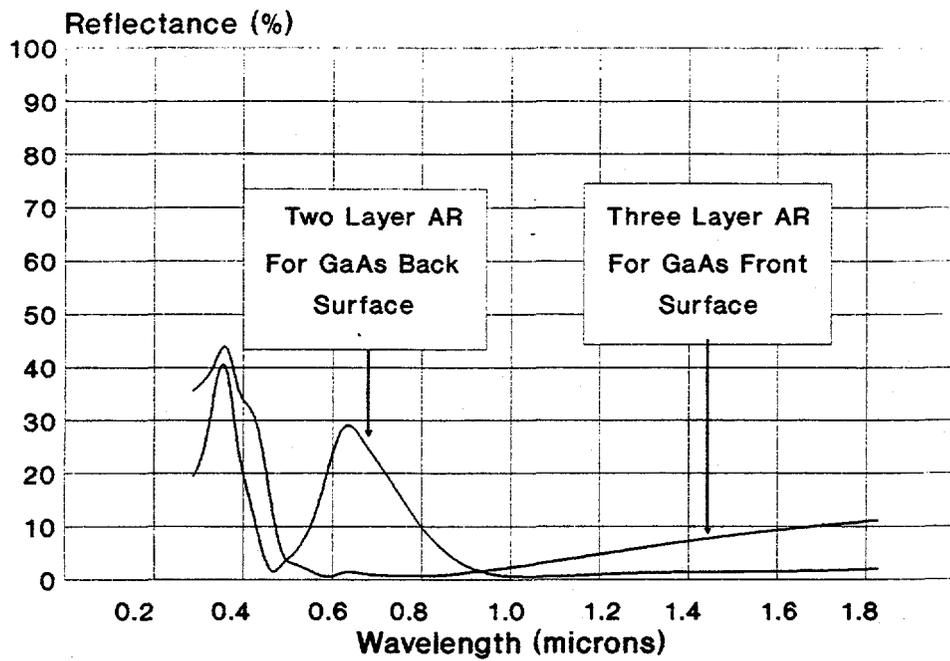


Figure 5.4 CALCULATED REFLECTANCE FROM FRONT AND BACK GaAs SURFACES

5.3.1.1.3 Front and Back Collector Designs

Computer models developed at Spectrolab were used to model cell performance in the 1 and 2 bus configurations. Grid geometries (5um high and 12 um wide) were chosen to be compatible with our present processing capabilities and also with published data for cells which have utilized the Entech cover (Ref. 9). These results are summarized in Figure 5.5. A single bus along one edge is unsatisfactory in a 200X concentrator with 1.25 cm long grids. The use of a second opposing bus results in an absolute efficiency increase of 1.9% for cells without a prismatic cover. At a grid spacing of .01 cm the efficiency of the 2-bus configuration is 27.9% (AM1.5, 200X, 28°C) compared a 26.0% peak value for the single bus.

5.3.1.2 Germanium Cell Optimization

In Section 4.3.2 we summarized important features of the germanium cell to maximize its' performance under the GaAs top cell. The basic design of the germanium cell structure is shown in Figure 4.2.

5.3.1.2.1 Germanium Material Selection

The mechanically stacked cell is assembled in the voltage matched configuration which allows for the use of either n or p type substrates. There are several advantages of the use of P-type germanium over N-type germanium for cell operation and manufacturability. Factors such as higher electron mobilities in P-Ge are important for germanium cell operation. The availability of a simple diffusion process as described in Section 2.2.4, simplifies the fabrication of germanium cells.

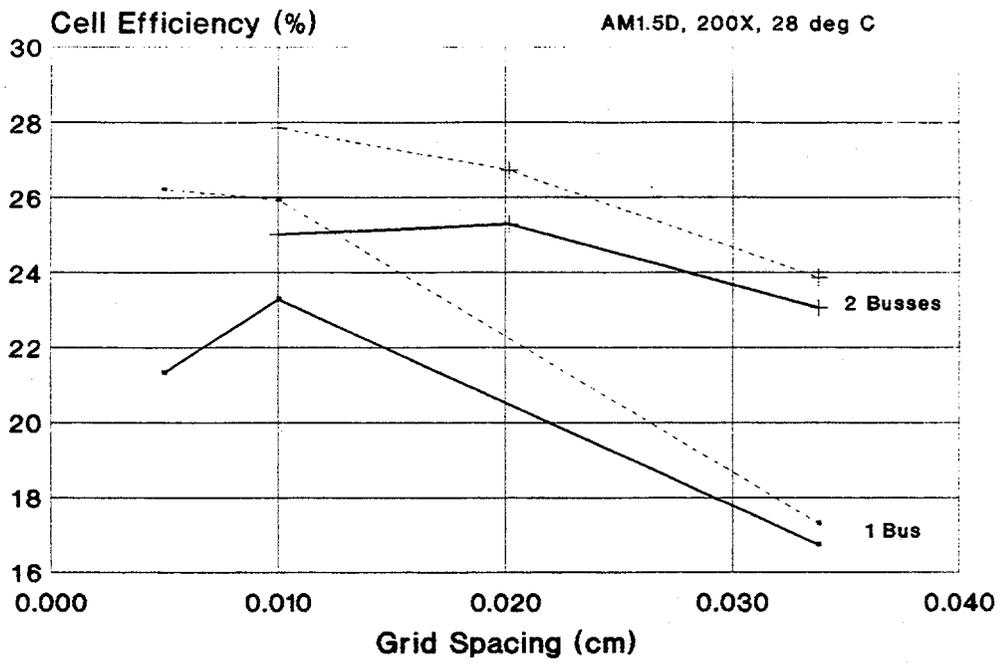


Figure 5.5 COMPUTED EFFICIENCIES FOR GaAs CELL AS FUNCTION OF TOP GRID SPACING

We have modeled germanium cell performance using both Spectrolab solar cell models and PC-1D version 2.1 (Ref. 10). These models were used to calculate cell performance as a function of the junction depth, diffusion lengths and doping levels. Figure 5.6 summarizes cell efficiencies under a GaAs filter for both N/P and P/N type cells for several values of base doping concentration. These results demonstrate that both types of cells have the same potential performance. Therefore substrate type selection will be dictated by ease of processing, availability and cost.

5.3.1.2.2 Germanium Diffusion Length

As described in Section 4.3.2, the germanium minority carrier diffusion length plays a major role determining current generation in the red end of the spectrum. A fifty micron diffusion length is needed to maintain a high quantum efficiency near the germanium band edge.

As part of our work on monolithic dual junction, current matched GaAs/Ge cells, discrete germanium cells were fabricated and characterized. Junctions were formed by ion implantation of aluminum. The measured quantum efficiency for one cell is shown in Figure 5.7. A germanium diffusion length of 75 microns was determined by curve fitting the measured response with PC-1D modeled data. This indicates that the base material is of sufficient quality to make high efficiency cells but that the junction formation process requires further development since the Q.E at shorter wavelengths is too low.

5.3.1.2.3 Germanium Surface Passivation

Surface recombination processes play an important role in determining Ge cell performance since Ge is highly absorbing

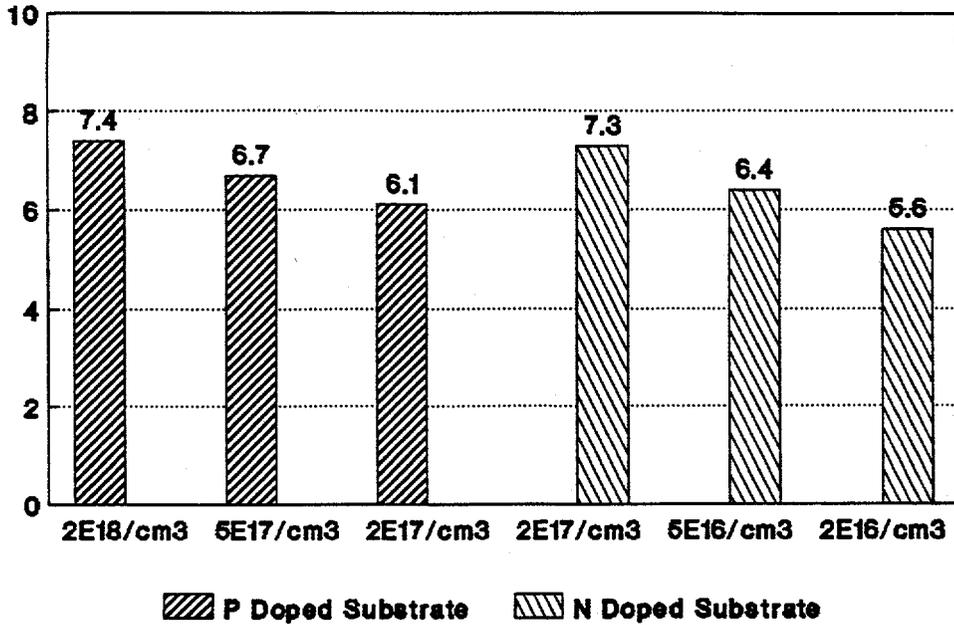


Figure 5.6 Ge CELL EFFICIENCIES UNDER GaAs FILTER

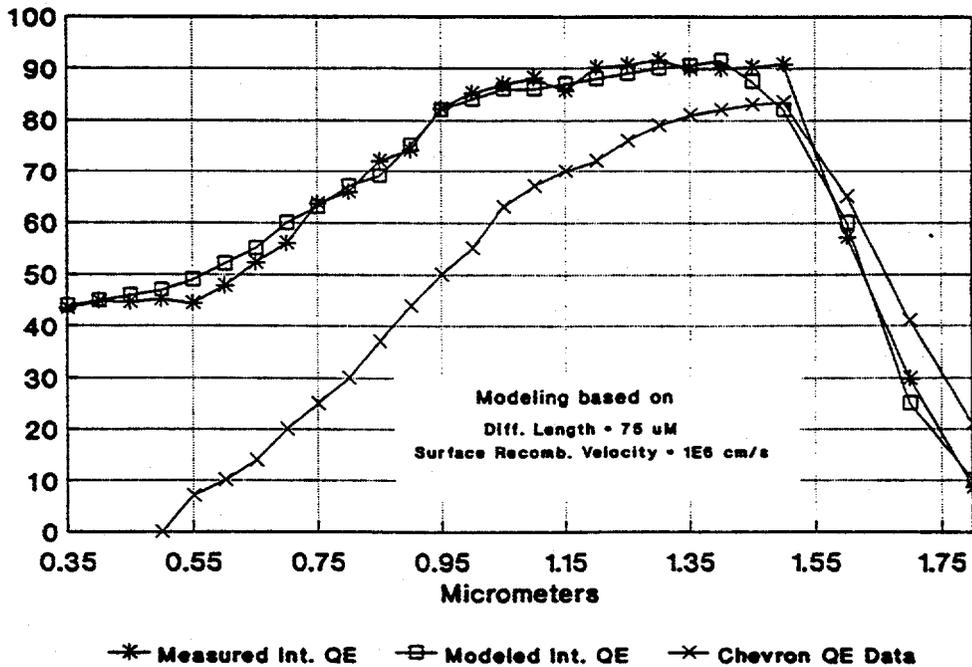


Figure 5.7 MEASURED Q.E. OF EXPERIMENTAL Ge CELL

even at wavelengths beyond the GaAs band edge. In Section 4.3.2 we showed the influence of surface recombination velocity on germanium cell efficiency. Surface passivation coatings will be used to obtain a recombination velocity of less than 1×10^4 . Candidate passivation materials are ZnS, GaAs and AlGaAs. These materials would provide a good AR coating in addition to possibly passivating the front surface.

5.3.1.2.4 Germanium Emitter Depth Optimization

The emitter depth plays an important role in determining germanium cell performance. In Section 4.3.2 we showed the influence of a thin junction on current generation. Both diffusion and implantation processes can be used to produce a thin junction. Current diffusion processes developed for silicon cells result in a 0.15 micron junction depth. As shown in Figure 5.7 this is shallow enough so that the emitter depth will not limit current production.

The following diagnostic measurements will be performed on cells and test structures to arrive at optimized Ge junction parameters:

1. Spreading resistance
2. Light and dark IV testing of Ge cell structures
3. Spectral Response

5.3.1.2.5 Germanium Back Surface Field

Back surface recombination velocity can be controlled by implementing a Back Surface Field (BSF). Modeling has shown that the presence of a BSF doped to $1 \times 10^{19} \text{ cm}^{-3}$ increases the short circuit current by approximately 2% and V_{oc} by 4% for a substrate doping of $5 \times 10^{17} \text{ cm}^{-3}$.

Spectrolab has verified the increase in germanium cell performance provided by a BSF. In Figure 5.8 we show the measured effects of a BSF on the Voc and Isc of 3 to 8 mil Ge cells. All measurements were performed at AMO, 28°C. Thin (3-4 mil) substrate thicknesses are required to produce an effective BSF, due to the relatively short diffusion length in germanium.

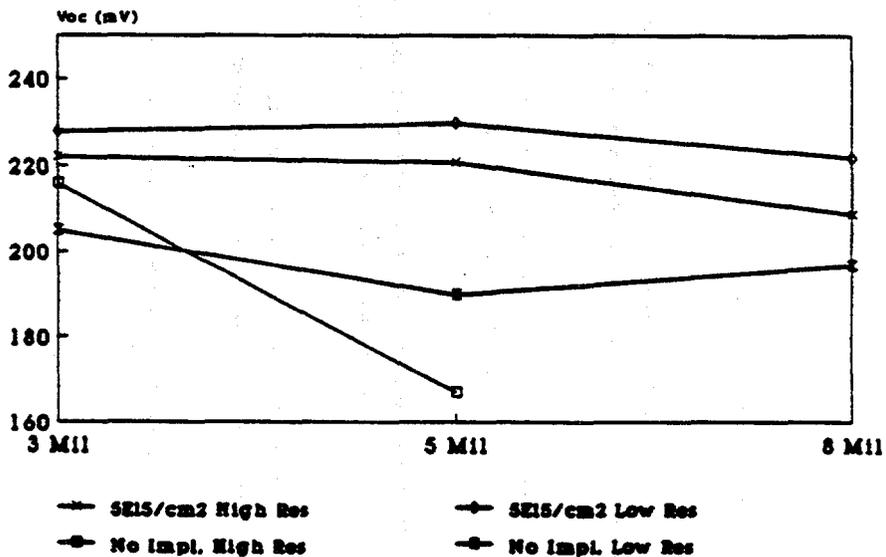
5.3.1.2.6 Light Trapping

Back Surface Reflector

Design analysis predicts that the use of a back surface reflector (BSR) on a germanium cell produces current gains of up to 1.5%. Our choice of a BSR for the germanium cell is aluminium with a separating SiO₂ dielectric layer over 90% of the back surface, as described in 4.3.2. Calculations show that a reflectance in excess of 99% is achievable when a half wave layer of SiO₂ is used to separate the back metal contact from the Ge substrate. We have also measured over 95% reflectance on experimental BSR structures thus validating our assumption of a 1.5% gain in our modeling.

Spectrolab will design the SiO₂/aluminum stack to optimize the BSR and minimize contact resistance to the substrate. A tuned SiO₂ layer with etched vias will be used to provide for ohmic contact formation. The cross-section of the vias must be wide enough so that the current density at 200X to 500X concentration flowing across the contact does not cause a significant voltage drop. The effectiveness of the BSR structure will be measured using optical methods and by fabricating and testing cells with and without the BSR.

**Cell Thickness and BSF Effects on Voc
For High and Low Resistivity Cells**



**Figure 5.8 EXPERIMENTALLY MEASURED EFFECT OF
A BSF ON Ge CELL PERFORMANCE**

Texturing

Germanium cell performance at wavelengths beyond approximately 1.6 microns (where Ge absorption becomes indirect) will be increased by texturing or microgrooving the front surface and specific anisotropic etchants must be developed to achieve this.

Several possible anisotropic etches are listed in Table 5-1.

Table 5.1 POSSIBLE ANISOTROPIC ETCHES FOR Ge

Etch / Concentration	Expected Surface Texture
1 H ₂ O ₂ : 1 Citric Acid	Octahedrons
1 H ₂ O ₂ : 1 Tartaric Acid	Rhombic dodecahedron
1 Tartaric Acid : Br ₂	Tetrahexadron
3 HNO ₃ : Tartaric Acid	Hexahedron (cube)

Our investigation of texture etches will include:

1. Surface examination using SEM and optical microscope
2. Optical absorption measurements near the Ge absorption edge using a modified Beckman spectrophotometer with Gier Dunkel sphere to correlate surface texture and increased light trapping.
3. Fabrication of cells with and without surface texturing and comparison of their performance.

5.4 STACKED MULTIJUNCTION CELL INTERCONNECTION AND PACKAGING

5.4.1 Cell Interconnection

The cell interconnection and bonding process is critical for the successful assembly of the stacked multijunction cell. The assembly design calls for the bottom cells to be connected in series with low resistive loss between cells. Each cell must be isolated from its' neighbor but the separation between cells must be minimized to maximize packing density. In order to maximize heat transfer to the heat sink, the insulating substrate upon which the cells are mounted must be thin, and highly thermally conductive.

The sequence of component assembly is shown in Figures 5.9 and 5.10 and is described below.

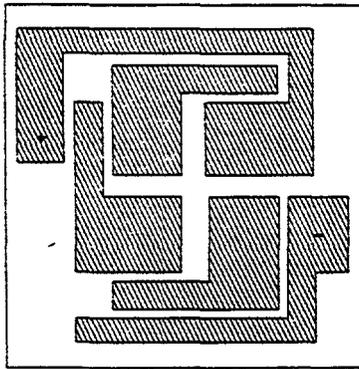
Step 1 Substrate Identification and Selection

Hughes Microelectronic Circuits Division will act as subcontractor to provide substrates to final specification.

The substrate size and pad layout will be finalized in this task. At this time the substrate dimensions are expected to be 2.5cm x 2.5cm, but this may change to accommodate manufacturers specific module designs. Substrate thickness is a factor in both mechanical reliability and thermal conductivity and different thicknesses will be evaluated.

One issue requiring particular attention will be the current carrying capacity of the copper or printed silver pattern on the substrate. Under concentration at 300 X the cell current will be over 9 amps. The thickness of the conductors will be adjusted so that the voltage drop at load is less than about 10 mV.

ALUMINUM OXIDE OR ALUMINUM NITRIDE CERAMIC SUBSTRATE

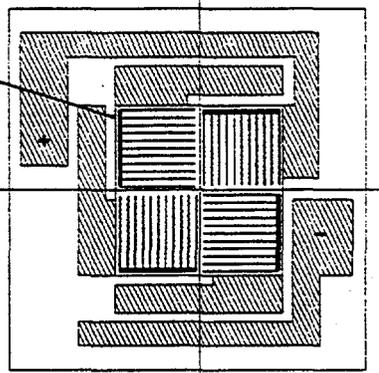


STEP 1. DEFINE CONDUCTORS ON INSULATING SUBSTRATE

SAW DICE LINE

QUAD Ge CELL CHIP

SAW DICE LINE

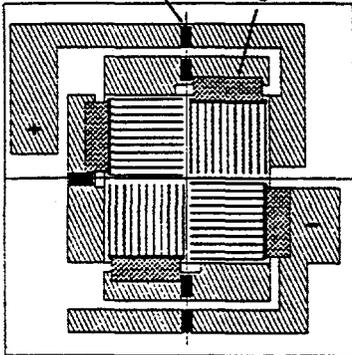


STEP 2. BOND Ge CHIP TO SUBSTRATE

STEP 3. DICE TO ISOLATE Ge CELLS

TRACK REPAIR

SERIES INTERCONNECTION BY WELDED Ag MESH OR Ag WIRE BALL BONDING

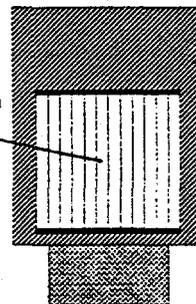


STEP 4. REPAIR BROKEN TRACKS

STEP 5. SERIES INTERCONNECT Ge CELLS USING Ag MESH OR BALL BONDING

125cm X 125cm GaAs CELL

PICTURE FRAME

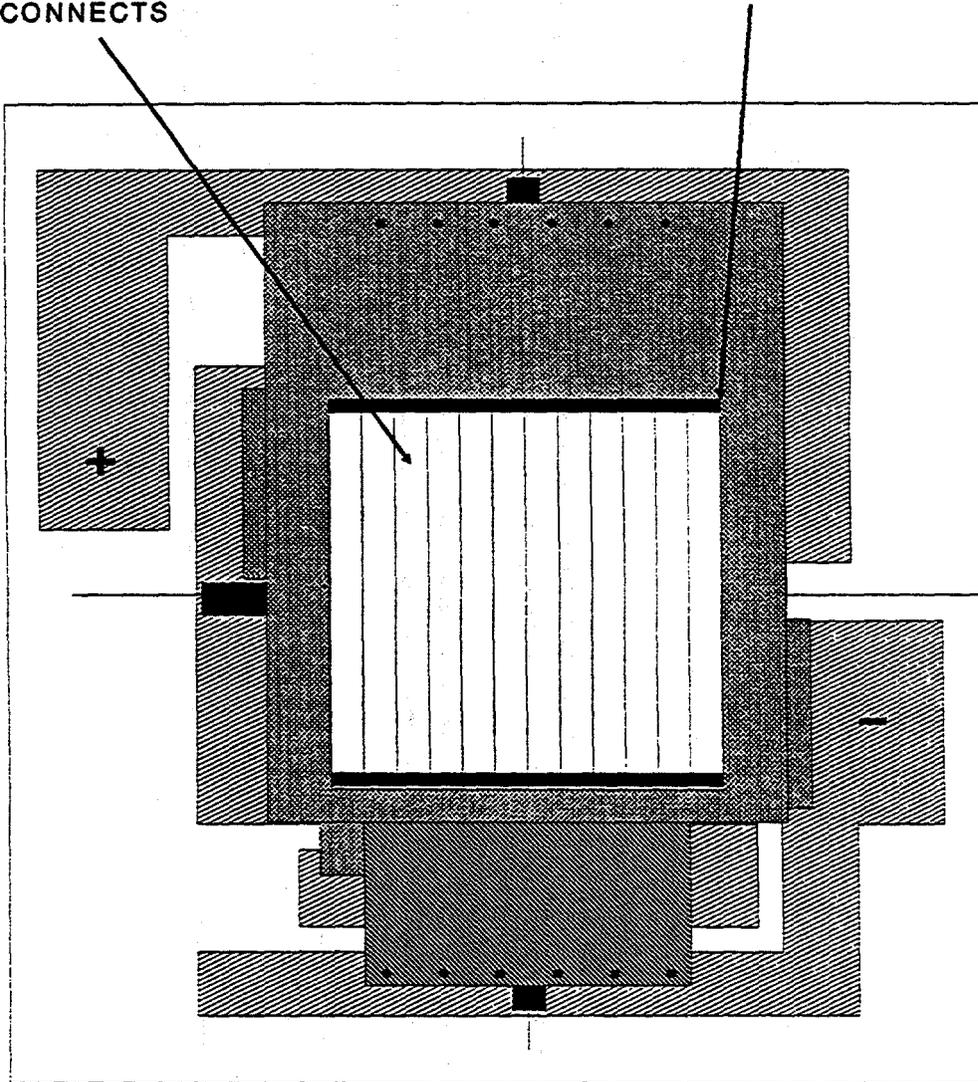


STEP 6. ATTACH PICTURE FRAME TO GRIDDED BACK GaAs CELL

Figure 5.9 PROPOSED CONSTRUCTION AND ASSEMBLY SEQUENCE OF CONCENTRATOR RECEIVER ASSEMBLY

GaAs CELL SLIGHTLY UNDERSIZED TO FIT INSIDE Ge CELL SERIES INTERCONNECTS

GaAs AND Ge CELLS SEPARATED BY GLASS WEAVE AND DC 93500 ADHESIVE



STEP 7. BOND GaAs CELL TO Ge CELLS AND CONNECT TO +ve AND -ve BUSES

Figure 5.10 COMPLETE CONCENTRATOR RECEIVER ASSEMBLY

Step 2 Ge chip bonding and cell isolation

Two methods of chip bonding will be evaluated as described below:

1. The method of Chiang (Ref. 11). This consists of placing a preform of SN 62 solder between the bond pad and cell which have been fluxed. The sandwich is then placed on a hotplate to melt the solder and bond the chip to the substrate.
2. An alternative method of chip attachment is to screen print solder paste to the chip and substrate pads prior to bonding. Heating on either a hotplate or belt furnace will cause the solder to reflow, thus bonding the chip to the substrate. Excellent wetting of both surfaces is expected, resulting in a very good bond.

The two processes will be analyzed by thermal cycling from -140°C to $+110^{\circ}\text{C}$ over 250 cycles to ensure the bond does not separate. X ray and ultrasound images will be made to determine bond quality before and after cycling and to determine the method of failure should it occur.

Prior to bonding the Ge chip will consist of four mesa or planar isolated cells each having their own contact design. After bonding the bases will be isolated by dicing through the Ge wafer into the ceramic substrate using a diamond saw. The depth of the cut will be designed so that it does not compromise the strength of the substrate.

Step 3 Series interconnection of germanium cells

Three possible methods for series interconnection exist:

1. Soldering of preform mesh
2. Welding of Ag mesh
3. Ball bonding

Soldering and welding of Ag mesh is an existing technology at Spectrolab. Both processes use Hughes parallel gap electrodes and power supplies. Feedback of weld temperature and pulse duration is made to the power supply to ensure adequate process control of the weld cycle. For soldering, a lower integrated energy pulse is applied to the electrode tips. In all cases, joints are inspected on a sample basis for conformance to MIL specification and NASA requirements.

Ball bonding is a new technology being developed at Spectrolab. Ball bonding could be very cost effective since it is highly automated and a large number of bonds can be made in a very short time.

Step 4 Interconnect attachment to front and rear of GaAs cell

A picture frame arrangement of wire mesh will be bonded to the front and rear collector bus of each cell. The picture frame arrangement will allow current to be collected from each end of the cell.

Step 5 Bond and interconnect GaAs to Ge cells

The top GaAs cell must be mounted on top of the bottom cells using an adhesive which provides electrical isolation, adequate

bond strength, optical stability and excellent optical coupling into the bottom cells. Candidate adhesives are DC 93500 or GE 615.

A glass weave will be placed between the cells to provide electrical isolation. Other options for isolation are to use a glass coverslide or an adhesive filled with a glass frit.

Interconnects from the GaAs cell will be either welded or soldered (as discussed above) to the common positive and negative buses on the substrate.

5.4.2 Predicted Performance

Modeling of the stacked multijunction cell utilizing a GaAs top cell and germanium bottom cells predicts a 200X AM1.5D efficiency of 33%.

The top GaAs cell measures 1.25 cm x 1.25 cm and incorporates highly efficient gridded contacts and optical coatings. Using known, and readily achievable, material parameters we predict an efficiency of 27.9% for the GaAs cell shown in Figure 5.11.

In performing the Ge subcell performance analysis an accurate accounting of the optical losses was made. These include all interface, obscuration and absorption losses. The predicted performance of four .313 cm x .313 cm Ge cells connected in series is shown in Figure 5.12. The efficiency of the Ge series interconnected string is 6.2% under the GaAs top cell at 200 X AM1.5D. At the GaAs maximum power point the germanium cells provide an additional 5.5% absolute efficiency points.

Projection of the 28°C efficiency to an operating value requires making several assumptions.

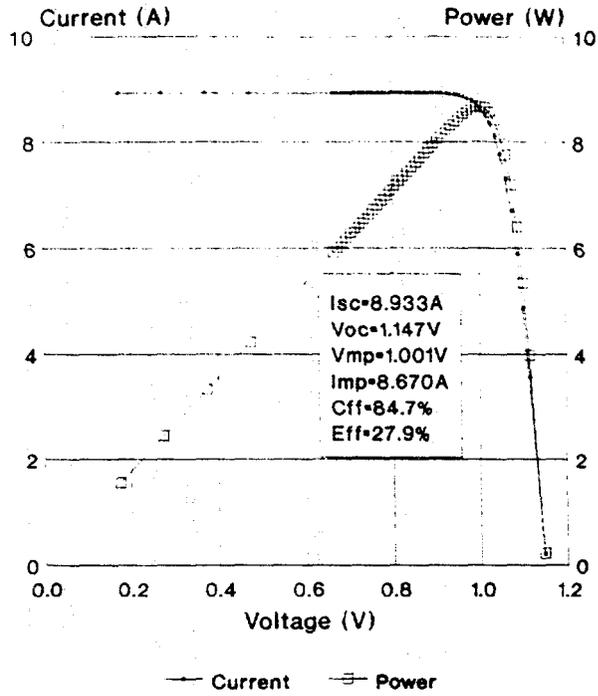


Figure 5.11 PREDICTED PERFORMANCE OF GaAs TOP CELL AT 200X AM1.5

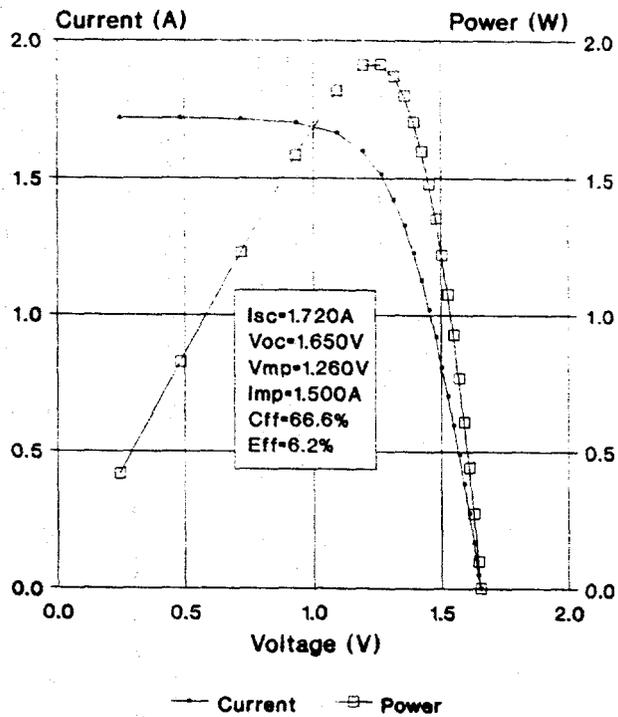


Figure 5.12 PREDICTED PERFORMANCE OF Ge SERIES INTERCONNECTED

Firstly, the temperature of the cells mounted on a concentrator module such as the SBM3 at 200X were extrapolated from data given by Gee. (Ref 11). The values so derived for the GaAs and germanium cells were 62°C and 56°C respectively.

Secondly, while accurate temperature coefficients are known for the GaAs cell (-0.031% absolute/ degree C) similar data does not exist for germanium. An estimate of -0.025% (absolute/ degree C) was made using PC1D modeling. With these data, operating efficiencies of 26.8%, 4.8%, and 31.6% were calculated for the GaAs, Ge and mechanically stacked cells respectively.

Matching the maximum power point of the top and bottom cells is important. A mismatch results in wasted energy. However, given individual subcells whose sum voltage exceeds that of the top cell, it is not profitable to reduce the voltage unless it results in an increase in current. The germanium cell must therefore be optimized to maximize current at the GaAs load voltage.

5.5 SILICON CONCENTRATOR CELL MANUFACTURING TECHNOLOGY

Spectrolab is currently under contract from Sandia to develop the manufacturing technology for a silicon concentrator cell. The schedule is shown in Figure 5.13. The objective is to achieve a 22% 250X AM1.5D efficiency with a cell price of \$1.7/cm² or less.

Additional cost savings may be realized if less ambitious goals are set for the cell efficiency. In Section 3.2.2 we described features of the cell that may be eliminated that may decrease the final cell cost. These features are sculpturing, back surface field and front surface passivation. Experiments would

TASK	YEAR	
	1	2
<p>PHASE 1</p> <p><u>SOLAR CELL DEVELOPMENT</u></p> <p>Device Design Photomask Designs Process Flow Prototype Fabrication Test Improvements Additional Cell Fabrication Test Design Freeze</p> <p>PHASE 2</p> <p><u>MANUFACTURING READINESS</u></p> <p>Cost Driver Analysis Process Improvements Yield Improvements Direct Materials Cost Reduction Manufacturing Methodology Capital Equipment Requirements Readiness Verification Cost Projections</p> <p><u>DELIVERABLES</u></p> <p>200 Cells 500 Cells 1000 Cells</p>	<p>▲</p> <p>▲</p>	<p>▲</p>

Figure 5.13 PROGRAM SCHEDULE SANDIA CONCENTRATOR INITIATIVE

be performed where these features would be deleted from the processing and their performance would be compared to cells that receive the processing. In addition to the cell development, environmental tests would be performed to ensure that the module will have a 30 year life. A cost comparison would be made to decide which cell configuration will best meet the DOE cost goals.

6.0 CONCLUSIONS AND RECOMMENDATIONS

This report has described the current silicon and gallium arsenide manufacturing capabilities at Spectrolab. As described in Task 1, the solar cell manufacturing line is used to fabricate simple and complex solar cells. This flexibility allows for testing out new designs in a manufacturing environment.

Several solar cell designs were described in Task 2 which have the potential to meet the DOE cost and efficiency goals. Of these designs the silicon concentrator requires the least development. The manufacturing capability currently exists on the silicon manufacturing line to meet the short terms cost goals. Additional work should enable these cells to fulfill the long term goals as well. A schedule to meet the cost goal of \$.06 kWh is shown in Figure 5.1. This plan could be implemented as part of Phase 2 of PVMat.

Modules that utilize GaAs solar cells are also described within Task 2. These designs require an extensive development program to meet cost and efficiency goals. Spectrolab recommends that Phase 2 of PVMat include a manufacturing technology program to develop these cells, as shown in Figure 5.1 Both process development and cell design would be performed during this program. Cost goals will be obtained by utilizing large area germanium substrates and uniform MOCVD GaAs growths. Task 4 describes in detail the work required to attain MOCVD growth uniformities needed and to implement batch processing in the production of these cells. Both of these goals are necessary to attain the DOE cost and efficiency goals.

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APPENDIX A

**SUMMARY OF SPECTROLAB EXPERIENCE
IN GaAs PANEL TECHNOLOGY**

SUMMARY OF SPECTROLAB EXPERIENCE IN GaAs PANEL TECHNOLOGY

PROJECT NAME YEAR	CONFIGURATION OF FLIGHT TEST PANEL	CONDITIONS	RESULTS
Soldered GaAs Panel 1982	SOLDERED PANEL 300 LPE GaAs CELLS 25 SERIES BY 4 PARALLEL 3 CIRCUITS AG PLATED KOVAR INTERCONNECT SUBSTRATE - ALUMINUM HONEYCOMB	FLIGHT FEBRUARY 1983 LOW EARTH ORBIT (600 nm)	PANELS FUNCTIONING AT 1650 DAYS (NOVEMBER 1987)
Soldered GaAs Panel 1983	SOLDERED PANEL 140 LPE GaAs CELLS 28 SERIES 5 CIRCUITS AG PLATED MOLYBDENUM INTERCONNECT SUBSTRATE - ALUMINUM FACESHEET	FLIGHT PANEL -40°C TO +40°C	PANELS QUALIFIED BUT NOT FLOWN
Soldered Panel 1983	CONCENTRATOR SOLDERED PANEL 50 LPE GaAs CELLS (6X) 10 SERIES BY 2 PARALLEL 10 SERIES BY 3 PARALLEL AG PLATED KOVAR INTERCONNECTS SUBSTRATE - ALUMINUM FACESHEET	1000 THERMAL CYCLES -100°C TO +150°C	PANEL PASSED QUALIFICATION
Welded Panel 1985	PARALLEL GAP WELDED 36 LPE GaAs CELLS 12 SERIES BY 3 PARALLEL SILVER MESH INTERCONNECT SUBSTRATE - GRAPHITE COMPOSITE FACESHEETS ON AN ALUMINUM HONEYCOMB CORE	500 THERMAL CYCLES -130°C TO +140°C AT SPECTROLAB 18,000 THERMAL CYCLES -80°C TO +80°C AT NASA LERC	NO POWER DEGRADATION NO MECHANICAL DAMAGE NO POWER DEGRADATION NO MECHANICAL DAMAGE

SUMMARY OF SPECTROLAB EXPERIENCE IN GaAs PANEL TECHNOLOGY (CONT'D)

PROJECT NAME YEAR	CONFIGURATION OF FLIGHT TEST PANEL	CONDITIONS	RESULTS
Welded Panel 1986	PARALLEL GAP WELDED 6 LPE GaAs CELLS 3 SERIES BY 2 PARALLEL SOLID SILVER INTERCONNECT SUBSTRATE - TITANIUM FACESHEETS ON A TITANIUM HONEYCOMB CORE SOLID 30 AWG SILVER-PLATED COPPER BUS WIRES WELDED DIRECTLY TO SILVER TERMINATION TABS	500 THERMAL CYCLES -130°C TO +140°C AT SPECTROLAB	1.3% POWER LOSS
Welded Panel 1986	PARALLEL GAP WELDED 9 LPE GaAs CELLS 3 SERIES BY 3 PARALLEL SILVER MESH INTERCONNECT SUBSTRATE - ALUMINUM FACESHEETS ON AN ALUMINUM HONEYCOMB CORE	1200 THERMAL VACUUM -80°C TO +80°C AT AEROSPACE CORP.	NO POWER DEGRADATION PANEL TESTED 17% EFFICIENT AND CYCLING IS CONTINUING
Welded Panel 1986	PARALLEL GAP WELDED GaAs PANEL 12 LPE HET GaAs CELLS (2 x 4cm) 6 SERIES 2 CIRCUITS SILVER-PLATED KOVAR INTERCONNECT SUBSTRATE - OPEN WEAVE GRAPHITE	FLIGHT PANEL (EARLY 1987) LOW EARTH ORBIT	INFORMATION PENDING
Welded Panel 1987	PARALLEL GAP WELDED GaAs PANEL 25 LPE GaAs (2 x 4 cm) 25 CICs SERIES SILVER MESH INTERCONNECT SUBSTRATE - ALUMINUM FACESHEETS ON AN ALUMINUM HONEYCOMB CORE	500 THERMAL CYCLES -140°C TO +140°C	NO POWER DEGRADATION

SUMMARY OF SPECTROLAB EXPERIENCE IN GaAs PANEL TECHNOLOGY (CONT'D)

PROJECT NAME YEAR	CONFIGURATION OF FLIGHT TEST PANEL	CONDITIONS	RESULTS
Welded Panel 1987	WELDED GaAs PANEL 80 LPE HET GaAs CELLS (2 x 4 cm) 16 SERIES BY 5 PARALLEL SILVER-PLATED KOVAR INTERCONNECT SUBSTRATE - ALUMINUM FACESHEET ON AN ALUMINUM HONEYCOMB CORE COMBINATION OF PARALLEL GAP WELDING AND SOLDERING FOR INTERCONNECTION	PANEL SUPPLIED TO CUSTOMER FOR FURTHER EVALUATION	PANEL MEASURE 18.2% EFFICIENT WITH A 0.82 CFF AS BUILT
GaAs on Ge 1988	WELDED GaAs PANEL 3 GaAs ON Ge CELLS (2 x 2 x 0.02 cm) 3 SERIES SOLID SILVER INTERCONNECT SUBSTRATE - ALUMINUM FACESHEET ON AN ALUMINUM HONEYCOMB CORE PARALLEL GAP WELD FRONT SOLDER BACK	PANEL SUPPLIED TO CUSTOMER FOR FURTHER EVALUATION	18.1% EFFICIENT AS BUILT AND CHARACTERIZED UNDER STEADY STATE SIMULATIC
GaAs on Ge 1990	WELDED GaAs/Ge CELLS 6 CELLS IN SERIES (2 x 2 x 0.02 cm) SOLID SILVER INTERCONNECT SUBSTRATE - GRAPHITE FACESHEET ON ALUMINUM HONEYCOMB CORE PARALLEL GAP WELDED	PANEL SUPPLIED TO CUSTOMER FOR FURTHER EVALUATION	18.6% EFFICIENT AS BUILT CHARACTERIZED UNDER LAPSS SIMULATION

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