

Technology Support for Initiation of High-Throughput Processing of Thin-Film CdTe PV Modules

**Phase III Final Technical Report
14 March 1997–1 April 1998**

R.C. Powell, G.L. Dorer,
U. Jayamaha, and J.J. Hanak
Solar Cells, Inc.
Toledo, Ohio

NREL technical monitor: H.S. Ullal



National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of
the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under Contract No. DE-AC36-83CH10093

Prepared under Subcontract No. ZAF-5-14142-05
September 1998

This publication was reproduced from the best available camera-ready copy submitted by the subcontractor and received no editorial review at NREL.

NOTICE

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling (423) 576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
(703) 487-4650



Table of Contents

Table of Contents	i-ii
List of Figures	iii-iv
Abstract	v
INTRODUCTION	1
1.0 VAPOR TRANSPORT DEPOSITION	2
1.1 The Vapor Transport Deposition System	2
1.2 Glass Transport in the VTD System	2
1.2.1 The Glass Transport Sub-system	2
1.2.2 Softening of the Glass	3
1.2.3 Glass Warping	3
1.2.4 Low-Emissivity Coating	3
1.2.5 Effect of SnO ₂ Layer on Temperature Uniformity	3
1.2.6 Effect of Glass Thickness on Transport	4
1.2.7 Effect of the Thermal History of the VTD Furnace	4
1.2.8 Estimation of the Substrate Temperature	4
1.3 Metering of the Source Powders	5
1.3.1 Sources of CdS and CdTe Powder	5
1.4 Deposition of CdS and CdTe Films in the VTD System	6
1.4.1 Comparison of the Surfaces of CdTe Films Deposited by the VTD, CSS and Magnetron Sputtering	6
1.4.2 Pinholes in CdTe Layers	6
1.5 Performance of the VTD System in Production	7
1.6 Environmental, Health and Safety Issues	8
2.0 CHARACTERIZATION AND PERFORMANCE OF PV DEVICES	8
2.1 Conversion Efficiency of CdTe PV Devices	8
2.1.1 Efficiency of PV Devices Coated in the RMS System	8
2.1.2 New SCI Record Cell	9
2.2 Efficiency of PV Devices Made in the VTD System	10
2.3 Evaluation of Commercial Substrates for PV Modules	10
2.3.1 Comparison of Tec8 and Tec15 TCO Coated Glass	10
2.3.2 Comparison of TCO-coated Glass Substrates from Two Vendors	11
2.3.3 Performance of PV Devices on Thin Glass Substrates	11
2.3.4 Best Performance Achieved with a Standard-Size Module Made by VTD ...	11
3.0 CONTACT LAYERS AND SURFACES	11
3.1 Cadmium Stannate Transparent Electrode	11
3.1.1 Film Deposition and Characterization	11
3.1.2 Optical Transmission of rf-Sputtered Cadmium Stannate	12
3.1.3 Fabrication and Performance of Cells Using Cadmium Stannate Electrodes..	13
3.2 Experiments on Wet CdCl ₂ Treatment of CdS/CdTe Layers	13

4.0	ALTERNATIVE CELL INTERCONNECTS	14
4.1	The Dot-Matrix Module	14
4.1.1	DM Substrate and Layer Structure	14
4.1.2	Methods of Forming M2/M1 and M2/TCO Vias	14
4.2	Option 1 Process for DM Modules	15
4.2.1	Performance of the Modules Made by the Option 1 Process	16
4.2.2	Status of the Option 1 Process for DM Modules	17
4.3	Option 1B Process for DM Modules	17
4.3.1	Fabrication and Performance of a DM Mini-Module	18
	Made by the Option 1B Method	
4.4	Electrical Scribing Experiments	19
4.5	Evaluation of Ink-Jet Printing as a Means of Filling in Scribe-1 Isolation Lines	19
4.6	Evaluation of a CO ₂ Laser for Edge Deletion	20
5.0	INSTRUMENTATION, MEASUREMENTS AND DOCUMENTATION	20
5.1	Film Thickness Measurements	20
5.1.1	Development of an Optical Absorption Thickness Monitor	21
5.1.2	Design of a Thickness Monitor for CdTe	21
5.1.3	Thickness Monitoring of CdS by Optical Absorption	22
5.1.4	Thickness Monitoring for Production	22
5.1.5	Thickness Measurements by Spectral Reflectance	22
5.2	Improvements in Film Thickness Uniformity in the RMS System	23
5.3	Detection of Shunts	23
5.4	Contactless Measurements of the Open Circuit Voltage	23
5.5	Upgrading of the PV Current-Voltage Curve-Tracer System	24
5.5.1	Dot Cell Measurements on Large Microscope	25
5.6	Management of Experimental Data	25
5.6.1	Computer Network	25
5.6.2	Downstream database	26
5.6.3	Data Retrieval	26
5.7	Device Marking for Identification	26
6.0	STABILITY TESTING OF PV DEVICES	26
6.1	Outdoor Testing of SCI Modules and Arrays	26
6.2	Accelerated Life Testing - A Joint Effort with the National CdTe Team	27
6.2.1	Results of the First Round of ALT	28
6.2.2	Improved Detection of the 'Roll-Over' in the I-V Curves	29
6.2.3	Attempted Recovery of Degradation by Forward Voltage Bias	29
6.2.4	Future Stability Work.....	29
	SUMMARY.....	30
	REFERENCES	31
	ACKNOWLEDGMENTS	31

List of Figures

Figure #	Page
1.1	Schematic of thermal warp due to top heating. Note the potential glass transport problem due to loss of contact with the rolls in the center and the collision of the glass leading edge with next roll 32
1.2	Temperature in the VTD system measured by thermocouples located below moving glass substrates..... 32
1.3	Photomicrographs of the surfaces CdTe film coated in the VTD system (a) as-deposited sample 33 (b) CdCl ₂ heat-treated sample 33
1.4	Photomicrographs of the surfaces CdTe film coated in the RMS system by CSS (a) as-deposited sample 34 (b) CdCl ₂ heat-treated sample..... 34
1.5	Photomicrographs of the surfaces CdTe film coated by magnetron sputtering (a) as-deposited sample 35 (b) CdCl ₂ heat-treated sample 35
2.1.1	Current-voltage NREL data for a new SCI record CdTe cell having efficiency of 14.1 % 36
2.1.2	Quantum efficiency of the CdTe cell having conversion efficiency of 14.1 % 37
2.2.1	Results of the conversion efficiency of dot cells made by VTD over a four-month period, through the end of February 1998 38
2.2.2	<u>Top</u> - Progress in the average conversion efficiency of dot cells made by VTD over a three-month period, through the end of February 1998 <u>Bottom</u> - Variation in the standard deviation of the average efficiency over the three-month period (each point in both graphs represents data for 13 cells)..... 39
2.2.3	Additional results of the conversion efficiency of dot cells and modules made by VTD over an 8 month period, through the end of February 1998 40
2.4	Results for the efficiency and stability of two 1-cm ² CdTe cells deposited by VTD on 3 mm-thick, glass, module substrate 41
2.5	Performance results for one of the best 60 cm x 120 cm modules made to date on the high-throughput VTD system (aperture efficiency 8.4 %) 42
3.1	Optical transmission and absorbance of SCI sputtered cadmium stannate 43
3.2	Optical transmission and absorbance of NREL cadmium stannate and F-doped tin oxide..... 44
3.3	A contour plot of the efficiency of CdCl ₂ - treated CdTe cells as a function of heat-treatment oven temperature and time after a 7-day light soak 45
4.1	A histogram of the efficiency of 14 Dot-Matrix modules made by the Option 1 process 46
5.1 a	Portable probe for contactless measurement of V _{oc} 47
5.1 b	Portable probe in use by the PV module production group measuring V _{oc} 47

List of Figures
(continued)

Figure #		Page
6.1.1	A histogram of the temperature for SCI CdTe module on an outdoor test at SWTDI, New Mexico	48
6.1.2	Outdoor Stability data for SCI module at SWTDI, New Mexico	49
6.1.3	Outdoor Stability data for the 1.0 kW SCI array at NREL.....	50
6.1.4	Outdoor Stability data for the 1.2 kW SCI Westwood array (Array #2)	51
6.1.5	Outdoor Stability data for the 10 kW TECO array (produced by SCI)	52
6.2.1	A summary of the Accelerated Life Testing (ALT)	53
6.2.2	Progression of the inflection point in the JV curve as a function of stress time ...	54
6.2.3	Progression of the derivative minimum for different stress conditions for devices made with the standard recipe	55
A1-A15	A collection of data of the Accelerated Life Testing	56-76

Abstract

Thin-film PV devices based on cadmium telluride have been identified as one of the candidates for high-performance, low-cost source of renewable electrical energy. Roadblocks to their becoming a part of the booming PV market growth have been a low rate of production and high manufacturing cost caused by several rate-limiting process steps. Solar Cells Inc. has focused on the development of manufacturing processes that will lead to high volume and low-cost manufacturing of solar cells and on increasing the performance of our present product. The process research in Phase III was concentrated on further refinement of a newly developed vapor transport deposition (VTD) process and its implementation into the manufacturing line. This development included subsystems for glass substrate transport, continuous feed of source materials, generation of source vapors, and uniform deposition of the semiconductor layers.

Supply of glass substrates coated with transparent conducting oxide (TCO) films are an important aspect of both performance and cost of PV devices. Research and evaluation of several types of substrates has been done. Cadmium stannate, identified by NREL as a superior TCO layer has been evaluated along with intrinsic tin oxide layer as a buffer material. Research has also continued on thin CdS layers for increasing the photocurrent and thereby cell efficiency. With the goal of establishing dry processing, evaluation of tellurium as a back, interfacial layer has been continued. The vapor process for CdCl₂ treatment initiated in earlier phases has been resumed at the end of Phase III. In the interim, process latitude of the wet CdCl₂ treatment used in production has been detailed.

Research toward the improvement in device performance and stability has been addressed both on small devices grown by the stationary close-space sublimation (CSS) process and on modules made by the rapid production VTD process. Both processes required extensive characterization of materials properties, including thickness, optical transmission and electronic properties. In order to generate and handle the large volume of data required, major improvements in the test equipment and data acquisition and data processing have been made. Study of device stability has been pursued both in-house and also in cooperation with the National CdTe Team organized by NREL.

Cell interconnection for thin film modules remains as one of the major bottlenecks. One of the approaches pursued was the SCI's Dot-Matrix process. Another patterning process being explored is a non-laser ablation process.

As a result of this R&D effort, the VTD process has now achieved a status in which linear coating speeds in excess of 8 ft/min have been achieved for the semiconductor, equal to about two modules per minute, or 144 kW per 24 hour day. The process has been implemented in a production line, which is capable of round-the-clock continuous production of coated substrates 120 cm x 60 cm in size at a rate of 1 module every four minutes, equal to 18 kW/day. Currently the system cycle time is limited by the rate of glass introduction into the system and glass heating, but not by the rate of the semiconductor deposition. A new SCI record efficiency of 14.1% has been achieved for the cells. For the modules produced by the rapid VTD process the best efficiency achieved thus far is 8.4 %, compared with the record of 9.1 % for the CSS process. Three arrays and one set of modules on outdoor stability tests for up to 3 years continue showing excellent stability. The National CdTe Team has implemented an Accelerated Life Testing (ALT) program and identified a high-temperature degradation process. The effort in the SCI's Dot-Matrix process has resulted in the development of one version of the process, showing PV performance comparable to the existing 'line-patterning' process done by laser scribing. The capability of patterning of TCO layers has been demonstrated by an alternative non-laser process.

INTRODUCTION

Solar Cells Inc. (SCI) has set out to create the technology to produce photovoltaic modules in volumes sufficient to compete with the economics of conventional electric technologies. CdTe is the material of choice because of its demonstrated good performance both in the laboratory and in pilot production manufacturing [1]. Furthermore, the deposition methods under development are consistent with eventual integration with a commercial-scale, glass production line. This approach shapes both the direction of research and the priority under which experiments are performed.

The main goal of SCI is to develop an in-line system in which all sub-processes are accomplished in the same length of time. Module production consists of a dozen such sub-processes. The semiconductor deposition, CdCl₂ treatment and cell interconnection steps all required improvement in throughput. A breakthrough in the former occurred during Phase II by the demonstration of a continuous Vapor Transport Deposition process. This process has received major attention in Phase III and has now become a production process.

Work that has been initiated in Phase II on a dry CdCl₂ process for the purpose of compatibility with other in-line processes has been resumed toward the end of Phase III. Mapping out of the parameter space for the wet CdCl₂ process has been done in the interim, in support of the existing production process.

For cell interconnection, development of one version of SCI's Dot-Matrix (DM) process, employing chemical etching, has been completed in Phase III, with the achievement of module performance comparable to the laser-scribed 'line-patterned' devices. Another version, employing laser-scribing, has been demonstrated on small devices. Means of in-line patterning by parallel, multiple laser beams or other methods is also being sought to overcome this bottleneck. One promising method, shown to work on TCO, is a non-laser ablation of TCO.

Front and rear contacts are areas which are most likely to produce gains in efficiency and longevity. Included in the front contacts was work on fluorine-doped tin oxide, overlaid with a thin layer of intrinsic tin oxide and sputtered layers of cadmium stannate, first identified by NREL. Further work on thin CdS layers to decrease absorbance and thereby increase the photocurrent was also pursued.

A sustained effort in stability testing is an important activity that affects the acceptance of the PV product. This effort is being pursued by continued outdoor testing of three arrays and a set of four modules, with three years completed. Also implemented in participation with the National CdTe Team is the program on Accelerated Life Testing (ALT), in which five laboratories are participating.

Development of instrumentation and means of automated testing, data collecting and data processing has been a major activity during this phase, to keep up with the rapid throughput of the VTD deposition process.

1.0 VAPOR TRANSPORT DEPOSITION

In Phase II of the Thin Film Project SCI had developed and tested equipment for Vapor Transport Deposition (VTD) of semiconductor CdS/CdTe layers for commercial-size PV modules [2]. Films of CdTe have been deposited at growth rates more than an order of magnitude greater than the original close-space-sublimation (CSS) method [3, 4]. In Phase III this accomplishment was followed by a redesign and rebuild of the VTD equipment to take advantage in the higher throughput and to demonstrate production of uniform, high-performance PV modules on a consistent basis sustainable over extended periods of time.

1.1 The Vapor Transport Deposition System

A VTD system was rebuilt for Phase III work and for limited production of PV modules. It employs a large vacuum system that comprises front and rear load locks as an entrance and exit for the PV module glass plates, an internal roller drive mechanism for transporting glass plate substrates, a bank of electric resistive heaters for bringing the substrates to the proper deposition temperature and two vapor generator subsystems, one for CdS and the second for CdTe. The VTD system has a maximum cycle time of 2.5 minutes. This system gives SCI a capability of producing 24 coated plates per hour (or 36,000 plates, 1.8 megawatts per shift per year, at 85 % up-time, 85 % yield).

The vapor generator subsystem consists of three major components:

- 1) A "powder feeder," external to the chamber, that provides a controlled supply of powdered source materials.
- 2) A "vaporizer" that converts the source material from a solid to a vapor state.
- 3) A "distributor" that spreads the vapor out so as to ensure a uniform coating and directs the vapor to the glass plate being coated. Patents are pending on the VTD system; consequently, the details are proprietary. Basically, however, the powdered source material supplied to the system is rapidly sublimated. The resulting vapors are moved with an inert carrier gas and directed towards the glass substrate. The system is constructed from off-the-shelf industrial heating components.

1.2 Glass Transport in the VTD System

1.2.1 The Glass Transport Sub-system

Transport of glass in the vacuum coating furnace requires attention to numerous details. SCI uses a friction drive system for the rollers in the coating furnace. The drive system consists of metal-capped ceramic rolls riding upon the smooth upper surface of a wide flat drive chain. Roll rotation is induced by chain-to-roll friction instead of a positive dog-bone chain and sprocket

system. The friction drive system, which has a proven track record in the glass industry, ensures constant speed of glass transport. However, the friction drive system is vulnerable to rotation hindrance caused by mechanical misalignment, insulation misplacement, thermal expansion, lubrication loss or coating build-up on bearings and insulation. A variety of these problems have been resolved during Phase III. At this time no fundamental problems are foreseen.

1.2.2 Softening of the Glass

For best PV performance the glass substrates are preheated to temperatures approaching the softening point of the glass. Ideally, uniform temperature is desired over the entire surface. Moreover, a symmetric temperature distribution throughout the glass thickness is required to maintain flatness. Within the VTD system glass heating takes place in two steps. The first is the initial glass preheating from both sides that seeks to provide the uniform and symmetric profiles mentioned above. The second additional heating on the top side of the glass occurs as it passes under the vapor distributor that operates at temperatures at least 100 °C higher than the substrate. In order to avoid overheating of the glass a balanced heat flow from below is not used.

1.2.3 Glass Warping

The consequence of the uncompensated heating of the top surface result in bowing of the glass caused by top-to-bottom thermal expansion difference as shown schematically in Fig. 1.1. This condition could interfere with the transport of the glass. A variety of solutions have been explored until the problem was minimized. With the proper chamber heat profile bowing can be minimized, primarily because of glass relaxation upon partial softening.

1.2.4 Low-Emissivity Coating

In an effort to minimize the heating of the glass by the distributor the use of low-emissivity, high-temperature coatings over the distributor has been explored. Three different refractory ceramic metal oxides having emissivity values in the range of 0.3 were tested. Following initial bench tests that indicated the effectiveness of the coating in reducing radiative heat transport the coating was tested on the vapor distributors with fair success.

1.2.5 Effect of SnO₂ Layer on Temperature Uniformity

The initial glass heating is further complicated by the SnO₂-coated surface, used as the front electrode. Because of its low emissivity it reflects infrared radiation resulting in a lower heating rate on the coated side of the substrate. Therefore offsets in top and bottom heater set points are used to compensate for the infrared reflectivity differences. The offsets depend on the characteristics of the SnO₂ layer so that four different SnO₂ coatings used in this work require different settings.

1.2.6 Effect of Glass Thickness on Transport

The glass plate thickness has been found to be an unexpected variable affecting glass transport. Although the roll spacing in the coating furnace was designed to handle 5-mm thick glass, coating tests have been made with 3-mm thick glass substrates, which required increased transport rate in order to prevent overheating of the glass. This operation also required higher deposition rates that were achieved by the adjustment of the VTD parameters. Surprisingly, glass transport with the thinner glass resulted in fewer problems due to higher transport speed.

1.2.7 Effect of the Thermal History of the VTD Furnace

Another complicating factor in the preheating of the glass is the thermal history of the furnace. Glass input represents one of the largest heat losses in the furnace. An important mechanism involved is heating of the glass by roll contact. Initially when the chamber is first heated without glass, the rolls are overheated. As a regular glass input frequency is established, a "steady state" is achieved. During this initial equilibration time glass transport problems can occur. None of these issues were apparent in the past when the system was operated by oscillating glass within a chamber until heated. Transport problems surfaced when the VTD system using one-directional transport replaced the CSS system that used the oscillating method.

1.2.8 Estimation of the Substrate Temperature

Glass temperature and glass temperature distribution are important for both glass transport and film deposition. Measurement of the temperature of a moving substrate within a vacuum coating furnace reliably remains far from trivial. The most reliable data derives from a series of close proximity thermocouples which sense glass temperature as the glass moves through the system. Figure 1.2 shows a plot of 3 such proximity thermocouples located below the glass. Glass passage is indicated by a drop in thermocouple output as the temperature decreases from the furnace ambient as the cooler glass passes, which occurs periodically. A more reliable record of the substrate temperature will occur in a future, in-line, production system in which the glass plates will be in close proximity in a continuous stream. Most recently a port for an infrared camera has been installed and a vendor conducted some very preliminary testing that indicates the glass is substantially hotter at the edges than at the center. This is consistent with the film thickness non-uniformity that has been observed.

1.3 Metering of the Source Powders

The CdS and CdTe source powders are fed and metered into the VTD system by separate powder feeders ideally at a ratio of rates of about 1:20. From the beginning of this work many problems with powder feed were encountered. With the 'powder fines' removed, CdTe could be fed and metered reliably with relative ease. The problems with the CdTe feed were first solved by removing the fines from the milled powder. Our current vendor must recycle these fines, whereby in the short term the material costs have increased slightly. CdS presented more difficulties because of the low feed rate needed and the nature of the CdS powder. It turns out that CdTe is prepared from the elements in granular form by sintering, followed by crushing and sifting to yield a certain range of grain sizes. On the other hand, CdS is prepared by precipitation from an aqueous solution, forming a fine-grain powder having a rather open structure, containing a large amount of chloride powder and water.

There are three problems presented by the precipitated CdS powder. First, the fine powder represents a significant safety hazard as the small particles can easily become airborne. Second, the powder is quite sticky and flows poorly, thus unsuitable for reliable transfer and metering. Third, the high chloride and water content are not acceptable for CdS film deposition. Therefore a method was needed either to re-form the CdS powder or to locate another supplier. For re-forming, both cold pressing and sintering were investigated. Sintering proved to be the most reliable re-forming method. It also removes water and chloride from the material.

The sintered CdS powder is essentially free-flowing. Numerous bench-top tests with this material using the original powder feeders were made. The results indicated a substantial improvement in the powder feed. Using the sintered material in the VTD system for the deposition of CdS layers met with only a few minor flow problems.

As reported in the sections to follow the PV the film properties and PV module efficiency have improved by switching to the sintered CdS powder.

1.3.1 Sources of CdS and CdTe Powder

Currently SCI has one main supplier of both CdS and CdTe. A second supplier of CdTe was identified and qualified. For CdS several potential suppliers have been located but important issues remain unresolved. One potential CdS supplier, whose material we have qualified, is in corporate restructuring and may not be able to supply any material. Another supplier is developing an off-shore source of very economical CdS. At this point however, our original supplier remains the sole source for CdS. Unfortunately, this CdS comes as a very fine powder formed in a solution precipitation process. As a backup for insuring a reliable supply, SCI has made tentative plans to produce its own CdS powder. The required methodology for this task has been identified as well as the type and source of the equipment needed.

1.4 Deposition of CdS and CdTe Films in the VTD System

The VTD system has been equipped with two vapor distributors, to facilitate the deposition of the CdS and CdTe films in tandem or individually. One of the deposition studies was to map out the process parameters for CdS and CdTe deposition. The independent parameters included the rate of powder feed, rate of flow of the carrier gas, type of carrier gas, vaporizer and distributor temperature, substrate temperature, rate of substrate transport, background gas pressure, and the type of glass substrate and TCO.

Using the VTD system, the deposition can be controlled at will both in spatial extent and in time. A demonstration of the deposition control has already been reported in Phase II report in Fig. 1, where the coating has been turned on and off as a plate moving at constant speed passes the distributor [2]. This technique allows one to create a deposition footprint and to determine the dependent parameters including the film thickness, thickness uniformity, deposition rate, material utilization and film properties, including the PV performance parameters. Some of the thickness profiles of the deposited layers have also been shown in the Phase II report.

A map of deposition parameters for both CdS and CdTe has been successfully generated for use in R&D and production. For deposition and production rates see Section 1.5).

1.4.1 Comparison of the Surfaces of CdTe Films Deposited by the VTD, CSS and Magnetron Sputtering

The deposition rates for the VTD, CSS and magnetron sputtering of CdTe are very different. The approximate values are 73, 7.5, and 0.031 $\mu\text{m}/\text{min.}$, respectively. It is well known that large grain size, of the order of 2 μm is needed for achieving good semiconductor properties. This requirement can be satisfied in part during the film deposition and also by subsequent CdCl_2 heat treatment, which also removes many of the defects. A comparison of the photomicrographs of the surfaces of the films made by these three methods is shown in Figures 1.3 a,b, 1.4 a,b and 1.5 a,b for as-deposited and CdCl_2 -treated films. In spite of the fact that a very high rate of deposition is used for the films from the VTD process, the grain size is substantial, compared with the very low rate available in the sputtering process. The difference is due to the substrate temperature, which for VTD is about 600 $^\circ\text{C}$ compared with about 250 $^\circ\text{C}$ for sputtering.

1.4.2 Pinholes in the CdTe Layers

A distinguishing characteristic of modules showing low efficiency was the presence of a substantial number of pinholes. Most of the pinholes were yellow in color, indicating that CdS coverage is not the problem. Upon close inspection of the deposited CdS layer, various surface features generally classified as dust have been observed. These surface particulates are bonded to the surface but can be removed by wiping. The CdS surface particulates occurred preferentially near the glass edges. When a CdTe layer is then deposited, the CdS dust is merely coated over, acting as a mask. The resulting pinholes are not circular and neither is the dust. Moreover, in a test where only CdTe was coated, no dust was found. Thus, although the CdTe grows at much

higher rates, it is the prior formation of CdS particulates that is the root of the problem. The CdS surface particulates were mostly chunky with sizes as large as 100 μm . In the regions of higher dust density, CdS whiskers growing from the chunks also appeared. A full matrix of designed experiments was run varying CdS growth parameters such as deposition pressure, glass temperature, and distributor temperature, as well as Taguchi multi-variant methods. The result was that essentially no growth parameter made a significant difference with respect to the formation of CdS particles.

After changing to a sintered CdS source material, the nature and the 'number density' (density per unit area) of the CdS particulates also changed. Rather than chunky forms, CdS whiskers constituted the dust. These whiskers were $<1\mu\text{m}$ in diameter and 10 to 50 μm long and generally much finer than the chunks. Thus, the cross-sectional area of the whiskers was only about 1/100 compared with the chunks and their length about 150 times greater than the thickness of the CdS film. Because of these differences one would expect that any shunts due to the whiskers would be orders of magnitude less detrimental than those due to the chunks. Moreover, the number density was significantly lower.

Although less troublesome, the formation of the CdS whiskers should be eliminated. One of the known mechanisms of whisker growth during CVD or VTD is via vapor-liquid epitaxy. One species that might cause small pools of liquid is the chloride ion, which in the form of CdCl_2 is used as a low-temperature flux (ca. 420 $^\circ\text{C}$) for the recrystallization of the CdS/CdTe layers. Lately, the occurrence of whiskers has subsided. Should it return, a more thorough sintering of the CdS powder to remove the chloride ion may be in order.

Cleaning of the glass substrate might be another source of pinholes. A review of the cleaning procedure has taken place and recommendations have been made where potential problems were noted. One operation where possible problems exist is the seaming of the glass edges that generates ground glass dust on the surface, which, if not removed thoroughly, is known to cause pinhole problems similar to the CdS dust.

1.5 Performance of the VTD System in Production

The main objective of the Thin Film Program is to conduct research in support of the development of a commercial process for the production of CdTe photovoltaic devices. At the conclusion of the third year a major goal in this direction has been achieved. As a consequence of methodical improvements of the VTD subsystems, the glass-handling problems essentially ceased. The vapor distributor sub-system continues to show its chemical durability so that the CdTe distributor has not been changed for more than 6 weeks. With these improvements an uninterrupted production run lasting 18 hours has been demonstrated during which 140 modules were produced. During the final month, production of 500 coated plates including standard module substrates measuring 60 cm x 120 cm has been made. The line speed achieved for the deposition of both semiconductor layers was 1.38 m/min. (4.5 ft./min.) with a 5-mm thick glass substrate, 2.0 m/min. (6.7 ft./min.) with a 3-mm thick substrate, and 2.7 m/min. (9 ft/min.), with a 2.3-mm thick substrate. Currently the system cycle time is limited by the rate of glass

introduction into the system and glass heating, but not by the rate of the semiconductor deposition.

1.6 Environmental, Health and Safety Issues

A new fume hood was installed for the VTD system that meets design specification of 250 fpm face velocity at 5 inches from the hood. This will provide sufficient velocity to capture respirable cadmium particles. Cadmium air sampling results are pending.

Dr. Vasilis Fthenakis of Brookhaven National Laboratories visited SCI for an independent EHS review. The review was not intended as a comprehensive compliance audit; simply an exchange on ideas about certain key cadmium control and use issues. He recommends finding suppliers of CdTe and CdS that will provide powders without fines to aid in dust control when transporting these materials. Dr. Fthenakis also recommends venting all HEPA dust collection equipment to the outside. This is an approach that must be taken as SCI scales operations and becomes more of a production-oriented facility. For now, at least pressure differential monitoring equipment should be installed so filter condition can be determined. The OSHA Cadmium Standard mandates monitoring if HEPA particle filters are vented in the work area.

2.0 CHARACTERIZATION AND PERFORMANCE OF PV DEVICES

A two-pronged effort has been pursued toward the improvement of the performance and reliability of CdTe solar cells. One part of the effort is performed on devices deposited on 10 cm x 10 cm TCO-coated glass substrates by the CSS method in the "RMS" system, and the other part on devices deposited by the VTD method 120 cm x 60 cm substrates. The progress on the performance of the devices is presented in that order.

2.1 Conversion Efficiency of CdTe PV Devices

2.1.1 Efficiency of PV Devices Coated in the RMS System

As part of ongoing research on module efficiency improvements, SCI has sought to improve efficiency by thinning the CdS layer. This requires that an intrinsic SnO₂ buffer layer be deposited between the TCO and CdS. Some research groups have postulated that the intrinsic SnO₂ layer reduces the effect of direct shunts because CdTe is said to form a better junction with intrinsic SnO₂ than with fluorine-doped SnO₂. If this were the case, then cells grown on intrinsic SnO₂ without a CdS layer should have acceptable performance.

To test this hypothesis, devices were processed on two 10 cm x 10 cm LOF Tec8 plates. Both plates were coated with a 3700 Å SnO₂ buffer layer. The first plate (labeled N2688) was then coated with 700 Å of CdS, 4μ of CdTe and processed into 1 cm² dot cells. The second plate (N2689) was similarly processed but without the CdS layer. Results in Table 2.1 would suggest the SnO₂ couldn't be used in place of the CdS. It should be noted that the intrinsic SnO₂, with a resistivity of 150 Ω-cm, should not introduce any significant series resistance.

Plate #	Substrate	SnO ₂ Buffer Layer Thickness (Å)	CdS Thickness (Å)	Avg. Voc mV	Avg. Jsc mV	Average Cell Efficiency (%)
N2688	LOF Tec8	≈ 3700	≈ 700	806	19.2	10.4
N2689	LOF Tec8	≈ 3700	0	255	16.0	1.7
N2692	Low-Fe glass with NREL TCO	≈ 1100	≈ 700	823	21.7	12.70
N2691	LOF Tec8	≈ 1100	≈ 700 (sputtered)	558	22.3	7.02
CD2	7059 glass with NREL CTO	0	≈ 1500	833	21.4	12.4

Thin CdS films grown in the RMS using the CSS process have always appeared to exhibit small pinholes that can cause shunts. Sputtered films, in contrast, appear to be pinhole free. Cell batch N2691 was fabricated to test the compatibility of sputtered, pinhole free, CdS with CSS CdTe. The CdS layer was grown at the University of Toledo while the CdTe layer was grown in the RMS at SCI. Although the Jsc was very high (see Table 2.1) the performance was poor due to low V_{oc} values. It is speculated that since the sputtered films have smaller grains the inter-diffusion occurring during the chloride treatment could be much greater resulting in too great a thinning of the CdS. It is obvious there is a dynamic interplay between the CdS thickness, grain size and chloride treatment.

Cadmium stannate (Cd₂SnO₄ or CTO) is an alternative TCO being investigated by Pete Sheldon's group at NREL. It is reported to have superior performance to the SnO₂:F presently supplied by LOF. We have fabricated cells grown on 7059 glass/cadmium stannate supplied by NREL and found it to be superior to the LOF Tec8 TCO. We achieved 12.4% on this substrate compared to 11.4% using LOF Tec8 under identical fabrication conditions.

2.1.2 New SCI Record Cell

The RMS was used extensively to make cells for the March deliverables. Several cells with efficiency over 13 % and mini modules with efficiency over 10 % were made. One of these cells, having an area of 1.1 cm², tested at NREL had efficiency of 14.1 % as shown in Fig. 2.1.1. A description of the type of substrate used is in Section 3.1.2. Figure 2.1.2 shows the QE curve of a cell with thin CdS, which was on the same substrate that was used for SCI's new record cell.

2.2 Efficiency of PV Devices Made in the VTD System

Figure 2.2.1 shows results of the conversion efficiency of dot cells made by VTD over a 3-month period, through the end of February 1998, while Figure 2.2.2 shows the progress in the average efficiency and standard deviation with time. Figure 2.2.3 shows similar data for modules made by the CSS and VTD methods over a 11-month period. Many modules made by VTD in the early production runs had low efficiency. Early in February the devices began to exhibit a more normal behavior. The efficiency of interconnected minimodule made of material from large coated plates rose to between 7.8 and 9.0 %.

2.3 Evaluation of Commercial Substrates for PV Modules

The choice of the glass substrate may have significant impact on manufacturability, production throughput, power output, product reliability and cost. As already stated in the preceding section, the transport of glass was affected by the glass thickness. It is also well known that increased glass thickness lowers the photocurrent. Ordinary soda-lime glass, which is most cost-effective, contains iron that absorbs a part of the incident light, thereby lowering the current. The "water-white," iron-free glass solves this problem, however, at an added cost. Different transparent front-electrode materials (TCO) such as tin oxide ($\text{SnO}_2\text{:F}$) and cadmium stannate [5] can affect the manufacturability, performance and the cost of modules. In this sections some results of the evaluation of some of the glass substrate candidates coated by VTD are presented. The glass used in these tests was the low-cost, 5-mm thick, soda-lime glass.

2.3.1 Comparison of Tec8 and Tec15 TCO-coated Glass

In the following tests a comparison of the performance was made of PV devices deposited by CSS or VTD on 5-mm thick soda-lime glass substrate coated with Tec8 or Tec15 $\text{SnO}_2\text{:F}$ electrodes having a sheet resistance of approximately 8 and 12 Ohm/sq., respectively.

In one test a comparison of PV performance on 1.1 cm^2 dot cells made on 2 standard-size module substrates has shown a 10+% efficiency for both types of TCO, indicating that Tec15 coated glass might be a low-cost candidate for module production. The apparent trade-off between the two coatings is that the former, having a lower sheet resistivity has a lower resistive power loss, whereas the latter, being thinner, has a lower optical loss and greater photocurrent.

A retrospective summary of data on extended life testing over the past several years for cells using CSS material on Tec15 substrates indicate acceptable long-term stability.

Several tests have been completed comparing the performance of full modules made on glass substrates coated with Tec8 and Tec15 TCO layers. The results were comparable, indicating that Tec15 can be used for modules. Some of the tests on full modules show a slight performance advantage of TEC15 over TEC8. On the basis of these results, a change to Tec15 substrates has been made that results in considerable cost savings in production.

2.3.2 Comparison of TCO-coated Glass Substrates from Two Vendors

A shipment of 10 standard-size substrates coated with tin oxide TCO on 5-mm soda-lime glass have been received from a Vendor B. Several large modules and a piece with dot cells were processed. The average module efficiency was somewhat lower, but more disconcerting was nearly a one order of magnitude increase in TCO resistivity during processing noted on the dot-cell sample. There had been no change in the resistivity of the TCO in Vendor A material. The conclusion at this stage is that TCO made by Vendor B is far less stable at high temperatures in vacuum. More experiments and interaction with the vendors are warranted since a second supplier is desirable.

2.3.3 Performance of PV Devices on Thin Glass Substrates

CdS and CdTe films were coated onto 3-mm thick 120 cm x 60 cm substrates using vapor transport deposition in a further search for more cost-effective substrates. Figure 2.4 shows the performance results of a set of 1.1 cm² dot cells made on these substrates. The cells were subjected to 1 month of light soak at 65°C under open-circuit conditions. The initial performance is similar to that expected from the established process. With respect to stability, one of the devices continues degrading while the other shows a stable behavior after the second month.

2.3.4 Best Performance Achieved with a Standard-Size Module Made by VTD

Current-voltage data taken under AM1.5 illumination for one of the best 120 cm x 60 cm modules made by the high-throughput VTD process to date are shown in Figure 2.5. Its aperture efficiency was 8.4%, compared with our record module of 9.1% made by CSS, verified by NREL.

The main remaining issues for the VTD process are the control of the thickness and uniformity of the CdS layer by improving the source distributor, elimination of dust and pinholes in the CdS layer, the use of sputtered tin oxide buffer layer, adoption of a vapor method for the treatment of CdTe surface with CdCl₂, improved back contact and improved quality of laser scribing.

3.0 CONTACT LAYERS AND SURFACES

3.1 Cadmium Stannate Transparent Electrode

3.1.1 Film Deposition and Characterization

Wu et al. [5] reported that cadmium stannate used as the front electrode in CdS/CdTe solar cells can enhance their performance because of higher conductivity and optical transmission than TCO made of tin oxide. Study of this material begun earlier is continuing. The films were deposited on

1-mm thick BF-37 glass in a rf sputtering system. The deposition parameters were as follows; Ar flow rate of 2.66 sccm, O₂ flow rate of 8 sccm and rf power of 400 W. The deposition rate was close to 100 Å/min. The films were annealed for about 20 minutes in the presence of CdS vapor, in an atmosphere of nitrogen at 200 Torr, at a temperature of about 640 °C. In order to prevent CdS from getting deposited on the cadmium stannate, the film was held at a slightly higher temperature than the CdS source. After the annealing, the films became very transparent and the resistivity decreased by several orders of magnitude. The sheet resistivity was in the range of 3-4 Ω/□ depending on the thickness. One of the annealed films was sent to Dr. Pete Sheldon of NREL for extensive characterization. Table 3.1 lists some of the important parameters.

Table 3.1 Selected Physical Properties of Sputtered Cd ₂ SnO ₄ Films on Glass						
Sample Source	Thickness (nm)	n (cm ⁻³)	μ (cm ² /Vs)	ρ (Ω cm)	R _{sheet} (Ω/□)	RMS roughness ^a (nm)
SCI	566	6.87×10 ²⁰	43.3	2.1×10 ⁻⁴	3.88	6.4
NREL ^b	510	8.94×10 ²⁰	51.6	1.28×10 ⁻⁴	2.58	2.0

^a Roughness was measured using atomic force microscopy (AFM)

^b NREL program review 1996, page 696

The optical transmission data are shown in Figures 3.1 and 3.2. It can be seen that except for the surface roughness, the SCI material is comparable to material prepared at NREL. The slight differences in the electrical parameters could be attributed to differences in process conditions. For example at NREL, cadmium stannate is sputtered in a magnetron system in pure oxygen environment, and the annealing is done in an Ar atmosphere.

The surface of the SCI cadmium stannate films seem to be rougher than the films prepared at NREL although they are still much smoother than commercial tin oxide based TCO (roughness ~21 nm). The most probable reason for greater roughness is substrate heating during the film deposition. Although we do not intentionally heat the substrate, during deposition the substrate is heated to over 150 °C due to the heat generated in the rf system. At NREL the substrate is mounted on a water-cooled stage to keep the substrate cool during the film deposition.

3.1.2 Optical Transmission of rf-Sputtered Cadmium Stannate

Fig. 3.2 compares the light transmission of cadmium stannate (CTO) and fluorine-doped tin oxide. It can be seen that the light transmission of CTO is better than that of tin oxide in the wavelength range of 400-1200 nm while below 400 nm tin oxide transmits light better. Most of the CdTe solar cells have very little current response below 400 nm. Therefore, for most cases, replacing tin oxide with CTO should result in a higher current. However, cells with a very thin CdS layer have considerable current response below 400 nm. For example, the record cell made at GPI had

more than 80% absolute quantum efficiency at 400 nm. Fig. 2.1.2 shows the QE curve of a cell with thin CdS, which was on the same substrate that was used for SCI's new record cell of 14.1 %. It can be seen that the QE of this cell below 400 nm is better than the light transmission of CTO below the same wavelength. Therefore for cells with very thin or no CdS layer, rf-sputtered cadmium stannate might not be a better TCO than the F-doped tin oxide.

It should be pointed out, that this problem of optical transmission below 400 nm did not appear with the NREL CTO films. They also have the same problem if the films are thick, so that the sheet resistivity is about $3 \Omega/\square$. However, if the films are thinner, so that the sheet resistivity is about $8 \Omega/\square$, then the blue cutoff moves to shorter wave lengths. They claim that the band gap is dependent on thickness [5].

3.1.3 Fabrication and Performance of Cells Using Cadmium Stannate Electrodes

Four substrates coated with cadmium stannate were used to fabricate CdS/CdTe cells in which the CdS layer had a thickness of about 200 nm. The initial efficiencies were close to 10% and after one to two days of light soak pushed the efficiency to 11+% range. Diagnostics of the cells revealed that during a CdCl₂ thermal treatment of 15 minutes at 395 °C almost all the CdS was consumed. Work done at NREL has shown that cells grown on CTO in fact need a less rigorous chloride treatment. This result clearly shows that the CdCl₂ treatment has to be re-optimized for cells using cadmium stannate.

3.1.4 Experiments on Wet CdCl₂ Treatment of CdS/CdTe Layers

With recent emphasis on increasing the performance of CdS/CdTe cells, especially the V_{oc} and J_{sc} , it was decided to establish the operating conditions for several processes in a more definitive manner. One of these processes is the wet CdCl₂ treatment of the CdS/CdTe layers. A set of experiments was designed to establish the minimum and maximum times and temperatures for the heat treatment, following the application of a thin layer of the cadmium chloride from a liquid solution. In the first series of experiments the temperatures and times selected ranged from 390°C to 450°C and treatment soak times from 5 to 35 minutes. The oven used was a small research oven and the device used was #20837 deposited on a 5-mm thick glass substrate from a past CSS production run. The 120 cm x 60 cm substrate was broken into 10 cm x 10 cm pieces and after each treatment the normal standard SCI process for applying IFL was completed. Then 18 "dot cells" 1.1 cm² in area were made on each sample. Performance data were taken on all the active dot cells and the number of shorted dot cells was noted.

A set of initial results of device efficiency after a 7-day light soak is shown in a contour plot in Figure 3.3. As the plotted data also covers regions away from optimal treatment, some of the extrapolated values become unrealistic (i. e., negative values). Further work is in progress that is expected to define the regions of interest with required accuracy.

4.0 ALTERNATIVE CELL INTERCONNECTS

4.1 The Dot-Matrix Module

The development of the Dot-Matrix (DM) module continued from Phase I. The objective for Phase II was to fabricate 120 cm x 60 cm Dot Matrix interconnected modules which exhibit efficiencies comparable to modules interconnected by the standard line-patterning technique. One of the designs of the DM interconnected modules consists of 44 cells measuring 5.1 cm x 29.5 cm connected in series. The module is conveniently divided into four quarter panels that can be tested individually to determine uniformity.

4.1.1 DM Substrate and Layer Structure

The reason for pursuing the development of the DM module is to (1) expedite the production process (2) make it possible to use 5 to 15 times wider cells than the usual "line-patterned" devices, (3) increase the efficiency by increasing the active cell area, and (4) to allow for using thinner TCO, thereby decreasing the cost of the substrate and increasing light transmission into the module. What makes these improvements possible is the addition of a second metallic electrode M2 that is connected through a matrix of vias to the TCO to improve the collection of the photocurrent. The M2 electrode is insulated from the first metal electrode M1 by means of a dielectric layer structure of the DM module which is described next. The arrangement of the layers of the finished module is glass/TCO/CdS/CdTe/IFL/M1/P1/M2/E in which TCO is the transparent conductive oxide, CdS/CdTe are the semiconductor layers, the IFL is the interfacial layer or layers, M1 is the first multi-layer metal electrode, P1 is perforated polymer, M2 is the second multi-layer metal electrode, and E is encapsulation (not yet developed for the DM modules). The materials for this structure, past the CdTe layer and CdCl₂ treatment have been developed in Phase I of this project.

4.1.2 Methods of Forming M2/M1 and M2/TCO Vias

The most critical process steps and materials to the development of the DM process are (1) the selection of the dielectric layer, (2) the method of forming vias in the dielectric material and in the underlying active layers, and (3) the electrical insulation of the rims around the vias to prevent shunting between M1 and M2/TCO.

Numerous methods of the formation of M2/M1 and M2/TCO vias have been proposed and explored in the current and previous programs. In our earlier program grit blasting was found to be effective in ablating the deposited layers in the M2/TCO vias, which resulted in the fabrication of a mini-module having a 9.3% efficiency. In Phase II the vias in the dielectric layer are formed by mechanical perforation in the Option 1 process and by laser ablation in Option 1B. In the same vias the deposited layers M1 through CdS are removed by wet chemical etching on Option 1 and

by laser ablation in Option 1B. The two process options are outlined in Tables 4.1, and 4.3 and described below.

4.2 Option 1 Process for DM Modules

The steps used in Option 1 are outlined in Table 4.1. The M1 and M2 are metallic layers formed by a physical vapor deposition (PVD) process, which at this time is magnetron sputtering. The M1 multi-layer is sputtered over the interfacial layer and the M2 over the subsequent P1 polymer film, which is pre-perforated by a vendor with M2/M1 and with M2/TCO vias. The perforated polymer serves as a dielectric layer, separating the M1 and M2 electrodes, and as an etching mask. The perforations are for vias connecting M2 to TCO. They measure 0.150 cm in diameter are arranged in a square pattern, in which the centers of the closest neighboring holes, or vias, are 0.090 cm apart. The perforated holes cover 2.1% of the total area.

The polymer is applied by a simple thermal lamination process in a roll laminator. The removal of the deposited layers from the M2/TCO vias is by means of three chemical spray-etching steps, each followed by water rinsing and, finally, by ultrasonic rinsing in de-ionized water. Masking of the M2/M1 vias during the etching is essential for protecting M1 from being eroded. At present an adhesive tape is used. For production, a mechanical mask and an in-line process are proposed. A thermal reflow of the polymer around the etched vias is used to eliminate shunts and shorts between M2 and M1 and to provide a continuous surface for interconnecting the M2 film with the

Step No.	Process
1	Start with a substrate processed through: glass/TCO/CdS/CdTe/IFL/M1
2	Laser scribe #1, ~5 cm spacing, 12 X (60 cm), 2Y (120 cm) scribe lines to isolate the cells down to the glass
3	Post-metalization heat treatment, 220 °C, 20 min.
4	Laminate a suitable perforated, polymer to module in a roll laminator
5	Etch M1 in M2/TCO holes and rinse
6	Etch CdTe/CdS in M2/TCO holes and rinse
7	Re-etch M1 in M2/TCO holes and rinse
8	Rinse in an ultrasonic bath with deionized water
9	Reflow polymer around the M2/TCO holes and anneal; cool
10	Sputtering of M2 metal electrode
11	Laser scribe #2, ~ 5-cm spacing, 12 X, 2Y scribe lines through the M2 to isolate adjacent cells and complete cell interconnection
12	Trim polymer and apply bus bars
13	To PV test and encapsulation

TCO. There are two sets of cell-isolation scribe lines. The first set of isolation lines from M1 to the glass is done conveniently by laser scribing. For the second set of isolation lines through M2 to the dielectric layer a masking tape has been used. Laser scribing of the isolation lines in the M2 has now been demonstrated on minimodules. For the demonstration of the feasibility of production practical DM modules twenty 60 cm x 120 cm substrates were coated up through the CdTe layer and then processed through the sputtering of first metal layer (M1). Fourteen of the substrates were used to make modules by the Option 1 process.

4.2.1 Performance of the Modules Made by the Option 1 Process

Performance tests were conducted as the fabrication of the DM modules was taking place. These tests included low-light Voc (LLVoc) on individual cells and I-V performance under AM-1.5 illumination for the total module and the quarter modules. From these data power and efficiency losses were observed that were related mainly to a) high R_{oc} , most likely due to contact resistance at the M2/M1 and/or M2/TCO contacts, b) low R_{sc} , due to electrical shunts and shorts and inhomogeneity of the deposited film. The LLVoc data corroborated the presence of shorts and shunts. The combination of high R_{oc} and low R_{sc} give rise to a low fill factor which is the main source of the power loss. The following technical issues have been identified:

- debris from the perforation that clings to the polymer that needs to be removed
- jagged edges in the perforated round vias
- persistent occurrence of shunts around the etched vias
- elevated contact resistance in the vias
- long duration of the chemical etch step

The following methods have been attempted and results obtained to resolve the issues:

- Thermal formation of vias in polymer dielectric by a laser beam produced smooth edges (see Option 1B).
- Segmenting of series-connected cells into parallel-connected columns to minimize power losses due to shunts resulted in a slightly improved performance.
- Locating shunts with a liquid crystal film and removing them by etching was fairly effective, but time-consuming.
- SEM did not indicate the presence of an organic film in the vias.
- Exposing the vias to u. v. light to burn off any organic films in the vias to lower contact resistance showed no effect.
- Rinsing the vias with an organic liquid showed some decrease in contact resistance.
- Increasing the size of the M2/M1 vias produced a substantial decrease in R_{oc} and an increase in efficiency, indicating contact resistance problems.
- In isolated cases, 4-hour light soak reduced shunts in the vias and increased efficiency.

One of the better modules made, #20766, that had initial aperture efficiency of 6.98% was selected for improvements by some of the methods listed above. First it was diagnosed as having a total of 45 shunts have been located in the M2/TCO vias. They were distributed in the quarter-

modules as follows: A - 2 shunts, B - 4 shunts, C - 26 shunts, and D - 13 shunts. The shunts were removed by chemical etching of M2 within the vias. There were also 32 shunts occurring within the cells outside of the vias; these could not be repaired, as they were under the polymer. Other improvements included painting the remaining M2/TCO vias with silver paint to enhance the contacts. The I-V results for this module are shown in Table 4.2. Data for the four quarter-modules after the repairs and light soak are also shown. As a result of the repairs the overall aperture-area efficiency for the module increased from 6.98% to 7.38% and the efficiency of quarter-modules A and B increased to 7.97% and 8.03%, respectively. The average aperture efficiency of the two adjacent quarter-modules A and B was 8.00%, which was the initial goal for a full DM module efficiency in this program.

Module Number	Format	Aperture Eff. (%)	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	R_{sc} (Ωcm²)	R_{oc} (Ωcm²)
20766	full module	7.38	787	17.6	54.2	567	13.8
20766-A	1/4 module	7.97	798	18.1	56.4	1279	13.2
20766-B	1/4 module	8.03	795	17.9	57.6	1627	12.7
20766-C	1/4 module	6.91	770	17.2	53.1	688	14.5
20766-D	1/4 module	6.46	748	16.9	52.1	512	14.4

*Note: Values in bold numerals signify new record for DM quarter-modules, an average of 8.0%.

4.2.2 Status of the Option 1 Process for DM Modules

A histogram of the aperture efficiency of the Dot Matrix Modules made by Option 1 is shown in Figure 4.1. The status of Option 1 is as follows:

- The best aperture-area conversion efficiency for a full module was 7.42%
- Two adjacent quarter-modules on the same substrate achieved efficiency of 8.0%
- A histogram of 14 DM modules shows conversion efficiency ranging from 5.5 to 8.0%, for an average of 6.43%, compared with an average of 7.24% for 24 line-patterned, standard production modules made of the same batch
- Persistent occurrence of shunts in the M2/TCO vias prompted the shifting of the effort to exploring other methods of forming the vias.

4.3 Option 1B Process for DM Modules

Option 1B, referred to as the “All Laser DM Cell Interconnection Method” outlined in Table 4.3 is in a number of ways similar to Option 1 with the following differences. One of them is the use of a non-perforated dielectric organic film, suitable for laser ablation, that is not pre-perforated. Another difference is that the M2/M1 and the M2/TCO vias in the dielectric layer and in the

Table 4.3 Outline of the Option 1B Dot-Matrix Process Using Laser Scribing

Step No.	Process
1	Start with a substrate processed through: glass/TCO/CdS/CdTe/IFL/M1
2	Laser scribing #1, ~5 cm spacing, 12 X (60 cm), 2Y (120 cm) scribe lines to isolate cells down to the glass
3	Laser scribing #2 of wide lines, in between and perpendicular to the scribe #1 lines
4	Post-metalization heat treatment, 220 °C, 20 min.
5	Apply an opaque polymer or paint to module over M1
6	Laser scribing of scribe #3 lines, narrower and shorter than and superimposed over the scribe #2 lines to form vias down to the TCO
7	Laser scribing of scribe #4 lines, parallel with the scribe #1 lines, to form vias to M1
8	Sputtering of the M2 metal electrode layer
9	Laser scribe #5, ~ 5-cm spacing, 12 X, 2Y scribe lines through the M2 to isolate adjacent cells and complete cell interconnection
10	Apply bus bars
11	To PV test and encapsulation

deposited layers are formed by means of laser ablation. The method is designed to circumvent completely the incidence of shunts or shorts within the M2/TCO vias by means of sequential, superimposed laser scribing (steps 2 and 5) and the application of the dielectric layer in-between (step 4).

The substitution of chemical etching by laser ablation removes all but one of the technical issues encountered in Option 1, which is elevated R_{sc} . Moreover, there is a gain in the useful cell area because of the well-defined and narrow laser beam. An additional important advantage is that the periphery of the ablated polymer is smooth and the ablated hole is such that it is wide at the top and narrow at the bottom. This shape precludes the formation of overhangs of the M1 over TCO that has been a source of shunts.

4.3.1 Fabrication and Performance of a DM Mini-Module Made by the Option 1B Method

Four two-cell DM mini-modules were fabricated using black paint as the dielectric layer and having a unit cell aperture areas of 32 cm². By oversight, the post-metalization heat treatment (step 3) had been omitted, which is required for developing a full value of V_{oc} . Nevertheless, the initial aperture-area efficiencies were 7.24%, 6.86%, 4.31%, and 3.98%, with V_{oc} ranging from 763 to 643 mV. Some incidence of shunting has occurred within the #4 scribe lines in spots

where the laser beam had penetrated through to the CdS layer. A modification of the scribe #4 procedure is warranted.

This result is very encouraging because of (a) the use of a potentially rapid, dry method, (b) the use of a cost-effective dielectric layer, (c) no apparent occurrence of shunts within the M2/TCO vias in the case of good scribing registration. A surprising result is that although there are 5 separate scribing steps as compared with 3 steps for the standard Line-Patterning Method, the actual total length of the scribe lines and the scribing time would be cut approximately by nearly 50%.

A single attempt was made to fabricate a full module by the Option 1B process. An aesthetically pleasing module was made, however it suffered from shunts and shorts in the M2/TCO vias on account of inadequate registry of the scribe #2 and scribe #3 lines. The reason for this problem was inadequate positioning reproducibility of the existing laser system. For this reason the work on the Option 1B process is on hold. It is anticipated that its development will be resumed.

4.4 Alternative Patterning Procedure for Cell Interconnection

We have experimented with a non-laser patterning method and demonstrated that it was suitable for scribing conducting tin oxide. The method is proprietary and it will be described in future reports.

4.5 Evaluation of Ink-Jet Printing for Filling in Scribe-1 Isolation Lines

In May, 1994 a vendor was invited to SCI to demonstrate the use of an ink-jet printer as a possible means of filling in Scribe-1 cell isolation lines. The demonstration was successful -- a three-cell, line-patterned device yielded aperture-area efficiency of 6.88%. A new visit by the same vendor was scheduled for mid September to determine the feasibility and get a cost estimate for incorporation of a jet printer on a module processing line.

The vendor made available a commercial ink-jet printer to SCI on a 2-1/2-week loan. The unit was mounted on the ILM laser table and a procedure was established for filling the S-1 scribe lines with ink on line-patterned modules to act as insulator. The printing logic was modified to draw continuous lines, 24 inches in length, to span the entire length of the S-1 scribe lines on our modules. SCI scientists then designed and had fabricated a bracket to mount the print head on the ILM laser carriage.

Four 60 cm x 60 cm modules fabricated using this procedure have shown aperture-area efficiency of up to 7.78%. This result establishes ink-jet filling as a potential replacement for the existing method of insulating the scribe #1 lines.

4.6 Evaluation of a CO₂ Laser for Edge Deletion

The CO₂ laser delivers very high power and, with a defocused beam, it is capable of cutting a wide path in the work piece. Consequently, two visits to a vendor have been made to evaluate the feasibility of edge deletion of all deposited layers in PV modules. The demonstration was successful. Single scribe lines of up to 6 mm in width were made through all the layers from the standard metal electrode down to the glass. Along with the layers up to about 0.5-mm thickness of the glass was also removed. The reason for the ablation of the glass was that the metal layer initially reflects the beam radiation thereby requiring high power to cut through the metal. Once the metal is ablated, there is still more than enough power to cut through the rest of the layers as well as into the glass. Scribing cells without the metal layer required only half the power; in this case the glass was still ablated significantly, the reason being that CdTe transmits the infrared light at this wavelength, whereas glass absorbs it. The scribing rate was conservatively estimated at 200 cm/min. The conclusion is that this method is potentially feasible for edge deletion that could be done within less than one minute per module. The estimated capital cost of the equipment is about \$375 K. Because of the high cost, lower-cost mechanical alternatives will be explored.

5.0 INSTRUMENTATION, MEASUREMENTS AND DOCUMENTATION

SCI is actively searching for methods to measure the module properties using non-destructive methods at various stages of its fabrication so as to insure good product yields. The objective is to develop and employ methods capable of making made in-situ measurements for use in closed loop mode to automate the process. Three of such properties are the semiconductor film thickness and its uniformity, the open circuit voltage (V_{oc}) of devices in process and the current-voltage characteristics, including device efficiency.

Another objective is automated data collection, processing, storage, retrieval and communication between R&D and production. Implementation of this technology has been one of the priorities in Phase III.

5.1 Film Thickness Measurements

Routine monitoring of film thickness is important for the deposition process development. For absolute film thickness measurements a stylus step profiler can be used. For large modules one needs a much faster non-destructive technique. At SCI beta-back scattering technique is used to estimate the film thickness over a large area. This technique works well with thick CdTe films; but for thin CdS long integration times are required to get an accurate measurement, however, it was still in use as of the end of Phase III. This technique also requires the monitor head to be in

contact with the film. For routine thickness measurements a much faster contactless technique would be desirable.

5.1.1 Development of an Optical Absorption Thickness Monitor

For automated film thickness monitoring a thickness monitor based on optical absorption has been under development. In this system the thickness is estimated from the attenuation of a nearly monochromatic light beam with known intensity when it passes through the film. For good sensitivity the film should attenuate the light beam adequately but not excessively. For semiconductor films this means using a wavelength comparable to the optical band gap. If the light beam is attenuated too much, the method becomes inaccurate. Thus the choice of the wavelength depends on the absorption coefficient and the intended thickness of the film. Another important factor to consider is the effect of the pin holes, which cause serious errors in underestimating the thickness. Because of a large difference in band gaps of CdS and CdTe, two different light sources are required. Generally a deep blue light source is used for CdS while a deep red source is used for CdTe.

Gas lasers such as He-Ne and Argon have been used in the past for CdS and CdTe film thickness measurements. In the equipment being developed at SCI, newly developed semiconductor light sources will be used because of numerous advantages they have. A diode laser operating in the range of 780-820 nm would be appropriate for CdTe and a source of blue light for CdS.

5.1.2 Design of a Thickness Monitor for CdTe

Light transmission spectra were taken through solar cells having CdTe layers of 2- μm and 4- μm thick, both grown in the VTD system. In both samples, the transmission at long wavelengths is virtually independent of the wavelength. However, the light transmission through the 4- μm sample was unusually low compared with that of the thinner sample. This was probably due to the light scattering from the much rougher CdTe surface of the 4 μm sample. The surface roughness increases significantly when the film thickness is increased because of the increase in the grain size. This observation indicates that a detector for diffuse light should be used to measure light transmission when surface roughness is present.

The thickness monitor should have a detection limit of at least 4 μm for CdTe. If the incident beam has an intensity of few milliwatts then with digital lock-in techniques one can measure an attenuation of about 10^5 with a good signal-to-noise ratio. Therefore a laser diode operating at the 810-820 nm range would be suitable for a detection range of at least 4 μm . However, a laser diode in the desired wavelength was not readily available. Hence a 780-nm laser diode was used instead. Still, attenuation by a 4- μm thick CdTe layer made in the VTD system was too high for an accurate detection. In fact the photoluminescence was much larger than the transmitted light. However, for samples up to about 2.5- μm thick the thickness monitor performed well.

The preceding data indicate that optical attenuation in thick CdTe films is much greater than what it should be due to the scattering at the CdTe surface. This greater optical attenuation requires using laser light with a wavelength close to the band edge so that the light transmitted is within the detectable limit for thicker films. However, on thinner films using the same laser would result

in poor resolution. Hence, for constructing a practical system it was decided to use two lasers, one operating at a wavelength of about 780 nm for thinner films and one operating at about 820 nm for thicker CdTe films. The appropriate laser will be selected by the computer depending on the light attenuation, i.e., film thickness. It was also decided to use a fiber optic patch cord to deliver the laser light on to the film. Using optical fibers will make it much easier for the two laser beams to be combined and also would isolate sensitive laser diodes from the moving parts.

For combining the two laser beams and coupling them to the optical fiber an optical system was built on a small bread board, consisting of infrared mirrors, lenses and kinematic mounts. A five-meter long, step-index silica fiber with a 200 μm core was selected to guide the light to the film. In order to make a scanning system for the thickness monitor several linear sliding systems were evaluated. A belt driven liner slide was selected because of the lower cost and faster speed. These slides can be moved as fast as 1 m/s and have an accuracy of better than 0.3 mm over a 60 cm traverse. Two slides are needed to move the light source and the detector together. Two synchronized stepper motors will drive the two slides.

5.1.3 Thickness Monitoring of CdS by Optical Absorption

A transmission spectrum of a 2500 Å thick CdS layer grown on a glass substrate LOF TEC 8 was measured. In the 400 - 490 nm range light is readily absorbed in the film. Unfortunately no semiconductor laser diode is available in this range. Therefore it was decided to use a narrow-band light source operating around 460 Å. The light output of this source is about 2 mW, which is comparable to that of a low-power laser diode. The emission spectrum of this diode was measured, showing that almost all the light is emitted below 490 nm, making this LED well-suited for CdS thickness monitoring.

5.1.4 Thickness Monitoring for Production

In the final month of Phase III, implementation of the optical absorption monitor for film thicknesses for the VTD production system has begun. While the monitor was being tested on the bench, preparations were made to gain experience with the mapping capabilities. A large traveling microscope X-Y table is used for this purpose.

5.1.5 Thickness Measurements by Spectral Reflectance

While optical absorption is the fastest thickness measurement technique, it is vulnerable to coating on the backside of the glass. As the backside coating of CdS and CdTe has not yet been eliminated, additional commercial options are being examined. Furthermore, to implement a CdS thickness mapping system in-situ, through ports and optical alignment are required. One option free from these problems is spectral reflectance. A manufacturer has been identified that makes an inexpensive unit that acquires full spectrum reflectance and then performs calculations to yield film thickness and index of refraction. The unit requires only one port, and has been used for monitoring in-situ growth. Testing at the vendor's facility is underway.

5.2 Improvements in Film Thickness Uniformity in the RMS System

The RMS system is used for the deposition of semiconductor layers and interfacial layers (IFL) onto 10 cm x 10 cm substrates using the CSS method. This system is dedicated for the optimization of the PV performance of CdS/CdTe solar cells and mini-modules. Measurements of the thickness of the deposited layers indicated significant non-uniformity over the area of the substrates. Consequently, the relevant parts of the system have been rebuilt. For this purpose CFD simulation program was used to model the temperature distribution of the source boats. After a few iterations that included boat redesign, different boat material, low-emissivity coating and radiation shields, satisfactory temperature and thickness profiles were obtained. The normalized thickness of the CdTe films ranged from 100% at the center to ~80% outward, before decreasing further at the corners.

After it was found that the CdTe uniformity could be improved by inserting a radiation shield in the middle of the boat, the same technique was applied to the CdS boat to improve the film uniformity. Addition of the radiation shield improved the film uniformity significantly. A thickness profile was determined, showing the normalized thickness diminishing from 1.0 at the center to ~0.7 at a radius of 5 cm from the center. The growth rate of the CdS film was also measured using the optical thickness monitor. The growth rate was time-dependent, as the substrate was apparently heated by the CdS boat, which was held at 710 °C. At 10 min. the rate was ~135 nm/min., decreasing to ~ 110 nm/min. at 20 min.

5.3 Detection of Shunts

In thin film PV devices shunts are a common occurrence that diminishes the device performance. Various ways of dealing with the shunts exist. At present the goal is to find a reliable and rapid method of identifying them, counting them and recording their location for their subsequent possible elimination. To date, temperature-sensitive LCD film has been used to identify them in the laboratory. For possible application in production the following four methods are currently under evaluation: (1) the infrared thermal imaging method, (2) a 116-contact method of detecting shunts in completed modules, (3) the McMahan method and (4) the optical beam induced current (OBIC) method. The first method appears to have complications because of the high reflectivity of the back electrode. The other three methods will be evaluated in the next subcontract.

5.4 Contactless Measurements of the Open Circuit Voltage

The objective of this project was to develop a technique to measure the open circuit voltage without making permanent or semi permanent contacts, during each step of cell fabrication. Such measurements would provide the necessary feedback to optimize the VTD process. Heretofore at SCI semi-permanent electrodag contacts have been used to the CdTe layer to measure V_{oc} right after the $CdCl_2$ treatment. Making the contacts, measuring the voltage and washing off the

contacts takes more than ten minutes for a single module. Additionally, with this technique measurements could be done only at very few spots.

The V_{oc} probe technique developed at SCI allows for very accurate measurements of V_{oc} in less than a second. The parts to build the V_{oc} probe described here costs less than \$100.

Two different versions of V_{oc} probe have been built so far. One is a portable version, which is powered by a 9V battery, was made mainly to be used with small research samples. This miniature V_{oc} probe is housed in a box measuring about 10 cm x 5 cm x 2.5 cm and weighing about 75 g. The system made for use in production is powered by a 115V AC source and has the sensing probe and the display housed in two separate enclosures which makes reading the display much easier (see Figure 5.1).

This system was used to study the changes in the open circuit voltage during each step of processing, i. e., as deposited, after $CdCl_2$ treatment, after each IFL step and after the heat treatment. The objective of this experiment was to explore the possibility of predicting the final device performance from V_{oc} measurements after $CdCl_2$ treatment. The results of some of the measurements are shown in Table 5.1. As expected, the V_{oc} improves progressively during each process step. There was no change in V_{oc} after the IFL processing although the subsequent heat treatment improved it considerably.

The contactless open circuit voltage measurements opens up the possibility of evaluating the effect of metal contacts on cell stability. Previous experiments have shown that certain metals are more stable than others. When cells degrade the most affected property is the V_{oc} . The degradation could be due to the migration of the contact metal. The new capability of measuring the V_{oc} without contacts, makes it possible to separate these two effects.

Sample	CdS deposition time (seconds)	V_{oc} (mV) as deposited	V_{oc} (mV) $CdCl_2$ treatment	V_{oc} (mV) IFL & heat treat
SD94	22	-	614	824
SD95	17	466	620	817
SD96	13	474	610	782
SD97	10	483	610	780
SD98	8	481	580	528

5.5 Upgrading of the PV Current-Voltage Curve-Tracer System

Upgrading of the large simulator I-V system was done during Phase III. Both software and database structure have been changed. The system now takes dark IV curves, conducts up/down traces and has enhanced analysis. It can measure both modules and small cells. The added capabilities are dark I-V, forward/reverse scans, better display, improved cell tracking, easier

operation, and extraction of dipole parameter (R_s , R_p , A_{diode} and J_0). The light source has also been improved after the detection of hot spots.

5.5.1 Dot Cell Measurements on Large Microscope

The capability to perform I-V measurements of 1 cm^2 dot cells on the full modules on the X-Y table of the large microscope was added. Basically a set of probes, and cables were assembled so that cell I-V measurements can be made using the large simulator computer system but with the module positioned on the large microscope and the cell illuminated with the W-filament back light. This technique has 2 advantages. First, the plate temperature doesn't increase in the time between first cell and last cell measurement. Second, each cell is illuminated with the same light source, unlike the situation with cells measured on the large simulator. Thus we can compare accurately photocurrent among cells and be confident that differences are not due to variations in incoming light intensity.

5.6 Management of Experimental Data

5.6.1 Computer Network

During January the SCI research group established its first local-area computer network. A simple peer-to-peer architecture was chosen and initial mappings created. The first computers to be tied together were the ones containing the deposition parameter database, the film thickness database, and the device performance databases. Future connections will include the database containing other equipment parameters and most members of the research group. Initial versions of custom retrieval software designed to sort information and display trends and histograms were completed. The entire network, database structure, and retrieval software will greatly enhance our statistical analysis capabilities.

During February the network was organized and connected to seven additional computers for a total of 16. The organizational model is that all measurement databases remain local to their machine. Daily the server downloads copies into a central directory for back-up and use by others. When retrieving database information, users move copies to their own machines (retrieval programs will prompt users). Information for general use should be stored on the server in a shared directory. This organization should protect individual computers, be fairly tolerant of mistakes, and should be relatively fast. Most of the above steps will be made virtually invisible to users. This system is expected to be a great boon to data handling and to file backup protection. A training session for SCI personnel is planned at the start of the next Thin Film Project subcontract.

A request was made to assess other network needs of SCI and make recommendations. Inputs for the needs have been gathered and tentative plans formulated for implementation in the next Thin Film Project. At this time the proposed system would move SCI to an all 32-bit architecture, utilizing at least 3 LANs and have e-mail, internet access.

5.6.2 Downstream Database

As an integral part of the information system, a downstream database was set up to record recipe settings for downstream process steps. The downstream database was finally implemented in late April. This system will allow the storage of recipe codes for all downstream processes, greatly enhancing our ability to track and sort experiments in these areas. The codes have been synchronized with the SOP structure currently in operation.

5.6.3 Data Retrieval

During Phase III several data extraction software tools were completed. The tools work with the Microsoft Access data engine and permit flexible sorting and plotting. The plotting program allows multiple device parameters and histograms to be plotted simultaneously, thereby concentrating more information on a single output page. Figures 2.2.1 and 2.2.3 show samples of output.

5.7 Device Marking for Identification

Identification marking of devices fabricated and tested is an important part of project documentation. Several options have been investigated including an engraving to form a permanent bar-code and alpha- numerics and CO₂ laser marking. The bar code quality was inferior, but alpha- numerics are very distinct. Different options are still under consideration.

6.0 STABILITY TESTING OF PV DEVICES

6.1 Outdoor Testing of SCI Modules and Arrays

Life testing of modules and arrays installed outdoors in different parts of the country is continuing with some of the arrays having undergone over 3 years of testing. As already stated in the Phase I final report, information of actual field performance is required for at least two reasons. First, one must verify that the same phenomena are occurring in the indoor stress tests and outdoor operating conditions. For example, one must test that normal daily and seasonal temperature, humidity and illumination cycling do not induce additional degradation mechanisms not simulated in indoor tests. Second, one must use outdoor performance as a reference to determine any acceleration factor of indoor stress conditions.

Following recommendations by NREL, we began compiling field temperature data to understand actual use temperature. For example, Figure 6.1.1 shows an annual temperature histogram from a module that has been under test in New Mexico. The module temperature was measured using a

thermocouple that was embedded during lamination. The module experiences a bi-modal distribution, with nighttime temperatures equal to ambient temperatures and daytime module temperatures about 35°C higher than ambient. The maximum temperature recorded was 70 °C. This result has prompted the selection of 65 °C and 100 °C as appropriate for temperatures for accelerated life testing described in the following section.

SCI has accumulated detailed life-test data of 30 months for four individual modules being monitored at SWTDI at Las Cruces, NM, 32 months for its 1 kW array at NREL, 31 months of outdoor exposure for the 1.2 kW array at its Westwood facility in Toledo (Array 2), and 25 months for a 10 kW Toledo Edison array, also produced by SCI. Stability data for these arrays and one representative module appear in Figures 6.1.2, 6.1.3 and 6.1.4, and 6.1.5, respectively. All arrays and modules continue showing excellent stability.

6.2 Accelerated Life Testing - A Joint Effort with the National CdTe Team

In early 1997 the National CdTe Team agreed to a "Stability Screening Test" protocol. SCI supplied CdTe-coated and chloride-treated substrate to all team members for back contact experiments. Some of the devices made with SCI semiconductor and other contacts were returned to SCI where they were subjected to some of the protocol stress conditions. Other samples were sent to Colorado State University for similar stress tests.

The protocol specifies measurements to consist of light and dark I-V taken at the 2 hour, 2 day and 2 month interval. The purpose of these tests is to evaluate the devices under identical stress conditions, as well as to determine failure mechanisms for those devices which did not survive the above stresses. SCI received samples for the University of South Florida, Institute of Energy Conversion, and Colorado School of Mines and SCI. Only South Florida supplied a substantial group of identical samples.

SCI prepared three sets of samples with different, proprietary, back-contact recipes. The screening tests at SCI on the three sets of samples were begun in July and were completed in September. The stress conditions for the stability screening test are listed in Fig. 6.2.1. These samples were left in test after the end of the screening tests. The data analysis capability was also improved that facilitated getting an initial feel for the data the very day the I-V measurements were complete.

Devices made by other laboratories using SCI semiconductors were received in October placed under the stability screening test in November. Unencapsulated cells from USF, CSM, and IEC were available. An optical alignment grid was built so that cells could be placed reproducibly on the simulator. The handling of cells from multiple sources somewhat tedious. Very small, and variable area cells require extra attention. As some of the laboratories had problems with their contact process to the cells, SCI had to provide them with additional CdS/CdTe films.

6.2.1 Results of the First Round of ALT

SCI presented the results of the first round of Accelerated Life Testing at the National CdTe Team meeting at Florida Solar Energy Center. A compilation of the data included in the Notes from that meeting follows. First we continue to note that ALL outdoor module and array performance is quite stable as shown in the data presented in the preceding section. Thus although some accelerated life test results show degradation after relatively short times, actual data indicate stable modules in field conditions.

Figure 6.2.1 gives a summary of the of the accelerated screening tests. The top row of the table indicates stress conditions and device fabrication recipes. X1, X2 and X3 are all SCI devices. X3 is the recipe used for all modules currently deployed in the field. Devices from the participating laboratories were also tested. However, due to a restricted sample set, these devices were only tested under a few conditions. All devices, including those made at the participating laboratories, were fabricated using semiconductor films deposited and chloride treated at SCI. Moreover, all samples were taken from a single 60-cm x 120-cm plate from SCI, identified as film 20819. Consequently all devices were made from the same starting semiconductors.

Figures A1-A15 convey the essential results of the tests. These figures consist of overlaid J-V curves as well as trend graphs of efficiency, V_{oc} , J_{sc} and R_{oc} . A summary of the results follows.

- All devices in this test were unencapsulated single cells. Four replicate devices for each test condition were used.
- Degradation commonly consists of “rollover” and decrease in V_{oc} .
- In the light, X3 devices are more stable at the maximum power point than at open circuit. However X1 devices show little of this bias dependence. (See Figures A1, A2, A3, A4, A10, A11b, A11c, A12, A12b, A12c)
- In the dark at elevated temperature (65 °C, 100 °C) all devices studied showed an increase in apparent R_{oc} and “rollover” in the 1st quadrant. The rate of change increases with temperature. (Figs. A5, A5b, A5c, A6)
- Reverse bias at 100°C in the dark was the most severe stress, producing large changes in all devices studied within ~50 hours. Open circuit and forward biased devices showed different responses at the same temperature. (Fig. A15)
- The difference in the responses of devices stressed with illumination levels of 30 and 70 mW/cm^2 is minimal. (Figs. A13, A14)
- Overall the X3 contacting scheme produced devices which showed the most temperature and bias dependence. USF and X3 devices exhibited similar responses. (USF devices were stressed only at open circuit in both the light and dark conditions at 65 °C and 100 °C). (Figs. A7, A8, A9, A11)
- The X1 devices exhibited the least dependence on bias and temperature. However, the initial efficiency and V_{oc} of these devices was lower than that of devices made with other contacting schemes (Figs. A1, A2). Further optimization of X1 with respect to efficiency is believed possible.

- The broad scope of stress conditions used in the ALT was useful in inducing responses in the devices under test. However, some devices showed little change, and more temperature levels would be useful. Thus a different mix of stress conditions may be appropriate in future tests.

6.2.2 Improved Detection of the ‘Roll-Over’ in the I-V Curves

A new way of looking at J-V curves has been implemented that involves following the trace of the inflection point in the J-V curve. This inflection point is characteristic of the extent of roll-over in the curve usually attributed to the back contact. The inflection point in the J-V curve is a minimum in the dV/dJ vs. V curve. The derivative curve shows the effect more clearly as seen in Figures 6.2.2 and 6.2.3 by the progression of the derivative minimum for different stress conditions for devices made with the standard recipe. A commonality is noted except for devices stressed in forward bias. Indications of partial device recovery have been noted in the past, primarily recovery induced by forward bias in devices degraded with hot-reverse bias. Other indications of recovery exist. The stability team is pursuing the recovery process as a possible means to understanding the degradation mechanisms. Specifically, the task is to explore whether devices degraded in light soak recover similarly to those degraded in hot reverse bias.

6.2.3 Attempted Recovery of Degradation by Forward Voltage Bias

In the past SCI has demonstrated that by the application of forward bias it was possible to recover the performance of CdTe cells degraded by a few days of hot reverse bias [6]. These cells had been made by CSS. In an effort to test whether cells degraded in the ALT project by hot, open-circuit light soak could also be recovered, forward biasing of the devices at room temperature was performed. Four current regulators were built such that forward bias is a 5 mA/cm^2 current bias. The initial results suggest that forward bias at room temperature causes significant further degradation in cells already degraded with hot open-circuit light soak. Cells previously stressed at hot light soak resistive load degraded slightly more with room temperature forward bias. Room temperature forward bias has partially recovered some of the degradation caused by a week of hot reverse bias, but the recovery was not as complete as in the past when hot forward bias was used. Consequently, application of forward bias at elevated temperatures was attempted, however only a minor recovery occurred. Clearly, the degradation is not simple and many further experiments will be needed. The preceding table summarizes the results.

6.2.4 Future Stability Work

As a result of the ALT screening test, SCI has re-evaluated its philosophy towards stress testing. In the future, we intend to perform more measurements on fewer devices and try to uncover mechanisms. The broad screening test is very useful in identifying important degradation conditions and the significant number of replicate samples ensures statistically valid conclusions. However, we now feel that more progress will be made with physical measurements such as SIMS and more in-depth electrical measurements such as IVT.

SUMMARY

In Phase III Solar Cells Inc. has focused on four major areas toward the development of the manufacturing process that will lead to high volume and low-cost manufacture of solar cells. They included (1) refinement of the newly developed, continuous-feed, deposition process for the semiconductor layers and its transfer to PV module production; (2) improvements in cell and module efficiency through materials and process control; (3) verification of device stability by indoor and outdoor monitoring of PV cells, modules and arrays and by setting up Accelerated Life Testing (ALT) procedure in conjunction with the NREL-sponsored National CdTe Team program; (4) cell interconnects, including further development of SCI's proprietary Dot Matrix process and alternative means of cell patterning.

Significant accomplishments have been realized in all four areas. Major achievements have been made in the development of the production prototype VTD system for continuous coating of glass plates with CdS/CdTe semiconductor layers. They included accurate means of metering of source powders, reliable transport of heated glass in vacuum, required uniformity of film thickness and record-breaking film deposition onto substrates moving at speeds up to 9 linear ft./min. (2.7 m/min.). A new SCI record efficiency of 14.1% has been achieved for small cells by the combination of the use of low-iron glass, intrinsic tin oxide over the TCO, thinning of the CdS layer, and various improvements in the film deposition, back contacts and device processing. For the 60 cm x 120 cm modules produced by the new, rapid VTD process, the top aperture-area efficiency achieved thus far is 8.4 %, compared with the SCI record of 9.1 % for the established CSS process. A successful test of the VTD system has been conducted under an environment of PV module production, in a continuous run lasting 18 hours, during which 140 plates were coated. At present the difference between the coating speed and the coated module production is due to the substrate handling capability by the vacuum load locks and glass heating capacity. The thickness of the glass substrate for modules has been reduced from 5 mm to 3 mm, thereby achieving higher optical transmission, faster heating and lower cost. The ALT program has been established, with the participation of four laboratories. Extensive data on accelerated degradation effects under electrical bias and elevated temperature have been collected and presented. All SCI-made CdTe devices in the field, including modules and arrays, some in their third year of outdoor exposure, continue showing excellent stability. The proprietary Dot Matrix process has been developed to the point of achieving efficiency of 7.4% for the modules and 8.0% for 1/4 modules. In a search of a new 'line-patterning' method, other than laser scribing, good quality patterning of TCO has been achieved. Extensive development has taken place in instrumentation and means of automated or accelerated testing of device performance, data collection and data processing to keep up with the rapid throughput of the VTD process.

REFERENCES

1. K. Zweibel and R. Mitchell, "CuInSe₂ and CdTe: Scale-Up for Manufacturing," SERI/TR-211-3571, UC Category: 273 DE89009503, NREL, Golden, CO (1989).
2. R.A. Sasala, R.C. Powell, G.L. Dorer, "Technology Support for Initiation of High Throughput Processing of Thin-Film CdTe PV Modules," NREL Subcontract ZAF-5-14142-05 (1997), Solar Cells Inc., Subcontractor, Phase II Technical Report, (1997).
3. Y. Tyan and E.A. Peres-Albuerne, Proc. 16th IEEE PVSC, pp. 794-800 (1982).
4. X. Zhou, "Fabrication of Stable Large-Area Thin-Film CdTe Photovoltaic Modules," NREL Subcontract AR-1-11059-1, Solar Cells Inc., Subcontractor, Final Technical Report (1995).
5. X. Wu, P. Sheldon, T.J. Coutts, D.H. Rose, and H.R. Moutinho, "Application of Cd₂SnO₄ Transparent Conducting Oxides in CdS/CdTe Thin-Film Devices," Conference Record of the 26th IEEE Photovoltaic Specialists Conference, pp. 347-350 (1997).
6. X. Zhou, R.A. Sasala, and R.C. Powell, "Fabrication of Stable Large-Area Thin-Film CdTe Photovoltaic Modules," in American Institute of Physics Conference Proceedings 353, 13th NREL Photovoltaics Program Review, H.S. Ullal and C.E. Witt, editors, Lakewood, CO, 1995, pp. 31-38.

ACKNOWLEDGMENTS

This work has been supported in part by NREL subcontract ZAF-514142-05.

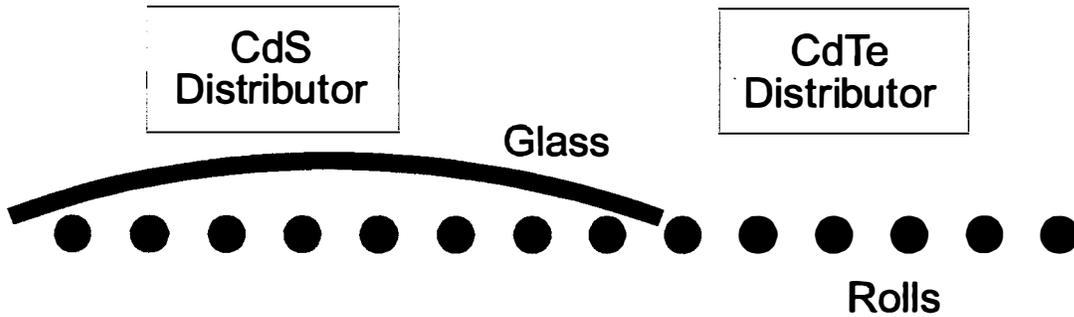


Figure 1.1 Schematic of thermal warp due to top heating. Note the potential glass transport problem due to loss of contact with the rolls in the center and the collision of the glass leading edge with next roll.

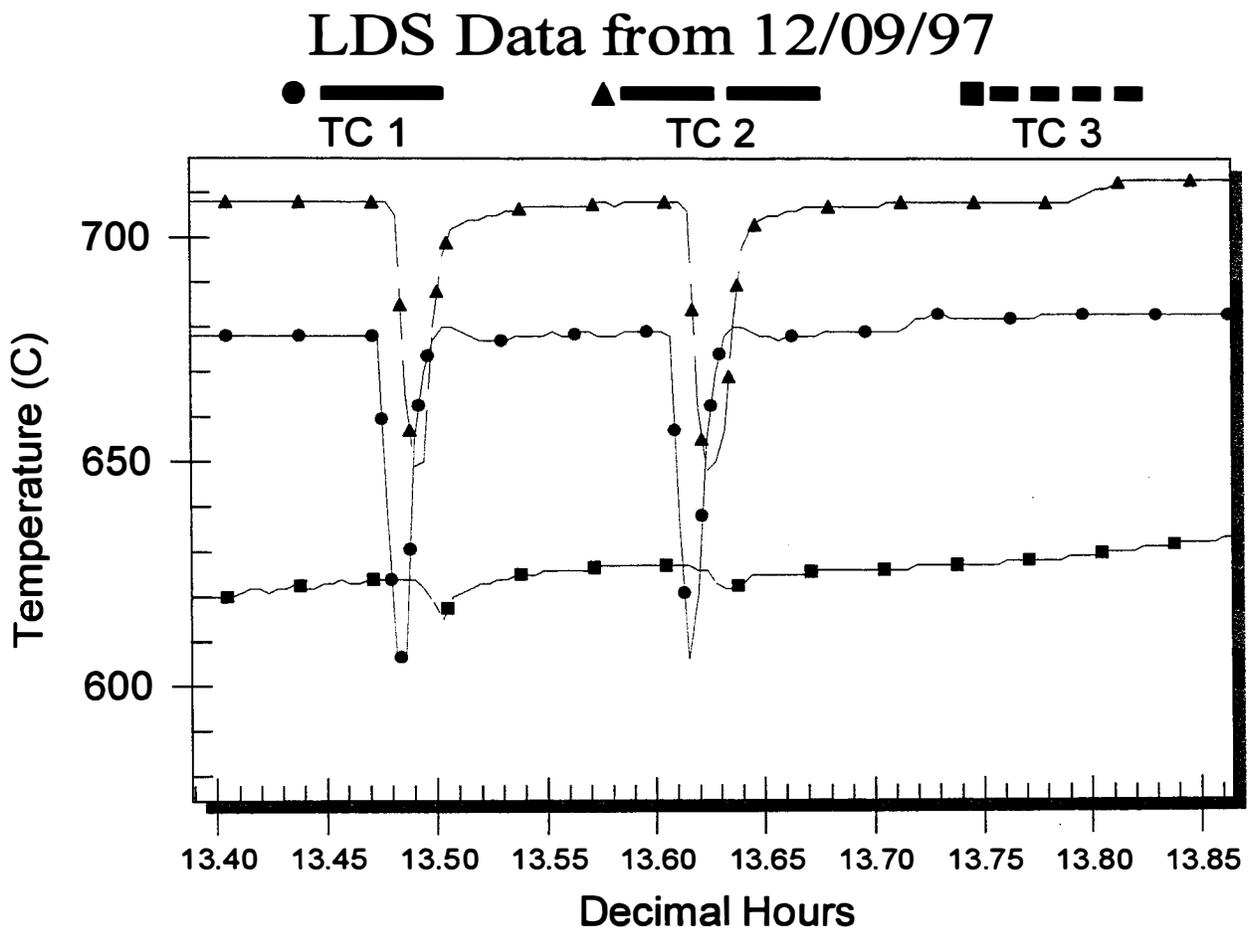
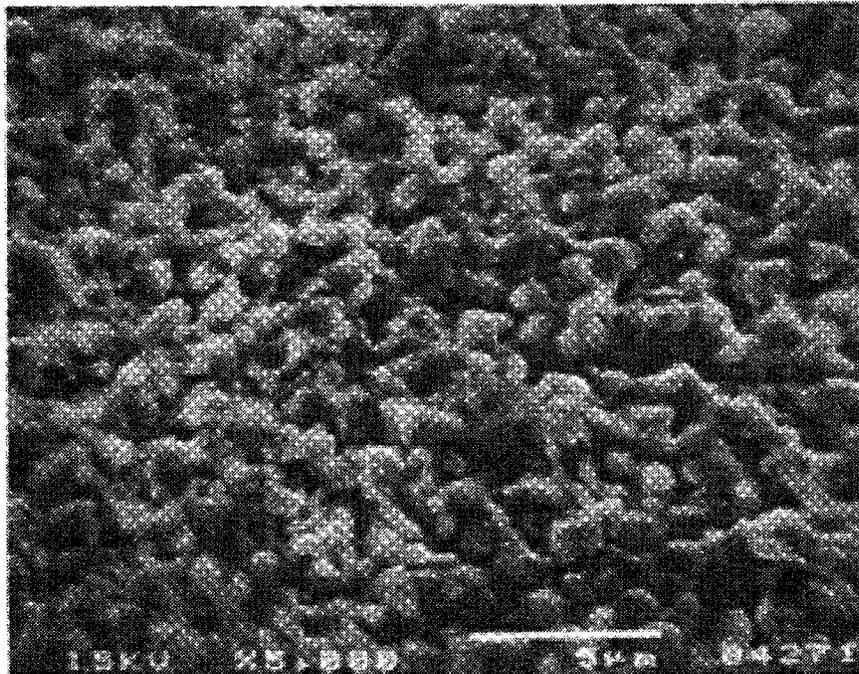


Figure 1.2 Temperature measured by thermocouples located below the glass substrates. Shown is the passage of 2 substrates through the VTD system. The minima indicate the approximate glass temperature. Numbers 1 and 2 represent positions near the CdS distributor before and after the CdS deposition, and #3 indicates position before exiting the system.

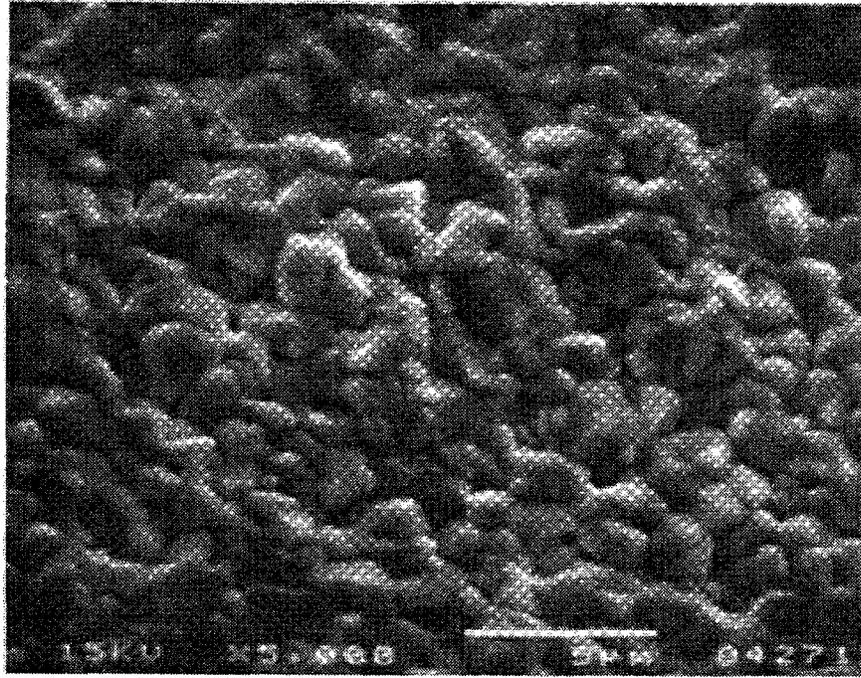


(a)

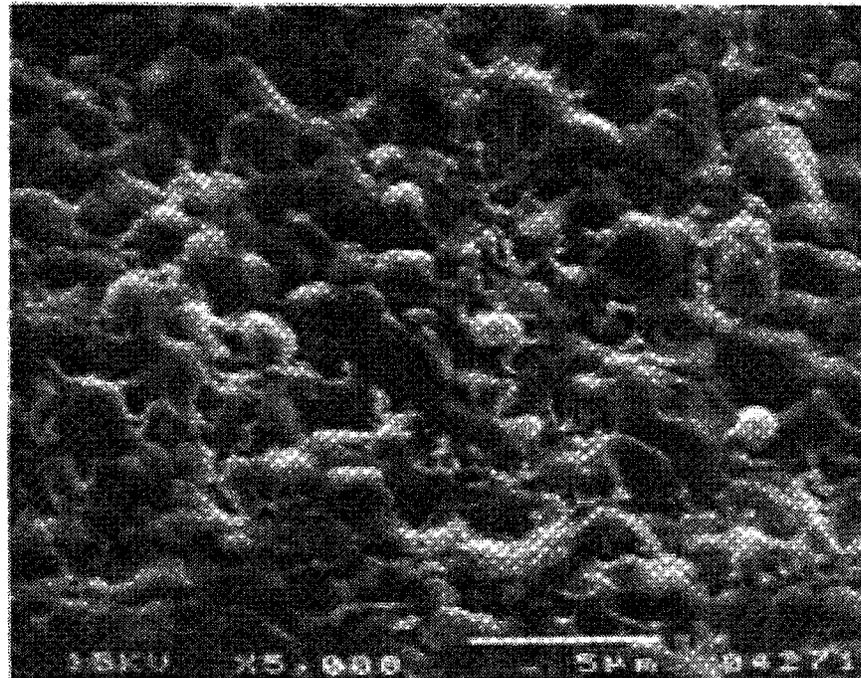


(b)

Figure 1.3 Photomicrographs of the surfaces CdTe film coated in the VTD system (a) as-deposited sample, (b) CdCl_2 heat-treated sample

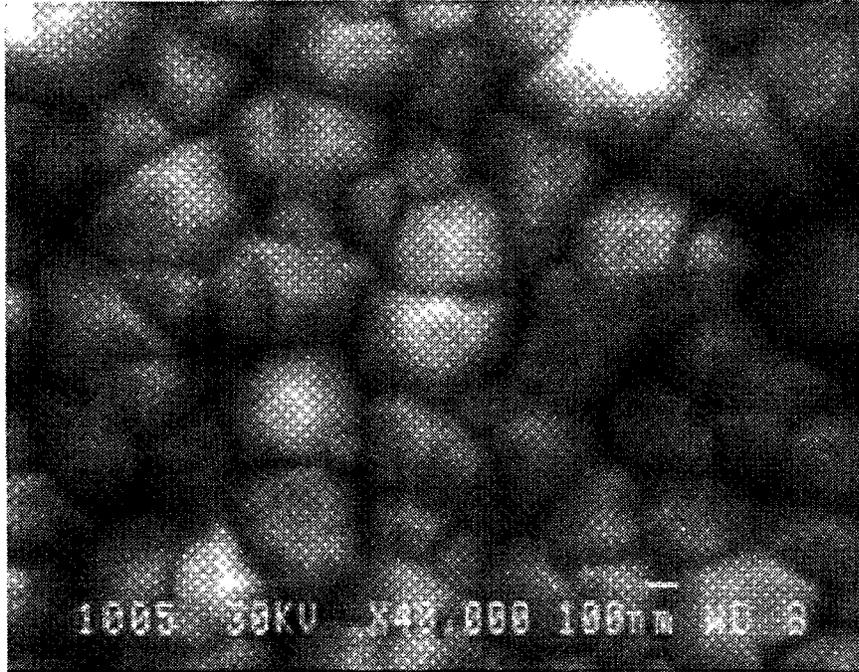


(a)

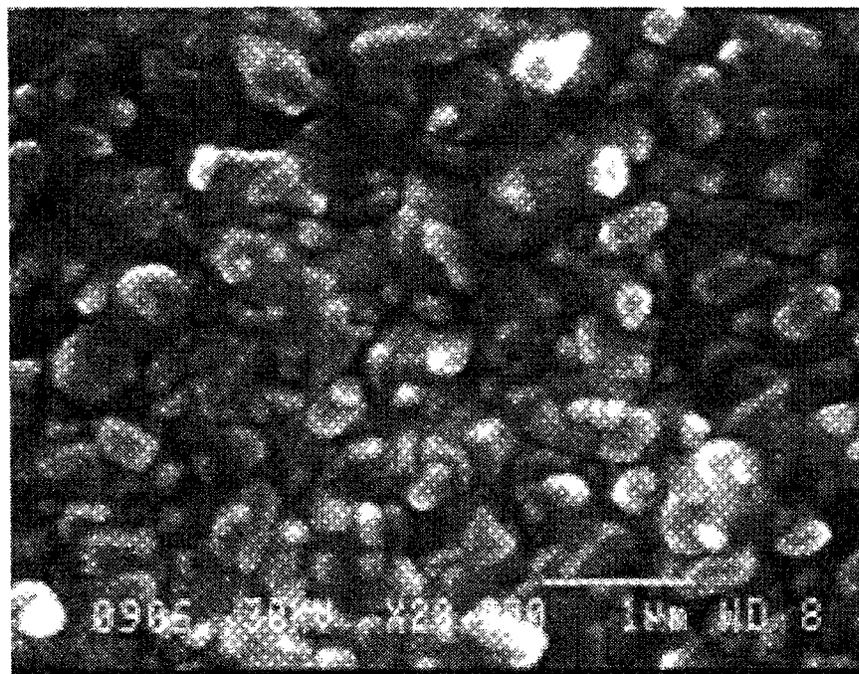


(b)

Figure 1.4 Photomicrographs of the surfaces CdTe film coated in the RMS system by CSS
(a) as-deposited sample, (b) CdCl_2 heat-treated sample



(a)



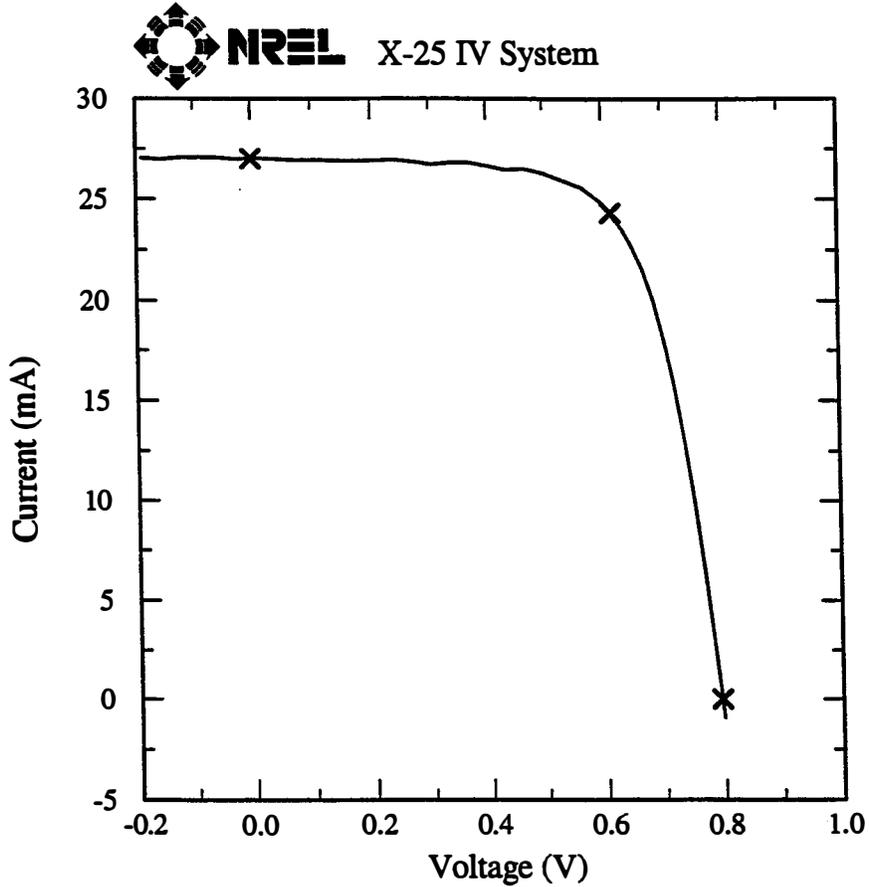
(b)

Figure 1.5 Photomicrographs of the surfaces CdTe film coated by magnetron sputtering (a) as-deposited sample, (b) CdCl₂ heat-treated sample (Note the differences in magnification between a and b and Figs. 1.4 and 1.5)

Solar Cells Inc. CdS/CdTe

Sample: SD84-31
Mar 30, 1998 2:26 PM
ASTM E 892-87 Global

Temperature = 25.0°C
Area = 1.058 cm²
Irradiance: 1000.0 Wm⁻²



$$V_{oc} = 0.7948 \text{ V}$$

$$I_{sc} = 27.01 \text{ mA}$$

$$J_{sc} = 25.52 \text{ mAcm}^{-2}$$

$$\text{Fill Factor} = 69.63 \%$$

$$V_{max} = 0.6146 \text{ V}$$

$$I_{max} = 24.32 \text{ mA}$$

$$P_{max} = 14.95 \text{ mW}$$

$$\text{Efficiency} = 14.1 \%$$

After 10 minute soak at P_{max} , 2 minute cool.

Figure 2.1.1 Current-voltage NREL data for a new SCI record CdTe cell having a conversion efficiency of 14.1 %

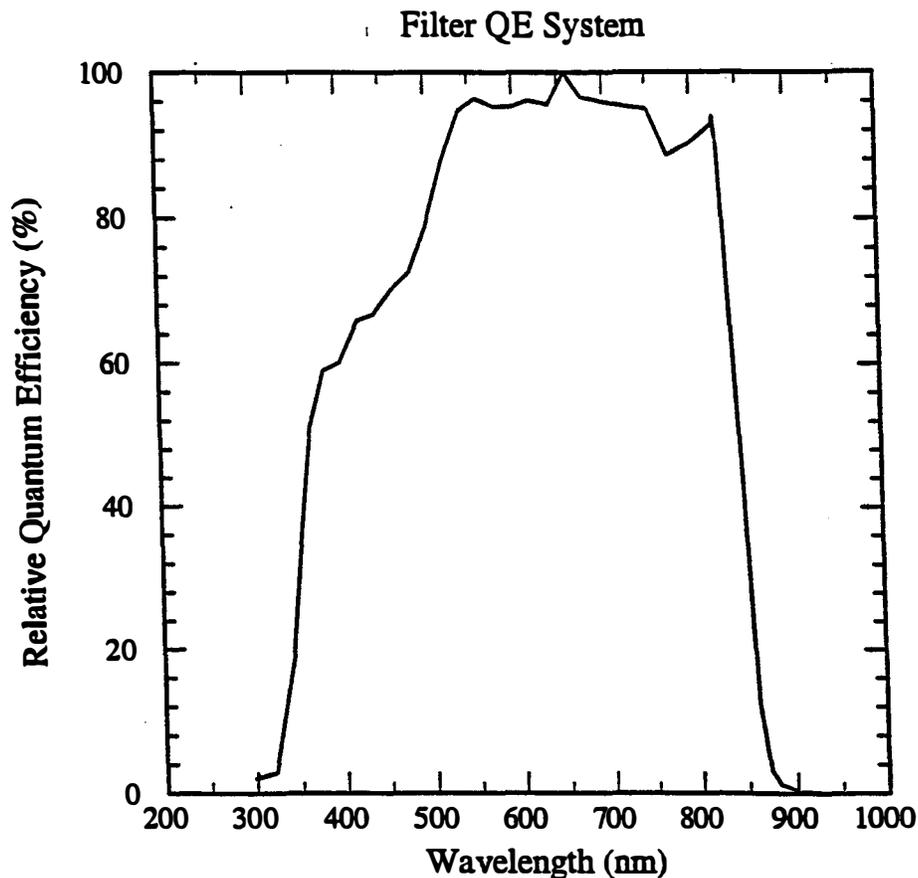
Solar Cells Inc. CdS/CdTe

Sample: SD84-42

Temperature = 25.0°C

Mar 23, 1998 7:46 AM

Device Area = 1.053 cm²



Light bias = 30.0 mA

Bias Voltage = 0.00 V

$J_{sc} = 26.33 \text{ mA/cm}^2$ for ASTM E 892 Global (1000 W/m²) Spectrum

Figure 2.1.2 Quantum efficiency of a CdTe cell similar to one having conversion efficiency of 14.1 %

Database: c:\AAAData\datahub.mdb
 Table/Query: Cell

Data from SERIALTIME between 11/01/1997 and 03/05/1998
 WHERE:
 ORDER BY: SUB_ID

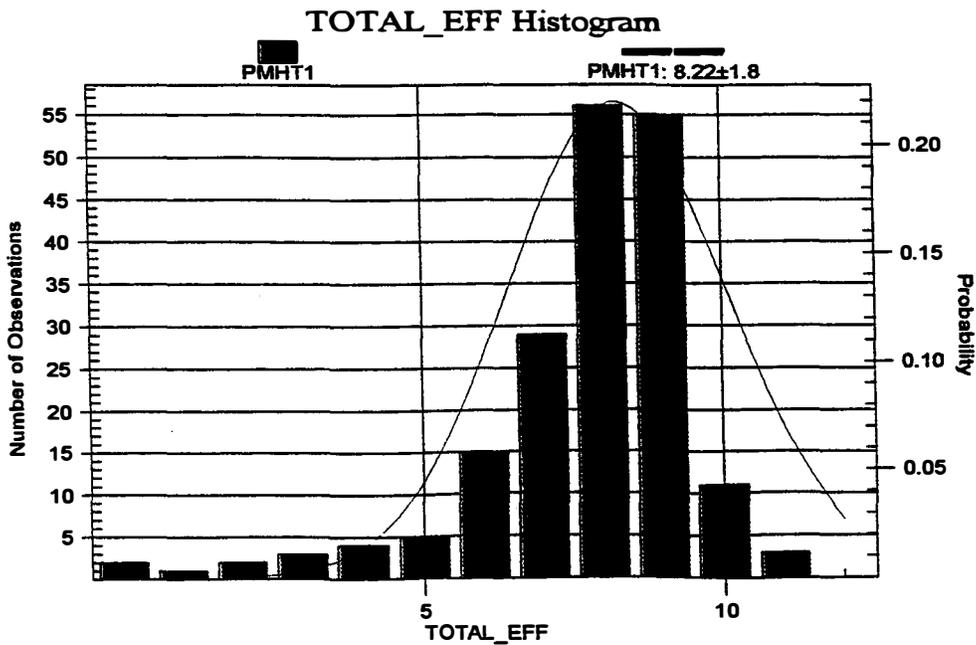
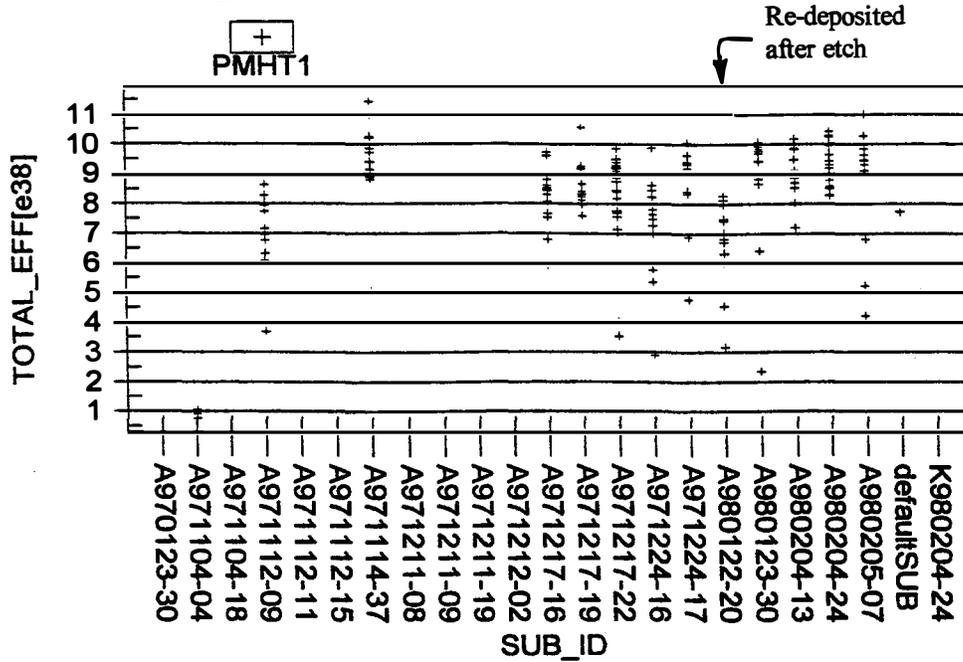


Figure 2.2.1 Results of the conversion efficiency of dot cells made by VTD over a 4 month period, through the end of February 1998

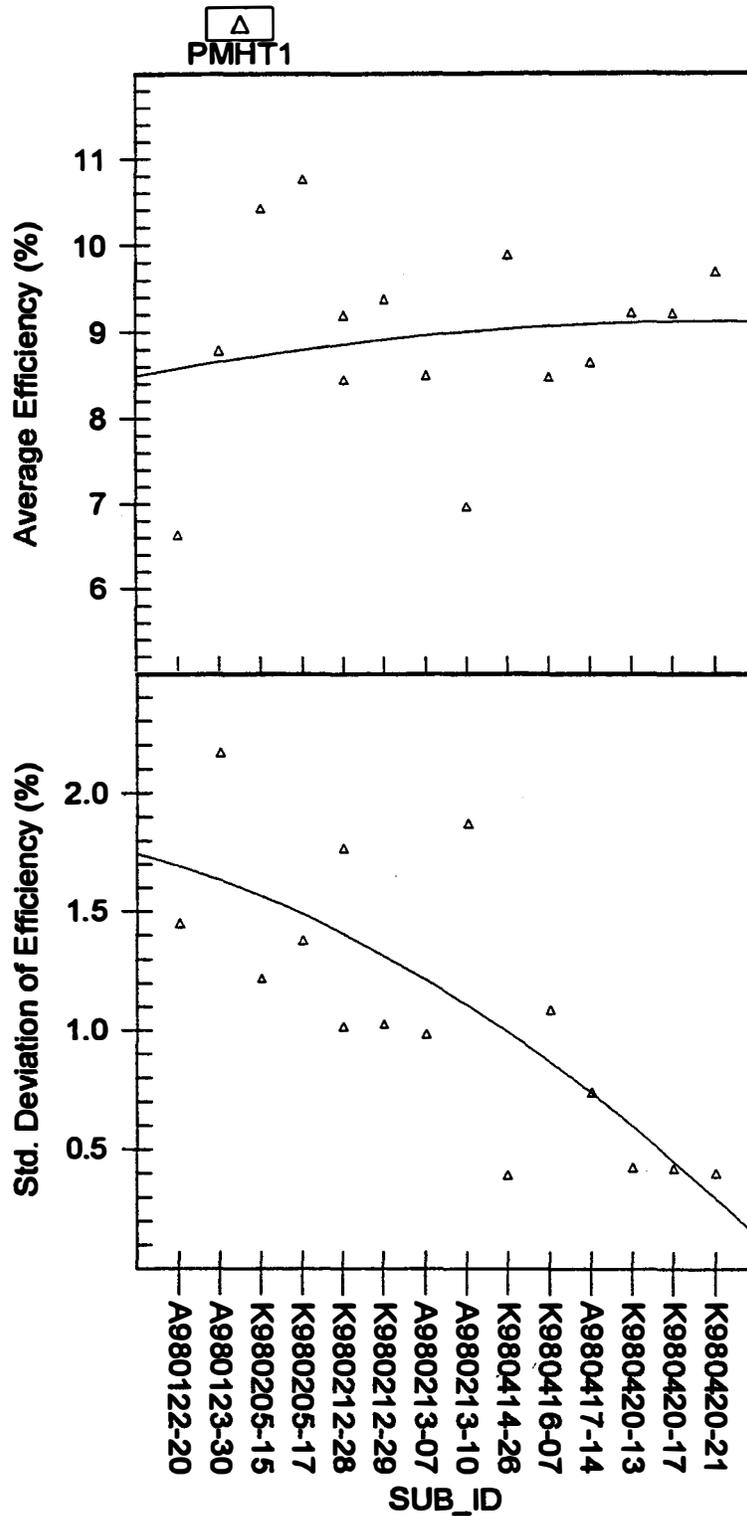


Figure 2.2.2 **Top** - Progress in the average conversion efficiency of dot cells made by VTD over a 3 month period, through the end of February 1998
Bottom - Progress in the standard deviation of the average efficiency with time (each point in both graphs represents data for 13 cells)

Database: c:\AAAData\datahub.mdb
Table/Query: Module65V

Data from SERIALTIMEbetween7/01/1995 and 03/05/1998
WHERE:
ORDER BY: SUB_ID

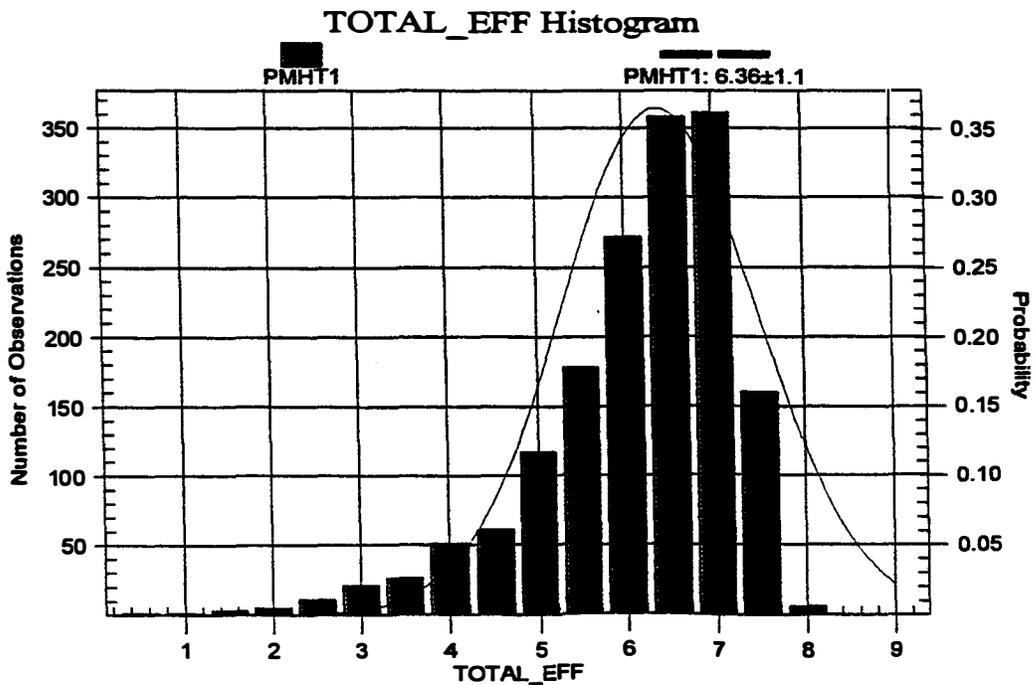
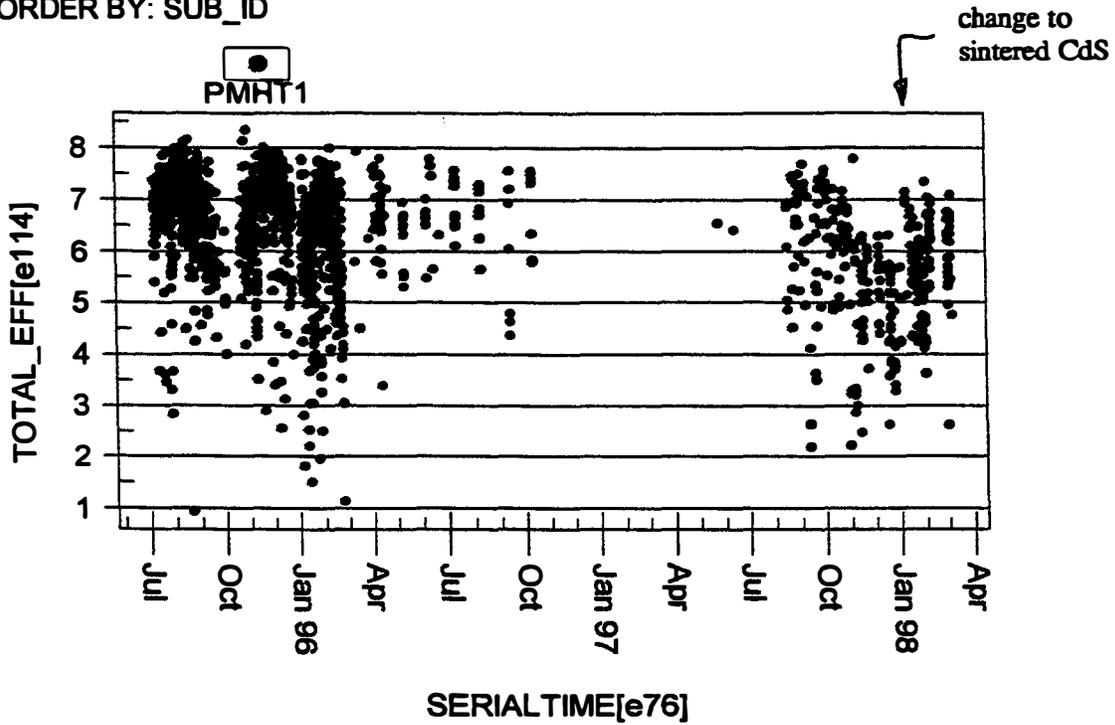


Figure 2.2.3 Results of the conversion efficiency of modules made by CSS and VTD over a 11 month period, through the end of February 1998. (Modules produced subsequent to August 1997 were made by VTD)

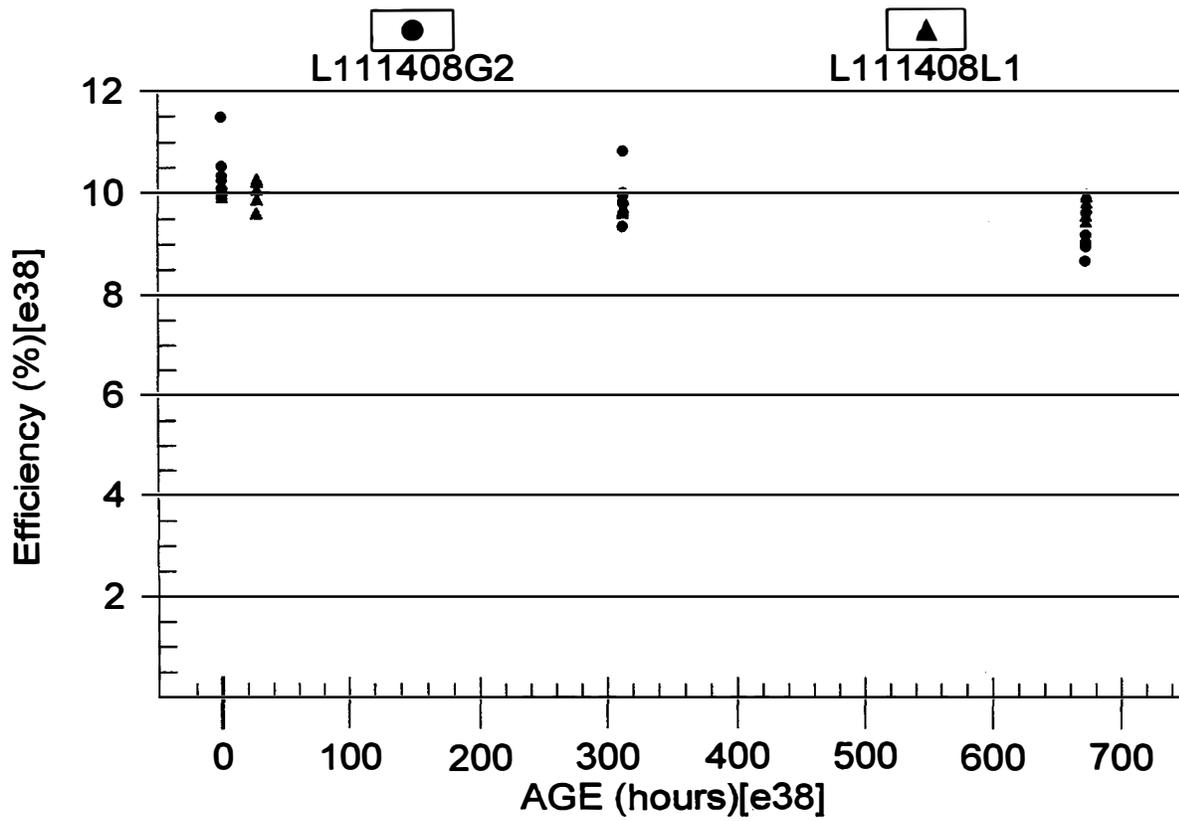
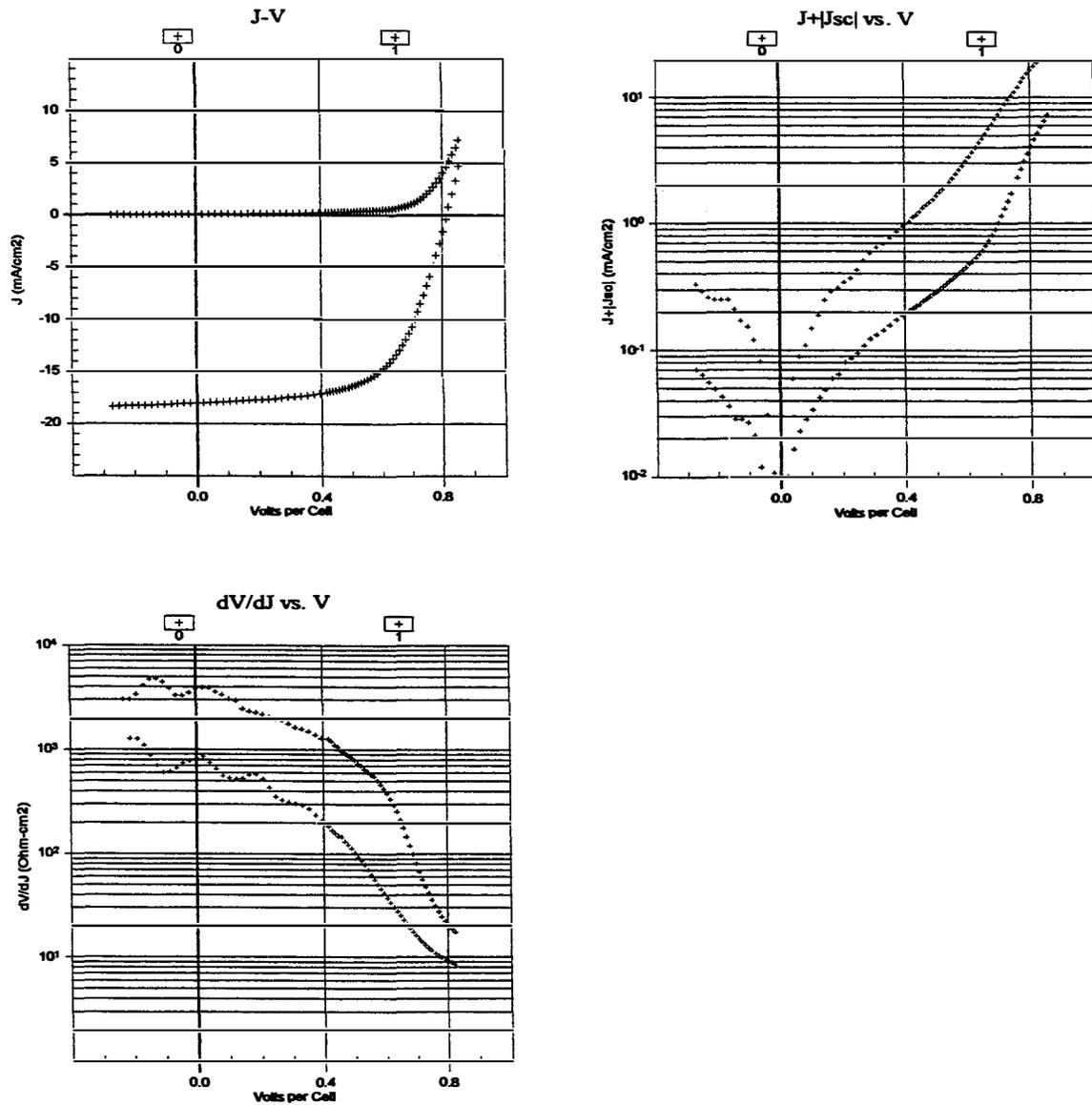


Figure 2.4. Performance of cells made on 3-mm thick substrate using VTD. Cells were light-soaked for one month at 65°C under open-circuit conditions.



Index	Sample	ProcessCode	File	Ap. Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	K980513-10	PMHT1	21\K980521E.688	8.4	-18.0	816	0.60	7.3e+2	8.5	-3.2e-4
1	K980513-10	PMHT1	C:\VTEST\VBRAWDATA\IE980521\K980521E.688							

Figure 2.5 Performance data for one of the best 60 cm x 120 cm modules made to date on the high-throughput VTD system (aperture efficiency 8.4 %)

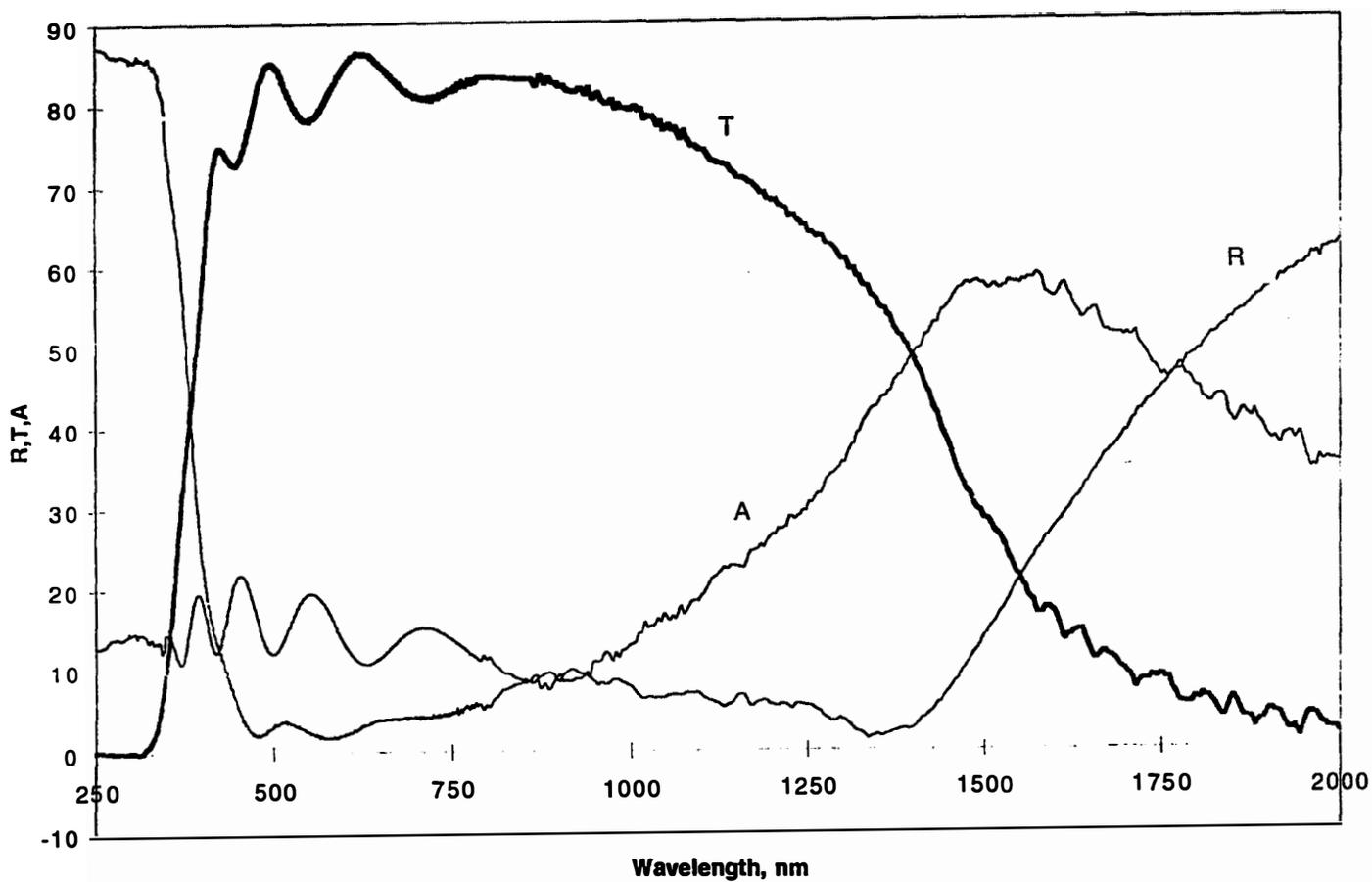


Figure 3.1 Optical transmission and absorbance of SCI sputtered cadmium stannate

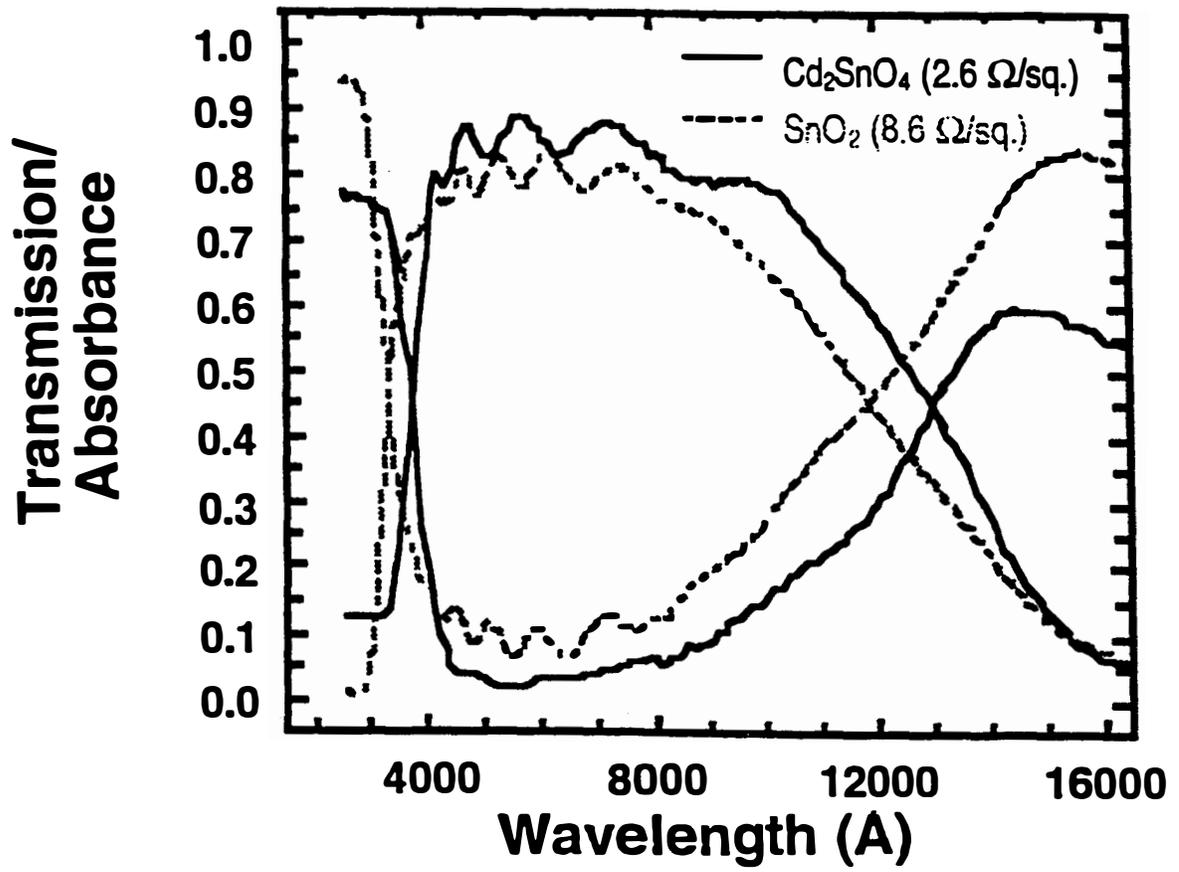


Figure 3.2 Optical transmission and absorbance of NREL cadmium stannate and F-doped tin oxide (from Wu, et al. (1997))

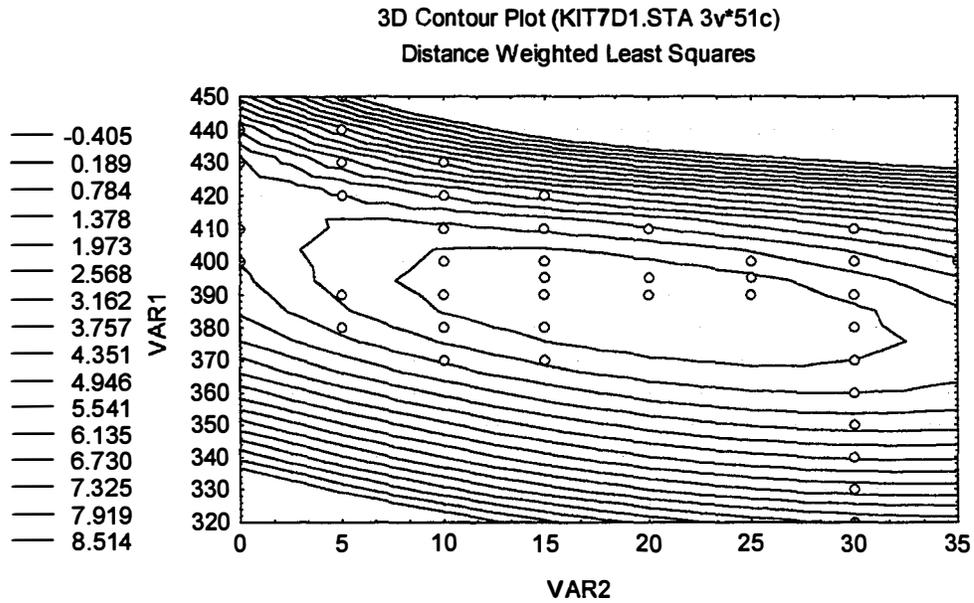
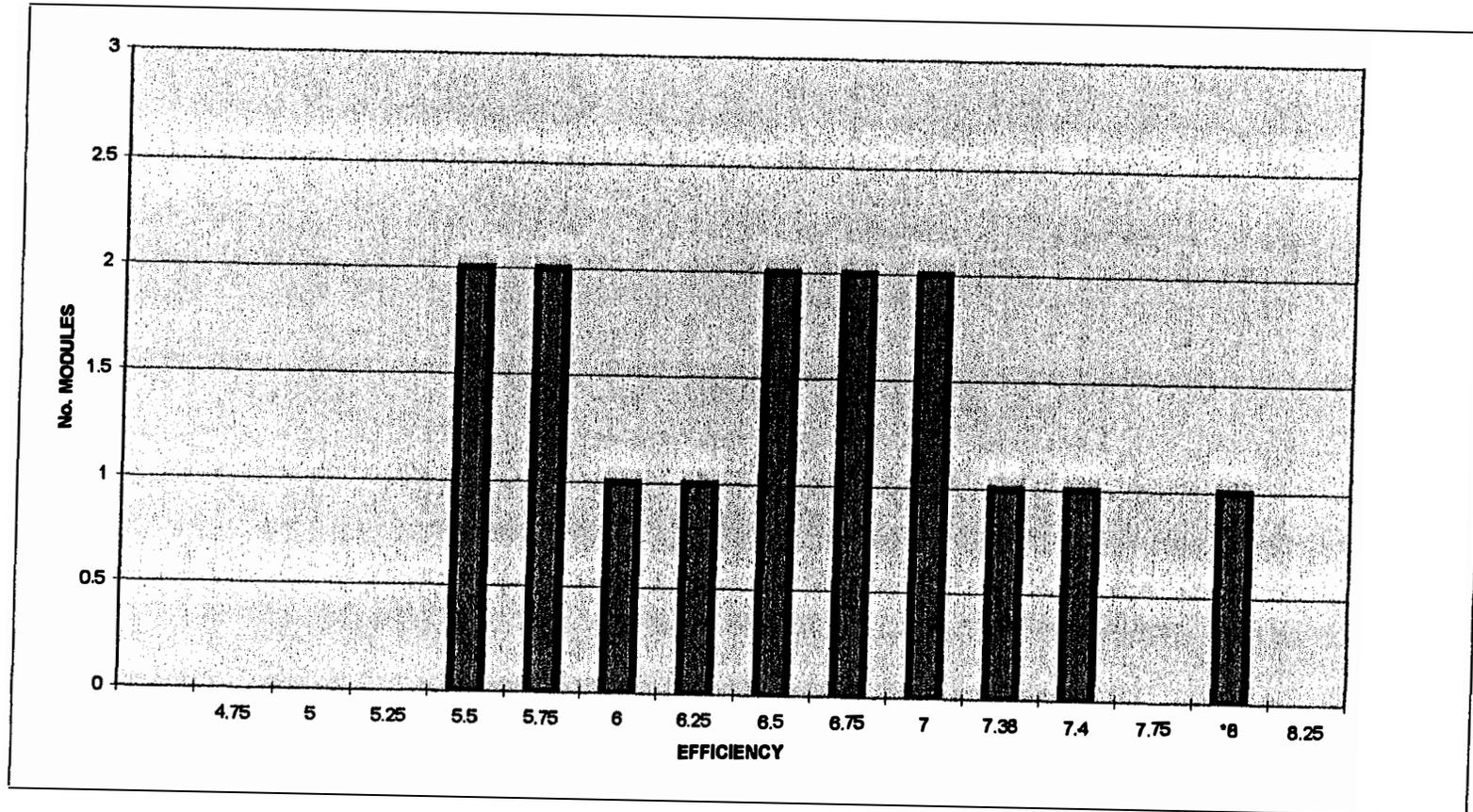


Figure 3.3 A contour plot of the efficiency of CdTe cells, as a function of oven temperature (VAR 1, °C), used in the CdCl₂ heat treatment, and time (VAR 2, min.), after a 7-day light soak. The values of the efficiency are the highest at the center, decreasing outward.



* 1/4 MODULE (11 CELLS)

Figure 4.1 A histogram of the efficiency of 14 Dot-Matrix modules made by the Option 1 process (avg. efficiency of 14 modules = 6.43%)

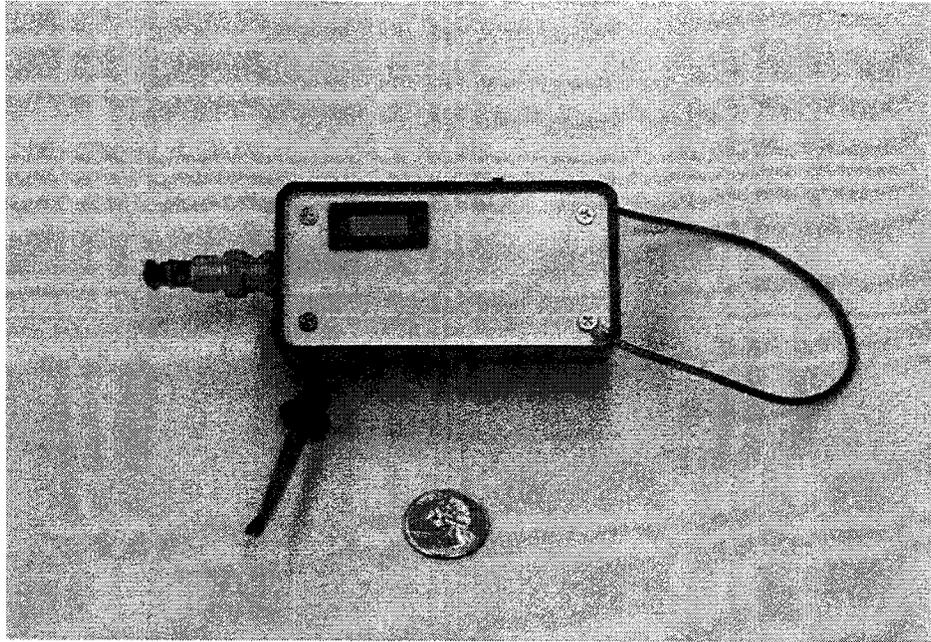


Figure 5.1 a Portable probe for contactless measurement of V_{oc}

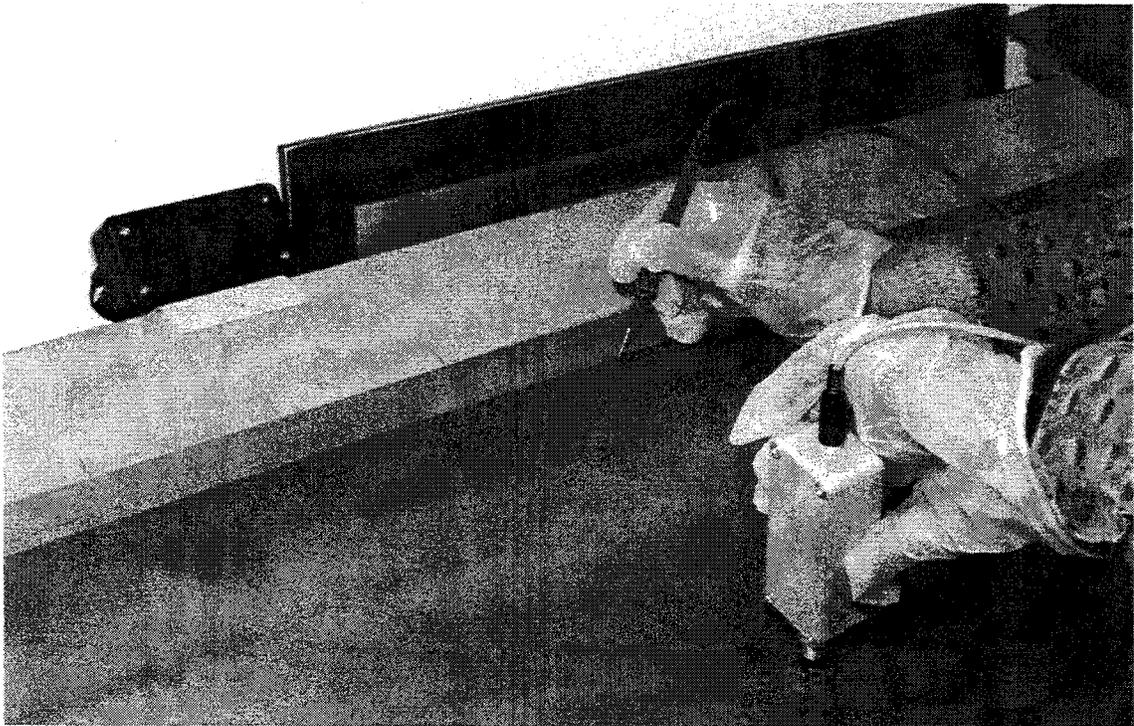


Figure 5.1 b Portable probe for measuring V_{oc} in use in PV module production

**Ambient and Module Temperature Distribution
Module B14409 at SWTDI, 54.1995 to 54.1996**

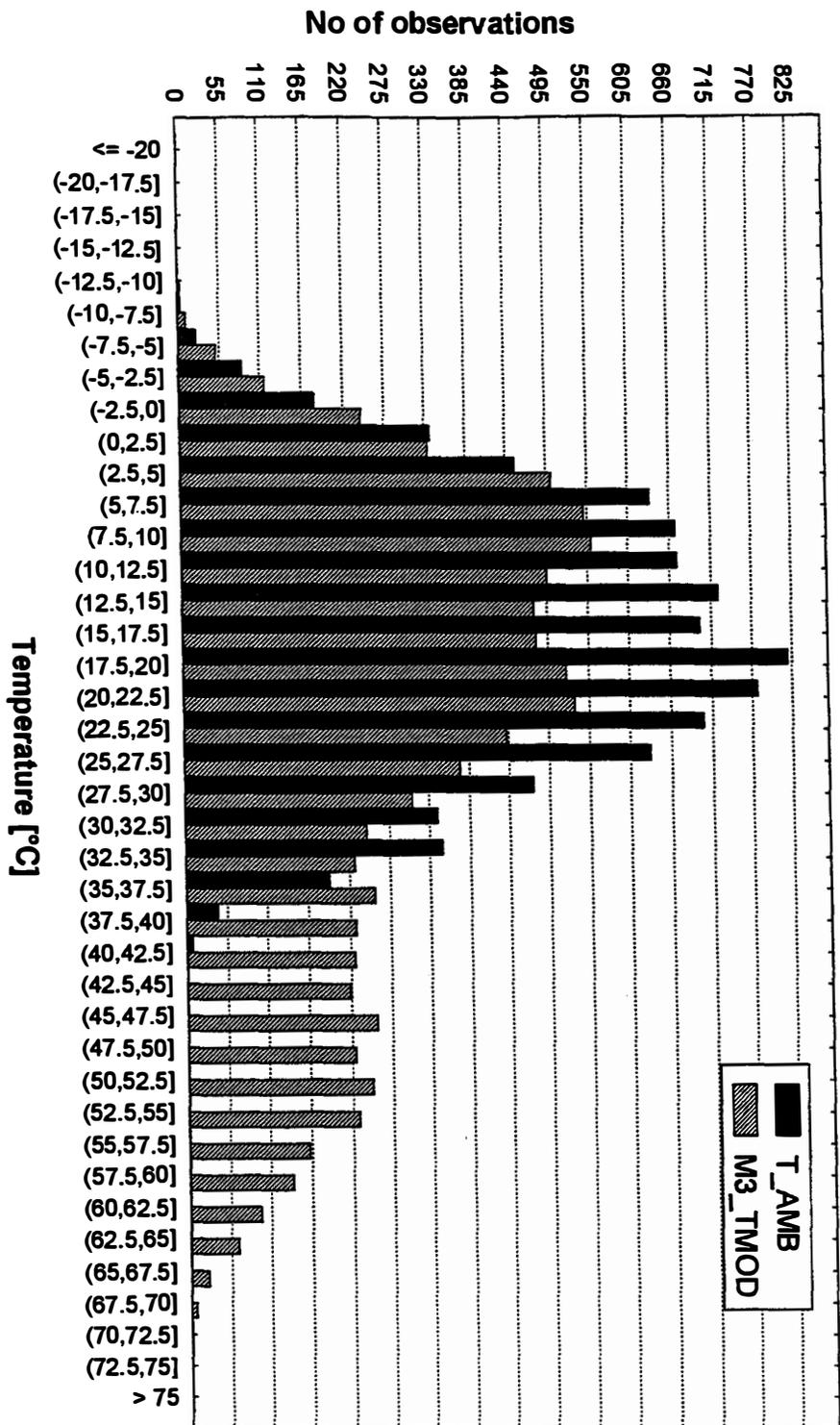


Figure 6.1.1 A histogram of the temperature for SCI CdTe module on an outdoor test at SWTDI, New Mexico

**Module B14412
under test at SWTDI**

Data are normalized to 1000 W/m² irradiance
Data are not corrected for temperature

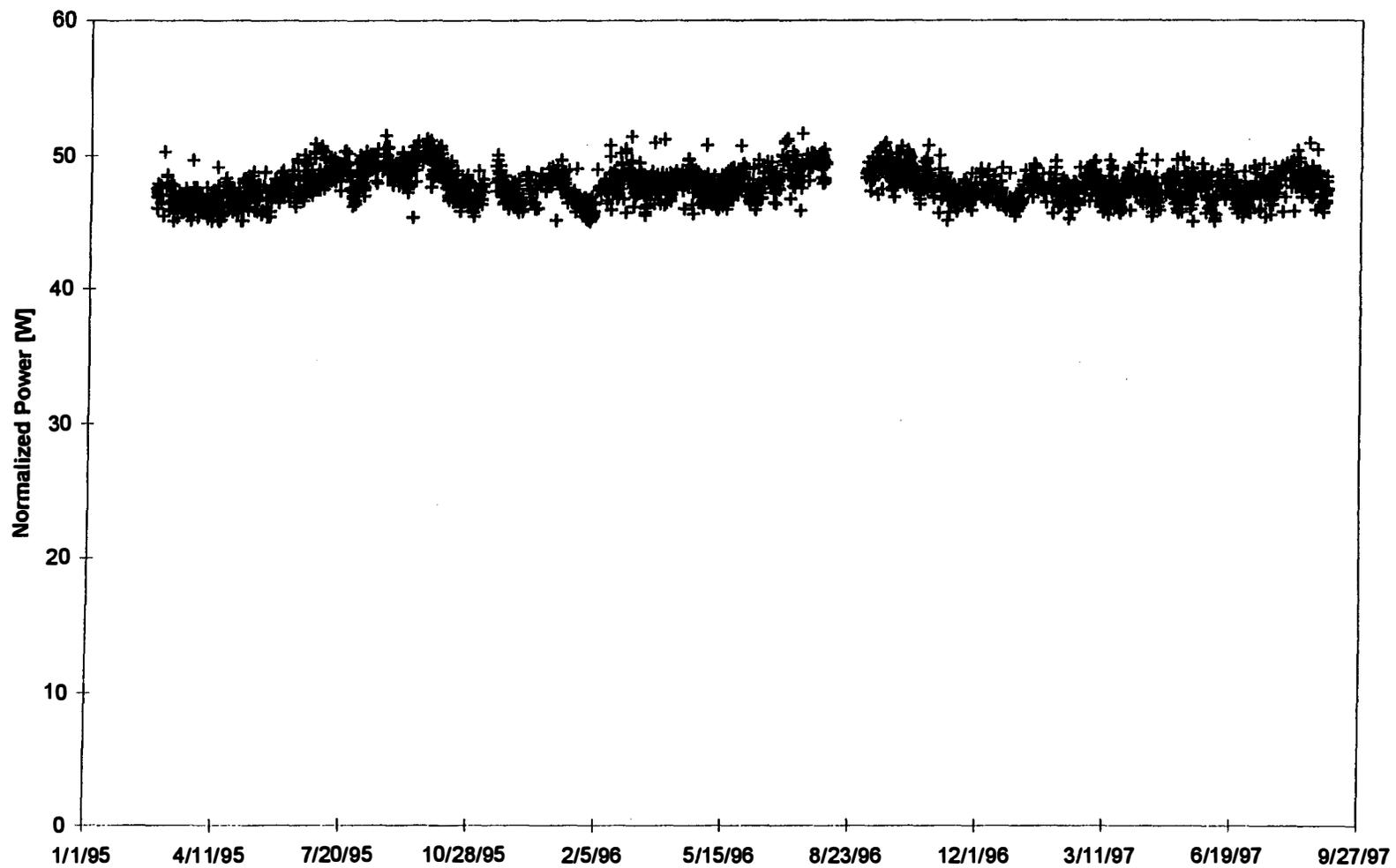


Figure 6.1.2 Outdoor stability data for SCI module at SWTDI, New Mexico

Solar Cell Inc. 1 kW Array Performance Installed at NREL, Golden CO. June, 1995

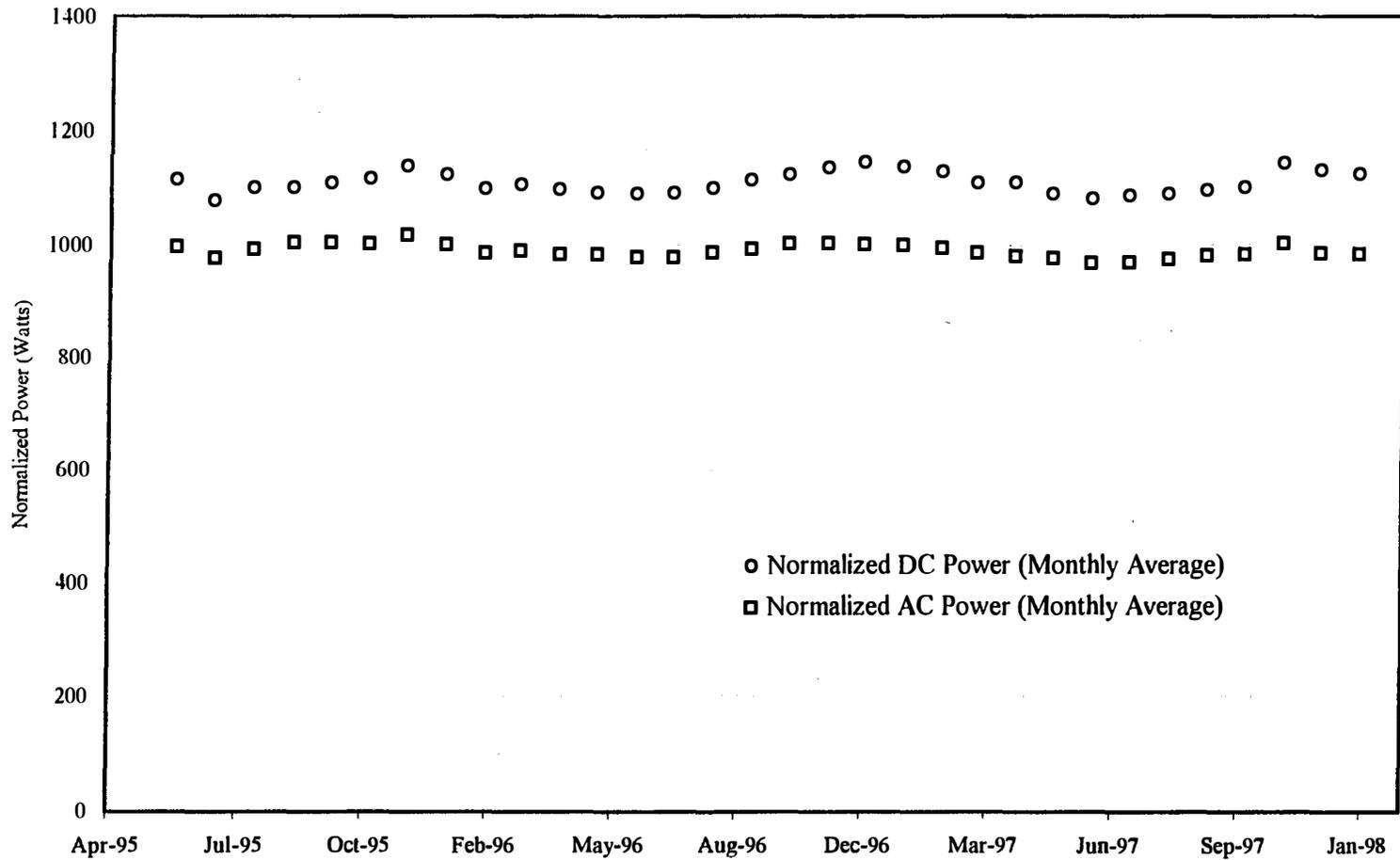
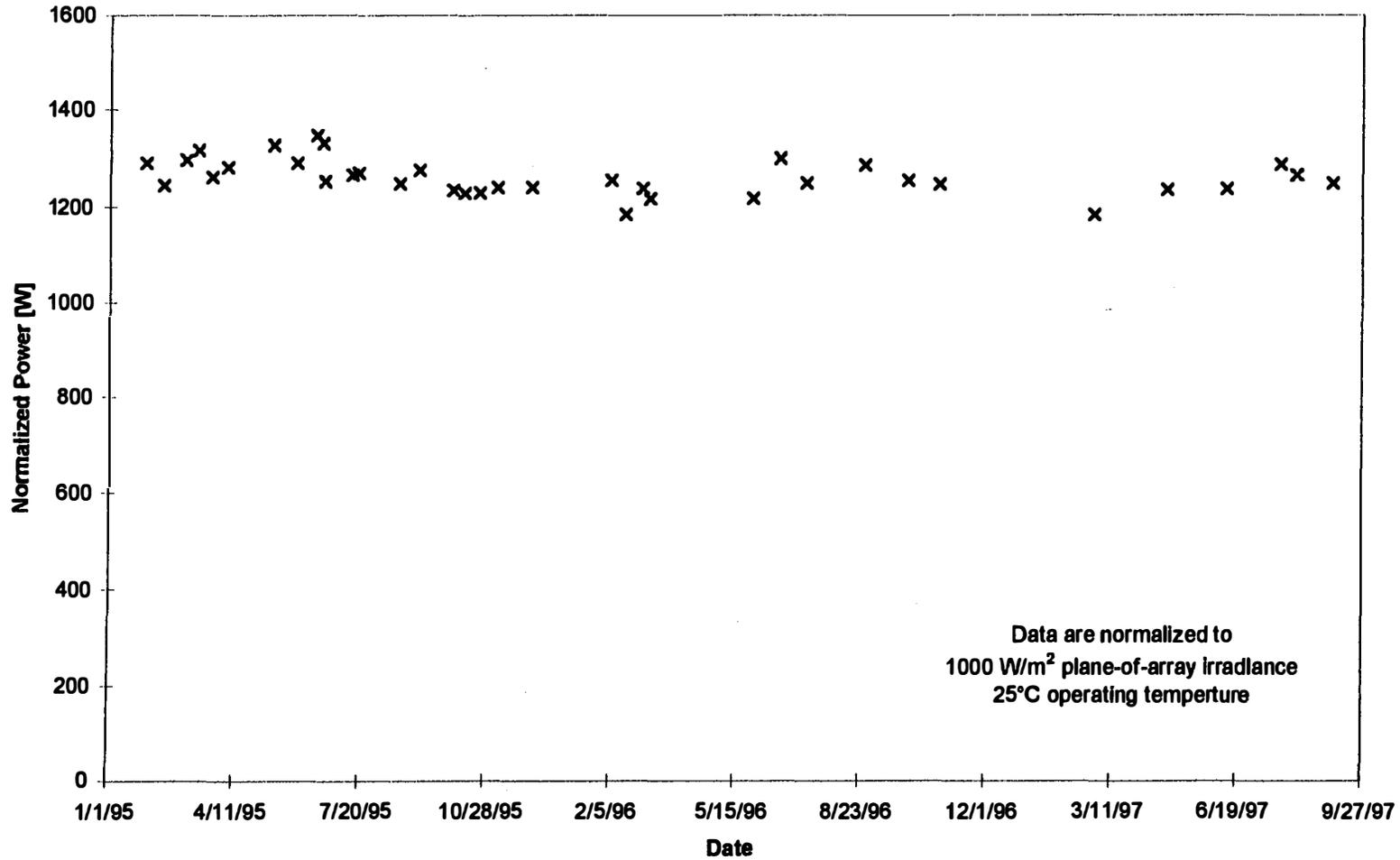


Figure 6.1.3 Outdoor stability data for the 1.0 kW SCI array at NREL

SCI Westwood 1.2kW Array Performance 24 Grid-connected CdTe Modules



51

Figure 6.1.4 Outdoor stability data for the 1.2 kW SCI Westwood array (Array #2)

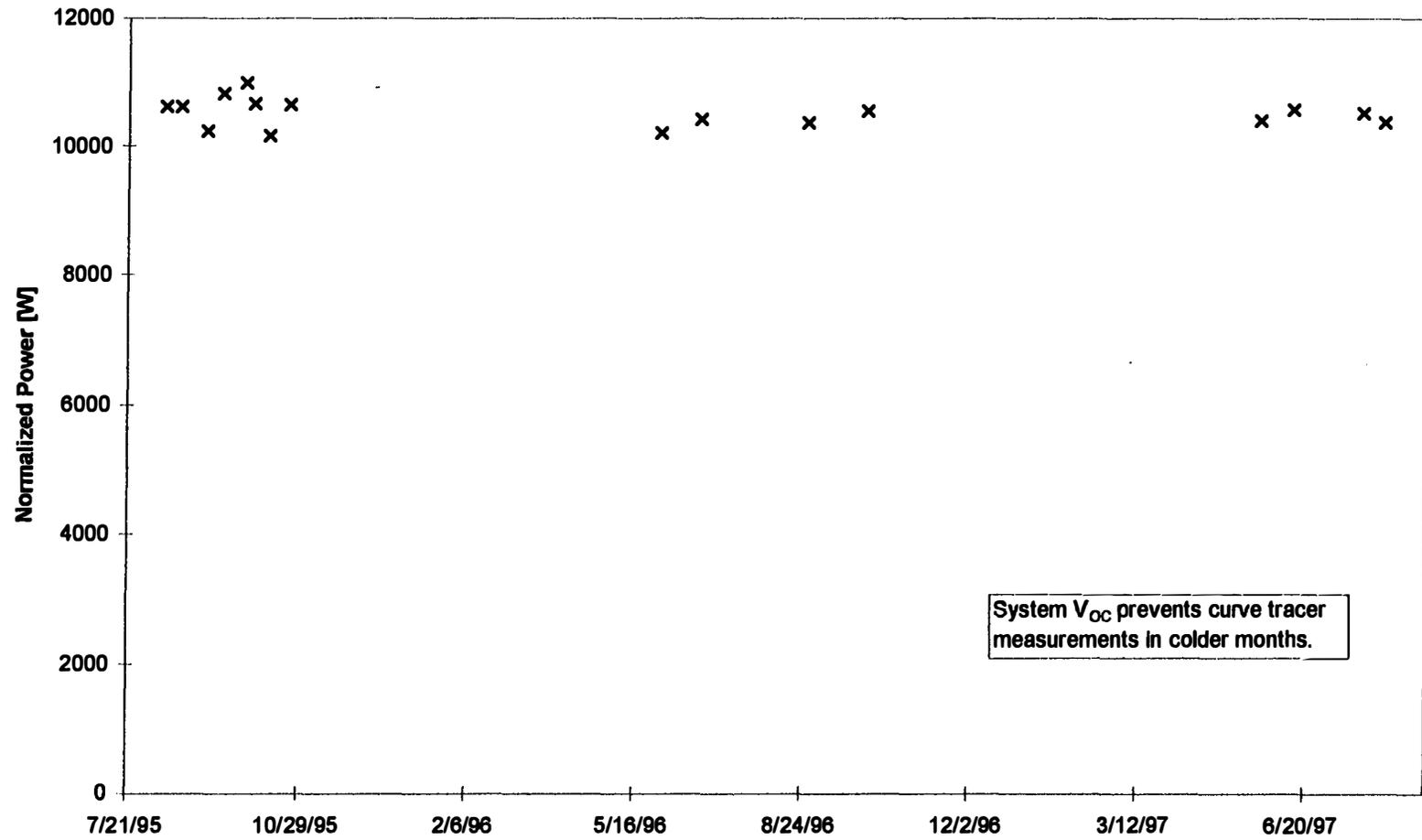


Figure 6.1.5 Outdoor stability data for the 10 kW Toledo Edison Co. array (produced by SCI)

Stress Condition/Contact Scheme Matrix

illumination	BIAS	T	X1	X2	X3	USF1	GSM1	IEC1	IEC2
30 mW/cm ²	LOAD	65							
		100							
	OC	65							
		100							
70 mW/cm ²	LOAD	65							
		100							
	OC	65							
		100							
DARK	OC	25							
		65							
		100							
	FWD 5 mA/cm ²	65							
		100							
	REV -3V/cell	100							

Figure 6.2.1 A summary of the Accelerated Life Testing (ALT)

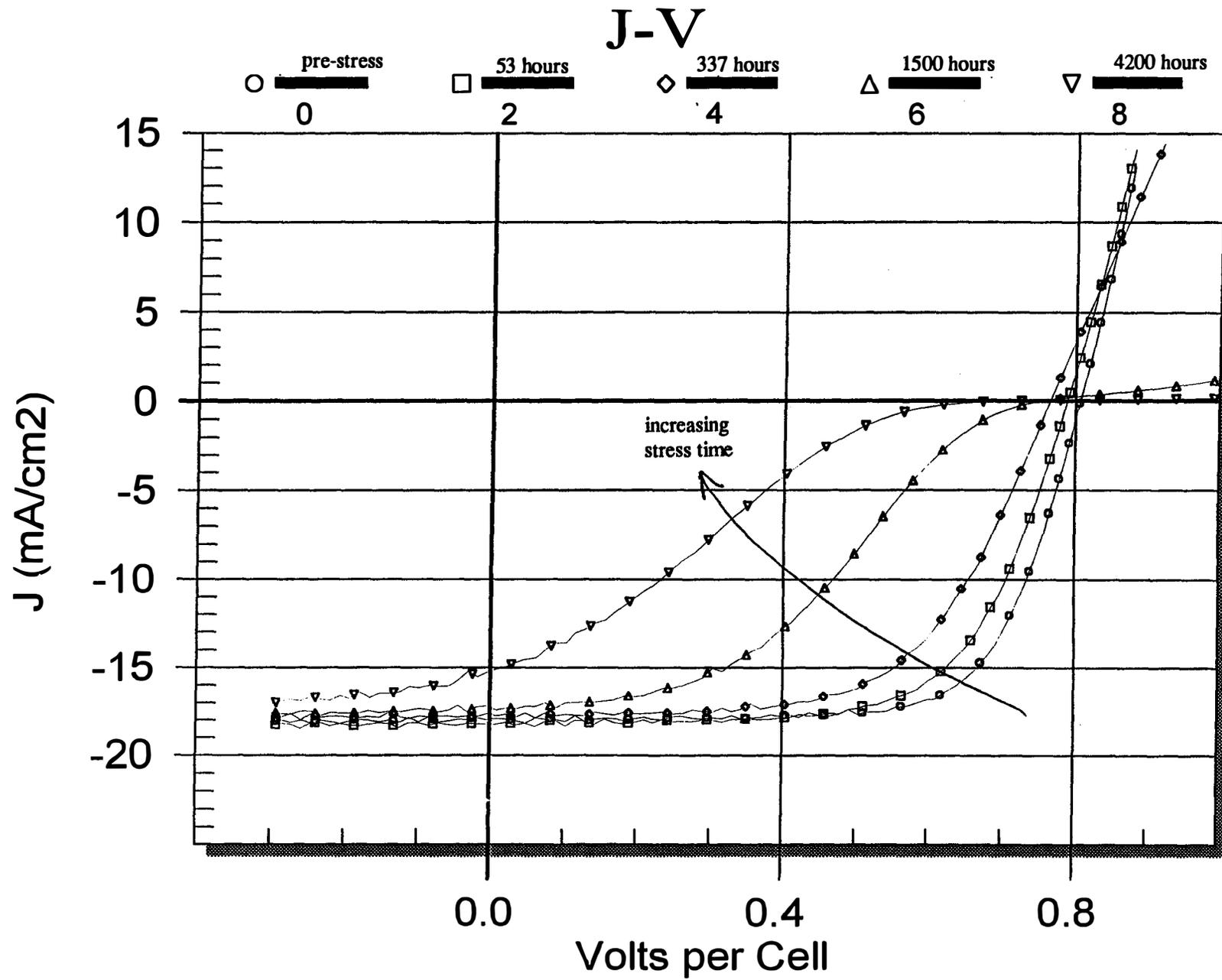
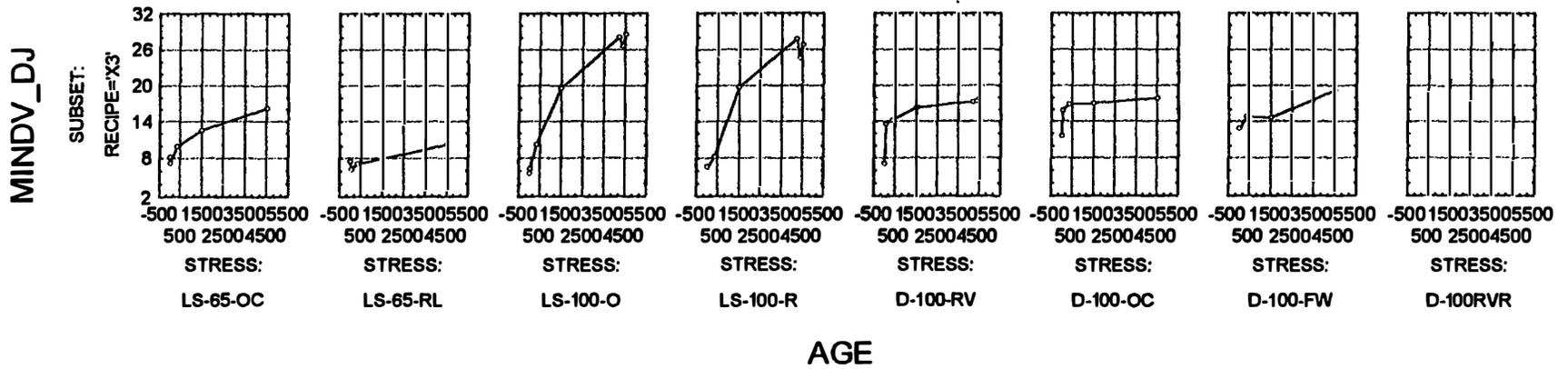


Figure 6.2.2 Progression of the inflection point in the JV curve as a function of stress time

Scatterplot (DVDJ.STA 7v*51c)



Scatterplot (DVDJ.STA 7v*51c)

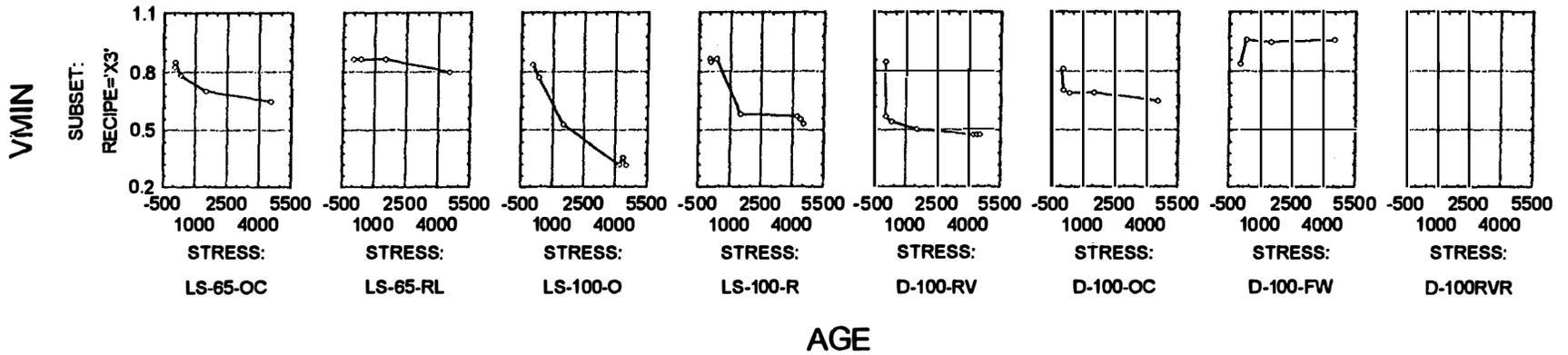
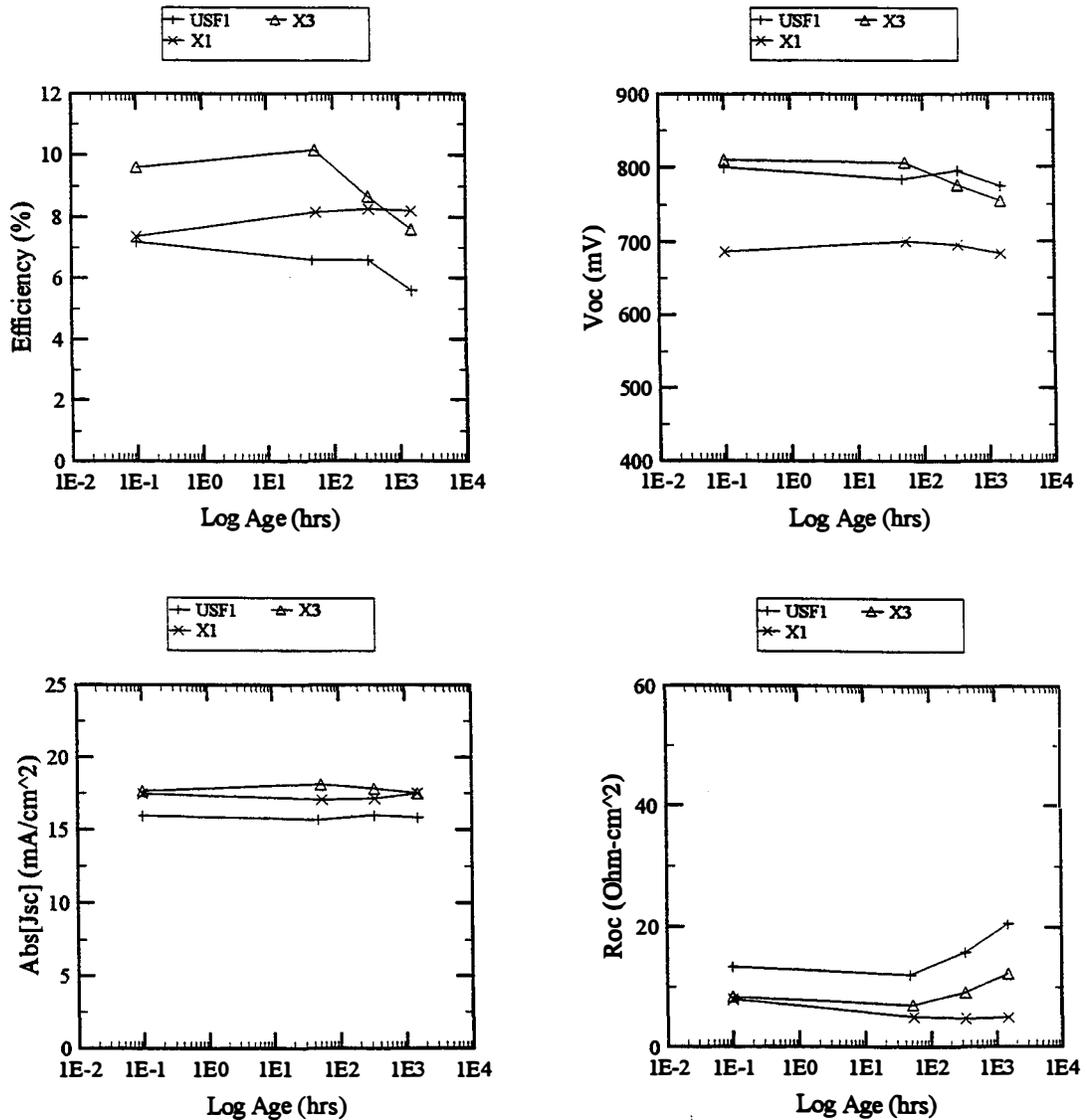


Figure 6.2.3 Progression of the derivative minimum for different stress conditions for devices made with the standard recipe

Bias=OC Illum=70 Recipe=USF1,X1,... Stress_T=65 Grouped by Recipe

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



NOTES:

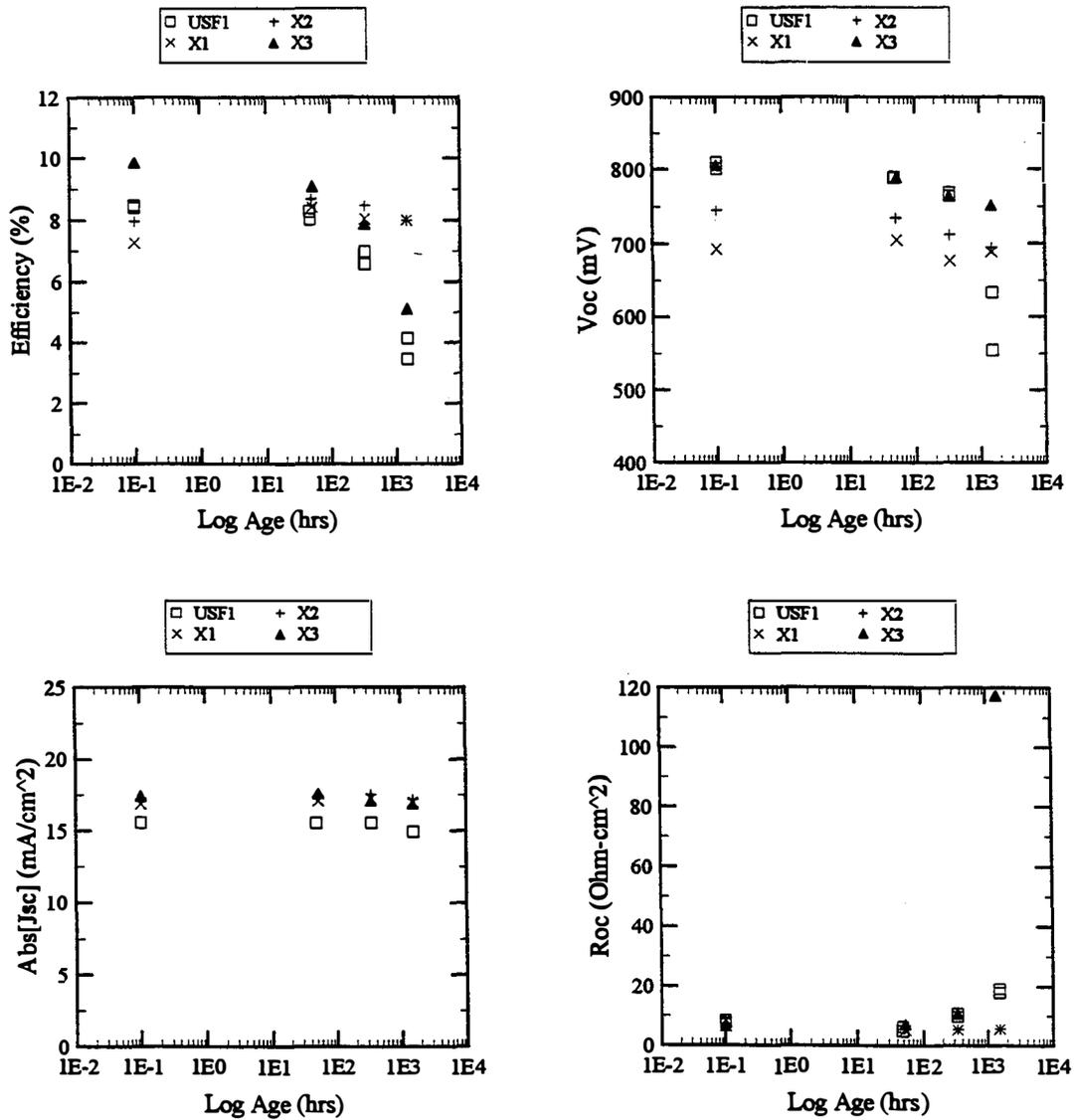
GROUPING METHOD: Group by Recipe

Figure A1

Comparison of two contacts from SCI and one from USF stressed with 70 mw/cm^2 illumination, $T=65^\circ\text{C}$, and a bias of V_{OC} . Similar behavior of the SCI X3 and USF contact samples is evident, especially regarding the increase in R_{oc} . While all three contact samples show an initial decrease in this parameter, only the X1 samples show a stabilized R_{oc} .

Bias=OC Illum=70 Recipe=USF1,X1,... Stress_T=100 Grouped by Recipe

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



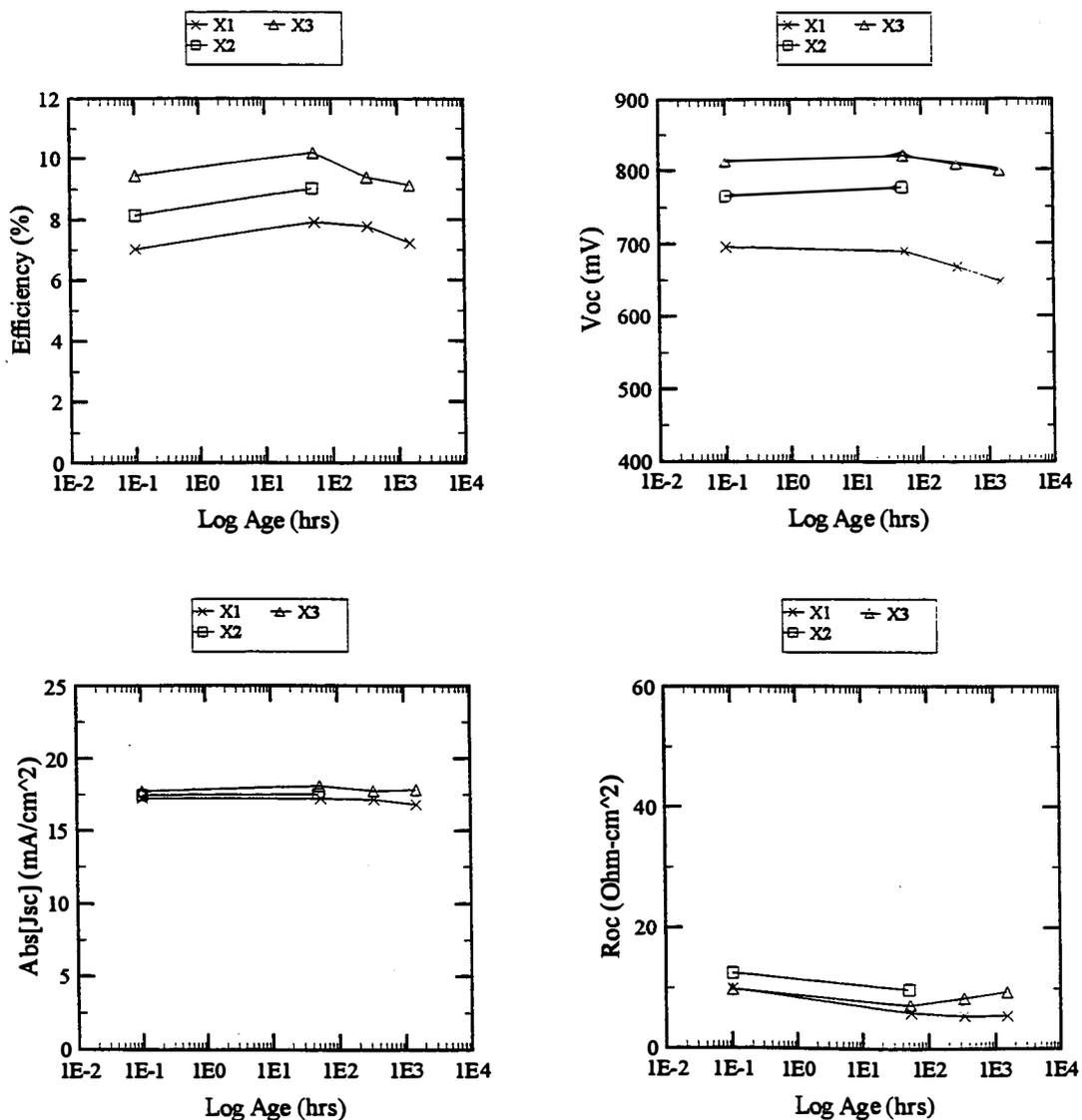
NOTES:

GROUPING METHOD: Group by Recipe

Figure A2

Similar to the data in figure 1, but for irradiance $\sim 70 \text{ mW/cm}^2$, $T=100^\circ\text{C}$, bias= V_{oc} . Again, the SCI X3 and USF samples show similar trends, both showing an increase in R_{oc} . Although the η changes are similar, the USF samples show more V_{oc} loss, whereas the X3 samples show much greater increase in R_{oc} at an age of ~ 1500 hours.

Bias=LOAD Illum=70 Recipe=CSM1,IEC... Stress_T=65 Grouped by Recipe
 Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



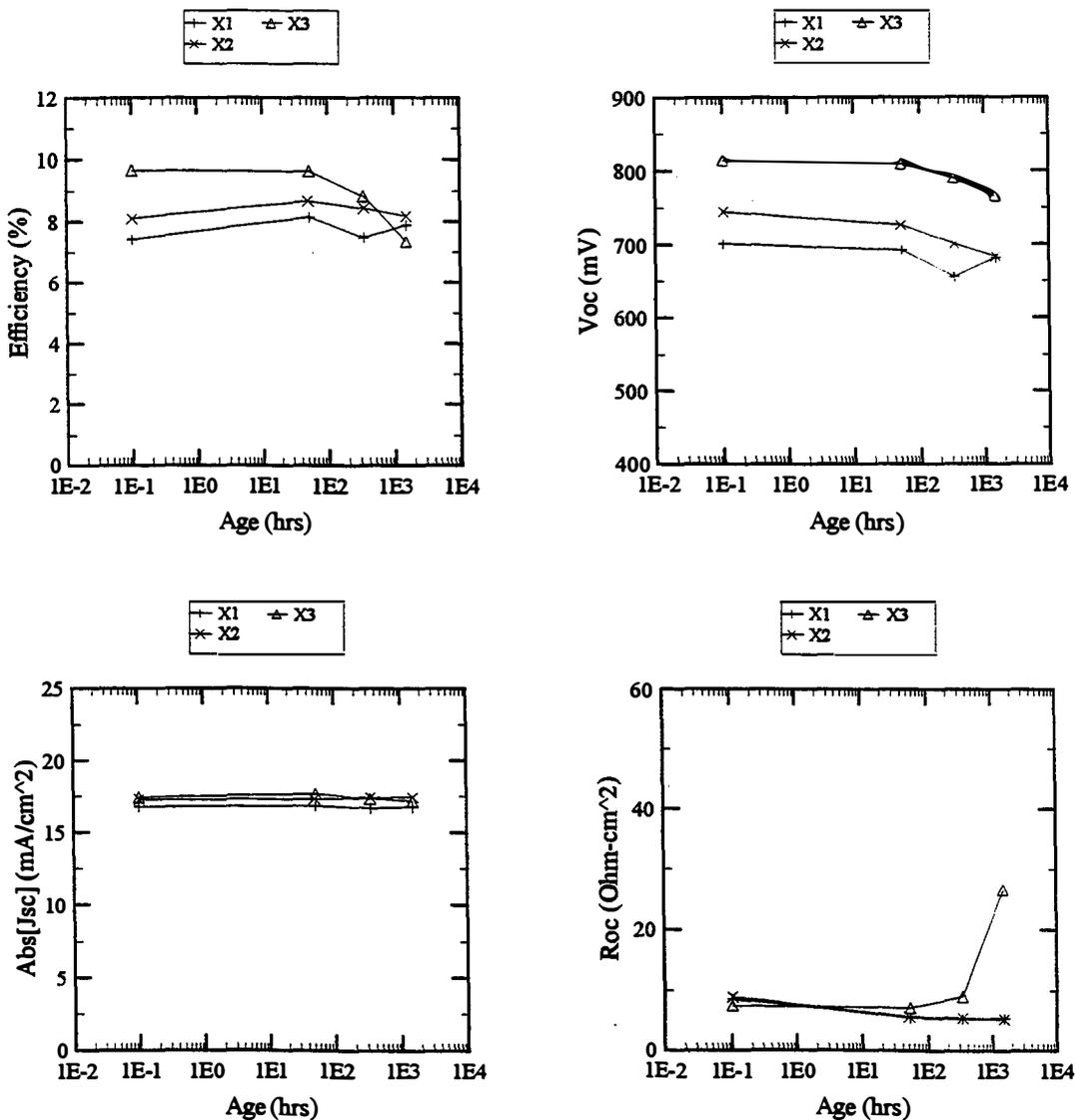
NOTES:

GROUPING METHOD: Group by Recipe

Figure A3

The devices shown here were stressed at illumination ~70mw/cm², T=65°C, bias ~V_{MP} (resistive load). Only the SCI-contacted samples were stressed in this condition, due to the small number of samples available from others. (The X2 substrate was accidentally dropped early in the test, destroying all the X2 devices). In comparison with the similar devices biased at V_{OC} (shown in figure 1), the X3 devices under resistive load are more stable.

Bias=LOAD Illum=70 Recipe=X1,X2,X3... Stress_T=100 Grouped by Recipe
 Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



NOTES:

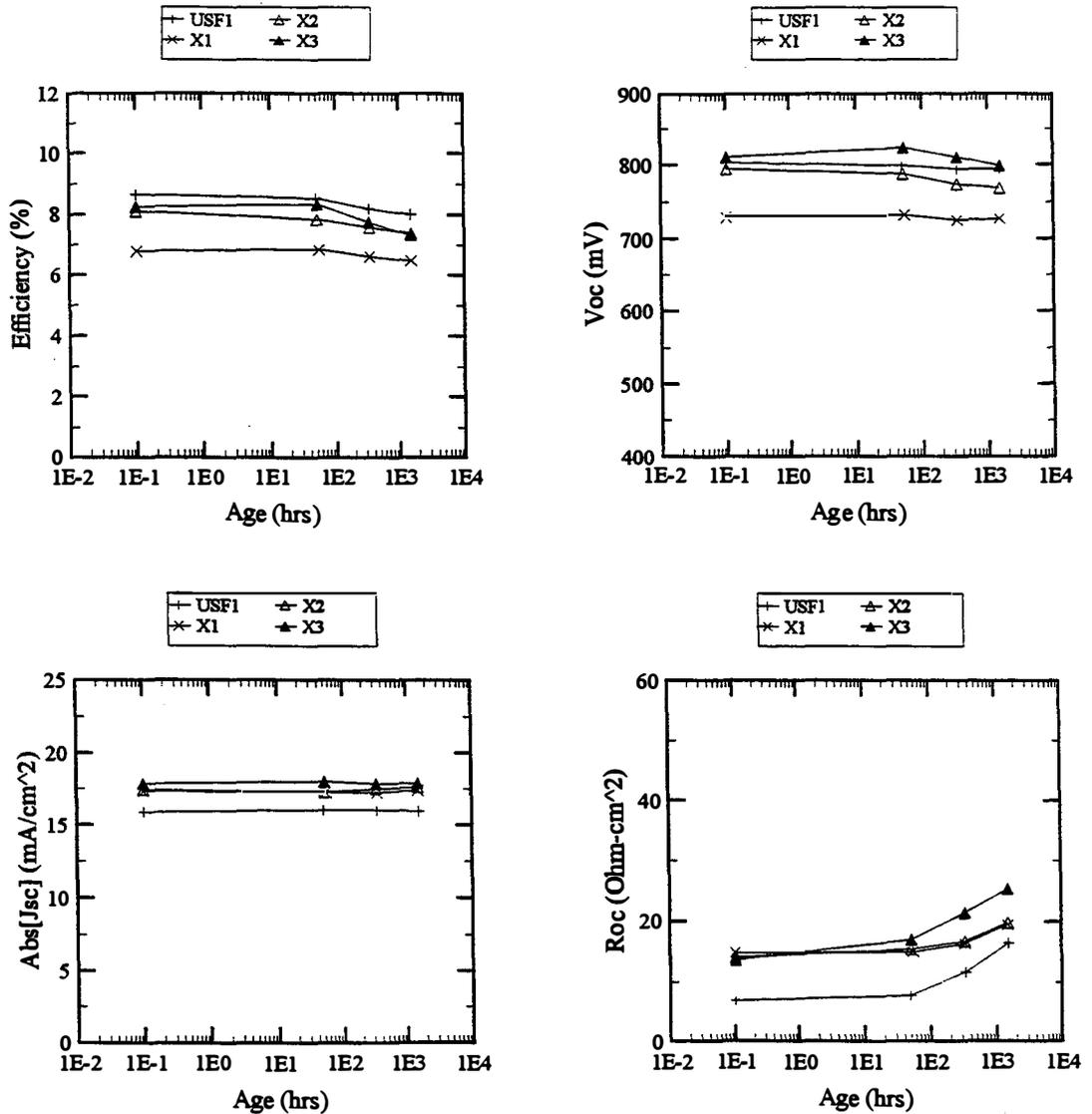
GROUPING METHOD: Group by Recipe

Figure A4

Data for devices stressed at illumination $\sim 70 \text{ mW/cm}^2$, $T=100^\circ\text{C}$, and bias $\sim V_{MP}$ (resistive load). Again, only SCI-contacted devices were tested in this bias condition. Although X3 devices show some loss, the magnitude is less than counterpart devices stressed under open circuit conditions (see figure 2). For SCI contacts X1 and X2, devices subjected to resistive load and open circuit conditions exhibit similar behavior with decreasing V_{oc} but low and stable R_{oc} .

Bias=OC Illum=0 Recipe=USF1,X3,... Stress_T=65 SUB_ID=CSM L10,... Grouped by Recipe

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"

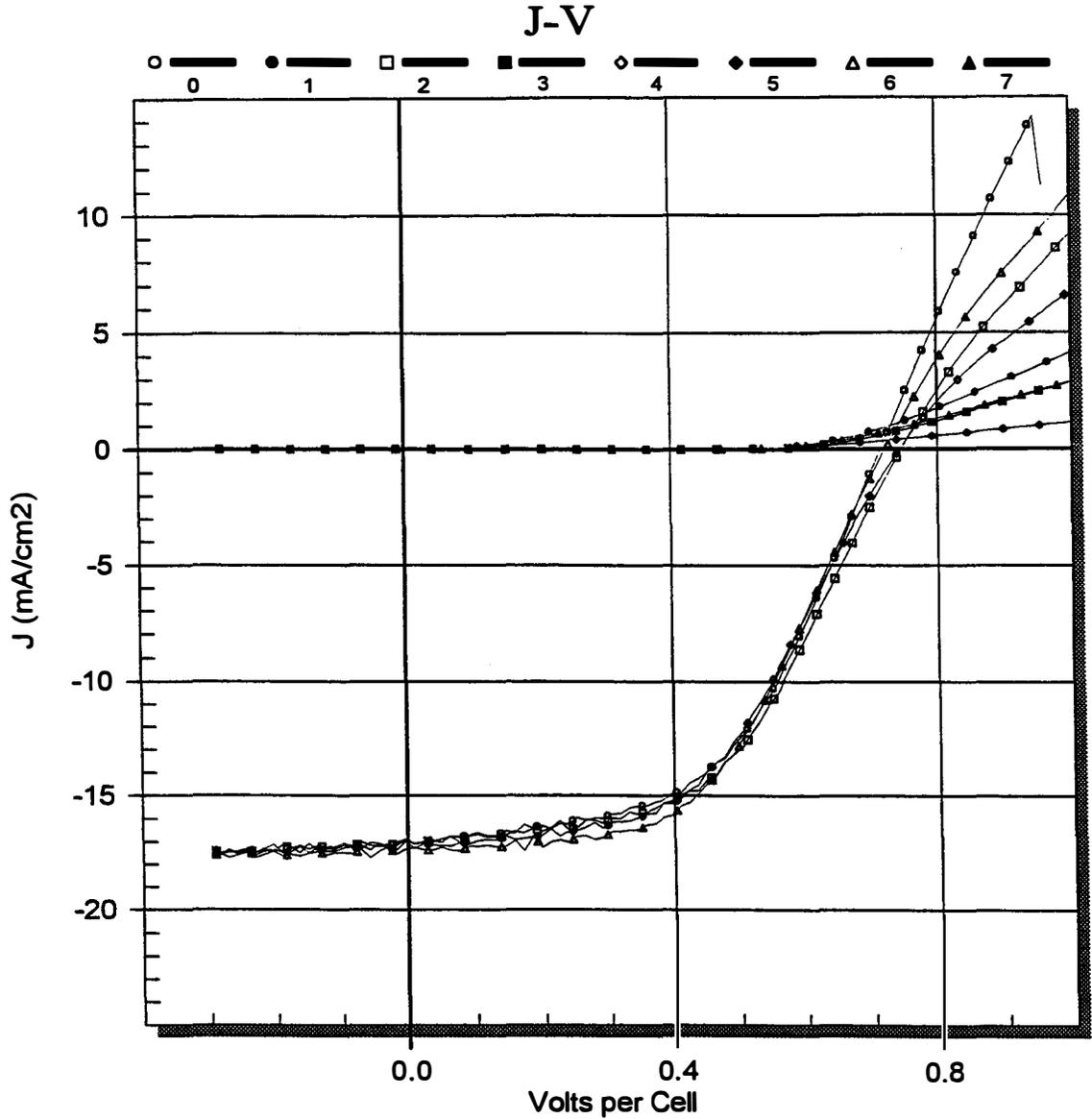


NOTES:

GROUPING METHOD: Group by Recipe

Figure A5

These data show the response of four different contacting schemes to the dark, open circuit bias condition at T=65°C. It is interesting to note that the R_{oc} increase is evident here for *all* contacts. As seen in figure 1, under illumination R_{oc} behavior varied with different contacting schemes, with the X1 devices showing the best R_{oc} performance. Here, both X1 and X2 show increasing R_{oc} , although it is occurring a slower rate than in the USF and X3 devices.



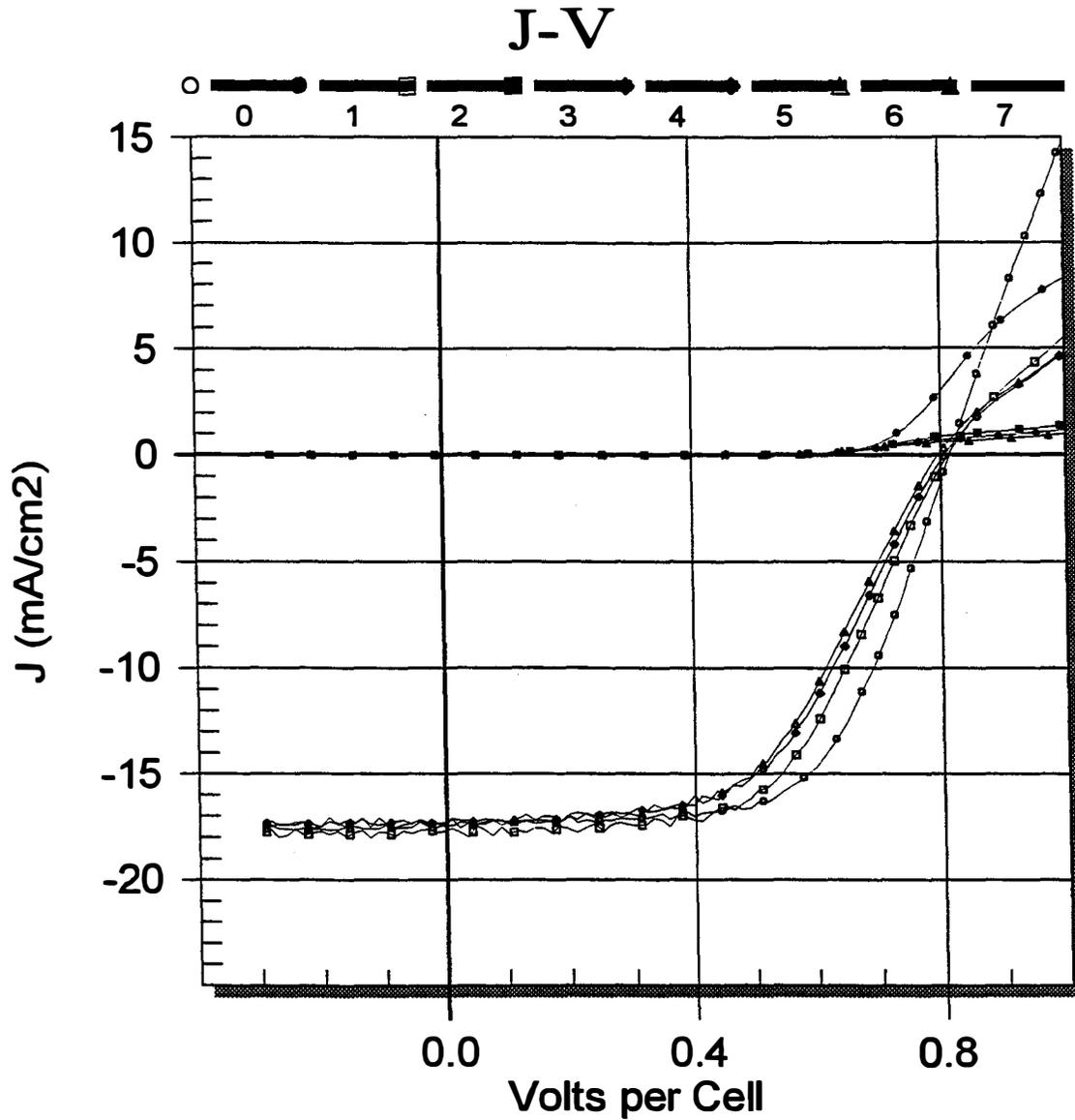
Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L20819B6OC22	PS	0.1	L970721X.615	6.3	-17.0	714	0.52	3.9e+2	14.9	1.8e-4
1	L20819B6OC22	PS		C:\VTESTVB\RAWDATA\X970721\L970721X.615							
2	L20819B6OC22	DARKBIAS	52.8	L970723X.816	6.5	-17.1	745	0.51	5.8e+2	19.7	1.6e-3
3	L20819B6OC22	DARKBIAS		C:\VTESTVB\RAWDATA\X970723\L970723X.816							
4	L20819B6OC22	DARKBIAS	339.1	L970804X.744	6.3	-17.2	742	0.50	1.1e+3	24.7	3.1e-3
5	L20819B6OC22	DARKBIAS		C:\VTESTVB\RAWDATA\X970804\L970804X.744							
6	L20819B6OC22	DARKBIAS	1520.6	L970922X.983	6.5	-17.4	721	0.52	8.4e+2	18.5	1.1e-3
7	L20819B6OC22	DARKBIAS		C:\VTESTVB\RAWDATA\X970922\L970922X.983							

Contact: X1

Illumination: Dark T:100°C

Bias: Voc [-0V]

Figure 5Ab



Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L20819H5OC33	PS	0.1	L970722X.620	8.8	-17.4	815	0.62	1.2e+3	11.6	2.1e-5
1	L20819H5OC33	PS		C:\VTESTVB\RAWDATA\X970722\L970722X.620							
2	L20819H5OC33	DARKBIAS	51.5	L970724X.755	8.1	-17.7	812	0.56	1.7e+3	20.8	4.3e-3
3	L20819H5OC33	DARKBIAS		C:\VTESTVB\RAWDATA\X970724\L970724X.755							
4	L20819H5OC33	DARKBIAS	336.4	L970805X.623	7.5	-17.2	806	0.54	1.7e+3	24.2	5.3e-3
5	L20819H5OC33	DARKBIAS		C:\VTESTVB\RAWDATA\X970805\L970805X.623							
6	L20819H5OC33	DARKBIAS	1494.7	L970922X.892	7.4	-17.4	796	0.54	9.3e+2	24.8	5.2e-3
7	L20819H5OC33	DARKBIAS		C:\VTESTVB\RAWDATA\X970922\L970922X.892							

Contact: X3

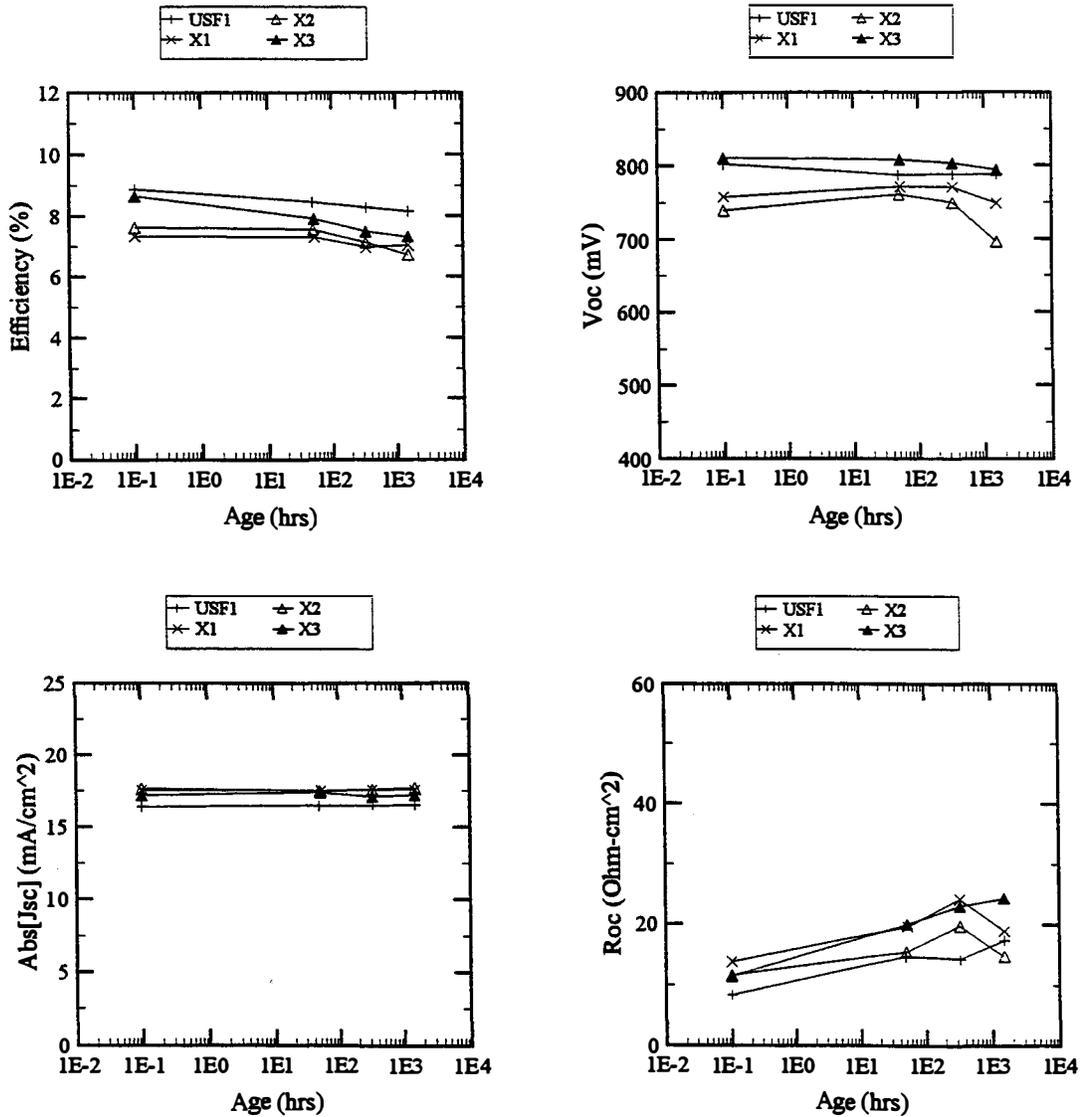
Illumination: Dark T:100°C

Bias: V_{oc} [-0V]

Figure 5Ac

Bias=OC Illum=0 Recipe=USF1,X3,... Stress_T=100 SUB_ID=CSM L10,... Grouped by Recipe

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



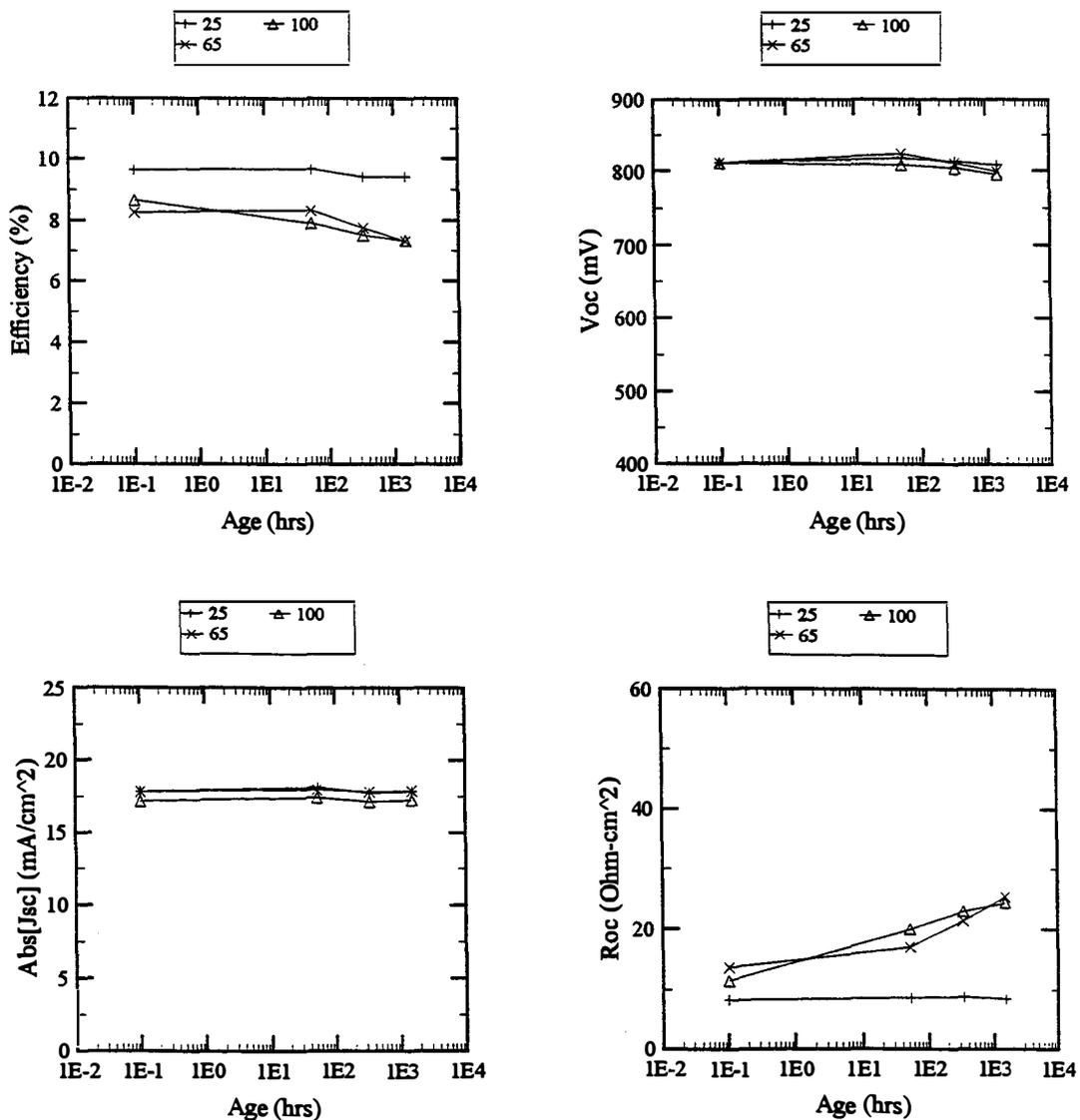
NOTES:

GROUPING METHOD: Group by Recipe

Figure A6

In the dark, open circuit bias condition with $T=100^{\circ}\text{C}$, increasing R_{oc} is again seen across the various contacting schemes shown here. This response is similar to that observed with the same bias condition at $T=65^{\circ}\text{C}$ (shown in figure 5). In this case the initial rate of the increase between the start of the test and the data point at ~50 hours of stress is greater than that observed in the $T=65^{\circ}\text{C}$ data. In addition, more V_{oc} loss is observed in the X2 devices than at the lower stress temperature.

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



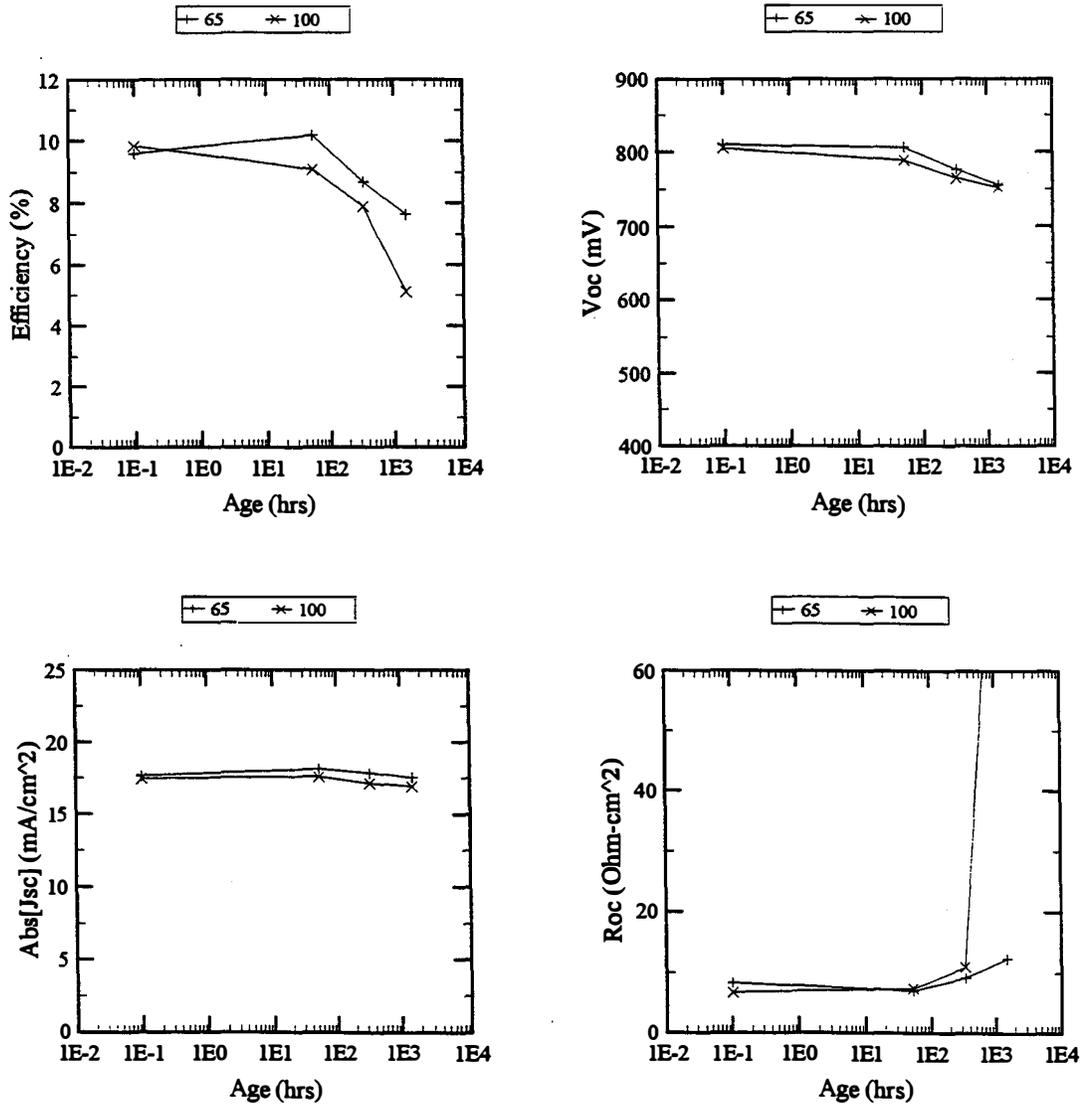
NOTES:

GROUPING METHOD: Group by Stress_T

Figure A7

The data shown here illustrate the effect of temperature (in the absence of light) on the rate of change seen in devices of the X3 contacting scheme. These devices were stressed in the dark, open circuit condition. The 25°C data shown here are the measurements of the control samples. Changes in both η and R_{oc} are more severe at higher temperatures but the difference between 65°C and 100°C is not large.

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



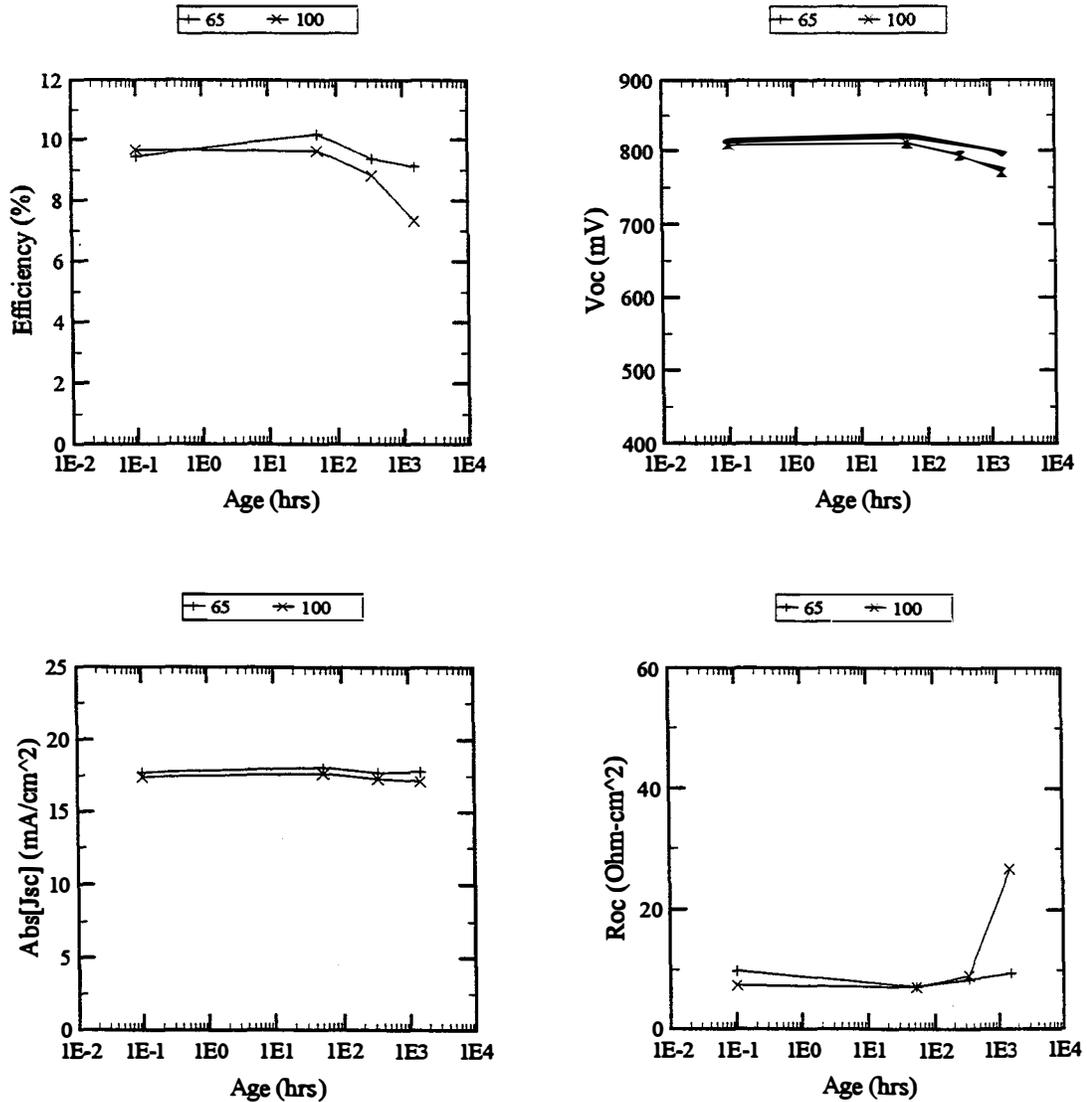
NOTES:

GROUPING METHOD: Group by Stress_T

Figure A8

The data shown here illustrates the effect of temperature in the 70mW/cm², open circuit condition on X3 devices. The η decrease is significantly greater for devices stressed at 100°C than for those stressed at 65°C, although the V_{oc} changes are similar at both temperatures.

Bias=LOAD Illum=70 Recipe=X3 Stress_T=25,65,... Grouped by Stress_T
 Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



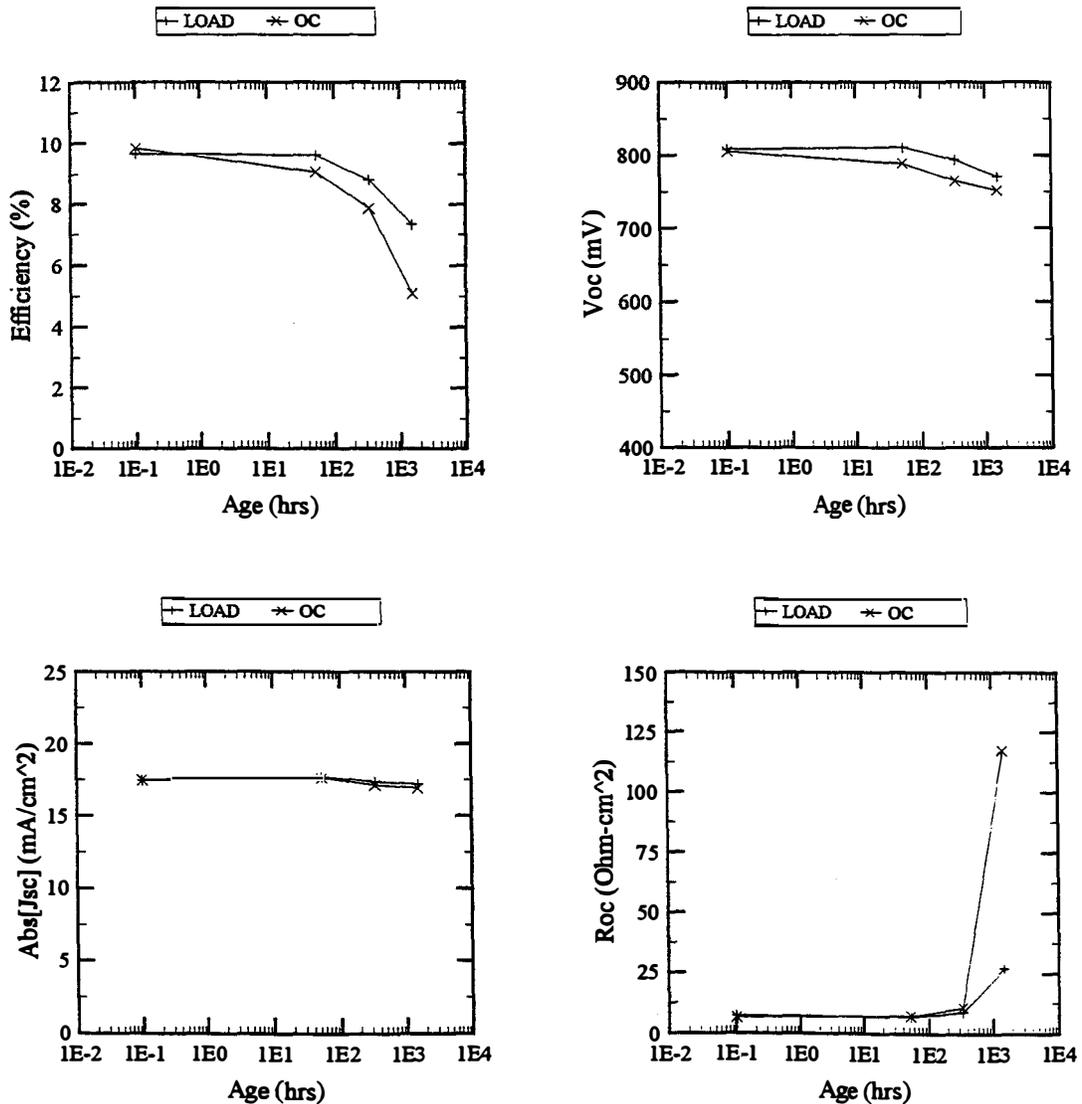
NOTES:

GROUPING METHOD: Group by Stress_T

Figure A9

Shown here are the data for X3 devices biased at $\sim V_{MP}$ (resistive load), and stressed at $T=65^{\circ}\text{C}$ and $T=100^{\circ}\text{C}$. Device changes are similar to but of a lesser magnitude than those seen in open circuit conditions.

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



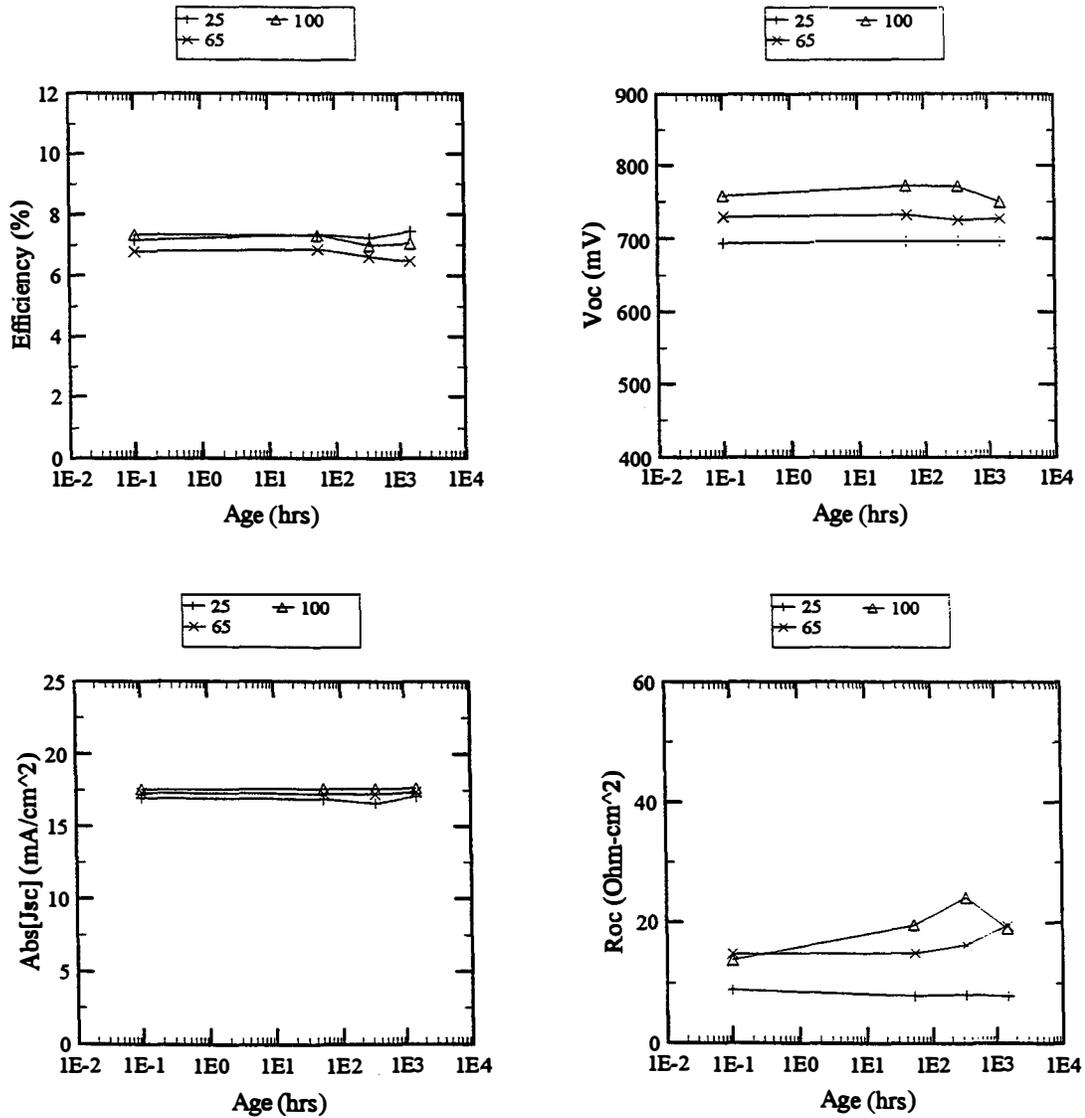
NOTES:

GROUPING METHOD: Group by Bias

Figure A10

The effects of bias voltage on X3 devices are shown here. Although these data resemble those of figure 8, here T is held constant and the devices are grouped by bias condition. It is clear that decreases in η , V_{oc} , are related to the bias on the devices, with the open circuit (V_{oc} at $\sim 70 \text{ mW/cm}^2$ illumination) condition producing more severe effects. Bias condition also appears to have a similar effect on increases in R_{oc} . Interestingly, these effects were not observed in all contacting schemes studied here. Refer to figure 13 for a similar set of plots involving the X1 contacting scheme.

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"

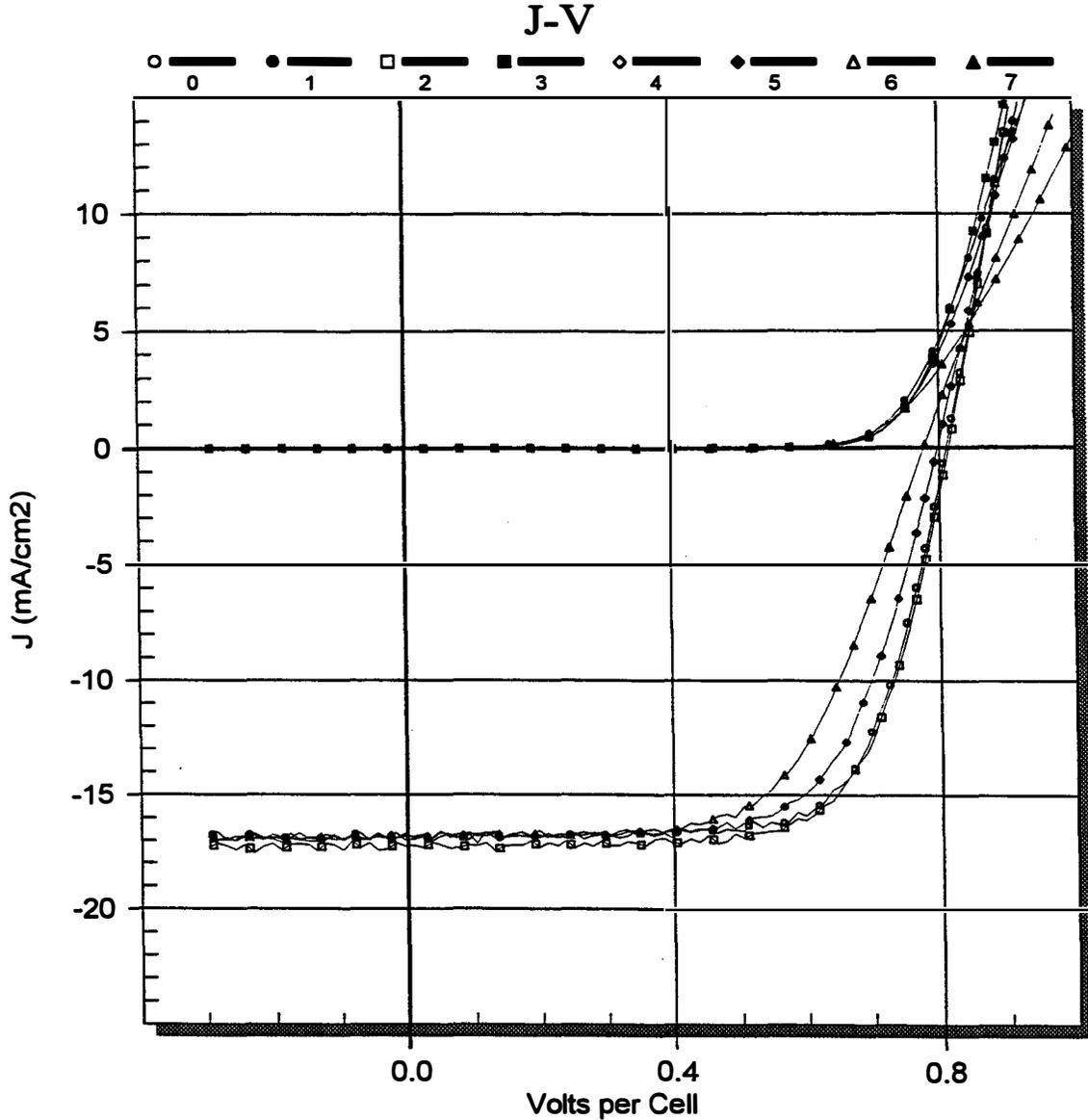


NOTES:

GROUPING METHOD: Group by Stress_T

Figure A11

These data show the response of the X1 contacting scheme to temperature, in the absence of light. Overall, the X1 devices are more stable, although some R_{oc} increase is evident. The temperature dependence of this contacting scheme is less severe than that of the X3 devices shown in figure 7.



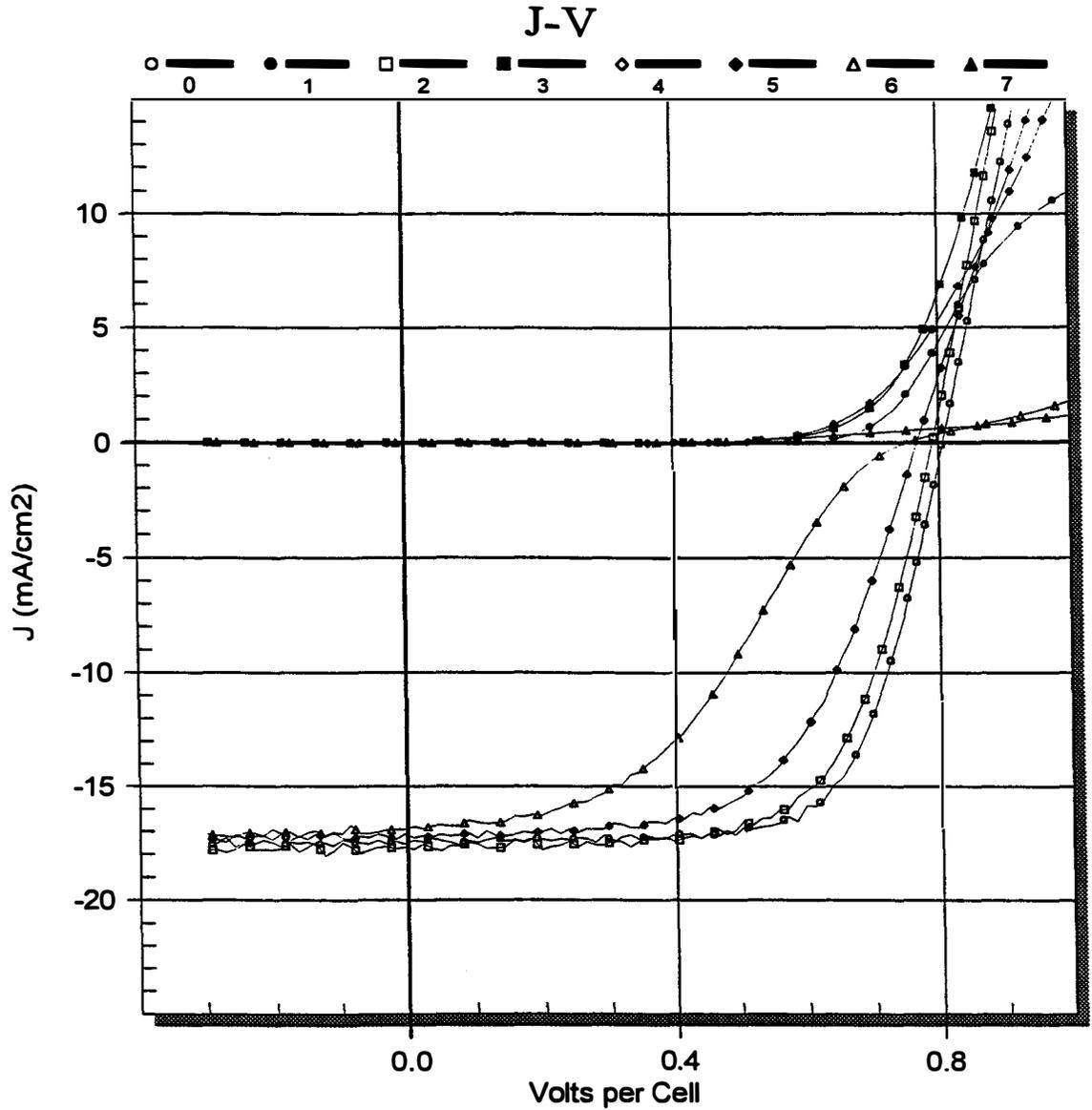
Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L2081914RL23	PS	0.1	L970722X.594	9.5	-16.8	810	0.70	2.1e+3	7.1	-1.1e-4
1	L2081914RL23	PS		C:\VTEST\B\RAWDATA\X970722\L970722X.594							
2	L2081914RL23	LS	52.5	L970724X.776	9.7	-17.2	813	0.69	1.2e+4	6.8	-8.5e-5
3	L2081914RL23	LS		C:\VTEST\B\RAWDATA\X970724\L970724X.776							
4	L2081914RL23	LS	337.1	L970805X.636	8.9	-16.9	797	0.66	1.3e+3	8.5	-5.3e-5
5	L2081914RL23	LS		C:\VTEST\B\RAWDATA\X970805\L970805X.636							
6	L2081914RL23	LS	1494.8	L970922X.876	8.0	-16.8	777	0.61	2.5e+3	12.3	3.0e-4
7	L2081914RL23	LS		C:\VTEST\B\RAWDATA\X970922\L970922X.876							

Contact: X3

Illumination: 70mW/cm² T:100°C

Bias: V_{MP} (resistive load)

Figure 11Ab



Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L2081914OC32	PS	0.1	L970722X.598	9.6	-17.5	806	0.69	1.0e+4	7.5	-2.3e-5
1	L2081914OC32	PS		C:\VTESTVB\RAWDATA\X970722\L970722X.598							
2	L2081914OC32	LS	52.5	L970724X.781	9.1	-17.8	790	0.65	1.4e+3	7.5	-9.6e-5
3	L2081914OC32	LS		C:\VTESTVB\RAWDATA\X970724\L970724X.781							
4	L2081914OC32	LS	337.1	L970805X.640	7.8	-17.2	767	0.59	1.3e+3	11.5	9.3e-5
5	L2081914OC32	LS		C:\VTESTVB\RAWDATA\X970805\L970805X.640							
6	L2081914OC32	LS	1494.9	L970922X.881	5.2	-16.9	752	0.41	4.5e+2	101.1	1.2e-1
7	L2081914OC32	LS		C:\VTESTVB\RAWDATA\X970922\L970922X.881							

Contact: X3

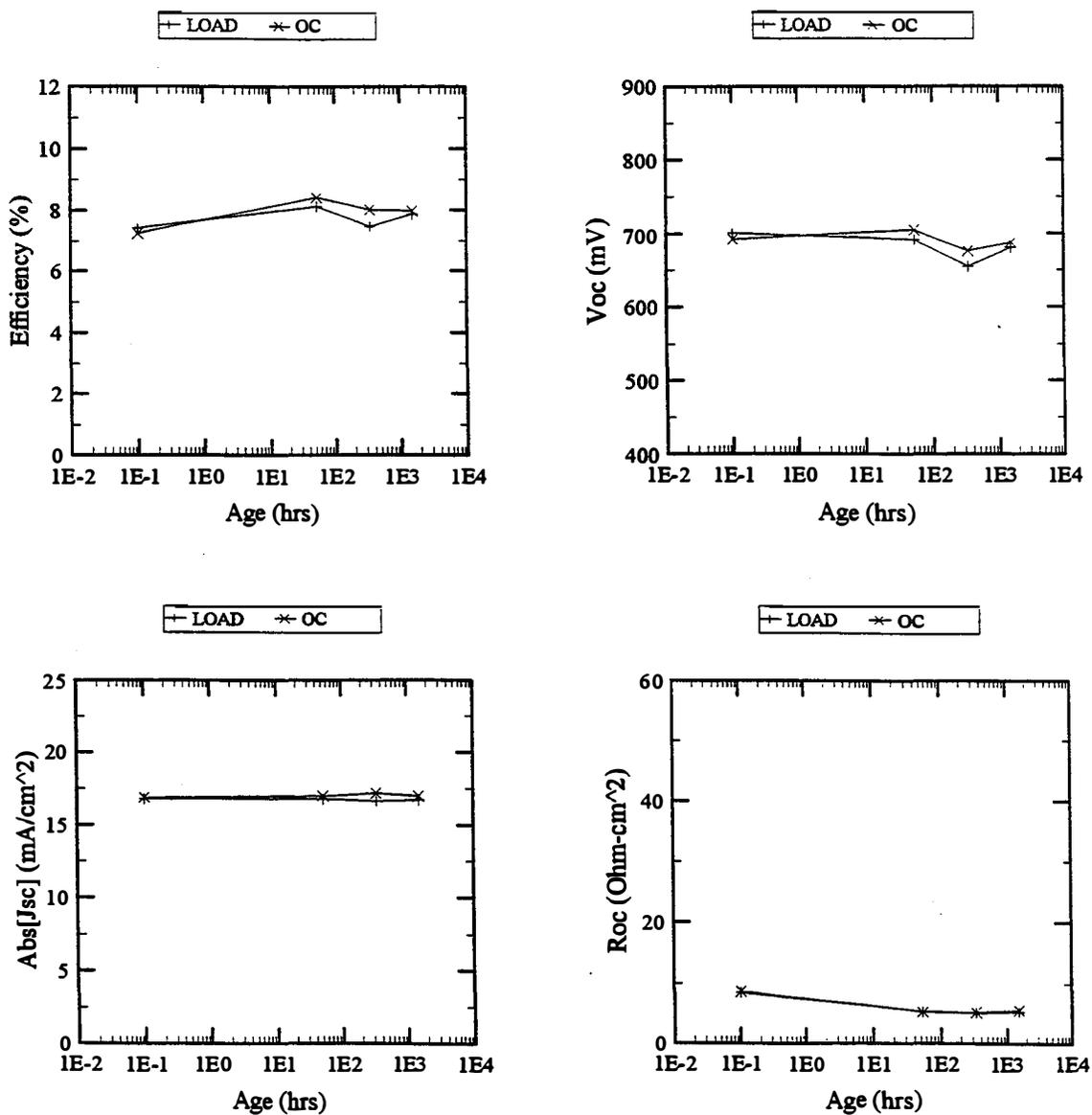
Illumination: 70mW/cm²

T:100°C

Bias: Voc

Figure11Ac

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"

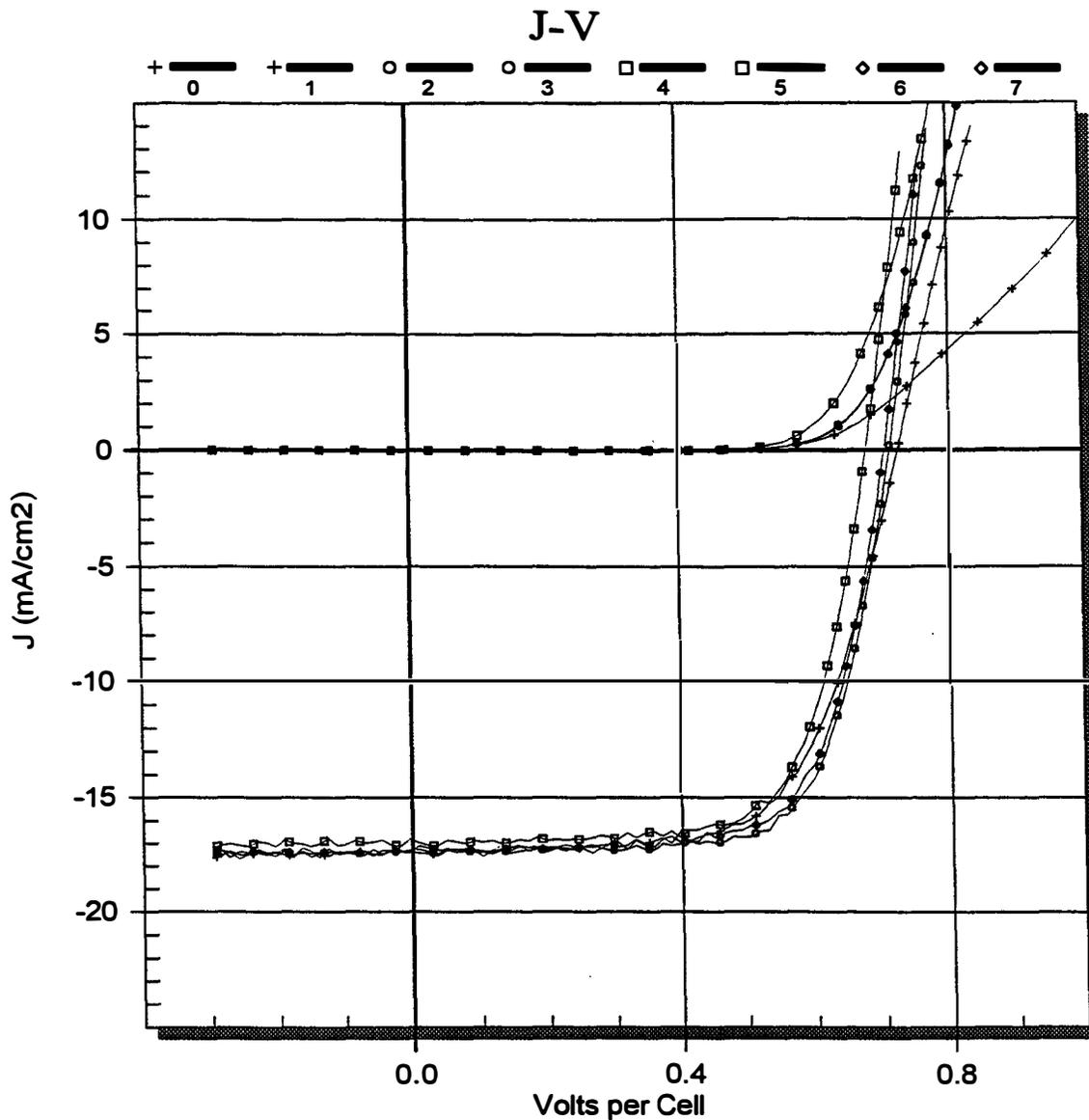


NOTES:

GROUPING METHOD: Group by Bias

Figure A12

The X1 contacting scheme shows significantly less bias dependence than the X3 devices in 70mW/cm² illumination at T=100°C. X1 devices exhibit little change with good R_{oc} behavior in both bias conditions.



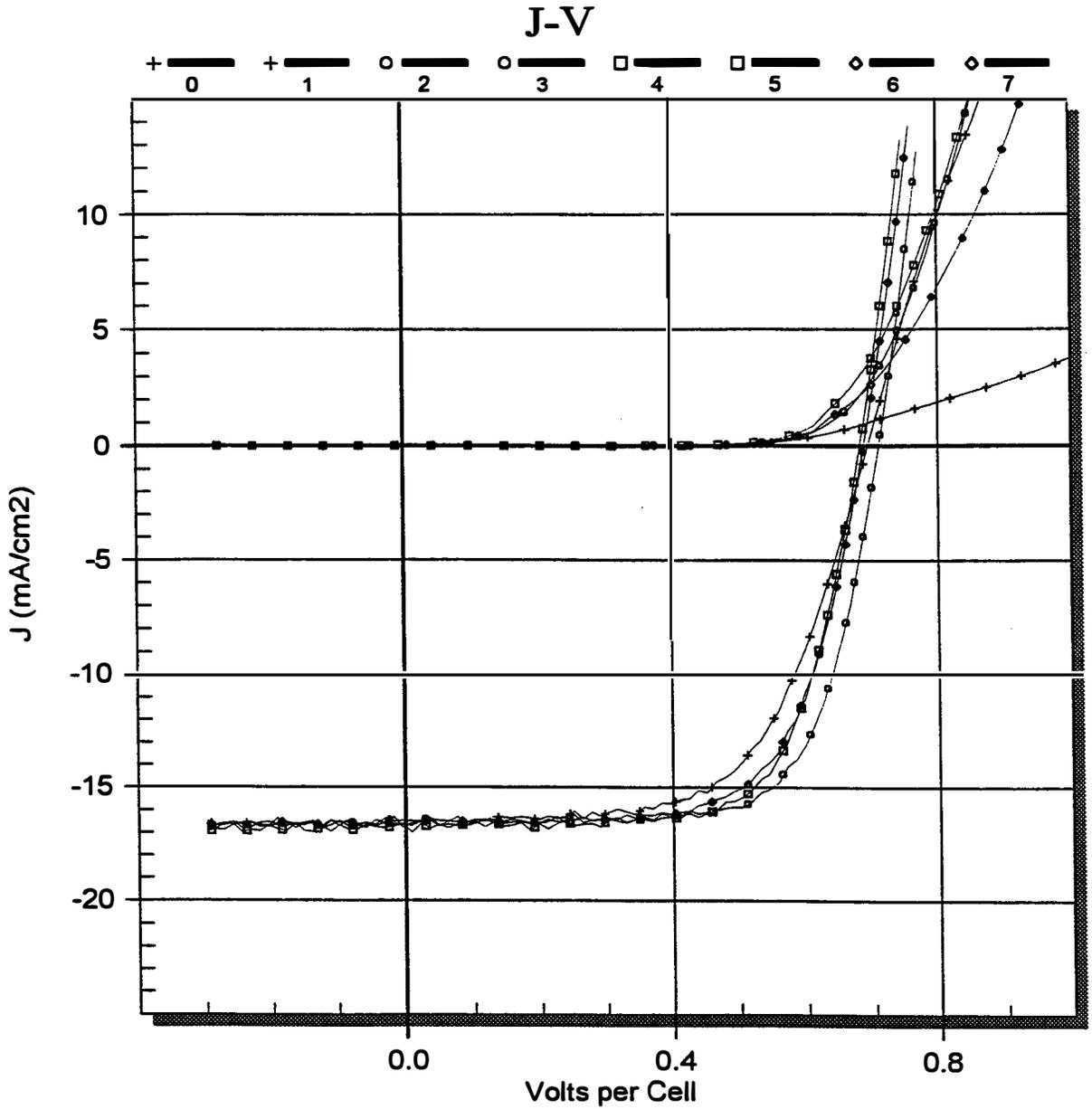
Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L20819K6RL21	PS	0.1	L970721X.651	8.1	-17.4	723	0.65	2.0e+3	7.8	2.3e-5
1	L20819K6RL21	PS		C:\VTTESTVB\RAWDATA\X970721\L970721X.651							
2	L20819K6RL21	LS	53.1	L970723X.856	8.7	-17.3	710	0.71	2.7e+3	5.1	-1.0e-4
3	L20819K6RL21	LS		C:\VTTESTVB\RAWDATA\X970723\L970723X.856							
4	L20819K6RL21	LS	339.2	L970804X.778	8.0	-17.0	676	0.70	7.7e+3	5.1	-1.2e-4
5	L20819K6RL21	LS		C:\VTTESTVB\RAWDATA\X970804\L970804X.778							
6	L20819K6RL21	LS	1519.4	L970922X.950	8.5	-17.3	703	0.70	1.1e+3	5.1	-1.1e-4
7	L20819K6RL21	LS		C:\VTTESTVB\RAWDATA\X970922\L970922X.950							

Contact: X1

Illumination: 70mW/cm² T:100°C

Bias: V_{MP} (resistive load)

Figure 12Ab



Index	Sample	ProcessCode	Age	File	Eff	Jsc	Voc	FF	Rsc	Roc	Sfactor
0	L20819K6OC23	PS	0.1	L970721X.647	7.0	-16.5	692	0.61	2.9e+3	9.7	1.3e-4
1	L20819K6OC23	PS		C:\VTESTVB\RAWDATA\X970721\L970721X.647							
2	L20819K6OC23	LS	53.2	L970723X.860	8.2	-16.6	709	0.70	2.2e+3	5.6	-1.1e-4
3	L20819K6OC23	LS		C:\VTESTVB\RAWDATA\X970723\L970723X.860							
4	L20819K6OC23	LS	339.3	L970804X.783	7.9	-16.8	680	0.69	2.4e+3	5.5	-1.0e-4
5	L20819K6OC23	LS		C:\VTESTVB\RAWDATA\X970804\L970804X.783							
6	L20819K6OC23	LS	1519.5	L970922X.954	7.6	-16.6	686	0.67	2.1e+3	6.1	-1.3e-4
7	L20819K6OC23	LS		C:\VTESTVB\RAWDATA\X970922\L970922X.954							

Contact: X1

Illumination: 70mW/cm²

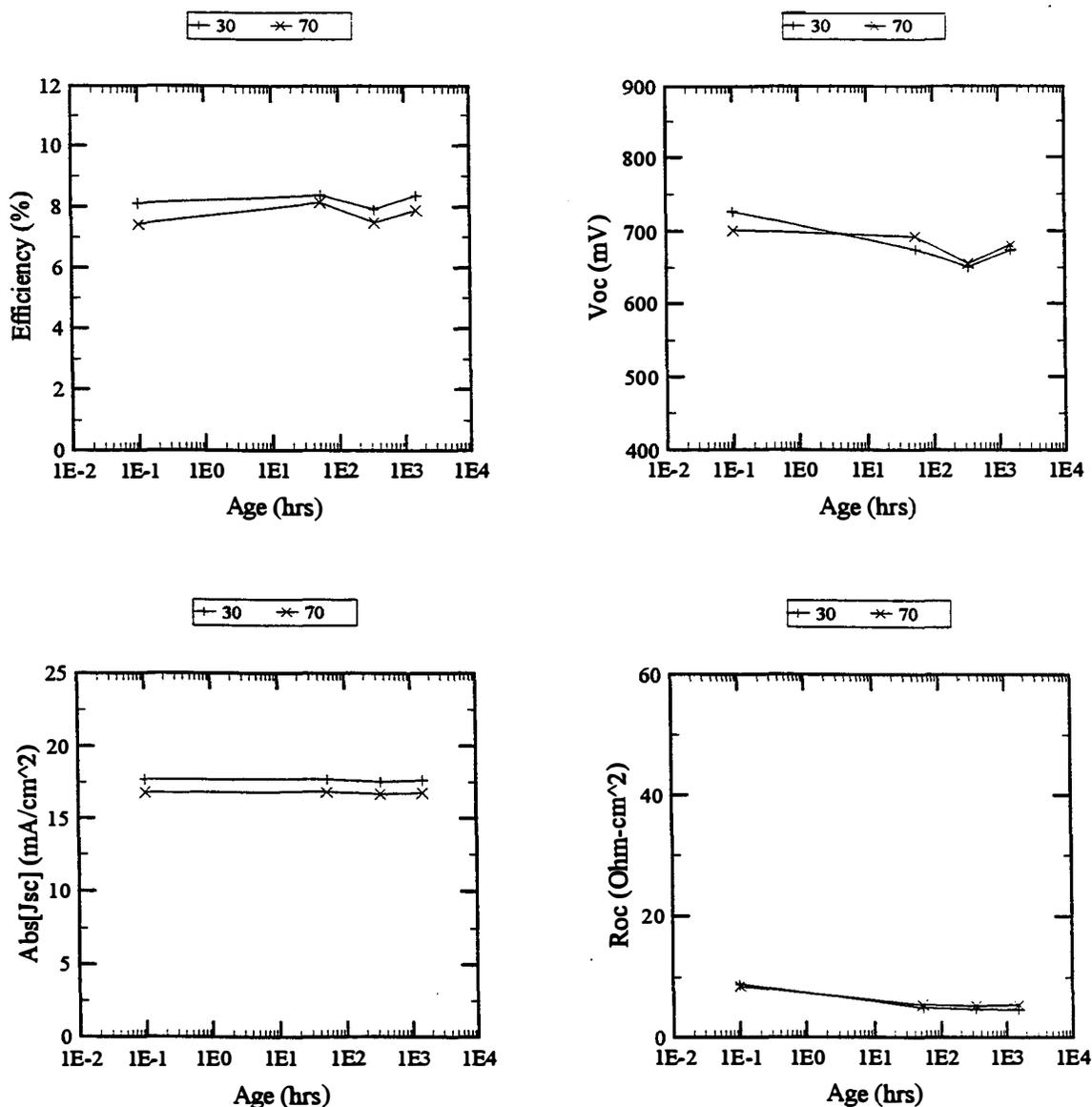
T:100°C

Bias: Voc

Figure 12Ac

Bias=LOAD Illum=30,70 Recipe=X1 Stress_T=100 Grouped by Illum

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



NOTES:

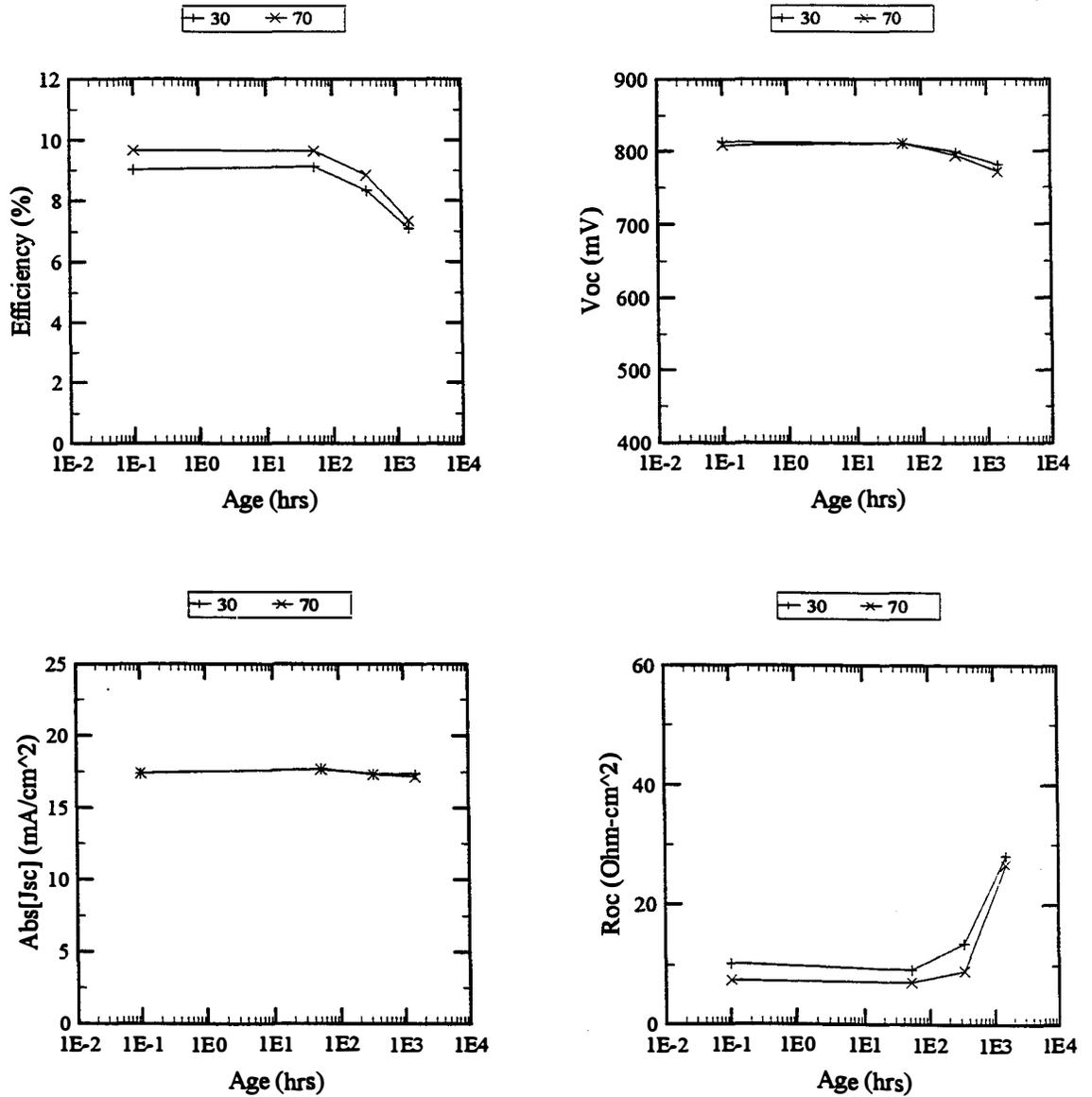
GROUPING METHOD: Group by Illum

Figure A13

In these plots the response of X1 samples to different irradiance levels is shown. These devices were stressed in illumination of ~30 mW/cm² and ~70mW/cm², biased near V_{MP}, at T=100°C. Similar performance is evident, indicating that the dependence of the X1 devices on irradiance level is weak, at least within the range used here. The X3 contacting scheme also showed little dependence on irradiance level, as shown in figure 14. Curiously, the 30mW/cm² devices showed more V_{OC} loss, while the R_{OC} performance is slightly better than the 70mW/cm² samples. However, in general the two sets of devices show nearly identical responses to the two different irradiance levels.

Bias=LOAD Illum=30,70 Recipe=X3 Stress_T=100 Grouped by Illum

Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



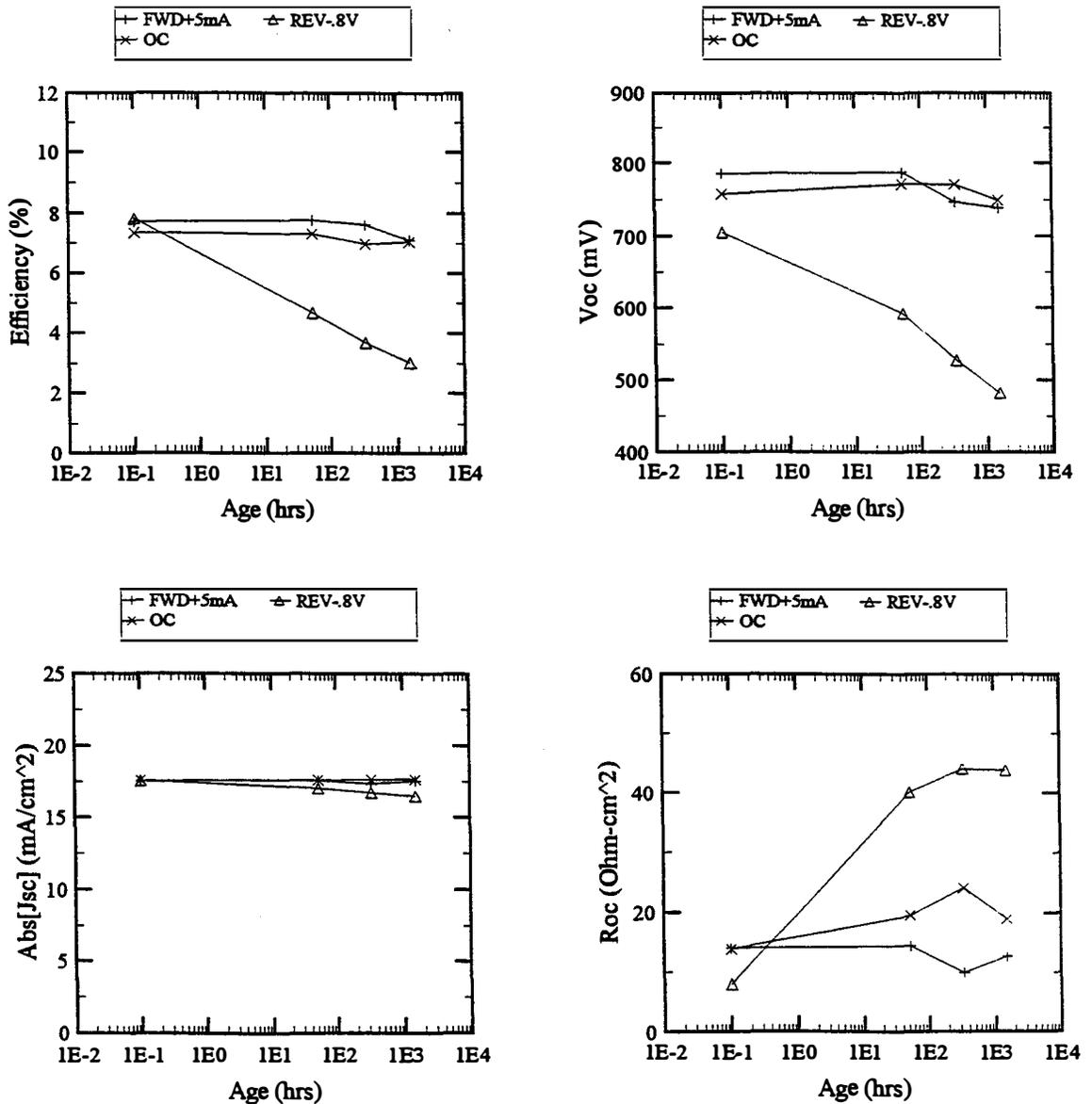
NOTES:

GROUPING METHOD: Group by Illum

Figure A14

These data are similar to those of figure 13, but for the X3 contacting scheme. The stress condition is again $\sim V_{MP}$ bias, $T=100^{\circ}\text{C}$, with two irradiance levels. Remarkably similar performance is seen between the two groups of devices. Unfortunately, no open circuit-biased devices were tested at the $30\text{mW}/\text{cm}^2$ irradiance level, so comparisons of open circuit-biased devices was not possible in this round of the test. It is suggested that the $30\text{mW}/\text{cm}^2$, open circuit at $T=65^{\circ}\text{C}$ and $T=100^{\circ}\text{C}$ be included in further testing if this comparison is of interest.

Bias=FWD+5mA,RE... Illum=0 Recipe=X1 Stress_T=100 Grouped by Bias
 Plots shown are averages of 4 replicate devices Data Source: Table "CellAverages" in database "IV_X.MDB"



NOTES:

GROUPING METHOD: Group by Bias

Figure A15

Response of the X1 contacting scheme to different biases in the dark at T=100°C is shown here. Dramatic differences in the responses are evident. Clearly, the reverse biased (-800mV/cell) condition is the most severe test. The data suggest an exponential time dependence for devices in the reverse bias condition. X1, X2, and X3 devices all are very susceptible to the reverse bias stress.

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE September 1998	3. REPORT TYPE AND DATES COVERED Phase III Final Technical Report, 14 March 1997-1 April 1998	
4. TITLE AND SUBTITLE Technology Support for Initiation of High-Throughput Processing of Thin-Film CdTe PV Modules; Phase III Final Technical Report, 14 March 1997-1 April 1998			5. FUNDING NUMBERS C: ZAF-5-14142-05 TA: PV804401	
6. AUTHOR(S) R.C. Powell, G.L. Dorer, U. Jayamaha, and J.J. Hanak				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Solar Cells, Inc. 1702 N. Westwood Ave. Toledo, OH 43607			8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393			10. SPONSORING/MONITORING AGENCY REPORT NUMBER SR-520-25422	
11. SUPPLEMENTARY NOTES NREL Technical Monitor: H.S. Ullal				
12a. DISTRIBUTION/AVAILABILITY STATEMENT National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161			12b. DISTRIBUTION CODE	
13. ABSTRACT (<i>Maximum 200 words</i>) This report describes work performed by Solar Cells, Inc. (SCI), during Phase III of this subcontract. As a result of the R&D effort, the vapor transport deposition (VTD) process achieved a status in which linear coating speeds in excess of 8 ft/min were achieved for the semiconductor, equal to about two modules per minute, or 144 kW per 24-h day. The process has been implemented in a production line, which is capable of round-the-clock continuous production of coated substrates 120 cm x 60 cm in size at a rate of 1 module every four minutes, equal to 18 kW/day. Currently, the system cycle time is limited by the rate of glass introduction into the system and glass heating, but not by the rate of the semiconductor deposition. A new SCI record efficiency of 14.1% was achieved for the cells. For the modules produced by the rapid VTD process, the best efficiency achieved thus far is 8.4%, compared with the record of 9.1% for the close-spaced sublimation process. Three arrays and one set of modules on outdoor stability tests for up to 3 years continue to show excellent stability. The National CdTe Team has implemented an Accelerated Life Testing program and has identified a high-temperature degradation process. The effort in SCI's Dot-Matrix process has resulted in the development of one version of the process, showing PV performance comparable to the existing "line-patterning" process done by laser scribing. The capability of patterning of transparent conducting oxide layers has been demonstrated by an alternative non-laser process.				
14. SUBJECT TERMS photovoltaics ; high-throughput processing ; thin-film CdTe modules ; vapor transport deposition ; characterization and performance ; PV devices ; contact layers ; alternative cell interconnects ; instrumentation ; measurements ; stability testing			15. NUMBER OF PAGES 85	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL	