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Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements

Semiannual Subcontract Report 1 January 1995 – 30 June 1995

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PREFACE

This Semi-Annual Technical Progress Report covers the work performed by Solarex for the period January 1, 1995 to June 30, 1995 under DOE/NREL Subcontract # ZAI-4-11294-01 entitled "Cast Polycrystalline Silicon Photovoltaic Module Manufacturing Technology Improvements". This is the third Semi-Annual Technical Report for this subcontract. The subcontract is scheduled to run from December 8, 1993 to December 7, 1996.

The following personnel at Solarex have contributed to the technical efforts covered in this report.

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In addition, Solarex has been supported by the staff at the Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI). ARRI staff working on the subcontract include:

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SUMMARY

The objective of this three-year program is to advance Solarex's cast polycrystalline silicon manufacturing technology, reduce module production cost, increase module performance and expand Solarex's commercial production capacities. Two specific objectives of this program are to reduce the manufacturing cost for polycrystalline silicon PV modules to less than $1.20/watt and to increase the manufacturing capacity by a factor of three. To achieve these objectives, Solarex is working in the following technical areas:

CASTING

The goal of the casting task is to develop the ability to cast ingots that yield four bricks with a cross-section of 15 cm by 15 cm with at least equivalent material quality as now achieved for 11.4 cm by 11.4 cm bricks. This represents a 73% increase in the useable silicon obtained from each casting.

WIRE SAWS

The goal of the wire saw task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μm centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

CELL PROCESS

The goal of the cell task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. The developed process must be compatible with automated manufacturing at large volumes.

MODULE ASSEMBLY

The goal of the module assembly task is to modify Solarex's present module assembly system to increase throughput by 100% and decrease the labor requirement by 50%. The Automation and Robotics Research Institute at the University of Texas at Arlington (ARRI) is to work with Solarex to model the present automated module assembly system and to recommend modifications to increase throughput and reduce labor.

FRAMELESS MODULE DEVELOPMENT

The goal of the frameless module task is to develop and qualify a frameless module design incorporating a lower cost back sheet material (less than $0.05/square foot) and user friendly, low cost electrical termination (less than $1.00/module). Since PVMaT is designed for large systems, modules can be designed to mount directly onto the support structure without integral frames.

AUTOMATED CELL HANDLING

The goal of the automated cell handling task is to develop automated handling equipment for 200 μm thick 15 cm by 15 cm polycrystalline silicon wafers and cells with a high yield (less than 0.1% breakage per process handling step) at a throughput rate of at least 12 cells or wafers per minute.

ACCOMPLISHMENTS

Accomplishments during the reporting period include:

- Cast first successful larger ingot producing 73 % larger volume of usable silicon.
- Increased the size of the ingot even further and cast an ingot yielding 9 - 11.4 cm by 11.4 cm bricks, representing a 125% increase in usable silicon from a single casting.
- Operated the wire saw in a semi-operational mode, producing 459,000 wafers at 94.1% overall yield during the 6 month period.
- Reduced the cost of wire saw consumables (grit and oil), spare parts (pulleys) and waste disposal.
- Developed a cost effective back surface field process that increases cell efficiency by 5% and began production trials.
- Developed a plan for increasing the capacity in the module assembly area to 18 Megawatts by 1998. Identified the equipment and personnel necessary to meet the projected market growth to 18 Megawatts and began to implement the plan by procuring the necessary equipment.
- Completed qualification testing of modules built using Spire's automated tabbing and stringing machine developed under their PVMaT Program.
- Selected, tested and qualified a low cost (less than $1.00 per module) electrical termination system.
- Completed long term UV testing of experimental back sheets. Qualified two low cost candidate materials and ordered large module size samples of each.
- Qualified the structure and adhesive tape system for mounting frameless modules and used the adhesive tape system to build a 100 kW system at SMUD.
- ARRI completed a study of the fracture properties of cast polycrystalline silicon wafers and provided the information necessary to calculate the maximum stresses allowable during wafer handling.

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1.0 INTRODUCTION

The goal of Solarex's Crystalline PVMaT program is to improve the present Polycrystalline Silicon manufacturing facility to reduce cost, improve efficiency and increase production capacity. Key components of the program are:

- Casting of larger ingots.
- Use of wire saws to cut thinner, larger size wafers with less kerf loss.
- Transfer of higher efficiency cell processes to manufacturing.
- Increased automation in module assembly.
- High reliability mounting techniques for frameless modules.
- Automated handling of large, thin wafers.

The results of these efforts will be to reduce the module cost per watt to less than $1.20/watt, to increase the production capacity of Solarex's Frederick plant by a factor of 3 and to provide larger, higher efficiency modules that reduce the customer's balance of systems cost. All of this is to be achieved without sacrificing the high reliability already achieved with the crystalline modules in use today.

The rationale behind the Solarex program is to use as much as possible of the present equipment and processes, making improvements that lead to larger sizes, better utilization of materials, higher efficiencies and reduced labor requirements. In this way the maximum increase in capacity and reduction in cost can be achieved with justifiable capital investments in equipment modifications. Specific areas to be addressed in the program are discussed briefly below.

Today Solarex casting stations are used to produce ingots from which 4 bricks, each 11.4 cm by 11.4 cm in cross section are cut. The stations themselves are physically capable of holding an ingot that would be large enough to cut 4 bricks 15 cm by 15 cm in cross-section or 9 bricks 11.4 cm by 11.4 cm. Task 6 involves making the modifications in equipment and process necessary to cast larger ingots. This effort will increase the production capacity of Solarex's casting stations by 73% to 125% and reduce the labor content by an equivalent percentage.

Wire saws can be used to cut thinner wafers with less kerf, than is possible on the Internal Diameter (ID) saws now in use at Solarex. The program goal is to reduce the center to center cut distance from 600 microns on the ID saw to 400 microns on the wire saw. This will result in a 50% increase in solar cell and module output from the same silicon feedstock purchased and cast. That is, with the same amount of feedstock material and the same casting capacity Solarex will be able to increase its output of PV modules by 50% (on top of the increase achieved by casting larger ingots). In addition, wire saws can also be utilized to cut larger wafers, something ID saws can not do.

Finally, wire saws have a much higher production capacity than ID saws. One wire is producing as many wafers as 16 ID saws. To increase capacity with wire saws requires a much smaller capital investment than would be required to achieve the same increase with ID saws. The major issue with wire saws was the ability to reduce the variable cost to cut a wafer. Efforts to reduce the cost of grit, oil, wire, spare parts and labor make up the major part of Task 7.

In this program, Solarex is working on the transfer of high efficiency cell technologies from the laboratory to production. Issues involved in the successful transfer include process cost, ability to scale to large volume, adaptability to automation and the degree to which each step integrates into the overall cell process sequence. Therefore, it is necessary as a part of this program to evaluate each component of the sequence that has proven effective at increasing cell efficiency to determine the most cost effective cell process sequence. Specific areas being evaluated include:

- Optical Coupling
  - double layer AR coating
  - mechanical texturing
  - porous silicon etching
- Passivation/Gettering
  - hydrogen passivation
  - phosphorous gettering
- Back Surface Field (BSF) Formation
  - Al paste BSF
  - back surface diffusion
- Interaction of metallization with emitter
  - screen printed Ag paste
  - plated buried contact system

The goal of the Task 8 cell effort is to increase average cell efficiency (as obtained from a production line, not just from the laboratory) to 15% as measured at STC (Standard Test Conditions - 1000 W/m^2, AM1.5, 25° C). This must be achieved with a process sequence that lowers the module $/Watt manufacturing cost.

Solarex has a first generation automation system in use at the Frederick facility for tabbing, matrixing and lay-up of the PV modules. This system has been highly successful at reducing manual labor in the assembly process. During Task 4 the present system was evaluated to determine how this system could be modified to increase production throughput, yield and process control and to minimize production labor and cost. To assist with this effort, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington is serving as a subcontractor. ARRI has assisted Solarex in analysis, modeling and development of handling concepts to improve the operation of the module assembly area. In Task 9 the assembly area is being modified as modeled.

Solarex modules use low iron tempered glass as a superstrate and Ethylene Vinyl Acetate (EVA) as the encapsulation system. No change is proposed in this encapsulation system to maintain the module reliability. However, a reduction in the cost of the backsheet was achieved during Task 5 without negatively impacting the module reliability.

Today most PV modules are sold with a frame to provide means for mounting the module and a junction box for electrical connection. This frame is the largest single contributor to module cost. In large systems, the support provided by the system structure is adequate making the module frame redundant. Eliminating this frame can reduce the module selling price by more than

$0.50/Watt. During Task 10, testing of a candidate frameless module mounting schemes was completed and utilized in a large scale system at SMUD.

Similarly, the junction box adds appreciable cost to the module, while requiring additional labor for system assembly. In Task 10, a simpler electrical termination scheme costing less than $1.00 per module was tested and qualified for use.

Task 5 also included the design of a 122 watt module using 36- 15 cm by 15 cm solar cells. Task 10 includes qualification of the design through accelerated environmental tests (CEC-503, IEC-1215, UL 1703, and IEEE-1262) and design of the automated equipment necessary to finish the module.

An important issue for many crystalline silicon PV manufacturers is the ability to handle thinner and larger wafers through the production line. Task 11 and 17 will address this issue. Once again, Solarex is supported in this effort by ARRI, whose background and experience is ideally matched to the task of developing handling methods for parts such as the large thin wafers to be used in this program. ARRI has perform detailed analysis and modeling of the requirements for thin wafer handling. Prototype stations will be built to evaluate various approaches to handling such wafers. Once the concepts have been verified at ARRI, Solarex will design and have built a production unit to verify its capability.

The results of this program will be the modification of today's polycrystalline production facility to:

- Increase production capacity by a factor of three
- Reduce the "profitable" selling price from over $4.00 per peak watt to less than $2.00 per peak watt.

Solarex plans to continue an aggressive market development program that would support the increased capacity obtained as a result of this program.

2.0 PRESENT PROCESS AND PRODUCTS

Solarex's Crystalline Silicon Technology is based on use of cast polycrystalline silicon wafers. The process flow is shown in Table 1. The primary product is a module with 36 solar cells each 11.4 cm x 11.4 cm, that produces 60 or 64 Watts under Standard Test Conditions (STC).

Table 1
Cast Polycrystalline Si Process Sequence

Casting

ID Wafering

Cell Process
(Thick Film Print)

Module Assembly

Lamination

Finishing

The various segments of Solarex's module manufacturing process as practiced at the beginning of this PVMaT program are described below.

Casting

Solarex has developed and patented a directional solidification casting process specifically designed for photovoltaics[1]. In this process, silicon feedstock is melted in a ceramic crucible and solidified into a large grained semicrystalline silicon ingot. In house manufacture of low cost, high purity ceramics is a key to the low cost fabrication of Solarex semicrystalline wafers[2].

The casting process is performed in Solarex designed casting stations. The casting operation is computer controlled. There are no moving parts (except for the loading and unloading) so the growth process proceeds with virtually no operator intervention.

Wafering

Wafering is done with Internal Diameter (ID) saws. These are the same saws that are used in the semiconductor industry to wafer single crystal CZ ingots. At present ID saws are the lowest variable cost wafering option. Solarex has many years of experience with these saws, resulting in low labor and process costs. This is a mature technology with little opportunity for significant increases in productivity or reduction in kerf loss.

Cell Process

The cell process sequence is based on the use of Thick Film Paste (TFP) metallization, where a commercially available screen printed silver paste is applied as the current carrying grid on the front of the solar cell. This process has been designed to be as cost effective as possible. The high temperature process steps including diffusion, firing of the front print paste and Chemical Vapor Deposition (CVD) of a TiO_2 antireflective (AR) coating are all performed in belt furnaces.

Polycrystalline cells processed through this line have an average cell efficiency of 12.5 to 13% at STC. There are many modifications to this process sequence that will increase cell efficiencies. However, many of these modifications would actually increase the total dollar per watt module cost rather than decrease it. Detailed cost analyses indicate what changes in cell processing can lead to both higher cell efficiencies and lower dollar per watt module cost.[3,4] Implementation of these changes require laboratory verification of the candidate process sequences as well as improvement in the accuracy of the input cost data.

Module Assembly

The first part of the module assembly sequence is to solder two solder plated copper tabs onto the front of the solar cells. Each tab is soldered in 4 places for reliability and redundancy. Solarex uses automated machines to perform the tabbing. Tabbed cells are then laid up into a 36 cell matrix by a robot. The tabs are then soldered to the backs of the solar cells by another robot. Each tab has 2 back solder joints.

Module Lamination

The module construction consists of a low iron, tempered glass superstrate, EVA encapsulant and a 3 part Polyethylene-Mylar-Tedlar backsheet. The lamination process, including the cure, is performed in a vacuum lamination system. Then the modules are trimmed and the leads are attached. Finally, every module is flash tested to determine its STC power output.

Finishing

Most modules are sold with a frame to protect the edges and provide a means of mounting. Solarex uses an extruded aluminum frame that is attached both with a butyl rubber adhesive between frame and glass as well as with 2 screws in each corner of the frame. The framing process is performed by an automatic, robotic framing system.

Most modules are also sold with a junction box to protect the output wiring and provide the terminals for electrically connecting the module to the balance of the system. The area where the lead wires are attached to the module is potted to protect the laminate from moisture incursion. The junction box is then attached to the module with adhesive to seal it to the back of the laminate.

3.0 PVMaT PROGRAM EFFORTS

The following sections detail the progress made during the period from January through June, 1995.

3.1 TASK 6 - POLYCRYSTALLINE SILICON CASTING IMPROVEMENTS

The goal of the casting task is to develop the ability to cast ingots that yield four - 15 cm by 15 cm bricks with at least equivalent material quality as now achieved when casting four - 11.4 cm by 11.4 cm bricks. During the first year of the program, Solarex designed and fabricated new larger ceramic pieces, designed and implemented modifications to a casting station and designed and implemented modifications to the sizing saws in order to be able to cast and size larger ingots.

During this reporting period efforts turned to casting full size ingots to yield 4 x 15 cm by 15 cm bricks. The first several large ingots had well-behaved runs, but had cracks extending upward from the bottom. An 11.4 cm by 11.4 cm brick was cut from one of these ingots, and then wafered and processed into cells. The cell efficiency from this brick was significantly lower than normal, with the average cell efficiency for this brick being approximately 90% of a standard production brick. A number of modifications to the insulation package and to the casting program were attempted, but none was able to eliminate the bottom cracking.

Analysis of the crystal growth and modeling of the casting process indicated that a larger separation between the bottom heater enclosure and the lower can was required. This change was made and the insulation configuration and process program optimized on standard sized ingots. We verified that this configuration could produce equivalent material by casting and processing 9 standard size ingots. There was no statistical difference in yield or efficiency between these 9 ingots and the overall production line average during that time period.

Using this configuration full size ingots for 4 x 15 cm by 15 cm bricks were cast. The first two ingots were successfully cast and sized without appreciable cracking. Sample 15 cm by 15 cm bricks and all of the wafers cut from one of these bricks on the wire saw have been delivered to NREL. Figure 1 shows the increase in wafer size achieved by this process. The picture shows a 10 cm by 10 cm wafer, an 11.4 cm by 11.4 cm wafer, the new 15 cm by 15 cm wafer and a baseball for perspective.

Most of Solarex's products are still based on the use of 11.4 cm by 11.4 cm solar cells, so an effort is underway to develop casting of ingots large enough to produce 9 x 11.4 cm by 11.4 cm bricks. Such an ingot requires approximately 20% more silicon than the PVMaT ingot. The initial efforts to cast these "mongo" ingots required changes in the insulation and receiver, but utilized the same pour crucible. We were able to load the added charge of silicon feedstock into the PVMaT crucible and successfully pour and freeze out the larger mongo ingot. Figure 2 shows the comparison of a standard Solarex ingot (4 x 11.4 cm by 11.4 cm bricks) next to a new mongo ingot (9 x 11.4 cm by 11.4 cm bricks).

Efforts are now underway to optimize the process for casting these larger ingots. Solarex is planning to increase casting capacity by modifying all of the casting stations to produce the larger ingots.

Figure 1
Wafer Size Comparison
(10 x 10, 11.4 x 11.4 and 15 x 15)

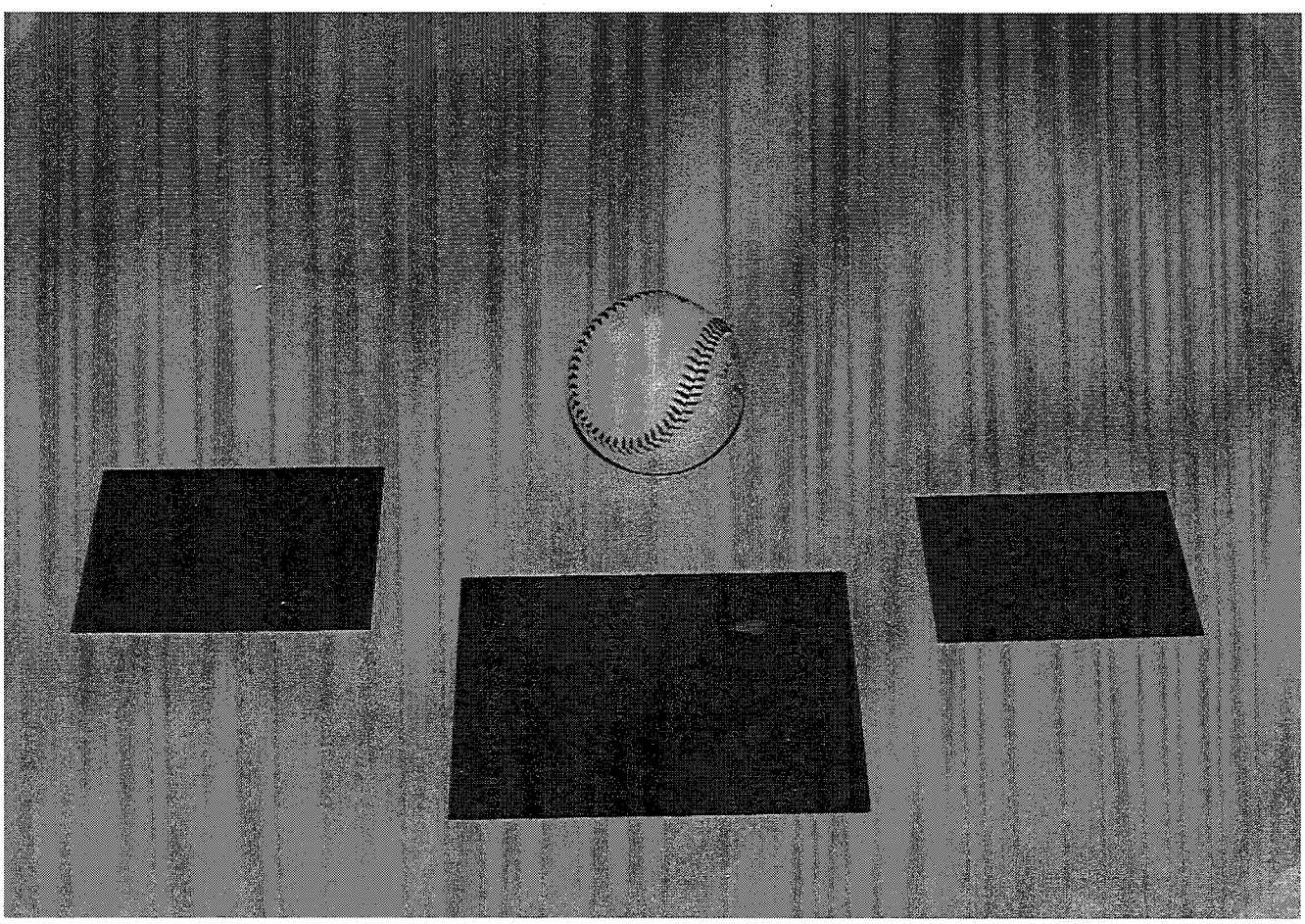
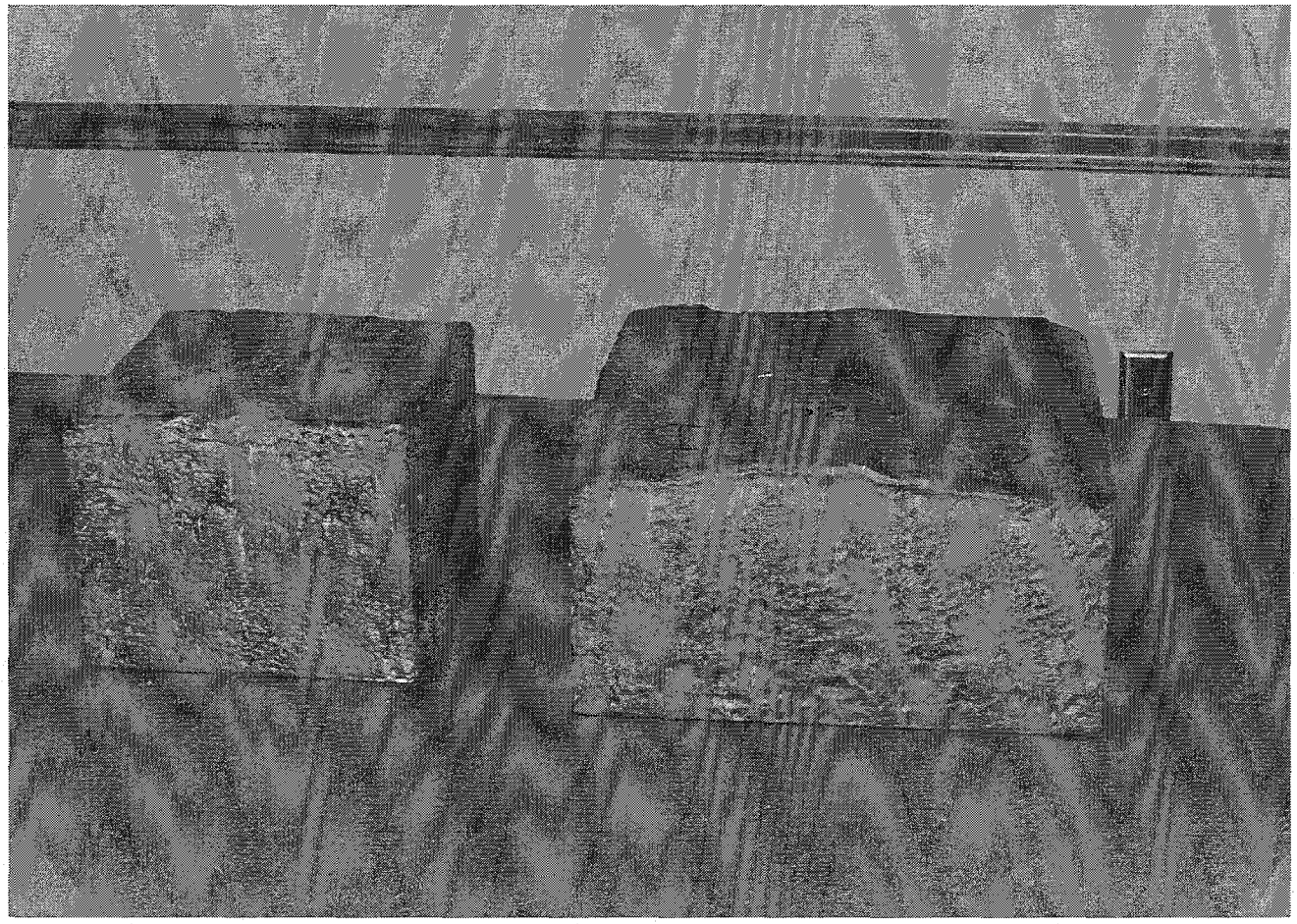


Figure 2
Ingot Size Comparison
(4 bricks and 9 bricks)



3.2 TASK 7 - WIRE SAW IMPROVEMENTS

The goal of this task is to develop the wire saw technology for cutting 15 cm by 15 cm polycrystalline wafers on 400 μm centers at lower cost per cut than achieved today on the ID saws. This represents a 50% increase in the useable silicon obtained from each cast and a 50% increase in the yield of wafers per purchased kilogram of Si feedstock.

3.2.1 Wire Saw Operations

The first step in this effort was to select and procure a wire saw. Solarex selected and purchased an HCT wire saw[4]. The HCT wire saw has been operational since July, 1994. The saw has performed well once start-up problems were solved with the help of HCT staff. During the first year of the program the saw was used to successfully demonstrate the ability to cut 11.4 cm by 11.4 cm, 11.4 cm by 15.2 cm and 15 cm by 15 cm wafers on 500 μm and 400 μm centers.

The major efforts during this reporting period were to:

- gain experience operating the saw in a semi-production mode.
- reduce the cost of consumables, spare parts and waste disposal.
- develop improved methods for demounting and cleaning the wafers after they are cut on the wire saw.

Production operators were trained on the saw and then used to operate the saw as a production operation on the off-shifts, while we perform experiments to improve the process and reduce costs during the day shift. For the 6 month period from January 1, 1995 to June 30, 1995 we processed 459,000 wafers at 94.1% overall yield. Much of the yield loss comes from aborts, where all of the bricks being cut are completely lost. Some of the reasons for aborts are:

1. lack of adequate operator training.
2. power outages, particularly due to thunderstorms.
3. use of experimental wire, grit, oil, etc.
4. problems with the vacuum clamping that holds the bricks in the machine.
5. occasional failure of parts on the saw.
6. failure of the glue joint between the glass plate and the aluminum base.

Most of these causes of aborted runs are avoidable. Better control of training and improved specification of the process can reduce the losses due to items 1 and 6. Development of a back-up power supply for short term power outages is required to eliminate aborts due to item 2. HCT has developed a new clamping system from pneumatic to hydraulic. We are planning to retrofit our saw with the new clamping system to eliminate this maintenance problem.

Cost saving efforts during the reporting period include:

1. Qualified a new oil that costs 32% less than the original oil. This change alone reduces the wafer cost by several cents.

2. Identified and qualified a new vendor of pulleys. The new pulley cost about one-third of what the saw vendor charged for the original pulleys.
3. Identified and qualified grit from several vendors. Negotiated a long term contract to save $0.25 per pound of grit.
4. Found someone who can recycle our waste slurry and in doing so reduced our cost to dispose of the waste by 90%.

3.2.2 Demounting and Cleaning

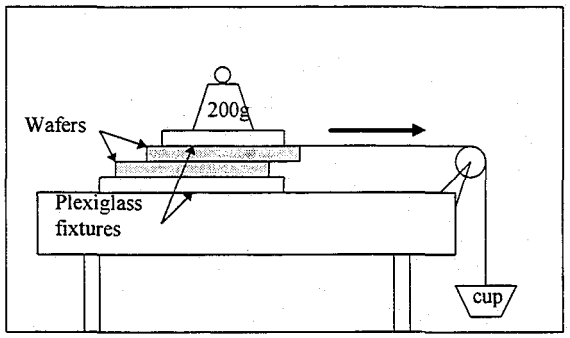
After wafers have been cut on the wire saw they must be removed from the hold down plate, placed in cassettes and cleaned. Today this process is done manually. An automated process is necessary to reduce cost and increase yield especially as the volume of wire saw wafers increases and the thickness of the wafers decreases. As a first step to better understand what is involved in removing wet wafers from a stack, ARRI performed a series of tests to evaluate the difficulty of separating wafers. They observed that the surface tension between wafers and liquid, be it slurry, cleaner or water, was very strong.

A set of experiments was then performed to gain a *quantitative* understanding of the forces involved in wafer separation under both dry and wet conditions. This information will be directly usable in the design of equipment to automate the wafer demounting process. A battery of six tests was run on each of six wafer samples. A sample consists of a pair of wafers, each mounted on a square Plexiglas surface by means of double-sided adhesive tape. The Plexiglas fixtures are used to hold the first (bottom) wafer stationary and to pull the second (top) wafer in the horizontal and vertical directions. The six test conditions are described below.

Test Condition 1: Dynamic friction coefficient, dry wafer

With the bottom wafer fixed, a 200-gram weight is placed on the top wafer. The entire top wafer assembly, including weight and fixture, is weighed. A string and pulley arrangement with a cup at the free end imparts a horizontal force on the top wafer. The cup is slowly filled with water until the top wafer begins to slide at a constant rate; cup and water are then weighed. The set-up for measuring the dynamic friction coefficient is shown in Figure 3.

Figure 3
Test Set-up for Measuring the Dynamic Friction Coefficient



Test Condition 2: Dynamic friction coefficient, semi-wet wafer

This is performed in the exact same manner as test condition 1, with the following exception: tap water in the amount of 0.1 cm^3 is dispensed at the center of the bottom wafer with a syringe, then the second wafer is laid on top and moved in a circular fashion so as to "spread" the water over the entire surface.

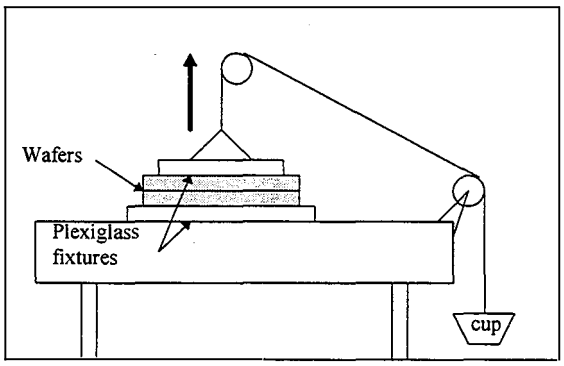
Test Condition 3: Dynamic friction coefficient, wet wafer

This is performed in the exact same manner as test condition 2, using 2 cm^3 of water instead of 0.1 cm^3. Unlike test condition 2, water will issue out of the wafer edges since 2 cm^3 is more than the surfaces can contain under the 200 gram weight. This provides the maximum water layer thickness that the wafers can withhold under the given load.

Test Condition 4: Normal separation force, dry wafer

The bottom wafer is fixed and the second wafer is laid on top. A string and pulley arrangement with a cup at the free end imparts a vertical (normal) separating force on the top wafer. The cup is slowly filled with water until the wafers become completely separated. The set-up for measuring the normal separation force is shown in Figure 4.

Figure 4
Test Set-up for Measuring the Normal Separation Force



Test Condition 5: Normal separation force, semi-wet wafer

This is performed in the exact same manner as test condition 4, with the following exception: tap water in the amount of 0.1 cm^3 is dispensed at the center of the bottom wafer with a syringe, then the second wafer is laid on top and moved in a circular fashion so as to "spread" the water over the entire surface. Because large forces at the interface between the wafers develop when water is present, a larger capacity container is used instead of a cup to provide the upward pull on the top wafer.

Test Condition 6: Normal separation force, wet wafer

This is performed in the exact same manner as test condition 5, using 2 cm^3 of water and spreading it with a 200 gram weight on the top wafer (the weight is removed prior to running the test).

The experimental data and computed values for the dynamic friction coefficient tests are given in Table 2. Coefficients are calculated by the ratio of sliding pull weight to top assembly weight. All weights (masses) are in grams.

Table 2
Dynamic Friction Coefficients

#	Top asm weight	Test 1 Dry sliding weight	Test 2 Semi-wet sliding weight	Test 3 Wet sliding weight	Dry sliding frict. coefficient	Semi-wet sliding frict. coefficient	Wet sliding frict. coefficient
1	202	111	2149	219	0.55	10.6	1.1
2	203	104	2053	208	0.51	10.1	1.0
3	204	102	2041	171	0.50	10.0	0.8
4	204	118	2589	105	0.58	12.7	0.6
5	206	114	2257	159	0.55	11.0	0.8
6	207	126	1976	208	0.61	9.5	1.0
avg	-	-	-	-	0.55	10.7	0.9

Theoretically, the static friction coefficient is higher than the dynamic friction coefficient and it is therefore of greater interest as a design parameter. In this experiment we report the latter, and then only as an *approximation*, since the slight warpage of the wafers prevented a completely clean breakaway of the top wafer past a certain horizontal force value. The recorded "sliding weight" value is the minimum amount of water that causes the top wafer to be displaced at a constant rate.

The experimental data for the normal separation force tests is given in Table 3. The wafer sample numbers do not correspond to those of the dynamic friction coefficient tests (wafers were not paired the same way). All weights (masses) are in grams.

Table 3
Normal Separation Force

#	Test 4 Dry separation weight	Test 5 Semi-wet separation weight	Test 6 Wet separation weight
1	7	2274	>5700
2	3	2018	>5700
3	12	2381	5101
4	16	1907	>5700
5	7	1864	>5700
6	6	1369	5573
avg	9	1969	>5700

Under dry conditions, the sliding friction between wafers is easily overcome without breakage. Similarly, normal separation forces amount to little more than the weight of the wafer itself, indicating that no significant binding forces develop at the interface.

The presence of water between the wafers, however, increases dramatically the sliding as well as normal forces required for separation. This can be explained by the presence of three additional effects:

- Surface tension within the water layer.
- Surface tension at the interface between the water and the wafer surface.
- Vacuum generated between the wafers due to air being displaced by water.

In the sliding tests, the separation force is greatest under semi-wet conditions. Under the presumption that surface tension effects are much stronger at the water-wafer interface than within the water itself, we may justify this result by noting that in the semi-wet condition the water layer is very thin, and consequently the majority of the separation occurs at the water-wafer interface. Conversely, when the water layer is thick, the separation occurs mostly within the water, requiring a smaller force.

Normal separation pull forces, however, are strongest under a fully wet condition. It is likely that vacuum effects are dominant, and that a fully wet condition is most effective in displacing air between the wafers. This appears consistent with the principle behind suction cups, and why they work better when slightly wetted. The pull forces required to separate semi-wet and wet wafers are well within the breakage-causing range, as happened with several of the samples tested (chipped corners).

These results indicate that it would be best to dry the wafers before destacking. However, the present cleaning solvent dries slowly. When we began evaluating the use of a solvent that would dry more quickly, we realized that evaporating slowly is an important feature of the solvent, since it raises the flash point and minimizes the release of organics into the air. Therefore, use of a more rapidly drying cleaning solvent is not recommended.

ARRI then proceeded to develop a number of concepts for equipment to destack wafers. Two of the ideas have been selected to build and test prototypes.

3.3 TASK 8 - HIGH EFFICIENCY CELL DEVELOPMENT

The goal of this task is to increase cell efficiencies to 15%, while decreasing the cost per watt at the module level. While a number of approaches to achieving high efficiency have been reported, many of these utilize processes and material that are not likely to be cost effective when applied to cast polycrystalline silicon in a manufacturing environment. The key to achieving the goal of this task is to select modifications to the present process that increase efficiency while lowering the cost per watt. That is, the increased cost of the process is less than the value of the increased power produced by the improvement.[5] During the period cover by this report, the major cell task efforts were in the areas of back surface fields (BSF), hydrogen passivation, phosphorous gettering and mechanical texturing. Each of these areas is discussed below:

3.3.1 Back Surface Field Formation

In the last Annual Report[6] it was reported that an aluminum paste back surface field (BSF) could be used to cost effectively increase cell efficiency by approximately 5%. During this reporting period program efforts included working with vendors to establish a usable paste product, continued process development to select the lowest cost option for implementation and finally initiation of efforts to environmentally qualify cells made with the Al paste in a module package.

In attempting to scale from small laboratory batches of paste to mid-size pilot scale batches, there was a problem with the ability to easily print the Al paste. Several batches were formulated for us by Ferro Corporation that produced similar electrical performance, but were very difficult to screen print. Ferro worked with us to optimize the formulation in terms of ease of printing. Once the process had been optimized for small laboratory batches, Ferro produced an 18 kg batch of paste for manufacturing trials. This paste printed easily, fired to a flat and bead-free surface and performed electrically as expected, matching the performance of the laboratory batch material as shown in Table 4. The production batch of paste will now be used in production trials and the resultant cells made into modules for environmental qualification to IEC 1215 and IEEE 1262.

Table 4
Laboratory Sample versus Production Lot of Al Back Paste

Sample	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Backspray	12.47	3.787	571.7	74.8
Lab Al Paste	13.39	4.034	583.6	73.9
Prod Al Paste	13.42	4.037	583.9	74.0

Another issue with production manufacture of Al back paste is the availability of the specified Al powder. To provide Ferro with more flexibility, a second source of Al powder was qualified for use in the paste. Ferro was able to format a second powder into a paste that printed and fired well. Table 5 shows that the second source Al powder provided equivalent electrical performance.

Table 5
Evaluation of Al Powder Source in Back Paste

Sample	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Backspray	12.65	3.85	574.2	74.3
Standard Al	13.41	4.066	583.4	73.5
Second Source Al	13.42	4.067	583.6	73.5

The lowest cost BSF process is the one that uses the least amount of Al paste while still providing equivalent electrical and mechanical results. The amount of paste applied to each 11.4 cm by 11.4 cm cell was varied from 0.9 grams up to 1.5 grams. All of the samples produced equivalent electrical results. However, samples with less than 1.4 grams of Al paste resulted in some bead formation on the back. Since bead formation results in yield loss during subsequent processing, the lower limit on paste application has been set at 1.4 grams.

In the initial development the back surface field was added to the standard cell process that included Solarex's patented backspray process[7]. The backspray process is ideally suited as a back contact when no BSF is used. However, with the added conductivity of the Al from the BSF paste, the added conductivity of the backspray may not be required. It may be more cost effective to replace backspray with a screen printed Ag-Al paste on the back. Table 6 compares BSF cells with backspray versus BSF cells with screen printed Ag-Al back contacts. The screen printed group matched the efficiency achieved with back spray.

Table 6
Backspray versus Back Print over BSF

	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Backspray	13.2	3.988	579.3	74.2
Back Print	13.26	3.985	581.8	74.3

3.3.2 Hydrogen Passivation

Rohatgi[8] reported on the use of a forming gas anneal to increase cell efficiency of several types of polycrystalline silicon substrates. We previously reported on the use of forming gas anneals at 400° C for 1 and 2 hours. Cells with and without Al paste BSF were annealed in forming gas both before and after the front metallization was printed and fired. Cells forming gas annealed after the front metallization was fired, exhibited no measurable improvement in short circuit current and the fill factor got progressively worse as the length of the anneal increased. For cells forming gas annealed before front metallization, there was no major degradation of fill factor and possibly a small (~1%) increase in short circuit current.

Experiments during this reporting period were designed to investigate the use of a forming gas anneal at higher temperatures. Since these high temperatures would certainly damage the screen printed metallization, all anneals were done before the front metallization was applied. The results for 600° C anneals are given in Table 7 and the results for 700° C anneals are given in Table 8. The samples processed for 1 hour at 700° C had a 1% enhancement in short circuit current.

Table 7
Forming Gas Anneal at 600° C

Anneal Time	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
None	13.46	4.092	586.5	72.8
1 hour	13.47	4.088	586.4	73.0
2 hours	13.22	4.042	584.9	72.7

Table 8
Forming Gas Anneal at 700° C

Anneal Time	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
None	13.22	4.098	582.1	72.0
1/2 hour	12.97	4.092	582.5	70.0
1 hour	13.30	4.142	583.8	71.5

With Solarex cast polycrystalline silicon we are not seeing the large improvements in performance that have been reported when treating other polycrystalline silicon substrates with forming gas anneals. The degree of improvements that we have seen, approximately 1% for the best case, is not enough improvement to justify adding a forming gas anneal to the cell process. Efforts in this area have been terminated.

3.3.3 Phosphorous Gettering

There have been a number of reports on the use of phosphorous gettering to improve the efficiency of solar cells, particularly on polycrystalline material[9,10]. The most compelling results to date were those published by James Gee[11]. For Solarex material he found a large increase in minority carrier lifetime after gettering, that was degraded by subsequent process heat treatments. This suggests the use of a process that minimizes heating after the gettering step. To evaluate this approach we designed a set of experiments to evaluate gettering at the optimum time and temperature reported in the Sandia work, looking at a variety of process variables. In several groups, the combination of back surface field and gettering lead to increases of short circuit current between 7 and 12%, considerably more than observed with back surface fields alone.

The second set of phosphorous gettering experiments utilized a back surface field control group. Table 9 gives the results of the control group and two of the experimental gettered groups, where the gettered region has been etched off and the cell is rediffused to form the emitter. Once again there is a small but measurable increase in short circuit current and efficiency from the phosphorous gettering step. This level of improvement is not large enough to justify adding a phosphorous gettering and etch-off process steps. However, if a phosphorous gettering step can be built into an integrated process sequence without requiring an etch-off process, it is likely to be cost effective. This will be discussed further in section 3.3.5.

Table 9
Phosphorous Gettering

Sample	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Control	13.28	3.981	590	73.5
Gettered #1	13.4	4.037	590	73.2
Gettered #2	13.39	4.015	592	73.2

3.3.4 Mechanical Texturing

An improved method for evaluating the performance of an optical coupling surface in terms of its performance on solar cells has been developed in this program[12]. The model predicted that chemical and mechanical texturing would increase the short circuit current and maximum power of encapsulated solar cells by approximately 3% over planar cells made on the same material with the same cell process[6]. To verify the model, matched polycrystalline wafers were processed with and without mechanical texturing. The matched cells were measured, encapsulated and remeasured. The results are given in Table 10. Mechanical texturing resulted in a 2.4 to 3.3% gain in encapsulated cell efficiency, consistent with the 3% predicted by the model using reflectance measurements.

Table 10
Mechanical Texturing versus Planar Controls

Cell	Structure	Unencapsulated		Encapsulated	
		Efficiency (%)	Isc (A)	Efficiency (%)	Isc (A)
107	Planar	12.7	3.857	13.02	3.964
207	Mech Tex	13.24	3.995	13.38	4.041
% Difference		3.8%	3.6%	2.4%	2.0%
108	Planar	12.81	3.856	12.89	3.948
208	Mech Tex	13.14	3.980	13.32	4.045
% Difference		2.6%	3.2%	3.3%	2.5%

A mechanical texturing tool has now been designed that can texture an entire 11.4 cm by 11.4 cm solar cell in a single pass. A prototype of the production tool has now been fabricated. Trials with this tool will begin soon.

3.3.5 Integrated Cell Sequence

Both mechanical texturing and phosphorous gettering result in increased cell efficiencies. To utilize these technologies, they must be incorporated into a cost effective integrated cell process sequence. To begin development of the integrated sequence, a set of experiments was conducted to evaluate the impact of combining gettering, oxide masking, mechanical texturing and oxide passivation. For simplicity in this experiment a back surface field was not incorporated in the process and a non-optimized grid pattern was used, resulting in lower than normal fill factors. The results are given in Table 11. There is a significant improvement over the controls. The next set of experiments will use an optimized grid pattern and a back surface field, along with the best case parameters from this experiment.

Table 11
Integrated Cell Sequence Experiment #1

Sample	Efficiency (%)	Isc (A)	Voc (mV)	FF (%)
Control	12.66	3.954	587	70.8
Gettered,Oxide mask, Mech Tex, Oxide Pass	13.09	4.158	589	69.5
Gettered, Oxide mask, Mech Tex	12.99	4.091	588	70.2
Gettered, Mech Tex	13.09	4.087	587	70.9

3.4 TASK 9 - AUTOMATED MODULE ASSEMBLY

The goal of this task is to modify Solarex's present automated matrix and module lay-up system to increase throughput by 100% and decrease the labor requirement by 50%. To assist Solarex in analyzing how this equipment can be improved to increase capacity and reduce labor, the Automation and Robotics Research Institute (ARRI) at the University of Texas at Arlington is serving as a subcontractor.

3.4.1 Modeling and Expansion

The first step in this task was the development of a process flow chart detailing all of the module assembly steps. ARRI used this information to model and analyze the manufacturing process. As a short term goal they identify the changes necessary to increase production capacity by 40% to meet Solarex's short term business plan. These changes were successfully implemented during the first year of the contract[6].

The second phase of the program was designed to meet the PVMaT contract goal of increasing capacity by a factor of 100% from the original 1993 baseline capacity. ARRI developed two Factory of the Future concepts to meet this requirement. They used AT&T's discrete event simulation package called Witness to evaluate each scenario. The Witness software is capable of modeling resource interactions in detail and providing an accurate representation of the factory using statistical analysis. The Witness software was used to analyze the two Factory of the Future concepts.

For Concept 1 Witness predicts an increase in production capacity of 58% over the present "As-Is" system or 120% increase over the PVMaT baseline. Labor utilization analysis indicates that Concept 1 requires no more labor than the baseline case, thereby reducing the labor content per module (or per watt) to 45% of the baseline.

For Concept 2 Witness predicts an increase in production capacity of 75% over the present "As-Is" system or 146% increase over the PVMaT baseline. Labor utilization analysis indicates that Concept 2 requires one less operator than the baseline case, thereby reducing the labor content per module (or per watt) to 37% of the baseline.

While the two proposed concepts could meet the PVMaT goals they could not meet Solarex's publicly announced polycrystalline expansion program designed to triple capacity by 1999. To meet this expanded capacity requirement, Solarex and ARRI developed a new factory concept that would allow for incremental increases to meet the shorter term capacity requirements and would ultimately result in the required tripling of module assembly capacity. The plan is based on replacing the back solder robots with XY positioners to increase the number of solder bonds made at one time from 2 to 4, thereby increasing the through-put by nearly a factor of two.

ARRI then used the Witness program to model the module assembly operation. As the volume of product is ramped up, various pieces of equipment will reach maximum throughput capacity. This analysis then became the basic for determining when capital investment must be made to increase the equipment base to meet the project volume. The following areas were identified as requiring increased capacity within the next year.

1. Tabbing Systems - Solarex has already begun the process of identifying and procuring an additional tabbing system.
2. Module Lay-up System - Modifications to the system are required to reduce the cycle time to handle the increased output of the XY positioners. ARRI is assisting Solarex in the development of an improved method for dispensing the EVA sheet.
3. Laminator Capacity - Solarex already procured, installed and is using a new Spire laminator to increase the lamination capacity.
4. Framing System - The cycle time of the framing system is too long to meet the framing requirements. ARRI is assisting in redesign of the system to reduce cycle time by 50%.

3.4.2 Spire Assembly System

Spire Corporation of Bedford, Massachusetts has a PVMaT contract to develop automated high throughput equipment for interconnecting large area solar cells[13]. To evaluate the Spire equipment and process, standard Solarex 11.4 cm by 11.4 cm polycrystalline solar cells were shipped to Spire. Spire first tabbed the cells, making four solder bonds on each of the two front side tabs. They then made strings of 9 cells each for incorporation into Solarex MSX-60 modules. Enough strings were produced to make 3 MSX-60 type modules with one additional string available for pull tests. The results of module performance is given in Table 12. All three of the modules made from Spire strings had normal electrical output.

Table 12
Modules Made from Spire Strings

Module	Isc (A)	Voc (V)	FF (%)	Pmax (W)
Spire 1	3.86	21.3	73.9	60.9
Spire 2	3.88	21.3	73.6	60.7
Spire 3	3.86	21.3	73.9	60.7
Reference	3.80	21.4	74.0	60.1

These modules were then subjected to accelerated stress tests from IEC 1215 and IEEE 1262 PV Module Qualification Test Sequences. One module successfully completed the UV exposure, 50

thermal cycles plus 10 humidity freeze cycles with a total power loss of 3.5%. The second module successfully completed 400 thermal cycles with a 1.8% power loss. Finally, the third module successfully completed a 1000 hours of damp heat (85/85) with a power loss of 3.1%. These power losses are all less than the 5% loss acceptable in IEC 1215 and the 10% loss acceptable in IEEE 1262. There were no measurable changes observed in visual inspection nor measured in high pot leakage tests.

The only noted problem with the Spire produced strings, was the fact that four out of five cells tested would have failed Solarex's standard criteria for front contact pull strength. Since the pass/fail criteria for pull strength is based on a different process, namely hot bar solder reflow, these results may not have much meaning. If the soldering process can successfully pass the thermal cycle test, it should be acceptable regardless of the measured pull strength.

3.5 TASK 10 - FRAMELESS MODULE DEVELOPMENT

In this task Solarex will develop and qualify a frameless module design incorporating a lower cost back sheet material (less than $0.05/square foot) and user friendly, low cost electrical termination (less than $1.00/module).

3.5.1 Backsheet

A key component in frameless module design is the backsheet, since the electrical termination and the support system itself must adhere to the backsheet. This offered an additional opportunity to reduce cost from the 3 part backsheet being used at Solarex at the start of this PVMaT Program.

Three candidate materials selected for evaluation are:

- Pigmented Chlorinated polyethylene (CPE)
- Affinity polyolefin
- Thin Tedlar - polyvinyl fluoride

Small modules were fabricated using the experimental backsheet materials. These small modules were then subjected to a set of environmental qualification tests similar to IEC 1215 - "Crystalline Silicon Terrestrial Photovoltaic (PV) Modules -Design Qualification and Type Approval", but with the addition of a wet high-pot test. The three materials successfully passed all of the environmental tests and successfully passed in-house simulated UL fire tests.

Each material was exposed directly to a equivalent of 2 years UV in Phoenix, AZ. We estimate that the normal UV exposure of the back sheet is no more than 10% of direct exposure, so this test should represent 20 years of UV on the back of the module. For each material we sent 2 mini-modules to be tested and retained one sample in the laboratory for comparison. The following materials were tested:

- Solarex 3 part backsheet (Polyethylene, Mylar, Tedlar)
- Salem blue Tedlar
- Regal blue Tedlar
- Orange Tedlar
- Gray Tedlar (0.5 mils thick)
- Denim blue Tedlar
- Clear Tedlar (like we use on front of Solarex Lite modules)
- Blue CPE from Springborn
- Dow Affinity Polyolefin
- Bare EVA

Nine of the materials showed no discernible change. There was no cracking or other physical change in the materials nor any fading of colors. They were identical to the control sample. The one exception was the CPE material. Both exposed CPE samples turned a dark black color with evidence of leaching of green pigment from the samples exposed to UV. Based on these results we have dropped CPE as a candidate, but will continue PVMaT work on both the thin Tedlar and the Dow Affinity Polyolefin.

Based on the results of the testing, Solarex has switched to a single sheet Tedlar back sheet in manufacturing.

3.5.2 Electrical Termination

Most commercial modules have junction boxes for electrical termination. While these provide for a great deal of flexibility in use, they are expensive to purchase, probably will not meet the PVMaT cost goals and require significant labor of skilled electrical personnel for field installation. Our initial approach was to use a quick connect-disconnect system that would eliminate most of the field assembly labor. However, we were unable to find such a system that would meet our environmental requirements and cost less than $1.00 per set of male and female connectors. Therefore, we changed our approach and decided to use a quick connect system that doesn't offer quick disconnect. This may actually have some advantages in the field because it will make it more difficult for unauthorized personnel to disconnect modules and such systems are less likely to accidentally become all or partially disconnected.

We have selected a butt crimp connector and SPC Technology type PHS black polyolefin shrink tubing. We have subjected samples of these wire connectors to:

- 1000 hours of damp heat at 85° C and 85% relative humidity with a constant current flow of 8.7 amperes.
- 10 humidity freeze cycles between +85° C and 85% relative humidity and -40° C.
- 400 thermal cycles between +85° C and -40° C.

The connector passed a wet hi-pot test at 2750 volts DC before and after each of the stress tests. The resistance across the connector did not change during the course of the testing.

These connectors are now under test outdoors.

3.5.3 Mounting System

The frameless module mounting system is based on the use of 3M's Very High Bond (VHB) Tape to attach the back of the module directly to galvanized B-Line cross members. The prototype system has now been under test at our Frederick facility for nearly 1 year. The array, especially the tape has held up well to the weather, including high winds during several severe storms. The only noticeable change is some minor corrosion occurring on the cut and machined areas of the galvanized steel cross members. These areas will have to be coated with a cold galvanizing compound to assure corrosion resistance of the entire system.

3.6 TASK 11 - Automated Thin Cell Handling

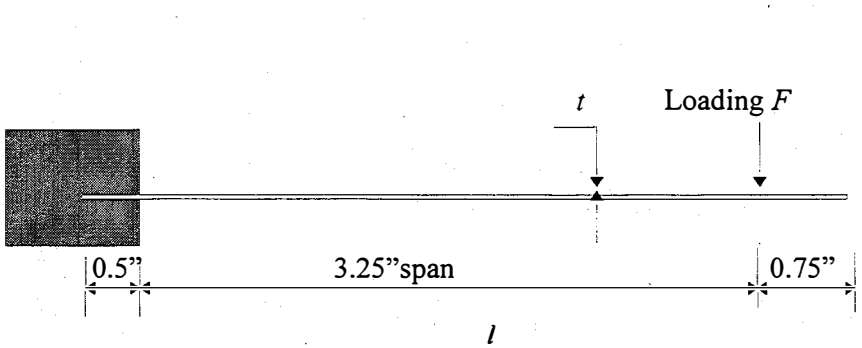
In this task Solarex will develop automated handling equipment for 200 μm thick 15 cm x 15 cm polycrystalline silicon wafers and cells that has high yield (less than 0.1% breakage per process handling step) and can handle at least 12 cells per minute. ARRI is under subcontract to assist Solarex in the development of handling methods and equipment for large thin wafers and cells.

3.6.1 Silicon Wafer Fracture Testing

ARRI begun the effort by determining the stress limits for handling large area wafers and solar cells. The initial analysis is based upon destructive testing of wafers. The amount of weight that must be applied to fracture a wafer can then be used to calculate the maximum stress a polycrystalline silicon wafer will withstand. Two types of tests were devised.

The first test was a cantilever test, where one end of the specimen is held fixed while the free end is loaded in steps until the specimen fractures. The set-up for this test is shown in Figure 5. The weight hanger is placed at a predetermined position of 0.75" from the free end. One end is held firmly to form the fixed end in such a way that the overhang is 3.25" from the fixed end. Weights are added in the weight hanger in steps, until the specimen fractures completely. The load to failure is recorded.

Figure 5
Cantilever Test Set-up



The following calculations are made to determine the ultimate strength in bending:

$$\sigma = M \times \frac{c}{I} \quad \text{Psi}$$

where:

$$M = F \times l \quad \text{lb-in}$$

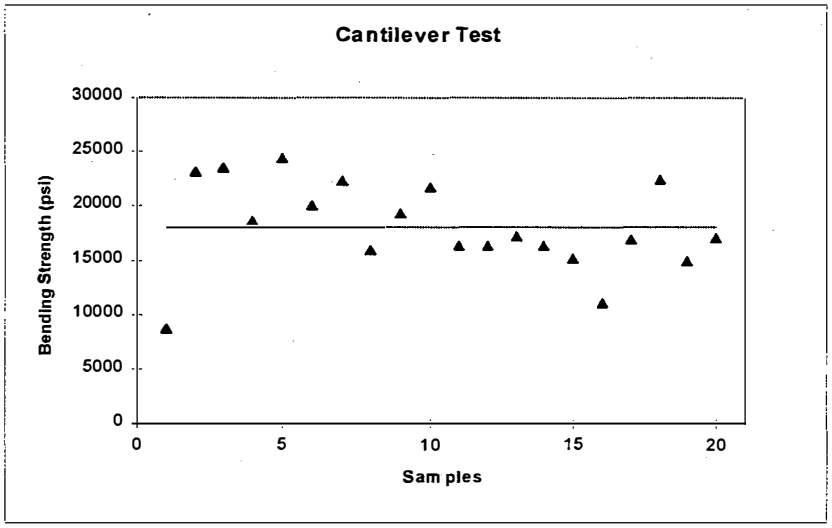
$$c = \frac{t}{2}$$

$$I = \frac{b \times t^3}{12} \qquad b = \text{width of specimen}$$

The above procedure was repeated for 20 samples in order to obtain an average value for the ultimate strength in bending (in Psi). The data for all of the strength values for 20 trials is plotted in Figure 6. The average value for the bending strength is 18,080 Psi.

The second test was a four-point bend test, where the specimen is supported along its length at two points and a distributed load is applied transversely causing the specimen to bend in flexure and ultimately fracture at a certain load. The test structure is shown in Figure 7. The bottom plate B contains 2 pins running the length of the plate, spaced 5.125 cm apart. A test wafer is placed on top of the pins. Plate A with 2 pins running the length of the plate, spaced 2.55 cm apart, is placed on top of the wafer. Weights are added in steps on the center of the top plate A till the specimen fractures. The deflection at each step of load is recorded as well as the final load to fracture. The load to deflection data is used to calculate the ultimate strength in bending as well as the Young's modulus.

Figure 6
Bending Strength of Polycrystalline Silicon Wafer from Cantilever Test



The bending strength is then given by:

$$\sigma = M \times \frac{c}{I} \qquad \text{Psi}$$

$$M = \frac{F}{2} \times a \qquad \text{lb-in}$$

where: F = Applied load and a = 2.575 cms, the distance between top pins on the bottom and top plates respectively. The data is shown in Figure 8. The average value for the bending strength is 18,335 Psi in excellent agreement with the value measured using the cantilever test.

Young's modulus E, can be calculated from the recorded maximum deflection. The maximum deflection which is at the center of the specimen, is given by:

$$Y_{\max} = \frac{M}{24 \times EI}\left(3 \times L^2 - 4 \times a^2\right)$$

The data is shown in Figure 9. The average value of Young's modulus for all of the bending tests was 24.5 Mpsi (169 Gpa) in excellent agreement with the value of 23.56 Mpsi as reported by King[14] for polycrystalline silicon and the value of 27.5 Psi (190 Gpa) as reported by McGuire[15].

3.6.2 Interpretation of Wafer Strength

The scatter in strengths may be modeled using Weibull statistics[16]. The strength of a brittle material is controlled by the presence of randomly distributed defects. Failure is controlled by the largest, most severely stressed defect. Fracture occurs when a defect in one particular element of the body reaches a critical loading. This analysis is also known as the weakest-link model, in direct analogy to the strength of a chain.
The Weibull strength distribution is given by:

$$F = 1 - \exp - \int_V \left(\frac{\sigma - \sigma_u}{\sigma_o}\right)^m dV$$

where F is the probability of failure of a specimen , V is the specimen volume, σ is the maximum tensile stress at any given point , σ_u is the threshold stress (below which no failure will occur), σ_o is the characteristic strength , and m is the Weibull modulus. This distribution is similar to a Gaussian distribution , except that there is a skew to lower strengths.

For the case of a test specimen experiencing a uniform tensile stress the probability of failure is given by:

$$F = 1 - \exp\left[-V\left(\frac{\sigma - \sigma_u}{\sigma_o}\right)^m\right]$$

Figure 7
Four Point Bend Test Set-up

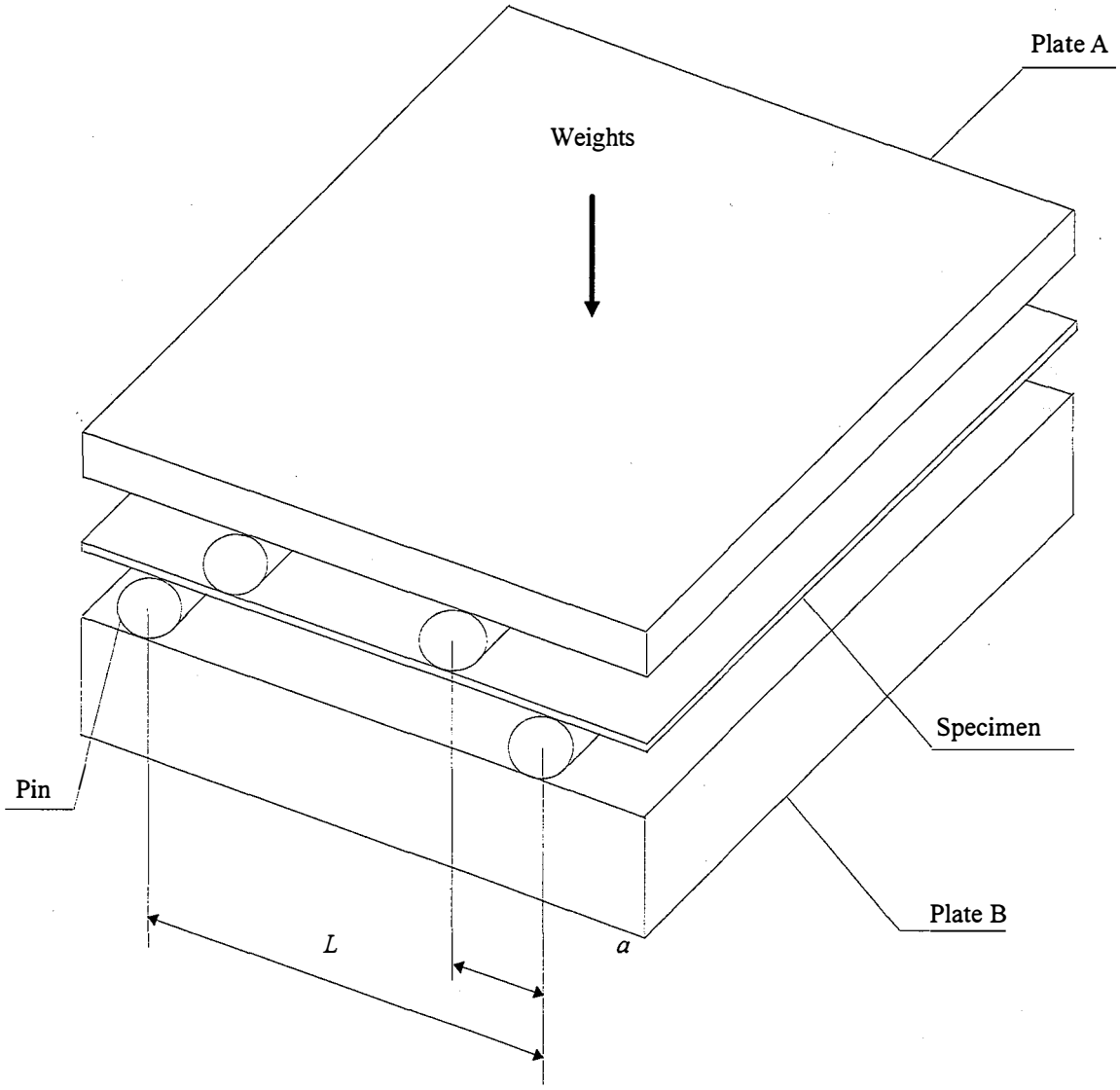


Figure 8
Bending Strength of Polycrystalline Silicon Wafer from Four Point Bending Test

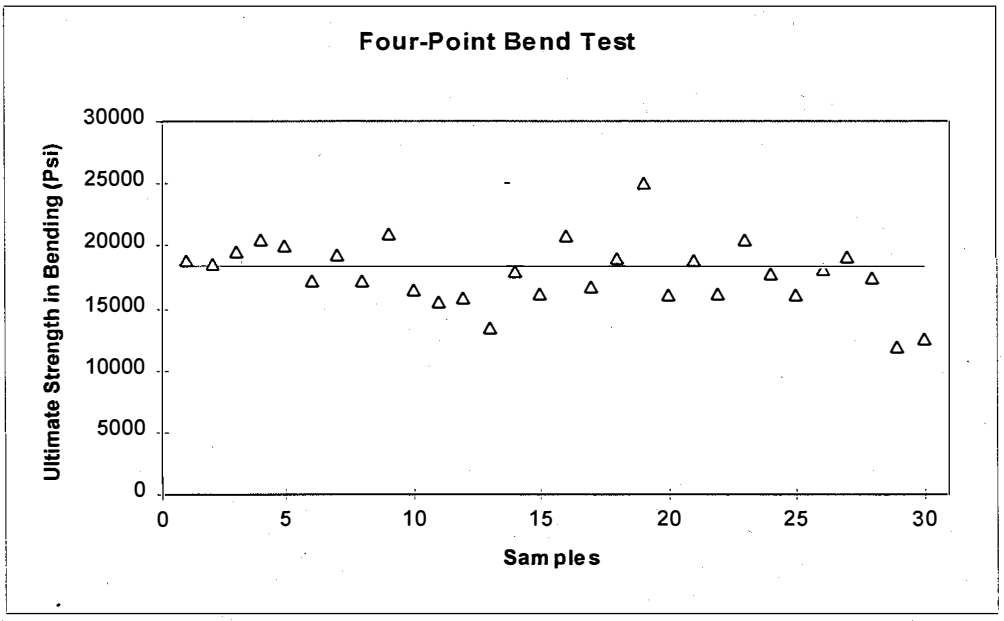
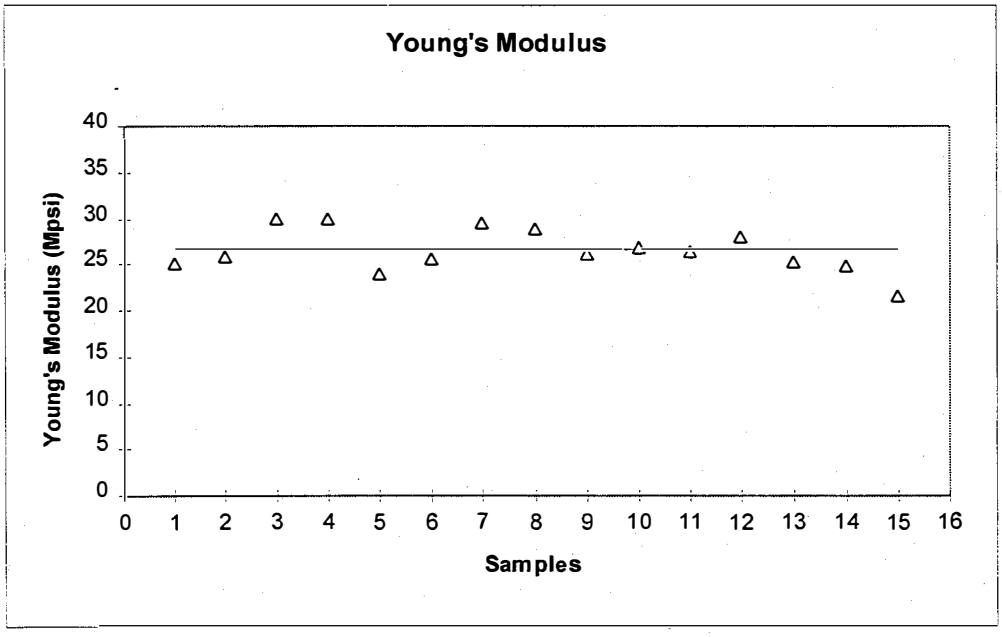


Figure 9
Young's Modulus



A rectangular specimen in four-point bending has an effective volume given by:

$$V_E = \frac{V(m+2)}{4(m+1)^2}$$

Weibull graphs are a convenient means to report strength data. The graph has special axes chosen to linearize the data. Each strength is assigned a probability estimate given by:

$$F = \frac{(i-0.5)}{N}$$

where i is the specimen number, and N is the total number of specimens. This estimator has been shown to have the least bias and lowest scatter[16]. Values of

$$\ln\ln\left[\frac{1}{(1-F)}\right]$$

are then plotted versus $\ln\sigma$ and a least square line is fitted to the data minimizing the scatter. The Weibull modulus is interpreted as the slope of the line on the graph. The characteristic strength of the test specimen is the stress for which the vertical axis has

$$\ln\ln\left[\frac{1}{(1-F)}\right] = 0.$$

The least square analysis places strong emphasis on the low-strength data point.

The plot of Strength Vs Probability of failure shown in Figure 10 can be used to predict the failure of a given polycrystalline silicon wafer in the range of stress. The Weibull graph shown in Figure 11 is used to determine the Weibull modulus and the characteristic strength of the specimen. All the experimental values from the four-point bending tests were used to draw the Weibull graph. The following can be concluded from these results:

- The slope of the line of least squares fit representing the Weibull modulus, is found to be 9.56.
- The characteristic strength σ_o extrapolated from this value of Weibull modulus from the graph is found to be 18,221 Psi for a 63.2% probability of failure.

Figure 10
Weibull Graph
Strength versus Probability of Failure

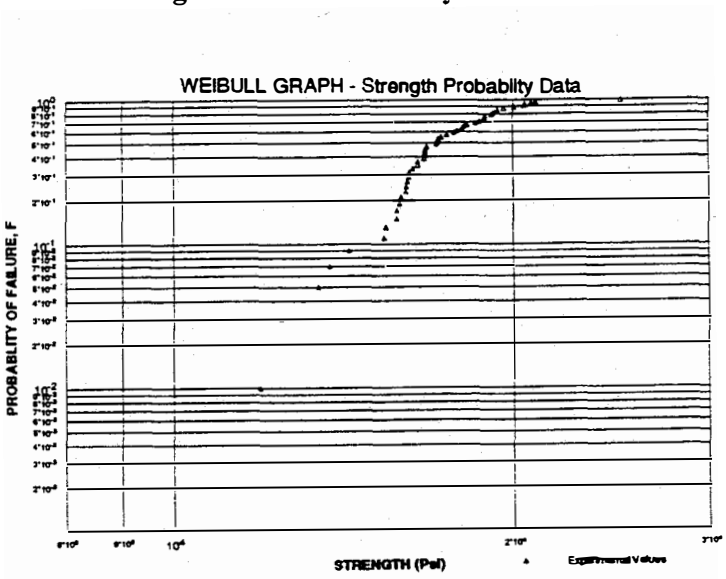
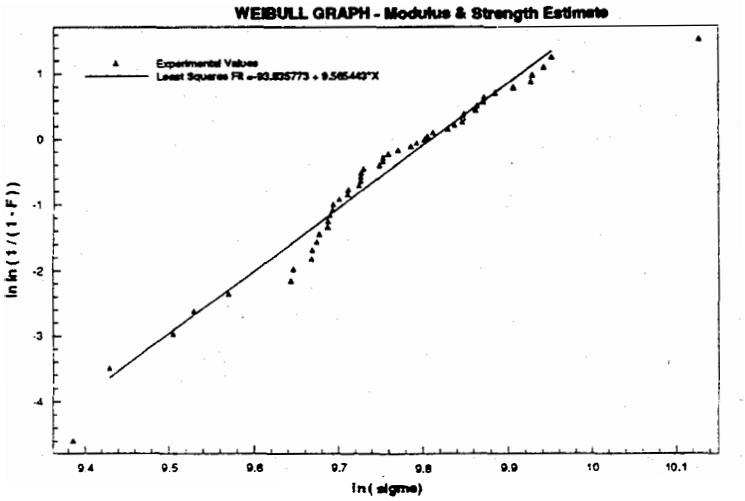


Figure 11
Weibull Graph
Modulus versus Strength



3.6.3 Simulation of Wafer Handling

Using the data on wafer strength that we have measured, a finite element model can be used to estimate the maximum stress levels and deflections that a wafer sees as the result of a particular handling step. The likelihood of the wafer fracturing at the applied stress level is determined based on the Weibull strength probability. This approach will be utilize to assist in the design of handling equipment for the 200 μm thick 15 cm by 15 cm wafers and cells being developed for this program

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13. ABSTRACT *(Maximum 200 words)*

This report describes work performed by Solarex, the objective of which is to advance Solarex's cast polycrystalline silicon manufacturing technology, reduce module production cost, increase module performance, and expand its commercial production capacities. Two specific objectives are to reduce the manufacturing cost for polycrystalline silicon PV modules to less than $1.20/W and to increase the manufacturing capability by a factor of three. To achieve these objectives, Solarex is working in the following technical areas: (1) casting, (2) wire saws, (3) cell process, (4) module assembly, (5) frameless module development, and (6) automated cell handling. Accomplishments reported include: (1) Cast first successful larger ingot producing 73% larger volume of usable silicon. (2) Increased the size of the ingot even further and cast an ingot yielding nine 11.4-cm x 11.4-cm bricks, representing a 125% increase in usable silicon from a single casting. (3) Operated the wire-saw in a semi-operational mode, producing 459,000 wafers at 94.1% overall yield. (4) Reduced the cost of wire-saw consumables, spare parts, and waste disposal. (5) Developed a cost-effective back surface field process that increases cell efficiency by 5% and began production trials. (6) Developed a plan for increasing the capacity in the module assembly area. (7) Completed qualification testing of modules built using Spire's automated tabbing and stringing machine. (8) Selected, tested, and qualified a low-cost electrical termination system. (9) Completed long-term UV testing of experimental back sheets. (10) Qualified the structure and adhesive-tape system for mounting frameless modules. (11) ARRI completed a study of the fracture properties of cast polycrystalline silicon wafers and provided the information necessary to calculate the maximum stresses allowable during wafer handling.

14. SUBJECT TERMS

cast polycrystalline silicon ; manufacturing ; modules ; photovoltaics ; solar cells

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