

# **Research on Polycrystalline Thin-Film Submodules Based on CuInSe<sub>2</sub> Materials**

**Final Subcontract Report  
11 November 1990 - 30 June 1995**

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Newtown, Pennsylvania*



National Renewable Energy Laboratory  
1617 Cole Boulevard  
Golden, Colorado 80401-3393  
A national laboratory of the U.S. Department of Energy  
Managed by Midwest Research Institute  
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## **Executive Summary**

Recent progress in photovoltaics has been particularly notable in several materials systems, especially in copper indium diselenide (CIS). Small area cells using this material have recently exhibited conversion efficiency in the range of 17% [1,2]. This material system exhibits a number of important advantages. It has a very high optical absorption coefficient throughout a major portion of the solar spectrum. It can be deposited in thin films having suitable electronic qualities on low cost substrates by a variety of methods. Modification of electronic properties such as band gap using ternary alloys has been accomplished, thus making the system versatile as well as robust.

This program marks the entry of Solarex into the development of CIS based photovoltaic (PV) product. This initial effort began with the development of manufacturable deposition methods for all required thin film layers and the development and understanding of processes using those methods. It necessarily included demonstration of the potential for high conversion efficiency, evidenced by the achievement of 14.4% conversion efficiency (total area) in small cells and followed with the development of viable methods for module segment formation and interconnection. Finally, these process steps were integrated to fabricate monolithic CIS based submodules which exhibited aperture area efficiencies exceeding 11%.

A more important result of this program is the basis of understanding that has been established in developing this material for PV applications. This basis of understanding is absolutely necessary to address issues of manufacturability and cost which are of paramount importance to the goal of commercialization. Early in the program, it was recognized that manufacturability would be determined by successful solutions to issues of yield, reproducibility and control as much as by material and energy costs, conversion efficiency and process speed.

Yield is strongly affected by shunt formation in modules, and shunt formation is in turn a strong function of the method used for absorber layer deposition. Issues of control and reproducibility are also strongly related to the absorber formation process. Accordingly, a significant effort was undertaken during this program to explore several alternative methods for absorber layer formation with attention to these issues. Specifically, the absorber layer formation techniques which were evaluated included: sputtering elemental precursors at low temperature followed by reaction at high temperature, a hybrid process using sputtered metallic precursors followed by reaction at high temperatures in an environment of elemental selenium, co-evaporation and concurrent reaction using elemental sources, and evaporation and/or sputtering of binary selenide precursors followed by reaction at high temperature with selenium. As a result, Solarex has identified at least one absorber formation process which is very robust to shunt formation from pinholes or point defects, tolerant of variation in processing temperature and elemental composition and capable of producing high conversion efficiency.

In addition to absorber layer formation, module scribing operations also have a significant impact on shunting, and thus on yield. This problem was attacked and greatly reduced through modifications to the scribing processes and the associated contacting layers. This program also allowed development and scale-up of processes for the deposition of all other substrate, heterojunction buffer, and window layers and associated scribing/module formation operations to 1000 cm<sup>2</sup> size. At the completion of this effort, Solarex has in place most of the necessary elements to begin transition to pilot operation of CIS manufacturing activities.

## Table of Contents

1.	Acknowledgments	page
2.	Executive Summary	
3.	Table of Contents List of Figures List of Tables	
4.	Introduction	1
4.1	Advantages of CIS Compared to Other PV Systems	1
4.2	General Structure - Devices and Modules	2
4.3	Manufacturability, Yield and Cost	4
5.	Technical Program	5
5.1	Overview	5
5.2	Summary of Phase 1 and Phase 2	5
5.3	Window Layers	10
5.3.1	The Buffer Layer	10
5.3.2	The High Resistivity ZnO Layer	11
5.3.3	The TCO: Low Resistivity ZnO Layer	11
5.4	Absorber Layer	14
5.4.1	Sputtered Compound Precursors	14
5.4.2	Co-evaporation of CIS	15
5.4.3	Spatial Uniformity of CIS Absorber Layers	18
5.4.4	Control and Reproducibility of CIS Deposition	23
5.4.5	Robustness and Process Tolerance of Variability in CIS Process	26
5.5	Module Processing	26
5.5.1	Module Scribing Improvements	26
5.6	Device and Module Results	30
5.6.1	Module Loss Analysis	34
5.6.2	Submodule Results	40
5.6.3	Submodule Encapsulation	40
5.7	Addendum	43
5.7.1	Device Improvements	43
5.7.2	Submodule Improvements	43
6.	Conclusions	50
7.	References	51

## List of Figures

Figure		page
4.2-1	Schematic view of solar cell device structure	3
4.2-2	Schematic view of standard module patterning structure	3
5.2-1	Effect of CdS thickness on the QE of a CIS solar cell	7
5.2-2	Optical transmission of RF sputtered and LPCVD ZnO on CdS	9
5.3.2-1	Arrhenius plot of conductivity of highly resistive ZnO prepared under various conditions	12
5.3.3-1	Spectral transmission of high conductivity ZnO made using various processes and conditions	13
5.4.1-1	Schematic representation of alternate methods of Se delivery	16
5.4.1-2	Cross-Section scanning electron micrographs of CIGS films deposited using various methods	17
5.4.3-1	Compositional uniformity of absorber layer over a 9" x 9" area	19
5.4.3-2	Uniformity of device performance over a 3" substrate	20
5.4.3-3a	Uniformity of average device performance over eight 3"x3" substrates	21
5.4.3-3b	Frequency histogram of device performance on eight 3"x3" substrates	22
5.4.4-1	Absorber layer composition for six consecutive depositions	24
5.4.4-2	Device J-V parameters for six consecutive absorber layer depositions	25
5.5.1-1	Measurement of J-V characteristic of a module segment either through a top grid or an interconnect	27
5.5.1-2	A scanning electron micrograph and schematic view of step coverage of ZnO at an interconnect	28
5.5.1-3	An optical micrograph of a defective substrate scribe	29
5.5.1-4	An optical micrograph of a high quality substrate scribe	29
5.6-1	The light J-V characteristic of the highest efficiency small area cell	32
5.6-2	The dark J-V characteristic of the highest efficiency small area cell	33
5.6.1-1	A schematic representation of the circuit used for module analysis	35
5.6.1-2	Calculated and measured J-V data for a module segment using various segment widths, front contact and interconnect resistivities	36
5.6.1-3	The calculated module efficiency using 18 or 12 mil interconnects	37
5.6.1-4	The calculated module efficiency using 6 or 0 mil interconnects	38
5.6.1-5	The calculated module efficiency for two values of interconnect resistivity	39
5.6.2-1	The J-V characteristic of a high efficiency submodule	41
5.6.3-1	The J-V characteristic of a submodule before and after lamination	42
5.7.1-1	The light J-V characteristic of a 15.5% efficient device	45
5.7.1-2	The dark J-V characteristic of a 15.5% efficient device	46

## **List of Figures (cont'd)**

<b>Figure</b>		<b>page</b>
5.7.1-3	A comparison of the quantum efficiency of a 14.4% and a 15.5% efficient device	47
5.7.2-1	The light J-V characteristic of a 13.0% efficient submodule	48
5.7.2-2	A comparison of the quantum efficiency of a 13.0% efficient submodule and a 15.5% efficient device	49

## **List of Tables**

<b>Table</b>		<b>page</b>
5.2-1	Comparison of Sputtered vs LPCVD ZnO	8
5.6-1	J-V parameters of best solar cells made in each contract phase	30
5.6-2	Comparison of J-V measurement on cells at Solarex and NREL	31

## INTRODUCTION

### 4.1 Advantages of CIS Compared to Other PV Systems

The CIS family of materials was originally considered as a "promising, low cost" technology using polycrystalline thin films that can be deposited in a relatively "dirty" ways and yet lead to material properties compatible with practical solar cells. In the past years laboratory scale progress has been very rapid and the CIS family can be considered as candidates for "high efficiency PV devices" as NREL has achieved over 17% in small area solar cells. Nevertheless, if CIS is to become a real economic product within the near future, the low cost potential must clearly be demonstrated for large area (1 to 4 square foot) module structures.

This low cost/high efficiency situation is quite unique and is challenged only by the CdS/CdTe (cadmium-sulfide/cadmium telluride) system. The main difference between CdTe and CIS is that CdTe can be considered easier to synthesize as shown by the large spectrum of successful techniques with which the films can be grown. On the other hand, the toxicity issues between the two materials clearly favor CIS.

It should be understood that the term "CIS", although derived from "copper indium diselenide" is used to refer to a large family of materials. Although confusing, the term "CIS" also often refers to ternary alloys in which some indium is replaced by gallium (i.e.  $\text{Cu}(\text{In,Ga})\text{Se}_2$ ) or where some selenium is replaced by sulfur (i.e.  $\text{CuIn}(\text{S,Se})_2$ ) or where both substitutions occur (as in  $(\text{Cu}(\text{In,Ga})(\text{S,Se})_2$ ). These ternary chalcopyrite alloys are sometimes denoted as CIGS, CISS and CIGSS respectively.

As the material system expands from a chemical point of view, so also do the associated physical and opto-electronic properties, thus offering great flexibility for materials and device engineering. For example, the energy bandgap of the absorber layer can be modified to achieve a better spectral match to the available insolation, or for use in a tandem structure. Indeed, even the depth profile of the absorber layer bandgap within the device may be varied to impact carrier collection and thus performance.

CIS also exhibits remarkable tolerance. Formation of the material appears to be quite tolerant to the variation of specific deposition conditions, such as substrate temperature and film stoichiometry, and the electronic properties seem to be very tolerant of point and crystal defects, including grain boundaries and interfaces. Tolerance to the quality of the deposition environment, tolerance to atmospheric exposure between various synthesis steps, and tolerance to feedstock quality are also valuable features relating to the potential for low cost materials and PV structures.

Manufacturability in large area has yet to be demonstrated for CIS, but when compared to a-Si, CIS has the potential for substantially higher conversion efficiency and does not exhibit any light-induced degradation. At Solarex, we believe that the two technologies are complementary in a commercial sense and even tandem structures between the two may be possible.

## 4.2 General Structure - Devices and Modules

### DEVICES:

Solar cells have been fabricated using the device structure:

light  $\implies$  Ni-Al grid/ZnO:Al/i-ZnO/CdS/CI(G)S/Mo/Glass

as shown in Figure 4.2-1.

The Mo back contact is deposited on soda lime glass substrates by DC magnetron sputtering.

The absorber layer is currently being deposited by two different methods: either by sputtering or thermal evaporation of CIGS films on the Mo/glass substrates.

A CdS layer (approximately 50 nm) deposited by chemical bath deposition (CBD) forms a buffer layer with the absorber material. On top of the CdS, a ZnO bilayer is deposited, an intrinsic ZnO layer of 50 nm, followed by a conductive ZnO layer 300 - 500 nm thick. The doped ZnO layer has a typical sheet resistance of 10-20 ohms/sq and 88-94% integrated transmission in the visible spectra.

The metal grid pattern has been designed for effective current collection with the described window layer. The grids are a bilayer of Ni-Al, both deposited by e-beam evaporation through a metal mask. Using the described structure, 14.4% solar cell efficiencies have been attained.

### MODULES:

The CIGS module made at Solarex has a ZnO:Al/i-ZnO/CdS/CIGS/Mo/glass structure, with light incident on the top ZnO contact. Serial interconnects between module segments are formed by three separate scribes; 1) the substrate scribe through the Mo, 2) the interconnect scribe through the absorber and CdS layers, and 3) the front contact scribe through the ZnO (and absorber) layers. The scribes in the Mo and ZnO layers electrically isolate the top and bottom segment contacts from the adjacent segment. The scribe through the absorber layer forms an interconnect between the top contact of one segment and the bottom contact of the adjacent segment as shown in Figure 4.2-2.

The Mo substrate scribe is done using a laser, while the interconnect and front contact scribe are made through mechanical means. In order to minimize module power losses, optimization of several parameters is necessary. They include; 1) top contact resistivity and transparency, 2) segment width, and 3) scribe or interconnect width. Submodules made using this process have demonstrated greater than 11% aperture area cell efficiencies.

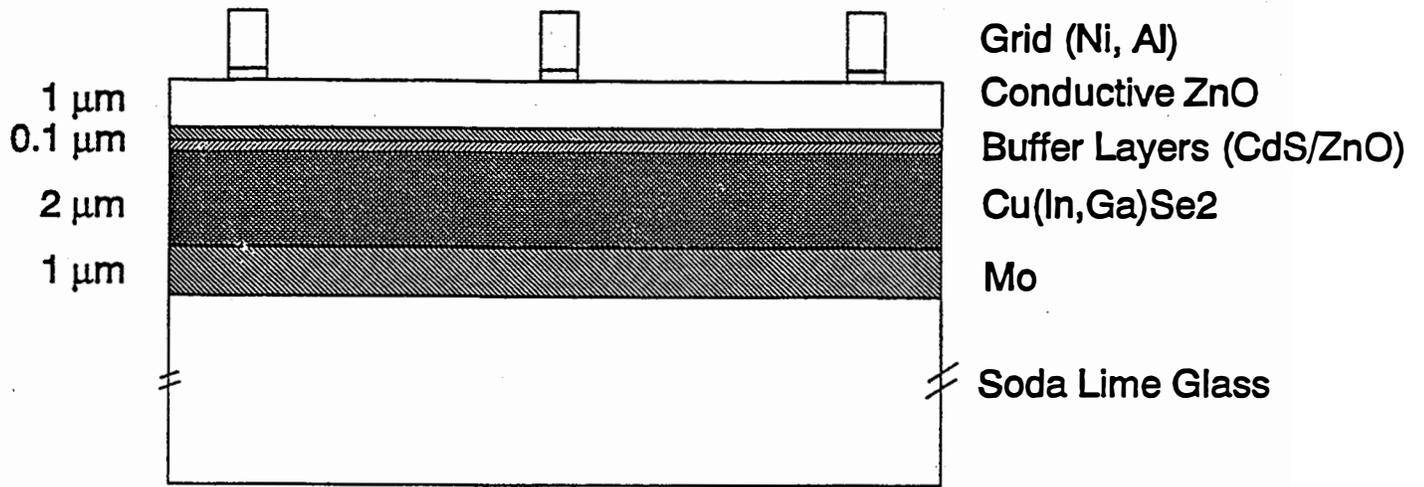


Figure 4.2.1 Schematic view of  $\text{Cu}(\text{In,Ga})\text{Se}_2$  based solar cell device structure.

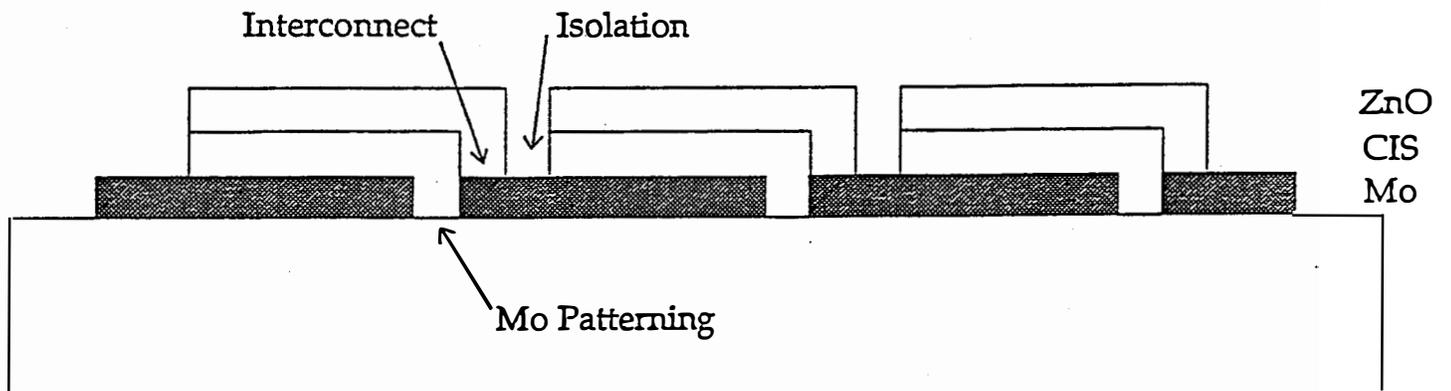


Figure 4.2.2 Schematic view of standard module patterning structure.

### **4.3 Manufacturability, Yield and Cost**

For CIS based PV to be commercially successful the module fabrication process must satisfy considerations of manufacturability, yield and cost. These factors must be considered for each constituent layer and for the aggregate operation of the entire module.

The initial steps of glass cleaning, Mo deposition and substrate scribing are not expected to present problems with regard to these considerations.

The absorber deposition process must exhibit good materials utilization for reasons of cost. The absorber deposition process must also be tolerant of run to run and spatial variations in elemental composition and temperature for manufacturability and yield considerations. Typically, absorber formation is expected to be one of the controlling factors for overall production rate, so process speed for this step is also a manufacturability and cost concern.

For the heterojunction buffer layer, because of the materials and thicknesses involved, cost is not an issue. However, consideration must be given to the disposal of hazardous material associated with the current wet CBD process of CdS to avoid significant costs.

Present methods for the deposition of the top contacting layer of zinc oxide (ZnO) are rapid and easily scaleable to large areas and thus are manufacturable. However, the materials cost involved can be significant if the ZnO is sputtered from fabricated zinc oxide targets. Fortunately, alternate methods of ZnO deposition exist and have been developed for use at Solarex[3].

Final yield for working modules remains as one of the largest concerns in developing an entire process. To date, our experience suggests that module yield should be expected to be most affected by shunting of module segments. Shunting of segments occurs typically at a point defect or pinhole in the absorber layer which allows current leakage from front to back segment contacts.

The two processes which bear most strongly on yield loss due to shunting appear to be absorber formation and module scribing operations. Adhesion of the absorber layer to the back contact is central to avoiding pinholes in that layer, and thus shunts, and is strongly dependent on the absorber deposition process. Adhesion at the absorber-substrate interface also affects control and reproducibility of scribing operations. Further, the tendency to form point defects which nucleate on substrate imperfections or particles of contaminant appear also to be strongly dependent on the absorber formation process.

Scribing operations, particularly the substrate scribe, cause module shunting through several means. During the substrate scribing operation, areas of the Mo rear contact are selectively removed by laser. The ejected metal is one source of substrate debris that can cause pinholes and point defects subsequently through the absorber layer. Irregular, flaked or partially removed contact material along substrate scribe edges easily result in shunts along the module segment edges. Shunts also arise if the interconnect and substrate scribe cross, which can occur due to poor registration or due to excessively wide chipping of the absorber layer during the interconnect

scribe. Again, the average width and the chipping in the interconnect scribe of the absorber layer is dependent on the absorber deposition process. Fortunately, the processes which typically possess excellent adhesion at the absorber-substrate interface also appear robust to shunt generation due to contaminating particulate/point defect generation and interconnect scribe irregularity.

## **5. Technical Program**

### **5.1 Overview**

In phase 1 of this program, effort was directed toward development of the basic processes used for the substrate/back contact, heterojunction/buffer, and top contact/window layers required for CIGS cell fabrication. Work was initiated on several different approaches to accomplish absorber deposition. In the second phase of this program emphasis was placed on scaling up all basic processes to 1000 cm<sup>2</sup> substrate size.

The second phase initiated the development of scribing and interconnect formation processes for submodule fabrication. Also, some approaches to absorber formation were discontinued or replaced with others based on experimental results and manufacturability concerns.

The third phase effort was focused on only the most promising methods for absorber formation. More emphasis was put on submodule fabrication, scribe and interconnect development, uniformity, control and performance optimization, and preliminary work on encapsulation.

### **5.2 Summary of Phase 1 and Phase 2**

Phase 1 saw the development of the window layer deposition process that allowed the in-house fabrication of CIS solar cells. The window layer consisted of two materials, a CdS buffer layer and a conductive ZnO top layer. The CdS was deposited by chemical bath deposition (CBD), while the ZnO films were deposited by low pressure chemical vapor deposition (LPCVD).

Conductive ZnO films were deposited by low pressure chemical vapor deposition from diethylzinc (DEZ) and water feedstocks with diborane gas used as the dopant source. The deposition process was optimized to form ZnO films with high optical transmission between 400 and 1400 nm combined with low electrical resistance. Typically, films with high optical transmission also have high sheet resistance. For maximum solar cell efficiency, a highly transparent film is required that does not compromise the current collection. This was accomplished through optimization of the LPCVD deposition variables including feedstock flow rate, dopant concentration and substrate temperature. ZnO films used in devices have a visible transmission of approximately 94% and sheet resistance ranging from 10-15 ohms/sq.

Molybdenum, deposited on either soda-lime or Corning 7059 glass, was used as the back contact. Both sputtering from a metal target and e-beam evaporation are used to deposit the Mo films. Films of 1 -2 um thickness exhibit a sheet resistivity of 0.15 - 0.25 ohms/sq. The front contact is a grid formed by e-beam evaporation of an aluminium-nickel bilayer through a metal mask.

At the start of Phase 1, the CIS absorber layer was deposited by magnetron sputtering from elemental targets onto heated Mo coated glass substrates. Circular motion of the heated substrate holder allowed for the sequential deposition of the individual fluxes and better spatial uniformity in stoichiometric CIS films.

Two problems inherent with sputtering elemental Se were encountered forcing the reevaluation of the Se deposition process. The Se flux contaminates the Cu and In targets causing the metal flux to vary depending on the degree of metal contamination and, additionally, spot evaporation of Se occurs during sputtering due to non-uniform heating of the Se target. To overcome these problems, a hybrid deposition process was developed in which the Se was thermally evaporated, while simultaneously co-sputtering the metals. Contamination of the metal targets was minimized by careful shielding of the Se source during the deposition. Solar cells with 6.2% efficiencies were made using the hybrid deposition process. A more comprehensive description of this work is contained in the annual report to NREL for this phase [4].

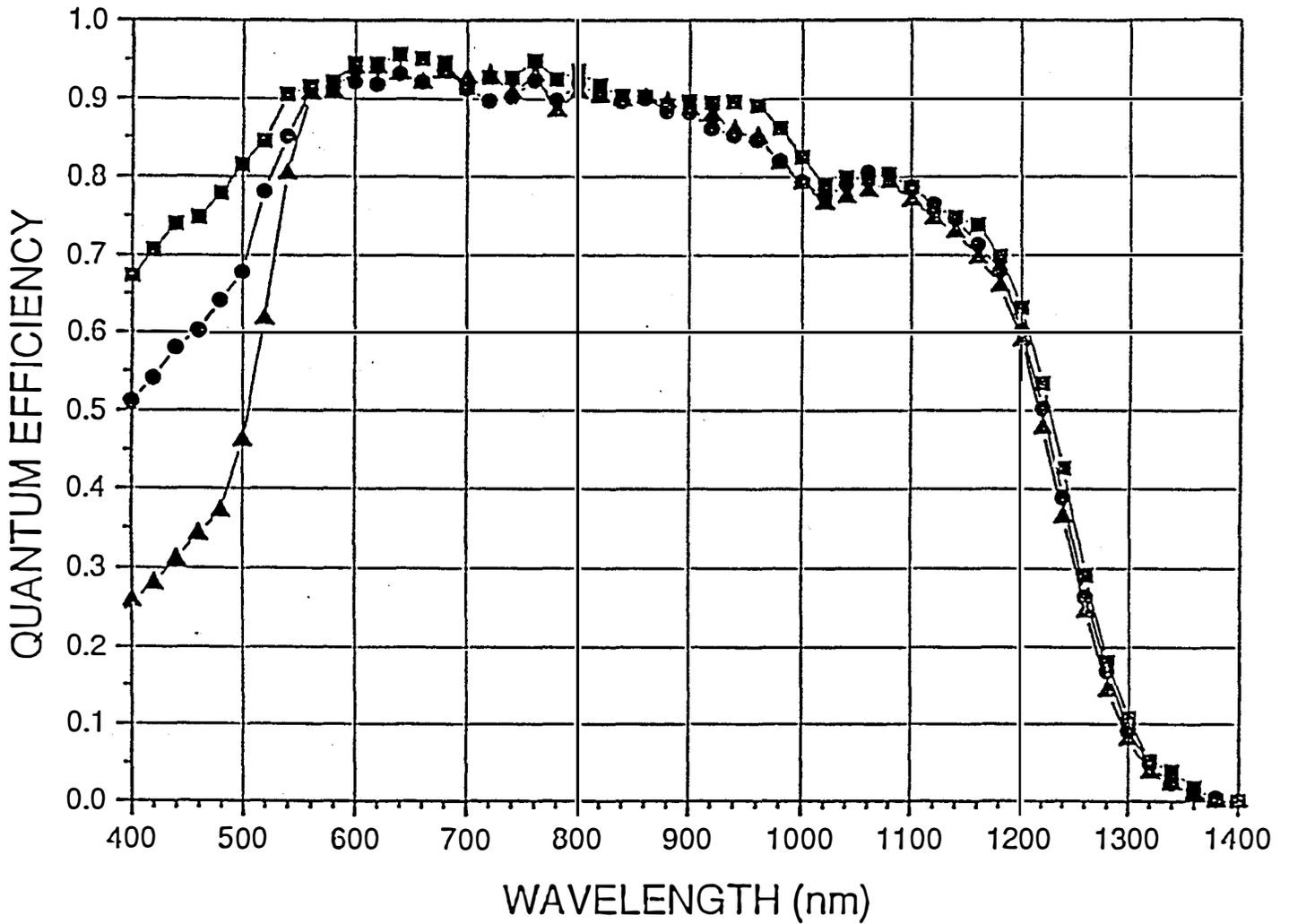
In phase 2, research was carried out on the window layers for two reasons: the CdS and ZnO window layers were characterized individually and in tandem in order to better understand their interaction with the absorber layer and, additionally, to evaluate cost effective methods for depositing the CdS and ZnO on large area modules.

The CBD process used to deposit the CdS films is a low temperature ( $< 90^{\circ}\text{C}$ ) deposition process utilizing an aqueous mixture of cadmium chloride, ammonium chloride, ammonium hydroxide and thiourea [5,6]. The films are presumed to be stoichiometric, exhibit excellent spatial uniformity and are highly resistive, approximately  $10^8 - 10^9$  ohm-cm when deposited on glass. By varying the CdS film thickness, changes are seen in the short wavelength optical transmission with thicker films being more absorbing. The sub-bandgap transmission is unaffected by the film thickness.

The chemical composition of the deposition bath was optimized to allow well controlled CdS film growth. Since the reaction proceeds by an ion by ion deposition mechanism, the CdS film is stoichiometric and highly resistive. The reaction mechanism also makes it very difficult to dope the films in situ.

The optical characteristics of the film were dominated by the film thickness. As the film thickness increases, the short wavelength transmission decreases. The effect of this absorption was also seen in the QE of completed CIS devices, where a decrease in short circuit current corresponds to an increase in CdS film thickness. The current loss occurred in the short wavelength region. This effect is seen in Figure 5.2-1, where the QE is shown as a function of CdS film thickness.

The CdS process was scaled up to allow uniform deposition over  $1000\text{ cm}^2$ . The scale-up required the use of a large rectangular deposition tank and modification to the stirring mechanism. The films are highly uniform and exhibited the same optical and electrical properties as films from the smaller bath. Although a larger total volume is required, the chemical yield per unit area is similar to that of the smaller CBD bath.



**Figure 5.2-1** Effect of CdS thickness on the QE of a CIS solar cell. Integrated current values for the three CdS thicknesses:

- CdS < 40 nm -  $J_{sc} = 40.55 \text{ mA/cm}^2$
- CdS ~ 50 nm -  $J_{sc} = 38.81 \text{ mA/cm}^2$
- ▲ CdS ~ 100 nm -  $J_{sc} = 36.87 \text{ mA/cm}^2$

The LPCVD ZnO process was further characterized to better understand its role as a top contact material. The three factors that most strongly effected the LPCVD ZnO optical and electrical properties were the dopant concentration, the substrate deposition temperature and film thickness. Through optimization of the deposition parameters, highly conductive and transmissive films were made with the major effort directed towards improving the long wavelength transmission while maintaining high electrical conductivity [7]. Quantum efficiency data was used as a guideline for process development. During this development, this process was also scaled up to uniformly cover 230 cm<sup>2</sup>.

An RF sputtering process for ZnO has also been developed, and was scaled up to uniformly cover 1000 cm<sup>2</sup> substrate size. This ZnO was deposited from an aluminium oxide doped ZnO target as a single conductive layer. The film used for CIS modules is nominally 500 nm thick with a sheet resistance of 10 -20 ohms/sq.. Under certain deposition conditions , the optical transmission was comparable with the LPCVD ZnO. Table 5.2-1 compares the properties of the LPCVD and RF sputtered ZnO, and in figure 5.2-2 the spectral transmission (on CdS) is shown. It should be noted that the RF sputter process has not been fully optimized for cell or module use.

**Table 5.2-1 Comparison of Sputtered vs. LPCVD ZnO.**

	LPCVD	RF Sputtered
Resistivity	1.2-1.5 x 10 <sup>-3</sup> ohm-cm	4.0-6.0 x 10 <sup>-4</sup> ohm-cm
Thickness	0.85 to 1.3 um	0.35 um
Sheet Resistance	10 to 15 ohms/square	12 to 18 ohms/square
Haze	5% to 15%	< 1%
Integrated Visible Transmission (film only)	92% to 94%	92%
Spectral Transmission @ 1200 nm	> 85%	>78%
Spectral Transmission @ 1400 nm	> 80%	>60%

The combined effect of both the ZnO and CdS window layers is critical for good solar cell device performance. Through optimization of the film thickness and the optical transmission of the ZnO and CdS layers and the electrical resistance of the ZnO layer, CIS devices with greater than 40 mA/cm<sup>2</sup> were made, as shown in figure 5.2-1.

During Phase 2 three separate deposition processes were evaluated based on manufacturability and CIS material quality. The three processes included:

1. three source co-sputtering of Cu, In and Se,
2. hybrid deposition process in which Cu and In are sputtered and the Se is thermally evaporated, and,
3. elemental deposition and compound formation (EDCF).

Because of the problems with cross contamination of sputtering targets and uncontrolled Se delivery rates, effort at the end of this phase was focused on the EDCF method.

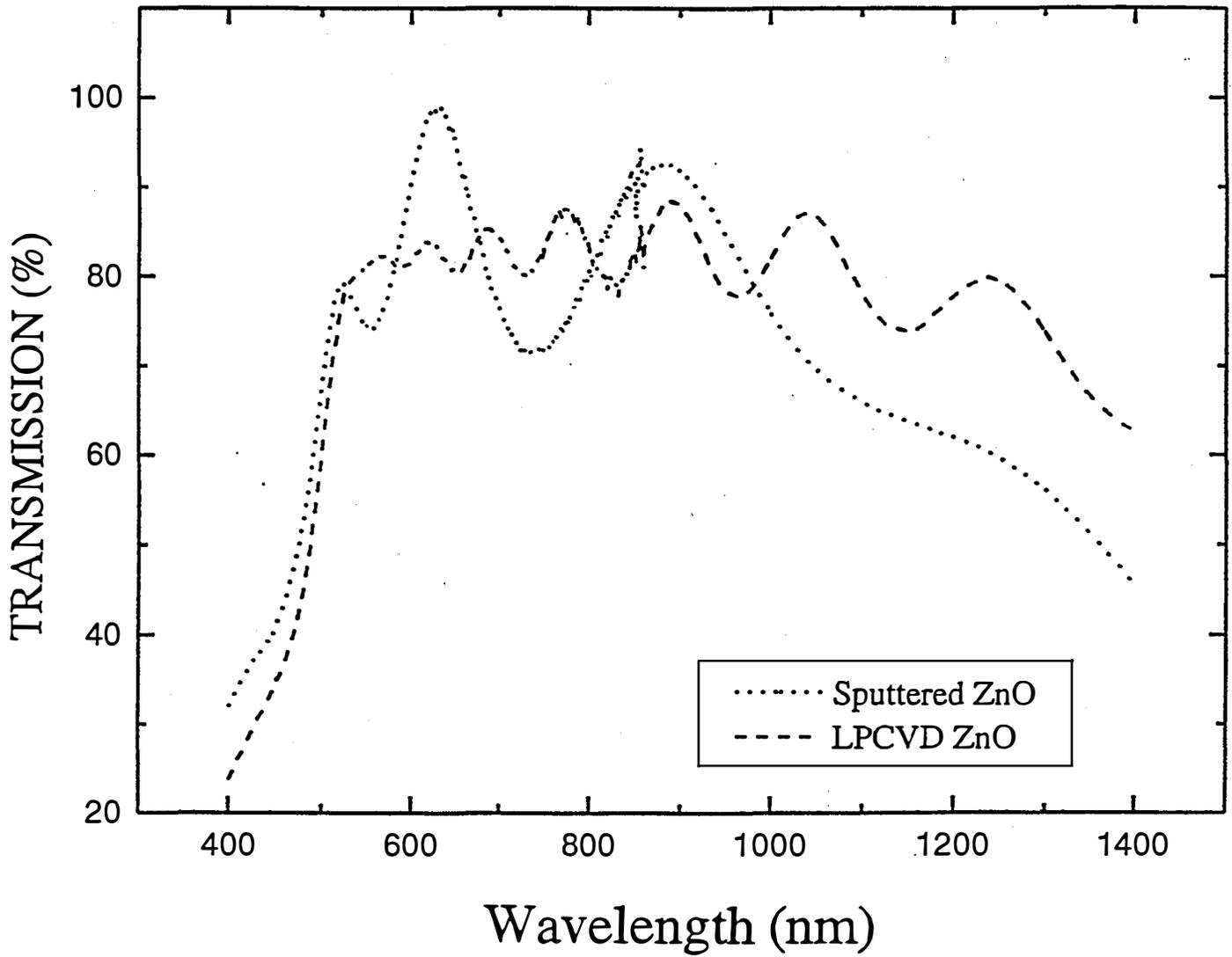


Figure 5.2-2 Comparison of RF Sputtered vs. LPCVD ZnO deposited on CdS coated glass substrates.

In the EDCF process the metals and Se were sequentially deposited onto a substrate at low temperature and, in a second step, the layers were thermally converted to chalcopyrite CIS by a high temperature heat treatment. The Cu and In layers were sputtered onto Mo/glass substrate as either elemental stacks or co-deposited metallic films. The Se film was then thermally evaporated onto the metallic layer and the entire stack was heated in controlled environment allowing for CIS formation.

In early experiments, using Se confinement during heat treatment, CIS devices with over 10% solar cell efficiencies were made. Maintaining a high Se overpressure during the compound formation step was critical to obtaining high quality stoichiometric CIS. During the heat treatment, the Se on top of the stack changes from solid to liquid to vapor, allowing for significant Se loss through evaporation.

In order to meet the goal of making large area CIS, the compound formation step is moved to a heated, load locked vacuum chamber capable of handling substrates up to 1000 cm<sup>2</sup>. Using this equipment, CIS was successfully formed on substrates up to 8" x8".

A more comprehensive description of this work is contained in the annual report to NREL for this phase [8,9]. The remainder of this report will describe work done in Phase 3.

### **5.3 WINDOW LAYERS**

For work in Phase 3, window layers for both devices and modules consist of the following sequence:

- 1) a buffer layer: often of CdS deposited by a CBD technique, thickness ~ 50 nm.
- 2) a high resistivity ZnO layer, thickness ~ 50 nm.
- 3) a low resistivity ZnO layer as TCO, thickness ~ 400-1000 nm.

#### **5.3.1 The Buffer Layer**

As stated in the Overview, at Solarex a variety of materials and deposition procedures have been explored. CBD of CdS is still found to be the most successful buffer layer in respect to the solar cell conversion efficiencies obtained. At Solarex, two different methods of preparing the bath lead to equivalent conversion efficiencies, but to considerably different junction behavior in some aspects.

In the first of these two procedures, the sample on which the CdS is to be deposited and the sulfur source (thiourea) are added together once the bath has reached its reaction temperature (~80C). In the second procedure the reactants are mixed at room temperature and heated up to the reaction temperature only after the sample on which the CdS is to be deposited has been immersed. Differences in the junction behavior are found when the illumination is void of photons that can be absorbed in the CdS itself (<550 nm). A publication concerning these effects is in progress.

### 5.3.2 The High Resistivity ZnO Layer

Although its role is still unclear, in the standard cell structure a thin (~50 nm) high resistive layer of ZnO is deposited between the buffer and the TCO. In the present stage of this work, only RF-sputtering from ceramic targets is considered and a parameter of interest has been the presence of additional oxygen during the sputtering, as this has shown its importance in the literature [10,11]. At Solarex, either pure ZnO targets are used (with or without additional oxygen) or  $(1-x)\text{ZnO}/x\text{Al}_2\text{O}_3$  with  $x\sim 0.02$  mixed targets are used with additional oxygen.

In the pure ZnO target case, the original idea of adding the extra oxygen to the sputter gas is to insure that the film does not grow to be oxygen deficient and therefore become more conductive (and probably less stable in air). Nevertheless, at Solarex the films grown without oxygen in the sputter gas show to be very resistive, as shown in figure 5.3.2-1.

In figure 5.3.2-1 is also shown highly resistive layers grown from a doped target (containing  $\text{Al}_2\text{O}_3$ ) but where the film resistivity can be modified by the quantity of oxygen introduced into the sputter gas, as has been shown by Birkmire et al. [12]. Although these films are far less resistive (~0.1 to 0.01 ohm-cm) than those deposited from the pure ZnO targets ( $1\times 10^{-5}$  to  $1\times 10^{-6}$  ohm-cm), cell results do not differ sufficiently to conclude.

### 5.3.3 The TCO: Low Resistivity ZnO Layer

The lateral collection of photogenerated current occurs predominantly in the highly conductive part of the window structure. The standard deposition procedure is RF-sputtering from a ZnO target doped with 2%  $\text{Al}_2\text{O}_3$  with or without traces of oxygen in the sputter gas. The addition of very small amounts of oxygen to the sputter gas can enhance the transparency of the films without any substantial losses to the conductivity. The quantities of oxygen necessary depend strongly on the state of the target, and thus the "memory" effects from the proceeding deposition conditions and oxygen rates can be remarkable.

For devices the low resistivity ZnO is typically 400 to 500 nm thick and 10 to 20 ohms/square whereas for modules, thicknesses on the order of 1000 nm and sheet resistivities between 5 and 10 ohms/square are used. Spectral transmission curves for such films are shown in figure 5.3.3-1.

Disadvantages of RF-sputtering from ceramic targets include high materials and system costs as well as low throughput. These difficulties increase for modules since thick or highly conductive ZnO films are required. Accordingly, we have also pursued alternative methods for the ZnO deposition. A "novel" process has been defined which can rapidly deposit thick films of both high conductivity and high transparency at low production costs. The optical transmission for a typical such film is also shown in figure 5.3.3-2. First devices and submodules using these ZnO layers appear to be of equivalent quality to those produced using the RF-sputtered ceramic targets.

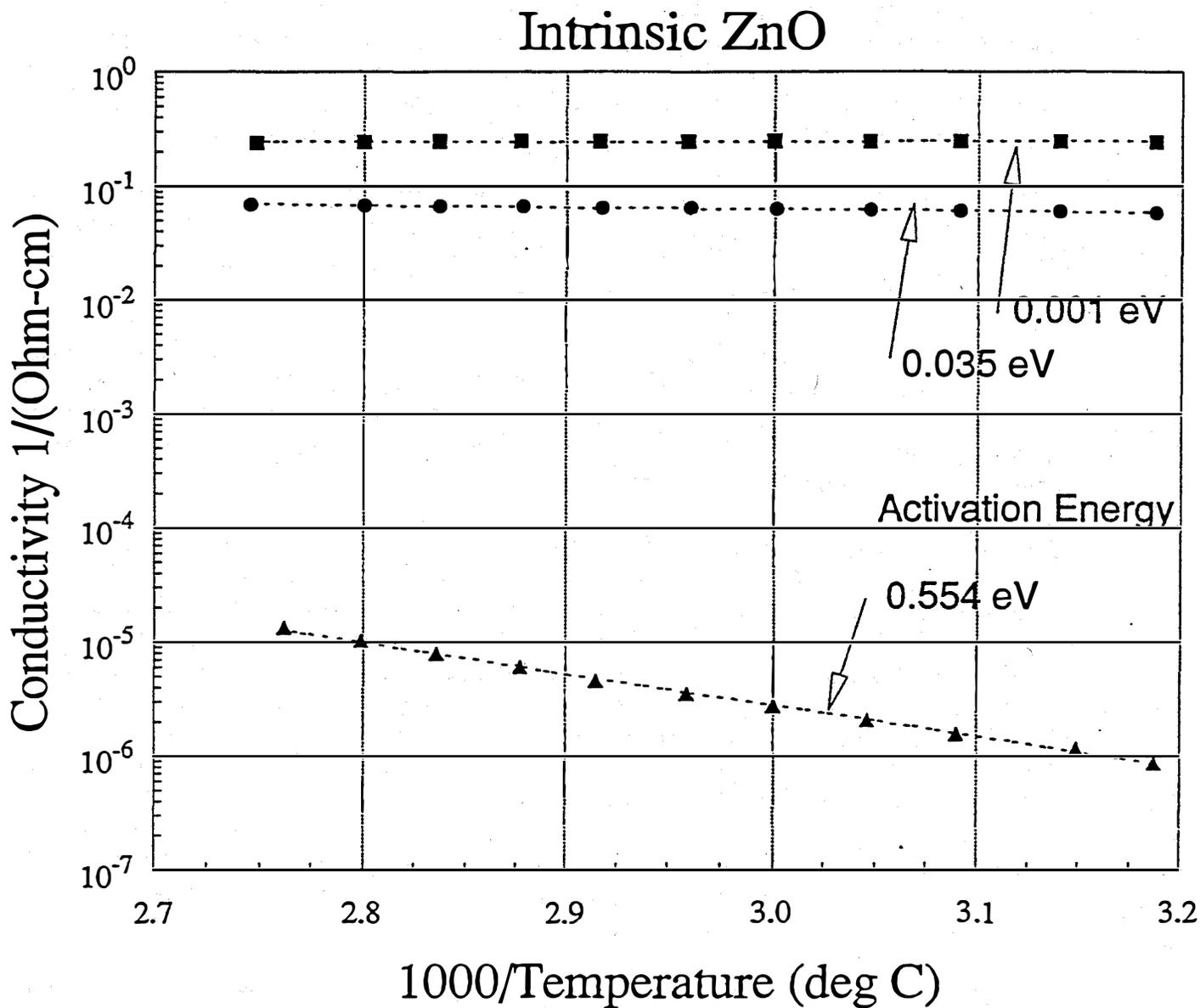


Figure 5.3.2-1 Arrhenius plot showing the activation behavior of conductivity of highly resistive ZnO used in the window layer made from various targets and gas mixtures.

- 0.6% O<sub>2</sub> in Ar, 2% Al<sub>2</sub>O<sub>3</sub>/98%ZnO target
- 1.2% O<sub>2</sub> in Ar, 2% Al<sub>2</sub>O<sub>3</sub>/98%ZnO target
- ▲ Pure Ar, pure ZnO target

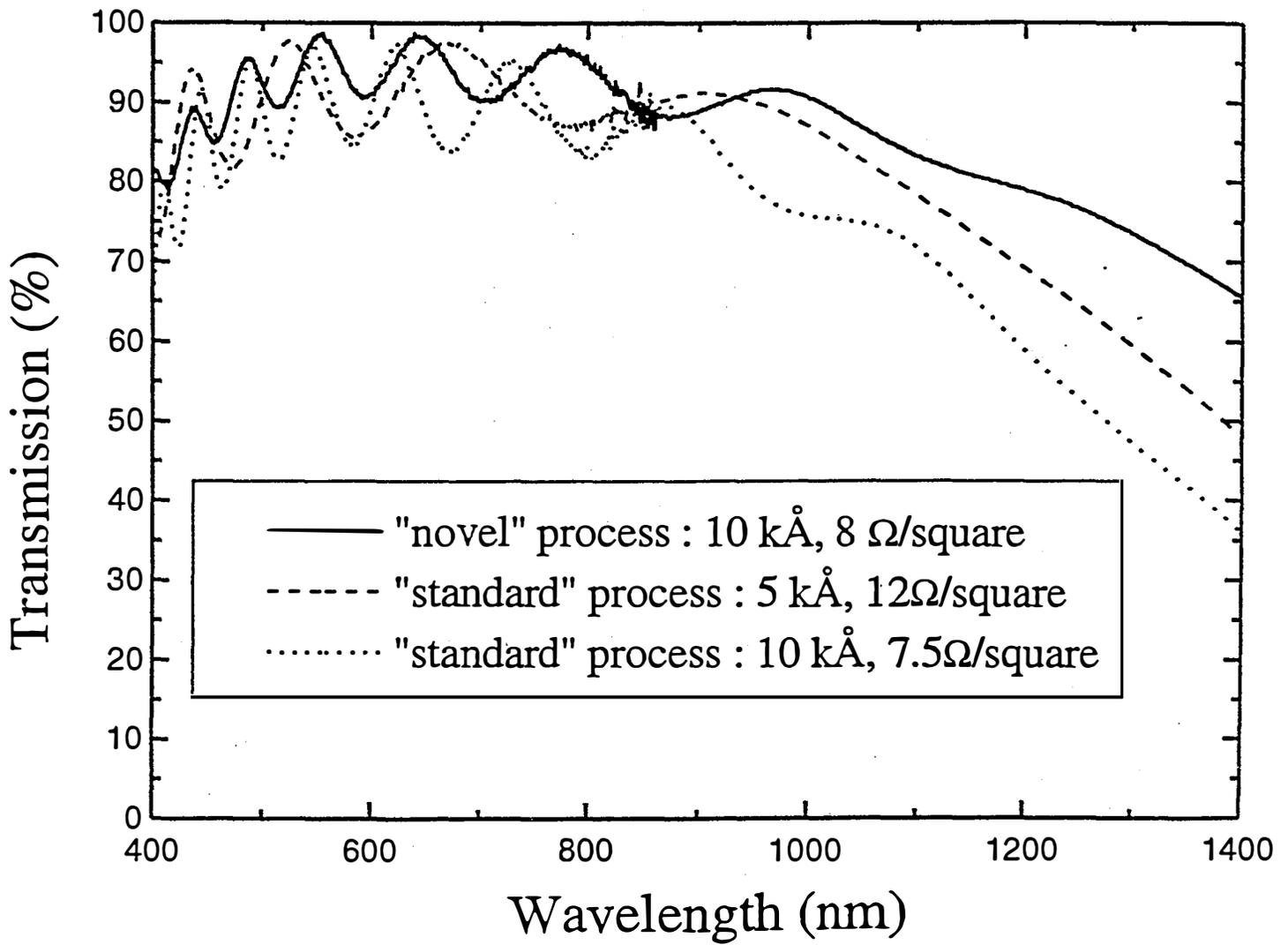


Figure 5.3.3-1 Spectral transmissin characteristics of high conductivity ZnO made using several different sputtering processes.

## 5.4 ABSORBER LAYERS

Although many of the absorber layer formation methods pursued in the previous phases demonstrated reasonable conversion efficiency and possessed numerous advantages, several difficulties had also become evident as well. Specifically, the difficulties in absorber layer adhesion, reproducibility and control were expected to have severe implications for module fabrication. Accordingly, the methods used for absorber formation were further expanded to include evaporative techniques onto high temperature substrates and sputtering/evaporation of binary compounds at low and intermediate temperatures. In phase 3 the window and substrate processes developed in the first two phases were coupled with the development of these additional absorber layer deposition processes. Successful module fabrication also necessitated the further development of scribing and module processing techniques. The following sections primarily constitute the details and results of this work.

### 5.4.1 Sputtered Compound Precursors

Sputtering is a well established large area deposition method applicable to numerous material systems. In the case of CIGS it is often believed that film synthesis from sputter techniques would be technically more simple to scale-up than film synthesis from evaporation techniques. The simple approach of sputtering "pure metal precursors" of Cu - In (-Ga) that are then submitted to a selenization environment (elemental selenium vapor or H<sub>2</sub>Se) can and has been successful [13,14] but, nevertheless, seems to have some limitations. The competition between the formation of intermetallics and of binary selenides as intermediate stages of the film growth may be complex and problematic. In particular, liquid phases of the intermetallics are suspected to be a common cause of morphological and adhesion problems.

Originally based on the idea of avoiding the intermetallics, an alternative approach consists of using metal selenides as starting materials [15,16,17]. Many of the questions that are addressed concern the properties and behavior of these sources themselves. Which binary selenides should be used? Are these materials cost effective? As sputter sources are these binary compounds well behaved or reproducible from run to run?

At Solarex we have experimented with a large variety of binary selenide sputter targets. Both DC- and RF- sputtering are used depending on the source materials. Usually copper selenides and/or pure and alloyed metals are DC- sputtered, while indium/gallium selenides are RF-sputtered. Conditions (sputter power, pressure, temperature) have been found where each source material is well behaved and the obtained films do not depend on target history, but strictly on substrate temperature and other vacuum chamber conditions.

Even when the binary selenide targets lead to films of correct Cu/In/Ga/Se compositions, these films require a selenization step in order to be device relevant. In this work, the selenization is performed using selenium vapor from the thermal evaporation of an elemental source. These sources can be "line of sight" to the substrate or not. When they are not, the technique consists of a Se oven and a heated transport tube equipped with a high temperature valve and a vapor distribution system. These two source configurations are schematically shown in figure 5.4.1-1A.

The "exterior Se oven" type configuration (figure 5.4.1-1B) can be seen as advantageous in a number of aspects. The control dynamics for the Se flux within the deposition system is far more rapid with the valve than by the thermal response of the internal Se evaporation source; in situ shuttering of Se is very inefficient. It is also argued that such a system is closer to a manufacturing environment than the "line of sight" Se crucibles.

Within the logic of sequential deposition, an attractive idea is to deposit the reactants first (i.e. sputter at low substrate temperatures) and then, secondly, to drive the reaction (i.e. anneal at high temperatures in a Se environment). From a processing point of view, this means that the sequence of Cu/In/Ga selenide depositions, which require line of sight (i.e. one machine, one substrate) can be performed rapidly. Then the reaction step, in which kinetics may require more time, can be performed without need of line of sight (i.e. batch processing ; one machine, n-substrates).

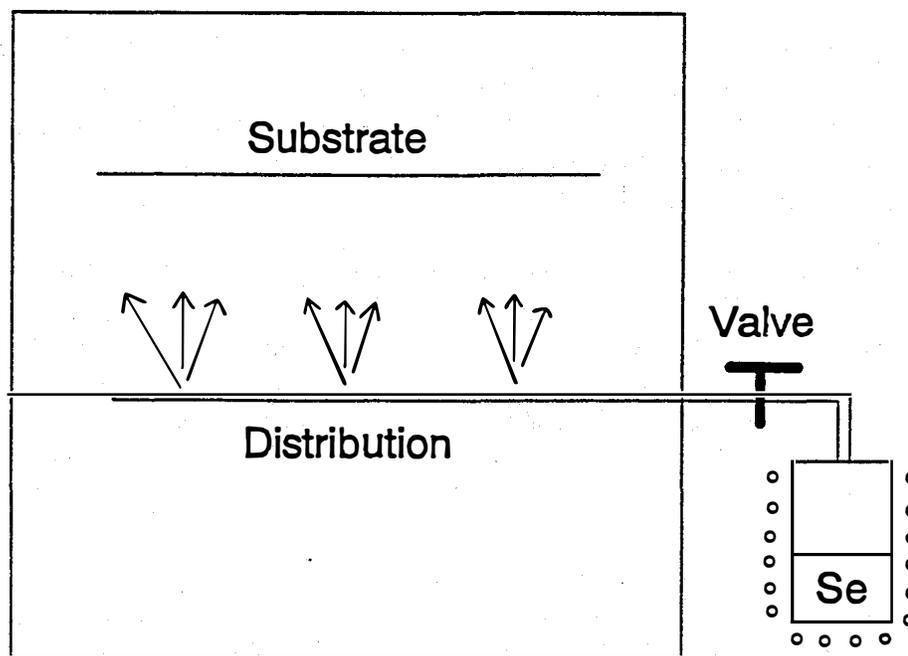
The compound sputtered precursor approach to CIGS formation capitalizes on the above expressed ideas. The films are found to be very easy to control from a compositional, morphological and adhesion point of view, and cell/submodule results are promising. In particular, in figure 5.4.1-2 is shown a comparison of the SEM cross-sections between a sequentially sputtered film and a sequentially evaporated film. No remarkable differences can be seen, both processes leading to very dense and smooth films.

#### **5.4.2 Co-evaporation of CIGS**

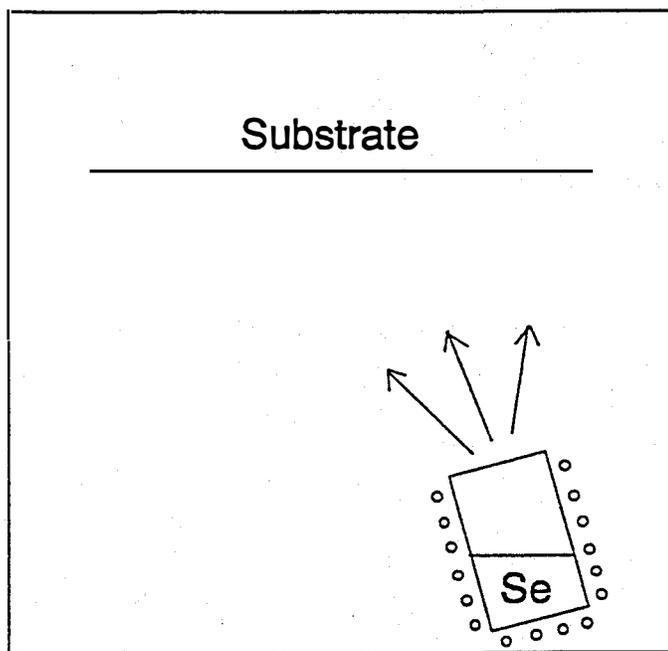
The use of thermal evaporation sources of the elements has been the most common small scale technique employed in highest quality CIGS film formation and a number of deposition sequences have been reported that lead to excellent material properties of the films.[18,19] The issue here addressed at Solarex is the question of scalability of such a process. In most of the work here presented we have concentrated on a deposition schedule that can be considered semi-sequential in the sense that the indium and gallium are co-evaporated in the presence of selenium followed by deposition of copper in the presence of selenium. The main advantages of this process are its large compositional tolerance and its excellent adhesion to the Mo coated substrates. The compositional tolerance plays a key role in the ability to obtain relatively uniform solar cell results over the larger areas with which we work.

Several advantages of this approach include substantial flexibility in terms of deposition sequence and stoichiometric control as a function of depth in the absorber layer. The benefits of bandgap variation or grading through the film depth have been reported.[20,21] With deposition techniques using intermetallic precursors, bandgap grading using some elements such as Ga is problematic due to apparent interface segregation.[22]

Process speed and feedstock and capital equipment costs are important issues of manufacturability. Recently, 12% device efficiency has been demonstrated using CIGS absorber layers for which the total deposition time using the evaporative process is about 6 minutes.[23] If the process speed is sufficient, the number or length of deposition chambers is reduced, and thus also the cost of capital equipment is minimized compared to a slower deposition process.



"Exterior Se oven"



"line of sight"

**Figure 5.4.1-1** Schematic representation of alternate methods of selenium delivery;  
*a. Exterior delivery to the chamber. (upper view)*  
*b. "Line of sight" delivery within the chamber. (lower view)*

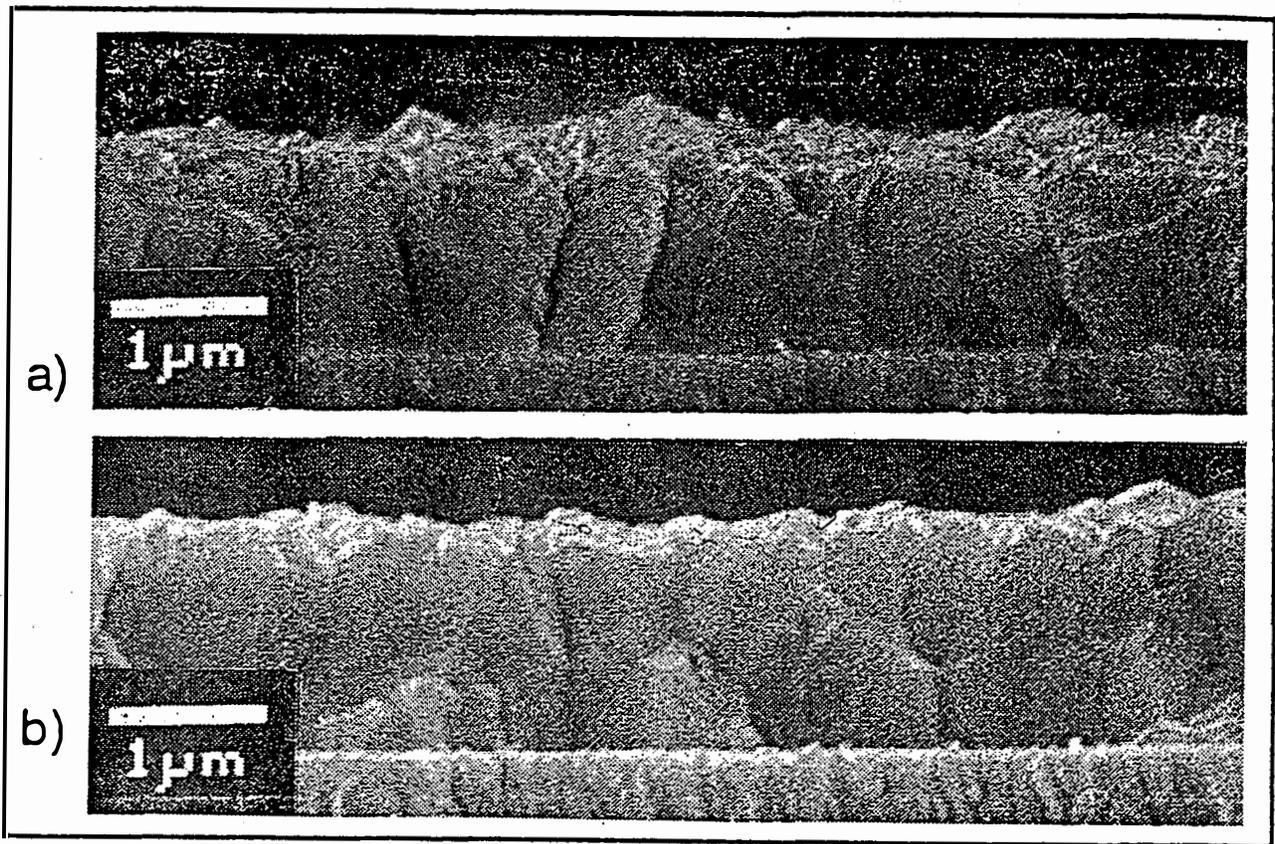


Figure 5.4.1-2 Cross-Section SEM micrographs of :  
a. CIGS formed by sequential sputtering.  
b. CIGS formed by sequential evaporation.

Moreover, capital cost is reduced since separate, dedicated chambers are not needed for each layer or element. Rather than multiple, separate chambers for several elements and steps, only one chamber is required for deposition of all elements and selenization, completing the absorber layer. Further, all high temperature processes are restricted to this one chamber. The starting feedstock materials for this type of process are pure metals, without requirement for feedstock fabrication, and are thus in their least expensive form.

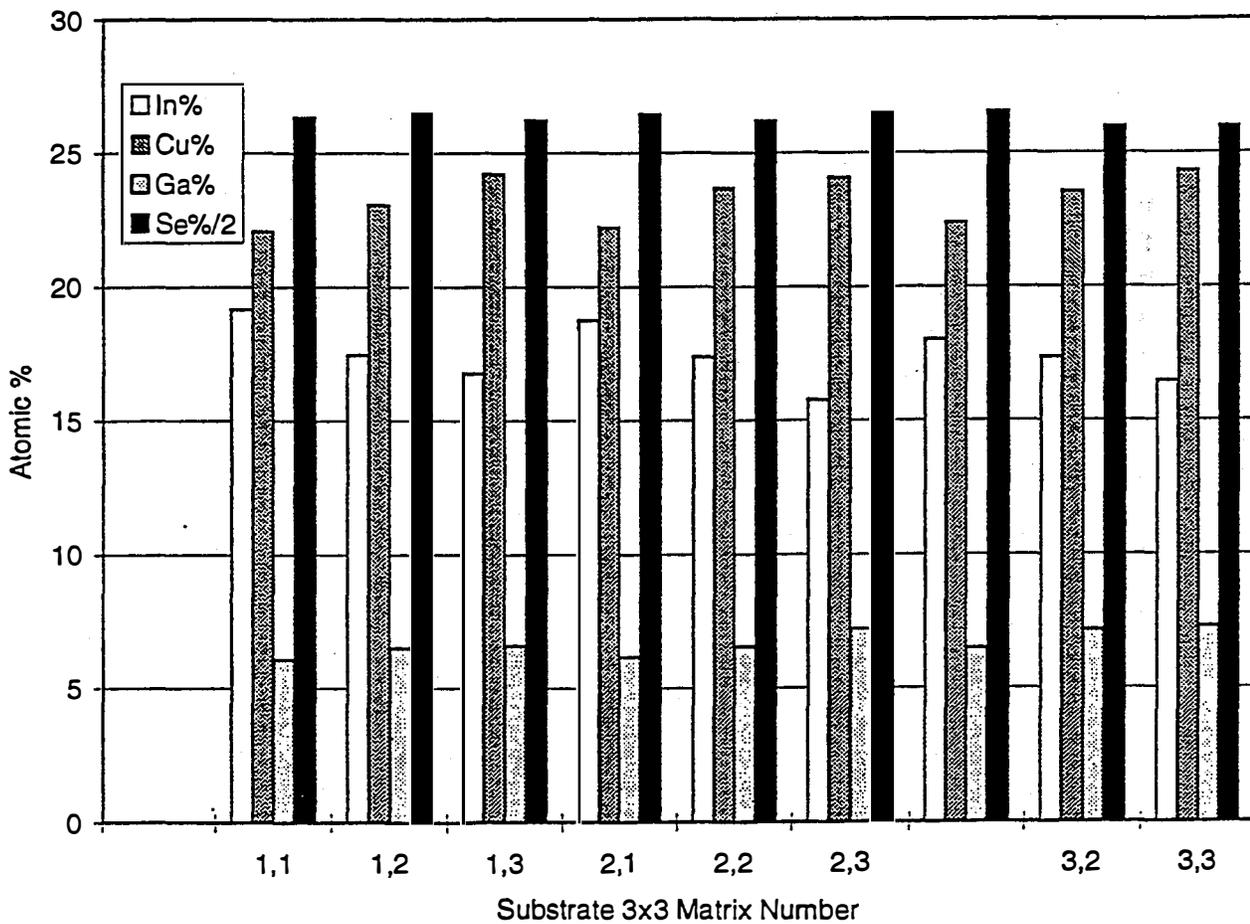
For evaluation of evaporative processes, we have constructed a system for square foot substrate areas using custom designed sources for each element. Many different “recipes” can be used in this system and our objective is to realize high quality results over the largest possible areas without losing sight of such factors as deposition times, reproducibility, and material yields.

For reasons of greater experimental flexibility, the preferred substrate size is 3”x3” and in order to demonstrate large area capabilities we simply use a number (usually nine, covering an area over 500 cm<sup>2</sup>) of 3”x3” substrates in a single deposition run.

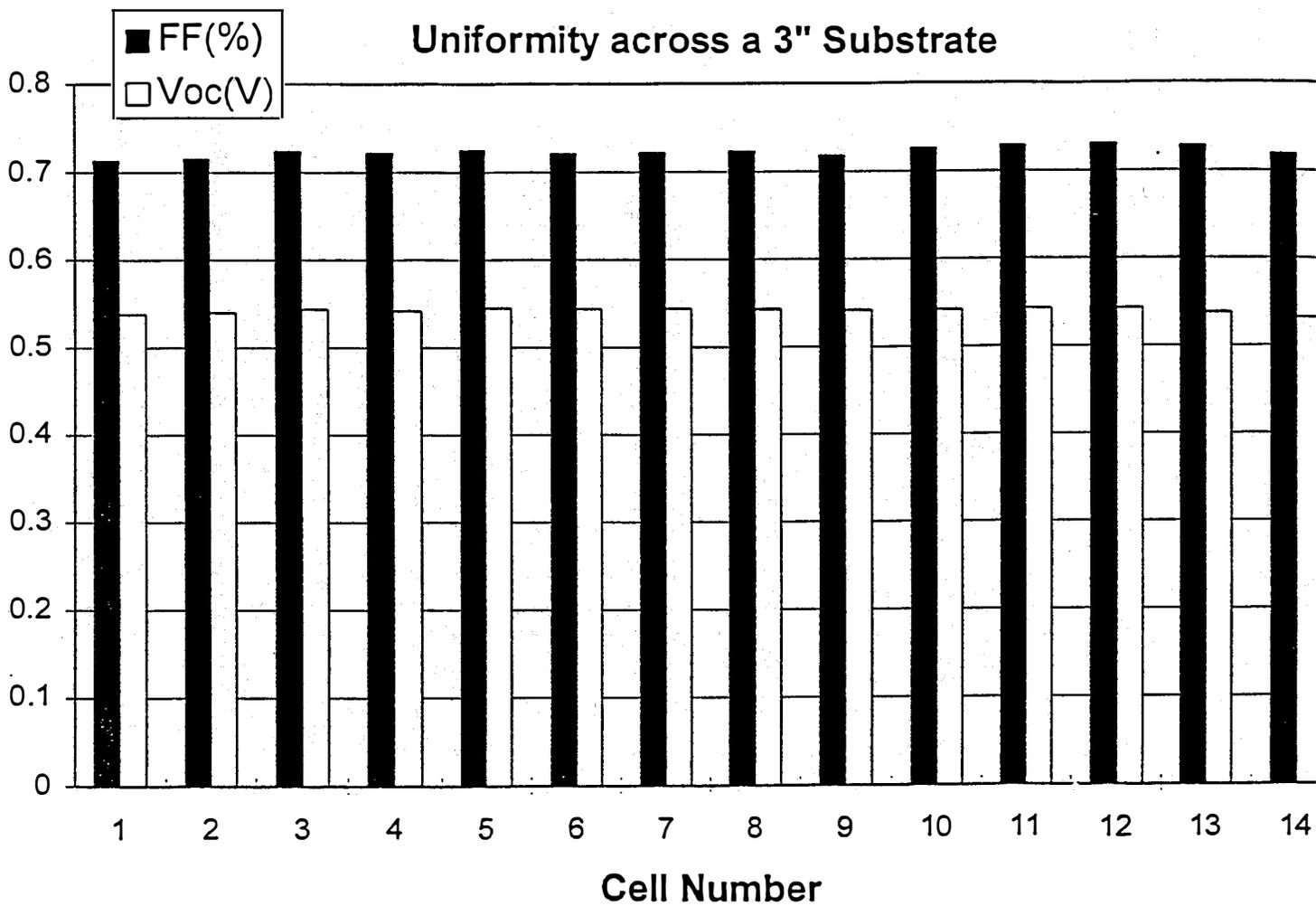
### **5.4.3 Spatial Uniformity of CIGS Absorber Layers**

Compositional uniformity is checked using energy dispersive analysis of x-rays (EDAX). As our electron microscope equipment only allows us to measure small samples (less than one square inch) we usually physically cut corners off from the substrates for this analysis. For depositions containing single 3”x3” substrates, the uniformity can be such that the EDAX measurements on the four corners of the substrate are within the experimental indetermination (~0.5%). When nine 3”x3” substrates are used in a single deposition, they are arranged in a 3x3 matrix and are numbered using the standard matrix notation. Their typical compositional uniformity is as shown by the example in figure 5.4.3-1. The influence of the spatial compositional variations on the cell behaviors is then given by a recipe dependent relationship, a “good” recipe being able to tolerate the various compositions.

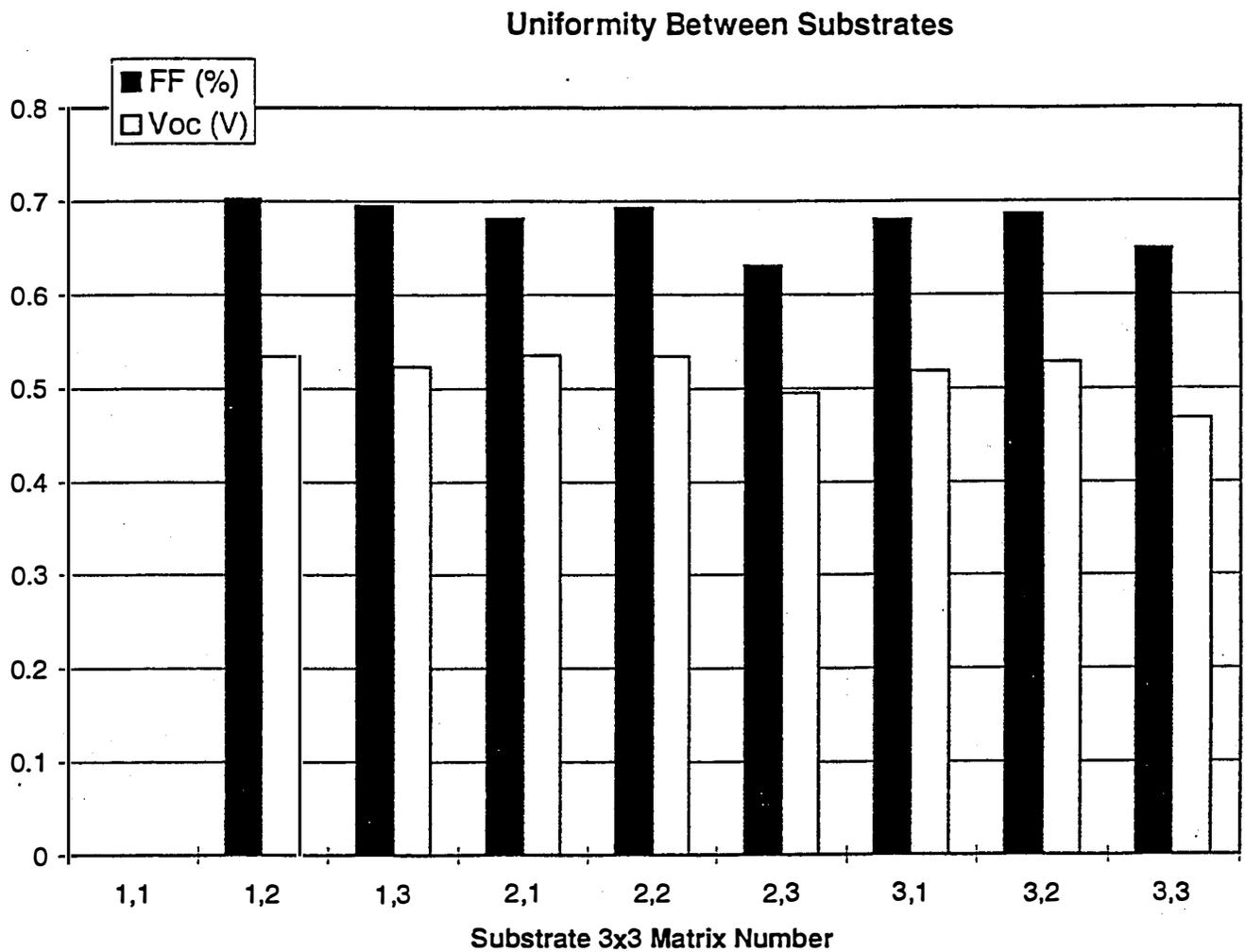
In order to examine the variations of cell behavior across a 3”x3” substrate we use a matrix of 84 (six rows of 14) small area (~0.4 cm<sup>2</sup>) cells to measure the photovoltaic parameters (Voc, Jsc, and FF) as well as to localize “defects” that are not part of the continuous spacial trend. We find that across most 3”x3” substrates, with the exception of a few random shunted cells, the photovoltaic parameters show only minor variations. An example is given in figure 5.4.3-2 where the Voc and FF uniformity across a row of 14 cells of a 3” substrate is shown, the current densities of these are all close to 31 mA/cm<sup>2</sup>, giving total area efficiencies around 12%. When nine 3”x3” substrates are used in a single deposition, the cell parameter uniformity can be as shown in the example in figure 5.4.3-3 (eight substrates only: one was lost in the processing) where the average Voc and FF for each substrate is given as a function of its position. These averages are based on about 90% of the cell population, the 10% loss being due to imperfect handling or being shorted cells that exhibited Voc values less than 100 mV. As complementary information, the total spread of the efficiencies for the population of the cells used in figure 5.4.3-3 is given in figure 5.4.3-4.



**Figure 5.4.3-1** Compositional uniformity shown by measurement of nine 3"x3" substrates. The absorber layer was deposited onto all nine substrates concurrently in a single, typical CIGS deposition. The position of each substrate is denoted using standard matrix notation.

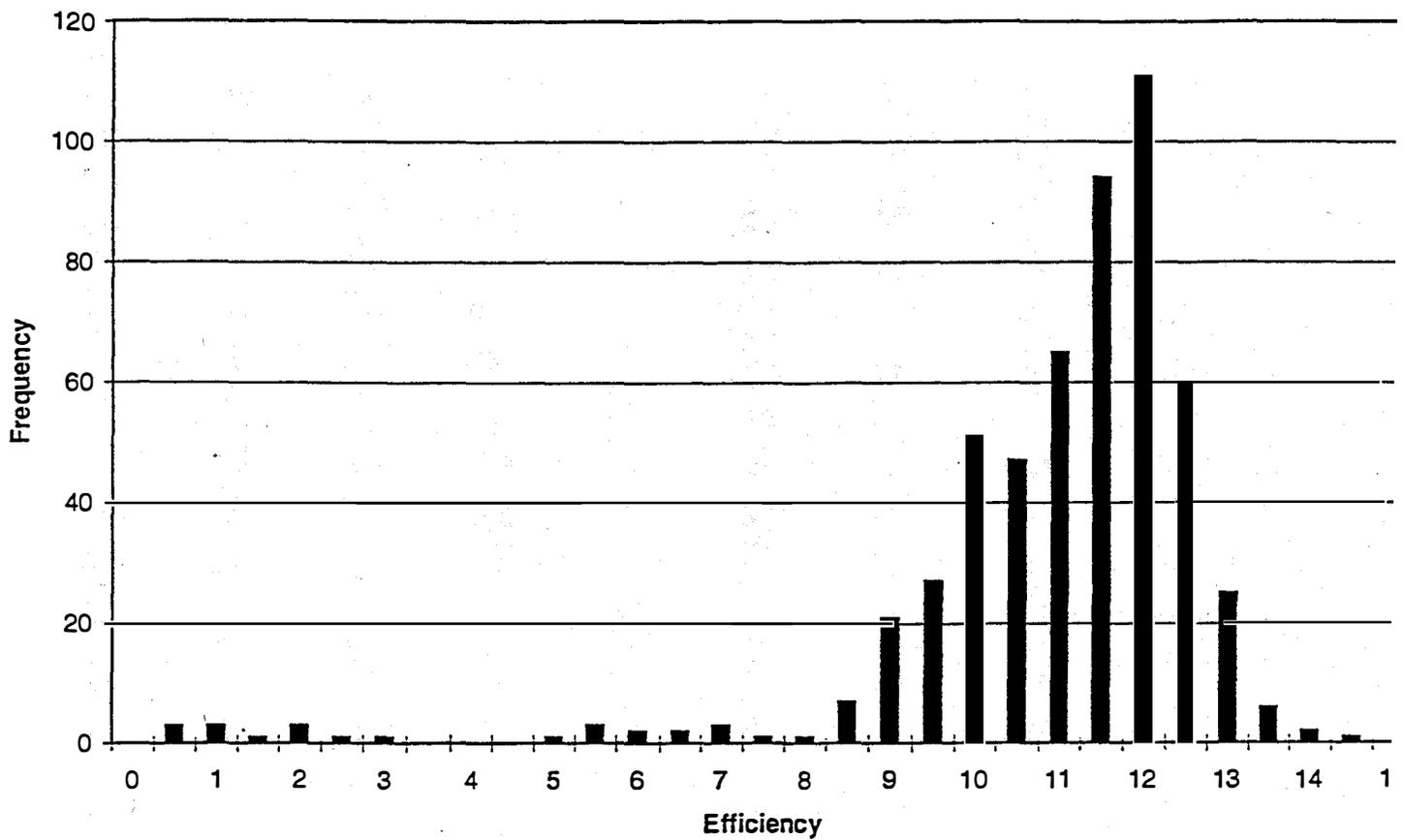


**Figure 5.4.3-2** *Spatial uniformity of device performance, showing Voc and fill factor for 14 adjacent devices across a 3" substrate.*



**Figure 5.4.3-3a** *Uniformity of device performance between substrates, showing average Voc and average fill factor for devices on each of eight (3"x3") substrates made in a single absorber layer deposition. One 3"x3" substrate was lost in processing. The data represents an average of about 65 devices per substrate.*

**Total Area Efficiency Distribution**



**Figure 5.4.3-3b** *A frequency histogram of the device efficiency of the population shown in Figure 5.4.3-3a. This histogram represents a total population of greater than 500 small area devices measured on the eight 3"x3" substrates.*

#### **5.4.4 Control and Reproducibility of CIS Deposition**

Adequate control and reproducibility of the deposition process is critical to manufacturability. The process variables which bear most strongly on reproducibility and control are deposition thicknesses, flux rates of constituents, and substrate temperature during absorber layer formation. The effects of variation in these parameters are apparent in the final elemental composition of the film and the photovoltaic performance of the resultant product. Figure 5.4.4-1 shows the run to run variation in composition for a sequence of several depositions in one system. The plot of the atomic concentration of Cu, In and Ga shows reasonably good control, although improvement is expected due to system modifications presently under implementation. A more discriminating measure of reproducibility is device performance, which is shown in Figure 5.4.4-2 for another series of sequential runs. In this figure, the open circuit voltage, fill factor and efficiency of the best device resulting from each run is plotted. Much progress has already been made in understanding the sources of deposition variance. The origins of this variation are presently being addressed through improved design and instrumentation of deposition equipment.

## Run to Run Variation in Composition (Cu, In and Ga)

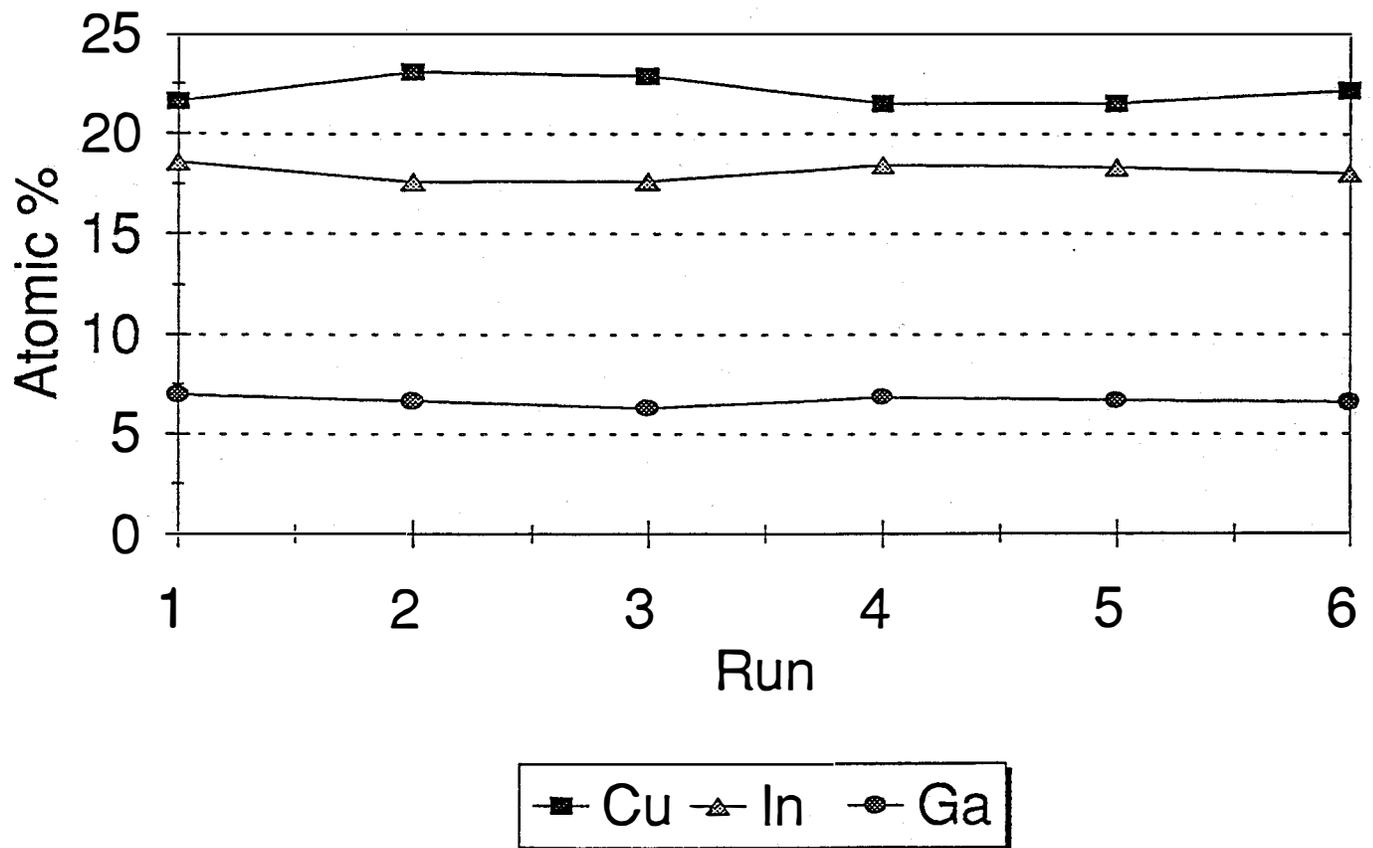


Figure 5.4.4-1 A plot of absorber layer composition for six consecutive runs having the same deposition parameter settings showing typical run to run variation.

## Run to Run Variation in Voc, Fill Factor and Efficiency

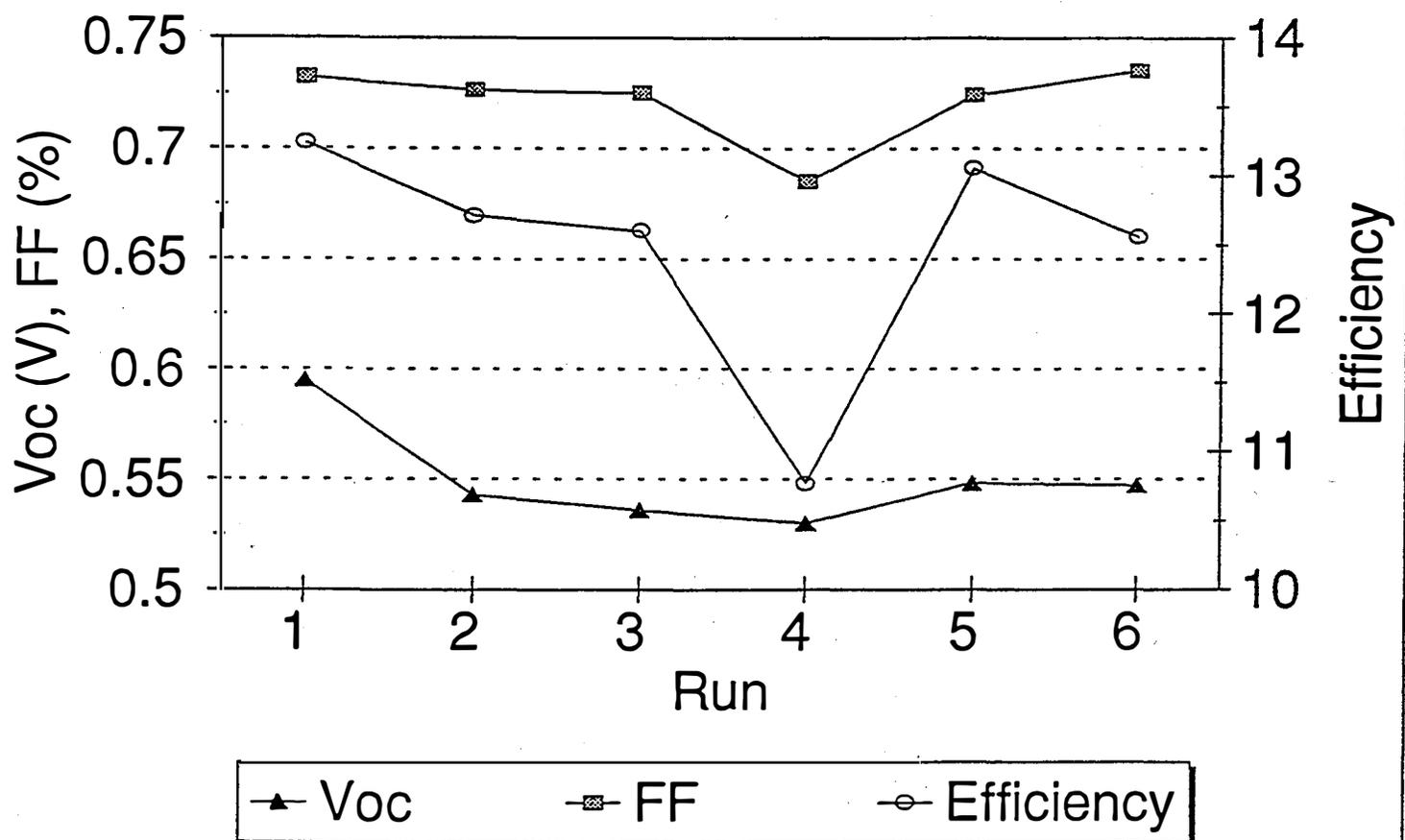


Figure 5.4.4-2 A plot of the highest device efficiency, Voc and fill factor for six consecutive absorber layer depositions showing run to run variation.

#### **5.4.5 Robustness and Process Tolerance of Variability**

Some degree of variation in processing is inevitable. In a manufacturing environment, process tolerance to this variation is desirable as this normally translates to a yield advantage over a less tolerant process. The efficiency of CIS based cells and modules is strongly dependent on the electronic properties of the absorber material [24,25] which in turn depends on factors such as composition [26,27]. Several groups have demonstrated that good device performance can result over a fairly wide range of composition in CIS. For instance, device efficiencies above 12% have been obtained despite variation in the Cu/In ratio from 0.80 to 0.95 for pure CIS [15,28]. It has also been shown that the addition of elements such as Ga and sulfur may further extend the compositional range over which good PV performance results. [22,29]

We have demonstrated deposition processes which evidence a very wide process window in terms of composition. For example, small area devices having a Cu/(In+Ga) ratio of 0.90 and 0.75 showed AM1.5 efficiencies of 10.8% and 11.5% respectively. These same processes also appear to be tolerant in terms of the effect of compositional variation on absorber layer adhesion and shunting.

### **5.5 Module Processing**

#### **5.5.1 Module Scribing Improvements**

Module scribing operations are central to achieving efficient delivery of power from a large area module. Power is lost due to the introduction of shunt and series resistances as a module is patterned to form monolithically interconnected segments. Some of the series resistance in the module is intrinsic to the diode junction itself, additional resistance originates in the lateral resistivity of the front and back contacting layers and resistivity present in the module interconnects. Figure 5.5.1-1 shows the I-V characteristic of a module segment and that of an individual device made on that segment. It is apparent that the efficiency of the segment is severely reduced by series resistance, very little of which can be accounted for in the front and back contacting layers. Rather, this resistance is mostly due to the interconnect. These interconnects were made using a mechanical scribe adjacent to the substrate scribe which exposes the back Mo contact of the segment. The ZnO top electrode of the preceding segment makes electrical contact through this opening. Substantial resistance could exist at the interconnect due to interfacial contact resistance between the ZnO and Mo electrodes in the interconnect scribe, possibly associated with the formation of a MoSe<sub>2</sub> layer on the Mo. We believe, however, that the largest contribution to interconnect resistance may be due to a lack of step coverage by the ZnO over the edge of the interconnect scribe. Figure 5.5.1-2 shows an SEM micrograph of an interconnect scribe, with notable appearance of voids in the ZnO coverage which could raise resistance. We have modified our scribing operations to minimize this effect, and we have methods under development to circumvent the difficulty altogether.

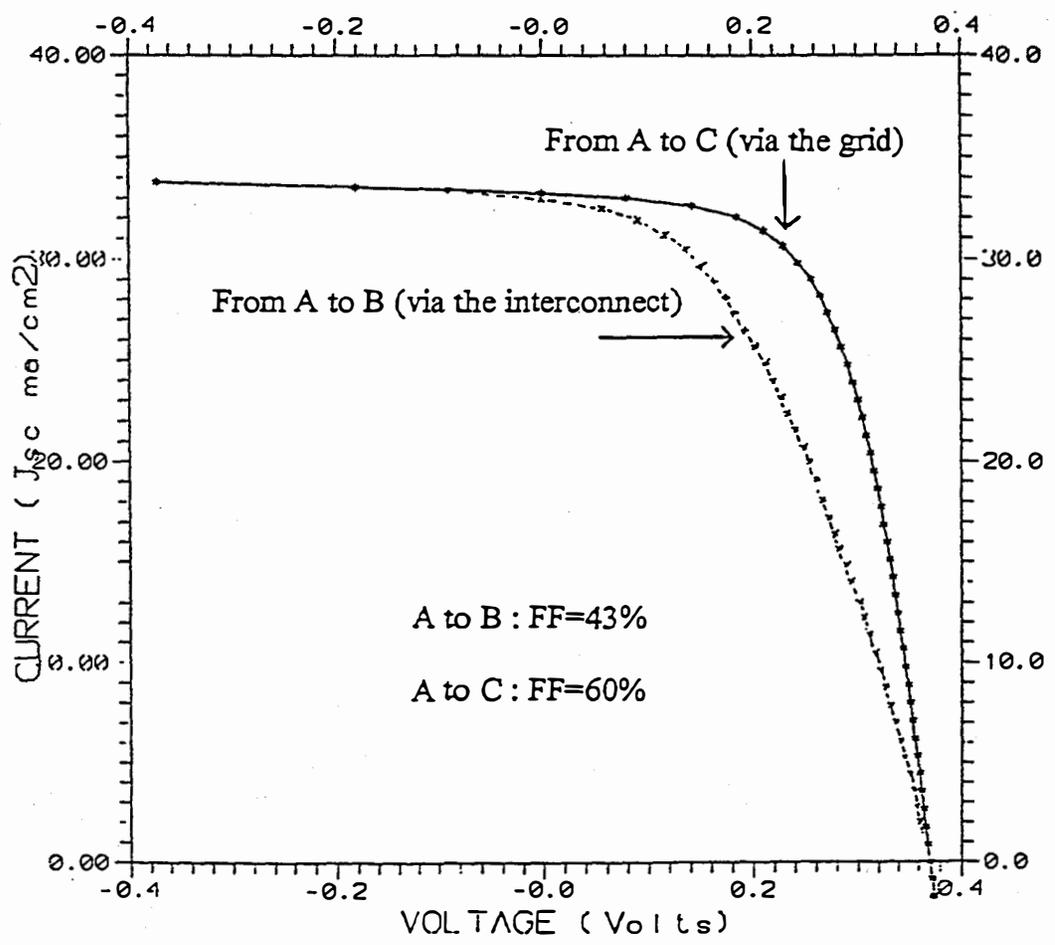
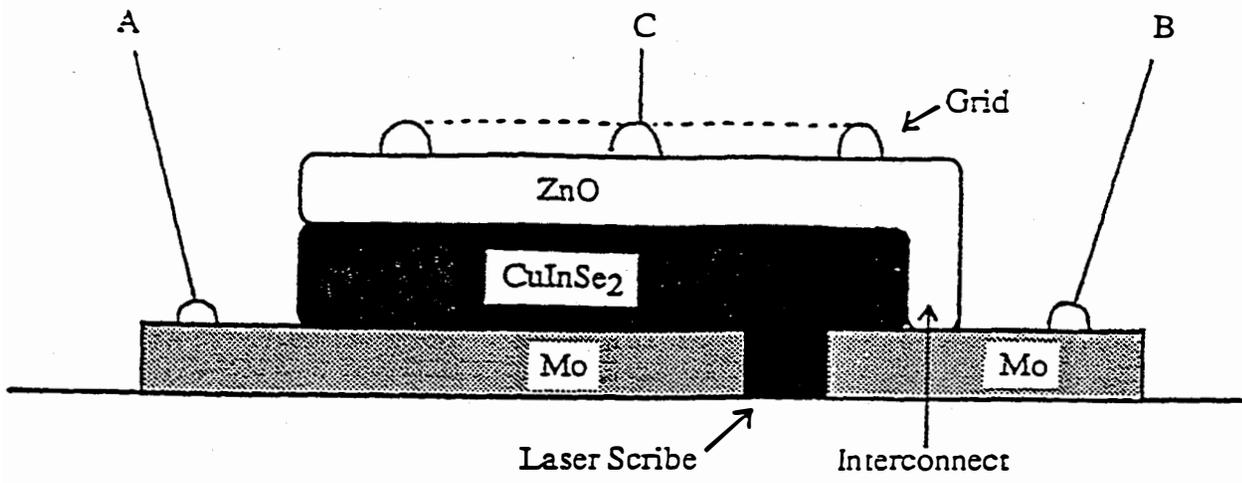


Figure 5.5.1-1 A schematic view and resulting J-V measurement of a module segment made by connecting either through a top grid or a serial interconnect.

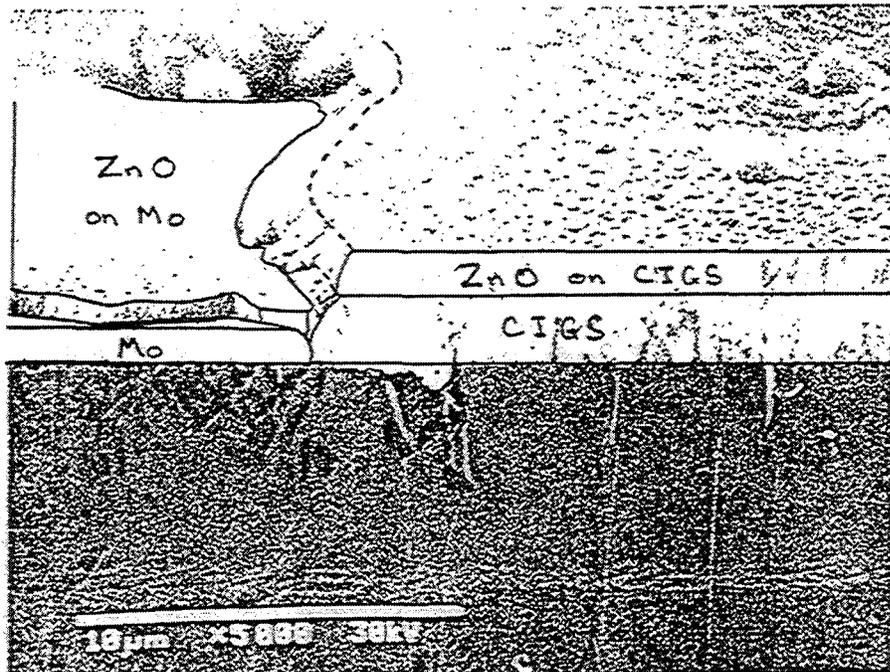
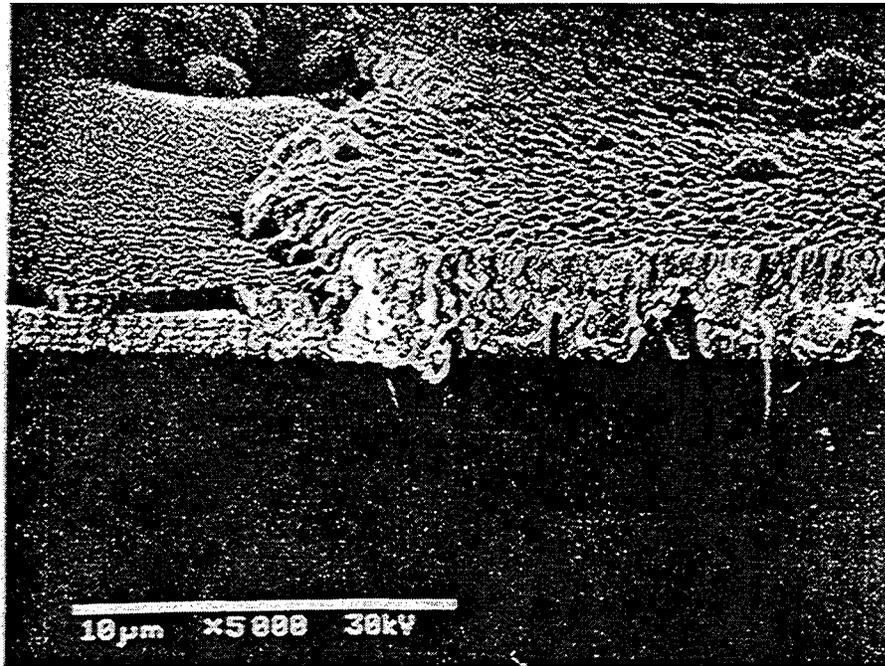
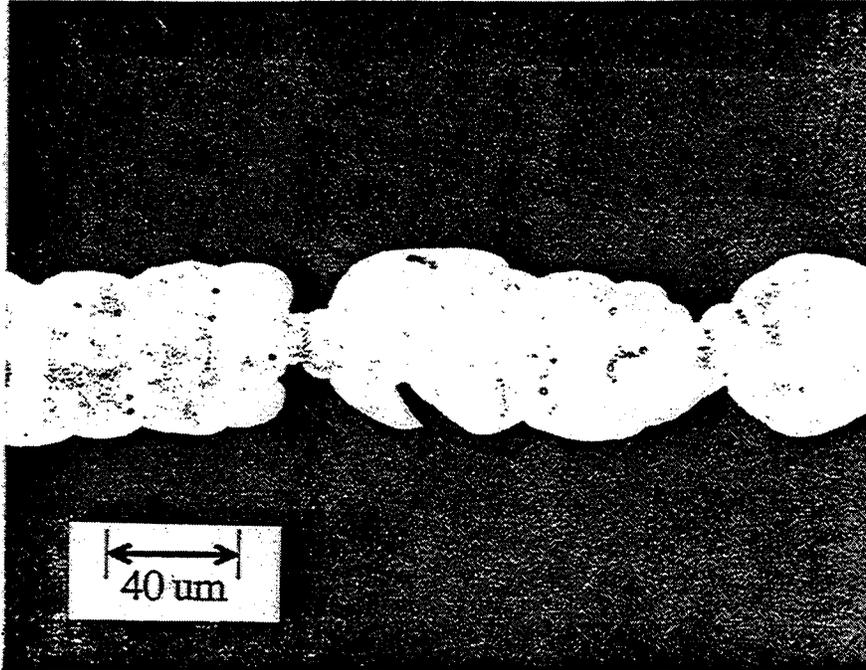
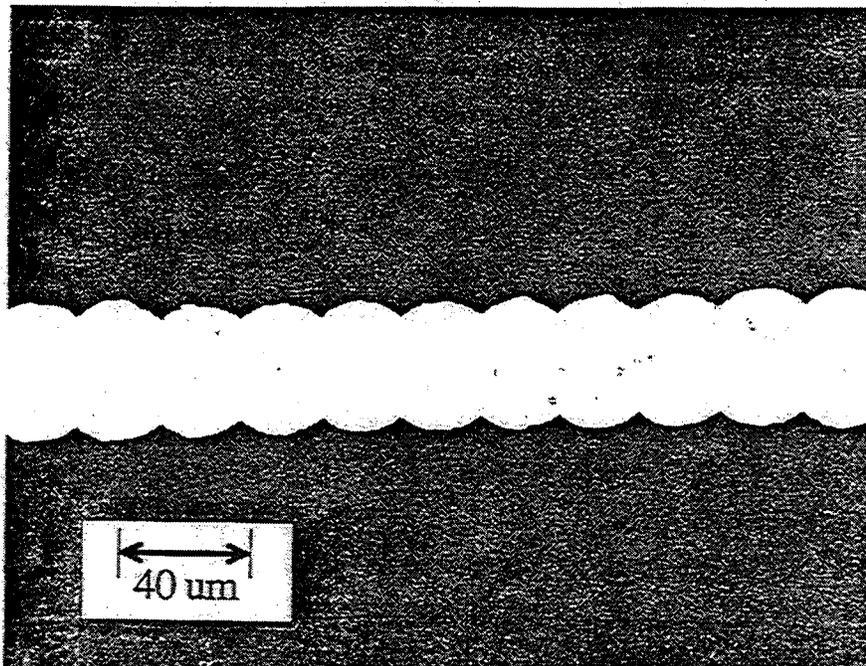


Figure 5.5.1-2 A micrograph of a module interconnect showing the ZnO coverage in the vicinity of the step over the absorber layer.



**Figure 5.5.1-3** *An optical micrograph of a defective substrate scribe showing chipping and cracking of the Mo back contact.*



**Figure 5.5.1-4** *An optical micrograph of a high quality substrate scribe showing no defects or debris generation.*

Shunt resistances also result in power losses in modules, and are often caused by particulate or debris near the substrate scribe. Figure 5.5.1-3 is an optical micrograph of a substrate scribe having irregular edges with debris, cracks and partially attached flakes of Mo near the scribe edges. These characteristics cause shunts in the finished module due to pinhole or point defects through the absorber layer. These problems have been successfully addressed through modification of laser scribing and substrate processing. The resultant substrate scribes are very clean and free of debris or flaked Mo, as shown in Figure 5.5.1-4.

## 5.6 Device and Module Results

Small area devices are, perhaps, the most important diagnostic of the aggregate PV structure and associated processes under test short of actual submodule measurements. The major milestones for this program included fabrication of small area, CIS devices having a conversion efficiency equal to or greater than 9%, 12% and 14% in phases 1, 2, and 3 respectively. The best small area devices produced at Solarex during each phase of the program is shown in table 5.6-1 below.

**Table 5.6-1**

	$V_{oc}$ (V)	Fill Factor (%)	$J_{sc}$ mA/cm <sup>2</sup>	Measured Efficiency (%)	Efficiency for Major Milestone (%)
Phase 1	0.34	56.2	31.9	6.2	9
Phase 2	0.43	64.1	37.41	10.2	12
Phase 3	0.59	73.8	32.8	14.4	14

There has, in some cases, been some discrepancy between small area cell measurements made at Solarex and those made on the same cells at NREL. Table 5.6-2 shows a comparison of cells measured at both locations. Miscalibration, measurement inaccuracy (particularly in area), and cell temperature variation existing in the solar simulator at Solarex is the most likely cause for these differences.

**Table 5.6-2**

Cell ID	Area (cm <sup>2</sup> )	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	Fill Factor	Efficiency (%)	Efficiency difference	Measurement Location
E50-4-E5	0.427	596	32.2	73.9	14.2		Solarex
	0.4192	590.0	32.80	72.90	14.1	+0.1	NREL
E50-4-E6	0.415	598	32.4	73.9	14.3		Solarex
	0.4080	588.9	32.51	72.64	13.9	-0.4	NREL
E50-4-E7	0.418	596	32.6	73.7	14.3		Solarex
	0.4101	587.9	32.26	72.18	13.7	-0.6	NREL
E50-5-E8	0.418	595	33.5	73.3	14.6		Solarex
	0.4158	586.1	32.33	71.39	13.5	-1.1	NREL
E50-5-F5	0.422	592	34.7	73.9	15.2		Solarex
	0.4202	586.5	32.49	71.83	13.3	-1.9	NREL
E50-4-F6	0.420	596	33.7	73.2	14.7		Solarex
	0.4117	586.8	32.68	72.52	13.9	-0.8	NREL
E50-4-F7	0.418	596	33.9	74.2	15.0		Solarex
	0.4097	587.1	32.83	72.78	14.0	-1.0	NREL
E50-4-F8	0.420	597	34.9	74.0	15.4		Solarex
	0.4102	585.9	33.53	72.81	14.3	-1.1	NREL
E50-4-F9	0.420	581	34.2	55.1	10.9		Solarex
	0.4102	580.5	33.25	68.00	13.1	2.2	NREL

The light and dark I-V characteristic of the best small area cell made at Solarex is shown in Figures 5.6-1 and 5.6-2 respectively. It should be noted that all small area cells made at Solarex, including this one, have not been optimized for small area performance, per se, by using very thin or highly resistive ZnO front contact. Rather, the ZnO front contact which is used is appropriate for module use, typically having a sheet resistivity of 15 ohms/square or less, and thus is non-optimal for small area devices. The improvement in small area device performance during the program has resulted somewhat from improved window and contact layers, but is mostly due to improved absorber deposition processes.

# solarex CIGS

Sample: E66-3 D5

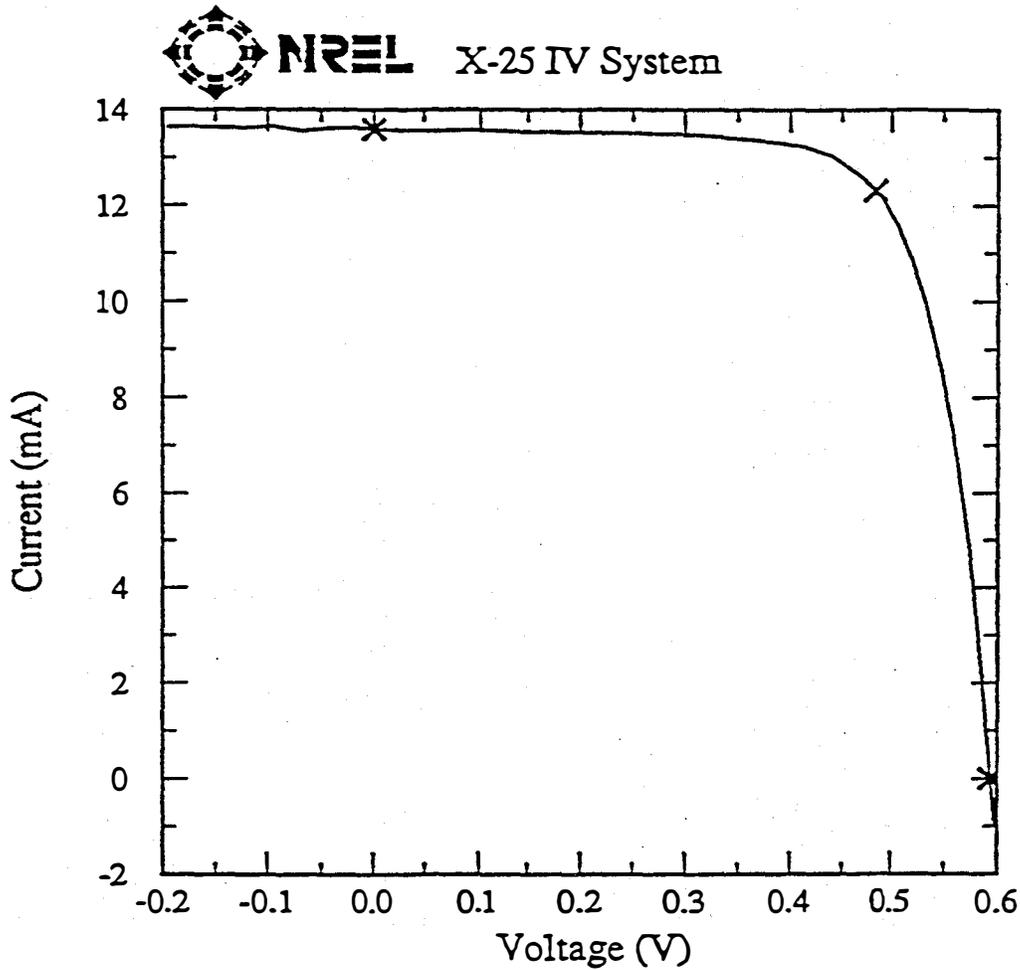
Nov 17, 1994 10:39 AM

ASTM E 892-87 Global

Temperature = 25.0°C

Area = 0.4140 cm<sup>2</sup>

Irradiance: 1000.0 Wm<sup>-2</sup>



$$V_{oc} = 0.5938 \text{ V}$$

$$I_{sc} = 13.60 \text{ mA}$$

$$J_{sc} = 32.84 \text{ mAcm}^{-2}$$

$$\text{Fill Factor} = 73.76 \%$$

$$V_{max} = 0.4836 \text{ V}$$

$$I_{max} = 12.31 \text{ mA}$$

$$P_{max} = 5.955 \text{ mW}$$

$$\text{Efficiency} = 14.4 \%$$

Figure 5.6-1 The light J-V characteristic of the highest efficiency small area device.

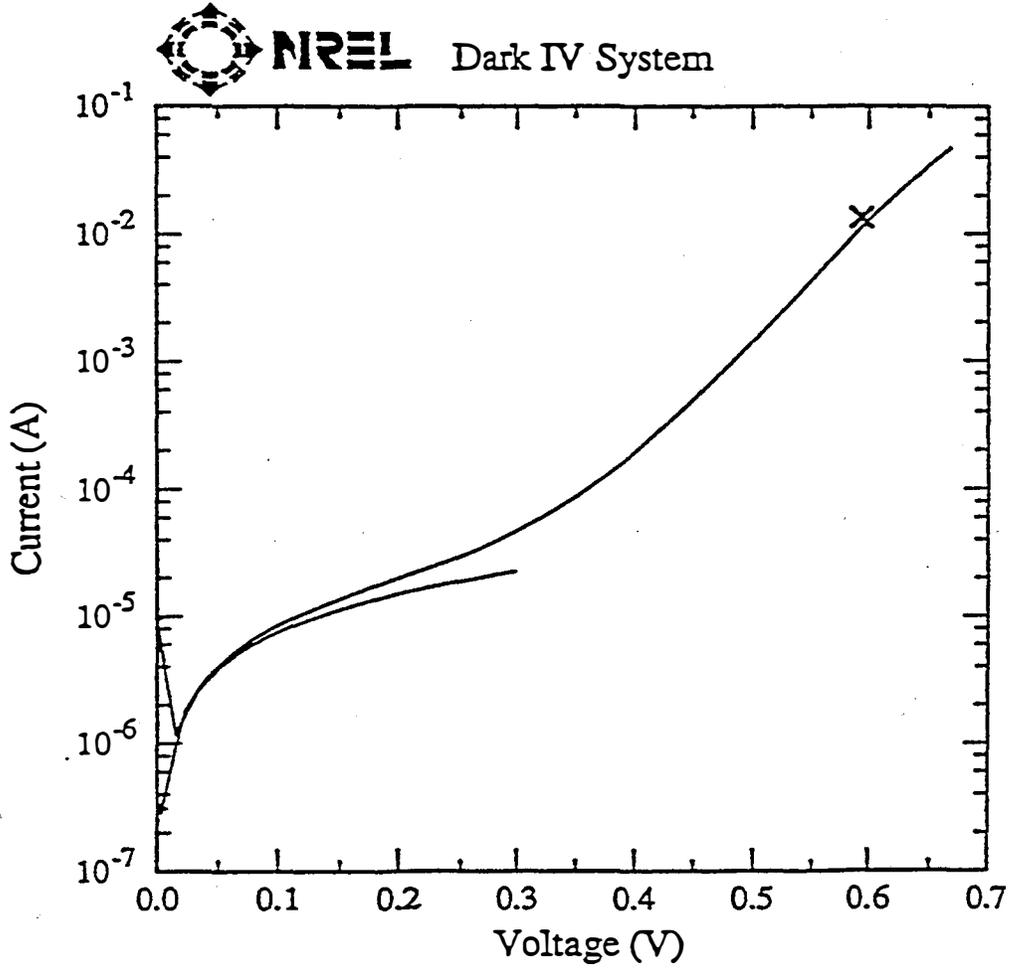
# solarex CIGS

Sample: E66-3 D5

Temperature = 25.0°C

Nov 17, 1994 10:44 AM

Area = 0.4140 cm<sup>2</sup>



$V_{\infty} = 0.5938 \text{ V}$

$R_{\text{shunt}} = 13.1 \text{ k}\Omega$

$I_{\text{sc}} = 13.60 \text{ mA}$

$R_{\text{series}} = 1.83 \text{ }\Omega$

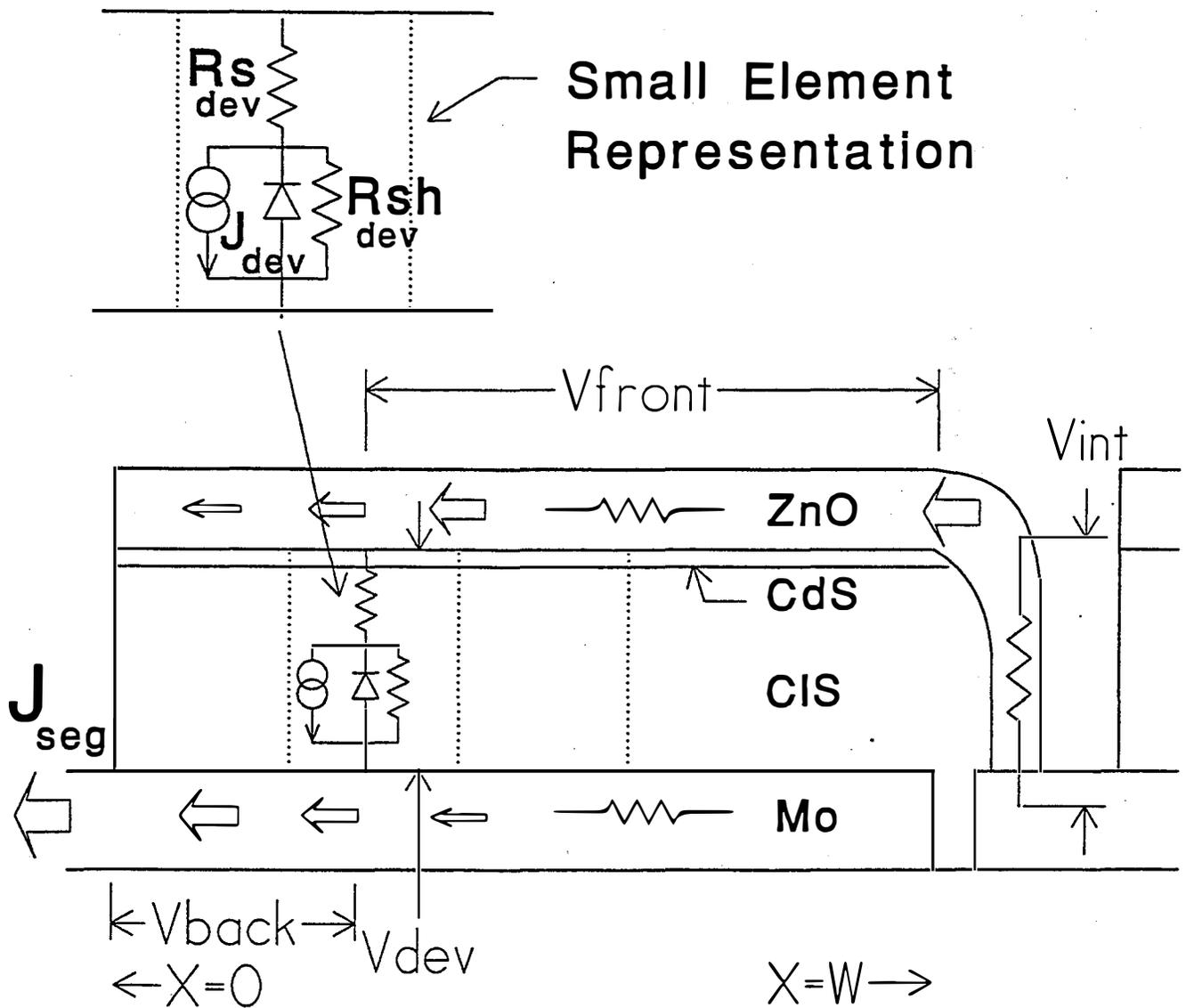
Equiv  $R_s = 0.544 \text{ }\Omega$

Figure 5.6-2 The dark J-V characteristic of the highest efficiency small area device.

### 5.6.1 Module Loss Analysis

Module losses can result from local imperfections such as pinhole shunts and regions of incomplete interconnects, or from pervasive mechanisms such as electrode contact resistivity. The former class of losses usually must be analyzed statistically, and the latter class can be understood through analytical modeling. We have started to develop a statistical base of submodule results, but it is not yet of sufficient sample size to use quantitatively. Concurrently, we have developed a model for understanding the latter class of module losses which is based on distributed current generation and collection in a module segment, through distributed resistances representing the front and back electrodes as shown in Figure 5.6.1-1. The model allows estimation of the I-V characteristic of a large area structure such as a module from the measured I-V characteristic of a small area cell on an identical substrate. The module and segment dimensions are taken as input, as well as the sheet resistivity of front and back contacts, the total interconnect width and the interconnect resistivity. The model assumes that the electrical operating point of the heterojunction varies spatially along the width of a module segment due to voltage dropped across the contacting electrodes, i.e. the front and back contacts of a module segment are not isopotential. The details of this approach are more thoroughly explained elsewhere.[30,31]

For example, figure 5.6.1-2 shows the effect on module I-V characteristic of different segment widths, interconnect resistivities and front contact sheet resistivity. The assumed small area J-V characteristic for this example also shown in that figure. For simplicity in figure 5.6.1-2, the optical transparency of the ZnO front contact is assumed to be invariant with the sheet resistivity of that contact over the range shown. The effect of total interconnect width on efficiency as a function of front contact sheet resistivity and module segment width is given by figures 5.6.1-3 and 5.6.1-4 assuming zero interconnect resistivity. The effect of interconnect resistivity on module efficiency is shown in figure 5.6.1-5, for a realistic value of interconnect width. For figures 5.6.1-3 through 5.6.1-5 the absorber/junction layers are assumed to be identical to that which produced the small area diode characteristics shown in figures 5.6.1 and 5.6.2. It is apparent that these module design factors will have significant impact on final module efficiency.



**Figure 5.6.1-1** A schematic representation of the elements and circuit assumed for module loss analysis..

# Calculated and Measured Module Segment J-V

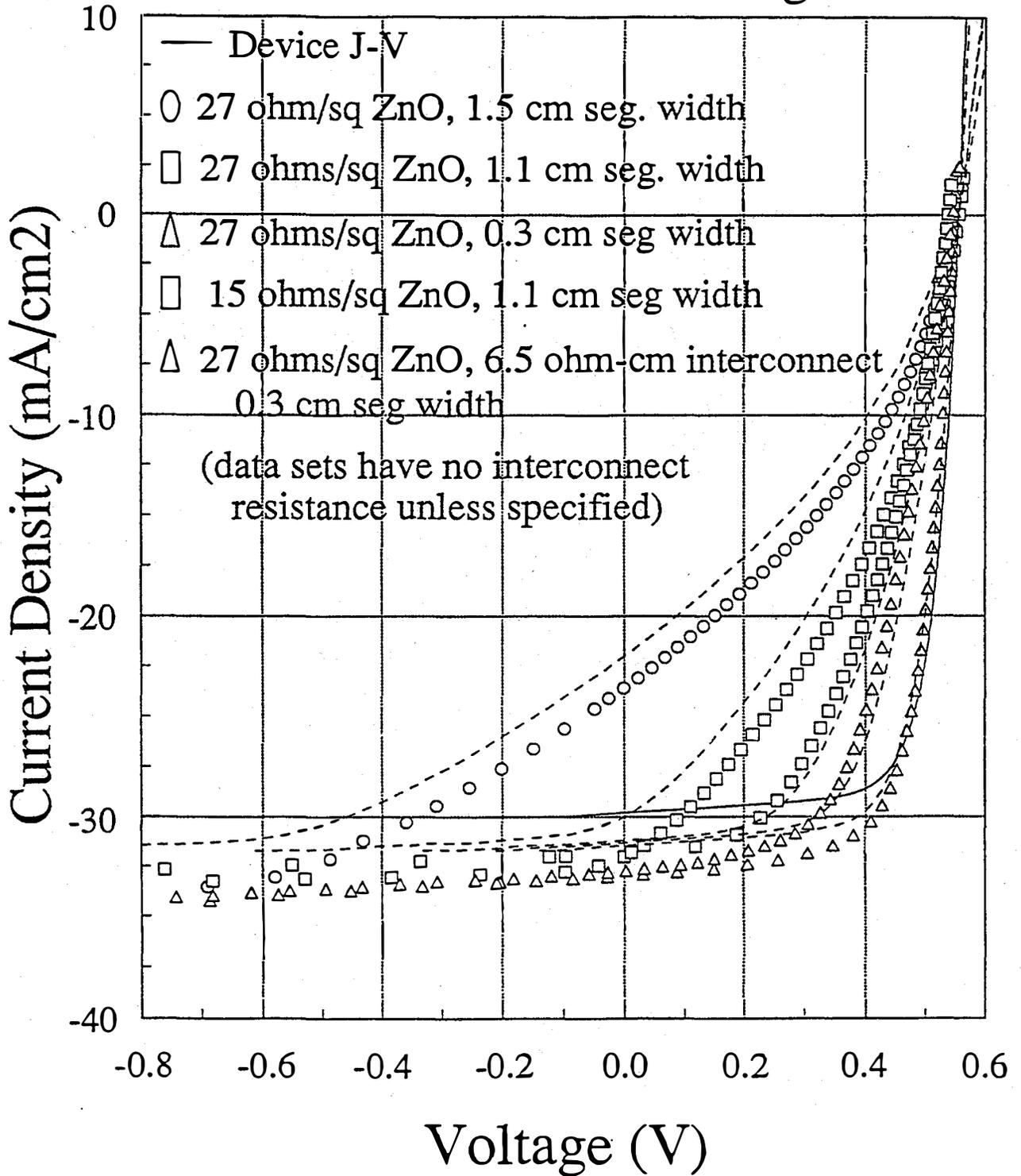
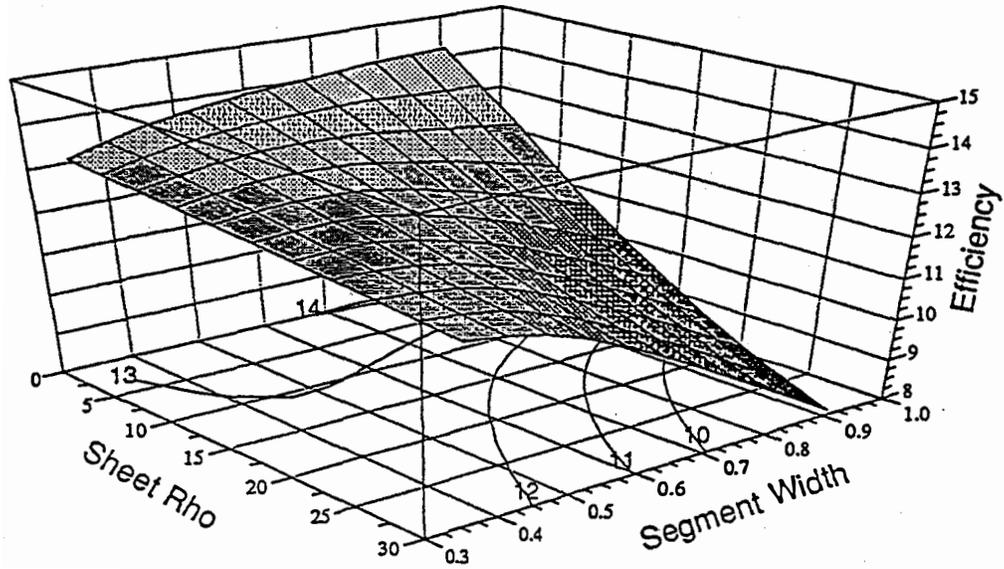
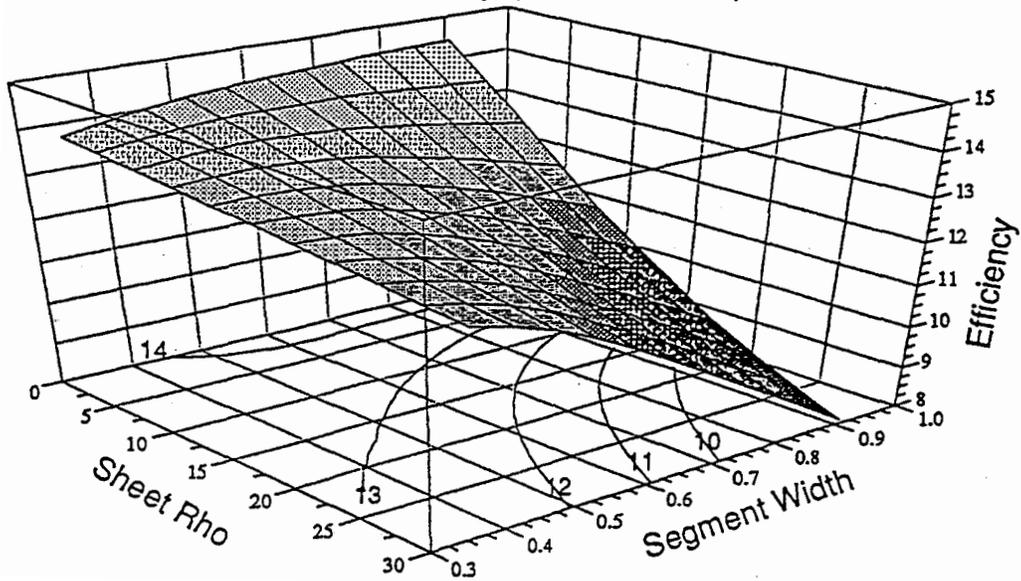


Figure 5.6.1-2 The measured (symbols) and calculated (lines) J-V behavior of a module segment using various segment widths, front contact resistivity and interconnect resistivity.

Module Efficiency (0.018" Scribe)

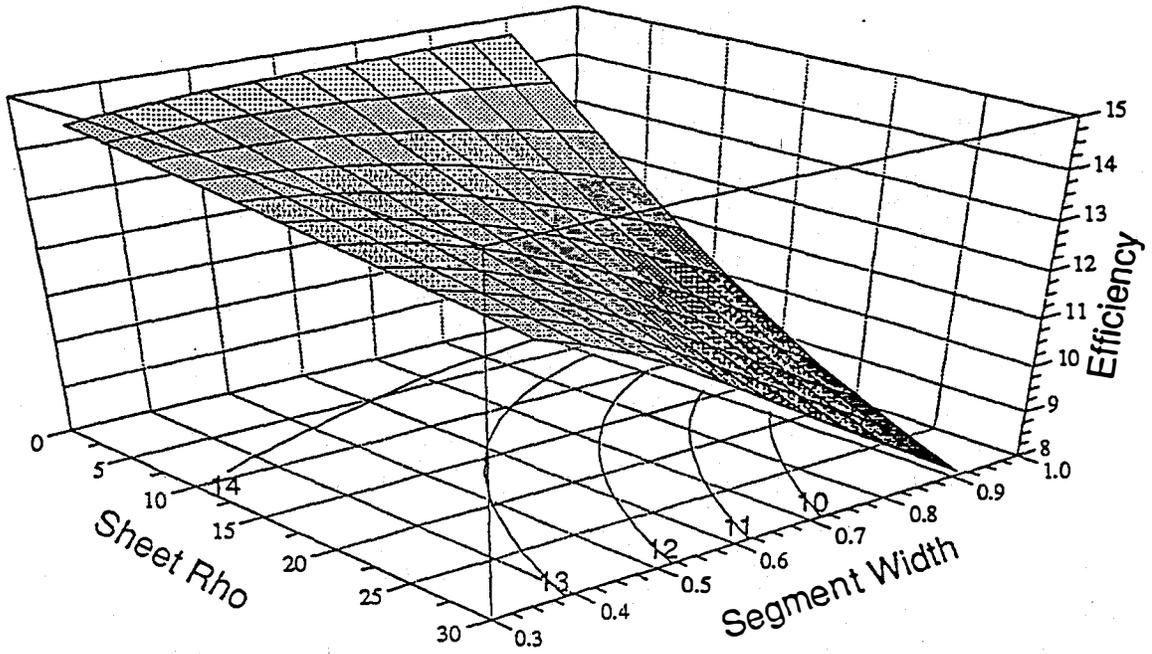


Module Efficiency (0.012" Scribe)



**Figure 5.6.1-3** The calculated module efficiency for 18 and 12 mil total interconnect width as a function of front contact sheet resistivity and module segment width.

Module Efficiency (0.006" Scribe)



Module Efficiency (0.000" Scribe)

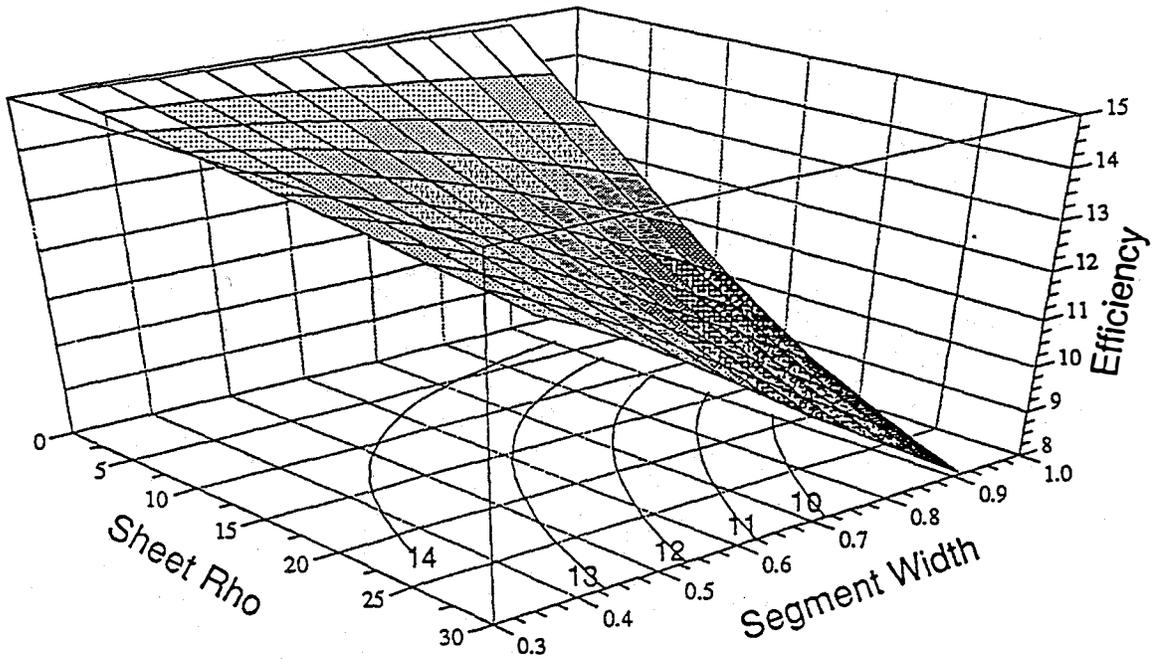
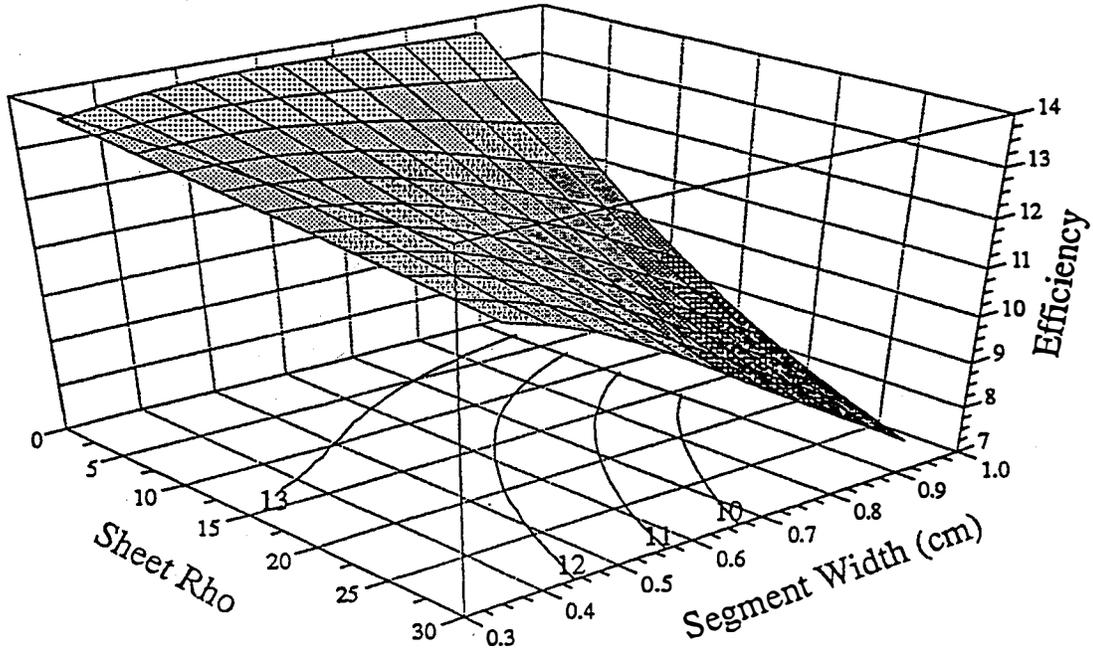


Figure 5.6.1-4 The calculated module efficiency for 6 and 0 mil total interconnect width as a function of front contact sheet resistivity and module segment width.

Interconnect: Res = 1.0 ohm-cm, width = 0.012"



Interconnect: Res = 2.0 ohm-cm, width = 0.012"

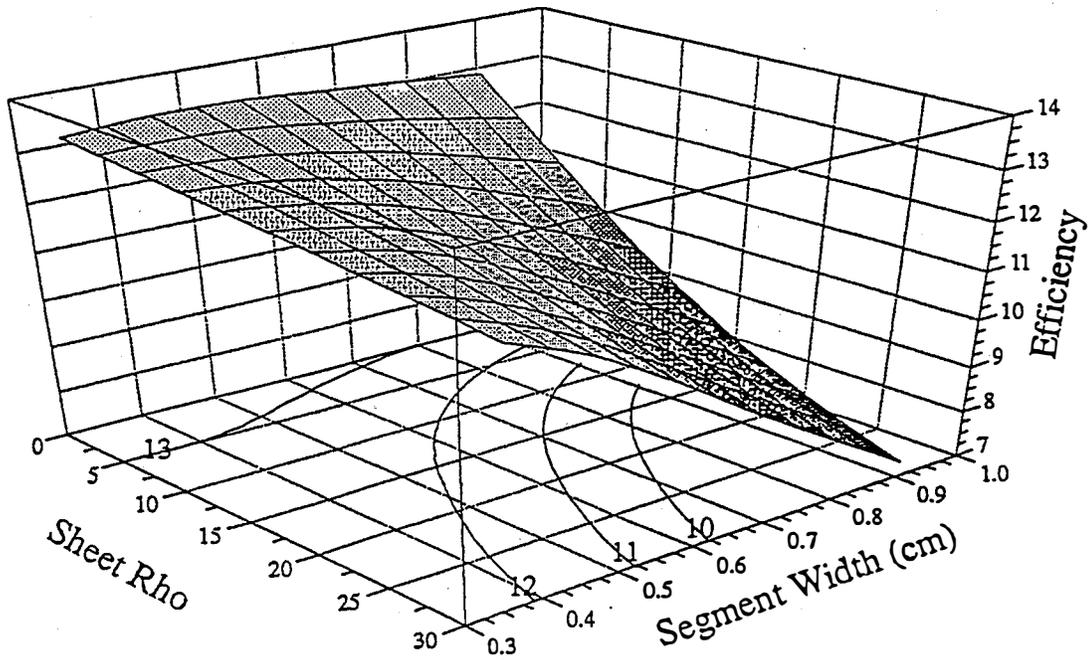


Figure 5.6.1-5 The calculated module efficiency for 1.0 and 2.0 ohm-cm interconnect resistivity (assuming 12 mil interconnect width) as a function of front contact sheet

## 5.6.2 Submodule Results

Most of the submodules made to date are suboptimal from a design point of view, according to the analysis above. Specifically, the current design uses module segments which are 0.635 cm wide, a front contact having sheet resistivity of 10 to 15 ohms/square and approximately 0.012" to 0.024" total interconnect width. The previous described analytical model indicates that a significant improvement could be expected by reducing the segment width under the present conditions, or by using a front contact having lower sheet resistivity, depending on the additional optical loss incurred. Nevertheless, the present suboptimal design has yielded submodules having an aperture efficiency exceeding 11%. Figure 5.6.2-1 shows the I-V characteristic of the best submodule produced to date. We expect further gains in aperture area efficiency primarily from optimization of the submodule design, and improvements in the absorber process, sheet resistivity and optical transparency of the ZnO front contact and reduction of resistivity and total width of the interconnect.

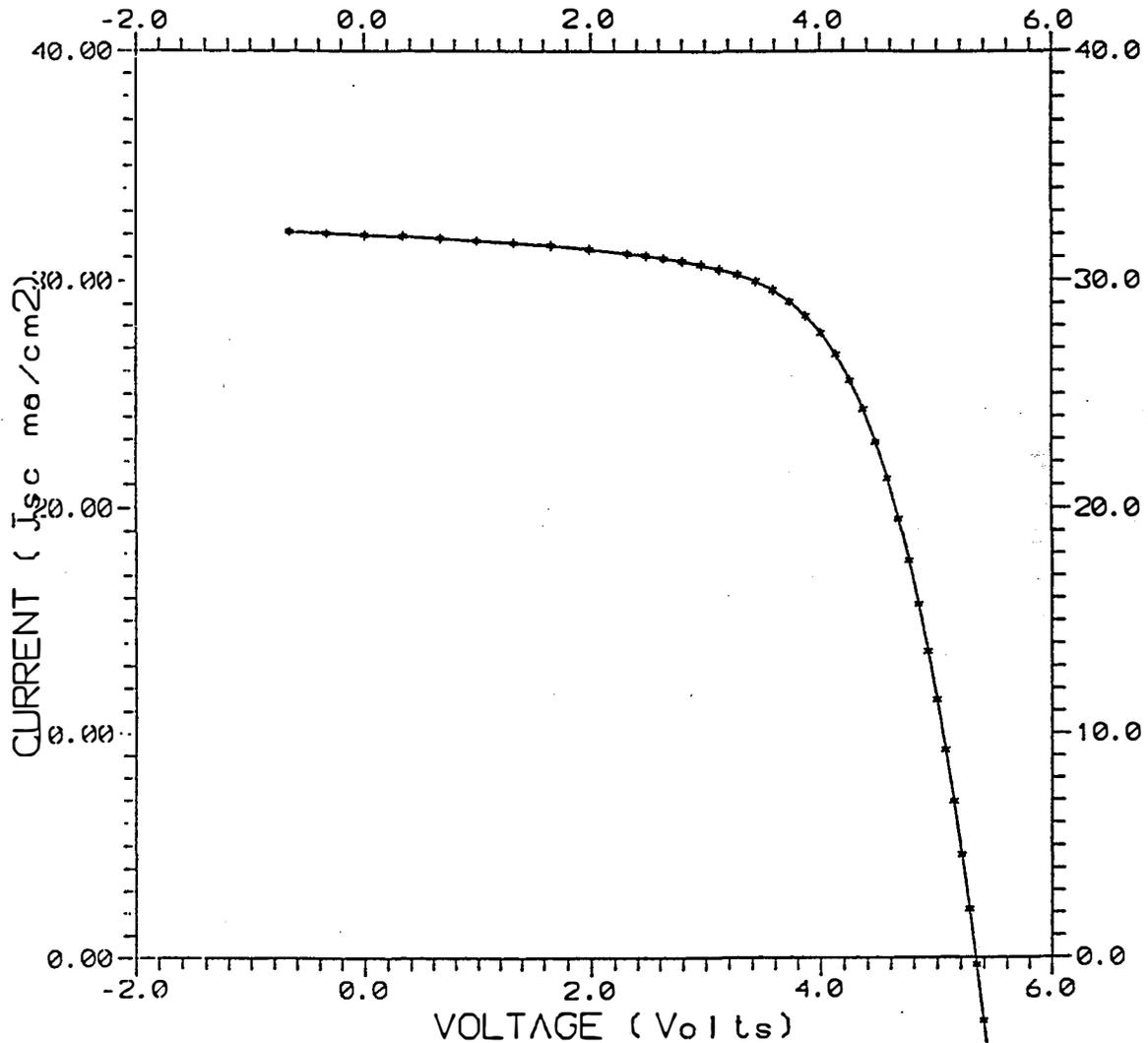
We are presently using at least one process for module fabrication which appears to be particularly tolerant of substrate and scribe imperfections, and fairly resistant to shunt formation in the finished module. This is expected to be of major importance in terms of manufacturing yield. As explained in earlier sections, this is mostly due to aspects of absorber layer formation and improvement of scribing processes. Although the entire I-V characteristic of an individual module segment is not easily accessible, the Voc of individual module segments can be measured easily on an unencapsulated module. The Voc of each segment is sensitive to the presence of shunts anywhere in that segment. In many cases, a submodule exhibits nearly constant Voc's on all individual segments of a 20 segment module, implying a complete absence of severe shunts in any of the segments. This result is not atypical for the present process.

## 5.6.3 Submodule Encapsulation

The encapsulation which has been used on CIS based submodules made at Solarex comprises a glass-to-glass seal made using ethylene vinyl acetate (EVA). The EVA is supplied as a transparent, flexible sheet between 10 and 40 mils thick. It is cut to size, inserted between the active face of the nude module and a cover sheet of glass and permanently laminated using vacuum, heat and pressure. Typically "water-white" low iron soda lime glass or a borosilicate glass is used rather than ordinary soda lime for the cover sheet because it has better optical transparency in the near infrared wavelengths.

The volume of systematic study which has been carried out on encapsulation is not yet large enough to allow statistical analysis of effects. Qualitatively, it has been observed that performance changes can occur due to the lamination process. It appears that high efficiency submodules usually exhibit no change in efficiency upon encapsulation, and that lower efficiency submodules often exhibit an increase in efficiency. When an increase in efficiency is evidenced, lamination primarily affects fill factor, but, open circuit voltage and short circuit current often increase as well. Figure 5.6.3-1 shows the J-V characteristic of a submodule showing this effect. The origin of this change is not yet well understood, but is suspected to involve spontaneous shunt formation or elimination. More recently produced submodules incorporate improvements

which have been implemented in other processes, specifically substrate scribing and interconnect formation. The improvements in these processes are designed to further minimize shunt problems, both before and as a result of encapsulation.



**Figure 5.6.2-1** The J-V characteristic for a 40.6 cm<sup>2</sup> monolithic submodule comprised of 10 segments, having the following parameters (at 25 °C, 100 mW/cm<sup>2</sup> illumination):

V <sub>oc</sub>	535 mV/segment
J <sub>sc</sub>	31.9 mA/cm <sup>2</sup>
Fill Factor	64.9 %
Efficiency	11.1 %

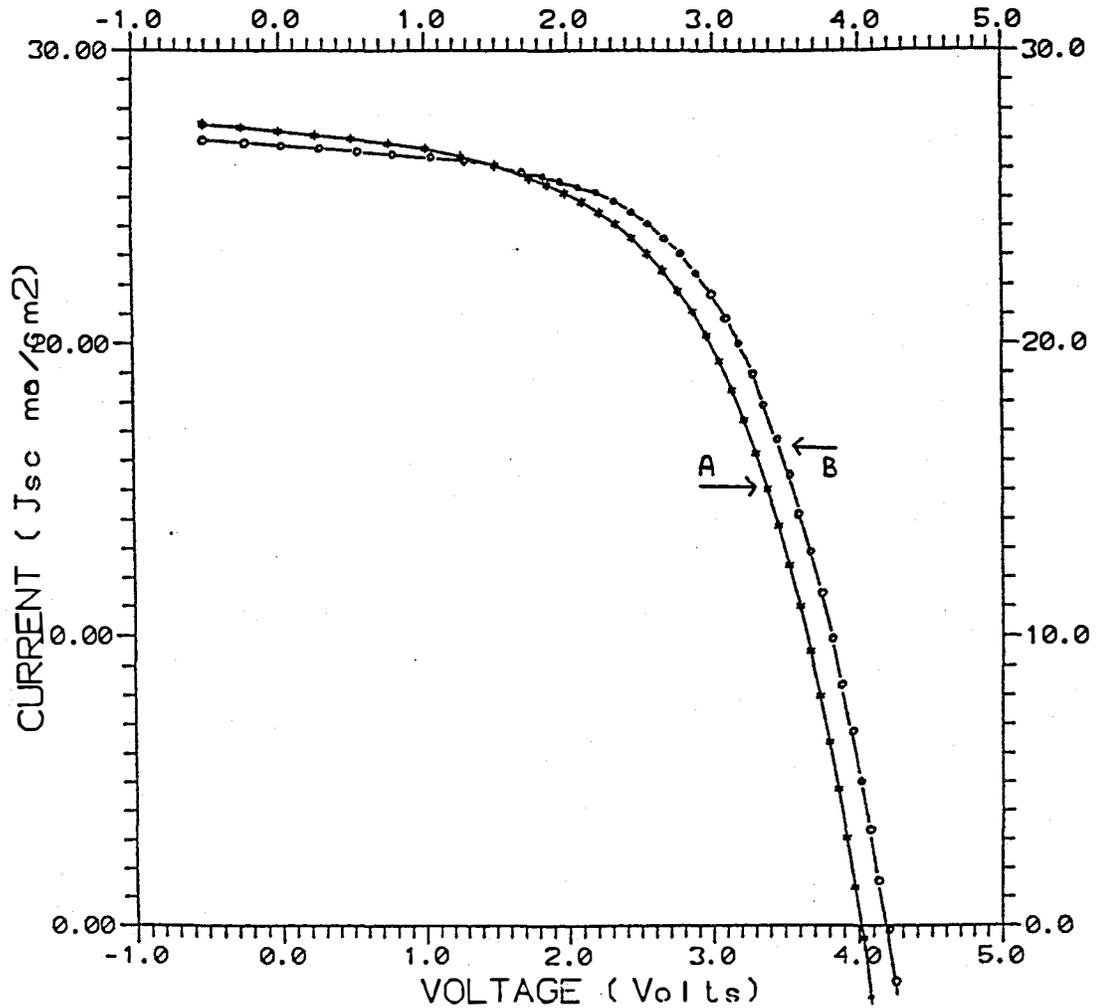


Figure 5.6.3-1 The J-V characteristic for a 40 cm<sup>2</sup>, 10 segment submodule before and after encapsulation. The J-V parameters are (at 25 °C, 100 mW/cm<sup>2</sup> illumination):

	A: Before Encapsulation	B: After Encapsulation
Voc	405 mV/segment	418 mV/segment
Jsc	27.3 mA/cm <sup>2</sup>	27.0 mA/cm <sup>2</sup>
Fill Factor	54.6 %	57.6 %
Efficiency	6.0 %	6.4 %

## 5.7 ADDENDUM

Following phase 3 of this contract there has been a no-cost extension during which much of the work and many of the concepts from phases 1, 2 and 3 have seen important progress. In particular, the best device and submodule characteristics obtained at Solarex have sufficiently improved to be noteworthy in this addendum.

### 5.7.1 Device Improvements

Our record devices have evolved from 14.4% to 15.5% total area efficiency by improvements in current and fill factor. This is seen by comparing figure 5.6-1 (p. 32) to figure 5.7.1-1 where quasi identical Voc values are given, but the Jsc and FF have improved. The fill factor improvement of 1.86% points (to 75.62%) occurs despite a less optimal dark JV characteristic which shows both greater series resistance and lower shunt resistance, as can be seen by comparing figure 5.6-2 (p. 33) with figure 5.7.1-2 of the “improved” device. The 1.7 mA/cm<sup>2</sup> increase in short circuit current is shown by comparing the quantum efficiency measurements in figure 5.7.1-3, to be essentially due to longer wavelength collection for the 15.5% device. Differences in the short wavelength characteristics are negligible, as might be expected for devices using similar conditions for the window layers (i.e. the ZnO and CBD CdS conditions). This QE difference could indicate a slightly smaller bandgap for the 15.5% device. This is supported by EDAX composition measurement, giving a Ga/(In+Ga) ratio of 0.288 for the 14.4% device and 0.246 for the 15.5% device, indicating an “equivalent” bandgap difference of a few tenths of an eV between these absorber layers. From this point of view, the improved device exhibits a superior Voc/Eg behavior. Using the bandgap (Eg) to composition relationship [32] given by:

$$E_g(x) = 1.018 + 0.575x + 0.108x^2 \quad \text{for } \text{CuIn}_{1-x}\text{Ga}_x\text{Se}_2 \quad \text{i.e. } x = \text{Ga}/(\text{In}+\text{Ga})$$

with our EDAX measurements, the resulting bandgap and Voc/Eg values would be:

for the 14.4% device	$E_g = 1.193 \text{ eV}$	$V_{oc}/E_g = 0.498 \text{ V/eV}$
for the 15.5% device	$E_g = 1.166 \text{ eV}$	$V_{oc}/E_g = 0.508 \text{ V/eV}$

### 5.7.2 Submodule Improvements

Our record 40 cm<sup>2</sup> submodule has improved from the 11.1% aperture area conversion efficiency shown in figure 5.6.2-1 (p. 41) to the 13% result shown in figure 5.7.2-1. It is important to remark that, unlike the 11.1% measurement, the 13% submodule is a confirmed NREL measurement. This submodule is composed of 20 interconnected segments and the voltage and current parameters per segment average to be: Voc = 0.580 V/seg. and Jsc = 33.80 mA/cm<sup>2</sup>. These numbers are impressively close to those given in figure 5.7.1-1 for the 15.5% device (i.e. 0.5924 V and 34.54 mA/cm<sup>2</sup>). It appears that the losses for the 13% submodule, relative to the 15.5% device, are almost completely due to the fill factor (66.62% for the submodule versus 75.62% for the device). The significant penalty imposed by both shunt and series resistances on fill factor is apparent in the shape of the 13% submodule JV characteristic. Other submodules produced at Solarex typically exhibit shunt resistances two to four times greater than that estimated from

figure 5.7.2-1 of the 13% submodule. This has been achieved through a different interconnect scheme and has led to a number of submodules with fill factors exceeding 70%, however aperture area efficiencies have been limited to about 12.5% due to lower voltages and currents.

As for the current differences between the “best” submodule and the “best” device, in figure 5.7.2-2 is plotted the QE measurements for both of these. Almost no differences can be seen and the “missing”  $0.74 \text{ mA/cm}^2$  could be accounted for in the total area/aperture area ratio, or by the lesser reflection losses of the device. This device uses a  $\text{MgF}_2$  antireflection coating deposited on the ZnO top contact whereas the submodule uses a glass-to-glass encapsulation composed of EVA and a  $\text{MgF}_2$  coated low-iron cover glass.

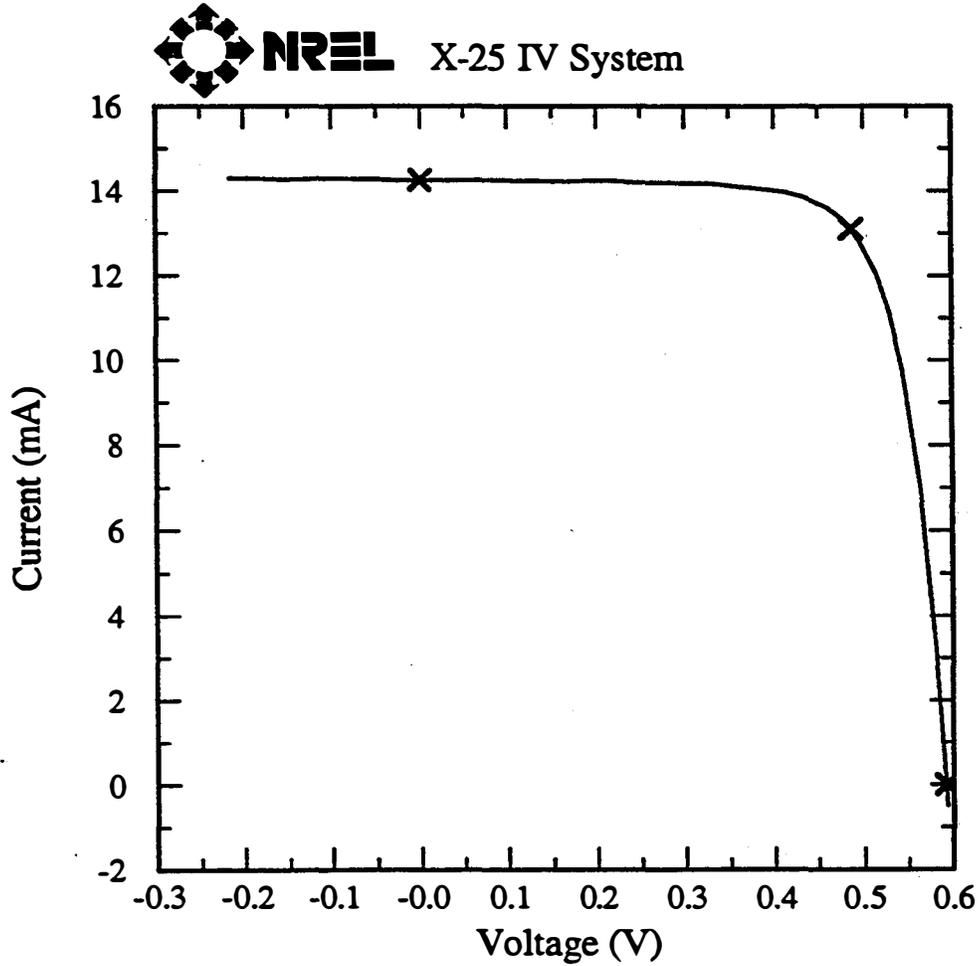
Thus, short circuit current densities have been achieved in modules that are essentially equivalent to those in devices made using the same semiconducting and contacting layers. Nevertheless, short circuit current is one parameter that may possibly be improved, as QE measurements of small area CIGS cells made by other groups show significantly improved current collection at long wavelengths for absorbers having approximately the same bandgap[1]. The extent of potential improvement is presently unclear, as some of this advantage may be due to the use of a more transparent ZnO front contact. As previously explained, higher front contact transparency normally entails decreased conductivity, and thus loss of module fill factor. Other groups also report open circuit voltages which are approximately 50 mV higher than those achieved by our current processes, for approximately the same bandgap absorber[1,2]. Incorporation of this advantage would have a significant impact on submodule performance.

Even without the improvements to  $J_{sc}$  or  $V_{oc}$  mentioned above, it appears that improvements to the 13% submodule can be readily achieved if the more recent interconnect concept is applied to samples where the individual layer quality is similar to that of the present 13% submodule. For example, if the  $V_{oc}$  and  $J_{sc}$  were unchanged, a fill factor of 71.35% would result in a 14% aperture area efficiency submodule. This level of conversion efficiency for thin film modules would have appeared overly optimistic until recently. If this could be achieved, thin film module structures would compare favorably to the module efficiencies cited for those using more mature crystalline technology.

# Solarex ZnO/CdS/CIGS

Sample: E154-3-D7  
Oct 17, 1995 8:45 AM  
ASTM E 892-87 Global

Temperature = 25.0°C  
Area = 0.4127 cm<sup>2</sup>  
Irradiance: 1000.0 Wm<sup>-2</sup>



$V_{oc} = 0.5924 \text{ V}$   
 $I_{sc} = 14.25 \text{ mA}$   
 $J_{sc} = 34.54 \text{ mAcm}^{-2}$   
Fill Factor = 75.62 %

$V_{max} = 0.4871 \text{ V}$   
 $I_{max} = 13.11 \text{ mA}$   
 $P_{max} = 6.385 \text{ mW}$   
Efficiency = 15.5 %

Figure 5.7.1-1 The illuminated J-V characteristic for a 15.5% efficient small area device.

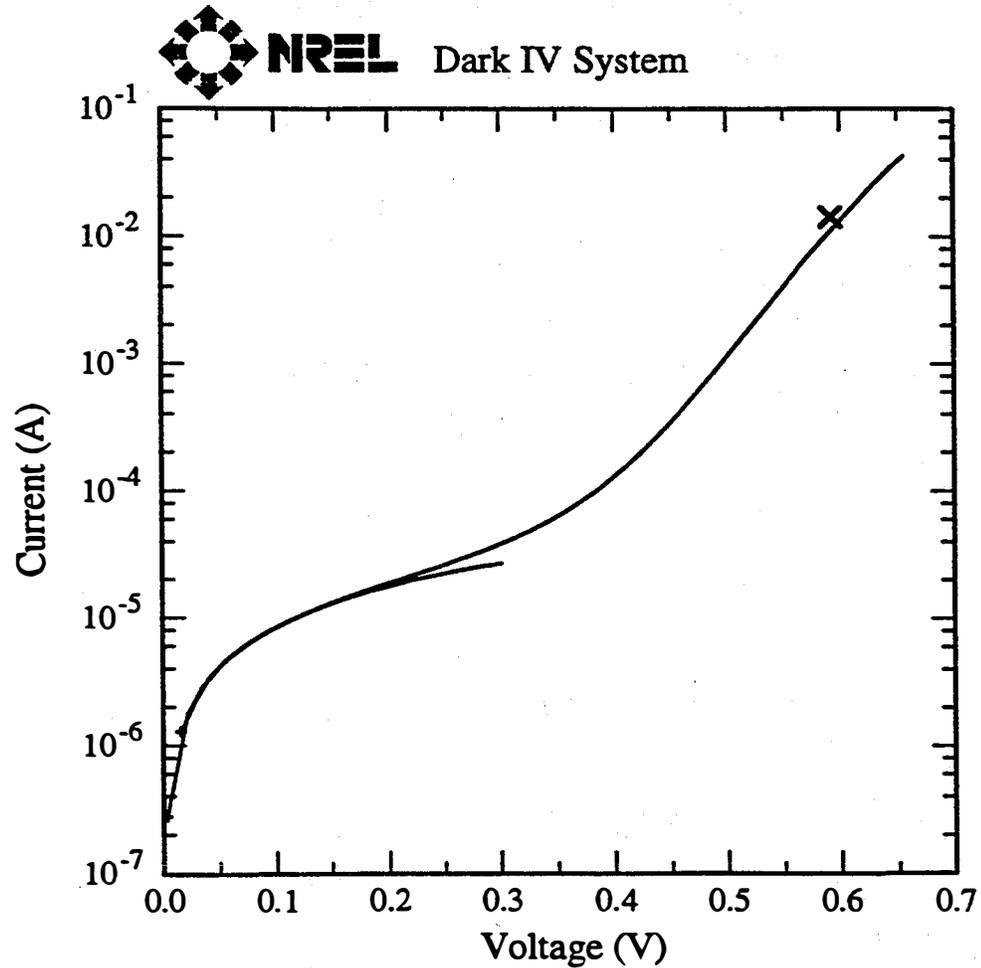
# Solarex ZnO/CdS/CIGS

Sample: E154-3-D7

Temperature = 25.0°C

Oct 17, 1995 8:51 AM

Area = 0.4127 cm<sup>2</sup>



$V_{oc} = 0.5924$  V

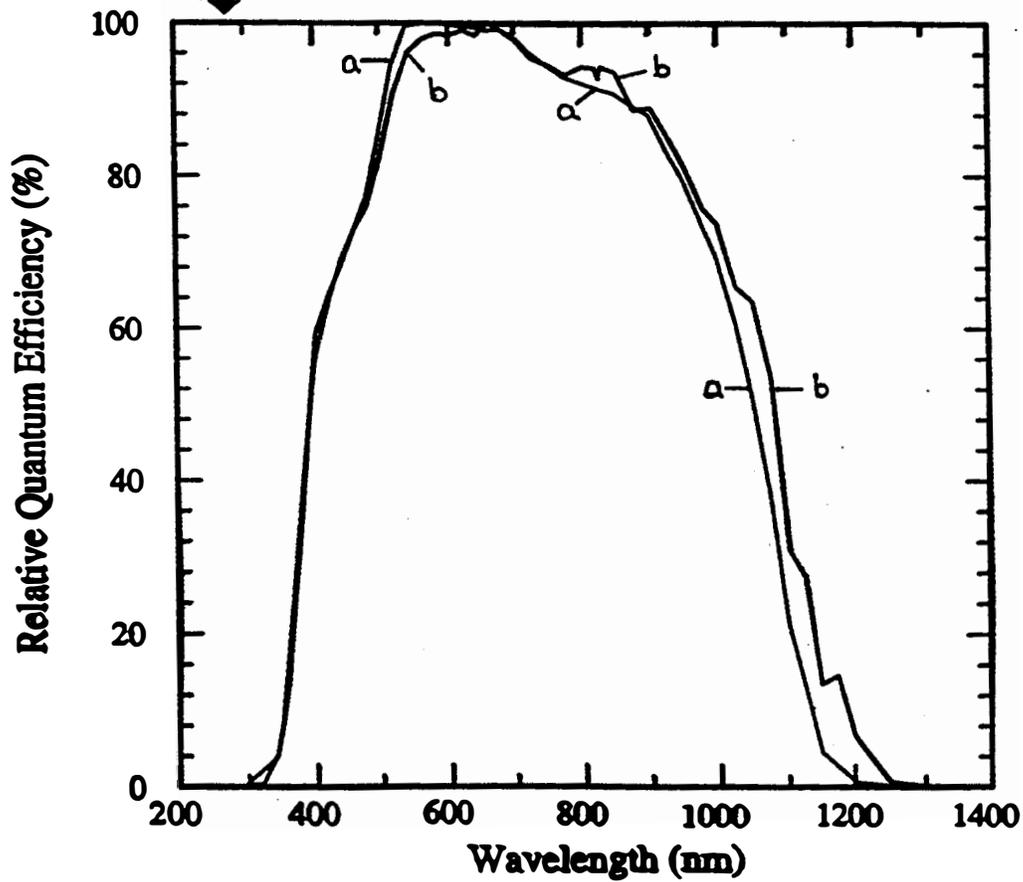
$R_{shunt} = 10.9$  k $\Omega$

$I_{sc} = 14.25$  mA

$R_{series} = 2.51$   $\Omega$

Equiv  $R_s = 1.86$   $\Omega$

Figure 5.7.1-2 The dark J-V characteristic for the 15.5% efficient small area device.



**Figure 5.7.1-3** *The relative quantum efficiency versus wavelength for the 14.4% efficient device (a) and the 15.5% efficient device (b). It must be noted that each measurement is normalized to 100% independently, and therefore cannot be compared in amplitude.*

# Solarex MgF<sub>2</sub>/glass/ZnO/CdS/CIGS/Mo Submodule

Sample: E157-6-7

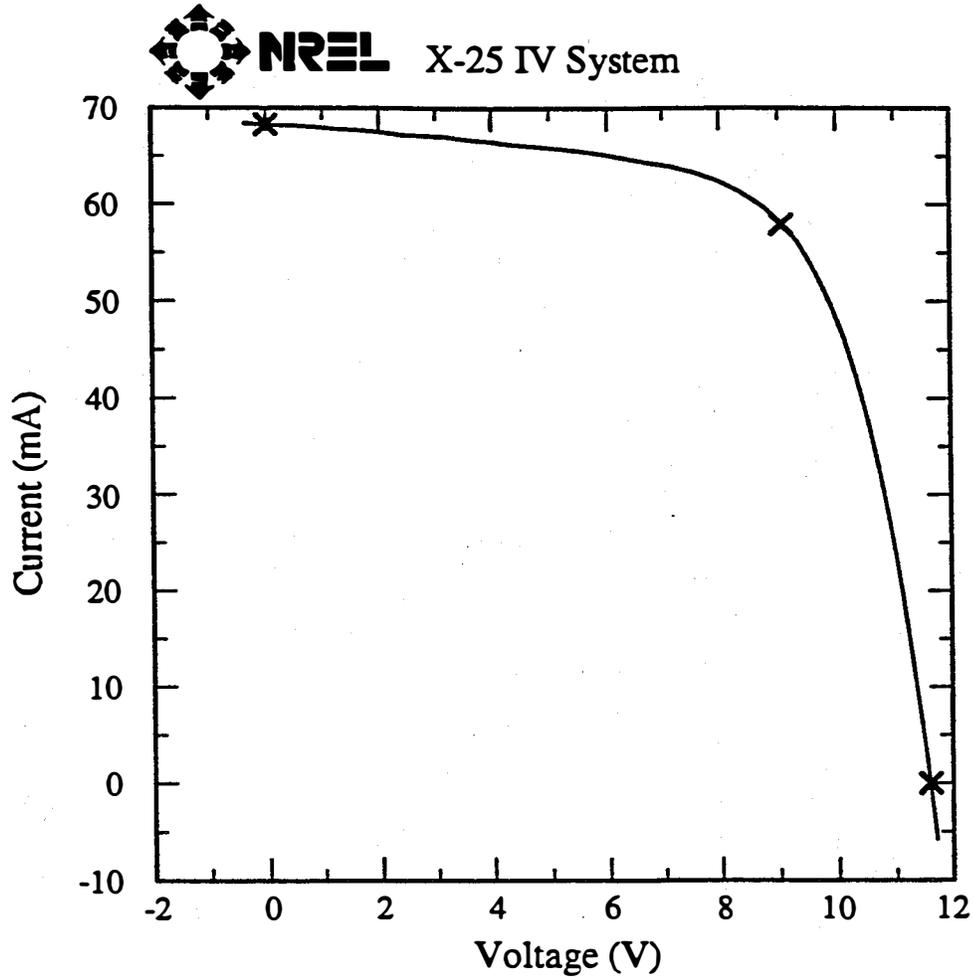
Nov 8, 1995 4:22 PM

ASTM E 892-87 Global

Temperature = 25.0°C

Area = 40.40 cm<sup>2</sup>

Irradiance: 1000.0 Wm<sup>-2</sup>



$$V_{oc} = 11.61 \text{ V}$$

$$I_{sc} = 68.29 \text{ mA}$$

$$J_{sc} = 1.690 \text{ mAcm}^{-2}$$

$$\text{Fill Factor} = 66.26 \%$$

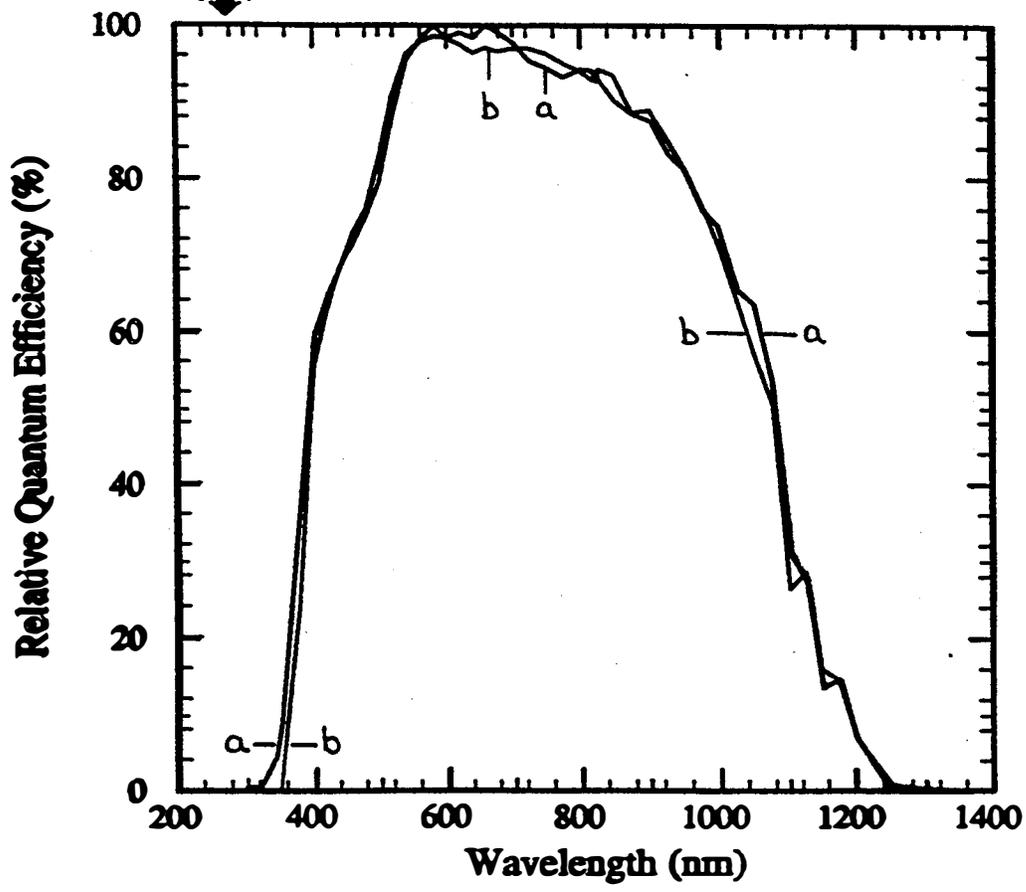
$$V_{max} = 9.062 \text{ V}$$

$$I_{max} = 57.97 \text{ mA}$$

$$P_{max} = 525.3 \text{ mW}$$

$$\text{Efficiency} = 13.0 \%$$

**Figure 5.7.2-1** The illuminated J-V characteristic for a monolithic submodule having 13% aperture area conversion efficiency. This 40.4 cm<sup>2</sup> submodule is comprised of 20 segments and is encapsulated using EVA and a MgF<sub>2</sub> coated cover glass.



**Figure 5.7.2-2** The relative quantum efficiency versus wavelength for the 15.5% efficient device (a) and for the 13% efficient submodule (b). It must be noted that each measurement is normalized independently and cannot be compared in amplitude.

## 6.0 CONCLUSIONS

As a result of this effort much progress has been made in the development and understanding of the process steps required for successful production of CIS based thin film PV. The required thin film deposition processes for all substrate and window layers have been scaled up to 1000 cm<sup>2</sup> size, and one absorber layer deposition process has been implemented in square-foot capable equipment. Module fabrication processes have also been developed for up to 1000 cm<sup>2</sup> substrate size. A preliminary evaluation of the interaction of processes and the impact of several alternative processing methods on module manufacturability has been completed.

Several attributes of the overall process have emerged as factors which will be key to successful commercialization of this system. Specifically, the impact of shunts on the yield of finished modules is a prime concern. Shunt formation, and thus ultimately yield, are most strongly governed by the method of absorber layer formation and by module scribing operations. The importance of yield to manufacturability, and its relationship to these specific processes required substantial improvements in these two areas over the course of the program. Scribing operations and associated front and back contact processes were continuously improved by necessity in order to reduce shunt formation. Substantially different methods of absorber layer formation were evaluated in succession from the viewpoint of robustness to shunt formation, as well as control, reproducibility and performance. As a result we have now identified an overall process which we believe is viable in terms of manufacturability. Moreover, we have demonstrated many of the key aspects of that overall process.

The challenges which remain include further optimization and understanding of the processes for front, back and absorber layers, module scribing operations, increasing process speed and materials utilization, and evaluation of methods to accomplish further scale-up. Opportunity also exists for improvement in module design, module interconnect formation and the development of a more attractive heterojunction buffer layer process, for example a Cd free, dry process. We expect that the robust, manufacturable process which was successfully developed under this program will allow rapid progress in these areas and others required for the pilot manufacture of CIS based PV modules.

## REFERENCES

1. J. R. Tuttle, A. M. Gabor, M.A. Contreras, A.L. Tennant, K.R. Ramanathan, A. Franz, R. Matson and R. Noufi, "Absorber Processing Issues in High-Efficiency, Thin-Film Cu(In,Ga)Se-Based solar Cells", 13th NREL PV Program Review Meeting, Lakewood, CO, May 1995, AIP Conference Proceedings 353, pp 47-57.
2. J. Hedström, H. Ohlsén, M. Bodegård, A. Klyner and L. Stolt, "ZnO/Cu(In,Ga)Se<sub>2</sub> Thin Film Solar Cells with Improved Performance", Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May 1993, pp 364 -371.
3. J. Kessler, S. Wiedeman, L. Russell, T. Lommasson, S. Skibo, J. Fogleboch, T. Kloss, R.R. Arya, Proceedings of the 24th IEEE Photovoltaics Specialists Conference, Waikoloa, Hawaii, 1994 (IEEE, New York, 1994), p. 206.
4. A. Catalano, R. Arya, L. Carr, B. Fieselman, T. Lommasson, R. Podlesny, L. Russell, S. Skibo, Solarex Phase 1 Annual Report to National Renewable Energy Laboratory under Subcontract No. ZN-1-19019-4, 11/11/90-10/31/91.
5. K.L. Chopra and S.R. Das, *Thin Film Solar Cells*, Plenum Press, 1983, pp 221.
6. W.J. Danaher, L.E. Lyons and G. C. Morris, "Some Properties of Thin Films of Chemically Deposited Cadmium Sulfide", *Solar Energy Materials*, 12(1985), pp. 137 - 148.
7. L. Russell, B. Fieselman and R. R. Arya, "Optimization of CIS Window Layers and Scale-Up for Large Area Sub-Module Application", Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May 1993, pp 581 - 585.
8. R.R. Arya, T. C. Lommasson, S. Wiedeman, L. Russell, S. Skibo and J. Fogleboch, "Solar Cells and Submodules on CIS Prepared by EDCF Method", Proceeding of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May 1993, pp 516 -520.
9. R. Arya, J. Fogleboch, T. Lommasson, R. Podlesny, L. Russell, S. Skibo, S. Wiedeman, Solarex Phase 2 Annual Report to National Renewable Energy Laboratory under Subcontract No. ZN-1-19019-4, 11/01/91-12/31/92.
10. J. Kessler, M. Ruckh, D. Hariskos, U. Rühle, R. Menner and H.W. Schock, "Interface Engineering Between CuInSe<sub>2</sub> and ZnO", Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May, 1993, pp 447 - 452.
11. J. Hedström, H. Ohlsén, M. Bodegård, A. Klyner, L. Stolt, D. Hariskos, M. Ruckh and H.W. Schock, "ZnO/CdS/Cu(In,Ga)Se<sub>2</sub> Thin Film Solar Cells with Improved Performance",

Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May, 1993, pp 364 -371.

12. R.W Birkenire, J.E. Phillips, W.A. Buchanan, S. S. Hegedus, B.E. McCandless and T. A. Yokimcus, "Processing and Modeling Issues for Thin Film Solar Cell Devices", Annual Report to NREL Under Subcontract Number X-AV-13170-01, March, 1994.

13. R. R. Arya, T. Lommasson, S. Wiedeman, L. Russell and A. Catalano, "Solar Cells on Copper Indium Diselenide Prepared by a Novel Method", Proceedings of the 11th EC PVSEC, Montreaux, Switzerland, October 1992, pp 112 - 115.

14. V. K. Kapur, B. M. Basol, A. Halani, C.K. Leidholm and A. Minnic, "Technical and Business Factors Affecting Commercialization of Thin Film CIS Technology", Proceeding of 12th EC PVSEC, Amsterdam, The Netherlands, April, 1994, pp 1608 - 1611.

15. J. Kessler, D. Schmidt, S. Zweigart, H. Dittrich and H. W. Schock, "CuInSe<sub>2</sub> Film Formation from Sequential Deposition on In(Se):Cu:Se", Proceeding of 12th EC PVSEC, Amsterdam, The Netherlands, April, 1994, pp 648 -652.

16. J. Kessler and H. W. Schock "Selenization From Sequential Deposition of Cu:In(Se):Se", Proceedings of the 11th EC PVSEC, Montreaux, Switzerland, October 1992, pp 838 -841.

17 T. C. Lommasson, S. Wiedeman, L. Russell, J. Kessler and R. R. Arya, "CIS Module Development at Solarex", Proceeding of 12th EC PVSEC, Amsterdam, The Netherlands, April, 1994, pp 1226 -1228.

18. J.R. Tuttle, M. Contreras, M.H. Bode, D. Niles, D.S. Albin, R. Matson, A.M. Gabor, A. Tennant, A. Duda and R. Noufi, "Structure, Chemistry and Growth Mechanisms of Photovoltaic Quality Thin Film Cu(In,Ga)Se<sub>2</sub> Grown from a Mixed Phase Precursor", *J. App. Phys.*, 77(1), 1 January 1995, pp 153 -161.

19. T. Walter and H.W. Schock, "Crystal Growth and Diffusion in Cu(In,Ga)Se<sub>2</sub> Chalcopyrite Thin Films", *Thin Solid Films*, 224(1993), pp 74 -81.

20. A. Dhingra and A. Rothwarf, "Computer Simulation and Modeling of the Graded Bandgap CuInSe<sub>2</sub>/CdS Solar Cell", Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May, 1993, pp 475 -480.

21. A.M. Gabor, J.R. Tuttle, M. Contreras, D.S. Albin, A. Franz, D.W. Niles and R. Noufi, "High-Efficiency Thin Film Cu(In,Ga)Se<sub>2</sub> Solar Cells: Achievement of a Confirmed World-Record 16.4% Total-Area Efficiency", 12th European Photovoltaic Solar Energy Conference, Amsterdam, The Netherlands, April, 1994, pp 939-943.

22. C.L. Jensen, D.E. Tarrant, J.H. Ermer and G. A. Pollock, "The Role of Gallium in CuInSe<sub>2</sub> Solar Cells Fabricated by a Two Stage Method", Proceedings of 23rd IEEE Photovoltaic Specialist Conference, Louisville, KY, May, 1993, pp 577 -580.
23. M. Contreras, (private communication).
24. J.Holz, F. Karg and H. von Philipsborn, "The Effect of Substrate Impurities on the Electronic Conductivity in CIS Thin Films", " Proceeding of 12th EC PVSEC, Amsterdam, The Netherlands, April, 1994, pp 1592 -1595.
25. M. Bodegård, L.Stolt, J. Hedström, "The Influence of Sodium on the Grain Structure of CuInSe<sub>2</sub> Films for Photovoltaic Applications", Proceeding of 12th EC PVSEC, Amsterdam, The Netherlands, April, 1994, pp 1743 - 1746.
26. S. Wiedeman, L. Russell, A. Dzinga, A. Rothwarf, W. Shafarman and R. Birkmire, "Characterization and Modeling of Cu(In,Ga)(S,Se)<sub>2</sub>-based Photovoltaic Devices: A Laboratory and Industrial Perspective, J.R. Tuttle, J.R. Sites, A. Delahoy, W. Shafarman, B. Basol, S. Fonash, J. Gray, R. Menner, J. Phillips, A. Rockett, J. Scofield, F. R. Shapiro, P. Singh, V. Suntharalingam, D. Tarrant, T. Walter, S. Wiedeman, and T.M. Peterson, Progress in Photovoltaics: Research and Applications, **3**, 1995, pp 89-104.
27. H. W. Schock, B. Dimmler, H. Dittrich, J. Kimmerle and R. Menner, "Heterojunction Solar Cells Based on Cu(Ga,In)Se<sub>2</sub> Chalcopyrite Thin Films", Proceedings of 7th EC PVSEC, Sevilla, Spain, October 1986 pp 465 -469.
28. J. Ermer, C. Fredric, J. Hummel, C. Jensen, D. Pier, D. Tarrant and K. Mitchell, "Advances in Large Area CuInSe<sub>2</sub> Thin Film Modules" Proceedings of 21st IEEE Photovoltaic Specialist Conference, Kissimmee, FL, May 1990, pp 595-599.
29. D. Tarrant and J. Ermer, "I-III-VI<sub>2</sub> Multinary Solar Cells Based on CuInSe<sub>2</sub>", Proceedings of 23rd IEEE Photovoltaic Specialists Conference, Louisville, KY, May, 1993, pp 372 -378.
30. S. Wiedeman, J. Kessler, T. Lommasson, L. Russell, J. Fogleboch, S. Skibo and R. Arya, "Challenges in Large-Area, Thin-Film CIGS Modules", Presented at 13th Annual Photovoltaic Program Review Meeting, Lakewood CO, May, 1995.
31. S. Wiedeman, J. Kessler, L. Russell, J. Fogleboch, S. Skibo, T. Lommasson, D. Carlson and R. Arya, "Optimization of Cu(In,Ga)Se<sub>2</sub> Photovoltaic Modules", Presented at 13th European Photovoltaic Solar Energy Conference, Nice, France, October, 1995. (to be published)
32. B. Dimmler, H. Dittrich, R. Menner, and H.W. Schock, "Performance and Optimization of Heterojunctions Based on Cu(Ga,In)Se<sub>2</sub>", Presented at 19th IEEE Photovoltaic Specialists Conference, New Orleans, LA, 1987, pp 1454-1460.

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13. ABSTRACT ( <i>Maximum 200 words</i> )  This report describes work performed by Solarex Corporation to enter into the development of CIS-based photovoltaic (PV) products. The activity began with developing manufacturable deposition methods for all required thin-film layers and developing and understanding processes using those methods. It included demonstrating the potential for high conversion efficiency and followed with developing viable methods for module segment formation and interconnection. These process steps were integrated to fabricate monolithic CIS-based submodules. An important result of this program is the basis of understanding established in developing this material for PV applications. This understanding is necessary to address issues of manufacturability and cost—which were recognized early in the program as being determined by successful solutions to issues of yield, reproducibility, and control as much as by material and energy costs, conversion efficiency, and process speed. Solarex identified at least one absorber formation process that is very robust to shunt formation from pinholes or point defects, tolerant of variation in processing temperature and elemental composition, and is capable of producing high conversion efficiency. This program also allowed development and scale-up of processes for the deposition of all other substrate, heterojunction buffer, and window layers and associated scribing/module formation operations to 1000-cm <sup>2</sup> size. At the completion of this program, Solarex has in place most of the necessary elements to begin the transition to pilot operation of CIS manufacturing activities.			
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