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This paper describes an improved CdS/CdTe polycrystalline thin-film solar-cell device structure that integrates a zinc stannate (Zn_2SnO_4 or ZTO) buffer layer between the transparent conductive oxide (TCO) layer and the CdS window layer. Zinc stannate films have a high bandgap, high transmittance, low absorptance, and low surface roughness. In addition, these films are chemically stable and exhibit higher resistivities that are roughly matched to that of the CdS window layer in the device structure. Preliminary device results have demonstrated that by integrating a ZTO buffer layer in both SnO_2-based and Cd_2SnO_4 (CTO)-based CdS/CdTe devices, performance and reproducibility can be significantly enhanced.

Cadmium telluride has long been recognized as a promising photovoltaic material for thin-film solar cells because of its near optimum bandgap of ~1.45 eV and its high direct absorption coefficient. Small-area CdTe cells with efficiencies of greater than 15% (1) and CdTe modules with efficiencies of greater than 9% (2) have been demonstrated. The field stability of CdTe modules has also been confirmed. One remaining challenge is to further improve device performance and reproducibility. In this paper, we report that by integrating a Zn_2SnO_4 buffer layer into CdS/CdTe devices, performance and reproducibility can be significantly enhanced.

Performance and reproducibility of CdS/CdTe devices can be impacted by many factors. For example, in heterojunction solar cells, it is well known that higher short-circuit currents can be obtained by reducing the window-layer absorption. In CdS/CdTe cells, this is achieved by reducing the CdS thickness to improve the blue spectral response. However, reducing the CdS layer thickness can adversely impact device open-circuit voltage (V_{oc}). As the CdS thickness is thinned, the probability of pinhole formation increases, causing localized TCO/CdTe junctions with inferior device parameters (V_{oc} and fill factor). Performance and reproducibility can also be affected by back-contact processing. Polycrystalline CdTe is very difficult to dope heavily p-type, and therefore, to make a low-resistance back-contact, a wet-chemical etch is typically used to form a p^+ surface region. Although this p^+ surface layer facilitates ohmic contact formation, this etch can also preferentially etch grain boundaries, leaving highly conductive shunt paths that degrade the device parameters. Finally, performance and reproducibility can be influenced by the $CdCl_2$ anneal used by all cell manufacturers. The $CdCl_2$ treatment is an important process for making high-efficiency CdTe devices and offers several substantial benefits such as: increased grain size, grain-boundary passivation, increased CdS/CdTe interface alloying, and reduced lattice mismatch between the CdS and CdTe layers. However, one disadvantage of the $CdCl_2$ treatment is that over-treatment can result in adhesion loss problems. Grain growth, which can occur

during $CdCl_2$ treatment, introduces stress at the interface between the CdS and CTO layer, resulting in film blistering or peeling.

The addition of a high-resistivity buffer layer, placed between the TCO and the CdS layers, could address the performance and reproducibility issues described above as follows: i) If the resistivity of the buffer layer were roughly matched to that of the CdS layer, the buffer layer could reduce the probability of forming localized TCO/CdTe junctions that can occur when the CdS layer is thinned. Thus, high V_{oc} could be maintained while reducing the CdS thickness to provide higher device short-circuit current density (J_{sc}); ii) If the buffer layer were resistant to the etches used for back-contact formation (i.e., served as a "stop etch" layer), these devices would be less susceptible to over-etching, which could greatly reduce shunting problems; and iii) A buffer layer could help relieve stresses between these layers, thereby improving adhesion during the $CdCl_2$ treatment. We have developed a ZTO buffer layer that, when integrated into a CdS/CdTe device structure, imparts all the above-mentioned benefits.

ZTO films were prepared by RF sputtering from a hot-pressed oxide target. The 2-in.-diameter target was ~60% Zn/(Zn+Sn), as determined by X-ray photoemission spectroscopic (XPS) measurements. ZTO films were deposited in pure O_2 at room temperature. We find that ZTO films have properties that make them ideal as a buffer layer in CdS/CdTe devices. They have low absorptance, are highly resistive, have low surface roughness, and are chemically stable. Figure 1 shows the transmittance, reflectance, and absorptance of a ZTO film. The films exhibit near-zero absorptance and have a wide optical bandgap (~3.3 eV). As-deposited ZTO films have resistivities of more than 1000 ˜-cm. The resistivity typically decreases to 0.1-10 ˜-cm (which roughly matches that of the CdS window-layer resistivity) after annealing in an Ar/CdS ambient for 5 minutes in a temperature range of 500°C to 600°C. As-deposited, ZTO films are amorphous and crystallize into a single-phase spinel structure after thermal annealing. As shown in Figure 2: an atomic force micrograph of a typical ZTO film, these films have very smooth surfaces, with an average surface roughness of ~20Å. We also find that ZTO films are chemically stable and cannot be etched in HCl, HNO_3, or nitric/phosphoric-based acid etches.

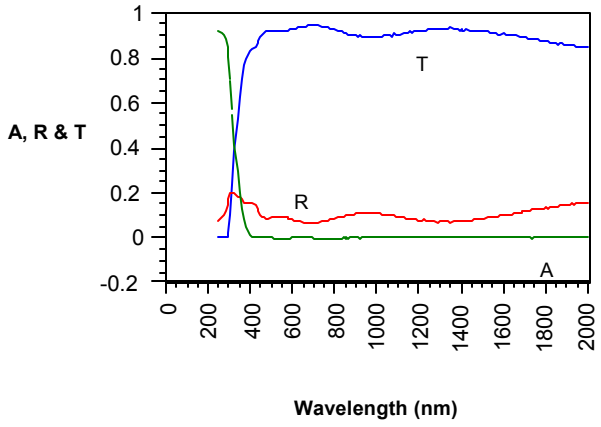
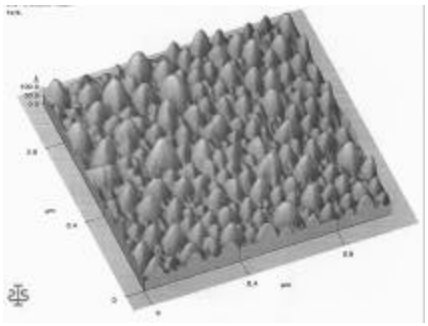


Figure 1. The transmittance, reflectance, and absorptance of a ZTO film.



R_a = 20Å

Figure 2. An atomic force micrograph of the surface of a ZTO film.

For the first time, we have fabricated CdTe devices with ZTO buffer layers. Figure 3 shows the modified CdS/CdTe device structure. Both SnO_2 and Cd_2SnO_4 (3,4) TCO films have been used in this work. Preliminary cell results have demonstrated that high-performance CdS/CdTe devices can be fabricated by integrating a ZTO buffer layer into CdS/CdTe devices. For example, a glass/Cd_2SnO_4/ZTO/CdS/CdTe device with a ~700Å CdS layer has been fabricated with a J_{sc} of 24.8 mA/cm^2. Although the CdS is thin, this device retained a high V_{oc} (816 mV) and fill factor (72.6%) due to the addition of a ZTO buffer layer.

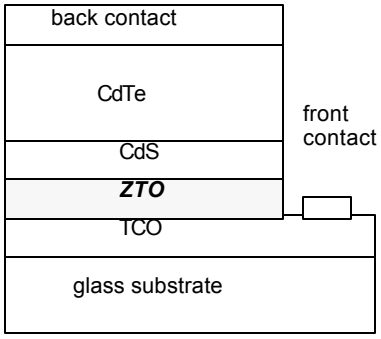


Figure 3. An improved CdS/CdTe device structure with a ZTO buffer layer.

Table 1 shows device parameters for two identically processed cells. Each of these devices uses an absorber layer that is thinner than we typically use in our standard device structure. Both devices were over-etched during back-contact formation. As shown in Table 1, the V_{oc} and efficiency of a device without a ZTO buffer layer are only 679 mV and 5.7%, respectively. In contrast, the device with a ZTO buffer layer is able to maintain a high V_{oc} (807 mV) and has a much higher efficiency (12.8%). The improved device parameters are attributed to the ZTO buffer layer acting as a nonconductive stop-etch layer, which reduces device shunting.

Table 1. Improved Thin CdTe Cell Performance

Cell structure	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)
CTO/CdS/CdTe	679	19.0	44.2	5.7
CTO/ZTO/CdS/CdTe	807	23.0	68.8	12.8

We also find that integrating a ZTO buffer layer can significantly improve the adhesion after $CdCl_2$ treatment. These results are summarized in Table 2, which shows a total of 98 CdS/CdTe devices, each of which received a 100% saturated $CdCl_2$ solution soak (50%-75% $CdCl_2$ solution is typical) and subsequent thermal anneal and was evaluated for adhesion. Eighty-four of these devices had the ZTO buffer layer integrated into the structure, and 14 did not. Without the buffer layer, under these extreme conditions, we found that one cell had good adhesion out of a total of 14 (7% yield). In sharp contrast, with the ZTO buffer layer, 79 cells had good adhesion out of 84 (94% yield). This result has significant manufacturing ramifications: The ZTO buffer layer provides far better adhesion, and thus, much greater process latitude when optimizing the $CdCl_2$ process step.

Table 2. Significantly Improved Adhesion after $CdCl_2$ Treatment

	CdTe cells without ZTO layer	CdTe cells with ZTO layer
Total	14	84
Good adhesion	1	79
Blister on edges	8	5
Completely peeled off	5	0

Finally, we find that the addition of a ZTO buffer layer provides excellent device reproducibility. This is clearly seen in Figure 4, which shows the efficiency of 30 identically processed devices (18 Cd_2SnO_4-based CdTe cells and 12 SnO_2-based CdTe cells), all of which included a ZTO buffer layer but did not have an antireflection coating to reduce reflection losses. This set of 30 devices had an average efficiency of 13.83%, with a standard deviation of 0.375%.

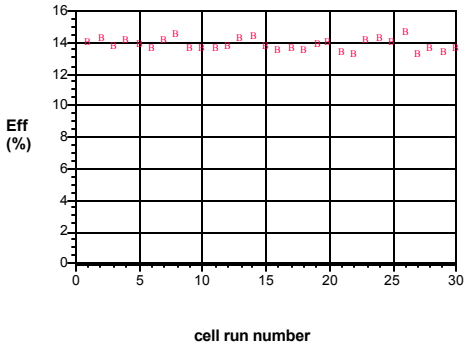


Figure 4. Performance and reproducibility of CdS/CdTe solar cells with ZTO buffer layers.

By integrating a ZTO buffer layer into a CTO-based CdS/CdTe cell, we have achieved efficiencies as high as 15.0% as shown in figure 5. Figure 5 shows the standard I-V curve of this cell. We believe that the performance of CdS/CdTe cells with the ZTO buffer layer is far from optimized and expect that improved understanding of the physics and

chemistry of how ZTO buffer layers impact CdS/CdTe devices will lead to further enhancements in device performance.

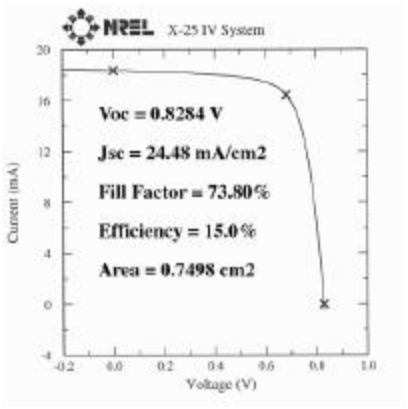


Figure 5. I-V curve of a Cd_2SnO_4-based CdS/CdTe cell with a ZTO buffer layer.

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