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Abstract: In this paper, we have studied the effect of high-resistance SnO$_2$ buffer layers, deposited by low-pressure chemical-vapor deposition, on CdS/CdTe device performance. Our results indicate that when CdS/CdTe devices have a very thin layer of CdS or no CdS at all, the i-SnO$_2$ buffer layer helps to increase device efficiency. When the CdS layer is thicker than 600Å, the device performance is dominated by CdS thickness, not the i-SnO$_2$ layer. If a very thin CdS layer is to be used to enhance device performance, we conclude that a better SnO$_2$ buffer layer is needed.

INTRODUCTION

High-resistance transparent (HRT) layers have been used as a buffer layer between the transparent conducting oxide (TCO) and the CdS layer to help maintain CdS/CdTe device performance when thin CdS films are used or there is a high density of pinholes. Several HRT materials have been used as a buffer layer, including undoped SnO$_2$, TiO$_2$, and Golden Photon's (GPI) proprietary HRT layer.

In our group, a sputter-deposited intrinsic SnO$_2$ (i-SnO$_2$) was used as a buffer layer in baseline process. Previous experiments incorporating this layer have yielded mixed results. In some instances, the buffer layer helped to maintain high device open-circuit voltages (V$_{oc}$) and fill factors (FF), thereby improving reproducibility. However, the device efficiency (η) did not always improve with the addition of the buffer layer. We found that, in part, this could be explained by the thermal instability of the buffer layer, which was deposited at room temperature.[1]

Recently, we installed a low-pressure chemical-vapor deposition (LPCVD) system for TCO research, which has yielded better quality SnO$_2$ films. With this ability, we investigated the effect of high resistance SnO$_2$ on CdS/CdTe device performance and its interaction with CdS layer thickness.

EXPERIMENTAL

In this study, both high resistance i-SnO$_2$ and conductive SnO$_2$ (SnO$_2$:F) films were deposited by LPCVD with growth temperatures of 500°C. The precursors for tin, oxygen, and fluorine dopant were tetramethytin (TMT), ultrahigh purity oxygen gas, and CBrF$_3$, respectively. The resistivities of the SnO$_2$:F and i-SnO$_2$ films were

approximately 5×10^{-4} Ω-cm and 1 Ω-cm, respectively. A bilayer structure with an i-SnO_2 buffer layer on the top of the SnO_2:F was used as a front electrode for CdS/CdTe device fabrication. The total bilayer thickness was kept around 6000Å, with the i-SnO_2 thickness varied from zero to 2000 Å. The sheet resistance of the bilayer-SnO_2 film used in this study ranged from ~8 Ω/sq (~6000Å SnO_2:F and zero Å of i-SnO_2) to ~12 Ω/sq (~4000Å SnO_2:F and ~2000 Å of i-SnO_2). Later in this paper, we will see that the sheet resistance of bilayer TCO does not affect the device performance under our experiment of conditions.

The CdS films were then deposited by chemical-bath deposition (CBD) and CdTe films were deposited by close-spaced sublimation (CSS). A source temperature of 660°C and a substrate temperature of 620°C were used in the CSS deposition. A vapor $CdCl_2$ treatment was chosen as a post-deposition treatment. The source-plate temperature varied between 395°-405°C, and the substrate temperature varied between 390°-400°C.   After the vapor $CdCl_2$ treatment, all the samples were finished with a nitric-phosphoric acid etch and a Cu doped HgTe/graphite back-contact. Finally, the device was isolated by physically removing the material around the back-contact area. The width of the device was carefully controlled to about 3 mm to limit the loss caused by the TCO sheet resistance. Moreover, by keeping the constant device width, we can assess the effect of sheet resistance on the device performance.

EXPERIMENTAL RESULTS

The Temperature Stability of SnO_2 Film

We have compared the temperature stability of the three types of SnO_2 films that were deposited by LPCVD using a TMT precursor, room-temperature (RT) sputtering, and high-temperature CVD using a $SnCl_4$ precursor. All the samples were annealed at 500°C for 15 minutes in a H_2 ambient. The TMT-formed SnO_2 did not show any reduction of either optical or electronic properties. The $SnCl_4$-formed SnO_2 film had a low optical transmission as formed and did not show a reduction after annealing. However its resistance increased by about one order of magnitude after annealing. The sputtered-formed SnO_2 film showed a dramatic reduction in quality. Fig. 1 shows that after annealing, the absorption of sputtered SnO_2 increased from an average of 10% to over 30%, and the absorption of LPCVD-formed SnO_2 did not change at all.   The X-ray results indicate that the optical reductions may be due to free tin resulting from the reduction of the SnO_2.[1] Because after annealing, a tin diffraction pattern was seen in the sputtered SnO_2 sample, but not in LPCVD-formed SnO_2 sample. We conclude that the SnO_2 film made by the high-temperature LPCVD process and TMT precursor is very stable thermally.

The Effect of Morphology of SnO$_2$ Film

For the front-wall structure CdS/CdTe device, the mechanical properties of the front TCO electrode could affect the CdS and CdTe layers that grow on it.[2] The film crystallite orientation was studied using X-ray diffraction (XRD). Fig. 2 is a plot of two XRD patterns obtained from SnO$_2$:F (1.25 μm thick) and i-SnO$_2$ (1.11 μm thick) films. The SnO$_2$:F film shows a strong (200) orientation, and the i-SnO$_2$ film shows a random orientation compared to the doped one. Because the two samples have a similar thickness, we believe the difference in crystallite orientation is due to the doping of the films not the film thickness.[3] For the bilayer SnO$_2$ structure, the XRD pattern is a composite of both the doped and undoped diffraction patterns. The atomic force microscopy image showed that the surface roughness (R$_{rms}$) of both the i-SnO$_2$ and SnO$_2$:F films depended strongly on the growth temperature and the film thickness. With a growth temperature of 500°C and a film thickness of 6000Å, the surface roughness of SnO$_2$ films was about 60 nm.

The preliminary device results indicated that adding a i-SnO$_2$ layer, which has different crystallite orientation than SnO$_2$:F, did not affect the adhesion of CdS/CdTe on the SnO$_2$ layer. The adhesion loss of CdS/CdTe films from the TCO substrate mainly depends on the CdS thickness and the strength of vapor CdCl$_2$ treatment.
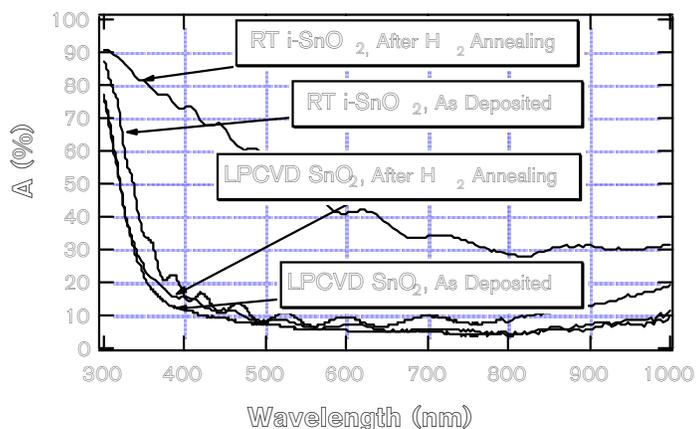
FIGURE 1.   The annealing effect on the absorption of SnO$_2$ film made by LPCVD and by RT sputtering. Both films were annealed at 500°C in a H$_2$ ambient for 15 minutes. The solid lines are for as-deposited samples and the dotted line are for samples after annealing.

The Effect of i-SnO$_2$ Film Thickness

Three groups of samples were studied to understad the relationship between the i-SnO$_2$ (t$_{i-SnO2}$) and the CdS/CdTe device performance. Each group of samples had a range of CdS thicknesses (300Å, 600Å, and 900Å), and a range of i-SnO$_2$ thicknesses (0Å, 600Å, 1200Å, and 1800Å). The device parameters were then studied as a

function of t_{i-SnO2}. Fig. 3 shows that for the first group of samples (t_{CdS} =300 Å), V_{oc} depended on the t_{i-SnO2} thickness. When t_{i-SnO2} increased from zero to 1800Å, the V_{oc} increased from ~500 mV to over 700 mV. For the second and third groups of devices, which have moderate CdS thicknesses (t_{CdS} =600 Å and 900Å), the V_{oc} was almost unchanged over the range of t_{i-SnO2}.
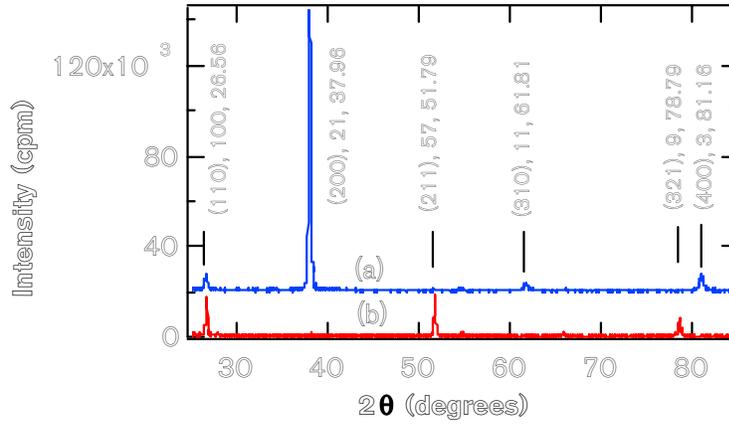
FIGURE 2. The X-ray diffraction patterns of fluorine-doped and undoped SnO_2. (a) SnO_2:F, (b) intrinsic SnO_2.
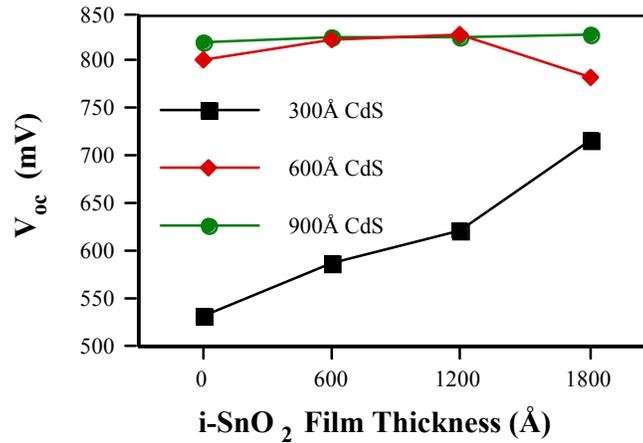
FIGURE 3. The relationship of V_{oc} to i-SnO_2 buffer-layer thickness for those devices made on different CdS and i-SnO_2 films thickness.

We did not observe changes in the short-circuit current density (J_{sc}) as t_{i-SnO2} was varied. This is likely because the transmission of the i-SnO$_2$ film is as good as the SnO$_2$:F film. The device series resistance (R_{s0}) and shunt resistance (R_{sh0}) were plotted as a function of bilayer sheet resistivity (R_{sq}). We did not observe a consistant relationship between R_{sq} and R_{s0} or R_{sh0}. Similarly, no clear trend was observed between the FF and t_{i-SnO2}. As a result, the η exhibits a pattern similar to that observed in figure 3 for V_{oc}. The devices made with a very thin CdS layer ($t_{CdS} = 300$Å) gained over 30% in η as t_{i-SnO2} increased from zero to 1800Å.

The Effect of Buffer Layer Resistance

GPI's proprietary HRT layer has a resistivity in the 10^4 Ω-cm range, about four orders of magnitude higher than for the i-SnO$_2$ buffer layer made by LPCVD using a TMT precursor. To study the effect of buffer layer resistance, both buffer-layer thickness (t) and resistivity (ρ) must be considered. Several SnO$_2$ samples with a similar thickness to GPI's HRT were made. The V_{oc} obtained from both types of samples was plotted as a function of ρ x t. Fig. 4 shows that when ρ x t is less than 10^{-4} Ω-cm^2, V_{oc} varied from 300 mV (with no CdS film) to 800 mV (with a CdS film thickness of over 300Å). When ρ x t is greater than 10^{-1} Ω-cm^2, like GPI's HRT film, the V_{oc} was not significantly affected by the CdS thickness. Whether there was a 900-Å-thick CdS film or no CdS at all, the V_{oc} values were about 800 mV (three data points are present in this range in figure 4). Because there was composition difference in between LPCVD-formed i-SnO$_2$ and GPI's high resistance SnO$_2$, we do not know yet whether the GPI buffer-layer works mainly because of its high resistance, or its chemical composition, or both. Further study in this area is needed.

SUMMARY

LPCVD-deposited SnO$_2$ films are very stable under a high-temperature condition. The optical and electronic properties of i-SnO$_2$ remains the same after a thermal annealing in H$_2$ ambient. The i-SnO$_2$ film has a different crystal orientation than the SnO$_2$:F film. However, we have not observed that the difference in crystal orientation affects the adhesion of the CdS film to the TCO substrate.

In varying the i-SnO$_2$ thickness from zero to 1800 Å and the CdS thickness from zero to 900 Å, we observe the following: for thin CdS films, the CdS/CdTe device performance (mainly V_{oc}) depends on the i-SnO$_2$ buffer-layer thickness. About a 30% gain in device efficiency can be obtained for a 300 Å CdS by increasing the i-SnO$_2$ layer thickness from 0 to 1800 Å. For moderate and thick CdS films, the CdS/CdTe device parameters were dominated by the CdS thickness and were not sensitive to the i-SnO$_2$ thickness.

Compared to GPI's HRT buffer layer, the LPCVD formed i-SnO_2 film has less of an effect on the CdS/CdTe device performance. Differences in buffer-layer resistivity and surface properties may contribute to the results. We are planning further study in this area.
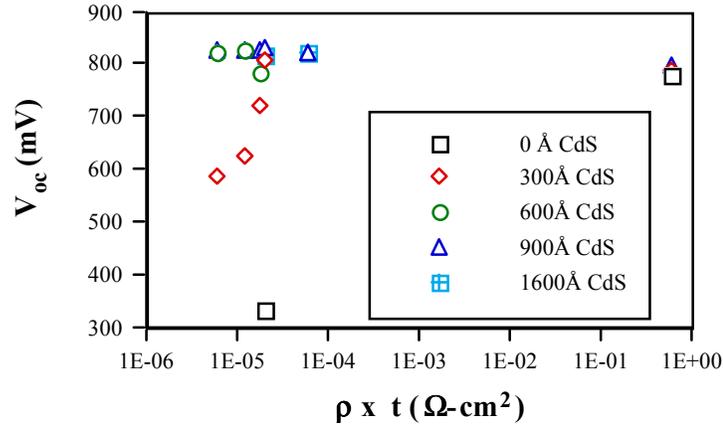
FIGURE 4. V_{oc} as a function of the product of resistance and thickness of high-resistance SnO_2 film.

ACKNOWLEDGMENTS

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