NREL/CP-520-25481

H Out-Diffusion and Device Performance in n-I-p Solar Cells Utilizing High Temperature Hot Wire a-Si:H I-Layers

A.H. Mahan, R.C. Reedy Jr., E. Iwaniczko,
Q. Wang, B.P. Nelson, Y. Xu, H.M. Branz, and R.S. Crandall
National Renewable Energy Laboratory

A.C. Gallagher
JILA, University of Colorado and NIST

J. Yang and S. Guha
United Solar Systems Corporation

Presented at the National Center for Photovoltaics Program Review Meeting
Denver, Colorado
September 8-11, 1998

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
A national laboratory of the U.S. Department of Energy
Managed by Midwest Research Institute
for the U.S. Department of Energy
under contract No. DE-AC36-83CH10093

Work performed under task number PV804101

November 1998

Available to DOE and DOE contractors from:
Office of Scientific and Technical Information (OSTI)
P.O. Box 62
Oak Ridge, TN 37831
Prices available by calling 423-576-8401

Available to the public from:
National Technical Information Service (NTIS)
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161
703-605-6000 or 800-553-6847
or
DOE Information Bridge
http://www.doe.gov/bridge/home.html

Printed on paper containing at least 50% wastepaper, including 10% postconsumer waste

H Out-Diffusion and Device Performance in n-i-p Solar Cells Using High Temperature Hot Wire a-Si:H i-Layers

A. H. Mahan, R. C. Reedy Jr., E. Iwaniczko, Q. Wang, B. P. Nelson, Y. Xu, A. C. Gallagher*, H. M. Branz, R. S. Crandall, J. Yang**, and S. Guha**

National Renewable Energy Laboratory, Golden, CO 80401
** JILA, University of Colorado and NIST, Boulder, CO 80309*
*** United Solar Systems Corporation, Troy, MI 48084*

Abstract . Hydrogen out-diffusion from the n/i interface region plays a major role in controlling the fill factor (FF) and resultant efficiency of n-i-p a-Si:H devices, with the i-layer deposited at high substrate temperatures by the hot wire technique. Modeling calculations have shown that a thin, highly defective layer at this interface, perhaps caused by significant H out-diffusion and incomplete lattice reconstruction, results in sharply lower device FFs due to the large voltage dropped across this defective layer. We have therefore employed buffer layers designed to retard this out-diffusion. We find that an increased H content, either in the n-layer or a thin intrinsic low temperature buffer layer, does not significantly retard this out-diffusion, as observed by SIMS H profiles on devices. However, if this low temperature buffer layer is thick enough, the out-diffusion is minimized, yielding nearly flat H profiles and a much improved device performance. We discuss this behavior in the context of the H chemical potentials and H diffusion coefficients in the high temperature, buffer, n-, and stainless steel substrate layers. Finally, we report a 9.8% initial active area device, fabricated at 16.5Å/s, using the insights obtained in this study. Light soaking data are also reported.

INTRODUCTION

High temperature a-Si:H, deposited by the hot wire (HW) technique, has demonstrated very different structural and electronic properties, including a reduced Staebler-Wronski metastability, a different H NMR 'signature', improved structural ordering, and a dramatic reduction in film internal friction, which until now had been thought to be unachievable for an amorphous material [1-4]. The additional possibility of depositing such materials at high deposition rates [5] has only added to its attractiveness as a candidate for incorporation into a solar cell structure. However, to successfully incorporate this high substrate temperature (T_S) deposited HW i-layer into such a device, it is necessary to retard, or compensate for, the H out-diffusion that occurs, not only during the deposition process itself, but also as this i-layer is cooled. Indeed, SIMS H profiles on both i-layers and devices have consistently shown evidence of sizable H diffusion out both the front and the back of the i-layers, and a thickness series of intrinsic high T_S HW i-layers, as examined by Electron Spin Resonance measurements, showed a large defective layer at one or both of the i-layer surfaces [6]. In previous publications, we addressed the issue of the H out-diffusion from the top surface of the i-layer during the growth and cooling processes, and although we obtained initial n-i-p solar efficiencies on untextured stainless steel (SS) substrates (no top surface grids) as high as 6.8% [7], with a low (10%) Staebler-Wronski degradation, the resulting SIMS profiles on these devices still showed sizeable H diffusion out the back of the device. This remaining H out-diffusion presents a very different type of

problem, in that it is not readily accessible to the surface treatments that were successfully used at the top of the i-layer.

In this paper, we discuss the most tractable approach that we have developed to date to deal with this problem. We found that we were unable to retard the out-diffusion of H in the back of the cell using i-layers deposited entirely at the high T_S, which led us to the use of lower T_S buffer layers. When we increased the H content (C_H) in both the n-layer as well as in a *thin* intrinsic low T_S buffer layer, we were again unsuccessful in retarding this out-diffusion. All these devices had defective i-layer regions near the n/i interface, and therefore gave poor device efficiencies. However, if this low T_S buffer layer was thick enough, the out-diffusion from the high T_S layer was minimized, yielding nearly flat H profiles and a much improved device performance. We discuss this behavior in the context of the H chemical potentials (μ_H) and H diffusion coefficients (D_H) in the high temperature, buffer, n-, and SS substrate layers. We further suggest that H out-diffusion near the n/i interface occurs to some extent even in lower-temperature-deposited glow discharge (GD) devices, and that this may be one reason why plasma treatments and/or i-layer bandgap (H content) profiling at this interface improve device performance. Finally, we present our latest device results using these flat H profiles on textured back reflecting substrates.

EXPERIMENTAL DETAILS

The HW devices were deposited using a two chamber, load locked deposition system with a second generation HW reactor. All devices used low T_S (220°C) GD n-layers and high T_S HW i-layers. Standard HW deposition conditions [5] and top surface i-layer treatments [7] were used, with the only variable being the filament current, which varied from 14 amp to 16 amp, resulting in HW film deposition rates ranging from 5Å/s-22Å/s. No evidence of W contamination in the films has been observed. In order to measure the shape of the H profile of the HW i-layer and to correlate these profiles to device performance (FF), the n-i composite structures were deposited on flat SS, and were completed using (amorphous) GD p-layers and semitransparent Pd small area (0.05 cm^2) top contacts. All SIMS H profiles were measured on this type of device. Once we obtained the desired i-layer H profile shape, we switched to devices deposited on Ag/ZnO textured back reflecting substrates and incorporated μc-Si(p)/ITO top contacts. In this case, United Solar supplied the textured substrates, and the partial n-i structures, deposited at NREL, were then sent to United Solar for completion. Devices of two different sizes were examined. Initially, 0.05 cm^2 devices, without Au grid structures, were deposited on 1" x 1" substrates. However, excess shunting of these devices forced us to explore device deposition on larger area (2" x 2") substrates. This enabled larger area (0.25 cm^2) devices with Au grid structures to be examined. The initial IV and light soaking measurements (to 1000 hr under AM 1.5 light) on the larger area devices were performed by United Solar, and QE measurements confirmed the magnitude of the device J_{sc}'s.

RESULTS AND DISCUSSION

In our earlier device publication [7], with the high T_s n- and i-layers deposited sequentially by HW in our single chamber HW system, we showed that surface treatments can effectively address the problem of H out-diffusion from the top surface of the i-layer during the growth and cooling processes and, as a result, improve device

performance. We showed that by using the proper surface treatment, the small area (0.05 cm^2) n-i-p test devices on flat SS substrates (without top-surface grid structures) yielded initial efficiencies as high as 6.8%. Further, we also showed in that publication that the amount of degradation (10%) compared quite favorably with published results for GD devices containing i-layers of similar thickness (4000Å). The HW i-layer deposition rate in this case was 8Å/s. However, both quantum efficiency (QE) and high illumination intensity red light FF measurements suggested a problem with the red response. One candidate to explain this relatively poor red response was P tailing; indeed, SIMS P depth profiles showed consistent dopant tailing into the HW i-layer for devices fabricated in this single chamber HW system [7,8]. Since trace P doping throughout an i-layer (but without the defective layer at the n/i interface) had previously been shown to enhance the blue response of the device at the expense of the red response [9], we attempted to minimize this tailing by fabricating devices in a load locked, multi-chamber system. This paper details the results of these efforts.

In this pursuit, we attempted to limit the amount of H out-diffusion in the region of the n/i interface (as well as that out the front of the i-layer), thus eliminating the need to introduce a 'density' of P donors which had previously been shown to 'compensate' the defects generated by incomplete lattice reconstruction after the diffusion of H out of this region [6-8]. Our goal, then, was to produce a flat H SIMS profile throughout the region of the HW i-layer, with the hope of obtaining a substantial improvement in device performance.

Our first attempt to do this involved the introduction of a thin (500Å), lower T_S buffer layer into the device at the n/i interface. We hoped that this layer would not only retard the out-diffusion of the H from the higher T_S layer, but would also serve as a

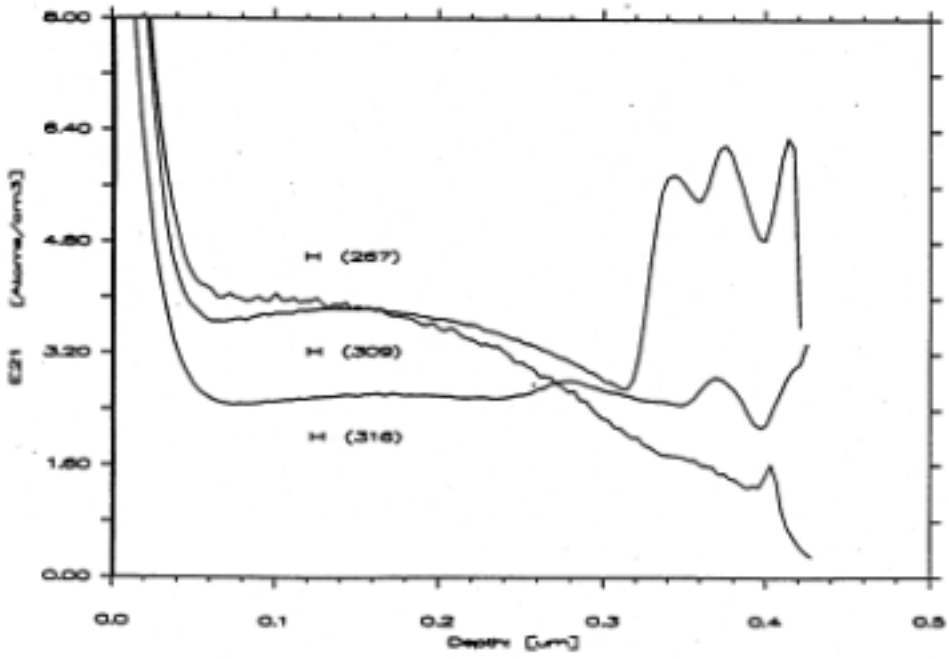

FIGURE 1. SIMS H profiles vs. depth into device. The buffer layers and n-layers are towards the right hand side of the profiles, with the n-layers located at depths of ~0.35-0.40 μm and the buffer layers (where appropriate) directly to the left of the n-layers. The device numbers are indicated, and the i-layer deposition conditions and device performance are shown in Table 1.

source of H which would spill over into the high T_s region and replace any H in this region which had diffused out. Figure 1 shows SIMS curves (plotted on a linear scale to emphasize the shape of the H profiles) for three devices, the first using a high T_s layer (no buffer), the second using a thin (500Å) lower T_s buffer layer, and the third using a thicker (1000Å) lower T_s buffer layer. As can readily be seen by comparing the first two profiles, in spite of the significantly higher C_H in the thin buffer layer (device 309), which was further enhanced by H from the filament during heating of the layer to the high T_s value, the diffusion out of the high T_s layer seems to be only slightly retarded. Indeed, the H in the high T_s layer diffuses towards the back of the device, apparently right through the buffer layer as if it was not even there. It is only when the buffer layer is quite thick (device 316) that the H out-diffusion in the high T_s layer is significantly retarded. The first four rows of Table I show the device FF vs. I-layer configuration, all for HW i-layer deposition rates of 5-8Å/s (14 amp filament current). These small area devices used GD amorphous n- and p-layers and semitransparent Pd top contacts; thus, the white light FF's were obtained for J_{sc}'s in the range 4.5-5.0 mA/cm^2. As can be seen, flattening the shape of the SIMS H profile by using a thick low T_s buffer layer increases the device FF significantly.

We propose to explain the out-diffusion behavior in terms of the H diffusion coefficients (D_H) and chemical potentials (μ_H) [10] of the different layers. It is well established that D_H in an n-layer is considerably higher than that in an a-Si:H intrinsic layer [11], most likely because of the high electronic Fermi level. In addition, because the n- and i-layers are connected in a device configuration, we expect that the high D_H values extend at least some distance into the intrinsic layer. However, the differences in D_H alone are not sufficient to explain the results in Fig. 1; one must also explain why the H diffuses toward the back of the device. Certainly the back of the device is a huge sink for H, due to the exceedingly high D_H for SS [12], and probably determines the direction of the H out-diffusion. This causes μ_H to decrease toward the rear of the cell, starting from the high T_s i-layer region where the diffusion is first noted, and continuing through the buffer and n-layers right into the SS substrate. That is, differences in μ_H between the layers control the direction of the H flow, and the respective D_Hs, which depend upon many factors including the local electronic Fermi energy and the extent of the H depletion, determine the rate. Thus, the only way to minimize D_H in the high T_s i-layer of the device is to make the buffer layer thick enough to avoid having the high D_H region extend all the way into the high T_s i-layer.

Device #	i-layer configuration (H profile)	deposition rate (Å/s)	FF
267	complete high T_s layer	5-8Å/s	.51
309	thin low T_s buffer	"	.49
316	thick low T_s buffer - flat H profile	"	.59
401	thick low T_s buffer - flat H profile (best FF@5-8Å/s)	"	.62
449	thick low T_s buffer - flat H profile (best FF@16-22Å/s)	16-22Å/s	.65

TABLE 1. Small area device performance vs. i-layer configuration. Deposition conditions leading to a flat H profile are noted, and the i-layer deposition rates are indicated.

Perhaps surprisingly, μ_H can be lower in certain layers despite their relatively higher C_Hs. This may be caused by structural differences between the layers [13]. We are currently examining this diffusion behavior with the aid of thin deuterium (D) profiles having been deposited both very near to and far away from the n-layer, where we are using SIMS to look at the D diffusion vs. distance from the n-layer in an actual device structure. We also point out that this phenomenon (enhanced H out-diffusion near the n/i interface) can occur to some extent even in lower-temperature-deposited GD devices, and that this may be one reason why plasma treatments and/or i-layer bandgap (H content) profiling at this interface improves device performance [14].

Finally, we report the latest results for our solar cell efficiencies, using the flat H i-layer profiles that we have generated using this procedure. As shown in the last row of Table I, when we increased the filament current from 14 amp to 16 amp, we not only increased our film deposition rate significantly, but also improved our small area device performance, and hence we used this higher filament current in our solar cell efficiency study [15]. As described above, our n-i composite structures were deposited on United Solar's Ag/ZnO coated SS back reflectors, and the partially finished devices were shipped to United Solar for their μc-Si(p)/ITO top contacts. The best initial active area efficiency (η) achieved to date for the larger area (0.25 cm^2) devices is 9.8%. The IV parameters for this device are V_{oc}=.926 V, J_{sc}=16.13 mA/cm^2 (as confirmed by QE measurements), and FF=.657. The i-layer deposition rate for this device was 16.5 Å/s.

These results should be put into context. First, taking state-of-the-art GD device parameters before light soaking to be in the range of V_{oc}=.90-1.0 V, J_{sc}=17.0-17.5 mA/cm^2, and FF>0.70, it is seen that an average initial η for such a device is ~ 11.0-11.5%. Thus, the present initial η value reported here for the HW device is not yet as good as its GD counterpart. Further, the 9.8% value is also not too different from a recent initial value reported for a p-i-n device using a HW i-layer [16]. However, two important distinctions must be made. First, both the previously mentioned GD and HW cells were fabricated at much lower deposition rates than that for the present device, on the order of 1-2Å/s for the GD device and ~3Å/s for the HW device. Indeed, we believe that our present results represent the highest initial η to date for deposition rates > 6Å/s utilizing silane as the source gas [17]. The latter issue is also important to consider in view of the fact that materials costs (source gases) as well as deposition rates can play vital roles in reducing the capital cost per delivered watt in commerial production facilities. Second, whereas the HW device in Ref. 16 used an i-layer deposited at a relatively low T_s, we have persisted in attempting to incorporate the high T_s HW i-layers into a device structure, because it is these high T_s layers that we believe have the potential of showing a reduced Staebler-Wronski metastability in a commercially viable device structure, and not just in a simple test structure [7].

Light soaking tests on our devices have just begun. In this preliminary study, United Solar selected four devices for light soaking, with initial efficiencies ranging from 9.6% to 9.07%. The most stable device to date exhibited an initial efficiency of 9.07% and degraded after 1000 hr of light soaking to an efficiency of 7.71%, a drop of 15%. Although this rate compares quite favorably with other high deposition rate materials, an additional problem was identified. That is, these devices all incurred a drop in FF (efficiency) between the time they were initially measured and the time the light soaking study was initiated. We believe this initial efficiency drop may be due to an interface instability, as companion Schottky n-i structures do not exhibit this behavior. This issue is currently being investigated.

CONCLUSIONS

Hydrogen out-diffusion from the n/i interface region is shown to play a major role in controlling the FF and resultant efficiency of SS/n-i-p a-Si:H devices, where the i-layer is deposited at high T_s by the HW technique. We address this problem by using lower T_s buffer layers introduced into the n/i interfacial region. We find that an increased C_H, either in the n-layer or in a thin buffer layer, does not significantly retard this H out-diffusion. Indeed, the H in the high T_s layer diffuses right through the high C_H buffer layer, moving towards regions of lower μ_H. All these devices exhibit poor cell efficiencies. However, if this low T_s buffer layer is thick enough, the out-diffusion in the high T_s layer is minimized, yielding nearly flat H profiles and a much-improved device performance. Using the SIMS H profiling information so obtained, we report on our latest device results. Using a filament current of 16 amp, giving us an i-layer deposition rate of 16Å/s, we obtain an initial device active area efficiency of 9.8%. We believe this is the highest initial device efficiency ever obtained at deposition rates greater than 6Å/s. Light soaking studies on these devices have been initiated.

ACKNOWLEDGEMENTS

The NREL work is supported by DOE under Subcontract DE-AC36-83CH10093, and that at United Solar by NREL subcontracts ZAN-4-13318-02 and ZAK-8-17619-09.

REFERENCES

1. A. H. Mahan and M. Vanecek, AIP Conf. Proc. 234, 211 (1991).
2. Y. Wu, J. T. Stephen, D. X. Han, J. M. Rutland, R. S. Crandall, and A. H. Mahan, Phys. Rev. Lett. 77, 2049 (1996).
3. A. H. Mahan, D. L. Williamson, and T. E. Furtak, MRS Symp. Proc. 467, 657 (1997).
4. X. Liu, B. E. White Jr., R. O. Pohl, E. Iwaniczko, K. M. Jones, A. H. Mahan, B. N. Nelson, R. S. Crandall, and S. Veprek, Phys. Rev. Lett. 78, 4418 (1997).
5. A. H. Mahan, J. C. Carapella, and A. C. Gallagher, U.S. Patent 5,397,737 (1995).
6. T. Unold, R. C. Reedy Jr., and A. H. Mahan, 17th ICAMS, Budapest, 1997, to appear in J. non-Cryst. Sol. (1998).
7. A. H. Mahan, E. Iwaniczko, B. P. Nelson, R. C. Reedy r., T. Unold, R. S. Crandall, S. Guha, and J. Yang, AIP Conf. Proc. 394, 27 (1996).
8. A. H. Mahan, R. C. Reedy Jr.,, E. Iwaniczko, Q. Wang, B. P. Nelson, Y. Xu, A. C. Gallagher, H. M. Branz, R. S. Crandall, J. Yang, and S. Guha, Proc. 1998 MRS Spring Conference, in press.
9. W. Kusian, W. Kruhler, and B. Bullemer, Proc. 19th IEEE PV Spec. Conf., 577 (1987).
10. R. A. Street, Phys Rev B, 43, 2454 (1991).
11. D. E. Carlson and C. W. Magee, Appl. Phys. Lett. 33, 81 (1978).
12. T.-P. Perng and C. J. Altstetter, Acta. Metall. 34, 1771 (1986).
13. W. Beyer and U. Zastrow, Proc. MRS Symp. 420, 497 (1996).
14. J. Yang, private communication.
15. From optical pyrometer measurements, filament currents of 14 amp and 16 amp correspond to approximate filament temperatures of 1930°C and 2100°C respectively.
16. S. Bauer, W. Herbst, B. Schroeder, and H. Oechsner, Proc. 26th IEEE PV Spec. Conf., 719 (1997).
17. S. Jones (private communication) reports an initial η of 10.6% for an a-Si:H device using the VHF-GD deposition technique, at deposition rates of 6Å/s.