From Modules to Atoms: Techniques and Characterization for Identifying and Understanding Device-Level Photovoltaic Degradation Mechanisms

Steve Johnston,[1] Helio Moutinho,[1] Chun-Sheng Jiang,[1] Harvey Guthrey,[1] Andrew Norman,[1] Steven P. Harvey,[1] Peter Hacke,[1] Chuanxiao Xiao,[1] John Moseley,[1] Dana Sulas,[1] Jun Liu,[1] David Albin,[1] Marco Nardone,[2] and Mowafak Al-Jassim[1]

1 National Renewable Energy Laboratory

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Contract No. DE-AC36-08GO28308

Technical Report
NREL/TP-5K00-72541
October 2019

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Suggested Citation
Johnston, Steve, Helio Moutinho, Chun-Sheng Jiang, Harvey Guthrey, Andrew Norman, Steven P. Harvey, Peter Hacke, Chuanxiao Xiao, John Moseley, Dana Sulas, Jun Liu, David Albin, Marco Nardone, and Mowafak Al-Jassim, 2019. *From Modules to Atoms: Techniques and Characterization for Identifying and Understanding Device-Level Photovoltaic Degradation Mechanisms*. Golden, CO: National Renewable Energy Laboratory. NREL/TP-5K00-72541. https://www.nrel.gov/docs/fy20osti/72541.pdf.

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National Renewable Energy Laboratory
15013 Denver West Parkway
Golden, CO 80401
303-275-3000 • www.nrel.gov

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Acknowledgments

We thank Neelkanth Dhere of the Florida Solar Energy Center for providing valuable discussions and examples of outdoor degraded modules; Jeff Aguiar for TEM measurements; Adam Stokes for APT measurements at the Colorado School of Mines (CSM); Dirk Jordan of NREL for providing an example of an outdoor degraded module; Jeff Squier, Nathan Worts, and Alyssa Allende Motz at CSM for evaluating laser cutting techniques; Rofin-Sinar and KM Labs for their attempts at laser cutting photovoltaic module tempered glass; Andreas Gerber (Jülich Research Center, Germany) for his contributions to reverse-bias testing and imaging; and Elizabeth Palmiotti (CSM) for her contributions to reverse-bias imaging.

This work was authored in part by Alliance for Sustainable Energy, LLC, the manager and operator of the National Renewable Energy Laboratory for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding provided by U.S. Department of Energy Office of Energy Efficiency and Renewable Energy Solar Energy Technologies Office. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes. This work was also supported by project DE-EE0007141 of PREDICTS2, and by the German ministry for Economic Affairs and Energy (BMWi) under the contract FK0325724A (OptiCIGS) and by the NREL-Helmholtz "Impuls und Vernetzungsprojekt" HNSEI (SO-075). This material is based on work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under Solar Energy Technologies Office (SETO) Agreement Number 30304.

List of Acronyms

AFM	atomic force microscope/microscopy
APT	atom probe tomography
CIGS	$CuIn_xGa_{1-x}Se_2$
DLIT	dark lock-in thermography
EBIC	electron-beam induced current
EDS/EDX	energy-dispersive X-ray spectroscopy
EELS	electron energy-loss spectroscopy
EL	electroluminescence
EVA	ethylene vinyl acetate
FF	fill factor
FIB	focused ion beam
IEC	International Electrotechnical Commission
ILIT	illuminated lock-in thermography
I_{SC}	short-circuit current
I-V	current-voltage
KPFM	Kelvin probe force microscope/microscopy
LIT	lock-in thermography
μ-PCD	microwave photoconductive decay
NREL	National Renewable Energy Laboratory
PID	potential-induced degradation
PID-s	potential-induced degradation – shunting
PL	photoluminescence
PV	photovoltaics
R_S	series resistance
R_{SH}	sheet resistance
SEM	scanning electron microscope/microscopy
SIMS	secondary-ion mass spectrometry
STEM	scanning transmission electron microscope/microscopy
TCE	trichloroethylene
TCO	transparent conducting oxide
TEM	transmission electron microscope/microscopy
TFE	thermionic field emission
TOF-SIMS	time-of-flight secondary-ion mass spectrometry
TPT	Tedlar-polyester-Tedlar
VBM	valence band maximum
V_{OC}	open-circuit voltage

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Executive Summary

This report documents how degraded modules are analyzed for cell-level performance reduction using combinations of spectroscopic imaging, numerical modelling, and high-resolution microscopy. The primary degradation topics presented here are 1) potential-induced degradation, 2) defect metastability and impurity diffusion, and 3) partial-shading-induced reverse-bias breakdown.

1) Potential-induced degradation is caused by the high voltage between the semiconductor device within the module and the electrical ground level (frame and packaging). Impurities from the glass drift toward and accumulate within the semiconductor device. We report the detection of sodium in crystal structures that lead to shunt formation in silicon modules. We model the shunts using experimental data, and our results suggest that thermionic emission currents at the defect interfaces are responsible for semi-shunting device behavior. We find that these shunt defects return to non-shunted regions during an electron-beam anneal as sodium accumulates near the silicon interface.

2) Thin-film modules such as CdTe are particularly susceptible to defect metastability and impurity diffusion. Imaging reveals degradation across a stressed CdTe module subjected to light and heat. Reduced cell performance correlates to increased Cu concentration at the front interface. Numerical modeling and measurements agree that the increased Cu concentration at the cell's p-n junction also correlates to a smaller space-charge region. Copper movement during the module's lifetime leads to some beneficial increase in doping, but to a larger extent, the increase in Cu impurity concentration near the cell's p-n junction correlates to a loss in the cell voltage and decrease in CdTe performance.

3) Reverse-bias breakdown can be caused by partial shading of the module during operation. Thin-film modules typically lack bypass-diode protection, so the induced reverse current in a shaded region of the module can become concentrated in localized defects. Such currents can locally generate extreme heat that propagates damage within the cells. We present a new method to detect early-breakdown cell regions using lock-in thermography to image heating under high reverse-bias voltages with current limited to prevent irreversible damage. We identify several built-in defects as likely culprits for initiating breakdown damage, including small pinholes and voids in the absorber layers of the device.

The cornerstone of the studies presented in this report is the use of multiple characterization techniques to locate the defects responsible for module-level degradation and track those defects down to the atomic scale. Optical imaging techniques—such as electroluminescence imaging, photoluminescence imaging, and lock-in thermography—provide spatial information of full modules on the meter scale. Areas of interest can then be imaged with higher spatial resolution by zooming in to millimeter-scale fields of view. We document procedures for coring cell samples from selected regions of interest using mechanical drilling. The small samples are then of suitable size for various microscopic analyses using techniques such as scanning electron microscopy, time-of-flight secondary-ion spectrometry, atomic force microscopy, electron-beam induced current, transmission electron microscopy, and atom probe tomography, which can provide chemical, structural, and electrical characterization down to the atomic scale.

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1 Introduction

As photovoltaic (PV) technologies mature and deployment rapidly increases, the issues of reliability and bankability become increasingly important. Improving module reliability and service lifetime will lead to significant reductions in financing risks and PV system costs. Weathering can cause materials to degrade outdoors, and PV module degradation can be described in three phases: infant mortality, mid-life failure, and wear-out failure [1]. The common infant-mortality failures are due to junction-box detachment or breakage, cable or connector failure, glass breakage, defective cell interconnects, loose frames, corrosion, and delamination [1]. International Electrotechnical Commission (IEC) standards describe module designs and tests to establish a minimum value of quality and performance. There are many standards for PV modules, and ongoing updates and editions continually address known stresses and failure issues. Some examples are IEC 61215, 61646, and 61730 for construction and general testing. Others pertain to transportation (62759), salt mist (61701), mechanical loading (62782), and system voltage (62804). IEC standards largely screen for infant-mortality issues but may not guarantee that modules will not eventually show significant degradation [2,3]. IEC standards continue to be refined and some may even become climate-specific (IEC 62892). For example, in various climates with high humidity and heat, potential-induced degradation (PID) may be considered a critical factor for PV performance and reliability; however, in other climates that are more arid and moderate, PID may be a less important consideration [2].

Many of the infant-mortality failures listed above can be visually observed, but transportation and shipping damages can also occur and may not be as readily apparent. For this reason, financiers and owners may request or require more advanced characterization, such as electroluminescence [4], or thermal imaging. These imaging techniques can also be used to detect broken and cracked cells even when glass is not broken or the backsheet is not visibly damaged. Although some degradation mechanisms such as encapsulant discoloration can be visually inspected, imaging techniques can detect degradation mechanisms that reduce solar module performance but are not visually apparent. In addition to cracked cells, some other types of these defects include hotspots and bypass-diode failures. This report documents examples of cell-level degradation where the semiconductor PV device has changed, often with microscopic or below-surface defects that are not readily identified by visual inspection. Examples of these types of degradation include the following:

- Potential-induced degradation causing shunts (PID-s)
- Initial metastabilities and degradation due to diffusion of elements
- Hotspots and partial-shading-induced breakdown and permanent damage

Electronic reliability issues lead to module power losses that develop from mechanisms such as PID, metastabilities of materials, impurity diffusion, and reverse-bias breakdown due to partial shading. Although current-voltage (I-V) curve analysis—and deduced factors from it, such as open-circuit voltage, V_{OC}; short-circuit current, I_{SC}; fill factor, FF; shunt resistance, R_{SH}; and series resistance, R_S—has been the main tool in degradation studies, direct evidence and analysis of the defects provides information and data for enhanced modeling, characterization, and understanding of the degradation mechanisms. This direct evidence is collected from modules that have shown degradation outdoors under actual operating conditions. In this report, the defects responsible for degradation are then studied on a scale from meters to millimeters by imaging techniques and from millimeters to atomic scales using various microscopy techniques.

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2 Imaging Techniques

Several camera imaging techniques have been applied to the characterization of PV modules. The imaging techniques include photoluminescence (PL) imaging [5], electroluminescence (EL) imaging [6–10], illuminated lock-in thermography (ILIT) [11], and forward- and reverse-bias dark lock-in thermography (DLIT) [12]. For PL imaging and ILIT, an optical excitation source is used to excite excess carriers in the semiconductor device. For EL imaging and DLIT, excess carriers are injected by applying voltage and current to the modules and cells under test. In both cases, a dark environment reduces background noise to help collect an image with optimized signal-to-noise ratio. For small samples, a light-tight box enclosure is used for imaging and to contain laser light when needed. Cameras in the enclosure are shown in Figs. 1(a) and 1(b). For large modules, a laser-curtain enclosure is used for imaging, as shown in Fig. 1(c). The camera is mounted on a scaffolding of motorized rails and can be moved far enough away to image an entire module within the field of view. This is useful for full-module EL and DLIT images. For PL and ILIT, the laser light sources have limited power to illuminate a large area. In these cases, a smaller field of view is used, such as the size of a cell within the module. The automated stages step from area to area to collect images across the entire module, which can then be stitched together to form a full-module PL or ILIT image.

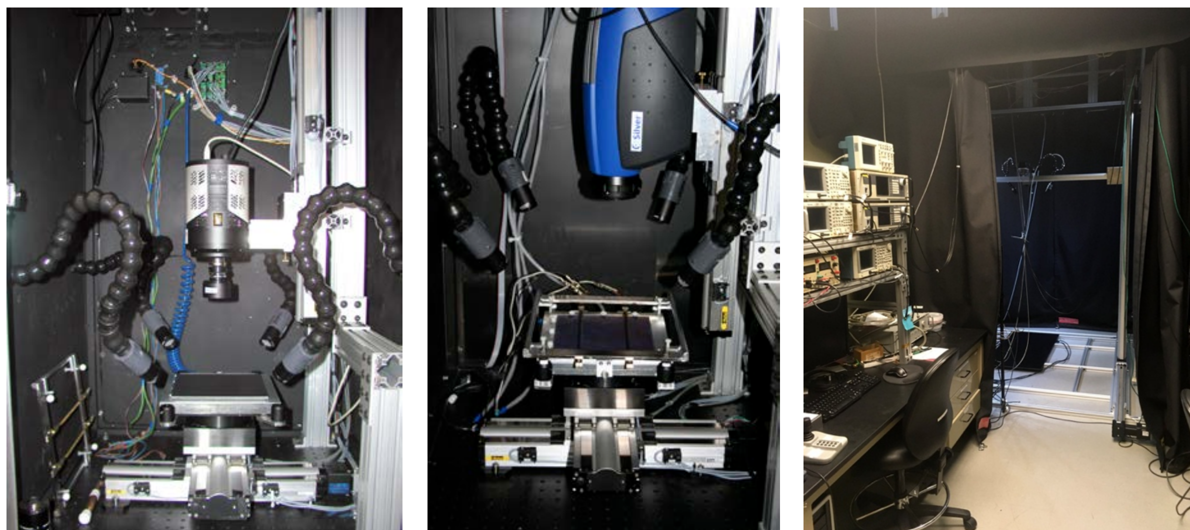

Figure 1. (a) Si CCD camera: Princeton Instruments PIXIS 1024BR, silicon charge-coupled device (CCD) 16-bit camera with 1024×1024 pixels (13-mm pixel pitch), cooled to ~ -60ºC, (b) InSb thermal camera: Cedip Silver 660M/FLIR SC5600-M InSb 14-bit lock-in camera with 640×512 pixels (15-mm pixel pitch), cooled to ~80 K. (c) laser-rated curtain enclosure with motion stages for imaging modules and large samples in a dark, laser-controlled area.

For PL imaging, we use a Princeton Instruments/Acton PIXIS 1024BR camera having 1024×1024 pixels, as shown in Fig. 1(a). A Schneider Optics Cinegon 1.8/16-mm compact lens gives a wide field of view for imaging modules with typical sizes up to 1 or 2 m from about 2 m away. A Schneider Optics 50-mm macro imaging lens with extension rings from 0 to 125 mm is used for imaging fields of view of about 150 mm (Si cell size) from less than 1 m away to 5 mm when using the full length of extension rings and the camera lens close to the sample. A Navitar 6X ultrazoom lens with a 20X Mitutoyo microscope objective combination is used for fields of view from 2 mm down to 200 µm. The camera is cooled to about -70°C. The optical excitation source used for PL imaging is composed of 30-W, 808-nm laser diode units coupled to optical fibers. The

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fibers are then coupled to collimators and engineered diffusers and emit from opposite angles to provide uniform excitation over the area of the sample. For materials with a suitable bandgap near 1 eV, such as silicon and CIGS, the 808-nm excitation light is used for PL imaging. For materials with larger bandgaps near 1.5 eV, such as CdTe and GaAs, laser diodes with shorter wavelengths such as 532 nm are used for optical excitation. When the short-wavelength lasers have limited power to expand over a large area, scanning galvanometer mirrors are used to sweep light over the sample area during a long camera exposure time. To block reflected light from the sample and stage area, long-pass filters are mounted to the camera lens. For EL imaging, the filters can be removed because the camera and sample are housed in a light-tight enclosure.

Both PL and EL intensities depend on the sample's material quality, defects, surface passivation, and excitation intensity. For PL imaging, surface reflection and material light absorption and thickness are also factors. With about 1-sun intensity of the 808-nm light, images can be collected with exposure times ranging between 1 and 30 seconds. For EL imaging, currents ranging from a few mA/cm^2 up to 45 mA/cm^2 are driven by a power supply through each cell while in the dark. Camera exposure times range from seconds to minutes. To compare various samples and plot them together, images are background-corrected and factored to account for different exposure times.

Lock-in thermography images are collected using a FLIR/Cedip Silver SC5600 InSb infrared camera with built-in lock-in detection as shown in Fig. 1(b). This 640×512-pixel detector is cooled to -190°C and has a spectral response of 3.6–5.1 µm. For ILIT imaging, the 808-nm laser diode optical excitation source is pulsed on and off instead of the constant illumination used for PL imaging. The camera can acquire frames at a rate of up to 100 frames per second and the camera's lock-in electronics are triggered at the same frequency as the light source, typically between about 0.5 Hz and 30 Hz, with a square wave. DLIT images are similarly acquired using voltages applied to the device instead of light. In forward bias, current flows throughout the device, causing the entire cell to rise slightly in temperature. Weak diodes or shunts can heat up above the background temperature and become detected in the DLIT image. In reverse bias, only small currents would typically flow, but shunts or diode breakdown can create a path for larger currents. These features are therefore more easily detected. For both forward- and reverse-bias DLIT, the excitation frequency is typically in the same 0.5 Hz to 30 Hz range. Depending on signal strength, lock-in thermography images are collected and averaged for a few seconds to minutes. The lock-in analysis produces amplitude and phase images of the cell and defect heat signatures.

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3 Locating and Coring Areas of Interest

The most relevant study of module reliability is to investigate defects on modules that have shown degradation outdoors under actual operating conditions. Figure 2 shows an example of a silicon module that has been weathered outdoors and experienced degradation classified as PID-s. Cells mostly located near the frame appear dark in the EL image. These same cells often show localized heating in the DLIT image of Fig. 2. These defect areas are located using imaging techniques and can then be identified or classified as defects of interest to study.

Once the defect areas are selected, their locations are marked on the module. Zoomed-in images are collected using the motion stages of the module imaging enclosure and provide higher spatial resolution and more accurate locations of the defective regions. Examples of zoomed-in EL and DLIT images are shown in Fig. 3. Selected areas of interest are shown with circles in the DLIT image of Fig. 3.

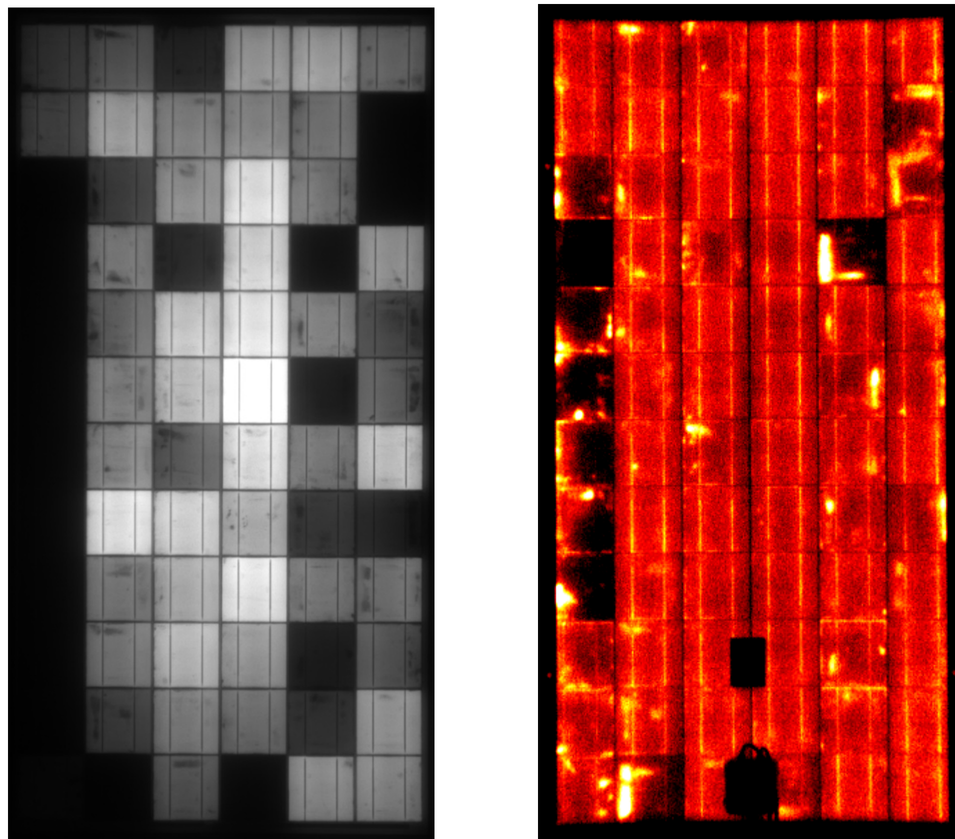

Figure 2. Images of a PID-affected 205-W crystalline-Si module from the field. The EL image (left) is collected using 2-A current in forward bias with 5-s exposure time. The DLIT image (right) is collected using 5-A forward bias pulsed at a frequency of 0.5 Hz, averaged for 2-min imaging through the backsheet.

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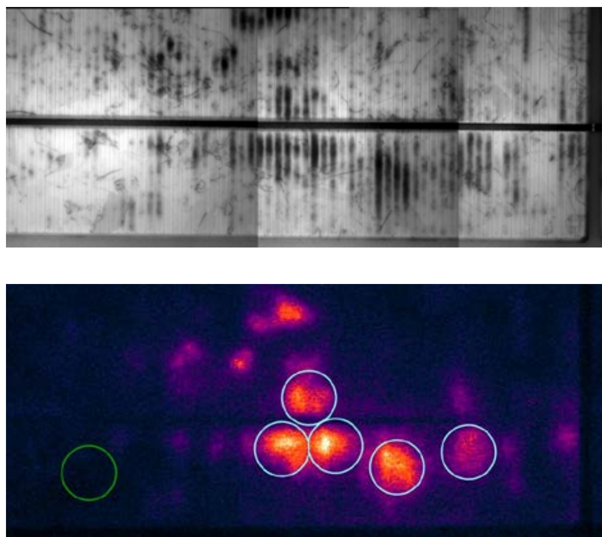

Figure 3. Zoomed-in images of a multicrystalline-Si cell from an outdoor-stressed module showing PID degradation. The top image shows stitched-together EL images where dark spots indicate carrier recombination and shunting. The bottom image is a forward-bias DLIT image of the same area where bright areas indicate current flow due to carrier recombination and shunting. Circles on the DLIT image identify possible coring locations for defects (blue) and a non-defect area (green) for comparison.

Once the areas of interest are marked, we core them out of the module for further microscopic study. The construction of silicon-wafer-based modules typically consists of cells encapsulated between layers of ethylene vinyl acetate (EVA) with glass on the front and a weather barrier sheet, Tedlar-polyester-Tedlar (TPT), on the back. We investigated options to core samples from the modules using traditional diamond-based drill bits or more modern laser-cutting techniques. We worked separately with the Colorado School of Mines (CSM) and Rofin-Sinar (recently purchased by Coherent) to experiment with laser cutting of the tempered glass for coring modules. Pulsed fiber lasers cannot cut tempered glass the way they are used to cut non-tempered glass, so a filamentation process is used for tempered glass. SmartCleave™ (Rofin-Sinar) is a kerfless separation process for strengthened (chemically and thermally) and non-strengthened glass of 100-µm to 10-mm thickness and other brittle materials. We attempted to cut the tempered glass of modules by the filamentation (SmartCleave) process. In this cutting process, a 10-µm-diameter beam is focused into the center of the glass thickness, and a 1-µm hole propagates through the thickness of the glass. The hole can be perpendicular for straight cuts or angled for tapered sections such as cutting a circular disk from a sheet. Up to ½"-thick glass can be cut, so the 2- to 3-mm thickness of tempered glass typically used in PV modules seemed feasible. The cutting laser is a ps-pulse laser, typically using an infrared wavelength for non-tempered glass and green for tempered.

Although the filamentation process seemed promising for coring samples from PV modules with tempered glass, there were still challenges that prevented implementation of this method. First, the process cannot initiate a filament on a non-smooth surface due to laser light refraction. PV solar panels tend to use textured glass. To overcome this challenge, the textured glass of a small commercial Si PV module was polished smooth on the top surface. We also tested the process on a small sample of smooth tempered glass of nominally the same thickness used in typical PV modules. When attempting to cut glass on each of these sample types using the filamentation process, both broke during cutting. The technique is successful for cutting gorilla glass (before and after hardening), which is a chemical and thermal hardening process, and sometimes successful for cutting light to moderate tempered glass. However, because PV modules must withstand

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outdoor stresses, the glass is strongly tempered, and today's state-of-the-art laser-cutting techniques were not able to successfully extract samples without shattering the entire glass panel.

Despite the challenges with laser cutting, we successfully developed techniques to fully core through the modules using mechanical drilling. In Fig. 4, we show our early results in which shattering of the tempered glass layer caused the cored cells to break into smaller pieces. However, as we discuss below, we further developed a multi-stage coring procedure to avoid cutting and breaking the tempered glass and allow the extraction of full pieces.

During our early coring trials, we found that a small cut on the tempered glass, outside the areas of interest, initiates the glass to shatter and crack into small pieces, which are still held in place by the EVA. The panel is then cored using a hollow, diamond-based bit and a water-circulated drill, where the coolant prevents overheating of the drill bit and sample and flushes glass bits from the cutting area. Whole pieces with the internal diameter of the coring bit can be cut from Si solar panels. However, the tempered glass on those samples is broken in smaller pieces due to the previous shattering. We then use trichloroethylene (TCE) heated at 60°C to dissolve the EVA that encapsulates both sides of the panel, allowing us to remove the Si layer from the cored samples. Heating accelerates the EVA removal, but less heat and more time may be used to ensure that any temperature-sensitive defects are not changed during the coring process. Likely because of the stress caused by the broken tempered glass, the solar cell is broken into pieces during the EVA removal process, as observed in Fig. 4. Despite being broken in small pieces, these samples are typically large enough for planned analysis using zoomed-in imaging and microscopy techniques. No additional damage was observed within the fragments, and the solar cell pieces generated a voltage when illuminated.

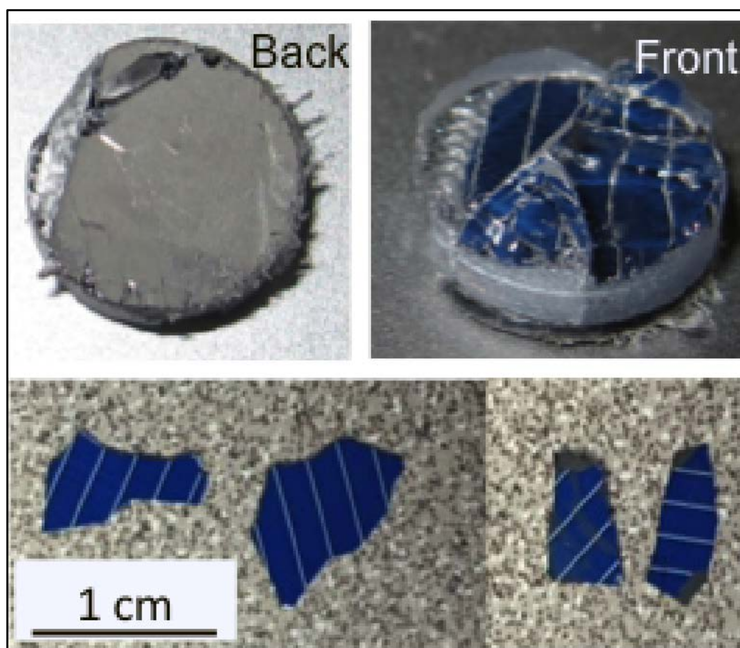

Figure 4. (a) Small pieces of a Si solar panel after full coring (top: whole cored sample; bottom: pieces of the solar cell after the removal of the EVA encapsulation layer and tempered glass).

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Since the front glass is typically tempered or strengthened, which shatters across the entire area when mechanically penetrated or cut, we developed an alternate method of only cutting through the backsheet and silicon cell. The defect locations are marked on the backsheet of the module as shown in Fig. 5. Because the backsheet will be removed at the defect areas, a duplicate paper map is taped in place such that it can be folded away and then back over to overlay on the areas of interest. The defect areas can then be relocated after backsheet removal.

Figure 5. Regions of interest for coring are marked directly on the backsheet of a silicon module. Paper duplicate maps are taped in place so that the regions can be accurately relocated after removing the backsheet in the coring locations.

For our new partial coring technique, we core only part of the panel structure and use a metallic post attached to the cored area to remove the sample from the module. This process avoids breaking the tempered glass, since the front glass panel is left in place and not removed with the core. The steps during the partial-coring procedure are listed below and shown with photos in Fig. 6.

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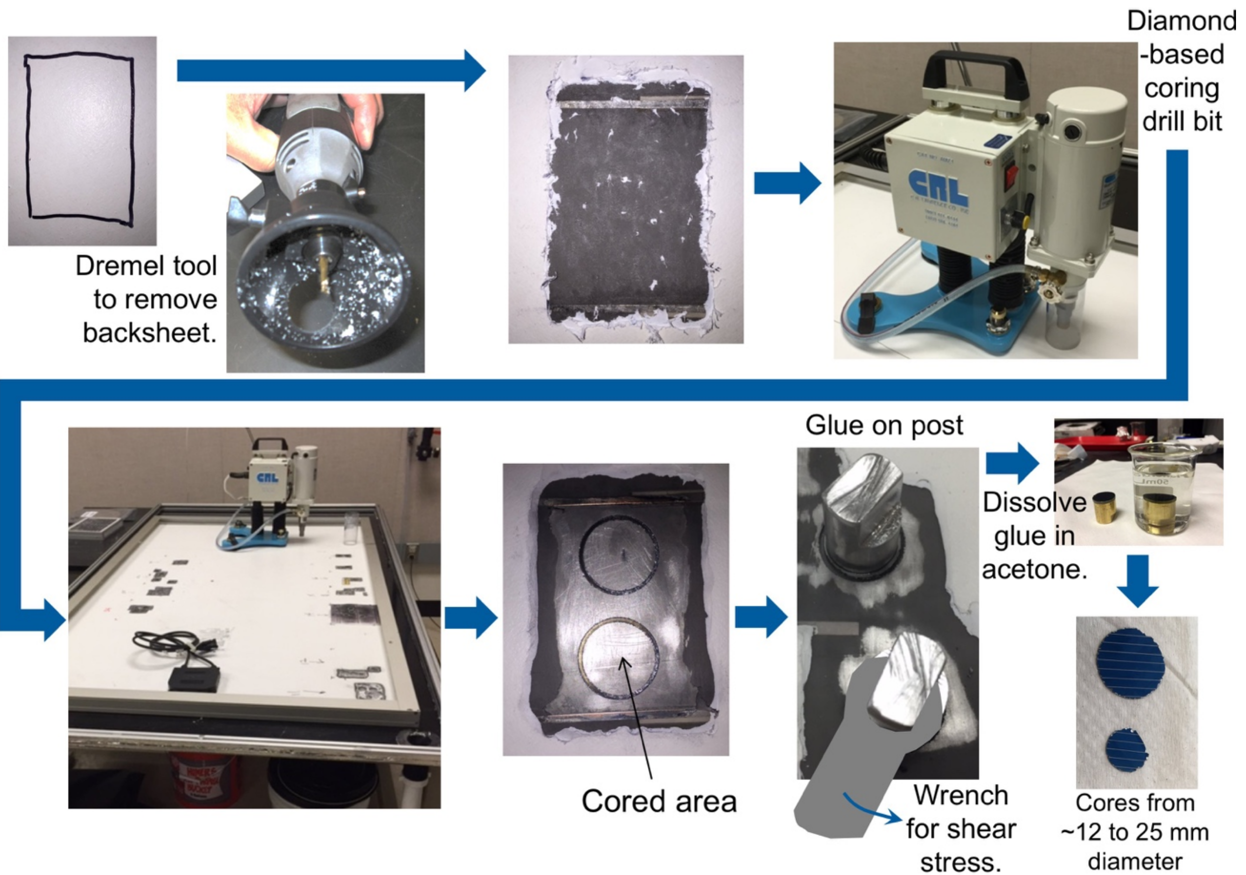

Figure 6. Process for partial coring of selected areas from Si modules having a backsheet. The upper left photos show an area of the backside of a silicon module where the backsheet has been removed with the Dremel rotary tool. A diamond-based coring drill (upper right photo) is shown on the backside of a silicon module in the lower left photo. The drill can be moved and aligned to cut selected defect areas and fixed in place using suction cups. The lower middle photo shows a silicon cell section where the backsheet has been removed and the coring drill has cut a circular perimeter around the defect area. The lower right photos show metal rods glued onto the circular cell sections to be extracted, Si solar cell samples after partial coring, and samples detached from the posts.

1. Identify specific areas to be cored using analytical imaging techniques such as EL and DLIT. Accurately locate defects on the backsheet. Use paper template to record defect locations.
2. Remove the TPT and EVA layers mechanically from the back of the panel using a rotary (Dremel) tool with accessories such as a grinding bit and buffing pad. There was no noticeable local heating of the panel during this procedure. After these layers are removed, the cell's back contact has been exposed.
3. Use a diamond-based coring bit and liquid-cooled drill to cut through the Si cell. This coring process includes cutting through the contacts and Si, and into the front EVA layer. The coring was done with running water to avoid heating the Si solar cell and to flush away particles during the cutting. The bits have diameters of about 12 to 25 mm.

4. Attach a metallic post to the cored area using cyanoacrylate adhesive, usually known as Super Glue. The post had the same diameter as the cored area. The type of adhesive used in this step is important, and we used one that is soluble in acetone.
5. After about two hours, which allowed the adhesive to cure and gain sufficient strength, the post is rotated very slowly around its axis with an open-end wrench until it shears from the panel. The weakest interface is typically between the Si and EVA, so the EVA stays on the panel, while the solar cell structure remains on the post.
6. Immerse the post overnight in acetone. During this time, the adhesive is completely dissolved in the acetone, and the Si solar cell can easily be separated from the post.

Examples of partial coring are shown in Figs. 7 and 8. The left images show a zoomed-in EL image of a defect area while still intact within the module. In Fig. 7, the area of interest is centered on a cluster of shunts within three columns between grid fingers, along with features of grain boundaries or other crystalline defects of this multicrystalline silicon cell. The right image of Fig. 7 shows a PL image of the cored piece after removal from the module and metal post removal. The outer edge shows cracking due to the mechanical-cutting damage. However, within the red outline, the defect features remain identical to those measured before the coring procedure. In Fig. 8, grain boundaries and dislocation networks are compared before and after coring. Only a few cracks propagating from the outer edge are seen as additional features due to coring. Measurements that were performed before and after coring show that the coring procedure did not introduce any significant defects in the original material.

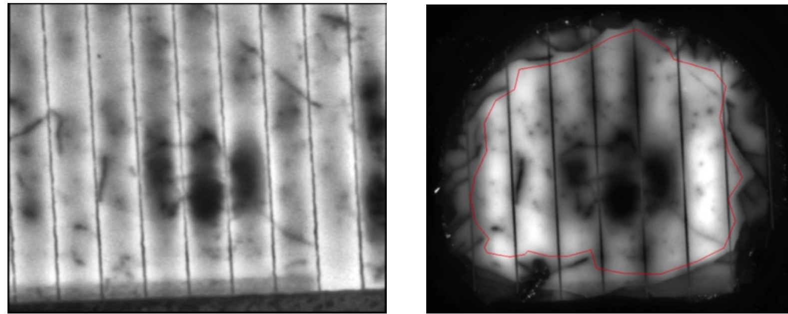

Figure 7. The left image shows zoomed-in EL of the defect area while the cell is still intact within the module. The right image shows PL imaging of this same area after the coring process. Grid fingers are spaced about 2.4 mm apart. Edge cracks appear due to shear stresses involved with removing the cell section from the module and breaking the cell/EVA interface. Inside the red outlined area, the defects appear unchanged.

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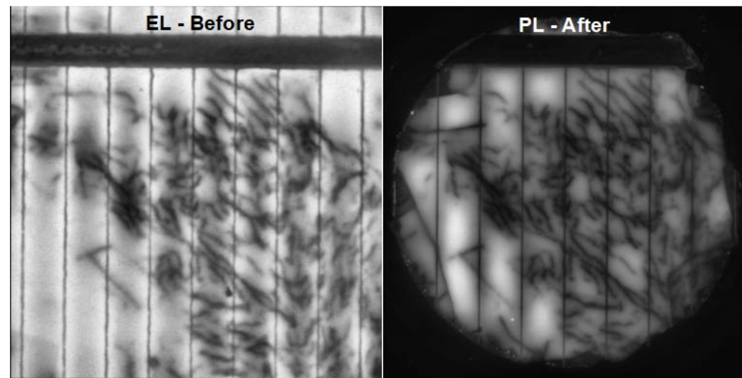

Figure 8. Comparison between EL and PL analyses performed on the same area of a Si solar cell before (EL) and after (PL) partial coring. The spacing between horizontal grid lines is about 2.4 mm.

The partial coring procedure has several advantages over full coring through the module. The process allows for the coring of samples with the desired intact size, preserves the solar panel's tempered glass, and avoids the use of TCE, which is toxic and carcinogenic. Because of its several advantages, partial coring has preferably been applied in the large majority of our studies.

Many CIGS and CdTe thin-film modules are processed on glass substrates (bottom) or superstrates (top). The processing steps and temperatures during module fabrication would typically not be compatible with tempered glass. For this reason, the glass used in thin-film modules can be cut through without shattering if the cut is made through the appropriate backside glass (for substrate configuration) or frontside glass (for superstrate configuration). For CIGS and CdTe modules, there is no need to mechanically remove TPT and EVA layers. For typical CIGS modules, the substrate glass can be cored from the back, and for typical CdTe modules, the superstrate glass can be cored from the front. The coring flowchart is slightly modified as shown in Fig. 9. On CIGS modules, due to the weak interface between Mo and CIGS, the best coring results were obtained using a solvent coolant solution, instead of water, and with the panel heated at temperatures as low as 60°C, to soften the EVA layer and prevent delamination at the Mo/CIGS interface. For CdTe modules subjected to PID, which results in the material becoming sensitive to humidity, the coring procedure was carried out inside a glovebox, and special sample holders and an environmental chamber were built to allow for the cored samples to be moved to and analyzed in microscopy systems. Currently, we routinely core different types of PV modules with a success rate of more than 90% for producing intact cores that are still electrically active.

Once cored samples have been successfully extracted from the module, imaging techniques can again provide spatial locations of defect regions. Using DLIT and a 3X zoom lens on the thermal camera, a defect can be resolved with an image having a field of view of just a few millimeters. A pulsed laser is used to mark the defect location for further study. As shown in Fig. 10, laser ablation marks identify a defect location, where the laser marks can be accurately generated in a range of ~0.5 to several mm apart and ideally define the defect location at the center point between the marks. The shunts detected by DLIT (dark spots show strong heating signal) correlate well to those identified in a scanning electron microscope (SEM) using electron-beam induced current (EBIC), where dark spots identify shunts with little to no current collection.

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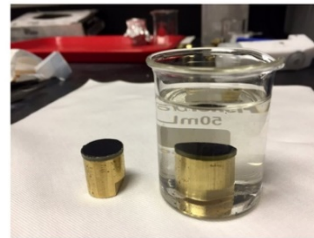

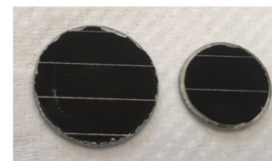

Figure 9. Coring procedure to extract defect-containing samples from a module.

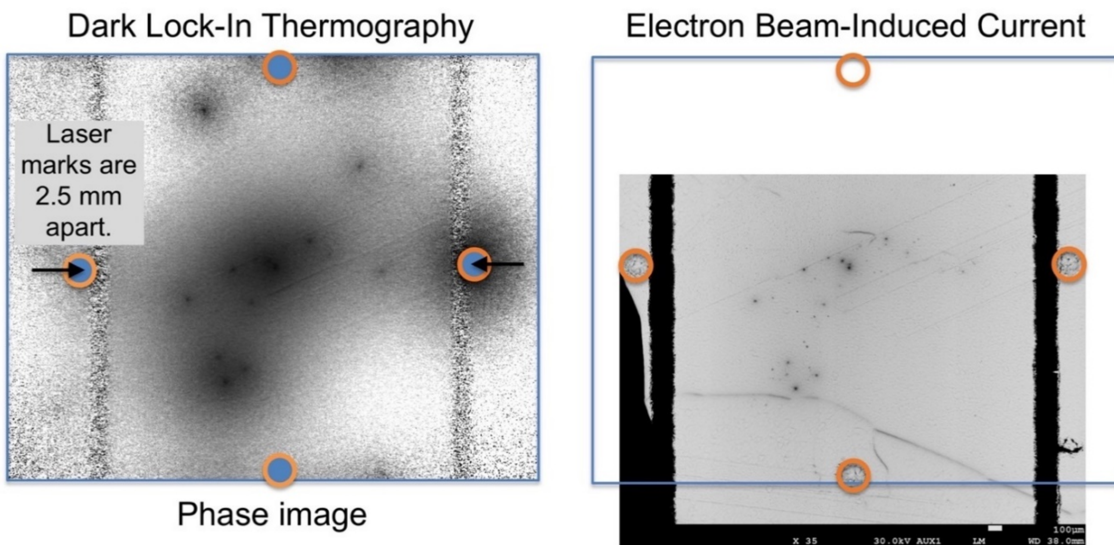

Figure 10. A zoomed-in thermal DLIT amplitude image shows a defect location. Horizontal and vertical laser ablation marks are 2.5 mm apart and ideally pinpoint the defect location at the center.

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4 Potential-Induced Degradation

Potential-induced degradation (PID) is a challenging reliability issue for crystalline-silicon (c-Si) solar cells. Shunting-type PID can cause significant power loss and even total module failure [13]. PID is believed to be caused by the diffusion of metal ions—largely, Na^+ from the front glass and encapsulation of the cell—that are driven into the silicon by the high voltage present in arrays of PV modules [14-24]. Currently, it is unclear whether the sodium diffuses along stacking faults that are already present in the material or if the sodium itself induces a stacking fault from a pre-existing defect at the surface of the silicon [17]. Although this area certainly warrants further investigation, a recent study has observed a direct correlation between PID susceptibility in cells and mini-modules and the initial defect density in both multicrystalline and single-crystal silicon [25]. Several studies have observed an increase of sodium in and around PID shunted areas [13, 16, 26]. We expand on prior work by continuing to develop methods that enable multi-scale, multi-technique characterization of PID shunting, thus enabling spatial characterization of the same PID shunted areas spanning 10 orders of magnitude [26, 27]. Atom probe tomography (APT) analysis of a PID shunt reveals a sodium content consistent with time-of-flight secondary-ion mass spectrometry (TOF-SIMS) data and transmission electron microscopy (TEM) results. We discuss the life cycle of sodium during PID stress and recovery as revealed through both bulk recovery and *in-situ* recovery of single shunts via annealing with an electron beam and subsequent TOF-SIMS analysis.

4.1 Microscopic PID Elemental Analysis

We investigated field-degraded c-Si modules in this work, in addition to laboratory-stressed mini-modules (details of the mini-module stressing were given in [26]). Further experimental details are given in our previous publications in this area [26, 28]. An image compilation is shown in Fig. 11, which illustrates the methods used in this study ranging from characterization at the entire module scale to chemical information at the nanoscale from a single PID shunt via TOF-SIMS. Figure 11A shows the DLIT imaging of an entire module (collected from the backside of the module; frontside EL and PL images were also collected at the module level, not shown). Figure 11B shows the DLIT image for a single cell from the module that has shunting present. Cored-sample-level DLIT was collected from the frontside of the device. Figure 11C shows the high-resolution DLIT image of this area, where individual shunts can now be seen.

Laser marks were subsequently placed around the defect of interest, providing a reference point for further characterization at the millimeter length-scale. The laser marks were used to find this same defect in the SEM. Figure 11D shows the shunt as identified with EBIC and four focused ion beam (FIB) marks that were then placed around the defect, providing a reference point at the micron length-scale for further characterization. The laser marks and FIB marks were used to find the same exact shunt in the TOF-SIMS. Figure 11E shows a 2-D TOF-SIMS image (200×200 µm) of the same area as shown in Fig. 11D. The gallium signal from the FIB marks is indicated in red, and the sodium signal is green.

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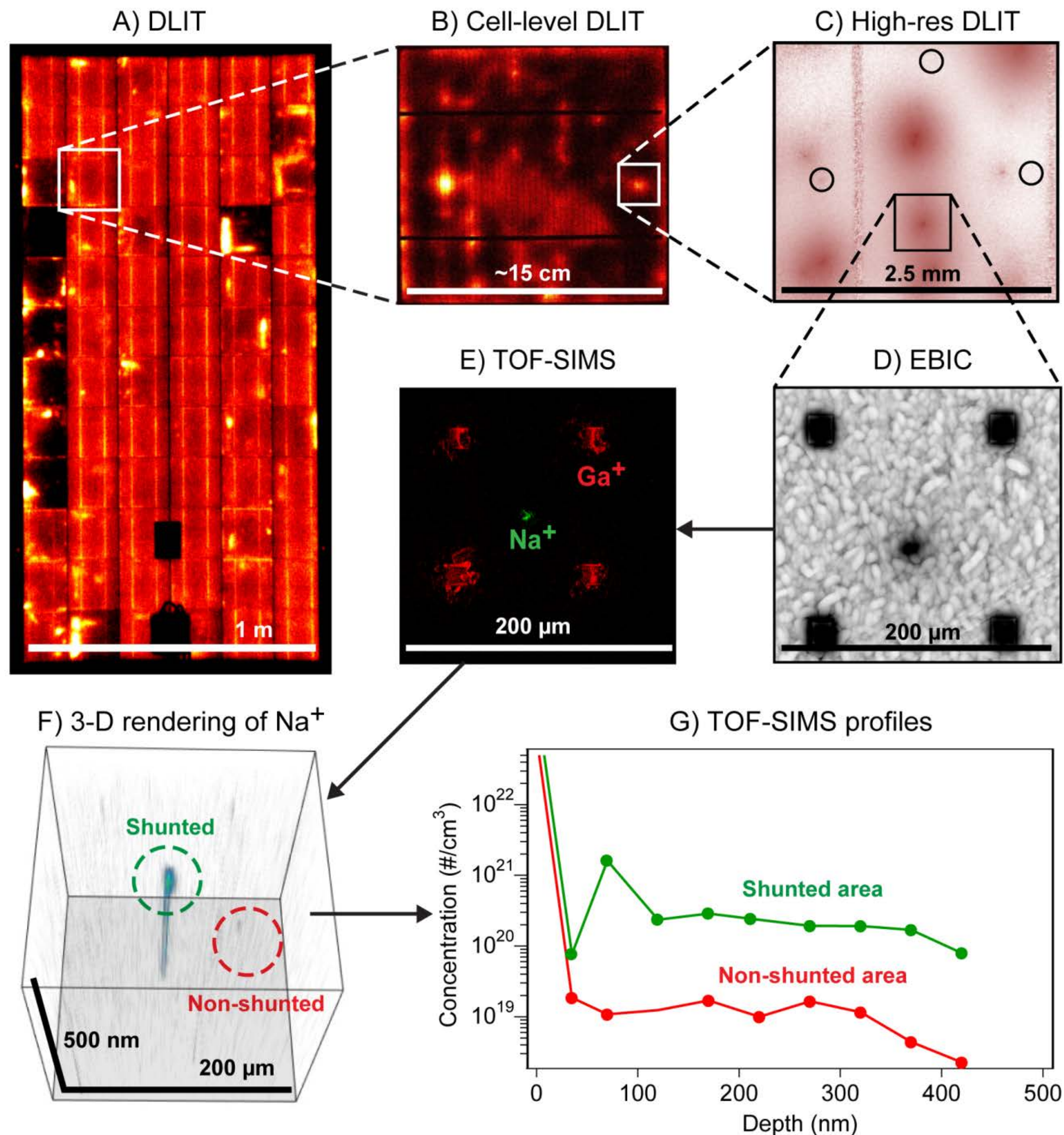

Figure 11. A) DLIT image of entire module (1–2 m). B) DLIT image of a single cell from the module. C) High-resolution DLIT of shunted area; black circles show location of laser marks around shunted area. D) FIB marks were put around single shunt identified with EBIC. E) TOF-SIMS image (200–200 µm), showing the Ga signal in red (corresponds to FIB marks), and sodium in green. The sodium spot matches the location of the shunt seen in EBIC. F) TOF-SIMS 3-D rendering of the shunt area. A single shunt is seen to persist through the depth of the measurement. G) Selected-area depth profiles from the shunted and an unshunted region, marked with circles in D. The sodium concentration peaks at ~1% at the SiN/Si interface in the shunted region, identified with the dashed line.

Importantly, the shunt identified with DLIT and EBIC correlates with high sodium content at the defect, consistent with a PID shunting-type defect [13]. We extend this analysis to three dimensions with TOF-SIMS tomography by combining imaging and sputter cycles. Figure 11F is a 3-D rendering of this same area (200×200×0.5 µm), showing the single shunt extending into the

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depth of the absorber. Two 1-D profiles are created from two different areas of interest from this 3-D dataset, identified with the dashed circles in Fig. 11F for the shunt and non-shunted regions (green for the shunted area and red for the non-shunted area). The 1-D profiles from these selected areas are shown in Fig. 11G. In this case, the defect that is causing local shunting and recombination is correlated with a sodium concentration on the order of 1% (1×10^{21} cm^{-3}) (green profile online), which is 1–2 orders of magnitude higher than the sodium content in the surrounding areas (red profile online). We have examined dozens of areas with similar shunts and consistently see similar trends as those observed in Fig. 11. The sodium content peaks at the Si/SiN interface, and the concentration in the shunted region is on the order of 0.1%–2% sodium (1×10^{20}–2×10^{21} cm^{-3}) [26, 27].

The procedure illustrated in Fig. 11 was also used to identify defects for FIB liftout of TEM lamella and atom-probe tip preparation. Consistent with prior observations [13, 26], the TEM results identified the defects as a subsurface, stacking-fault-like, planar defect [29]. The scanning TEM energy-dispersive X-ray spectroscopy (STEM-EDS) line profile for this defect is shown in reference [28], where a higher concentration of sodium is noted in the stacking fault. The sodium content of ~2 atomic % correlates well with the TOF-SIMS data. From the work of Alber et al. [30], the area density of Na atoms (cm^{-2}) at the planar defect can be estimated as $\Gamma_{Na} = N_{Si}(C_{Na}/C_{Si})w$, if one neglects beam broadening in the sample, where N_{Si} is the Si atom number density in the matrix material (5×10^{22} cm^{-3}), C_{Na} and C_{Si} are the weight percents of Na and Si, respectively, measured from a scan window of width w perpendicular to the planar defect. Using the Cliff-Lorimer k-factors supplied with the EDAX TEAM software used for the analysis, a linear background subtraction, and a scan window width of 100 nm perpendicular to the plane of the defect, an area density of $\cong 4\times10^{15}$ cm^{-2} was calculated for Na atoms for the planar defect. This is the same order of magnitude as the area density of Si atoms on a (111) plane that is calculated to be $\cong 0.8\times10^{15}$ cm^{-2}.

We performed atom probe tomography (APT) of the same PID shunt defect as that from which the STEM EDS line profiles of reference [28] were obtained, and the results are shown in Fig. 12. Figure 12 displays the 3-D reconstruction of the atom probe tip, showing the silicon (96% isoconcentration surface, gray) matrix and sodium (0.4% isoconcentration surface, green) in the stacking fault. Again, this sodium content is consistent with the TOF-SIMS results. Figure 12B also includes the oxygen (1.6% isosurface, blue) and gallium (5% isosurface, yellow) in the data reconstruction; the residual gallium is an artifact from the FIB sample preparation. The sodium content measured with the atom probe is consistent with both the STEM-EDS and TOF-SIMS results.

Interestingly, during high-resolution EBIC scanning of PID shunts, the shunt contrast decreased over time. To study this effect in detail, we conducted the experiment discussed in detail in reference [28]. First, DLIT imaging was used to find an area with several PID shunts. A low-current, low-magnification EBIC image was then taken on the same area, and a few individual shunts were subsequently subjected to e-beam annealing. As shown in reference [28], the EBIC contrast at the e-beam annealed shunts is significantly reduced after this e-beam annealing. Another iteration of DLIT imaging indicated that these shunts were no longer visible (via DLIT), confirming the recovery effects of the e-beam annealing. Finally, using the laser and FIB marking procedure outlined in Fig. 11, the same area was analyzed by TOF-SIMS. Figure 13 shows the EBIC image and TOF-SIMS 3-D rendering (300×300×0.3 μm) of the annealed shunts. The TOF-

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SIMS data in Fig. 13B show that the location of the FIB marks seen in EBIC (Fig. 13A) correspond to the gallium signal (red) in the TOF SIMS data. There are four identified shunts within the TOF-SIMS dataset—three of which were subjected to the e-beam annealing and one of which was not. For all the shunts subjected to the e-beam annealing, a large amount of sodium “pooled” around the shunt location at the surface of the sample. This sodium is no longer present after the first few sputter cycles of depth profiling. In contrast, the non-annealed shunt in Fig. 13A does not have a large amount of surface sodium present around the shunt location.

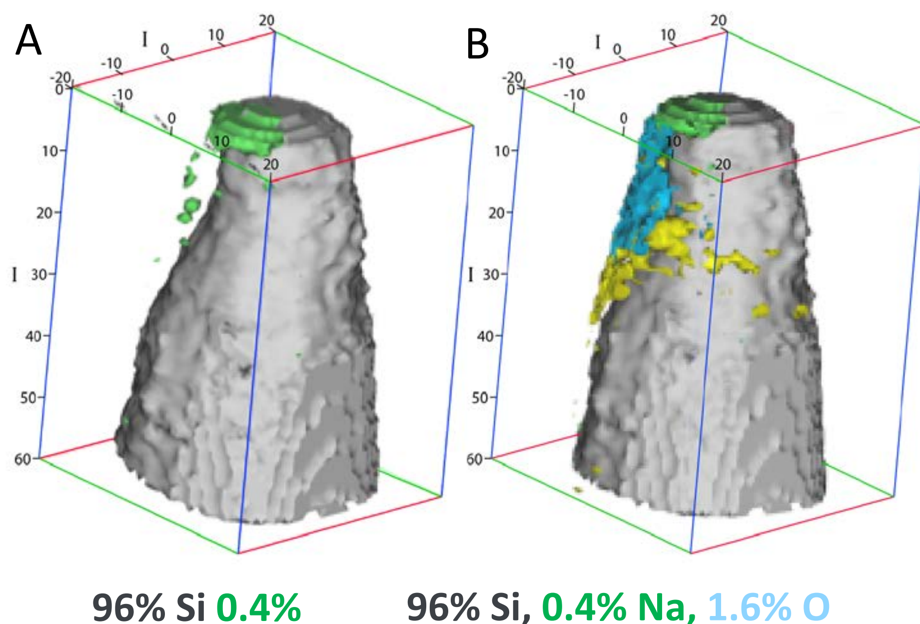

Figure 12. 3-D reconstruction of atom-probe analysis of a PID-related {111} planar defect identified with the TEM. A) Silicon (gray) and sodium (green) isosurface. B) The results reveal Na (green), O (blue), and Ga (yellow) (likely contamination from FIB sample preparation) present at the defect consistent with the STEM results.

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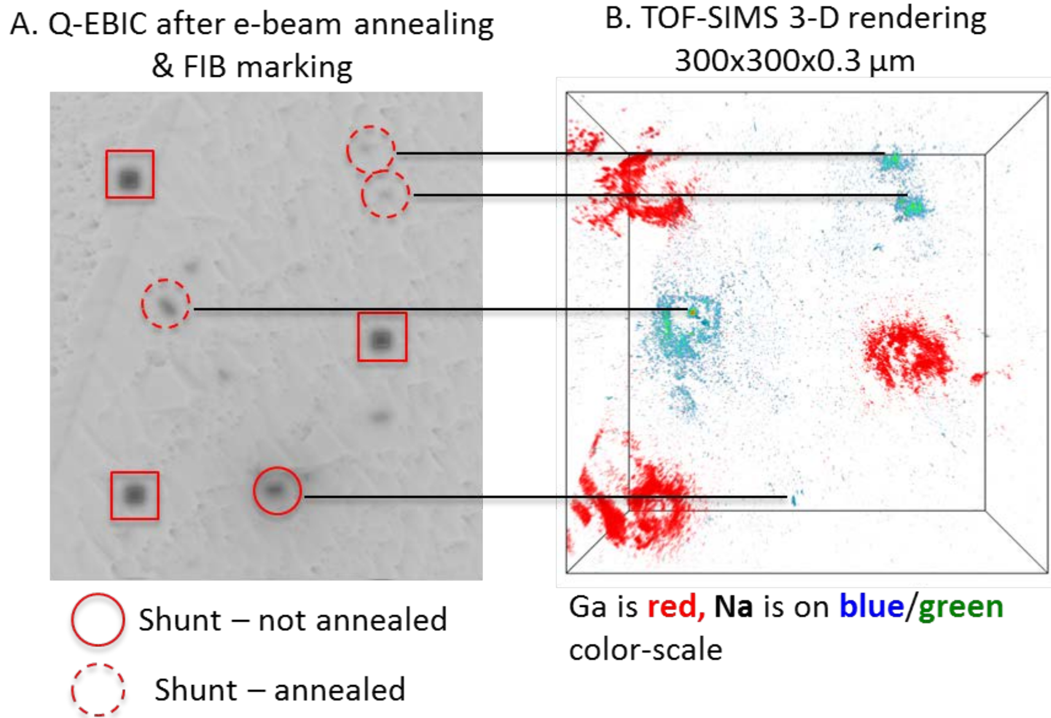

Figure 13. A) EBIC image shows shunts that were subjected to e-beam annealing (circled, dashed), and one that was not (circled), as well as three FIB marks (outlined with squares). B) TOF-SIMS 3-D rendering of same area, showing gallium near the FIB marks (red online); comparison to the one non-annealed shunt reveals significant sodium out-diffusion to the surface from the annealed shunts.

The recovery mechanism that we propose is that the e-beam annealing likely leads to localized heating of the PID shunts, and thermodynamic and diffusive driving forces lead to out-diffusion of the sodium from the region of high concentration (the PID shunt) to the surface (a region of low concentration). Surface diffusion then moves the sodium away from the shunt, but it still remains generally localized to the shunt because the energy for such migration being provided from the electron beam itself is localized to the shunt area. This proposed mechanism is supported by the selected area 1-D profile data shown in reference [28] comparing sodium content within a cylinder (~5-micron diameter) for both the non-annealed and annealed shunts. Except for the very surface of the sample, where the sodium content is much higher, the sodium content in the annealed shunt is 1–2 orders of magnitude lower compared to the non-annealed shunt. These results are consistent with a FIB-marked sample that was bulk-annealed for PID recovery on a hot-plate, where significant amounts of surface sodium were observed in the areas where shunts were noted [28].

Further experiments revealed that not all PID shunt defects recover on e-beam annealing. STEM analysis of one of these recovery-resistant defects by both EDS and electron energy-loss spectroscopy (EELS) revealed Na to still be present at the {111} planar defect that extended several microns below the SiN_x/Si interface. A STEM EELS elemental map showing Na segregated at the defect is shown in Fig. 14.

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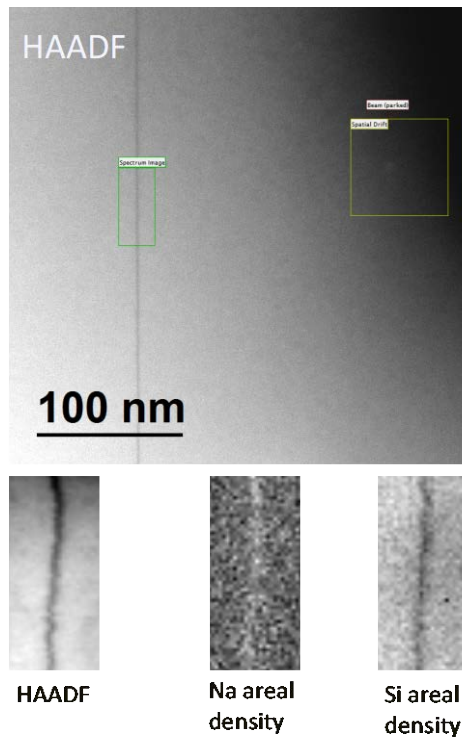

Figure 14. STEM high-angle annular dark-field (HAADF) images and EELS areal density maps showing Na present at a {111} planar defect associated with a PID shunt that was resistant to recovery by e-beam annealing in a SEM.

These results suggest a life cycle of sodium related to PID where sodium ions are driven toward the silicon by drift from the electric fields present during module operation. After diffusion into the silicon [31], sodium will migrate out of the structural defects to the surface during recovery or to the SiN/EVA interface, where it will accumulate. This is consistent with prior observations of PID recovery done on a TEM lamella [16]. Once the driving force for PID recovery is removed and the module is placed back in operation, the driving force for sodium migration that can cause PID shunting returns, and it can again lead to further sodium migration and degradation.

4.2 Theory and Modeling of PID-s in Si

The observations of near-surface stacking faults heavily contaminated with Na extending through the p-n junction combined with the I-V characteristics exhibiting shunting behavior all suggest that a metal-like precipitate forms that causes ohmic shunting. Given that these shunts do not extend through the entire device, it is not immediately clear how they exhibit ohmic behavior because a Schottky barrier would form at the metal/semiconductor interface. Furthermore, enhanced recombination or barrier-lowering effects would be manifested primarily as V_{oc} loss, which is not the case in PID-s. Since ohmic shunting through fully metallic pathways is not consistent with the observed device characteristics, our hypothesis is instead based on the idea of semi-shunts [32], which allow for thermionic field emission (TFE) at the edge of the metal protrusion due to the enhanced electric field there. Figure 15(A) shows numerical calculation of the electric potential near a 1-µm-deep metal plane through the Si p-n junction. A 10-fold electric-field enhancement at the tip relative to the typical built-in field is evident.

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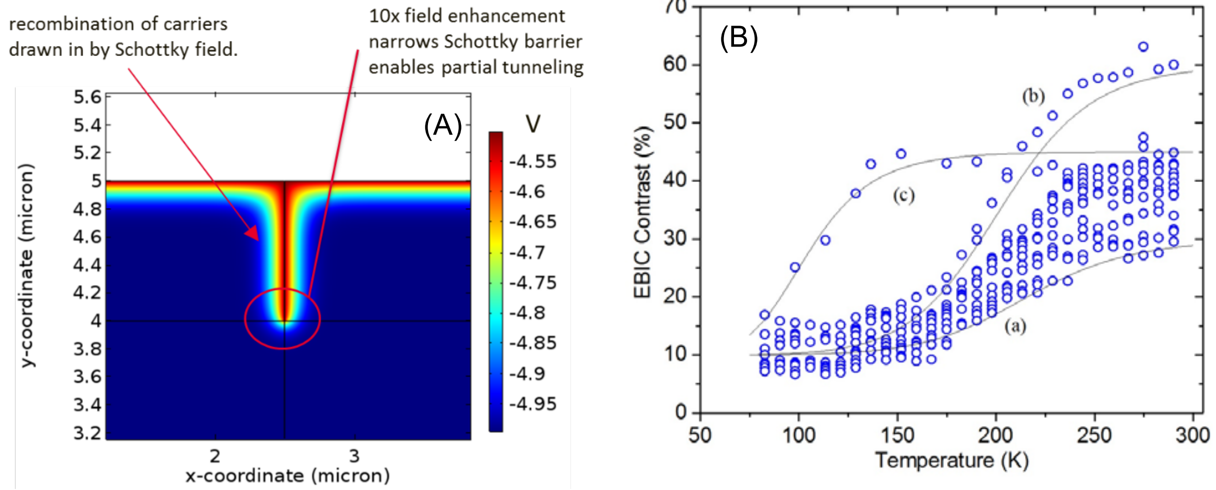

Figure 15. (A) Electric potential (in volts) due to the Schottky contact of a 2-nm-thick metal plane, 1 µm deep in silicon. The color gradient near the top surface is the typical p-n junction depletion region. Significant electric-field enhancement at the edge of the plane enables thermionic field emission of charge carriers and enhanced recombination. (B) EBIC contrast versus temperature data (circles) for thirteen defects identified as PID-induced shunts. Solid lines are model fits with (a) C_{max} = 0.30, ϕ_b = 0.40 eV; (b) C_{max} = 0.60, ϕ_b = 0.50 eV; and (c) C_{max} = 0.45, ϕ_b = 0.35 eV.

The semi-shunt hypothesis is tested against the EBIC vs temperature data shown in Fig. 15(B) for 13 different PID shunts. EBIC contrast is given by $C = 1 - I/I_0$, where I is the measured current and I_0 is the defect-free current. When TFE allows for current I_c to flow across the contact tip of resistance R_c, the defect-free (or total possible) current is $I_0 = I + I_c$. So, the total current is divided through the p-type base (I) of resistance R_p and through the semi-shunt resistance, R_c, resulting in $I/I_0 = 1 - R_p/(R_p + R_c)$. The latter expression implies the contrast, $C = R_p/(R_p + R_c)$. The specific contact resistance due to TFE is given by [33]:

$$R_c = R_{c0} \exp\left[\frac{q(\phi_b - \phi_p)}{E_0 \coth(E_0/kT)} + \frac{q\phi_p}{kT}\right] \tag{1}$$

with the pre-exponential,

$$R_{c0} = \frac{k\sqrt{E_0}\cosh(E_0/kT)\coth(E_0/kT)}{A^{*}Tq\sqrt{\pi q(\phi_b - \phi_p)}}, \tag{2}$$

where q is the elementary charge, k is Boltzmann's constant, T is temperature, ϕ_b is the Schottky barrier height to holes, ϕ_p is the difference between the valence band and Fermi level, and $A^{**} \approx$ 30 A/(cm^2 K^2) is the effective Richardson constant for holes in Si. The characteristic tunneling energy, E_0, depends on the local electric field (barrier width), which we calculate can be rather large at room temperature, $E_0 \approx kT$, in the region of field enhancement. Finally, it is reasonable to assume a minimum contrast, C_{min}, that is measured when TFE is not present and a maximum contrast C_{max} when TFE is most efficient, yet not all generated electron-hole pairs recombine. Overall, the contrast is given by:

$$C = C_{min} + \frac{1}{1 + R_c/R_p}(C_{max} - C_{min}). \tag{3}$$

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C_{min} is set to 10%, and C_{max} and ϕ_b are fitting parameters with the values given in the caption of Fig. 15. All other parameters are fixed, and the model provides good agreement with the data. We note that this EBIC temperature dependence is opposite to that observed at grain recombination sites [34].

As a rough estimate for cell-level effects, a barrier height ϕ_b = 0.45 eV and tunneling energy, E_0 = 0.02 eV, yields R_c = 0.03 Ω cm^2 at room temperature. At that point, the contact resistance is similar to or less than that of the p-type Si base, which defines the shunt as ohmic. Although it is a small area contact, it can collect current from a characteristic length close to the thickness of the p-type base, $L \sim 100 - 300$ μm. Therefore, a shunt resistance of 10 to 100 Ω may be expected in the vicinity of a shunt. Cell-scale simulation results in Fig. 16 show the effects of several 50-Ω shunts on the cell I-V curves. Reasonable agreement with data is obtained with this model [35].

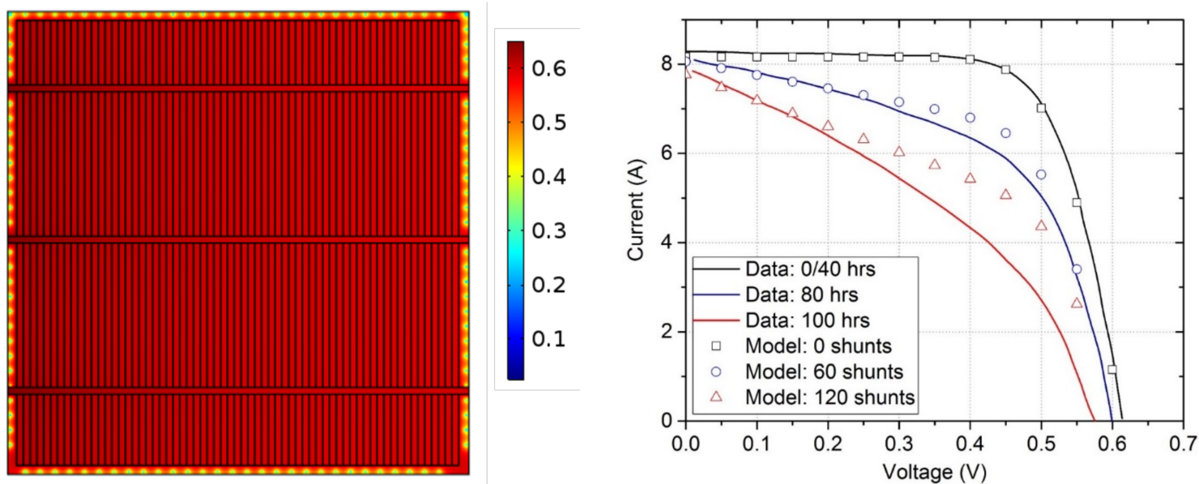

Figure 16. Left: Electric potential in a 15.6×15.6 cm Si cell with 120 50-Ω ohmic shunts placed around the periphery (based on imaging results in Ref. [35]. Conditions are 1-sun light intensity and V = V_{oc}. Right: I-V curves for measured (lines) and simulated (points) results. Data pertain to hours of PID stress, and the model pertains to the number of shunts.

4.3 Large-Area Material and Junction PID in Si

In addition to Na precipitation at stacking faults, we have detected another PID mechanism for c-Si in which substantial Na diffusion causes large-area material and junction degradation due to distributed point defects [36–38]. In this study, we have combined multiple characterization techniques—PL, Kelvin probe force microscopy (KPFM), EBIC, TEM, TOF-SIMS, and microwave photoconductance decay (μ-PCD)—as well as density functional theory calculations. These characterization techniques are complementary in various aspects of a material's chemical, structural, electrical, and optoelectrical nature, as well as in atomic, nanometer, micrometer, millimeter, and cell and module scales. All the results point consistently to a new mechanism: substantial large-area deterioration of materials and junctions that plays a major role in c-Si PID, in addition to the local shunting defect caused by Na diffusion to planar defects [21]. This finding reveals an additional PID component that is expected to lead to new strategies for tailoring c-Si photovoltaics to resolve PID.

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We investigate the electrical potential across the p-n junction on the cross section through the darkest PL area between the two silver grids over a total length of ~2 mm, as shown in Fig. 17. Three different kinds of areas—labeled as "No PID," "abnormal junction area," and "transition area"—were found by the KPFM imaging, where the electric-field peak is, respectively, at the normal junction location, at the cell front surface, and between them. Typical KPFM results across a normal junction ("No-PID region) are shown in Figs. 18(a)–18(e). The black, purple, and blue dashed lines were drawn following the Si/Ag-epoxy interface (Ag epoxy was for KPFM sample preparation), p-n junction location, and depletion edge of the p-type Si cell, respectively. We took the potential images with varying bias voltage (V_b) applied to the device (Fig. 18c) to derive the potential change in the bulk by measuring the surface potential changes (Fig. 18d) [39, 40]. The V_b-induced change in the electrical field was obtained by taking the first derivative of the potential difference (Fig. 18e). The peak of the electric field indicates the p-n junction location.

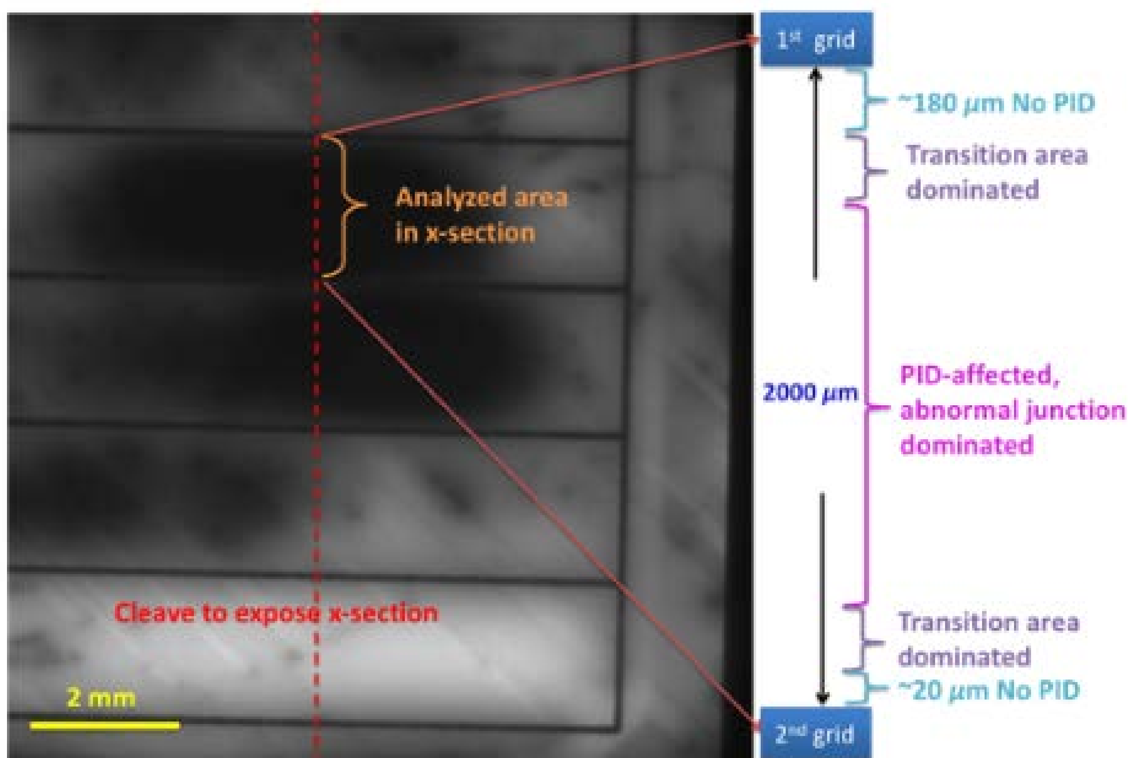

Figure 17. PL mapping of a PID-affected area. The sample was cleaved to expose the cross section, as indicated by the red dashed line. The KPFM analyzed region is between the two metal grids with most serious PID-affected area.

Figures 18(f)–18(h) show typical KPFM results in the PID-affected region. The appearance of the electric-field peak at the cell/epoxy interface instead of a normal junction location (~500 nm away from the Si surface) suggests a significantly damaged junction; external reverse-bias voltage applied to the cell does not drop at the junction. Instead, the V_b drop at the interface suggests a shunted junction because it implies that the equivalent resistance of the junction is much smaller than the contact resistance at the epoxy/cell interface. The equivalent resistance depends on the quality of the junction, e.g., the gap state density and recombination velocity. Therefore, the abnormal electric potential/field in PID-affected regions is likely caused by junction damage or shunting.

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Figures 18(i)–18(l) show potential images in the transition region. We observe two types of transitions. The first is shown in Figs. 18(i) and 18(j), where the transition occurs over ~1 μm, which is slightly larger than the depletion range generated by a V_b of -1.5 V. This type of transition region has a relatively abrupt transition between the normal and damaged junctions. The second type of transition region is shown in Figs. 18(k) and 18(l), where the electric-field peak is at a location significantly shallower than the normal junction depth. The green circle in Fig. 18(l) indicates such an area adjacent to two junction-damaged areas. This apparent movement of the electric-field peak may be caused by a moderately damaged junction, where the equivalent resistance is comparable to that at the epoxy/cell interface. In this case, the voltage would drop at both the junction and interface. If the KPFM measurements cannot resolve the two voltage drops, then the electric-field peak would appear at a location between the junction and interface. Therefore, this type of transition may indicate a moderately damaged junction.

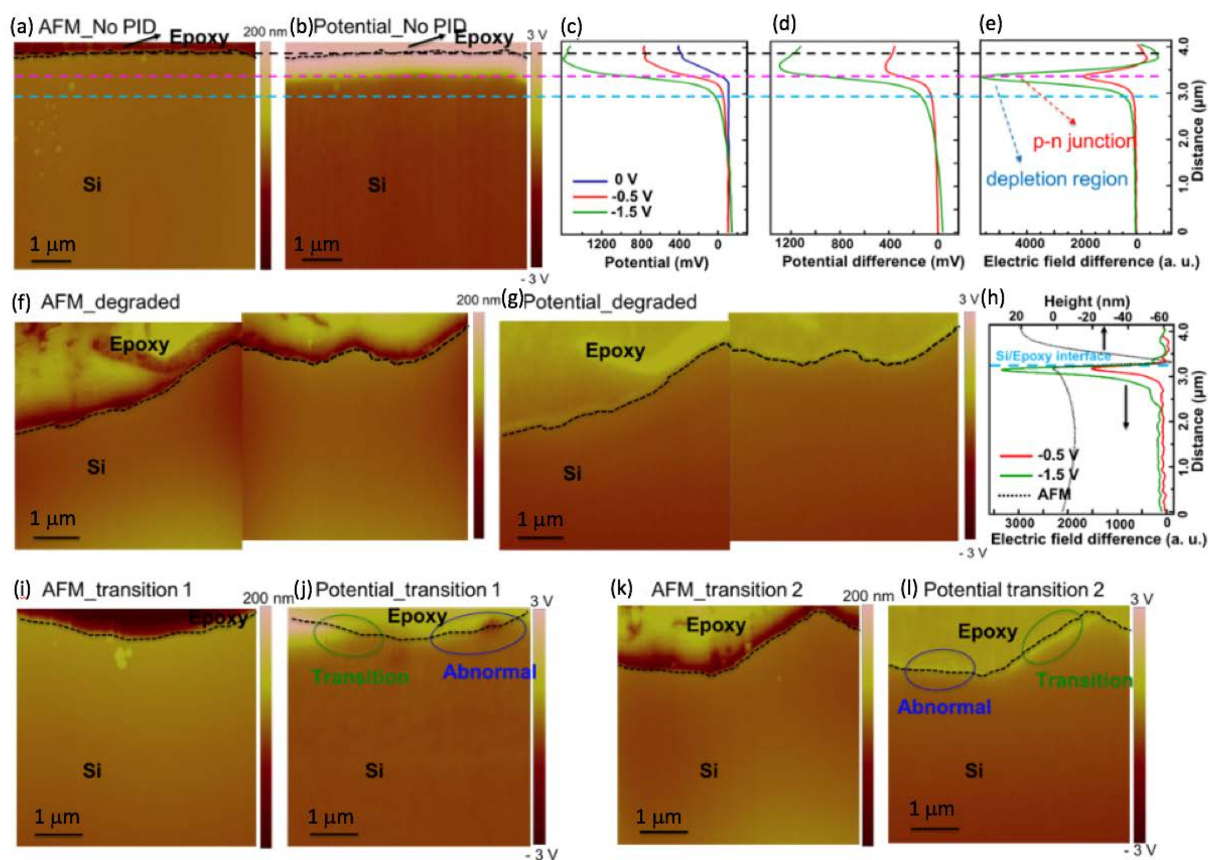

Figure 18. (a) An AFM of a non-degraded area with a normal p-n junction; (b) the KPFM image at -1.5 V corresponding to (a); (c) potential profiles of an area in (b); (d) potential difference curves; (e) electric-field difference curves showing a good p-n junction characteristic; (f) AFM of a PID-affected area; (g) the KPFM potential image at -1.5 V corresponding to (f); (h) electric-field difference curves showing an abnormal p-n junction characteristic; the electric field peak is at the epoxy/Si interface instead of junction; (i)–(l) AFM and the corresponding KPFM of two types of normal/abnormal junction transition area.

The rapid transitions between large areas of material with and without junction damage suggest semiconductor material and junction degradation rather than the well-reported local shunting induced by Na-decorated planar defects that penetrate the p-n junction [21]. One may argue that a point shunt could also lead to the apparent junction collapse. If local shunting was the reason for the observed large-area

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abnormal junction collapse, then the potential drop must gradually change from the shunt location to the good area over a much longer range of ~100 μm, because the ~100-Ω emitter sheet resistance would gradually increase resistance of the electrical current path through the local shunts and the emitter. However, the short transition distance suggests that the PID we observe is not caused by a local shunting and is instead associated with a different large-area PID mechanism that has not been previously observed.

To further confirm our results in Fig. 18 on field-degraded samples, we developed *in-situ* stressing capabilities on an AFM platform to investigate various solar cell degradation mechanisms [41]. By applying *in-situ* KPFM over the course of PID stressing on a different set of samples, we observe the evolution of electrical potential across the junction along with the stressing time. These results are consistent to what we observed in Fig. 18. In both cases, we attribute the large-area material degradation to point defects. Point defects formed by Na^+ in Si have been reported to induce six gap states [42]—two of which can be detrimental for photovoltaics, with one at 0.27 eV above the valence band maximum (VBM) (deep level) and the other being donor-like at 88 mV above the VBM. These two defects can, respectively, degrade the solar cell performance by different mechanisms of either Shockley-Read-Hall recombination or altering doping around the junction and in the Si bulk.

Multiple complementary characterization methods were also performed in conjunction with KPFM to confirm the large-area material and junction deteriorations associated with point defects. EBIC imaging across the junction showed sharp transitions between the functional/malfunctional junctions. TEM did not find an extended structural defect in the degraded area by randomly sampling. TOF-SIMS exhibits a higher Na concentration in the highly degraded area than the less-degraded area. Microwave-PCD illustrates a shorter lifetime of the degraded area by probing near-surface carriers in the μm range.

In conclusion, we investigated the root-cause mechanisms for PID shunting in field-degraded and laboratory-stressed multicrystalline silicon modules using a multi-scale, multi-technique characterization approach. A combination of techniques and marking—high-resolution DLIT, laser marking, EBIC, and FIB marking—allowed chemical analysis at the micron- and nanoscale by TOF-SIMS, TEM, and APT. We found that the shunted areas correspond to structural defects in the silicon, and that these semi-shunts could be modeled based on an enhanced electric field due to the sharp physical features. The sodium content in the defects' peaks at the SiN/Si interface has been consistently observed at a concentration of 0.1%–2%. We also report on PID recovery done *in-situ* in an SEM by use of an electron beam. The recovery is a result of sodium out-diffusion from the shunt to the surface of the silicon nitride, and we project that these results would also apply to large-scale module recovery. The enhanced sodium content at the SiN/EVA interface upon recovery will reduce adhesion, which can lead to delamination. These Na-compound deposits may also be responsible for the observed reduction in PID sensitivity after PID recovery in c-Si PV modules by further blocking ingress of Na into the silicon. Finally, we found that PID occurs not only at Na-decorated planar defects (local shunting) but can also occur in larger areas and can cause material and junction degradation. Substantial large-area deterioration of materials and junctions could also play a role in c-Si PID. Our studies have revealed PID features and components that could lead to new strategies for tailoring c-Si photovoltaics to ultimately resolve PID issues.

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5 Thin-Film Metastability

5.1 CdTe Module Degradation Imaging

To monitor degradation of thin-film CdTe modules, we collected PL, EL, and DLIT during stressing of a CdTe module under 1-sun light at an elevated temperature of 100°C. We obtained, through an industrial source, a CdTe mini-module for testing and characterization that had not undergone any stress prior to our tests. The mini-module was produced using a commercial process that is scalable to production quantities. It has a standard polycrystalline film stack, and after fabrication, it has more Cu near the back surface.

The CdTe module is initially characterized by imaging before stresses are applied. Figures 19(a)–(c) show PL, EL, and DLIT images for the initial state of the module. The PL image of Fig. 19(a) shows that the module is mostly uniform, with only a few spatially localized defects or anomalies. The EL image, Fig. 19(b), shows that the upper three-quarters of the module are slightly darker. The darker EL regions correlate with shunting defects in the DLIT image (Fig. 19(c)). These results indicate that a large number of fabrication-related shunting defects are present in the central/upper half of the module even before stressing. In the DLIT images, elevated temperatures are represented by orange and yellow colors, while blue colors represent the lowest temperatures, and red shades are temperatures in between. Because the EL is collected with only about one-third of the J_{SC} expected at 1-sun, the shunts within each cell can reduce the EL emission by dropping the voltage across that cell. The currents applied during the imaging were intentionally kept low to reduce the risk of generating new defects or accelerating defect degradation during the study.

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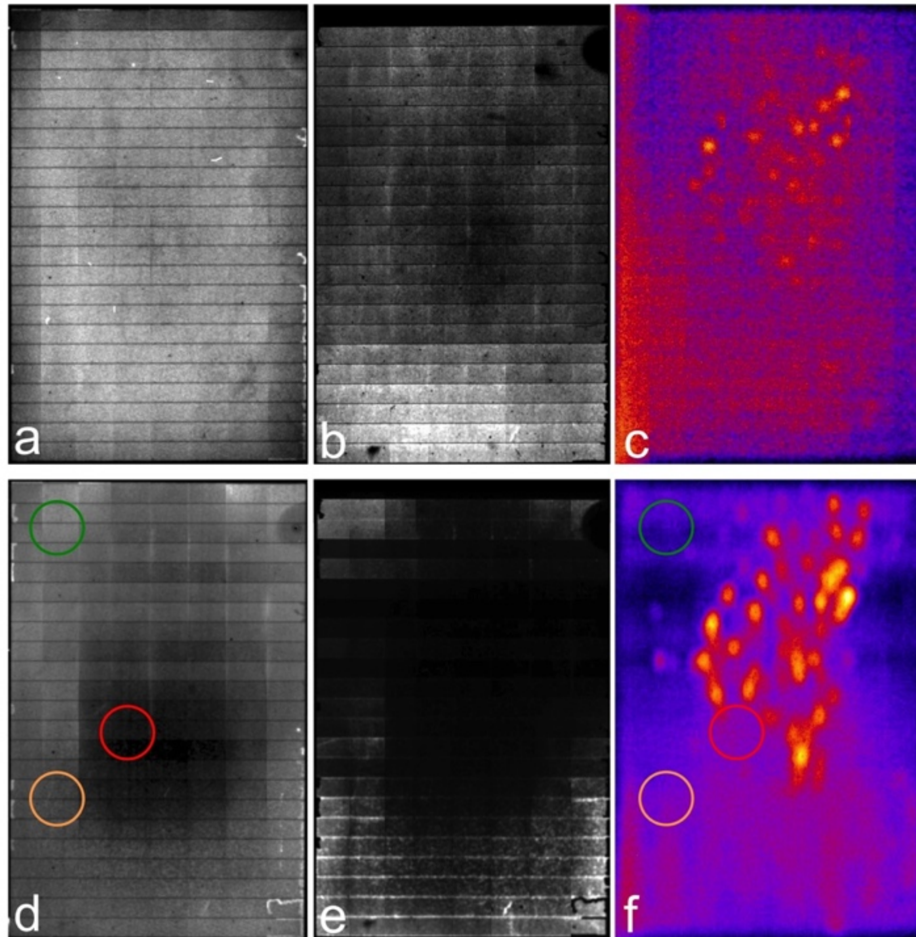

Figure 19. Pre-stress images of the CdTe module show (a) PL, (b) EL, and (c) forward-bias DLIT. Post-stress images of the CdTe module show (d) PL, (e) EL, and (f) DLIT. Circles (green for least degraded and red for most degraded) mark regions of interest away from shunts, where PL imaging shows various degrees of degradation.

The module was stressed by subjecting it to 1-sun light exposure at an elevated temperature of 100°C. A hotplate only slightly larger than the module was used for heating. Consequently, the edges of the module were about 15% cooler relative to the center, which was maintained at 100°C. Dark and light I-V curves were measured periodically, and the V_{OC} consistently drops over the time of stressing. The fill factor and efficiency initially show slight improvement before later decreasing. The J_{SC} remains fairly constant throughout the stress time.

The module was also periodically imaged during the stressing time. EL images began to show more contrast, with the upper-right two-thirds of the cell appearing dark after just 5 hours of stress. The PL images began to show a darker region in the center, likely due to the nonuniform heating during stress, after about 60 hours of stress. The final images after 400 hours of stress are shown in Figs. 19(d)–(f). The EL image, Fig. 19(e), again shows more contrast with dark regions due to both shunting in the upper half and degradation in the center region, which also appears dark in the PL image, Fig. 19(d). The DLIT image, Fig. 19(f), shows that the shunts have become more pronounced during stress. Based on the images, regions of least, middle, and most degradation are chosen for coring and further investigation. We chose regions where pre-stress shunting and initial

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defects are not apparent in the DLIT image. These areas are represented by green, orange, and red circles, where the green-circled area is the least degraded and the red-circled area is the most degraded.

To apply advanced microscopy to further study the degradation, samples were extracted from the module using a drill bit with a 25-mm (1-inch) diameter. For CdTe modules, the drill cuts through the front glass because the CdTe is grown in a front glass/TCO/window/CdTe/contact superstrate configuration. Once the cut is through the front glass, encapsulant layers, and device layers, then a cylindrical post with machined flat edges is glued to the glass. An open-end wrench applies torque to slowly sheer the cut specimen from the back glass. These extracted cores can now be imaged again to ensure that the device is still intact. PL images of the cored specimens are shown in Fig. 20. Although there appears to be some artifacts of coring damage in the form of circular lines where fractures have occurred within the semiconductor device, much of the area is intact and still shows similar ratios of PL intensity. Using the same excitation-light parameters and camera settings, the PL intensity of the middle-degraded sample is ~80% of the PL intensity of the least-degraded sample, and the PL intensity of the most-degraded sample is ~40% of the least-degraded sample.

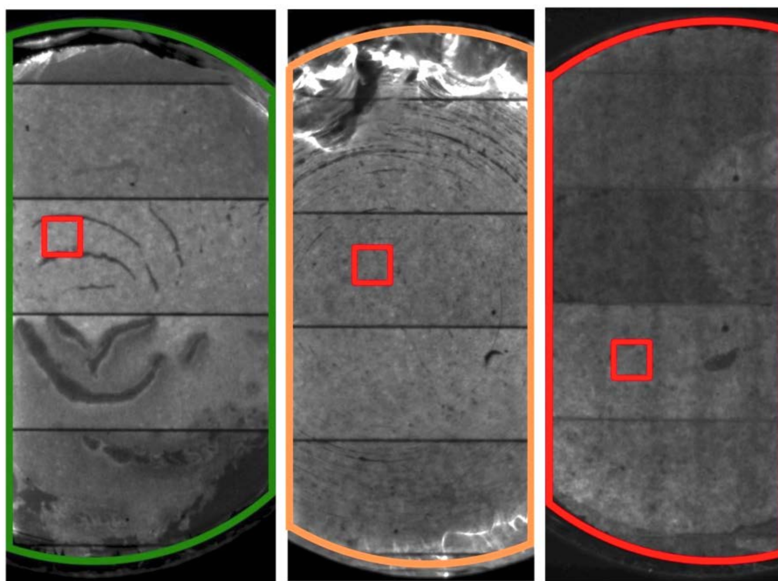

Figure 20. Post-stress PL images of cored sections that were cut out of the CdTe module where various degrees of degradation exist. Each image is individually adjusted for contrast and brightness. The left image outlined in green represents a cored section from the least-degraded area of Fig. 19. The center image is outlined in orange for the middle-degradation region, and the right image outlined in red is from the most-degraded region. The small red boxes show regions away from coring damage where microscopy analysis is performed.

5.2 Cu Redistribution in Degraded CdTe Modules

TOF-SIMS is performed to profile elements in the CdTe device at the cored regions with various degrees of degradation shown in Fig. 20. In Fig. 20, a small red box identifies an area that is ideally representative of that cored region and is located away from coring damage. The back contact of the device is the top surface during the measurement. As shown in Fig. 21, Cu is present in the

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back contact where the sputtering depth is near zero. However, Cu is also detected at the device's front interface after sputtering through the CdTe absorber layer, which is about 2,000 nm thick. The peak of the Cu signal matches the peak in S during the depth profile, which indicates that Cu is mostly accumulating in the CdS layer near the front of the cell during degradation. The Cu peak locations also match the transition as the Te signal decreases to lower values, further indicating that Cu accumulates in the CdS layer and not the CdTe absorber. We note that surface roughness and instrument sensitivity may limit the detection of lower concentrations of Cu in the interface region of the CdTe layer. We further describe the implications of Cu at the CdTe interface region in Section 5.3.

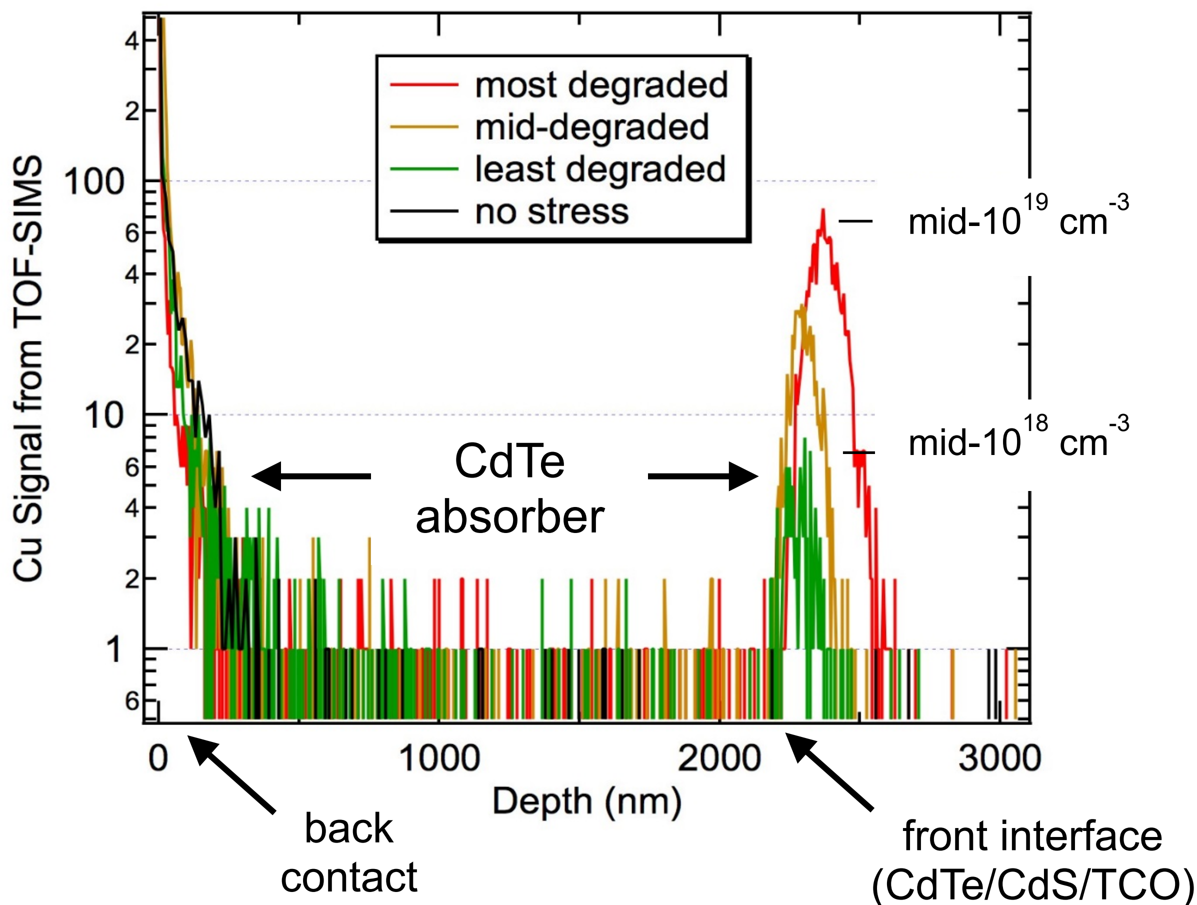

Figure 21. TOF-SIMS shows depth profiles of Cu on selected regions of the cored CdTe samples. The back contact corresponds to zero depth, and the thickness of the CdTe absorber layer is about 2,000 nm. There is no Cu at the interface of the sample without stress.

At the front interface where the TOF-SIMS Cu signals have a peak, the most-degraded region peak corresponds to a Cu concentration of mid-10^{19} cm^{-3}. The least-degraded region has about an order-of-magnitude less Cu accumulated at the front interface. An unstressed CdTe sample is similarly measured and shows similar Cu content in the back contact, but no Cu is detected at the front interface. Our observation of Cu accumulation toward the front interface of the device during degradation is consistent with pervious studies, and the evidence of Cu diffusion corresponds to poorer material quality and device performance [43–47].

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5.3 CdTe Electrical Potential Mapping

Using KPFM potential imaging across CdTe devices we show a change in depletion width for the degraded CdTe devices with Cu accumulation at the CdS/CdTe interface[48]. The least-degraded piece and most-degraded piece cored from the module were both cleaved and polished by ion milling. Then, the sample was annealed at 250ºC for 5 minutes in a vacuum oven to passivate the cross-sectional surface. Figure 22(a) shows the KPFM potential image with a reverse-bias voltage of V_b = -1.5 V applied to the device, and Fig. 22(b) shows the simultaneously taken AFM image. Because different material layers of the device can be identified from the AFM image (Fig. 22b), we are able to correlate electrical features such as the electric-field peak (Fig. 22(c)) with the device structure.

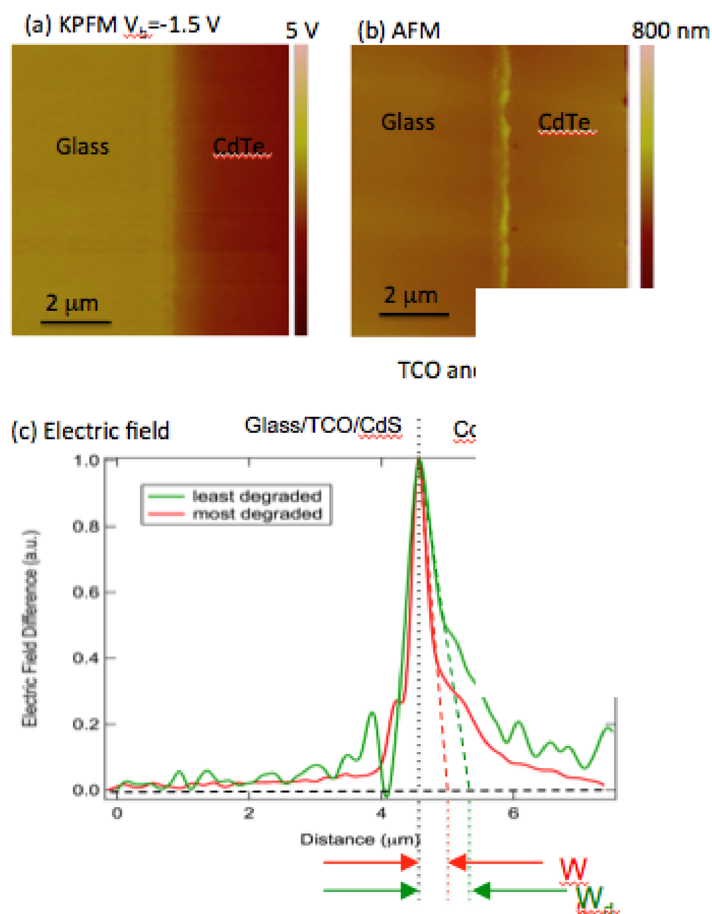

Figure 22. (a) A KPFM potential image taken with V_b = -1.5 V and (b) the corresponding AFM image. (c) shows profiles of the electric field on the most (red) and least (green) degraded samples, deduced from the potential imaging. Dashed lines show extrapolation of the electric field, assuming a constant carrier concentration. Depletion width obtained from the extrapolation are indicated.

By imaging the potential under various V_b voltages, the potential changes were used to deduce the change in electric field. Figure 22(c) shows the electric-field profiles on the most (red) and least (green) degraded pieces. The electric-field peak positions are the same and are all at the CdS/CdTe heterojunction interface, illustrating that the degradation does not change the junction location.

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However, the depletion width significantly decreases with degradation. Because the carrier distributions are not uniform across the device, the electric field in the depletion region is not linear and shows complicated profiles. In the first-order approximation of a constant carrier concentration, the depletion width is estimated by linearly extrapolating the electric field (dashed lines in Fig. 22c), giving values of ~790 nm and ~470 nm for the lease degraded and most degraded samples, respectively. The decrease in depletion width with the degradation is consistent with Cu diffusion from the back contact toward the front junction. Cu is a fast diffuser in CdTe due to the small diffusion energy barrier [49]. $Cu_{Cd}^{(-)}$ is believed to be the main acceptor defect in CdTe, with a shallow level of ~0.2 eV from the valence-band maximum and a small formation energy of ~0.5 eV in Te-rich condition [50]. Because Cu in CdTe can also create deep levels by forming interstitial Cu_i^+ defects [50], degradation can induce both an increase in carrier concentration (shallow levels) and an increase in nonradiative recombination (deep levels).

5.4 Theory and Modeling of CdTe Module Degradation

We hypothesize that the performance loss associated with Cu diffusion in degraded CdTe devices occurs through a defect reaction driven by light or forward bias (charge injection). In this process, Cu (or related defect complex) would serve as a reactant and the products would include both deep recombination centers and shallow acceptors [51]. This theory predicts narrowing of the depletion width and increase in the built-in electric field as degradation increases, which our KPFM and SIMS data support [52].

Our 2-D device simulation consisted of a layered structure with back contact/CdTe (2,300 nm) / $CdTe_{1-x}S_x$ (100 nm) / CdS (25 nm) / SnO_2:Al (300 nm). The interdiffused $CdTe_{1-x}S_x$ layer can form during common CdTe cell fabrication processes [53]. A 10-nm-wide grain boundary was included from the back contact through the center of the CdTe to the CdS layer. COMSOL Multiphysics® was used to solve the semiconductor equations (to calculate device performance metrics), equation for charge-induced degradation [51], and ion-transport equation (see Eq. (4)). A detailed list of the parameters and their values are provided in Refs. [54, 55].

The mechanism of charge-induced defect formation was shown to provide good correspondence to light-soak/heat-stress degradation in CdTe cells [51]. Quantitative evaluation of that hypothesis predicted that both mid-gap recombination centers and shallow acceptor levels are created over time with exposure to light (or forward bias) and heat resulting in V_{oc} and FF loss while maintaining a relatively constant J_{sc}, just as our data in Fig. 23 indicate. Hence, both recombination near the junction and the built-in electric field increase (i.e., depletion-width narrowing) with time under stress. A comparison of our calculations of the depletion width as a function of stress time with our KPFM measurements is also shown in Fig. 23. There is reasonable agreement between the data and model.

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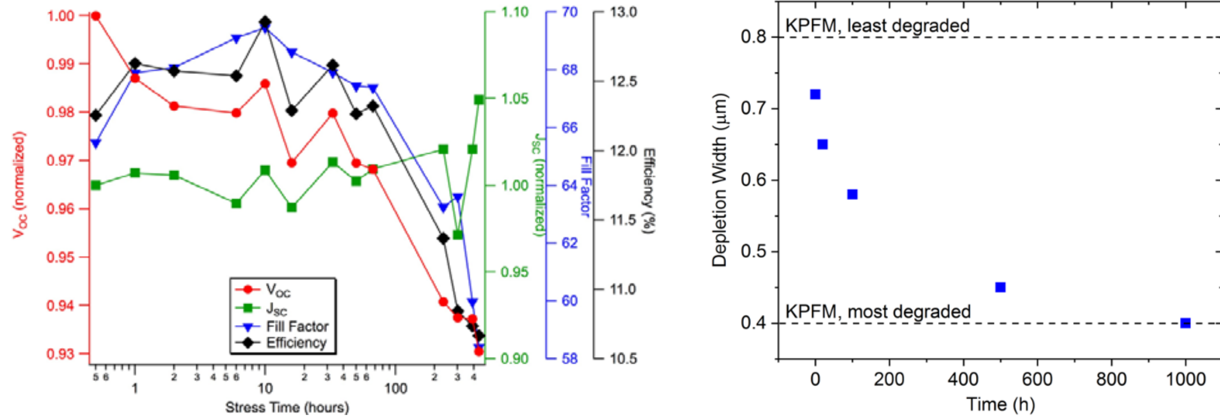

Figure 23. Left: Module parameters V_{OC}, J_{SC}, fill factor, and efficiency as functions of time that the module is stressed under 1-sun light, V_{oc}, and 100°C. Right: Simulated depletion width (points) as a function of time under light/heat stress. Dashed lines indicate KPFM measurements for the least- and most-degraded conditions.

We further correlate the modelled change in depletion width to the time-dependent evolution of Cu distribution in these devices by comparing numerical calculations with our TOF-SIMS data. We calculated the Cu distribution in the device as a function of time, $c(\boldsymbol{x}, t)$, by solving the ion-transport equation,

$$\frac{\partial c}{\partial t} = \boldsymbol{\nabla} \cdot (D\boldsymbol{\nabla}c) - \boldsymbol{\nabla} \cdot (c\mu\boldsymbol{E}) + R, \quad (4)$$

where $\boldsymbol{E}$ is the electric-field vector and D is the diffusivity that we distinguish as bulk, D_b, or along interfaces, D_i, such as grain boundaries. The diffusivity is related to the mobility, μ, by the Einstein relation, $D = \mu kT/q$, where k is Boltzmann's constant, T is temperature, and q is the elementary charge. Ion mobility through solids is thermally activated, and for Cu in CdTe we use diffusivity values of $D_b = 3.7 \times 10^{-4}\exp(-0.67[\text{eV}]/kT)$ cm^2/s [56] and $D_i = 7.3 \times 10^{-7}\exp(-0.33[\text{eV}]/kT)$ [57]. For comparison to SIMS data, we are concerned with total Cu concentration rather than its species or position in the lattice. Hence, we set the reaction rate $R = 0$ in Eq. (4) and assumed that Cu moves primarily as a positive ion through interstitial lattice and interface sites Cu_i^+. We note that typical CdTe cell fabrication includes an annealing step with a high Cu concentration at the back contact. Because our model started with a completed cell, the initial condition was set to $c(x, y, t = 0) = 10^{17}$ cm^{-3}, except for the back-contact boundary where $c(x_0, y_0, t = 0) = 5\times10^{22}$ cm^{-3}, in accordance with our SIMS data for unstressed cells. Simulations were run under the conditions of 1-sun light, V_{oc}, and $T = 373$ K (i.e., same as stress conditions).

A critical factor in Eq. (4) is the field, $\boldsymbol{E}$, which is obtained by solving the Poisson equation (as one of the semiconductor equations). Although we would expect the built-in field to be minimal at V_{oc} conditions (stress was applied at open circuit), the accumulation of shallow acceptors near the junction results in a remnant, localized electric field there, even at V_{oc}. As the acceptor concentration, N_a, increases, the depletion width decreases and the electric field increases. Three scenarios are reported here corresponding to band bending at the p-n junction with maximum electric fields of 7, 18, and 50 kV/cm at V_{oc}. Simulated concentration profiles within the bulk at time $t = 1$ hour are shown in Fig. 24. The results are shown at 1 hour because that is the approximate time at which equilibrium in the Cu distribution was achieved, as described below. There is agreement with the SIMS data in Fig. 21, which exhibited an increasing Cu hump with stress time and peak concentrations in the 10^{19}–10^{20} cm^{-3} range.

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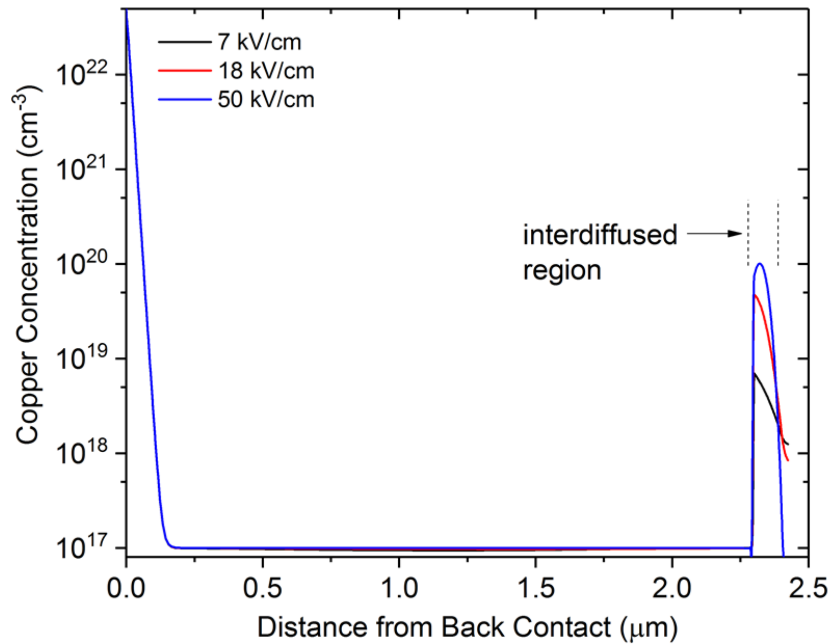

Figure 24. Simulated copper concentrations in the bulk and CdTe/CdS interface region for various electric fields near the interface. Increasing shallow-acceptor concentrations with stress time correspond to a larger electric field, narrower depletion width, and greater copper accumulation. Calculations are shown for T = 100ºC at t = 1 h.

The time-dependent simulations show that the Cu peak magnitude increases with degradation due to the increasing electric field near the absorber/buffer interface. At 100ºC, the time required for fast diffusion along the grain boundary and hump formation is $t_{diff} = L^2/D_i \approx 1$ hour, where $L \approx 2$ μm is the CdTe thickness and D_i is the interface diffusivity [cf. Eq. (4)]. Subsequent slower diffusion into the bulk will occur on a time scale that is about 4 to 6 orders of magnitude longer. These results suggest that the degradation rate (observed over tens to hundreds of hours) is controlled by the kinetics of a defect reaction involving Cu rather than the rate of Cu transport.

In conclusion, PL imaging is less sensitive to shunting and high series resistance than EL imaging, and its intensity often directly correlates to minority-carrier lifetime, diffusion length, and V_{OC} of the device. Here, PL imaging was used to characterize module degradation and identify regions that had degraded differently within the module. PL, EL, and DLIT signals in the initial module often predicted regions of enhanced degradation during stress due to shunts and other irregularities. In regions where shunts and defects were not apparent, TOF-SIMS indicated that the Cu concentration at the front interface correlated to the amount of degradation observed by PL imaging. KPFM revealed that doping at the junction increased during degradation by measure of the reduced depletion width. Numerical device simulation and ion-transport modeling indicate that the observed loss in performance, decrease in depletion width, and copper accumulation can be described by a charge-induced degradation mechanism that creates both shallow acceptors and mid-gap recombination centers in response to light/heat.

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6 Partial-Shading Reverse-Bias Breakdown

6.1 Module Damage Evaluation

Partial shading can induce a reverse bias in shaded cells of modules with series-connected cells. When breakdown occurs in localized defects, significant heating due to high current density and power dissipation can permanently damage the device [58,59]. The resulting power losses and reduced performance are important long-term degradation concerns for thin-film modules [60]. The EL images of Fig. 25 show examples of localized shunts in outdoor-fielded CIGS ($CuIn_xGa_{(1-x)}Se_2$) modules. Dark spots are shunted regions where carriers recombine through non-radiative paths. Brighter regions are typically found adjacent to the dark spots due to higher currents crowding to the shunt locations.

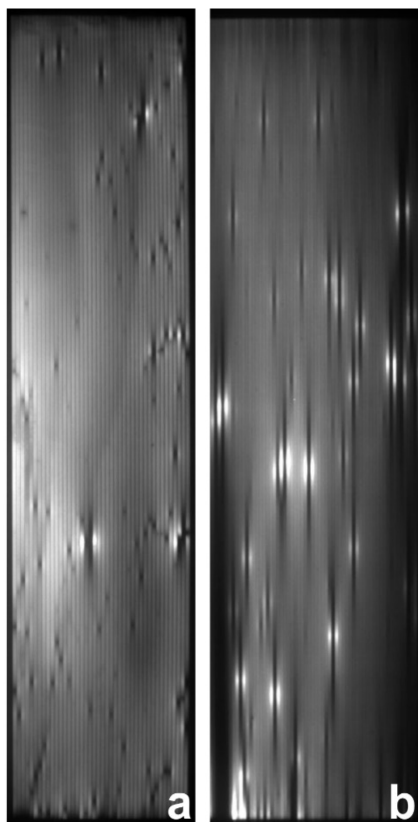

Figure 25. EL images of modules that have aged and degraded for years in the field. Dark areas show shunt-like defects that result in voltage drops and extension of low EL intensity along the cell near the shunt. Bright areas result from higher current density as carriers crowd toward the shunt defects.

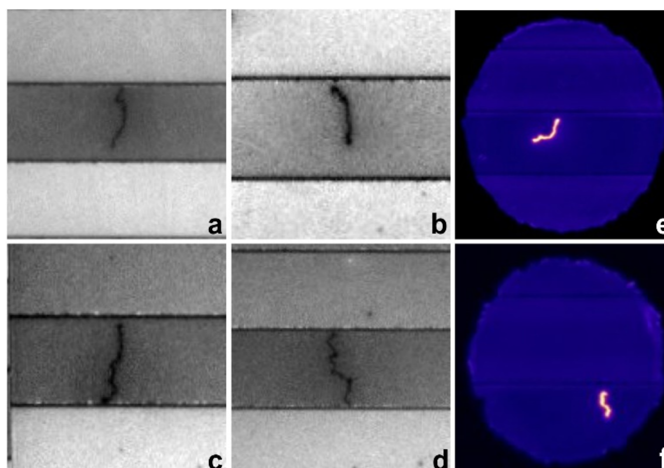

Figure 26. PL imaging (a)–(d) of shunt defects in the modules from Fig. 25 show long, narrow defect features where material has become damaged and is leading to higher carrier recombination. The decrease in voltage due to the shunts also causes the cell near the defect to emit a lower PL intensity. ILIT imaging (e)–(f) of the defect regions shows that carrier recombination through the shunts results in increased heating.

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In Fig. 26, we show higher resolution PL and ILIT images of the reverse-bias breakdown sites. Reverse-bias breakdown in CIGS modules causes damage in the form of "wormlike defects" [4] that appear to initiate at the scribe lines [61, 62] or within the main fields of the cells [63]. Cells that contain defects often have darker PL intensity due to the lower shunt-limited voltage. Thermal imaging using ILIT (Figs. 26(e)–(f)) show that the wormlike defects are bright, indicating heating as current flows through these shunt defects when voltage is induced by light pulses during the measurement.

We further characterize the wormlike defects by EBIC using an SEM. The EBIC image of Fig. 27(a) shows a bright background field where current is collected due to carrier excitation from the electron beam. The wormlike defect structures appear dark due to their lack of current collection. A cross section is prepared at one of the propagation fronts of the wormlike defects using a FIB. As shown in Fig. 27(b), the FIB cross section reveals voids in the CIGS device where the wormlike defect exists. The damage done during the heating of the reverse-bias breakdown appears to generate voids in the upper part of the CIGS layer near the CIGS and transparent conducting oxide (TCO) interface. The voids lead to slightly lifted films in the vicinity of the wormlike defects, which gives them a raised texture when viewed overhead by the SEM or optical microscope. There are also Cu-rich regions at the propagation front of the thermal runaway damage. This provides evidence that the damage propagation process may proceed by movement of a molten CIGS front along weaknesses in the front and or back interface regions followed by re-solidification and formation of Cu-rich regions within the CIGS layer.

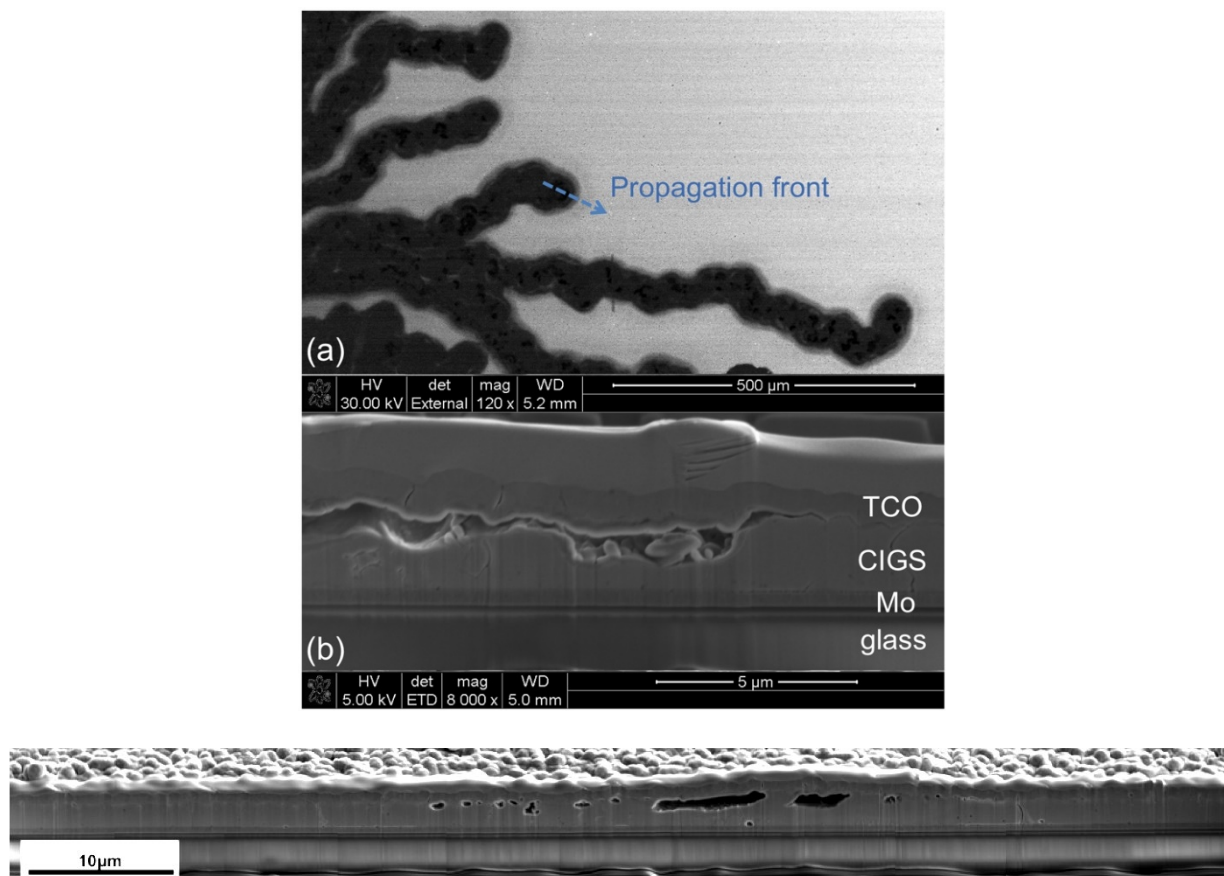

Figure 27. An EBIC image (a) from an SEM shows an overhead view of a wormlike defect, where dark areas correspond to poor current collection. An SEM image of FIB-prepared cross section at the propagating end of a wormlike defect (b) shows voids near the top of the CIGS layer. The bottom image shows a cross-sectional view perpendicularly across a wormlike defect.

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6.2 Pre-Breakdown Defect Detection Technique

To reproduce and further study the wormlike defects, thin-film module sections are stressed under reverse bias to simulate partial-shading conditions. Such stresses can cause permanent damage in the form of wormlike defects that is very comparable to outdoor defects. The mini-modules used in these experiments are either commercial-size modules that are cut into smaller sizes or small-scale modules produced with similar processes and architectures of the full-scale module. These samples from various sources have cells that are ~4 to 5 mm wide and ~80 to 100 mm long, and they are characterized by probing across two cells at a time. DLIT images are collected using a Cedip Silver 660M (FLIR SC5600-M) InSb camera with lock-in data acquisition. A Keithley source-meter has been used to apply a large reverse-bias voltage and to limit the current. The applied reverse-bias voltage exceeds a sample's breakdown threshold, and the current limit can prevent uncontrolled thermal-runaway damage that leads to wormlike defects or other permanent damage.

DLIT imaging shows spatially resolved heating when currents flow through the device in either forward or reverse bias. An example of uniform current and cell heating of a CIGS sample in forward bias is shown in Fig. 28(a). A current of about 15 mA/cm^2 is pulsed at 1 Hz in a square wave. Reverse bias is then applied to this series-connected pair of monolithic CIGS cells within the mini-module. Using a large upper-limit voltage, such as 10 V, with a current limit of about 0.3 mA/cm^2, reverse-bias DLIT indicates heating in localized defects as shown in Figs. 28(b) and 28(c). The zoomed-in view of Fig. 28(c) shows a pre-breakdown defect in the left center of the top cell, another directly below that defect in the middle of the bottom cell, and heating along the scribe lines.

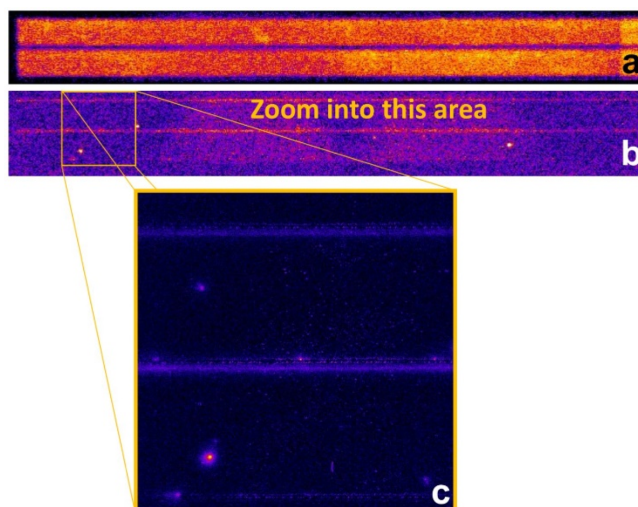

Figure 28. (a) DLIT imaging shows fairly uniform heating of two series-connected CIGS cells in forward bias. (b) With limited current, the reverse-bias DLIT image identifies possible breakdown sites. (c) Zooming in for higher spatial resolution shows the location of defects in their pre-breakdown state.

Using the zoomed-in field of view of Fig. 28(c), the thermal camera is then set to collect frames for a video, which is not using lock-in thermography. As current is increased in reverse bias, heating in the defects becomes strong enough for the camera to detect it without the need for the averaging and improved signal-to-noise ratio that lock-in acquisition provides. A selection of frames from the reverse-breakdown video are shown in Fig. 29. Frame 1 shows the defects

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beginning to heat more substantially as the current density is increased to 30 mA/cm^2 when considering the entire cell area. Because current is more concentrated at the defect locations, current density at the defects is significantly larger. Wormlike defects begin to form and propagate in seemingly random directions near the defect origin. After a few seconds, the propagation appears to stop, possibly because the shunted area is now larger and has reduced the current density and heating within the defects. The current limit is increased to roughly 60 mA/cm^2 (full cell area equivalent) and the wormlike defects begin to propagate again, as shown in Fig. 29, frames 2 and 3. At a high current density of ~150 mA/cm^2, breakdown continues to propagate for nearly a minute. As shown in Fig. 29, frames 4 through 13, some trails approach the scribe lines and tend to travel along the scribe lines, suggesting they can sometimes more easily propagate along those features. Some trails later break away from the scribe lines and either propagate within the field of the cell or once again return toward a scribe line. At this high current density, wormlike defects more sustainably continue to propagate and create damage. A final room-temperature thermal image shows the paths of the damage in Fig. 29, frame 14.

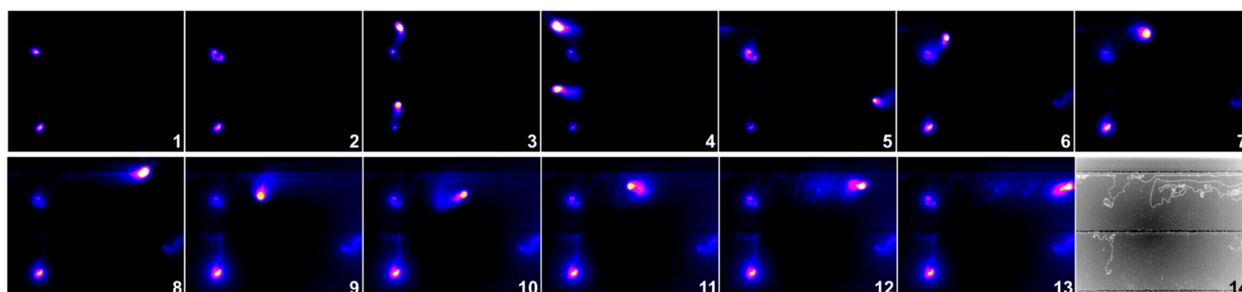

Figure 29. Selected frames from a thermal camera video show the propagation of wormlike defects during reverse-bias breakdown of the CIGS sample. Frame 1 shows heating at the defects when current density is limited to a low value (30 mA/cm^2). Frames 2 and 3 show how the defects begin to propagate when current density is increased to ~60 mA/cm^2. Frames 4 through 13 show how breakdown sustainably travels for roughly a minute within the cells and along scribe lines at a high current density of ~150 mA/cm^2. After stressing, the thermal camera captures the accumulated damage due to breakdown defect propagation as shown in frame 14.

The number of wormlike defects and amount of damage have led to some permanent shunting within these cells. A comparison of the before-stress and after-stress I-V plots are shown in the graphs of Fig. 30, where cells with different degrees of damage have been measured. After the current-limited reverse-bias, only minor changes are detected in the I-V curve, which would indicate that most defects have not been significantly damaged. After the reverse-bias stress and wormlike defect formation, the I-V curves indicate the cells have become significantly shunted.

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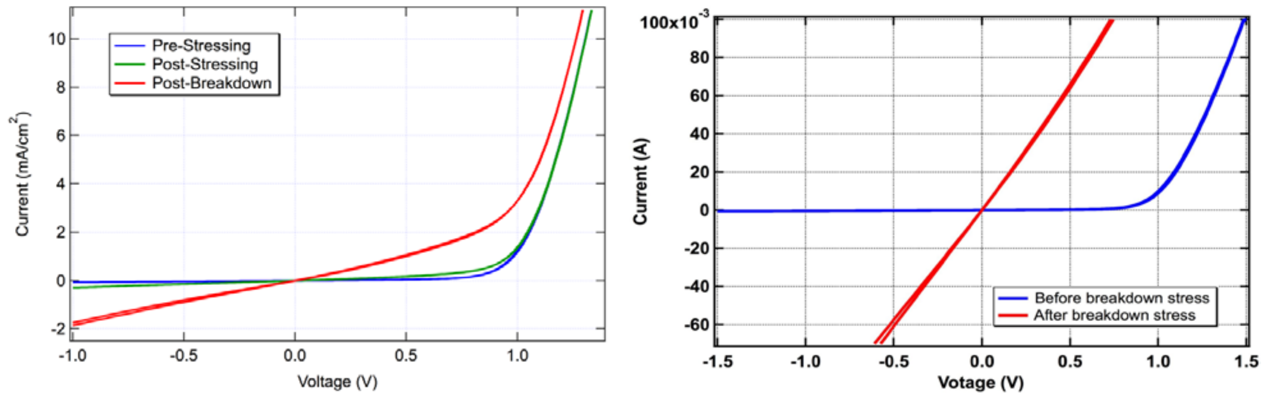

Figure 30. Left: I-V curves are collected for a pair of cells before testing, after current-limited reverse bias is applied, and after reverse-bias breakdown without current limitation. The post-stressing curve shows minimal damage after stressing with a current limit. Right: I-V curves collected before and after reverse-bias stressing are shown for the two series-connected CIGS cells. Reverse-bias breakdown has created permanent shunting within the device.

Figure 31 shows an example of breakdown occurring when measuring current as a function of applied reverse bias. Starting with forward bias, the voltage is reduced and then reverse bias is increasingly applied. As the reverse bias increases, breakdown begins, and the current quickly jumps to an increased (negative) value. Because the breakdown defect may burn itself out, the current may increase less quickly until another site begins to break down. Thus, the current jumps to different levels as breakdown at various sites in the sample initiates and propagates.

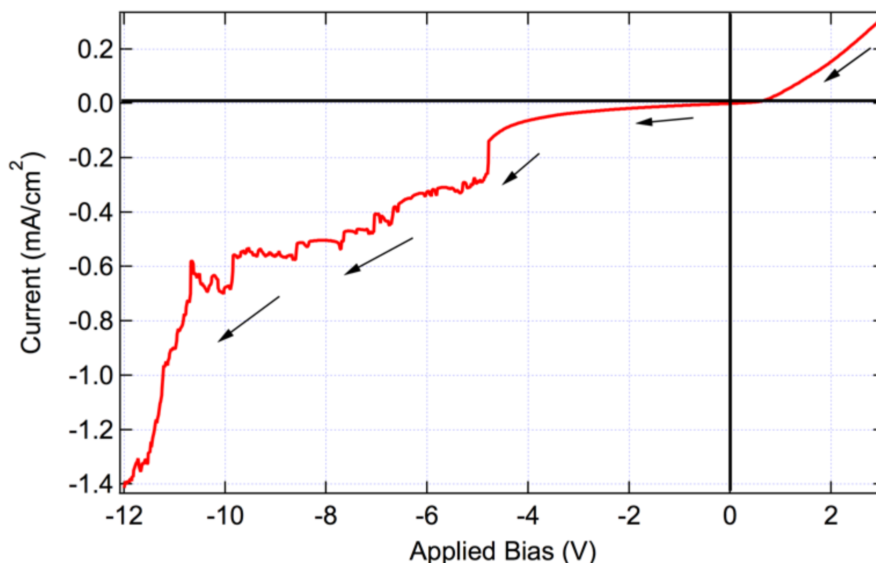

Figure 31. An I-V curve collected during stressing. The applied voltage begins in forward bias and progresses to increasing reverse bias. The graph shows jumps in reverse current as wormlike defects are formed and propagate.

We have applied our thermal-imaging technique with limited reverse-bias current to detect the defects in several kinds of CIGS samples [64]. We have also applied this technique to CdTe to predict early-breakdown defect locations and then track wormlike defect development as current

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is increased. We later show examples of the types of as-grown defects such as voids or pinholes in the absorber layer that instigate early breakdown and wormlike defect formation.

For applying this technique to a CdTe sample, two series-connected cells are imaged using significant reverse bias but with a current limit equivalent to 0.2 mA/cm^2 for the full cell area. A DLIT image is collected as before, and the potential breakdown sites detected using limited current are shown in red color in Fig. 32, frame 1. One defect appears near the center scribe lines on the left half of the image, while a second defect is within the lower cell on the right half of the image.

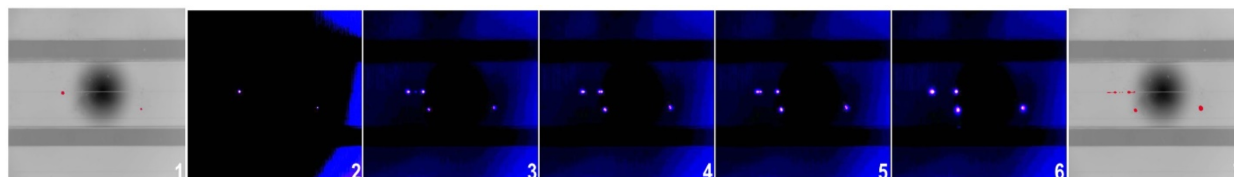

Figure 32. Selected frames from a thermal camera video show the propagation of defects during reverse-bias breakdown of the CdTe sample. Frame 1 shows the starting current-limited DLIT image in red overlaid on the gray-scale thermal image. The dark spot is due to reflection of the cold camera sensor. Frame 2 shows heating at the defects when current density is limited to a low value (40 mA/cm^2). Frame 3 shows how breakdown travels quickly along the scribe lines, and an additional defect becomes apparent when the current density is increased to ~100 mA/cm^2. Then, frames 4 through 6 show how the defect heating changes rather slowly for roughly a minute. After stressing, the thermal camera captures the accumulated damage due to breakdown defect propagation as shown in frame 7, where the DLIT image in red is overlaid on the gray-scale thermal image.

Using this zoomed-in view, the camera is set to collect video and capture the frames with applied reverse bias. With current densities of 20 and 40 mA/cm^2, the defects heat up but do not appear to propagate, as shown in Fig. 32, frame 2. As current is increased to 100 mA/cm^2, the scribe-line defect quickly propagates left and right along the scribe line as shown in Fig. 32, frame 3. A third defect appears within the lower cell on the left half of the sample below the scribe-line defect. Propagation of these defects does not significantly increase (Fig. 32, frames 4 through 6) because these defects tend to remain rather stationary over time (minutes) with the 100 mA/cm^2 current-density limit. A final DLIT image is collected, and the defect heating is shown in red color in Fig. 32, frame 7. The damage done by this reverse-bias stress has led to increased shunting as seen by the before-stress and after-stress I-V curves of Fig. 33.

By limiting current during applied reverse bias, potential early-breakdown sites can be identified before significant heating due to large current densities occurs. This allows for characterization of the types of defects that lead to localized breakdown and wormlike defects. The previous examples have shown that the identified defects became sources and initiation points of thermal damage and wormlike defects when current densities were increased. When only identifying defects with limited current, their structure in their as-grown condition can be preserved and studied to identify the types of defects that exist after cell manufacture.

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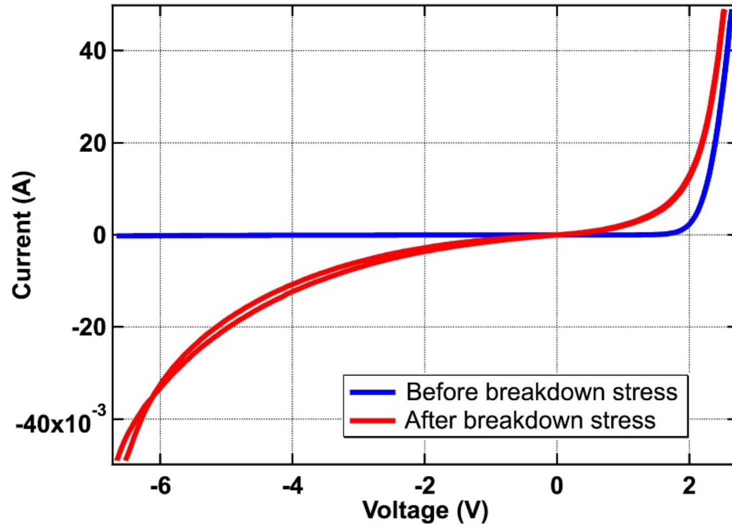

Figure 33. I-V curves collected before and after reverse-bias stressing are shown for the two series-connected CdTe cells. Reverse-bias breakdown has created permanent shunting within the device.

Applying sufficient breakdown voltage with limited current has allowed us to identify possible breakdown sites, but those sites can only be verified as breakdown sites if we allow current to freely flow and thermal-runaway processes to proceed. We collected statistics to determine the probability of a current-limited detected breakdown site actually forming a wormlike defect under full-current, reverse-bias conditions. We analyzed several modules by locating and counting regions of localized heating using limited current. We then allowed current to flow freely with reverse bias exceeding breakdown and again located and counted the wormlike defects formed. Table 1 summarizes the current-limited defects that were identified and predicted, along with how many of those defects initiated thermal runaway and formed wormlike defects. After breakdown, there were sometimes additional locations of wormlike defects that were not obviously seen using the current limit, and these defects were "not predicted." The statistics of Table 1 confirm that this method is useful for identifying potential breakdown defects, because more than 85% of the total number of breakdown sites were predicted by identifying localized heating locations when limiting current.

Table 1. Statistics summarizing predicted breakdown sites.

	Company 1			Company 2	
	Module 1	Module 2	Module 3	Module 1	Module 2
Predicted Breakdown	4	9	10	12	12
Correct Prediction	4	9	10	11	12
Not Predicted	0	1	2	4	0

With the statistical confidence that most current-limited detected defects become wormlike defects under reverse-bias breakdown, we have measured a pair of cells using only the current-limited condition. Using both forward bias and reverse bias, we have collected DLIT images when the current is limited to prevent thermal-runaway conditions. Figure 34 shows the DLIT images of the

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cells under forward bias (a) and reverse bias (b). The observed defects are numbered, where defects 1, 2, and 4 appear in both forward-bias and reverse-bias conditions. Defect 3 appears only in reverse bias. We then zoom into each defect using the thermal-imaging camera. We use a pulsed laser to mark with laser burn marks the location of the potential breakdown defect sites. The diameter of the laser burn marks is about 100 µm, and the burn marks are placed 0.5 mm above, below, and to the sides of the defect. The laser marks allow precise location of the defects in an SEM.

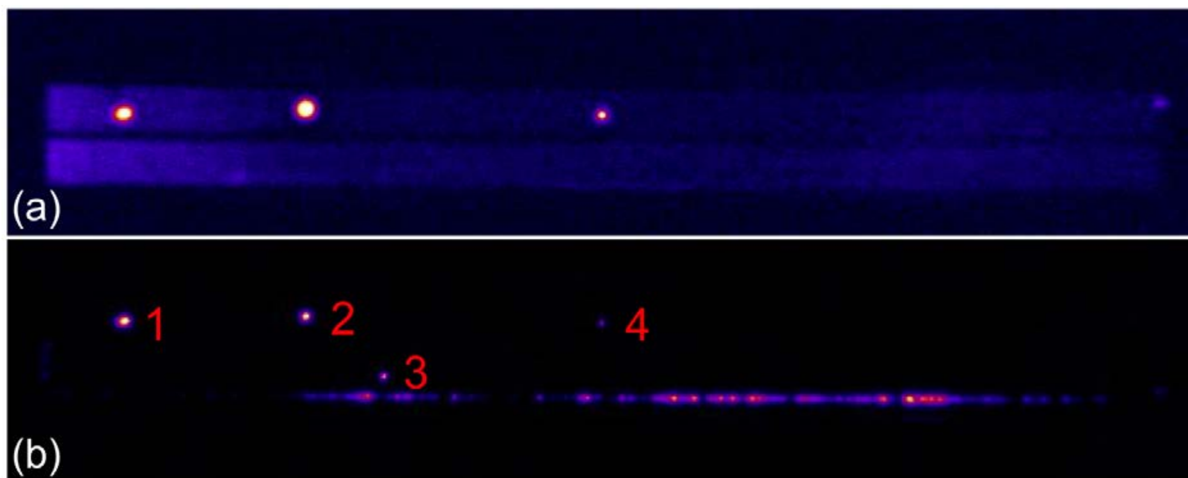

Figure 34. (a) DLIT images for a pair of cells show localized heating at defects in forward bias and (b) reverse bias. A current limit of 0.2 mA/cm^2 protects the defects from damaging breakdown conditions. Defects 1, 2, and 4 are observed in both forward and reverse bias, whereas defect 3 is only detected with reverse bias.

The defects identified as potential breakdown sites have been imaged in an SEM. The defects from Fig. 34 that appeared in both forward and reverse bias (defects 1, 2, and 4) appear to be pinholes or small craters in the CIGS absorber layer. Figure 35 shows an example SEM image of this kind of defect. Such defects have been observed in previous work [65], which showed a missing volume of CIGS material in the absorber layer, and that the TCO layer has contacted the sidewalls of the CIGS crater and possibly even the Mo substrate below.

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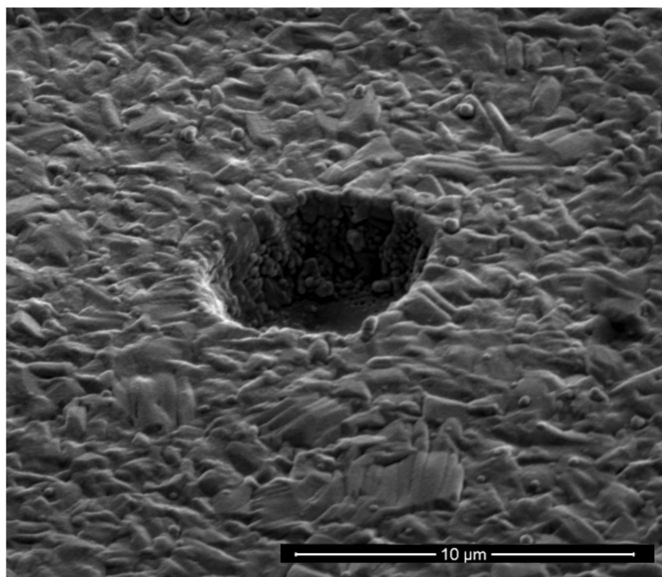

Figure 35. An SEM image of a crater or pinhole type of defect that is representative of defects 1, 2, and 4 of Fig. 6 that were observed in forward- and reverse-bias conditions.

The defect from Fig. 34 that appears only in reverse bias (defect 3) has also been examined in an SEM. Figure 36(a) shows the overhead SEM view where a bump or nodule is apparent from the top surface. To further investigate this type of defect, a FIB cross section was prepared and then analyzed using an SEM. The cross section of Fig. 36(b) shows voids or cracks in the CIGS layer in a "U" or bowl-shaped structure, where the bottom of the voids is near the bottom of the CIGS layer, or just above the Mo substrate surface. The rounded shape of the voids as seen in the FIB cross section suggests that the defect could potentially have become a crater and is perhaps a partial-crater defect. This type of defect has also been previously observed [65].

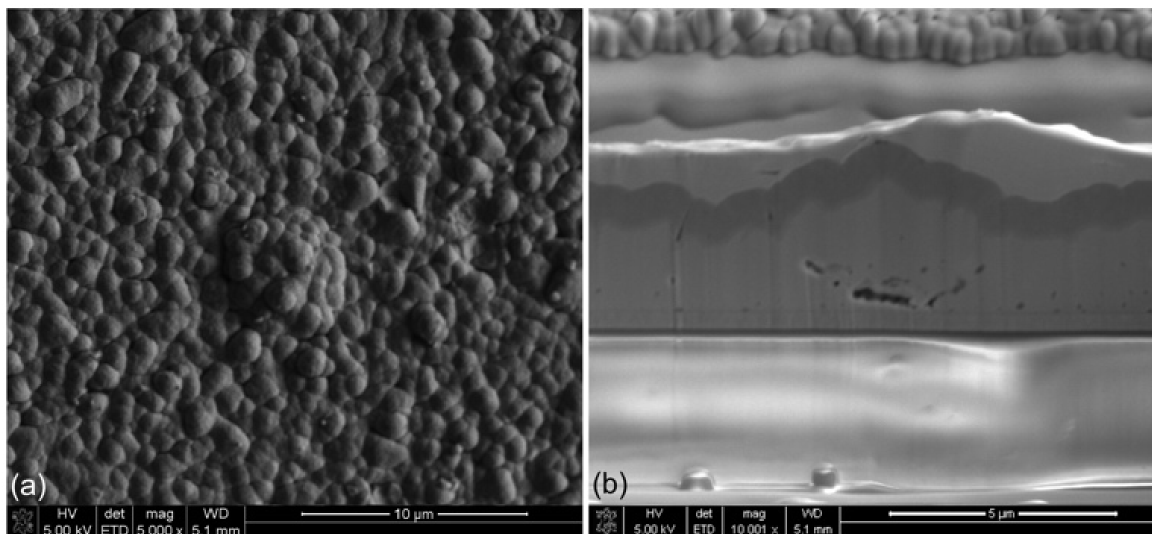

Figure 36. (a) An overhead SEM image of defect 3 of Fig. 34 that showed localized heating only with large reverse bias and limited current. (b) A FIB-prepared, cross-sectional SEM image of this nodule type of defect is shown.

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The crater type of defect has relatively larger void space that would allow for a lower resistance contact to be formed when TCO is deposited into the defect. This low resistance allows for significant current to flow through this type of defect, which results in substantial heating that becomes detectable even when forward current is flowing throughout the cell and generating background heating. The *nodule* type of defect has a smaller area where shunting could be generated by TCO deposition within the cracks in the film. This limited area would lead to a higher resistance type of shunt defect that would flow less current for a given applied voltage. For this reason, the defect may not substantially heat above the cell temperature during forward bias, and thus, it was not detected in Fig. 34(a). However, in reverse bias, current through the device is nominally very small before breakdown is reached. The defects, both craters and nodules, have lower resistance and conduct current to allow their detection by thermal imaging.

During processing, contamination may lead to particulates and pinholes affecting the uniformity of layer depositions and generate defects. The deposition method, such as sputtering or evaporation, and process conditions may also determine if such crater or nodule types of defects are formed during growth and processing. The schedule of preventive maintenance and equipment cleanliness may correspond to the density of these types of defects, and the measurement technique described here may be a potential tool to track correlations of breakdown susceptibility to processing conditions.

In Fig. 37, we show cross-sectional SEM images of additional early-breakdown sites in both CIGS and CdTe modules that we identified with current-limited DLIT and prepared with FIB milling. . The top image, Fig. 37(a), shows the cross-sectional view of a CIGS defect that had appeared as a small pit in the surface. This defect is about 10 μm in length. The cross section shows a nonuniform absorber-layer thickness where there is a void of material and different layers that are likely the top TCO material. This leads to poor device quality in the defect region and likely low device resistance due to the deposition of the top-contact material near or on the bottom contact layer. The bottom image, Fig. 37(b), shows a cross-sectional view of an early-breakdown defect in a CdTe sample. This image similarly shows voids and nonuniformities in the absorber-layer thickness, and the width of this defect is also roughly 10 μm. Together, these results suggest that similar hole/void defects may arise in both CIGS and CdTe devices under partial-shading conditions.

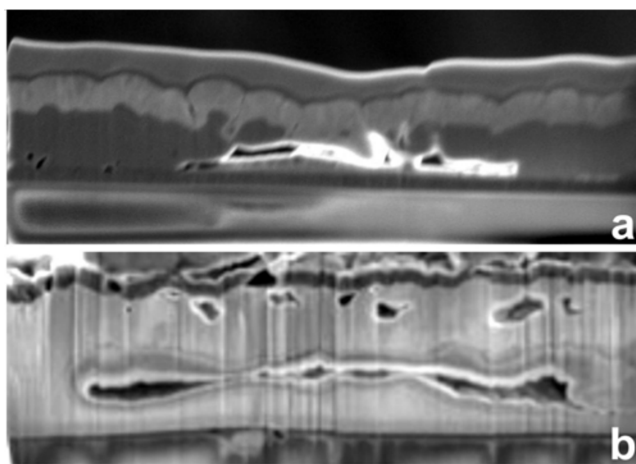

Figure 37. SEM cross-sectional views show ~10-μm size features associated with the initiation of reverse-bias breakdown. The hole/void type of defects are within the absorber layer of (a) CIGS and (b) CdTe.

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In summary, we studied degradation mechanisms due to partial shading on thin-film modules where reverse-bias early-breakdown defects cause localized heating and permanent damage. To investigate how these defects are initiated, reverse bias was applied while limiting the current to prevent thermal runaway. DLIT imaging was used to locate sites where heating shows that early breakdown will likely occur. Thermal imaging revealed that the identified defects were the initiating sites for early breakdown, and thermal video recorded the defect propagation. Defects such as film pinholes or voids appear to be weaknesses for reverse bias and may be origins for the formation of wormlike defects under conditions of partial shading.

6.3 Theory and Modeling of Shading-Induced Breakdown

The data present two categories of shunt-like defects that could be responsible for reverse-bias/shading-induced breakdown in CIGS cells and modules: 1) non-ohmic shunts, or weak diodes, with relatively low reverse breakdown voltage relative to the module average, and 2) ohmic shunts where nodules or voids have been observed. Type 1 shows up in forward-bias DLIT, whereas Type 2 shows up in both reverse- and forward-bias DLIT. In both cases, our modeling results show that thermal-runaway breakdown can occur under reverse bias at these sites. We find that type 2 defects tend to be more susceptible than Type 1 (e.g., runaway may occur at a lower reverse bias for Type 2). Also, because encapsulant materials can affect the thermal properties of the module, we found that runaway likely occurs sooner in encapsulated versus unencapsulated modules [66]. Figure 38(a) shows a simulated CIGS mini-module with non-ohmic shunts heating up prior to breakdown, where partial shading induces a negative bias across each shaded cell of -2.4V. Figure 38(b) shows the maximum module temperature with time and thermal-runaway events for encapsulated and unencapsulated cases.

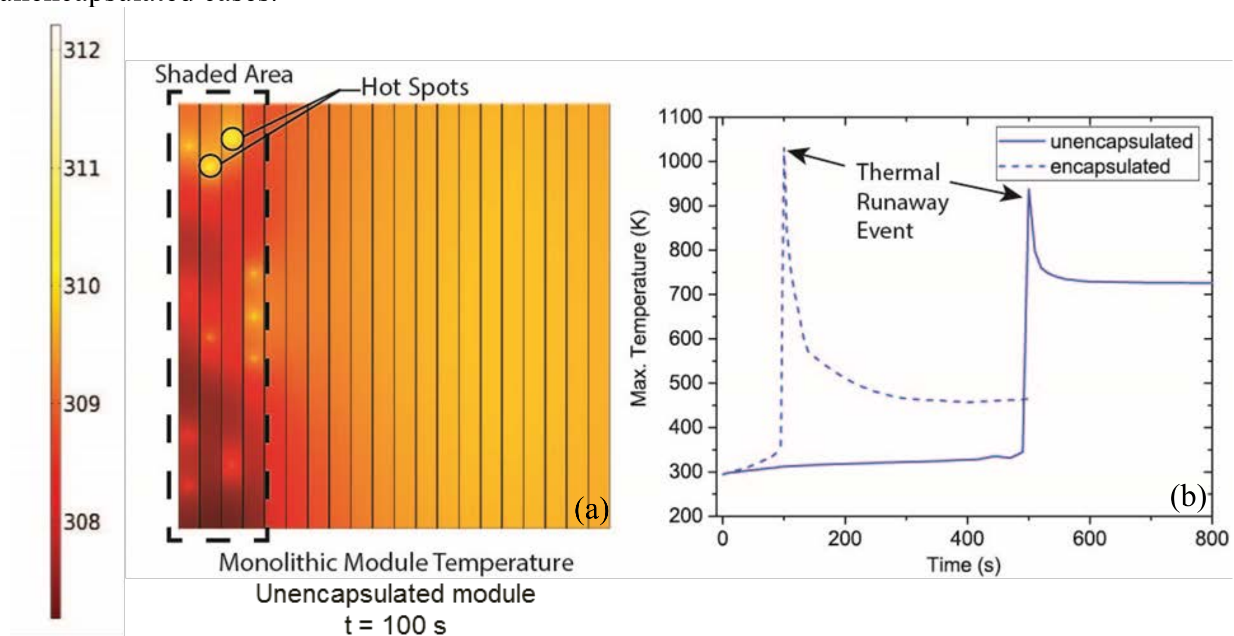

Figure 38. (a) Temperature distributions (in K) in a 20%-shaded, unencapsulated mini-module with non-ohmic shunts (hotspots in the shaded area) at 100 s after turning on the light source of 1,000 W/m² intensity at J_{sc} condition (before thermal runaway). Dashed box delineates shaded region. (b) Maximum temperature in the module over time showing the thermal-runaway event for encapsulated and unencapsulated modules.

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The general theory is based on coupled electro-thermal modeling of PV cells and modules. A complete description can be found in Ref. [66]. This approach enables prediction of current-voltage-temperature characteristics in the lab or field with various types of nonuniformities (e.g., light, bias, structural defects, electronic defects). Furthermore, it can be applied to monolithic thin-film modules and Si cells of arbitrary shape. An important result for the case of CIGS with shunt-like defects is that under reverse bias, the temperature of a shunt will increase, thereby increasing the current of nearby diodes—which causes further Joule heating until a thermal runaway initiates significant damage to the cell structure (see Fig. 38(b)).

In Fig. 39(a), we present the effect of ohmic shunting on a CIGS cell under various reverse-bias voltages. Thermal runaway occurs much more rapidly in this scenario compared to the non-ohmic shunted cells, even though an unencapsulated condition was considered. Peak temperatures reach almost 1,300 K. The melting temperature of $CuInGaSe_2$ ranges from 1,260 K to 1,340 K depending on the Ga content of the film [67]. Note that even without thermal runaway, ohmic shunts can cause heating and significant performance loss under normal operating conditions. Figure 39(b) shows the simulated current density-voltage (J-V) curves for a cell in an ambient temperature of T = 293 K, and 1-sun light. Shunt-induced heating of the cell causes significant V_{oc} loss [68].

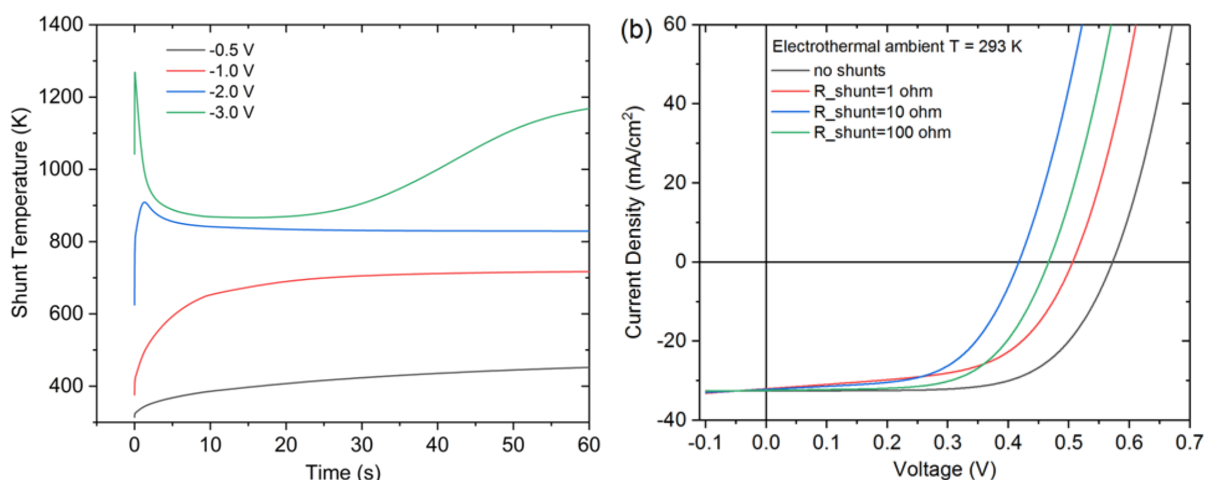

Figure 39. (a) Shunt temperature as a function of time for a CIGS cell under various reverse-bias voltages. Assumes dark condition, ambient T = 293 K, and a shunt resistance R_{shunt} = 10 Ω. (b) Light J-V curves for a cell with no shunt and one shunt with various resistances for field condition of 1-sun light intensity and ambient T = 293 K.

After thermal runaway, trails of damaged material are found to extend from the original bright spot identified by DLIT. Although the trails are visible to the naked eye, our optical and electron microscopy indicated that they are regions of negligible current collection that can cover an area of about 1 mm^2. For simplicity in the model, we considered a 1-mm-diameter circular region as an ohmic shunt with resistivities of ρ = 50, 500, and 5000 Ω cm to represent the worm-trail region, which are equivalent to large-area shunts of R_{shunt} = 1, 10, 100 Ω, respectively. Calculated field J-V curves shown in Fig. 40 indicate only slight differences for various shunt magnitudes because the Joule heating of the large-area shunt creates a small temperature increase in the cell under normal operating conditions. In this case, the decreases in V_{oc} are essentially due to the V_{oc} temperature coefficient, which we calculate to be -0.31%/K; that value is close to measured values near -0.30 to -0.32%/K [69].

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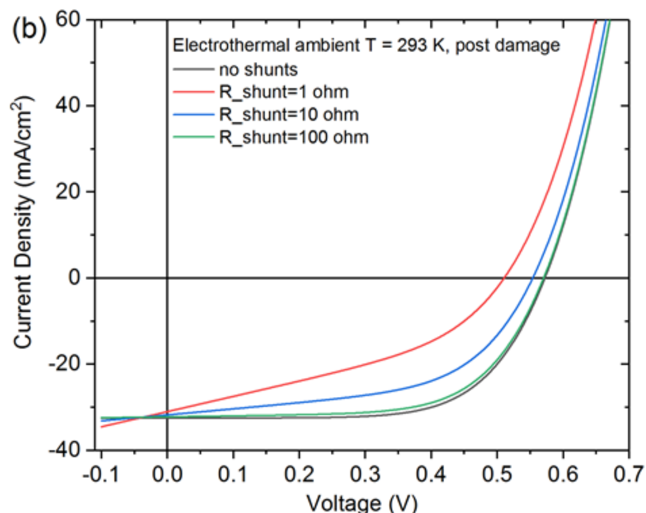

Figure 40. Light I-V curves for a cell with no shunt and one large-area shunt to represent the post-damage scenario. Various shunt resistances are shown for field conditions of 1-sun light intensity and T = 293 K.

In summary, we probed the structure, chemistry, and electronic properties of sites where thermal-runaway breakdown occurs under reverse-bias conditions in thin-film PV devices. The structure and chemistry of as-grown defects suggest that these features act as resistive heating elements when the devices are placed in a reverse-bias operating condition. Based on these observations, a device model was adapted to describe the electrical potentials, current densities, and thermal effects of localized resistive-heating elements within thin-film devices. We have shown that the experimentally observed inclusions and voids can result in significant local heating under reverse-bias conditions and initiate thermal-runaway breakdown in the devices. Furthermore, such defects can result in significant performance losses under normal operating conditions due to localized heating. As suggested in Ref. [64], the deposition method, contamination during processing, and substrate cleaning may play a significant role in mitigating the formation of as-grown inclusions and voids in thin-film PV devices. Although these features may be easily controlled on the laboratory scale, mitigation may present challenges at the industrial scale, where rapid production of large-area structures is required. Large-scale processing operations may experience material buildup during or after extended deposition processes. This can result in subtle nonuniformities in material deposition or sputtering of microscale particles during absorber growth resulting in formation of pits and voids. To reduce the frequency of such features, we suggest that thin-film PV producers track the relationship between susceptibility of devices and maintenance of deposition equipment.

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Appendix: List of SuNLaMP 30304 Publications

Journal Publications:

1. S.P. Harvey, J. Aguiar, P. Hacke, H. Guthrey, S. Johnston, M. Al-Jassim "**Sodium Accumulation at Potential-Induced Degradation Shunted Areas in Polycrystalline Silicon Modules,**" *IEEE J. Photovoltaics,* August 11, 2016.
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5. M. Nardone and S. Dahal, "**Anomalous Reverse Breakdown of CIGS Devices: Theory and Simulation**," *MRS Advances*, 2017, 1–6.
6. C. Xiao, C.-S. Jiang, S. Johnston, X. Yang, J. Ye, B. Gorman, and M. Al-Jassim, "**Development of *In-Situ* High-Voltage and High-Temperature Stressing Capability on Atomic Force Microscopy Platform,**" *Solar Energy*, **158**, 2017, 746–752.
7. H.R. Moutinho, S. Johnston, B. To, C.-S. Jiang, C. Xiao, P. Hacke, J. Moseley, J. Tynan, N.G. Dhere, and M.M. Al-Jassim, "**Development of Coring Procedures Applied to Si, CdTe, and CIGS Solar Panels,**" *Solar Energy*, **161**, 2018, 235–241.
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10. E. Palmiotti, S. Johnston, A. Gerber, H. Guthrey, A. Rockett, L. Mansfield, T. Silverman, and M. Al-Jassim, "**Identification and Analysis of Partial Shading Breakdown Sites in $CuIn_xGa_{(1-x)}Se_2$ Modules**" *Solar Energy*, **161**, 2018, 1–5.
11. S.P. Harvey, J. Moseley, A. Norman, A. Stokes, B. Gorman, P. Hacke, S. Johnston, M. Al-Jassim, "**Investigating PID Shunting in Polycrystalline Silicon Modules via Multiscale, Multitechnique Characterization**," *Prog. Photovolt. Res. Appl.,* 2018, 1–8.
12. S.P. Harvey, H. Guthrey, C.P. Muzzillo, G. Teeter, L. Mansfield, P. Hacke, S. Johnston, and M. Al-Jassim, **Investigating PID Shunting in Polycrystalline CIGS Devices via Multi-Scale, Multi-Technique Characterization**," IEEE PVSC WCPEC7, June 2018, submitted to *IEEE J. PV* (2018).

13. H. Guthrey, M. Nardone, S. Johnston, J. Liu, A. Norman, J. Moseley, and M. Al-Jassim, "**Characterization and Modeling of Reverse-Bias Breakdown in $Cu(In_{1-x}Ga_x)Se_2$ Photovoltaic Devices**," submitted to *Prog. Photovolt. Res. Appl.* (2018).

Conference Publications:

1. S. Johnston, M. Al-Jassim, P. Hacke, S.P. Harvey, C.-S. Jiang, A. Gerber, H. Guthrey, H. Moutinho, D. Albin, B. To, J. Tynan, J. Moseley, J. Aguiar, C. Xiao, J. Waddle, and M. Nardone. "**Module Degradation Mechanisms Studied by a Multi-Scale Approach**," IEEE PVSC, Portland, OR, 2016.
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